# Dual N-Channel Power MOSFET

20V, 6.0A, 30mΩ
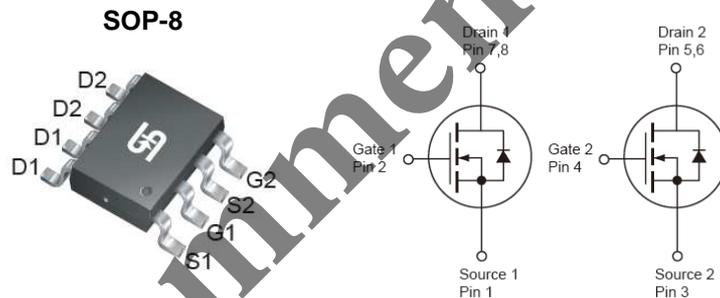
## FEATURES

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

## KEY PERFORMANCE PARAMETERS

| PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| $V_{DS}$ | | 20 | V |
| $R_{DS(on)}$ (max) | $V_{GS}$ = 4.5V | 30 | mΩ |
| | $V_{GS}$ = 2.5V | 40 | |
| $Q_g$ | | 4.86 | nC |

## APPLICATION

- Specially Designed for Li-on Battery Packs
- Battery Switch Application

**SOP-8**



**Notes:** Moisture sensitivity level: level 3. Per J-STD-020

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| PARAMETER | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±12 | V |
| Continuous Drain Current (Note 1) | $T_C$ = 25°C | $I_D$ | 6 | A |
| Pulsed Drain Current (Note 2) | | $I_{DM}$ | 30 | A |
| Continuous Source Current (Diode Conduction) | | $I_S$ | 1.7 | A |
| Total Power Dissipation | $T_A$ = 25°C | $P_{DTOT}$ | 1.6 | W |
| | $T_A$ = 75°C | | 1.1 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | - 55 to +150 | °C |

## THERMAL PERFORMANCE

| PARAMETER | SYMBOL | LIMIT | UNIT |
|---|---|---|---|
| Junction to Case Thermal Resistance | $R_{\Theta JC}$ | 40 | °C/W |
| Junction to Ambient Thermal Resistance | $R_{\Theta JA}$ | 77 | °C/W |

**Notes:** $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.

## ELECTRICAL SPECIFICATIONS ($T_A$ = 25°C unless otherwise noted)

| PARAMETER | CONDITIONS | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Static** [(Note 3)] | | | | | | |
| Drain-Source Breakdown Voltage | $V_{GS}$ = 0V, $I_D$ = 250µA | $BV_{DSS}$ | 20 | -- | -- | V |
| Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA | $V_{GS(TH)}$ | 0.6 | -- | -- | V |
| Gate Body Leakage | $V_{GS}$ = ±12V, $V_{DS}$ = 0V | $I_{GSS}$ | -- | -- | ±100 | nA |
| Zero Gate Voltage Drain Current | $V_{DS}$ = 20V, $V_{GS}$ = 0V | $I_{DSS}$ | -- | -- | 1 | µA |
| On-State Drain Current | $V_{DS}$ = 5V, $V_{GS}$ = 4.5V | $I_{D(ON)}$ | 30 | -- | -- | A |
| Drain-Source On-State Resistance | $V_{GS}$ = 4.5V, $I_D$ = 6.0A | $R_{DS(ON)}$ | -- | 21 | 30 | mΩ |
| | $V_{GS}$ = 2.5V, $I_D$ = 5.2A | | -- | 30 | 40 | |
| Forward Transconductance | $V_{DS}$ = 10V, $I_D$ = 6A | $g_{fs}$ | -- | 30 | -- | S |
| **Dynamic** [(Note 4)] | | | | | | |
| Total Gate Charge | $V_{DS}$ = 10V, $I_D$ = 6A, $V_{GS}$ = 4.5V | $Q_g$ | -- | 4.86 | -- | nC |
| Gate-Source Charge | | $Q_{gs}$ | -- | 0.92 | -- | |
| Gate-Drain Charge | | $Q_{gd}$ | -- | 1.4 | -- | |
| Input Capacitance | $V_{DS}$ = 8V, $V_{GS}$ = 0V, F = 1.0MHz | $C_{iss}$ | -- | 562 | -- | pF |
| Output Capacitance | | $C_{oss}$ | -- | 106 | -- | |
| Reverse Transfer Capacitance | | $C_{rss}$ | | 75 | | |
| **Switching** [(Note 5)] | | | | | | |
| Turn-On Delay Time | $V_{DD}$ = 10V, $R_{GEN}$ = 6Ω, $I_D$ = 1A, $V_{GS}$ = 4.5V, | $t_{d(on)}$ | -- | 8.1 | -- | ns |
| Turn-On Rise Time | | $t_r$ | -- | 9.95 | -- | |
| Turn-Off Delay Time | | $t_{d(off)}$ | -- | 21.85 | -- | |
| Turn-Off Fall Time | | $t_f$ | -- | 5.35 | -- | |
| **Source-Drain Diode** [(Note 3)] | | | | | | |
| Forward Voltage | $I_S$ = 1.7A, $V_{GS}$ = 0V | $V_{SD}$ | -- | 0.7 | 1.2 | V |

**Notes:**

1.  Pulse width limited by the Maximum junction temperature.
2.  Surface Mounted on FR4 Board, t ≤ 5 sec.
3.  Pulse test: PW ≤ 300µs, duty cycle ≤ 2%.
4.  For DESIGN AID ONLY, not subject to production testing.
5.  Switching time is essentially independent of operating temperature.

## ORDERING INFORMATION

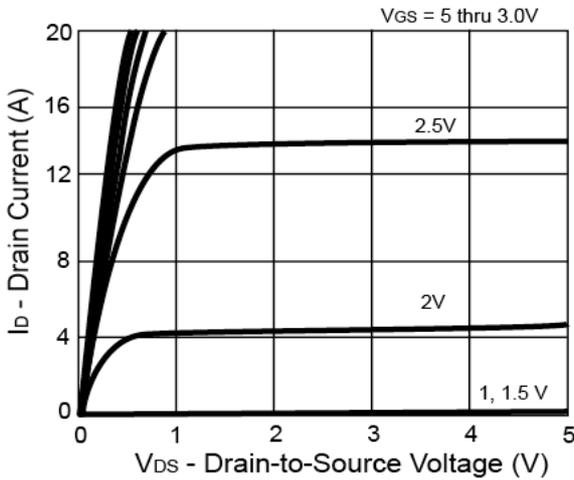| PART NO. | PACKAGE | PACKING |
|----------|---------|---------|
| TSM9926DCS RLG | SOP-8 | 2,500pcs / 13" Reel |

**Note:**

1.  Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC

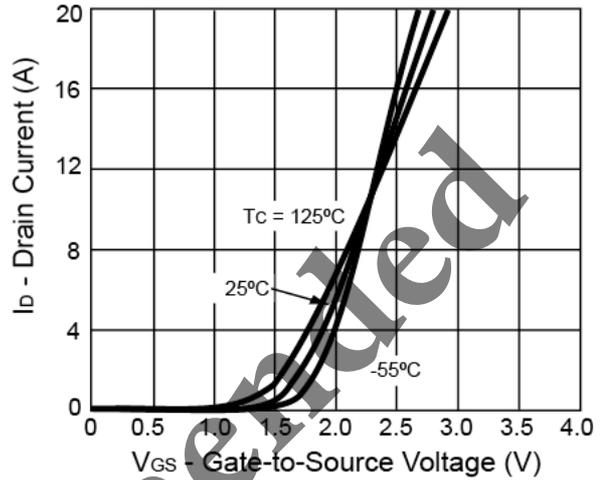2.  Halogen-free according to IEC 61249-2-21 definition

## CHARACTERISTICS CURVES
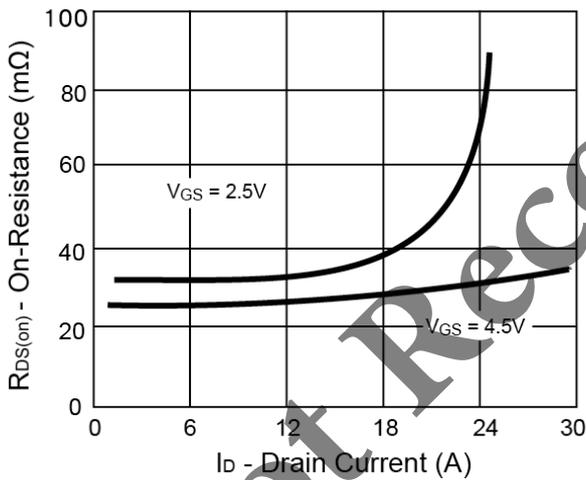
($T_A$ = 25°C unless otherwise noted)
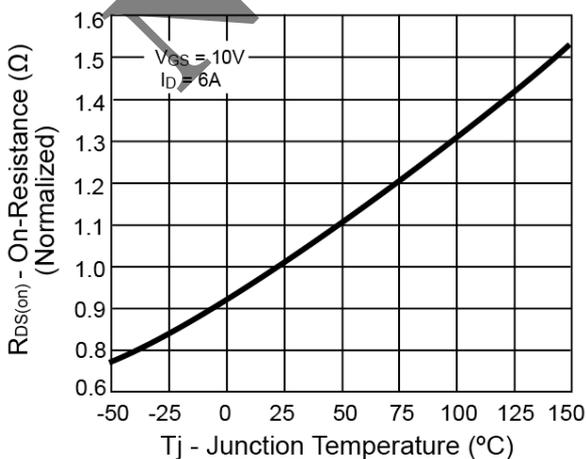
**Output Characteristics**



**Transfer Characteristics**



**On-Resistance vs. Drain Current**



**Gate Charge**
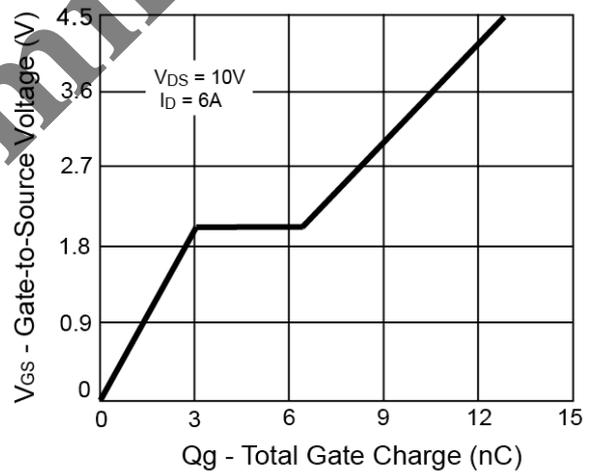


**On-Resistance vs. Junction Temperature**
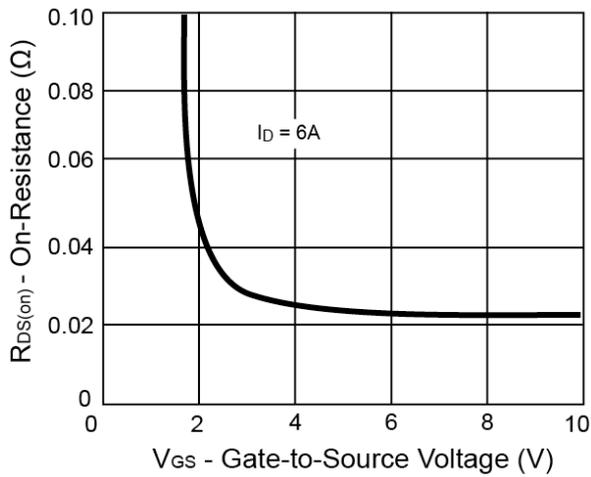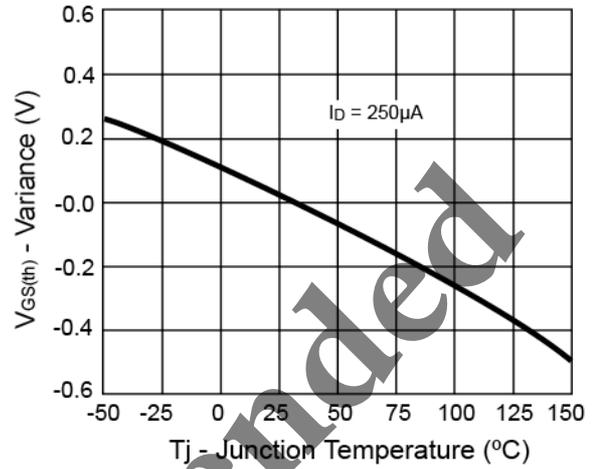


**Source-Drain Diode Forward Voltage**
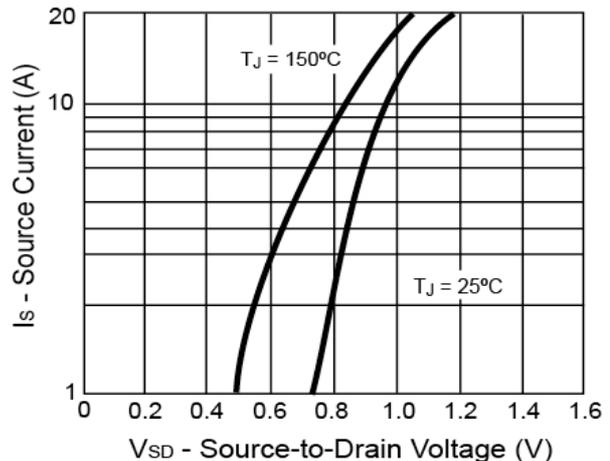
## CHARACTERISTICS CURVES
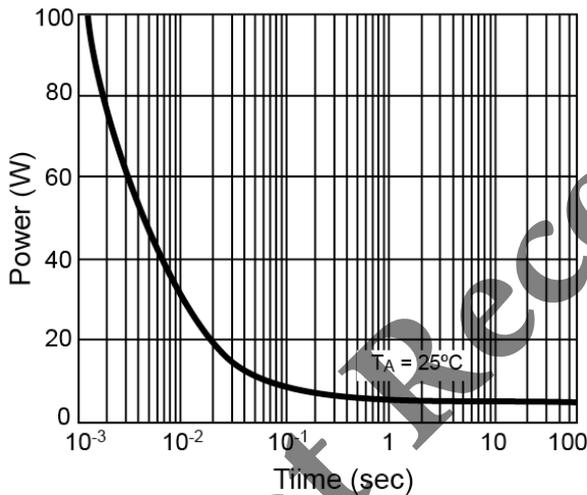
($T_A$ = 25°C unless otherwise noted)
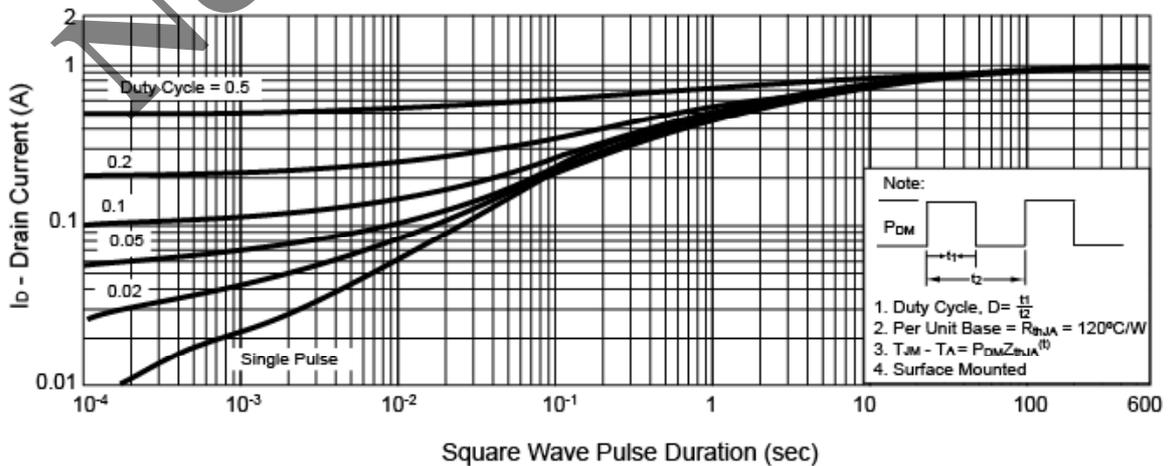
**On-Resistance vs. Gate-Source Voltage**



**Threshold Voltage**



**Single Pulse Power**



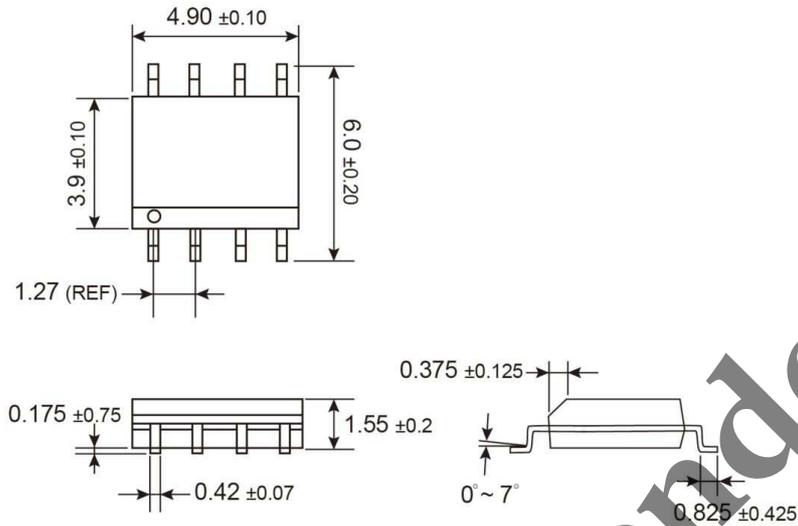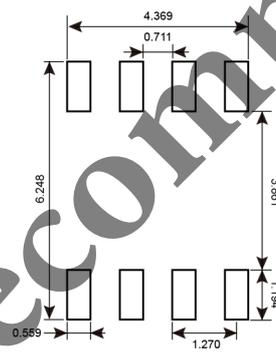**Normalized Thermal Transient Impedance, Junction-to-Ambient**



Note:

1. Duty Cycle, D= $\frac{t1}{t2}$
2. Per Unit Base = $R_{thJA}$ = 120°C/W
3. $T_{JM}$ - $T_A$= $P_{DM}Z_{thJA}^{(t)}$
4. Surface Mounted

## PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

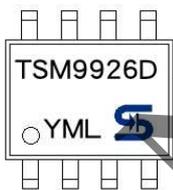**SOP-8**



## SUGGESTED PAD LAYOUT (Unit: Millimeters)



## MARKING DIAGRAM



**Y** = Year Code

**M** = Month Code for Halogen Free Product

| | | | |
|---|---|---|---|
| **O** =Jan | **P** =Feb | **Q** =Mar | **R** =Apr |
| **S** =May | **T** =Jun | **U** =Jul | **V** =Aug |
| **W** =Sep | **X** =Oct | **Y** =Nov | **Z** =Dec |

**L** = Lot Code (1~9, A~Z)

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