

### iJB Parallel Eval Board Operators Guide



This Guide shows you how to Get Started and use your IJB Parallel Evaluation System.

Please contact to TDK-Lambda if you have any questions or need further product details.

Note: The GUI software is provided on a CD-ROM and is also available at <u>http://www.us.tdk-lambda.com/lp/contacts/gui-</u> <u>download-page/.</u> If downloading from the web, registration is required.

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# **EVAL KIT CONTENTS**



#### Ordering Information

Code	Input Voltage	Output Voltage	Output Current	Note
iJBEB2	8.0-14.0V	0.6 – 2V	110A	Comes with two JB modules installed to allow parallel module evaluation



### About the iJB

### TDK·Lambda

#### 60A Non-isolated SMT Point of Load with PMBus

#### Features

- Only 1.0 in<sup>2</sup> Board Space
- PMBus Compliant (Read & Write)
- Surface Mountable
- Digital Adaptive Control
- Parallel Operation with Current Sharing
- Configurable Sequence & Fault Management

#### Key Market Segments & Applications



Vi: 8 – 14 VDC Vo: 0.6 to 3.3 Volts 100 Watts 35 Amps



**iJB** Series

# **STDK** Install GUI Interface Tool

The Smart Power Interface tool allows the user to configure and operate the iJB device via the PMBus. Install as shown.



\*Require Windows XP or later



A icon will appear on your desktop after install.

#### Please check latest version on our website

http://www.us.tdk-lambda.com/lp/contacts/gui-download-page/

# **ATDK** iJB Eval Board Installation

•System requirements

•Windows XP, Windows 7 (32bit or 64bit)

•Java

•Free USB port

•GUI installation

•Do not connect USB cable !

Install "SmartPower\_1.1\_20130926\_win32-setup.exe"

•Follow the instruction by the installer

•Close GUI

•Evaluation board set-up

•Apply 12V source to the Vin terminal (see picture 1)

•Connect USB cable to board and PC

•Driver will be installed



**Connect the Power** 





### **Get Connected**



1) Connect USB from computer to Dongle Input



# Run the GUI

Launch the Single mod	GUI e Screen:			Configure Tab Shows Default Basic Configuration Settings
<ul> <li>Single Mode</li> <li>System Mode</li> <li>PV3012 [0000:10]</li> <li>PV3012 [0000:11]</li> </ul>	General Configure Store Demo Basic Fault Configuration Vour Trim: Vour Max:	0.000 × V 1.600 × V	0.000 V 1.600 V	Controls Output voltage Trim values, allowable maximum output voltages and scaling selection (internal or external).
Status A BUSY OFF OFF	Vou⊤ Scale Loop:     Internal Rdiv On/Off       Vou⊤ Tracking: <ul> <li>Off</li> <li>50%</li> </ul> Slew Rate:           ON Rise Time:	1.0000 ★ 0 100% 1.042 ★ mV/µs 2.9 ★ ms	1.0000 OFF 1.042 mV/µs 2.9 ms	Controls Ratiometric output voltages for non parallel operation.
Faults	ON Time Delay: OFF Time Delay:	2.0 💌 ms	2.0 ms	Controls Output voltage timing on power up and power down.
Output LOS Output LOS Output UV (Warning) Output OCP SCP	Lower Voltage Margin: On/Off Configuration Requires OPERATION ON: O Yes	-5.0 🖈 %	0.950 V	Sets incremental voltage
OTP OT (Warning) UTP UT (Warning) Invalid Data	Requires CTRL Pin Asserted: <ul> <li>Yes</li> <li>CTRL Pin Polarity:</li> <li>Active High</li> <li>CTRL Pin Off Action:</li> <li>Immediate Of</li> </ul>	<ul> <li>No</li> <li>Active Low</li> <li>Turn Off Delay</li> </ul>	YES HIGH DELAY	Establishes on/off hardware
CML Fault	Power Stage Calibrated Current Sense Element (@ 25°C):	0.770 <u>*</u> mΩ	0.770 mΩ	control features.

# **STDK** About the Internal Voltage Divider

General Configure Store Demo		
Basic Fault		
Configuration		<b>▲</b>
Vour Trim:	0.000 ≑ V	0.000 V
Vout Max:	1.600 🌩 V	1.600 V
VOUT Scale Loop: Internal Rdiv On/Off	1.0000 🜩	1.0000

- The Power Modules feature an internal voltage divider which can be disabled to enhance voltage setpoint accuracy when no attenuation is required. (output voltage 1.500 volts or lower). During startup the module will turn the divider on or off depending on the VOUT\_OV\_FAULT\_LIMIT that was determined based on Rset value. With voltage attenuation off, VOUT\_MAX = 1.6 V. With voltage attenuation on, VOUT\_MAX = 3.5 V.
- If you want to change to higher voltage then you must turn voltage divider on (select 0.2857). This will happen automatically if resistor on Vset pin is changed so generally a user does not need to worry about this item, but in case of EV-kit they may need to turn on or off.



Run the GUI (cont.)





# Run the GUI (cont.)

Connect the Converters • Use the GUI Schematic Capture feature to connect the two System Mode onboard converters for parallel operation Single Mo System System Mode System Components ^ POL 0 0000:10 PV3012 D Master Add Power Src Add Power Out PV3012 [0000:11] 0.00 A Save Load Graph Scale 25% 50% 75%100% 150% 200% Status -Device Configuration BUSY ^ 0000:11 POL 1 OFF Vour Setting: 1.000 🔷 V 0 Vir. 13.500 Slave Power Good ۲ 0.00 A Faults -Input OVLO 0 Operation On/Off: OPERATION Input UVLO 0 OPERATION ON not required to turn unit on Output OVP 0 Power Good: Output LOS None 
 Low Margining: High Output UV (Warning) Output OCP Digital Stress Share: ( On ○ Off SCP Disable 👻 DSS Auto-Zero: OTP OT (Warning) 0 Sync Selection: Master 👻 UTP 0 UT (Warning) 0 Slave Phase Shift: 0 - 0 Invalid Data 0 **Device Properties** -CML Fault POL 0 Name: Clear Faults Color: PMBus Address: 0000:10 -V Monitoring On/Off: Description Line 1: Description Line 2:

#### Run the GUI (cont.) **公TDK** Connect the Converters • **Click Add Power** . Use the GUI Schematic Capture feature to connect the Source Click Add Power Out two onboard converters for parallel operation Single Mode System System Mode System Components VIN: POL 0 0000:10 15-PV3012 [0000:10] O Vin II 🕀 🖯 Add Power Src Add Power Out PV3012 [0000:11] 13.533 V Power in0 10-Power out0 Save Load 5 Graph Scale 01 07:40 07:50 25% 50% 75%100% 150% 200% ۰ III Status Þ. $\sim$ Device Configuration BUSY POL 1 0000:11 OFF 0 Slave Vour Setting: 1.000 ÷ V Vin Power Good 13.499 V +5.0 Faults $\wedge$ Input OVLO +4.0Operation On/Off: OPERATION Input UVLO Power Good: Output Voltage Output OVP Margining: None Low High Output LOS Output UV (Warning) Digital Stress Share: (i) On OOff Output OCP DSS Auto-Zero: Disable 👻 SCP 2.0 OTP Sync Selection: Master 👻 OT (Warning) 0 - 0 Slave Phase Shift: UTP UT (Warning) **Device Properties** -Invalid Data CML Fault Name: Time Clear Faults Color: POL Vout ... ON Delay (... ON PMBus Address: -P.... 1.000 2.0 Monitoring On/Off: P.... 1.000 2.0 Description Line 1: Description Line 2: • III .

# Run the GUI (cont.)



Power in0 Block as shown.

connect POL0 and POL1 Vout connections to the Power out0 Block as shown.

Remaining Connections are made automatically!

**公TDK** 

# **Establish Fault Limits**

Selects which of the two modules the settings apply to.

Single Mode	General Configure Store Demo       O Single Mode				General Configure Store Demo				
🔿 Syrtem Mode	Basic Fault			System Mode		Basic Fault			
PV3012 [0000:10]	Fault Limits			PV3012 [0000:10]		Fault Limits			
• PV3012 [0000:11]	Input OVLO Limit:	15.00 🌩 V	15.00 V	(0) PV5012 [0000.11]		Input OVLO Limit:	15.00 🜩 V	15.00 V	
	Input UVLO Turn-On Threshold:	7.60 🔷 V	7.60 V			Input UVLO Turn-On Threshold:	7.60 🔷 V	7.60 V	
	Input UVLO Turn-Off Threshold:	7.00 🗢 V	7.00 V			Input UVLO Turn-Off Threshold:	7.00 🔷 V	7.00 V	
Status 🔺				Status -		Output OVD Limits	1.500 AV	1.520.14	
BUSY 🥥	Output OVP Limit:	1.520 V	1.520 V	BUSY (		Output OVP Limit:	1.520 V	1.520 V	
OFF 🧿	Output OVP Response Delay:	39.99 ≑ µs	39.99 µs	OFF (	•	Output OVP Response Delay:	39.99 ≑ µs	39.99 µs	
Power Good 🥥	Output OVP Retry/Latch:	Retry 👻	Retry	Power Good (	•	Output OVP Retry/Latch:	Retry 👻	Retry	
Faults 🔺	Output OCP Limit:	50 🚔 A	50 A	Faults		Output OCP Limit:	50 🜩 A	50 A	
Input OVLO	Output OCP Response Delay:	1500.0 🌩 µs	1500.0 µs	Input OVLO	211	Output OCP Response Delay:	1500.0 🌩 µs	1500.0 µs	
Output OVP	Output OCP Retry/Latch:	Retry 👻	Retry	Output OVP (	0	Output OCP Retry/Latch:	Retry 👻	Retry	
Output LOS	Output OCP Retry Delay:	500 🌩 ms	500 ms	Output LOS (		Output OCP Retry Delay:	500 🔷 ms	500 ms	
Output UV (Warning)	OTP Limit:	125 🛋 🖤	125 %	Output OCP	ŏII	OTP Limit:	125 € ℃	125 °C	
SCP 🔘				SCP (	•	ITO Limite		40.90	
OTP	UTP Limit:	-40 🖵 °C	-40 °C	OTP (	●   l	OTP LIMIC		-40 -0	
OT (Warning)	Warning Limits			OT (Warning) (	21	Warning Limits		<b>A</b>	
UT (Warning)	Output UV Limit:	0.801 🜩 V	0.801 V	UT (Warning)	ŏ	Output UV Limit:	0.801 🜩 V	0.801 V	
Invalid Data 🔘				Invalid Data	9	07.1 - h		105.05	
CML Fault 🔘	OT Limit:	125 🔷 ℃	125 °C	CML Fault (	•	OT Limit:	125 🖵 °C	125 °C	
Clear Faults	UT Limit:	-40 🚔 ℃	-40 °C	Clear Faults		UT Limit:	-40 ≑ ℃	-40 °C	

Since both modules are connected in parallel, all values for each of the converters must be the same for uniform operation.

- Set Output OVP to 1.52 Volts for both converters
- Set Output OCP to 50 Amps for both converters



### **The Store Tab**

Default Settings			_		
Default Settings					
Derault Settings		-			_
Storage Space Usage: 21	.% S	tore Pestore		Lrast	
Customer info	_	_		Digital Stress Share	
Customer Name:	TDK		(21)	Digital Stress Share:	Off 🚽
Product ID:	Digital POL N	Iodule	(4)	DSS Auto-Zero:	Disable -
A Customer name and product ID field	is can not be empty			DSS Vout Correction Range:	100 + mV
Vout ~ Margins				DSS Bandwidth:	10 -
Vout Setting:		1.500 🚔	V	Nominal Current Sense Element (@ 25%);	0.28 mo
Vout Trim:		0.000 🜲	V	Fault Limits	0,20 + 1132
Vout Max:		1.600 🚖	v	Input OVLO Limit:	15.00 AV
Vour Scale Loop:		1.0000 🜩	1	Input I M O Turn-On Threshold	7.60 Å V
Vout Tracking:		Off 👻	]	Input UVLO Turn-Off Threshold:	6.80 🗘 V
Slew Rate:		1.042 🌩	mV/µs	Output OVP Limit.	1.600 AV
ON Rise Time:		2.9 ≑	ms	Output OVP Delay:	40 1 us
ON Time Delay:		2.0 🚔	ms	Output OVP Retry/Latch:	Retry -
OFF Time Delay:		0.0 ≑	ms	Output OCP Limit:	118 🗢 A
Upper Voltage Margin:		10.0 🜲	%	Output OCP Delay:	300.0 🜩 µs
Lower Voltage Margin:		-10.0 🚖	%	Output OCP Retry/Latch:	Retry -
Current Sense ~ Power ~ Margi	ining			Output OCP Retry Period:	500 🚔 ms
Calibrated Current Sense Element (@	25°C):	0.277	mΩ	OTP Fault Limit:	135 4 90
Operation On/Off:		On 👻	]		
CONTROL Pin Asserted required t	to turn unit on			UIP Fault Limit:	-40 - UC
Margining:		None 👻	]	warning Limits	0.001
On/Off Configuration				Output OV Warning Limit:	0.801 V
Requires OPERATION ON:		Yes 👻	]	OTP Warning Limit:	135 ♀ ℃
Requires CTRL Pin Asserted:		Yes 👻	]	UTP Warning Limit:	-40 ≑ °C
CTRL Pin Polarity:		Active Low 👻		Dynamic phase dropping only applies to dual	phase mode
CTRL Pin Off Action:		Turn Off Delay 👻	1	Programmable Power Good	
Control loop				Programmable Power Good:	12 - %
Optimization Factor (Dynamic):	9	Lowest Transient 👻	1	PMBus Address	

The NVM capacity on the ijX devices is limited; using the Store function is not advised.

Values can be changed in working memory without using the "store" command. Turn ENABLE switch on eval board "ON".



### **Exercise the Modules**



# **Exercise the Module (cont.)**

Change the output voltage to 1.5 Volts:



# **CONVENIENT Test Points**

i<sup>2</sup>C Test Points :

- TP 24: i<sup>2</sup>C Bus Signal Ground
- TP 23: i<sup>2</sup>C Bus Signal Alert
- TP 21: i<sup>2</sup>C Bus Signal Data
- TP 22: i<sup>2</sup>C Bus Signal Clock





- iJB Parallel Eval Board Simplified Schematic
- Simplified Layout

# **Simplified Schematic**



# **Simplified Layout**

SIMPLIFIED LAYOUT – showing vias & placement of suggested ceramic filter capacitors near power module



REF DESIGNATOR	VALUE, SIZE, RATING	PART NUMBER	SUPPLIER
COUTPUT – 12 pieces	100uF, 1206, 6.3V	C3216X5R0J107MT	TDK
Note 10 additional output of	apacitors of same type (C40	1-C410) are populated furthe	r away from power module
CINPUT – 10 pieces	22uF, 1206, 16V	C3216X5R1C226MT	TDK

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 PROPOWER-3.3V

 MYGTM01210BZN
 40C24-N250-I5-H
 40A24-P30-E
 3V12-P0.8
 10C24-N250-I10-AQ-DA
 4AA24-P20-M-H
 3V12-N0.8
 3V24-P1
 3V24 

 N1
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 BMR4652010/001
 6AA24-P30-I5-M
 6AA24-N30-I5-M
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 R-7212P
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 10C24-P125
 10C24-P250-I5
 6A24-P20-I10-F-M-25PPM
 1A24-P30-F-M-C
 TSR 1-24150SM
 1/2AA24-N30-I10
 1C24 

 N125
 12C24-N250
 V7806-1500
 PTV12020LAH
 PTV05010WAH
 PTN04050CAZT
 PTH12020WAD
 PTH12020LAS
 PTH05050YAH

 PTH05T210WAH
 PT
 PT