

N-Channel Enhancement Mode MOSFET

TDM31058A

DESCRIPTION

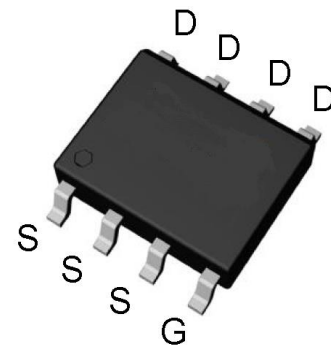
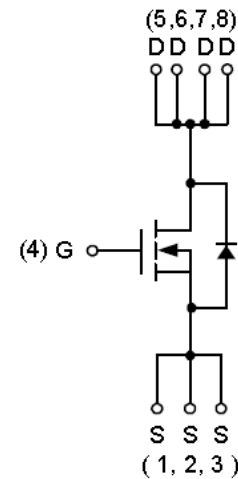
The TDM31058A uses advanced trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications.

GENERAL FEATURES

- RDS(ON) < 16mΩ @ VGS=10V
RDS(ON) < 22.5mΩ @ VGS=4.5V
- Extremely low switching loss
- Excellent stability and uniformity
- Lead free product is available
- SOP-8 Package

Application

- High Frequency Switching
- Synchronous Rectification



Top View of SOP-8

ABSOLUTE MAXIMUM RATINGS(Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	+20	V
Drain Current @ Continuous (Note 1)	I _D (T _c =25°C)	40	A
	I _D (T _c =100°C)	27	A
Pulsed Drain Current (Note 2)	I _{DM}	160	A
Maximum Power Dissipation (Note 3)	P _D (T _c =25°C)	50	W
Thermal Resistance, Junction-to-Ambient (Note 4, Note 5)	R _{θJA}	35	°C/W
Avalanche Current, Single pulse (Note 2, Note 6)	I _{AS} (L=0.5mH)	6	A
Avalanche Energy, Single pulse (Note 2, Note 6)	E _{AS} (L=0.5mH)	32	mJ
Maximum Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55 To 150	°C

ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.8	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	14.3	16	m Ω
	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=10A$	-	18.8	22.5	m Ω
Gate Resistance	R_G	$V_{DS}=0V, V_{GS}=0V, F=1.0MHz$	-	1.5	-	Ω
DYNAMIC CHARACTERISTICS (Note7)						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V, F=1.0MHz$	-	1130	-	PF
Output Capacitance	C_{oss}		-	496	-	PF
Reverse Transfer Capacitance	C_{rss}		-	60	-	PF
SWITCHING CHARACTERISTICS (Note 7)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DS}=50V, V_{GS}=10V, R_G=3.3\Omega, I_D=40A$	-	46	-	nS
Turn-on Rise Time	t_r		-	55	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	249	-	nS
Turn-Off Fall Time	t_f		-	105	-	nS
Total Gate Charge	Q_g	$V_{DS}=50V, I_D=40A, V_{GS}=10V$	-	30	-	nC
Gate-Source Charge	Q_{gs}		-	6	-	nC
Gate-Drain Charge	Q_{gd}		-	8.2	-	nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Continuous Source Current	I_S		-	40	-	A
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=20A$	-	0.8	1.0	V
Reverse Recovery Time	T_{rr}	$I_F=20A, di/dt=100A/\mu s$	-	70	-	nS
Reverse Recovery Charge	Q_{rr}		-	224	-	nC

NOTES:

- The maximum current rating is package limited.
- Single pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.
- The power dissipation PD is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- The value of $R_{\theta JC}$ is measured in a still air environment with $T_A=25^\circ\text{C}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.
- The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
- The EAS data shows Max. rating. The test condition is $V_{DS}=50V, V_{GS}=10V, L=0.5mH$
- Guaranteed by design, not subject to production testing

Typical Operating Characteristics

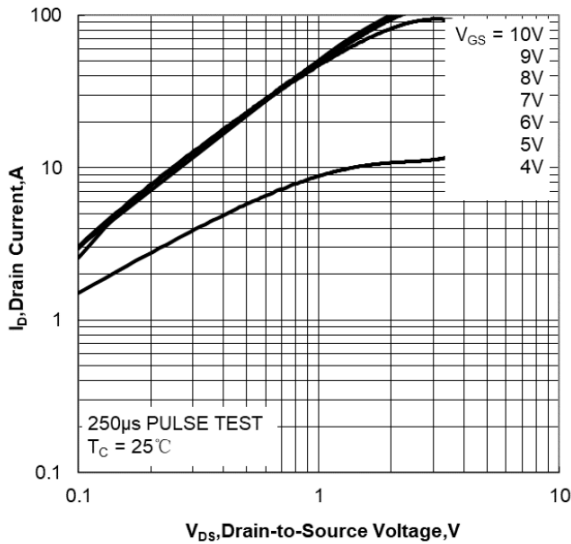


Figure 1. Output Characteristics

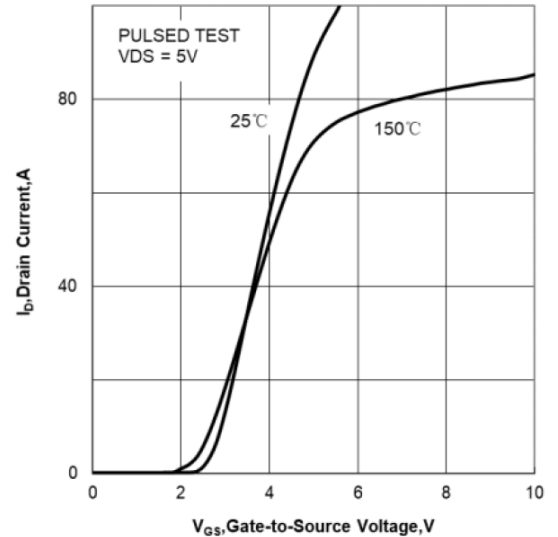


Figure 2. Transfer Characteristics

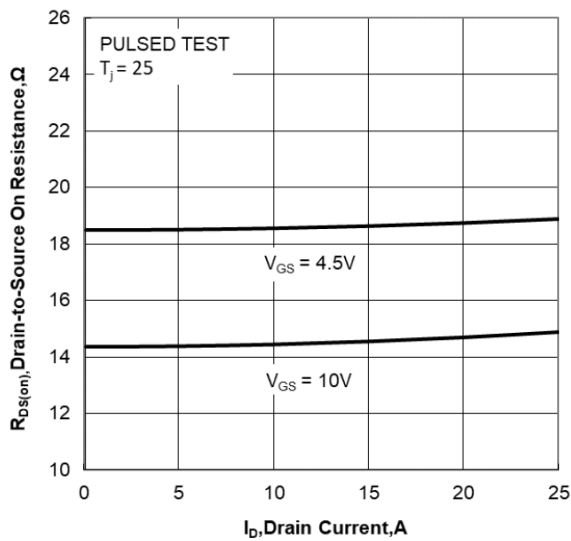


Figure 3. Drain-to-Source On Resistance vs Drain Current

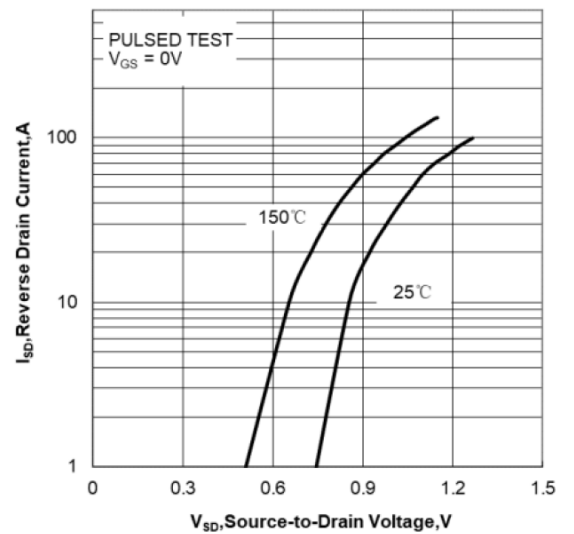


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

Typical Operating Characteristics (Cont.)

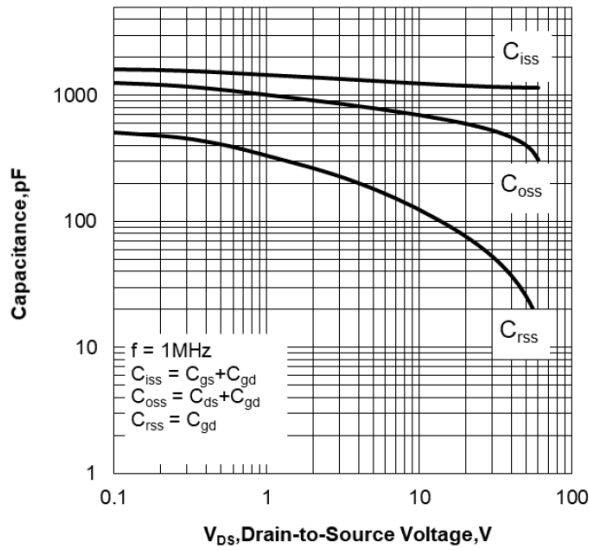


Figure 5. Capacitance Characteristics

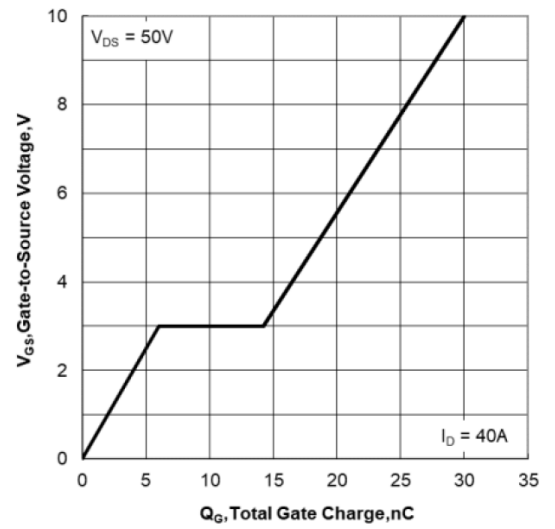


Figure 6. Gate Charge Characteristics

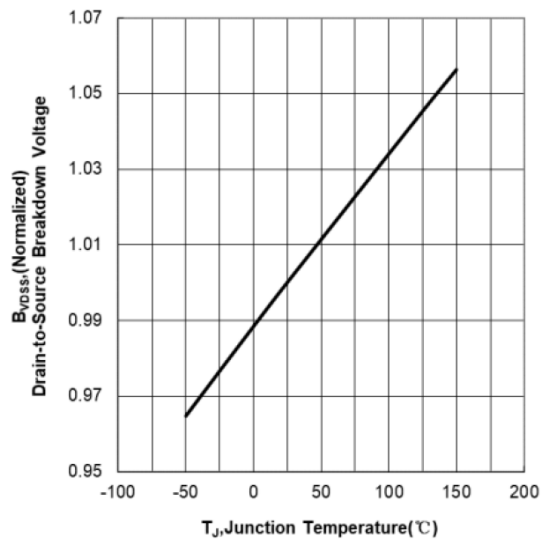


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

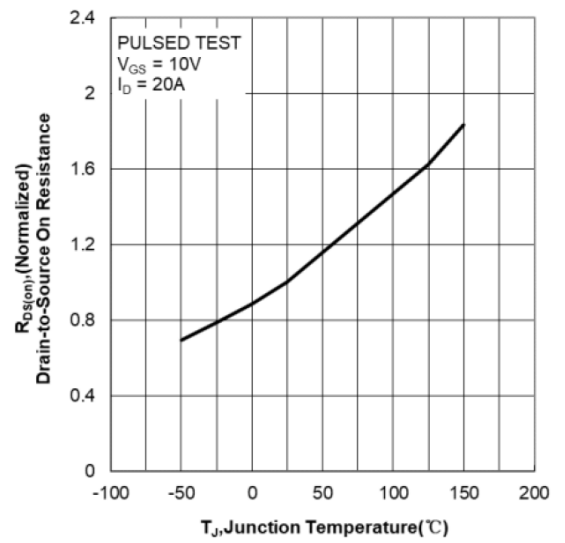


Figure 8. Normalized On Resistance vs Junction Temperature

Typical Operating Characteristics (Cont.)

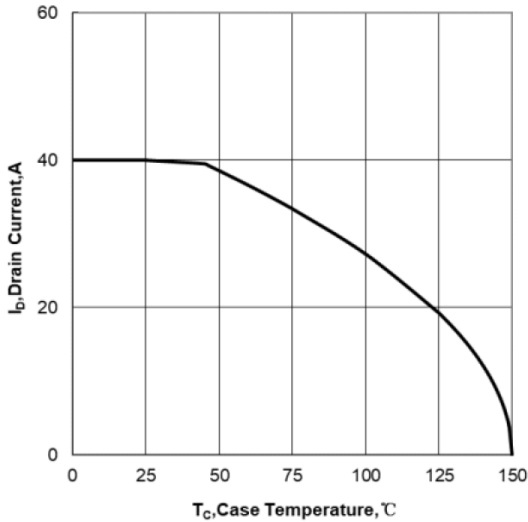


Figure 9. Maximum Continuous Drain Current vs Case Temperature

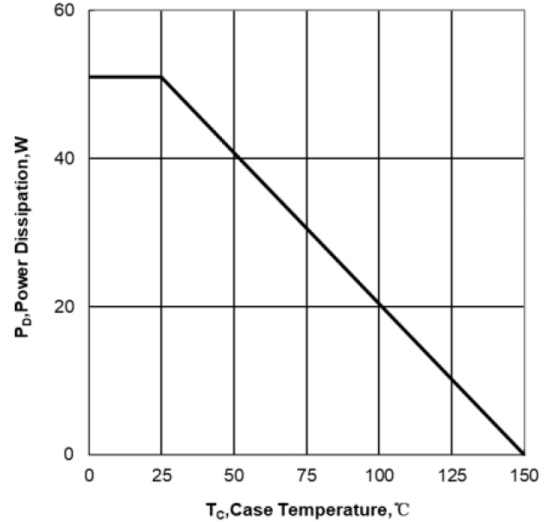


Figure 10. Maximum Power Dissipation vs Case Temperature

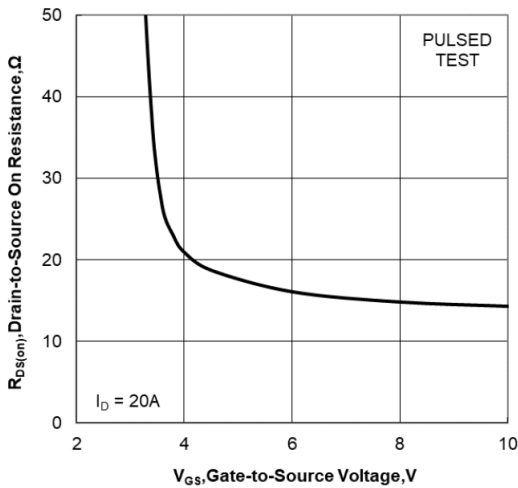


Figure 11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

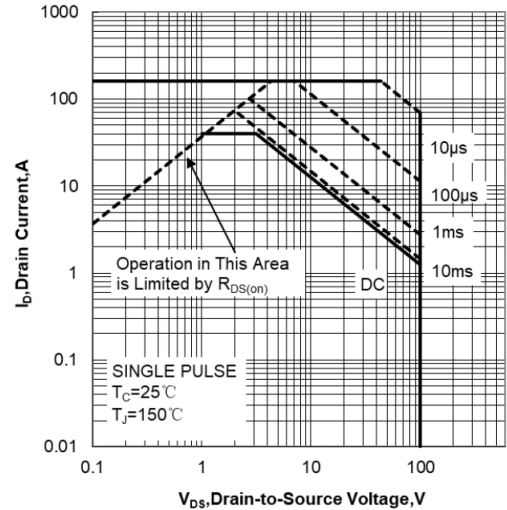


Figure 12. Maximum Safe Operating Area

Typical Operating Characteristics (Cont.)

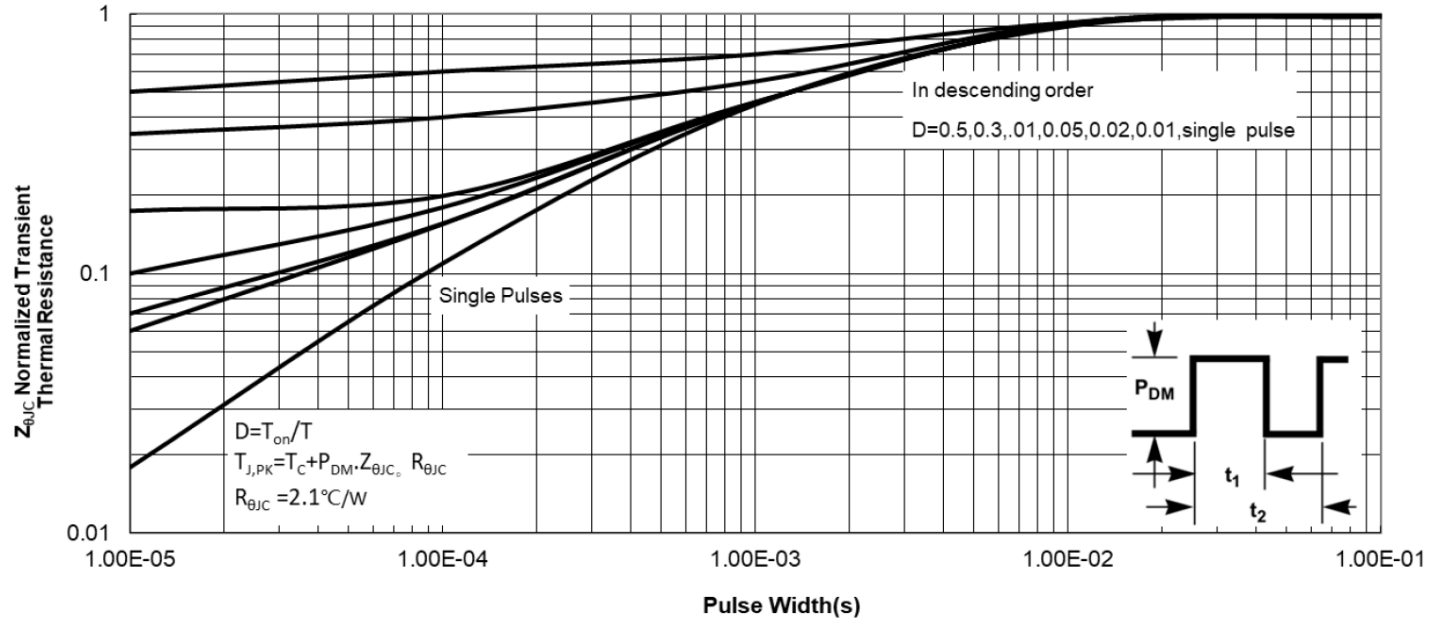
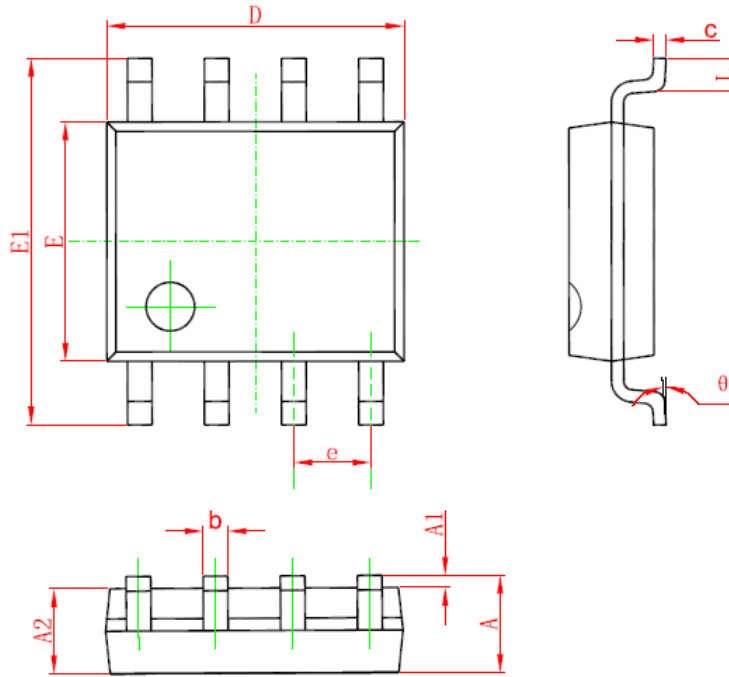


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Information

SOP-8 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Design Notes

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