



BUK9875-100A

N-channel TrenchMOS logic level FET

19 March 2014

Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources

3. Applications

- 12 V, 24 V and 42 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

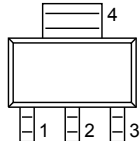
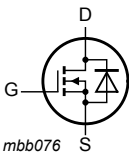
4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--|---|-----|-----|-----|------------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$ | - | - | 100 | V |
| I_D | drain current | $V_{GS} = 5\text{ V}; T_{sp} = 25\text{ °C};$ Fig. 2 ; Fig. 3 | - | - | 7 | A |
| P_{tot} | total power dissipation | $T_{sp} = 25\text{ °C};$ Fig. 1 | - | - | 8 | W |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 4.5\text{ V}; I_D = 8\text{ A}; T_j = 25\text{ °C}$ | - | - | 84 | m Ω |
| | | $V_{GS} = 10\text{ V}; I_D = 8\text{ A}; T_j = 25\text{ °C}$ | - | 62 | 72 | m Ω |
| | | $V_{GS} = 5\text{ V}; I_D = 8\text{ A}; T_j = 25\text{ °C};$ Fig. 12 ; Fig. 13 | - | 64 | 75 | m Ω |
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 7\text{ A}; V_{sup} \leq 100\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 5\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped | - | - | 49 | mJ |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|---|---|
| 1 | G | gate |  SC-73 (SOT223) |  mbb076 |
| 2 | D | drain | | |
| 3 | S | source | | |
| 4 | D | drain | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-----------------|---------|--|---------|
| | Name | Description | Version |
| BUK9875-100A | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |
| BUK9875-100A/CU | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-----------------|--------------|
| BUK9875-100A | 987510A |
| BUK9875-100A/CU | 987510 |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$ | - | 100 | V |
| V_{DGR} | drain-gate voltage | $R_{GS} = 20\text{ k}\Omega$ | - | 100 | V |
| V_{GS} | gate-source voltage | | -10 | 10 | V |
| P_{tot} | total power dissipation | $T_{sp} = 25\text{ °C}$; Fig. 1 | - | 8 | W |
| I_D | drain current | $T_{sp} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2 ; Fig. 3 | - | 7 | A |
| | | $T_{sp} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2 | - | 4 | A |
| I_{DM} | peak drain current | $T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 3 | - | 28 | A |

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|--|--|-----|-----|------|
| T _{stg} | storage temperature | | -55 | 150 | °C |
| T _j | junction temperature | | -55 | 150 | °C |
| V _{GSM} | peak gate-source voltage | pulsed; t _p ≤ 50 μs | -15 | 15 | V |
| Source-drain diode | | | | | |
| I _S | source current | T _{sp} = 25 °C | - | 7 | A |
| I _{SM} | peak source current | pulsed; t _p ≤ 10 μs; T _{sp} = 25 °C | - | 28 | A |
| Avalanche ruggedness | | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | I _D = 7 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped | - | 49 | mJ |

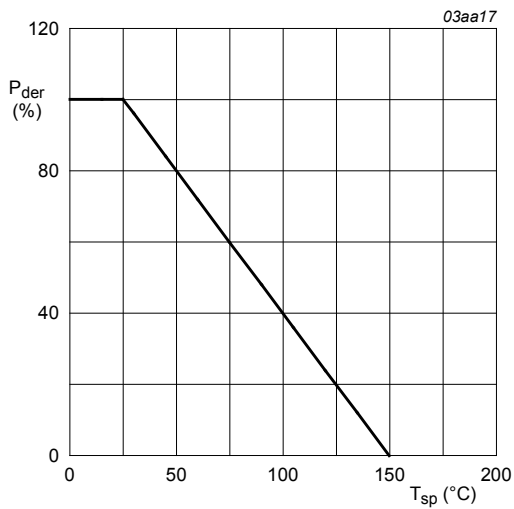


Fig. 1. Normalized total power dissipation as a function of solder point temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

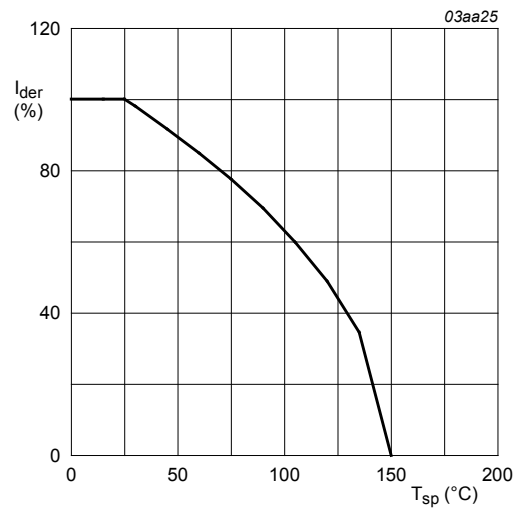


Fig. 2. Normalized continuous drain current as a function of solder point temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

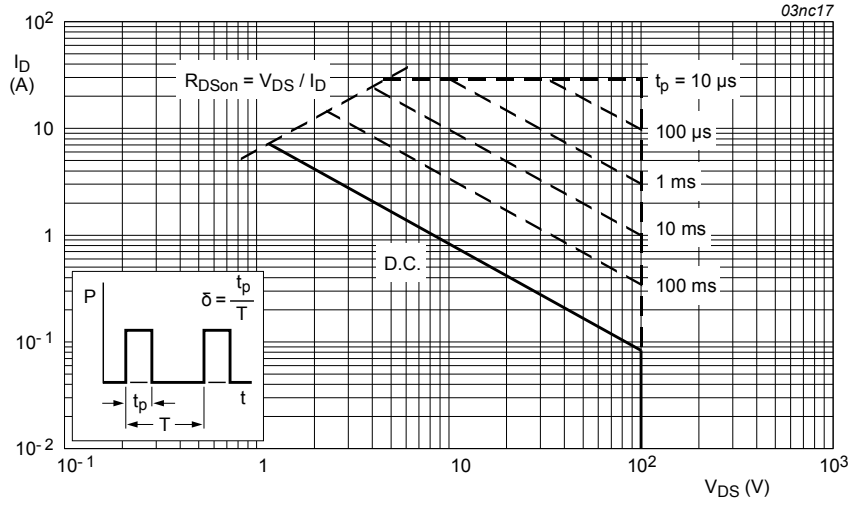


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{amb} = 25^\circ C; I_{DM}$ is single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--|------------------------|-----|-----|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | | - | - | 15 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Fig. 4 | - | 120 | - | K/W |

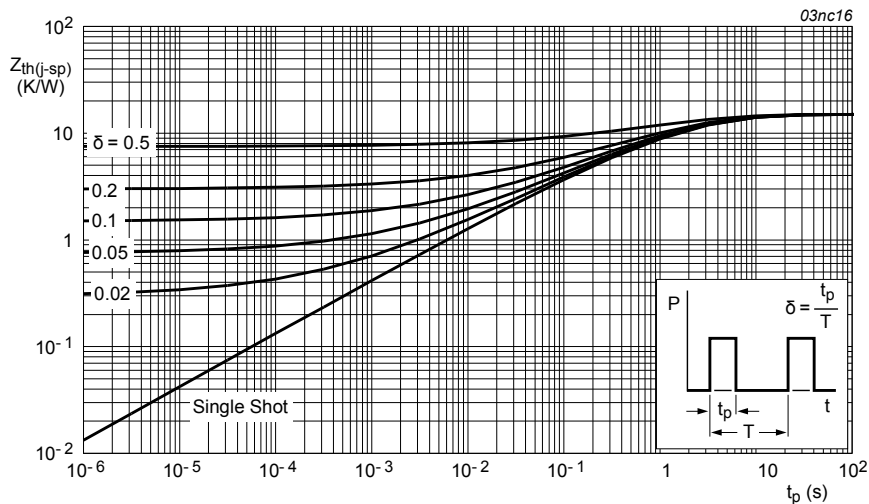


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|-----|------|------|---------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | 100 | - | - | V |
| | | $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$ | 89 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 11 | 1 | 1.5 | 2 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 11 | - | - | 2.3 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ Fig. 11 | 0.6 | - | - | V |
| I_{DSS} | drain leakage current | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 0.05 | 10 | μA |
| | | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$ | - | - | 500 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 2 | 100 | nA |
| | | $V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 2 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 5 \text{ V}; I_D = 8 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ Fig. 12; Fig. 13 | - | - | 162 | m Ω |
| | | $V_{GS} = 4.5 \text{ V}; I_D = 8 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ | - | - | 84 | m Ω |
| | | $V_{GS} = 10 \text{ V}; I_D = 8 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ | - | 62 | 72 | m Ω |
| | | $V_{GS} = 5 \text{ V}; I_D = 8 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 12; Fig. 13 | - | 64 | 75 | m Ω |
| Dynamic characteristics | | | | | | |
| C_{iss} | input capacitance | $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ Fig. 14 | - | 1270 | 1690 | pF |
| C_{oss} | output capacitance | | - | 140 | 167 | pF |
| C_{rss} | reverse transfer capacitance | | - | 90 | 124 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$ | - | 13 | - | ns |
| t_r | rise time | | - | 120 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 58 | - | ns |
| t_f | fall time | | - | 57 | - | ns |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 15 | - | 0.85 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s};$ | - | 63 | - | ns |
| Q_r | recovered charge | $V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 220 | - | nC |

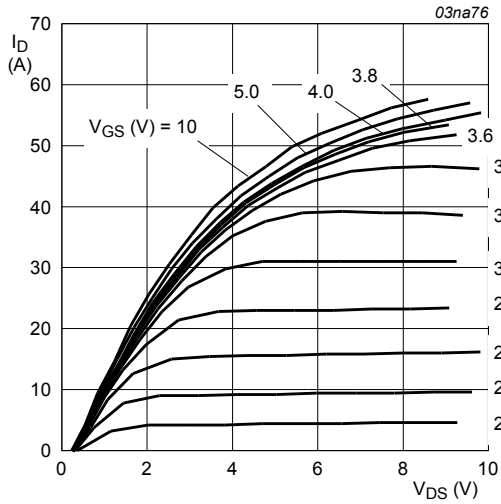


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ\text{C}$

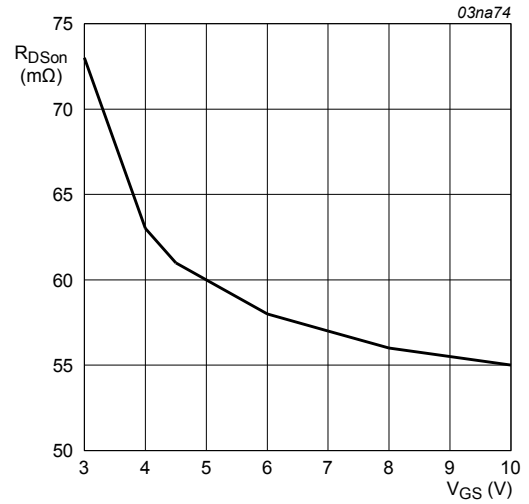


Fig. 6. Drain-source on-state resistance as a function of gate-source; typical values

$T_j = 25^\circ\text{C}; I_D = 8\text{A}$

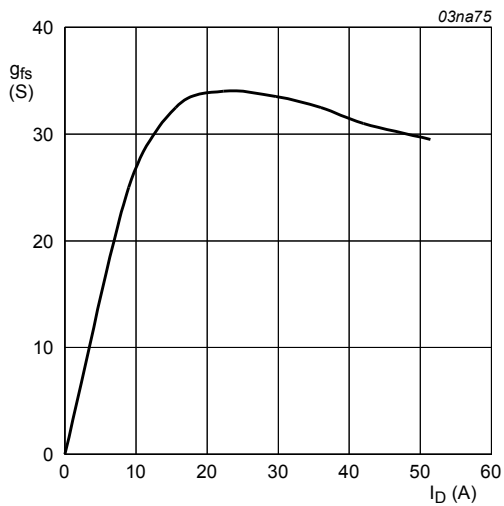


Fig. 7. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

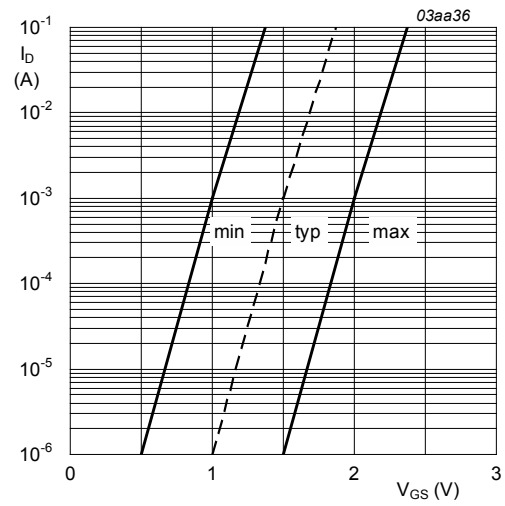


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

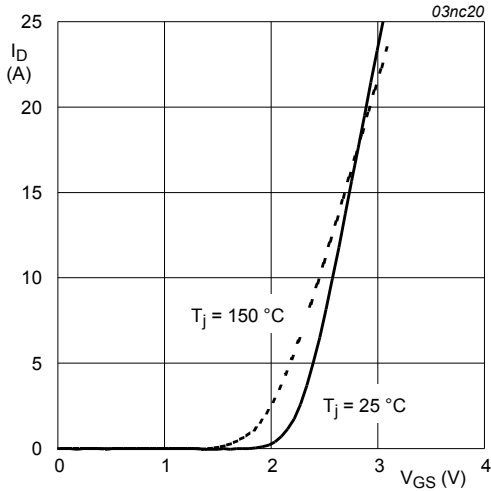


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} = 25V$$

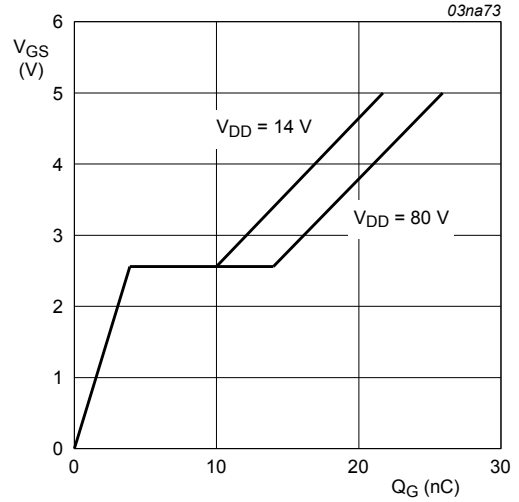


Fig. 10. Gate-source voltage as a function of turn-on gate charge; typical values

$$T_j = 25^\circ C; I_D = 20A$$

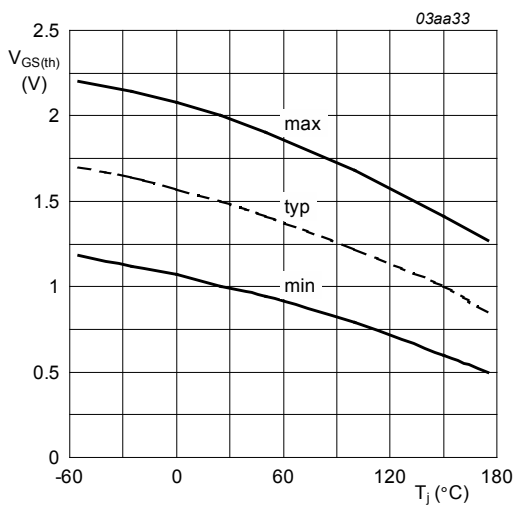


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1mA; V_{DS} = V_{GS}$$

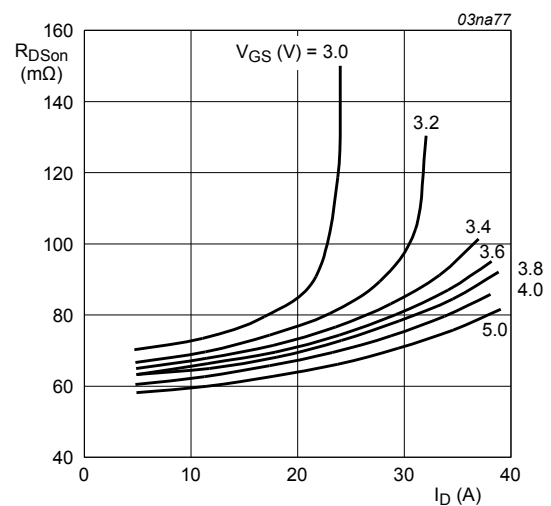


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ C$$

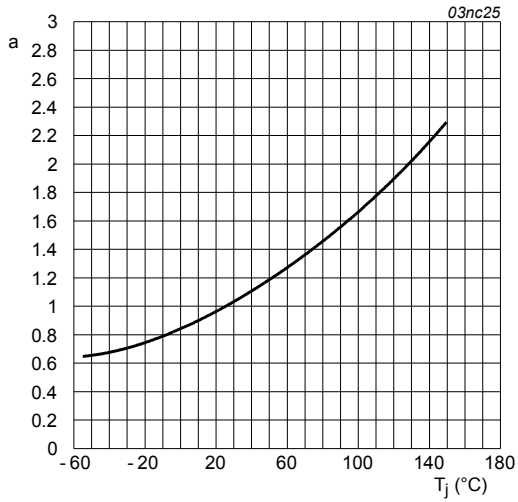


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon@25^\circ C}}$$

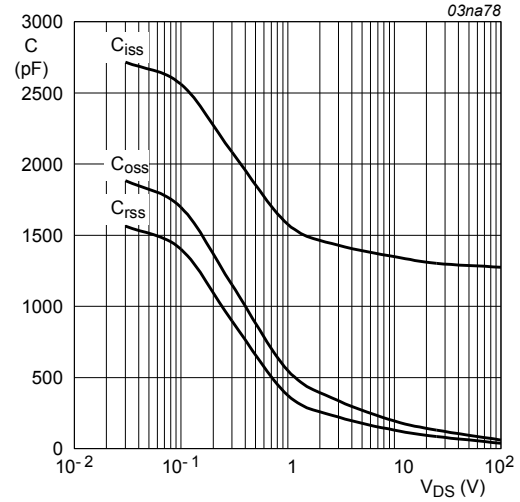


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

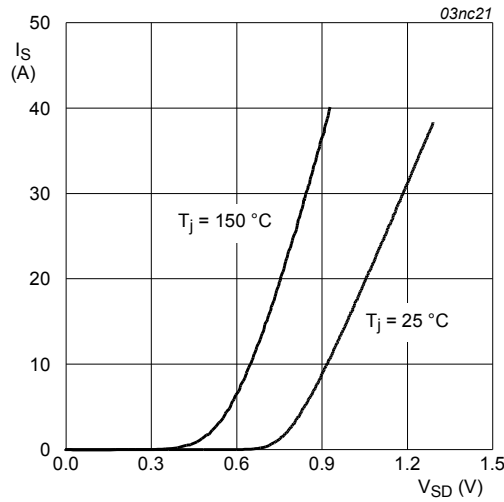


Fig. 15. Reverse diode current as a function of reverse diode voltage; typical value

$$V_{GS} = 0V$$

11. Package outline

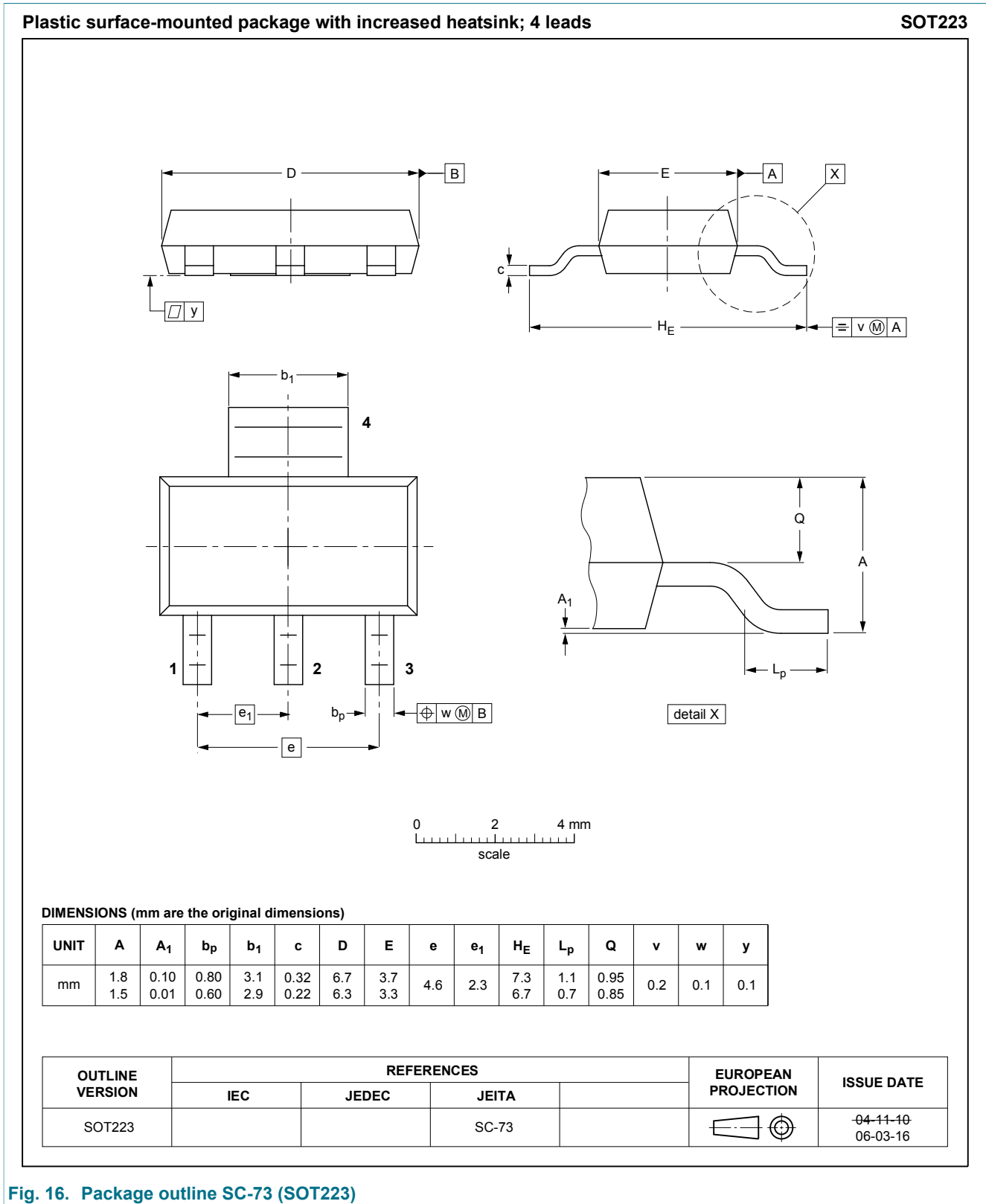


Fig. 16. Package outline SC-73 (SOT223)

12. Legal information

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