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DMP21D0UFB4-P

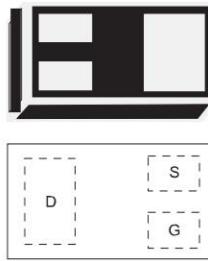
P-Channel Enhancement Mode MOSFET

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Features

- Lead free product is acquired
- Surface mount package
- P-Channel switch with low $R_{DS(on)}$
- Operated at low logic level gate drive
- ESD protected gate
- Complementary to TPM2008EP3

Package and Pin Configuration

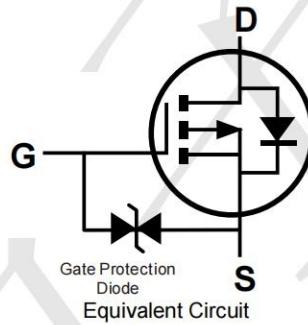


DFN1006-3L

Application

- Load/Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

Circuit diagram



Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	-20	V
Typical gate-source voltage	V_{GS}	± 12	V
Continuous drain current (note 1)	I_D	-0.66	A
Pulsed drain current ($t_p=10\mu\text{s}$)	I_{DM}	-1.2	A
Power dissipation (note 2)	P_D	100	mW
Thermal resistance from junction to ambient (note 1)	R_{QJA}	1250	$^\circ\text{C}/\text{W}$
Junction temperature range	T_J	150	$^\circ\text{C}$
Storage temperature range	T_{STG}	-55 ~ +150	$^\circ\text{C}$
Lead temperature for soldering purposes (1/8" from case for 10s)	T_L	260	$^\circ\text{C}$



Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

A

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}$, $I_D = -250\mu\text{A}$	-20			V
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}} = -20\text{V}$, $V_{\text{GS}} = 0\text{V}$			-1	μA
Gate-body leakage current	I_{GSS}	$V_{\text{GS}} = \pm 10\text{V}$, $V_{\text{DS}} = 0\text{V}$			± 20	μA
Gate threshold voltage (note 2)	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = -250\mu\text{A}$	-0.35		-1.1	V
Drain-source on-resistance (note 2)	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = -4.5\text{V}$, $I_D = -1\text{A}$			520	$\text{m}\Omega$
		$V_{\text{GS}} = -2.5\text{V}$, $I_D = -0.8\text{A}$			700	
		$V_{\text{GS}} = -1.8\text{V}$, $I_D = -0.5\text{A}$			950	
Forward transconductance (note 2)	g_{FS}	$V_{\text{DS}} = -10\text{V}$, $I_D = -0.54\text{A}$		1.2		S
Diode forward voltage	V_{SD}	$I_S = -0.5\text{A}$, $V_{\text{GS}} = 0\text{V}$			-1.2	V
DYNAMIC PARAMETERS (note 4)						
Input capacitance	C_{iss}	$V_{\text{DS}} = -16\text{V}$, $V_{\text{GS}} = 0\text{V}$, $f = 1\text{MHz}$		113	170	pF
Output capacitance	C_{oss}			15	25	
Reverse transfer capacitance	C_{rss}			9	15	
SWITCHING PARAMETERS (note 4)						
Turn-on delay time (note 3)	$t_{\text{d(on)}}$	$V_{\text{GS}} = -4.5\text{V}$, $V_{\text{DS}} = -10\text{V}$, $I_D = -200\text{mA}$, $R_{\text{GEN}} = 10\Omega$		9		ns
Turn-on rise time (note 3)	t_r			5.8		
Turn-off delay time (note 3)	$t_{\text{d(off)}}$			32.7		
Turn-off fall time (note 3)	t_f			20.3		



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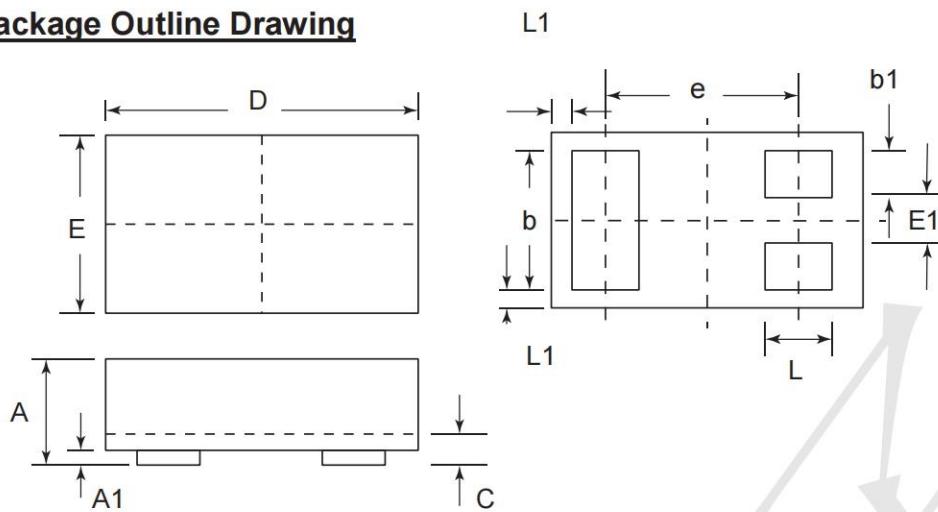
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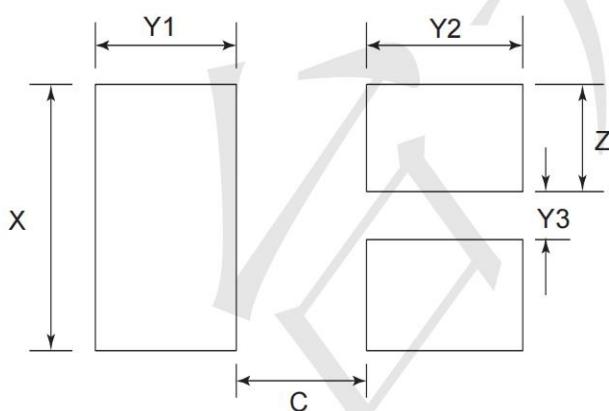
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DFN1006-3L Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.45	0.50	0.55	0.018	0.020	0.022
b1	0.10	0.15	0.20	0.004	0.006	0.008
C	0.12	0.15	0.18	0.005	0.006	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
e	0.65 BSC			0.026 BSC		
E	0.55	0.60	0.65	0.022	0.024	0.026
E1	0.15	0.20	0.25	0.006	0.008	0.010
L	0.20	0.25	0.30	0.008	0.010	0.012
L1	0.05 REF			0.0002 REF		

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	0.25	0.010
X	0.65	0.024
Y1	0.50	0.020
Y2	0.50	0.020
Y3	0.25	0.010
Z	0.20	0.008

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