

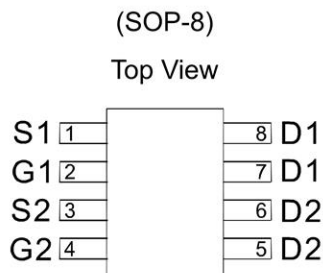
GENERAL FEATURES

- $R_{DS(ON)} \leq 16 \text{ m}\Omega @ V_{GS}=10\text{V}$
- $R_{DS(ON)} \leq 20 \text{ m}\Omega @ V_{GS}=4.5\text{V}$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

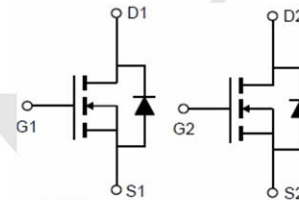
Application

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

Package and Pin Configuration

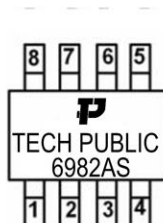


Circuit diagram



Schematic diagram

Marking:



Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_A=25^\circ\text{C}$	10
		$T_A=70^\circ\text{C}$	8.3
Pulsed Drain Current	I_{DM}	38	A
Maximum Power Dissipation	P_D	$T_A=25^\circ\text{C}$	2
		$T_A=70^\circ\text{C}$	1.2
Operating Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	52.0	$^\circ\text{C}/\text{W}$

Electrical Characteristics (TA=25°C Unless Otherwise Specified)

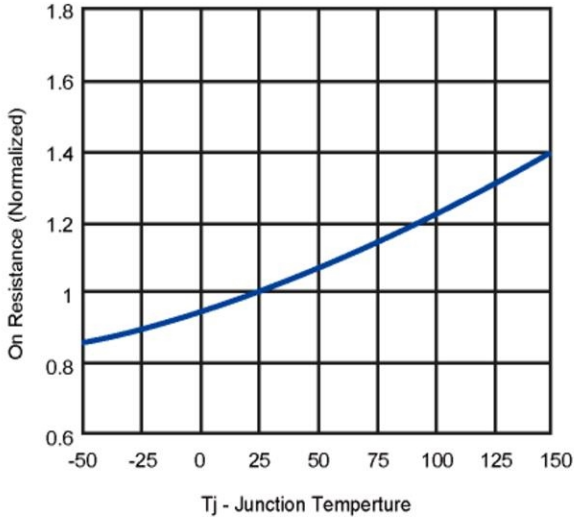
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V, ID=250 μ A	30			V
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250 μ A	1		3	V
IGSS	Gate Leakage Current	VDS=0V, VGS=±20V			±100	nA
IDSS	Zero Gate Voltage Drain Current	VDS=24V, VGS=0V			1	μ A
RDS(ON)	Drain-Source On-Resistance ^a	VGS=10V, ID= 10A		11.2	16	m Ω
		VGS=4.5V, ID= 8A		15.6	20	
VSD	Diode Forward Voltage	IS=8.2A, VGS=0V		0.8	1.2	V
DYNAMIC						
Rg	Gate Resistance	f=1MHz		1		Ω
Qg	Total Gate Charge	VDS=10V, VGS=4.5V, ID=8.2A		9.5		nC
Qgs	Post-Vth Gate-Source Charge			3.6		
Qgd	Gate-Drain Charge			3.4		
Ciss	Input Capacitance	VDS=25V, VGS=0V, f=1MHz		841		pF
Coss	Output Capacitance			250		
Crss	Reverse Transfer Capacitance			71		
td(on)	Turn-On Delay Time	VDD=15V, RL =15 Ω ID=1A, VGEN=10V, RG=6 Ω		14		ns
tr	Turn-On Rise Time			12		
td(off)	Turn-Off Delay Time			43		
tf	Turn-Off Fall Time			4		

Notes: a. pulse test: pulse width \leq 300us, duty cycle \leq 2%, Guaranteed by design, not subject to production testing.

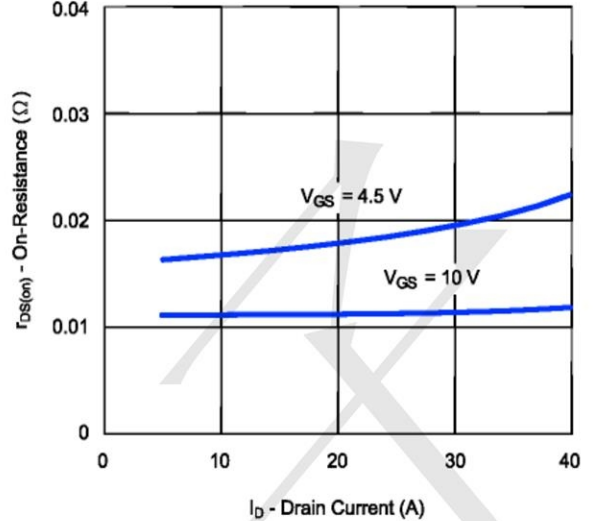
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice



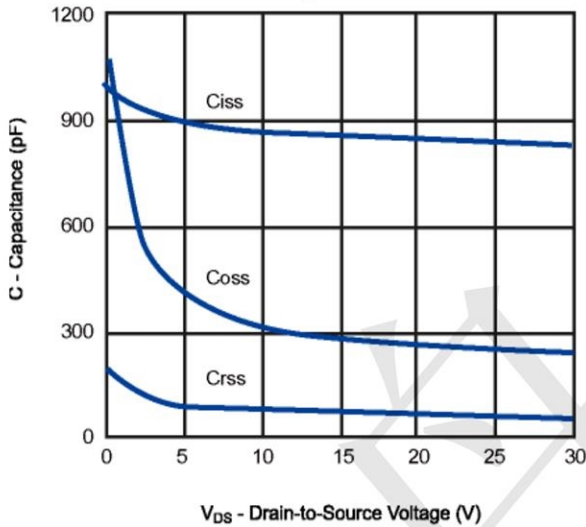
On Resistance vs. Junction Temperature



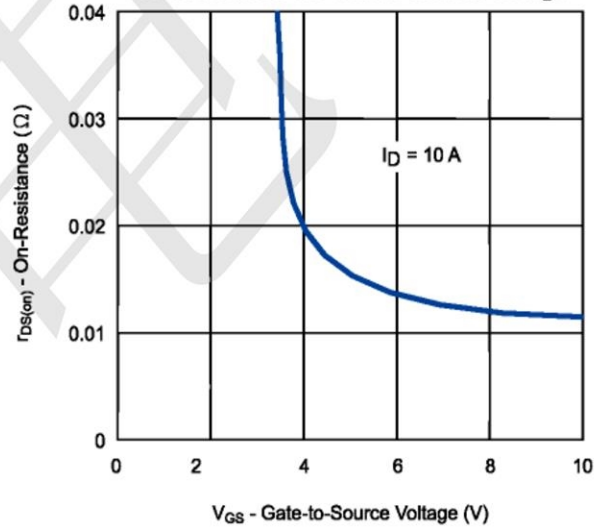
On-Resistance vs. Drain Current



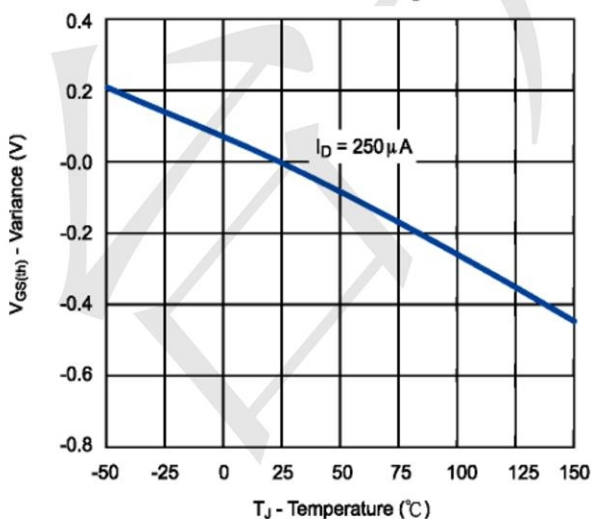
Capacitance



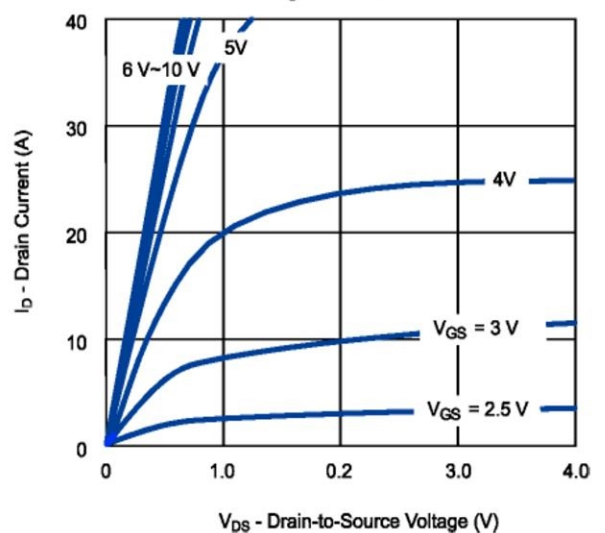
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics





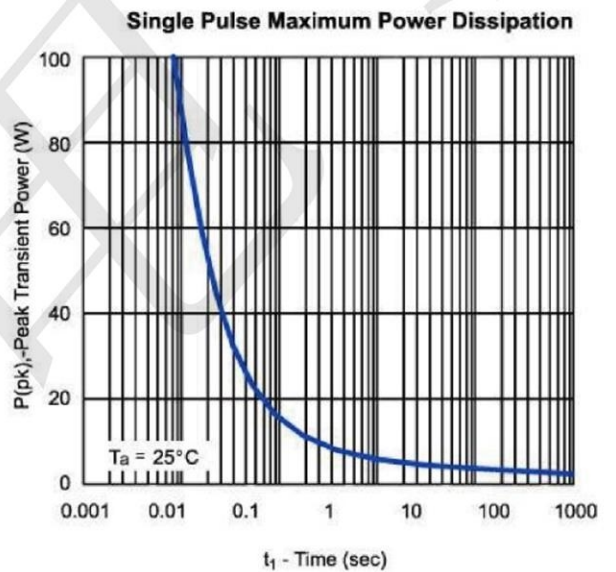
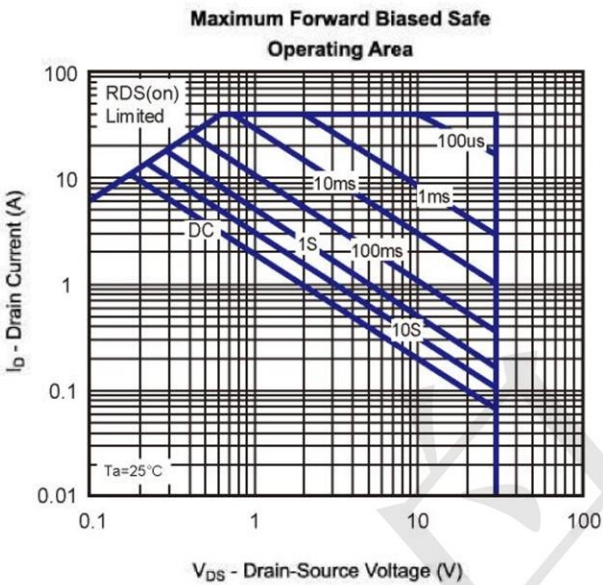
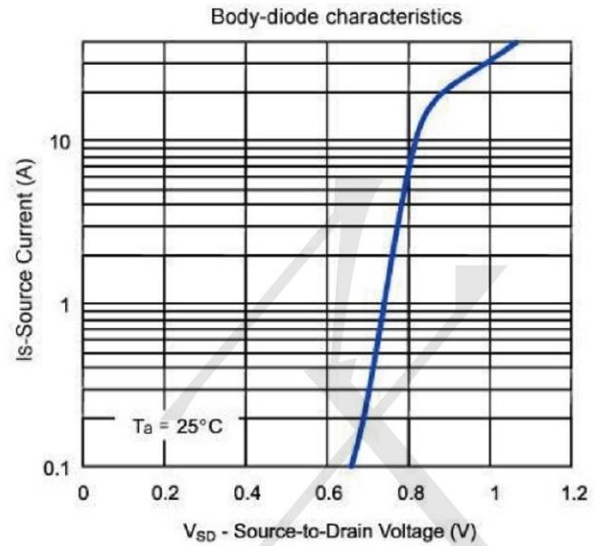
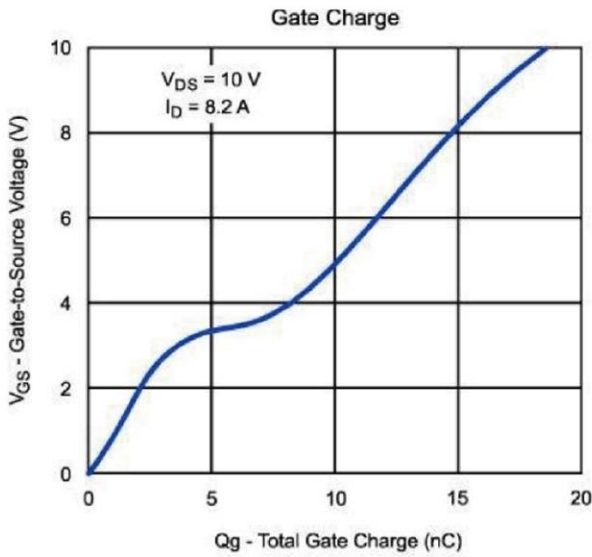
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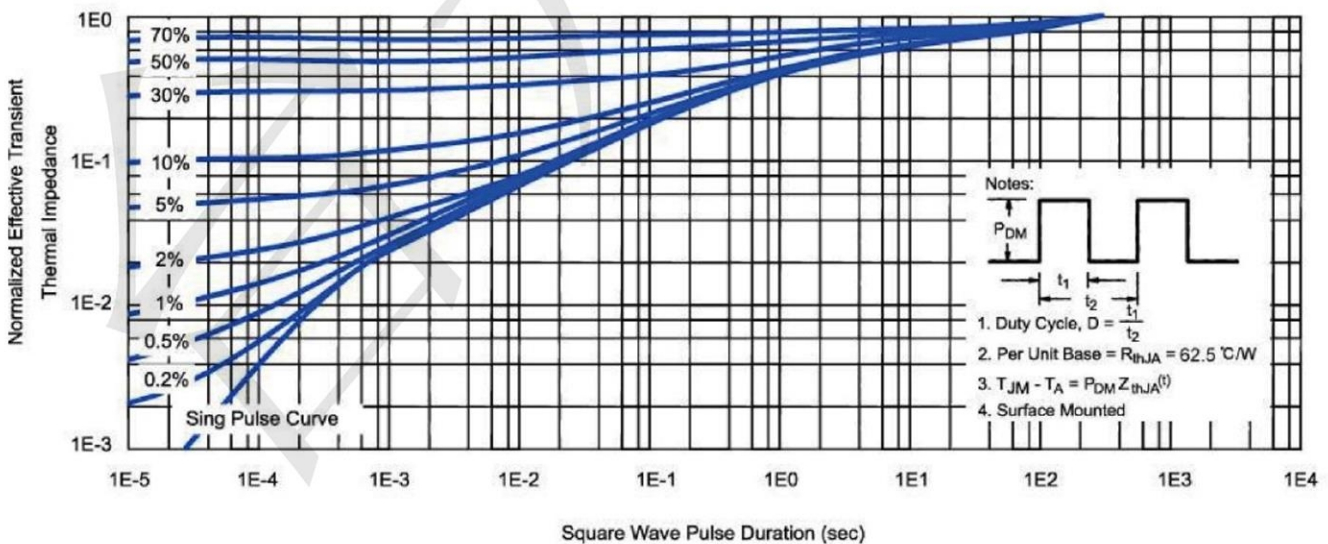
FDS6982AS

Dual N-Channel Enhancement Mode Power MOSFET

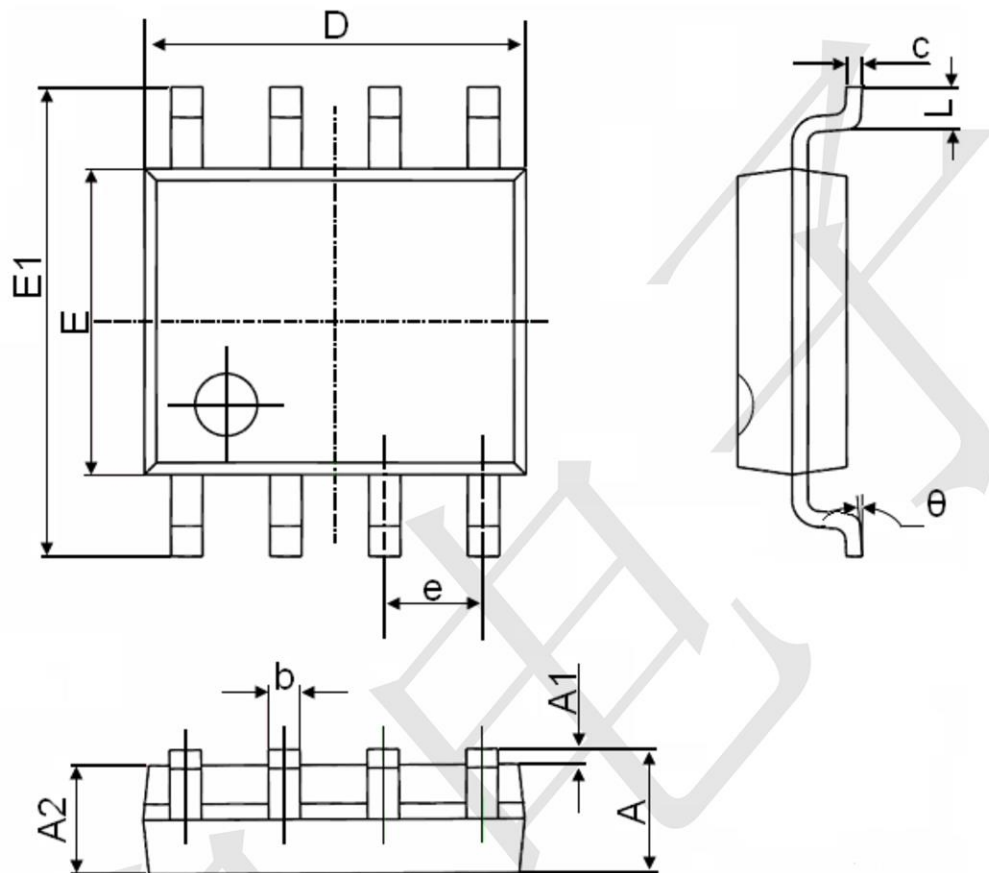
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Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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