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NC7SZ00

Single 2-Input Positive-NAND Gate

www.sot23.com.tw

General Description

This single 2-input positive-NAND gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The NC7SZ00 performs the Boolean function $Y=\overline{A \times B}$ or $Y=\overline{A}+\overline{B}$.in positive logic. The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

The NC7SZ00 device is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8 mm × 0.8 mm.

Features

- **Supports 5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Provides Down Translation to V_{CC}**
- **Max t_{pd} of 3.8 ns at 3.3 V**
- **Low Power Consumption, 10-μA Max I_{CC}**
- **±24-mA Output Drive at 3.3 V**
- **I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back Drive Protection**

Applications

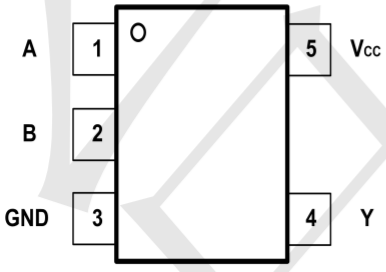
- **AC Receiver**
- **Audio Dock: Portable**
- **Blu-ray Players and Home Theaters**
- **Embedded PC**
- **MP3 Player/Recorder (Portable Audio)**
- **Personal Digital Assistant (PDA)**
- **Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital**
- **Solid State Drive (SSD): Client and Enterprise**
- **TV: LCD/Digital and High-Definition (HDTV)**
- **Tablet: Enterprise**
- **Video Analytics: Server**

Ordering Information

ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION
NC7SZ00M5X	SOT23-5	Tape and Reel,3000
NC7SZ00P5X	SOT353	Tape and Reel,3000

Pin Configuration

SOT23-5/SOT353



Marking

NC7SZ04M5X Marking:7Z00D

NC7SZ04P5X Marking:Z00C

Logic Diagram

Function Table

INPUT(A)	INPUT(B)	OUTPUT(Y)
H	H	L
H	L	H
L	H	H
L	L	H

Note: H: HIGH voltage level; L: LOW voltage level.

Absolute Maximum Ratings

Parameters			Min	Max.	Unit
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range		-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state		-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature under bias			150	℃
T_{stg}	Storage temperature range		-65	150	℃

ESD Ratings

ESD			VALUE	UNIT
V(ESD)	Electrostatic discharge	Human-body model (HBM)	4K	V
		Charge device model (CDM)	2K	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply Voltage		1.65	5.5	V
V_{IH}	High-level input voltage	V_{CC}=1.65V to1.95V	0.65×V_{CC}		V
		V_{CC}=2.3V to 2.7V	1.7		
		V_{CC}=3V to 3.6V	2		
		V_{CC}=4.5V to 5.5V	0.7×V_{CC}		
V_{IL}	Low-level input voltage	V_{CC}=1.65V to1.95V		0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		0.7	
		V_{CC}=3V to 3.6V		0.8	
		V_{CC}=4.5V to 5.5V		0.3×V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC}=1.65V		-4	mA
		V_{CC}=2.3V		-8	
		V_{CC}=3V		-16	
				-24	
		V_{CC}=4.5V		-32	
I_{OL}	Low-level output current	V_{CC}=1.65V		4	mA
		V_{CC}=2.3V		8	
		V_{CC}=3V		16	
				24	
		V_{CC}=4.5V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC}=1.8V±0.15V,2.5V±0.2V		20	ns/V
		V_{CC}=3.3V±0.3V		10	
		V_{CC}=5V±0.5V		5	
T_A	Operating free-air temperature		-40	125	℃

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	–40°C to 85°C			–40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = – 100 µA	1.65 V to 5.5 V	V_{CC}-0.05			V_{CC}-0.05			V
	I_{OH} = –4 mA	1.65 V	1.5			1.5			
	I_{OH} = –8 mA	2.3 V	1.9			1.9			
	I_{OH} = – 16 mA	3 V	2.6			2.6			
	I_{OH} = –24 mA		2.5			2.5			
	I_{OH} = –32 mA	4.5 V	4.0			4.0			
V_{OL}	I_{OL} = 100 µA	1.65 V to 5.5 V			0.05			0.05	V
	I_{OL} = 4 mA	1.65 V			0.1			0.1	
	I_{OL} = 8 mA	2.3 V			0.1			0.1	
	I_{OL} = 16 mA	3 V			0.2			0.2	
	I_{OL} = 24 mA				0.3			0.3	
	I_{OL} = 32 mA	4.5 V			0.3			0.3	
I_I A or B inputs	V_I = 5.5 V or GND	0 to 5.5 V			±5			±5	µA
I_{off}	V_I or V_O = 5.5 V	0			± 10			± 10	µA
I_{CC}	V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10			10	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			10			10	µA
C_i	V_I = V_{CC} or GND	3.3 V		5			5		pF

Electrical specifications(continued)

Switching Characteristics, CL = 15 pF

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tpd	A or B	Y	1.5	7.2	0.7	4.4	0.8	3.6	0.8	3.4	ns

Switching Characteristics, -40°C to 85°C

over recommended operating free-air temperature range, CL = 30 pF or 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tpd	A or B	Y	2.4	8	1.1	5.5	1	4.5	1	4	ns

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 125°C								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tpd	A or B	Y	2.4	10	1.1	7	1	6	1	5	ns

T_A=25°C

	PARAMETER	TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
Cpd	Power dissipation capacitance	f = 10 MHz	16	18	19	20	pF

Typical Characteristics

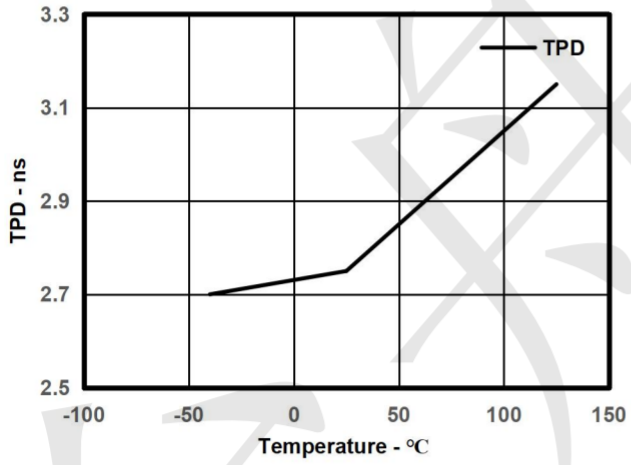


Fig. 8-1. TPD Across Temperature AT 3.3 V V_{CC}

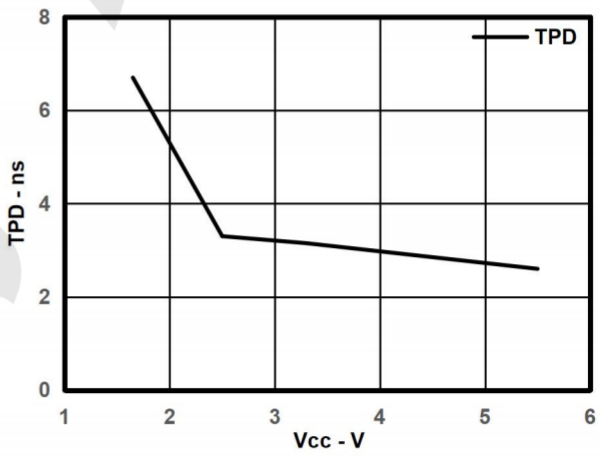


Fig. 8-2. TPD Across V_{CC} at 25°C

Detailed Description

1 Overview

The NC7SZ00 device contains one 2 -input positive NAND gate device and performs the Boolean function $Y=\overline{A\times B}$ or $Y=\overline{A}+\overline{B}$. This device is fully specified for partial-power-down applications using I_{off}.The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

2 Functional Block Diagram

3 Feature Description

- Wide operating voltage range.
- Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

4 Device Functional Modes

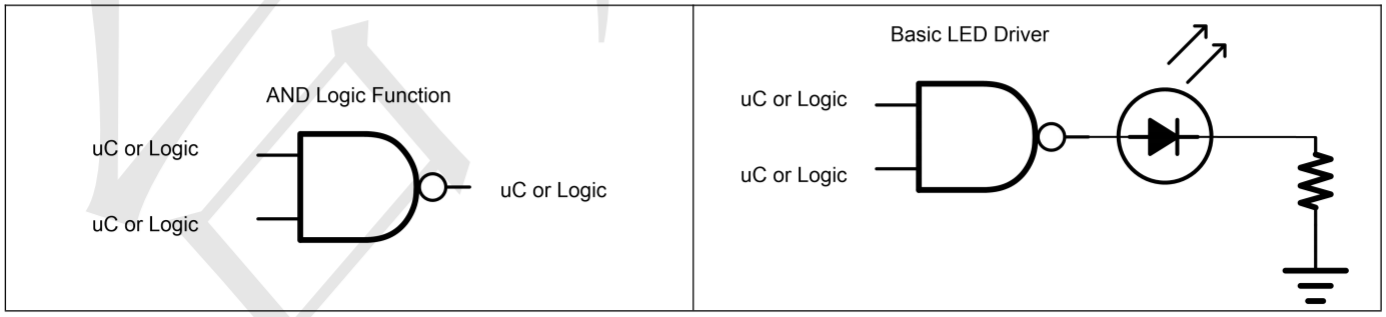
INPUT A		OUTPUT Y
A	B	Y
H	H	L
L	X	H
X	L	H

Application note

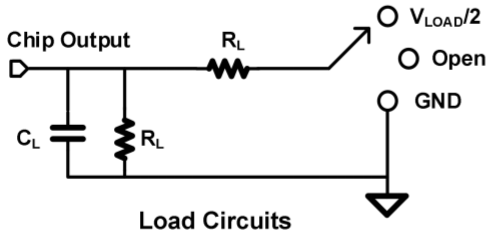
1 Application Information

The NC7SZ00 is a high drive CMOS device that can be used for implementing NAND logic with high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5V tolerant allowing it to translate down to V_{CC}.

2 Typical Application



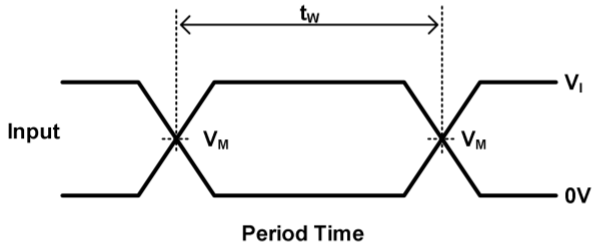
Parameter Measurement Information



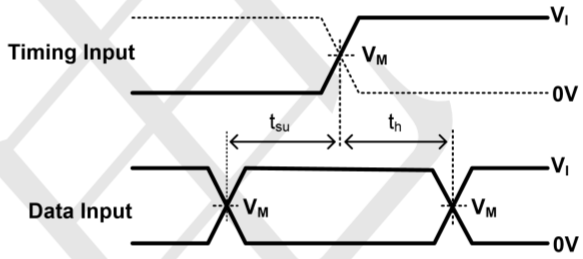
Load Circuits

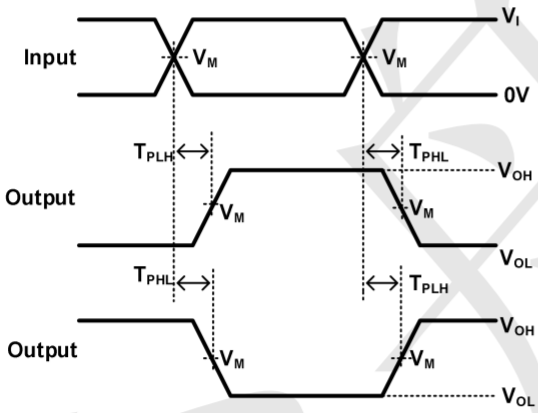
TEST	S1
T_{PHL}/T_{PLH}	OPEN
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LAOD}	C_L	R_L	V_Δ
	V_I	T_r/T_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	15pF	1MΩ	0.15V
2.5V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	15pF	1MΩ	0.15V
3.3V±0.15V	3V	≤2.5ns	1.5V	6V	15pF	1MΩ	0.3V
5V±0.15V	V_{CC}	≤2.5ns	$V_{CC}/2$	$2\times V_{CC}$	15pF	1MΩ	0.3V

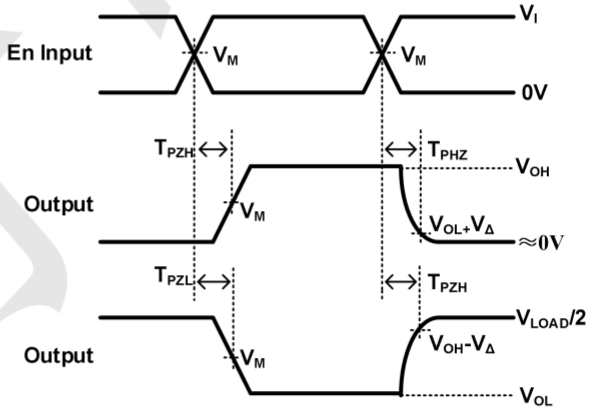


Period Time



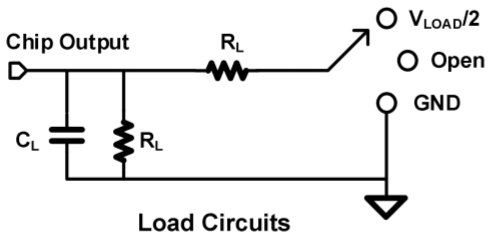


Propagation Delay
for Output and Inverted Output



Enable and Disable Times
Low-And High-Level Enabling

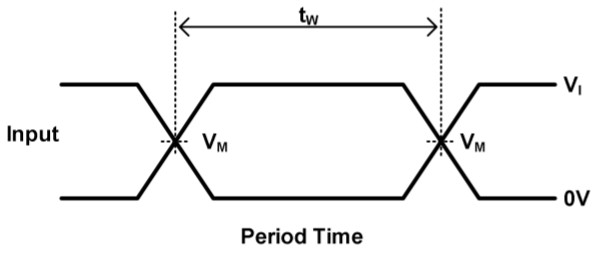
Notes: A. C includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z = 50.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all device.



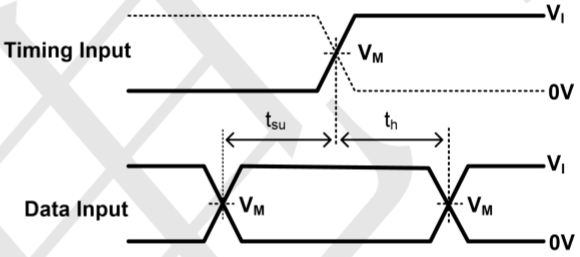
Load Circuits

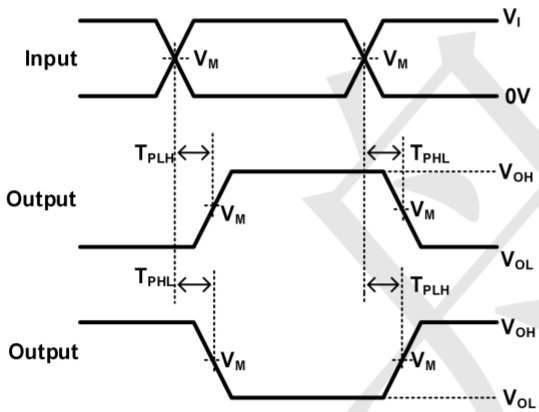
TEST	S1
T_{PHL}/T_{PLH}	OPEN
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LAOD}	C_L	R_L	V_Δ
	V_I	T_r/T_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2×V_{CC}	30pF	1kΩ	0.15V
2.5V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2×V_{CC}	30pF	500Ω	0.15V
3.3V±0.15V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.15V	V_{CC}	≤2.5ns	$V_{CC}/2$	2×V_{CC}	50pF	500Ω	0.3V

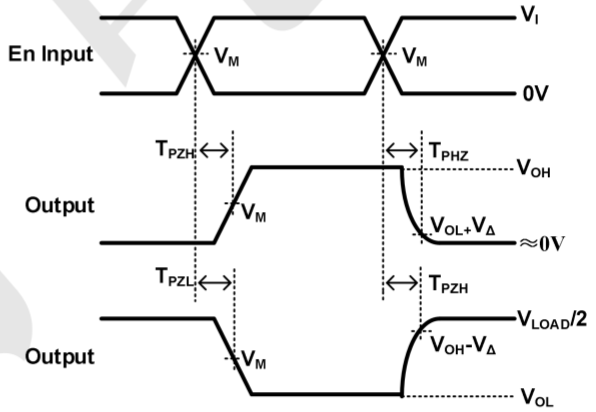


Period Time





Propagation Delay
for Output and Inverted Output



Enable and Disable Times
Low-And High-Level Enabling

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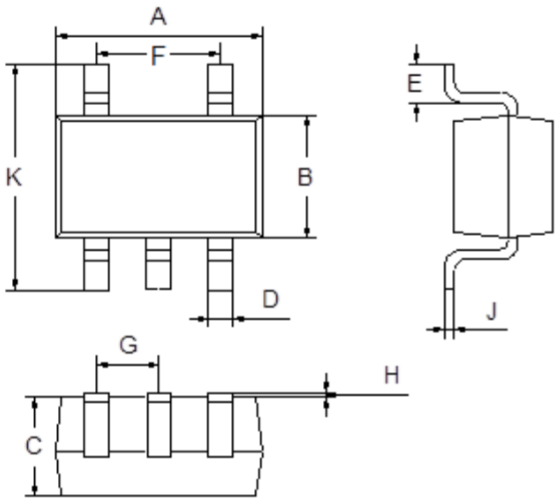
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all device.

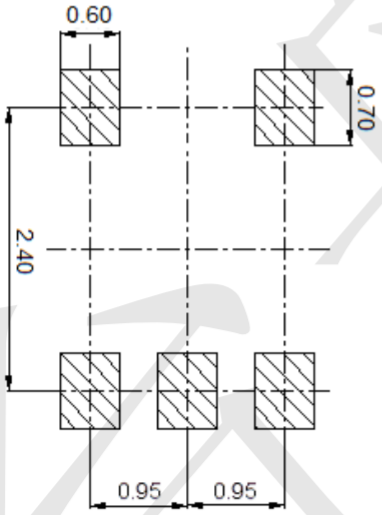
Package Outline Dimensions (Unit: mm)

SOT23-5



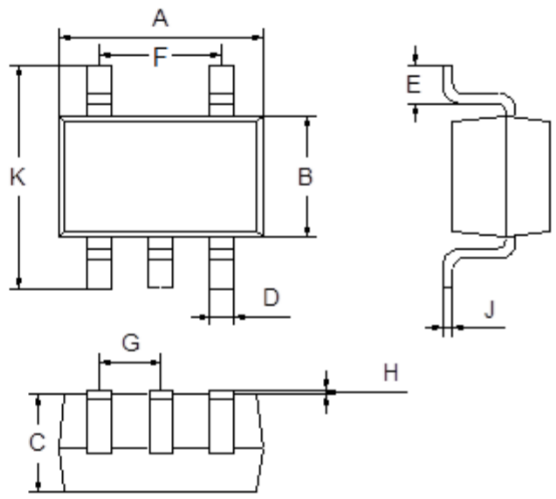
Dimension	Min.	Max.
A	2.80	3.00
B	1.50	1.70
C	1.00	1.20
D	0.35	0.45
E	0.35	0.55
F	1.80	2.00
G	0.90	1.00
H	0.02	0.10
J	0.10	0.20
K	2.60	3.00

Mounting Pad Layout (Unit: mm)



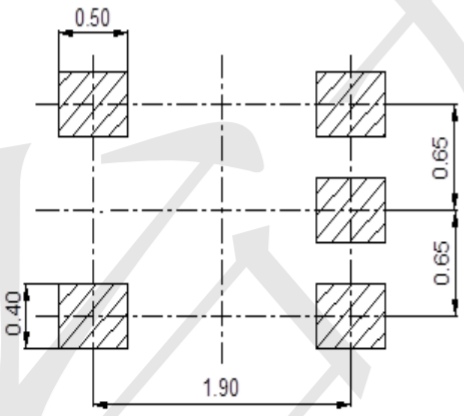
Package Outline Dimensions (Unit: mm)

SOT353



Dimension	Min.	Max.
A	2.00	2.20
B	1.15	1.35
C	0.85	1.05
D	0.15	0.35
E	0.25	0.40
F	1.20	1.40
G	0.60	0.70
H	0.02	0.10
J	0.05	0.15
K	2.20	2.40

Mounting Pad Layout (Unit: mm)



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