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Vishay Siliconix

N-Channel 20 V (D-S) MOSFET

SOT-23 (TO-236)

Top View

Marking code: P5

PRODUCT SUMMARY						
V _{DS} (V)	20					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0318					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 2.5 \text{ V}$	0.0356					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 1.8 \text{ V}$	0.0414					
Q _g typ. (nC)	8.8					
I _D (A) a, e	6					
Configuration	Single					

FEATURES

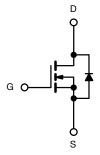
- TrenchFET® power MOSFET
- 100% R_g tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912



ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- DC/DC converters
- Load switch for portable applications



N-Channel MOSFET

ORDERING INFORMATION				
Package	SOT-23			
Lead (Pb)-free and halogen-free	Si2312CDS-T1-GE3			

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	20	V	
Gate-source voltage		V _{GS}	± 8	v	
	T _C = 25 °C		6 ^a		
Continuous dusin comment /T 150 °C)	T _C = 70 °C	1 .	5.1		
Continuous drain current (T _J = 150 °C)	T _A = 25 °C	I _D	5 b, c		
	T _A = 70 °C	<u> </u>	4 b, c	Α	
Pulsed drain current		I _{DM}	20		
Continuous source-drain diode current	T _C = 25 °C		1.75		
	T _A = 25 °C	- I _S	1.04 ^{b, c}		
Maximum power dissipation	T _C = 25 °C	_	2.1		
	T _C = 70 °C		1.3	14/	
	T _A = 25 °C	P _D	1.25 ^{b, c}	W	
	T _A = 70 °C	1	0.8 b, c		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	00	
Soldering recommendations (peak temperature)		İ	260	°C	

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT			
Maximum junction-to-ambient b, d	t ≤ 5 s	R _{thJA}	80	100	°C/W		
Maximum junction-to-foot (drain)	Steady state	R_{thJF}	40	60	7 °C/W		

Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 5 s
- d. Maximum under steady state conditions is 125 °C/W
- e. Based on T_C = 25 °C

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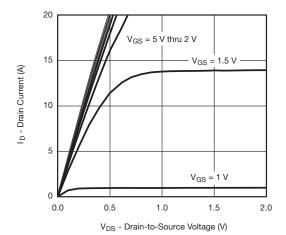
PARAMETER	SYMBOL						
Static	OT MIDGE	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Drain-source breakdown voltage	\ \/	V0V I250 W	20		l	V	
V _{DS} temperature coefficient	V_{DS} $\Delta V_{DS}/T_{J}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20	25	-	V	
V _{GS(th)} temperature coefficient	$\Delta V_{DS}/T_J$ $\Delta V_{GS(th)}/T_J$	$I_D = 250 \mu A$		-2.6	-	mV/°C	
Gate-source threshold voltage	` '	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.45	-2.0	1	V	
~	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$ $V_{DS} = 0 \text{V}, V_{GS} = \pm 8 \text{V}$	0.45	_	± 100	nA	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$ $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$		-	1	IIA	
Zero gate voltage drain current	I _{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 \text{ °C}$	-		10	μΑ	
On-state drain current ^a	+ , +	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 \text{ C}$ $V_{DS} \le 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	20	-	10	Α	
On-state drain current -	I _{D(on)}		-	0.0265	0.0318	A	
Drain acuras an atata registance à		$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	-				
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 2.5 V, I _D = 4.7 A	-	0.0296	0.0356	Ω	
Formal Laboratoria	1	V _{GS} = 1.8 V, I _D = 4.3 A	-	0.0345	0.0414		
Forward transconductance a	9 _{fs}	$V_{DS} = 10 \text{ V}, I_{D} = 5 \text{ A}$	-	24	-	S	
Dynamic ^b			1		I	I	
Input capacitance	C _{iss}		-	865	-	pF	
Output capacitance	C _{oss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	105	-		
Reverse transfer capacitance	C _{rss}		-	55	-		
Total gate charge	Q _g	$V_{DS} = 10 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 5 \text{ A}$	-	12	18		
			-	8.8	14	nC	
Gate-source charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	-	1.1	-		
Gate-drain charge	Q_{gd}		-	0.7	-		
Gate resistance	R_g	f = 1 MHz	0.5	2.4	4.8	Ω	
Turn-on delay time	t _{d(on)}		-	8	16		
Rise time	t _r	V_{DD} = 10 V, R_L = 2.2 Ω	-	17	26		
Turn-off delay time	t _{d(off)}	$I_D\cong 4~A,~V_{GEN}=4.5~V,~R_g=1~\Omega$	-	31	47		
Fall time	t _f		-	8	16	no	
Turn-on delay time	t _{d(on)}		-	5	10	ns	
Rise time	t _r	$V_{DD} = 10 \text{ V}, R_L = 2.2 \Omega$	-	13	20		
Turn-off delay time	t _{d(off)}	$I_D\cong 4$ A, V_{GEN} = 5 V, R_g = 1 Ω	-	21	32		
Fall time	t _f		-	6	12		
Drain-Source Body Diode Characteristi	cs						
Continuous source-drain diode current	Is	T _C = 25 °C	-	-	1.75		
Pulse diode forward current	I _{SM}		-	-	20	Α	
Body diode voltage	V _{SD}	$I_S = 4 A, V_{GS} = 0 V$	-	0.75	1.2	V	
Body diode reverse recovery time	t _{rr}	- 	-	12	20	ns	
Body diode reverse recovery charge	Q _{rr}	$I_F = 4 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	5	10	nC	
body diode reverse recovery charge							
Reverse recovery fall time	t _a	T _J = 25 °C	-	7	-		

Notes

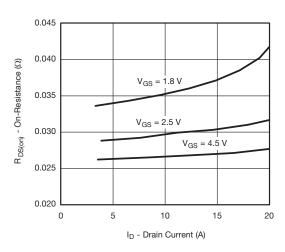
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

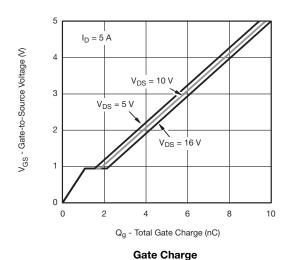


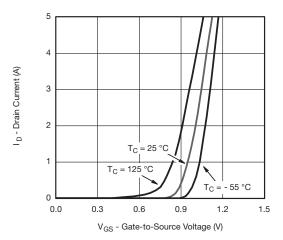


Output Characteristics

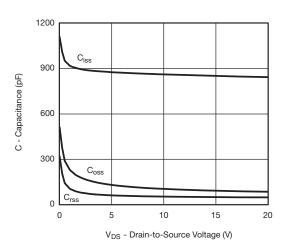


On-Resistance vs. Drain Current and Gate Voltage

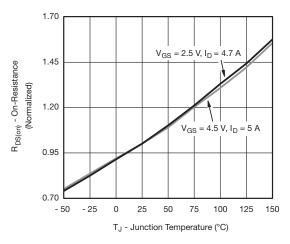




Transfer Characteristics

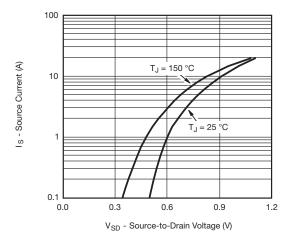


Capacitance

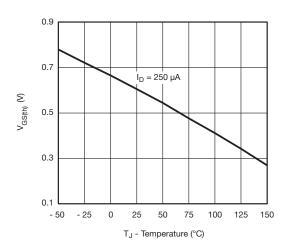


On-Resistance vs. Junction Temperature

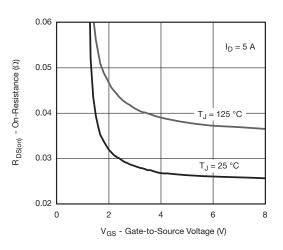




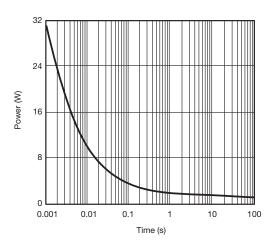
Source-Drain Diode Forward Voltage



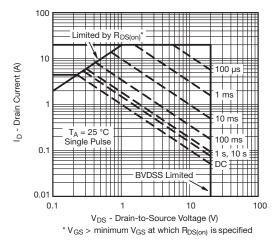
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

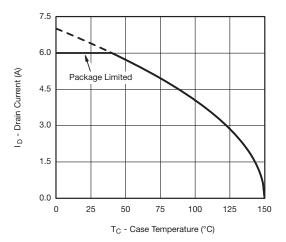


Single Pulse Power (Junction-to-Ambient)

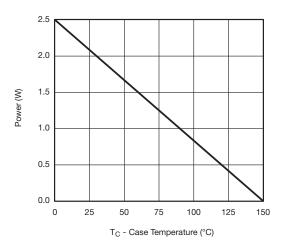


Safe Operating Area, Junction-to-Ambient

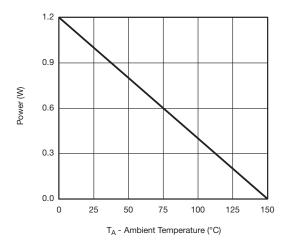




Current Derating a



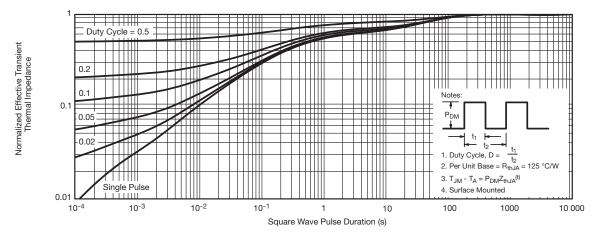




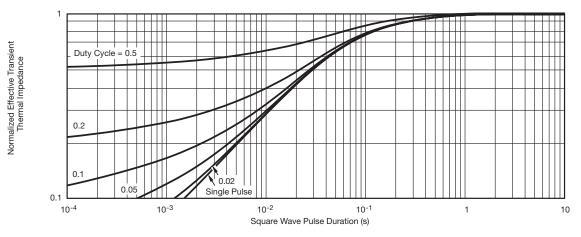
Power Derating, Junction-to-Ambient

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for silicon technology and package reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65900.

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SOT-23 (TO-236): 3-LEAD







Dim	MILLI	METERS	INCHES		
	Min	Max	Min	Max	
Α	0.89	1.12	0.035	0.044	
A ₁	0.01	0.10	0.0004	0.004	
A ₂	0.88	1.02	0.0346	0.040	
b	0.35	0.50	0.014	0.020	
С	0.085	0.18	0.003	0.007	
D	2.80	3.04	0.110	0.120	
E	2.10	2.64	0.083	0.104	
E ₁	1.20	1.40	0.047	0.055	
е	0.95 BSC		0.0374 Ref		
e ₁	1.90 BSC		0.0748 Ref		
L	0.40	0.60	0.016	0.024	
L ₁	0.64 Ref		0.025 Ref		
S	0.50 Ref		0.020 Ref		
q	3°	8°	3°	8°	
FCN: S-03946-Bev K 09-Jul-01					

ECN: S-03946-Rev. K, 09-Jul-01

DWG: 5479

Document Number: 71196 www.vishay.com 09-Jul-01





Mounting LITTLE FOOT® SOT-23 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs, (http://www.vishay.com/doc?72286), for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint. In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the ambient air. This pattern uses all the available area underneath the body for this purpose.



FIGURE 1. Footprint With Copper Spreading

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.

Document Number: 70739

26-Nov-03



RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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