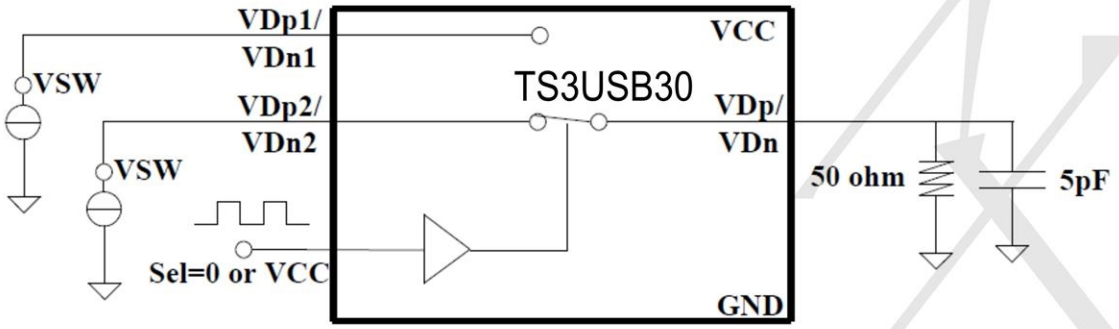
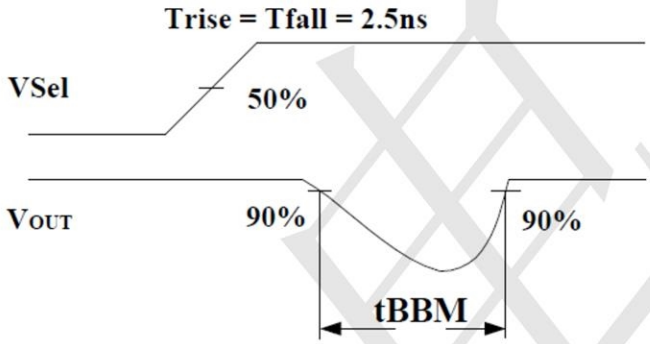
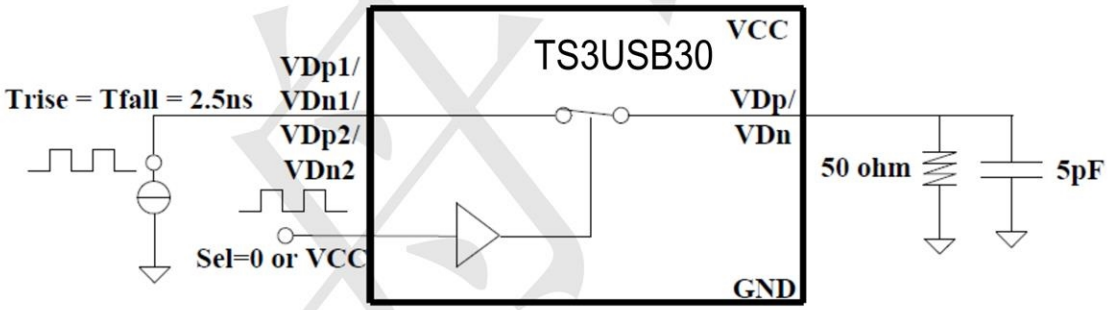
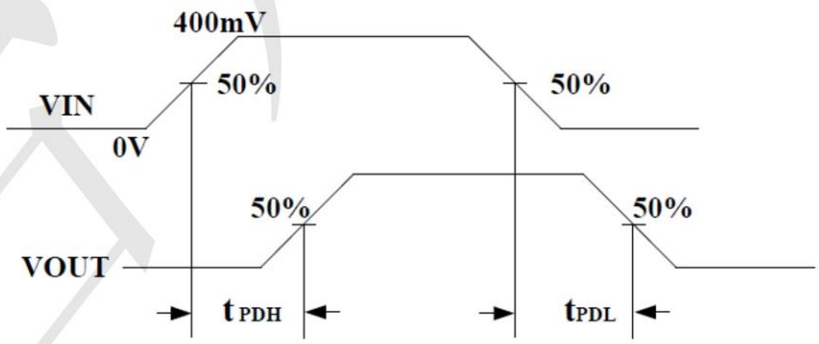
6. Test Circuit for Break-Before-Make Time Delay, $t_{BBM}$



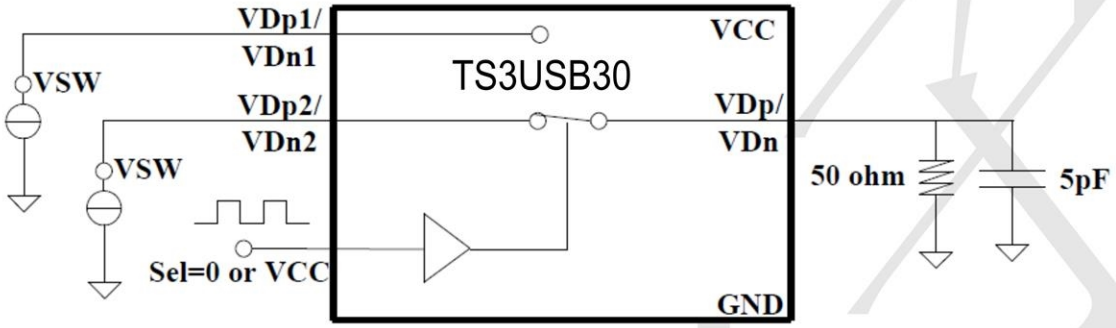



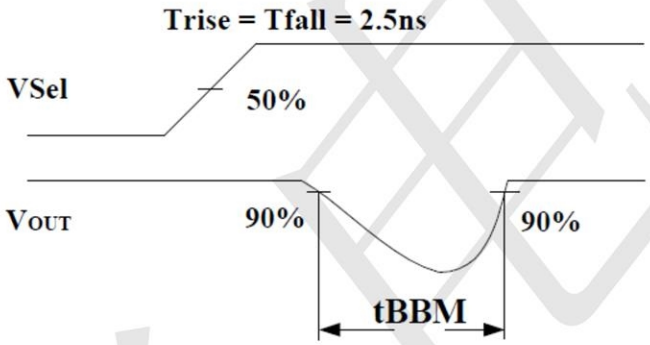

7. Test Circuit for Propagation Delay, $T_{PD}$



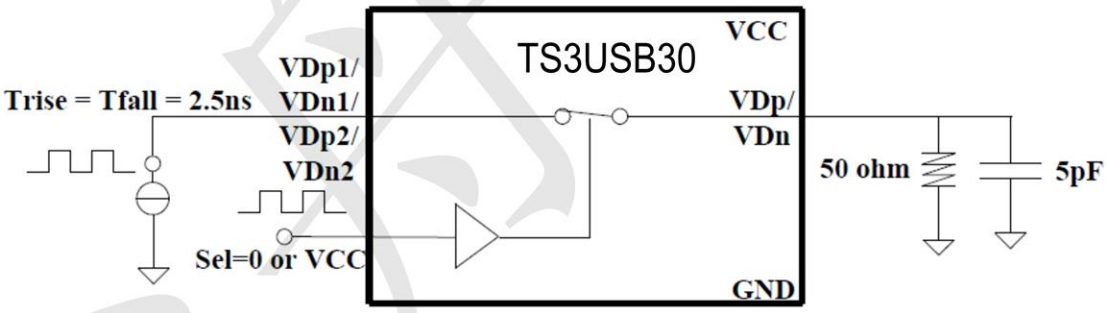



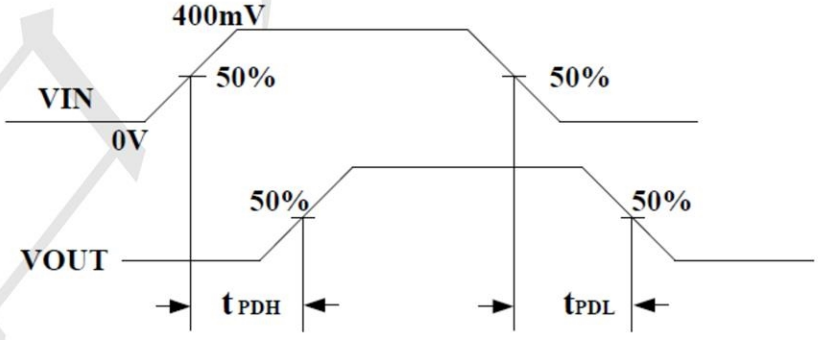
6. Test Circuit for Break-Before-Make Time Delay, $t_{BBM}$



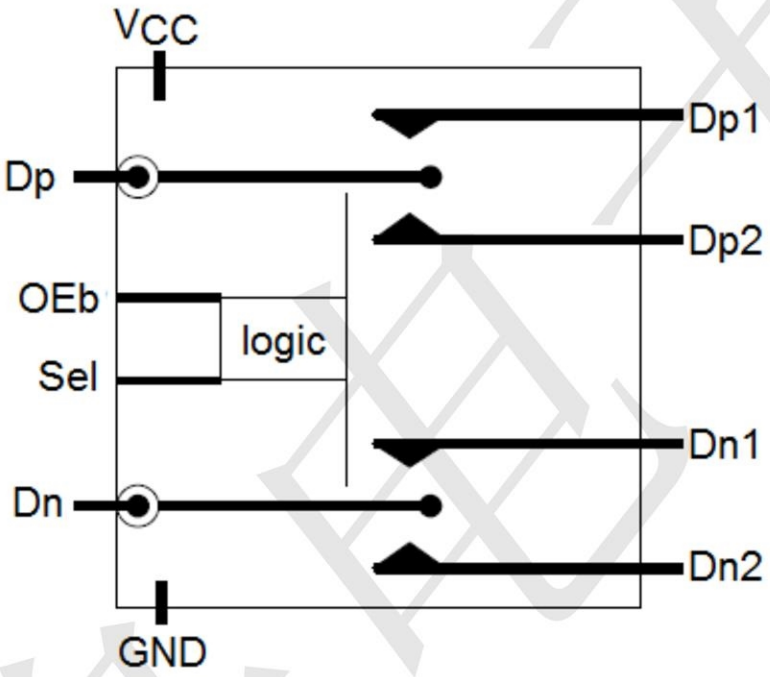




7. Test Circuit for Propagation Delay, $T_{PD}$



## BLOCK DIAGRAM



## DETAILED INFORMATION

APPLICATION NOTE

Meeting USB 2.0 $V_{BUS}$ Short Requirements

Power-Off Protection

For a $V_{BUS}$ short circuit the switch is expected to withstand such a condition for at least 24 hours. The TS3USB30 has the specially designed circuit which prevents unintended signal bleed through as well as guaranteed system reliability during a power-down, over-voltage condition. The protection has been added to the common pins (Dp, Dn).

Power-On Protection

The USB 2.0 specification also notes that the USB device should be capable of withstanding a $V_{BUS}$ short during transmission of data. This modification works by limiting current flow back into the $V_{CC}$ rail during the over-voltage event so current remains within the safe operating range.

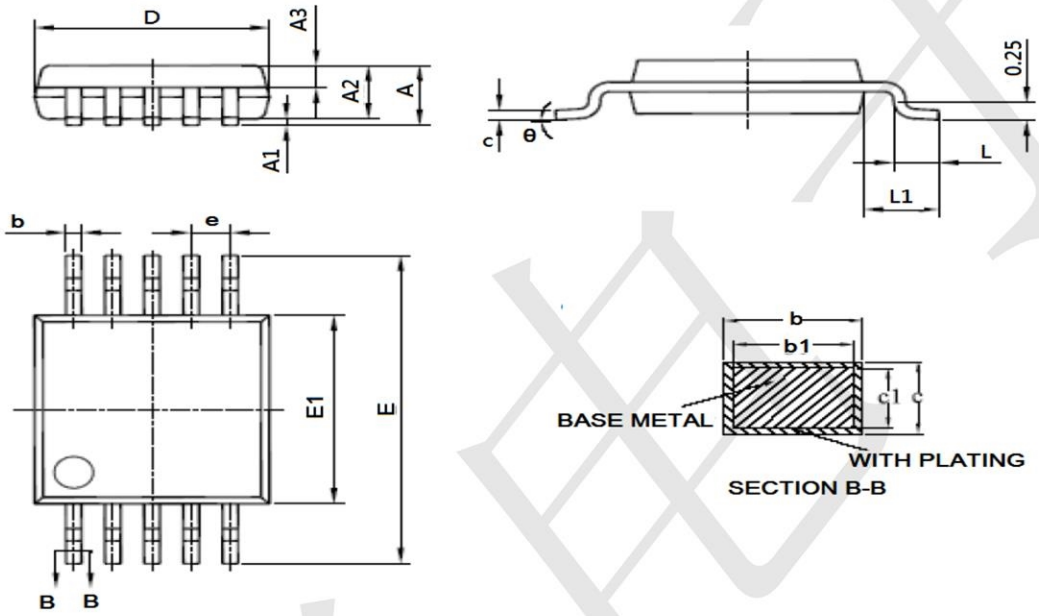
11

Time (250μs/Div)

Time (10μs/Div)

## Package informantion

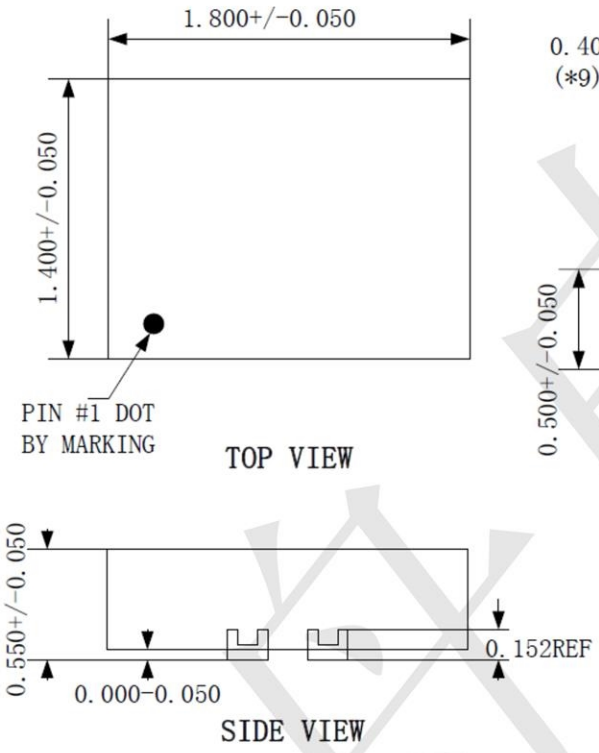
Dimension in MSOP10 (1.8x1.4) (Unit: mm)




| Symbol | Min | Max |
|---|---|---|
| A | - | 1.100 |
| A1 | 0.050 | 0.150 |
| A2 | 0.750 | 0.950 |
| A3 | 0.300 | 0.400 |
| b | 0.190 | 0.280 |
| b1 | 0.180 | 0.230 |
| c | 0.150 | 0.200 |
| c1 | 0.140 | 0.160 |
| D | 2.900 | 3.100 |
| E | 4.700 | 5.100 |
| E1 | 2.900 | 3.100 |
| e | 0.500(BSC) | |
| L | 0.400 | 0.700 |
| L1 | 0.950(BSC) | |
| θ | 0° | 8° |

## Package informantion

Dimension in TQFN10 (Unit: mm)



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# TP3USB30D10

**DPDT ANALOG SWITCH**
**LOW-POWER, TWO-PORT, HIGH-SPEED, USB2.0 (480Mbps)**

www.sot23.com.tw

## General Description

The TP3USB30 is a Low-Power, Two-Port, High-Speed, USB2.0 (480Mbps) double–pole double-throw (DPDT) Analog Switch featuring an On-Resistance of 4.5Ω at $V_{CC}$=3V and a Low On Capacitance 3.7pF Typical.

The TP3USB30 is compatible with the requirements of USB2.0 and the wide bandwidth needed to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to channel crosstalk also minimizes interference. Break-before-make function for both parts eliminates signal disruption during switching from preventing both switches being enabled simultaneously.

The TP3USB30 contains special circuitry on the switch I/O pins for applications where the $V_{CC}$ supply is powered-off ($V_{CC}$=0), which allows the device to withstand an over-voltage condition. This device is designed to minimize current consumption even when the control voltage applied to the Sel pin is lower than the supply voltage ($V_{CC}$). This feature is especially valuable to ultra-portable applications, such as cell phones, allowing for direct interface with the general purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

The TP3USB30 is available in TQFN10 (1.8x1.4) and MSOP10 packages.

## Applications

- Wide Power Supply Range: 2.3V to 5V
- Low On Capacitance 3.7pF Typical
- Low On Resistance 4.5Ω (typ.) at 3V $V_{DD}$ when $V_{SW}$=0.4V
- High Bandwidth (-3db): >720MHz without $C_L$ and >550MHz with $C_L$=5pF
- Low Power Consumption: 1uA Maximum
- ESD: pass 8kV HBM test
- Over voltage tolerance (OVT) on all USB ports up to 5.25V without external components
- TTL/CMOS Compatible
- Break-Before-Make Switching
- Operation Temperature Range: -40℃ to 85℃
- Available in TQFN10 (1.8x1.4) and MSOP10 Packages

## Features

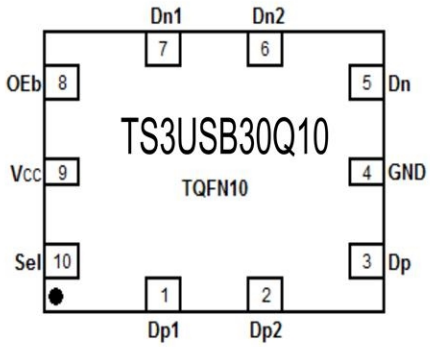
- Cell phone, PDAs, Digital camera, Notebook, LCD Monitor, TV, SET-TOP BOX

## Ordering Information

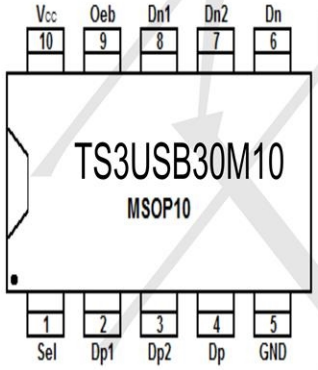
**TP3USB30D10**

M10:MSOP10 Package
Q10:TQFN10 Package

## PIN CONFIGURATION




Top View



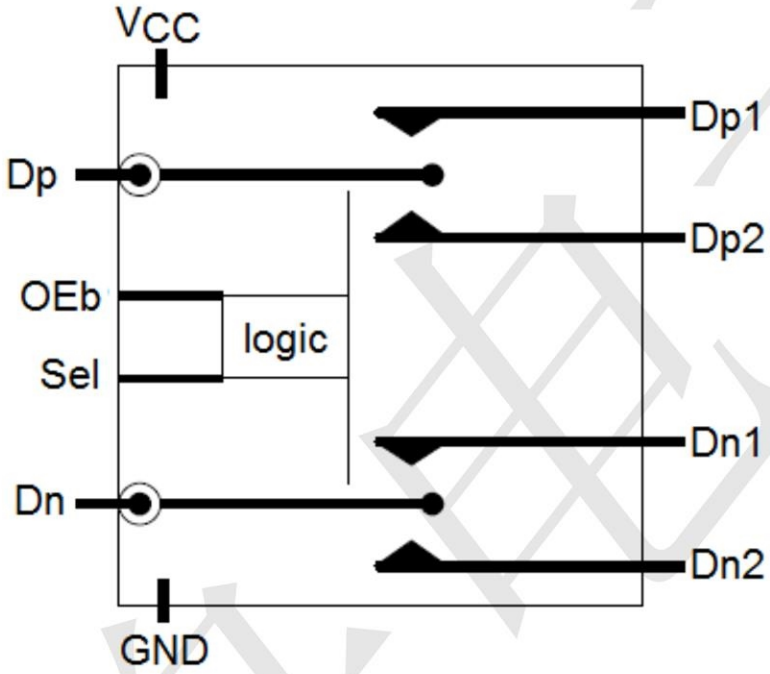

Top View

| Pin # | | Symbol | Type | Function |
|---|---|---|---|---|
| TQFN10 | MSOP10 | | | |
| 1 | 2 | Dp1 | Input / Output | Data Port |
| 2 | 3 | Dp2 | Input / Output | Data Port |
| 3 | 4 | Dp | Input / Output | USB Data BUS |
| 4 | 5 | GND | Ground | Ground |
| 5 | 6 | Dn | Input / Output | USB Data BUS |
| 6 | 7 | Dn2 | Input / Output | Data Port |
| 7 | 8 | Dn1 | Input / Output | Data Port |
| 8 | 9 | OEb | Input | Switch enable |
| 9 | 10 | $V_{CC}$ | PWR | Power Supply |
| 10 | 1 | Sel | Input | Switch select |

## FUNCTION TABLE

| OEb | Sel | Function |
|---|---|---|
| 1 | X | Disconnect |
| 0 | 0 | Dp , Dn=Dp1, Dn1 |
| 0 | 1 | Dp , Dn=Dp2, Dn2 |

## BLOCK DIAGRAM




## Absolute Maximum Ratings

| | |
|---|---|
| $V_{CC}$, DC Supply Voltage | -0.5V~5.5V |
| Dpn / Dnn / Dp / Dn, DC Switch Voltage | -0.5V~$V_{CC}$+0.3V |
| $V_{Oeb}$ / $V_{Sel}$, DC Input Voltage | -0.5V~$V_{CC}$ |
| $I_{(Dpn/Dnn/Dp/Dn)}$, Continuous Current | -50mA~+50mA |
| $I_{PEAK(Dpn/Dnn/Dp/Dn)}$, Peak Current NOTE1 | -100mA ~+100mA |
| $T_A$, Operating Temperature Range | -40℃~85℃ |

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE1: Pulsed at 1ms, 50% duty circle

## Electrical Characteristics

Typical characteristics are at +25°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Analog Switch | | | | | | |
| Analog Signal Range | $V_{Pn}/V_{Nn}/V_p/V_n$ | | 0 | | $V_{CC}$ | V |
| On-Resistance[NOET2] | $R_{ON}$ | $V_{CC}$ = 3V,$V_{SW}$=0.4V, $I_{ON}$=-8mA | | 4.5 | | Ω |
| On-Resistance Match Between Channels[NOTE3] | $\Delta R_{ON}$ | $V_{CC}$ = 3V,$V_{SW}$=0.4V, $I_{ON}$=-8mA | | 0.1 | | Ω |
| Current | | | | | | |
| Source Off Leakage Current | $I_{Pn\ /\ Nn\ (OFF)}$ | $V_{CC}$=3.6V,$V_p/V_n$= 3.6/0.3V, $V_{Pn}/V_{Nn}$=0.3/3.6V | -1 | | 1 | uA |
| Channel on Leakage Current | $I_{Pn\ /\ Nn\ (ON)}$ | $V_{CC}$=3.6V,$V_p/V_n$= 3.6/0.3V, $V_{Pn}/V_{Nn}$=3.6/0.3V | -1 | | 1 | uA |
| POWER OFF leakage current | $I_{OFF}$ | $V_{CC}$ = 0V,$V_{SW}$=0V to 3.6V, Vcontrol=0 or $V_{CC}$ | -1 | | 1 | uA |
| Quiescent supply current | $I_{CC}$ | $V_{CC}$=3V, Vcontrol=0 or $V_{CC}$, $I_{OUT}$=0 | | | 1 | uA |
| Increase in ICC current per control voltage and $V_{CC}$ | $I_{CCT}$ | $V_{CC}$=3.6V, Vcontrol=2.6V | | | 4 | uA |
| Input Leakage Current | $I_{OEb\ /Sel}$ | $V_{OEb\ /\ Sel}$ = 0 or $V_{CC}$ | | | 1 | uA |
| Digital I/O | | | | | | |
| Input Voltage High | $V_{IH}$ | $V_{CC}$ = 3.0 to 3.6V | 1.6 | | | V |
| Input Voltage Low | $V_{IL}$ | $V_{CC}$ = 3.0 to 3.6V | | | 0.5 | V |

NOTE2: Measured by the voltage drop between Dpn/Dnn and Dp/Dn pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (Dpn/Dnn and Dp/Dn ports).

NOTE3: $\Delta R_{ON}= R_{ON(MAX)} - R_{ON(MIN)}$, between Dp and Dn .

## DYNAMIC CHARACTERISTICS

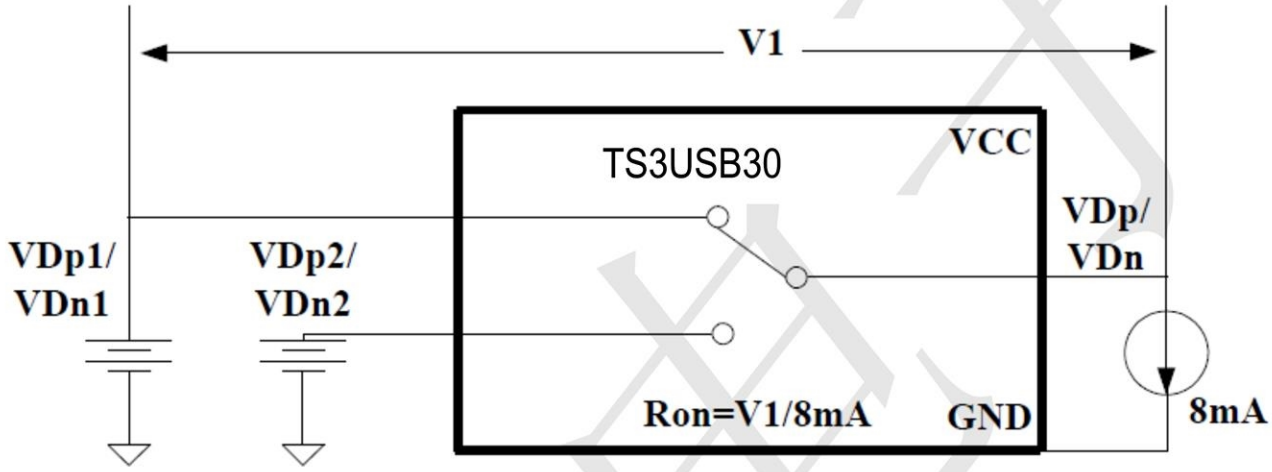
Typical characteristics are at 25°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| DRIVER CHARACTERISTICS | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{CC}$=3.3V, $R_L$=50Ω, $C_L$=5pF, $V_{SW}$=0.8V | | 10 | 30 | ns |
| Turn-Off Time | $t_{OFF}$ | $V_{CC}$=3.3V, $R_L$=50Ω, $C_L$=5pF,$V_{SW}$=0.8V | | 20 | 25 | ns |
| Break-Before-Make Time | $t_{BBM}$ | $V_{CC}$=3.3V, $R_L$=50Ω, $C_L$=5pF,$V_{SW1,2}$=0.8V | 2.0 | 3 | 6.5 | ns |
| Propagation Delay | $t_{PD}$ | $V_{CC}$=3.3V, $R_L$=50Ω, $C_L$=5pF | | 0.2 | | ns |
| CAPACITANCE | | | | | | |
| Control Capacitance | $C_{IN}$ | $V_{CC}$=0V | | 1.5 | | pF |
| ON Capacitance | $C_{ON}$ | $V_{CC}$=3.3V,OE=0V, f=240MHz | | 3.7 | | pF |
| OFF Capacitance | $C_{OFF}$ | $V_{CC}$=3.3V,OE=3.3V, f=240MHz | | 2.0 | | pF |
| APPLICATION CHARACTERISTICS | | | | | | |
| 3dB Bandwidth | $f_{3dB}$ | $V_{CC}$=3.3V,$R_L$=50Ω,$C_L$=0pF | | 720 | | MHz |
| | | $V_{CC}$=3.3V,$R_L$=50Ω,$C_L$=5pF | | 550 | | MHz |
| Off Isolation[NOTE4] | $V_{Iso}$ | $V_{CC}$=3.3V,$R_L$=50Ω,f=250MHz | | -30 | | dB |
| Channel crosstalk | XTALK | $V_{CC}$=3.3V,$R_L$=50Ω,f=250MHz | | -35 | | dB |

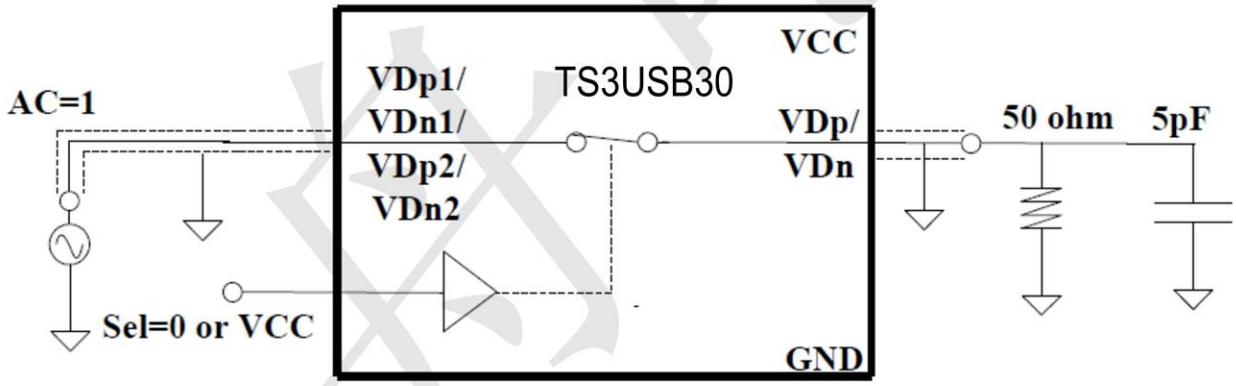
NOTE3: Off Channel Isolation = $20\log_{10}[(V_{P1\backslash P2})/V_P]$ or $20\log_{10}[(V_{N1\backslash N2})/V_N]$

## TEST CIRCUIT

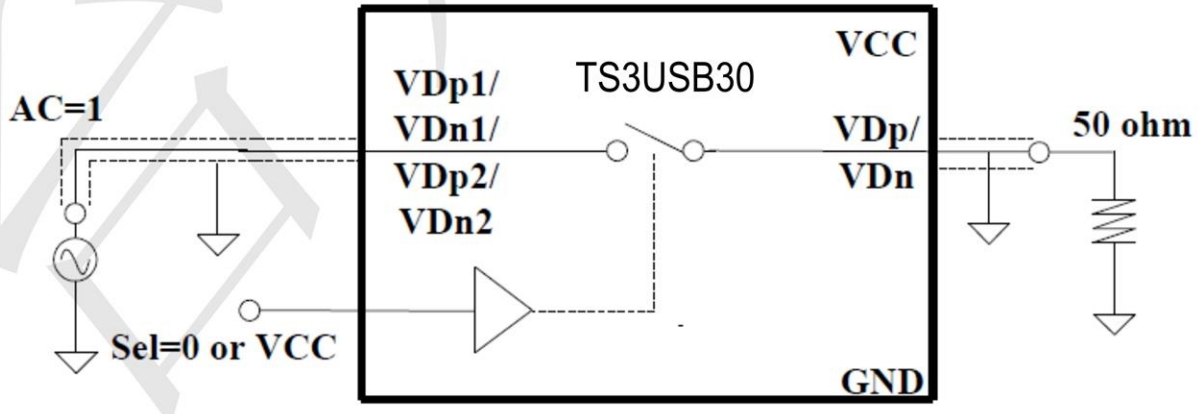
1. Test Circuit for On Resister



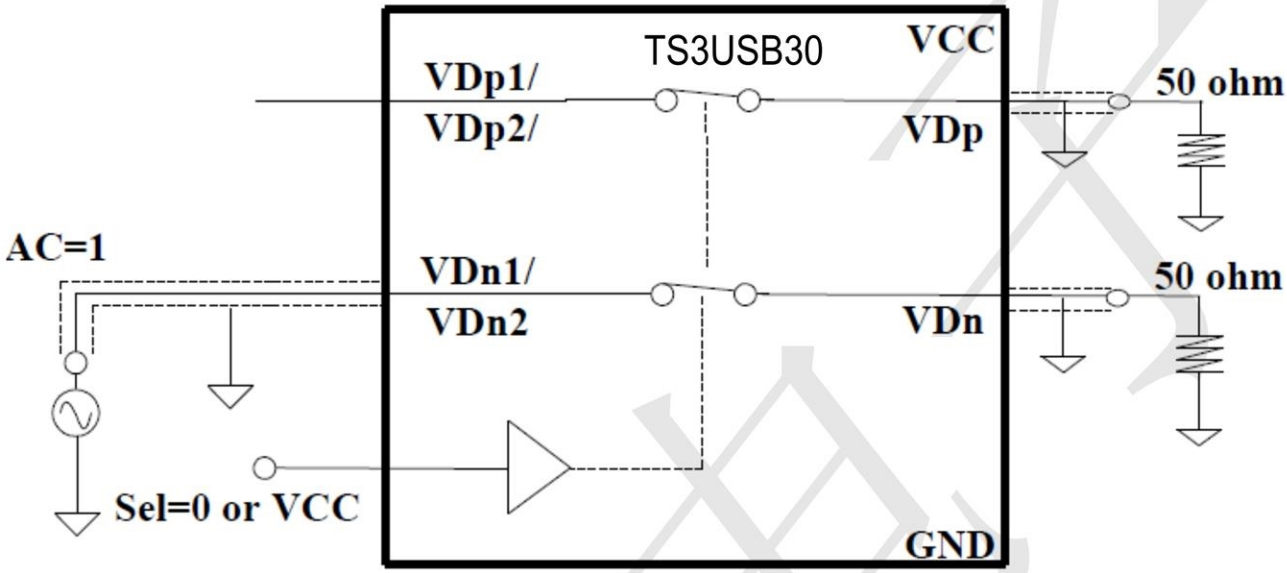

2. Test Circuit for Bandwidth



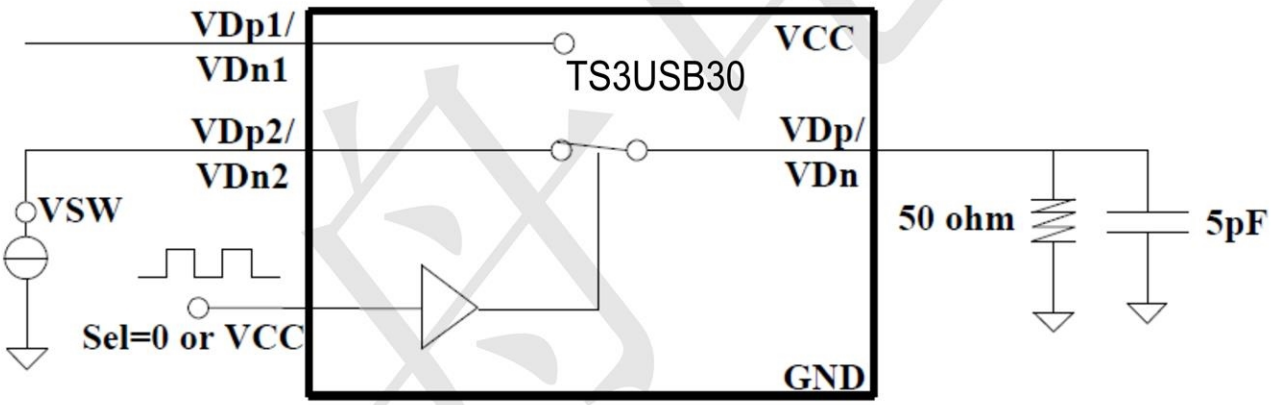

3. Test Circuit for Off Isolation

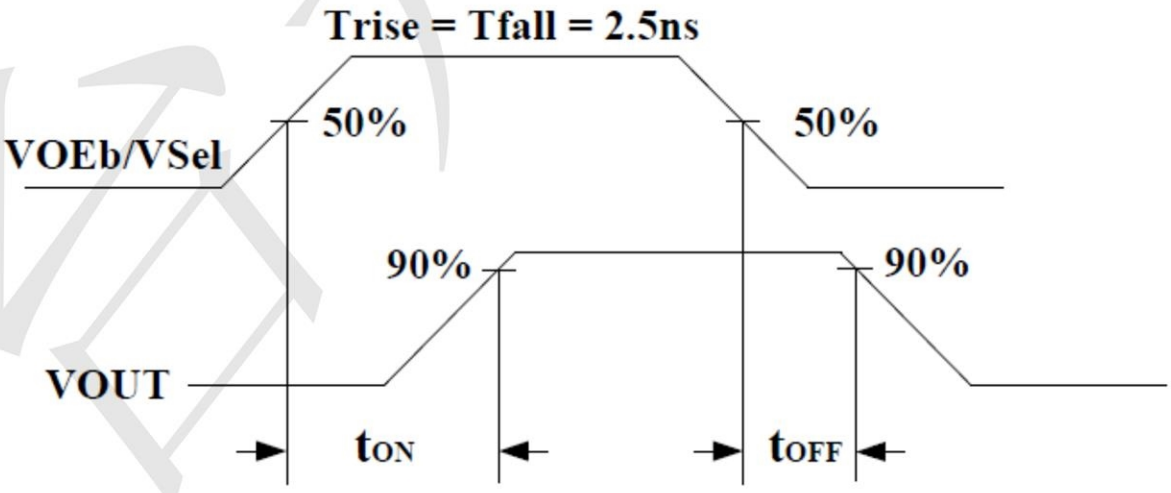


4. Test Circuit for Crosstalk




5. Test Circuit for Switch Times



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