



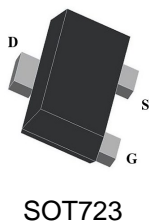
### Product Summary

- \*  $R_{DS(on)} = \text{Typ } 200\text{m}\Omega @ V_{GS} = 4.5\text{V}$
- \*  $R_{DS(on)} = \text{Typ } 250\text{m}\Omega @ V_{GS} = 2.5\text{V}$
- \* Lead free product is acquired
- \* Surface mount package
- \* N-channel switch with low  $R_{DS(on)}$
- \* Operated at low logic level gate drive
- \* ESD protection

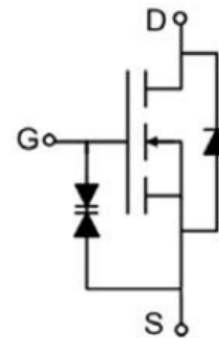
### Application

- \* Load/Power switch
- \* Interfacing, logic switching
- \* Battery management for ultra portable electronics

### Package and Pin Configuration



### Circuit diagram



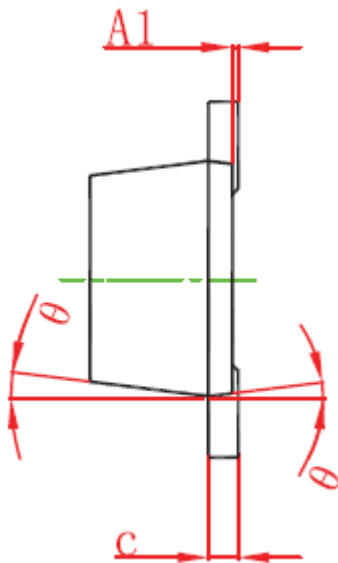
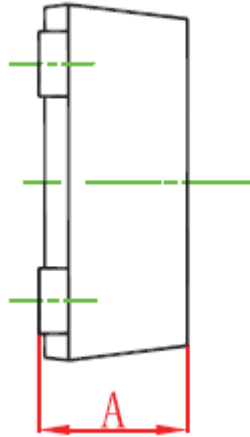
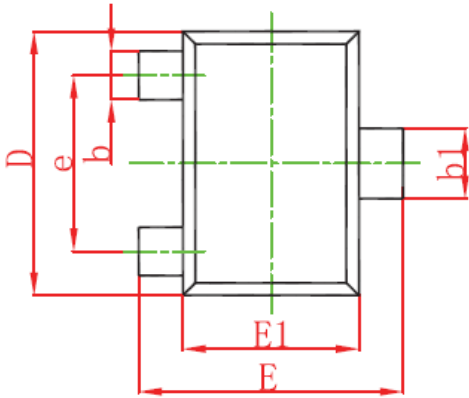
### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	V
Continuous Drain Current @25°C (note 1)	$I_D$	0.95	A
Pulsed Drain Current @25°C (tp=10 $\mu\text{s}$ )	$I_{DM}$	1.5	A
Diode Continuous Forward Current	$I_S$	0.5	A
Power Dissipation @25°C (note 1)	$P_D$	150	mW
Thermal Resistance from Junction to Ambient (note 1)	$R_{\theta JA}$	820	$^\circ\text{C}/\text{W}$
Maximum Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

**Electrical Characteristics (  $T_A = 25^\circ\text{C}$  unless otherwise noted )**

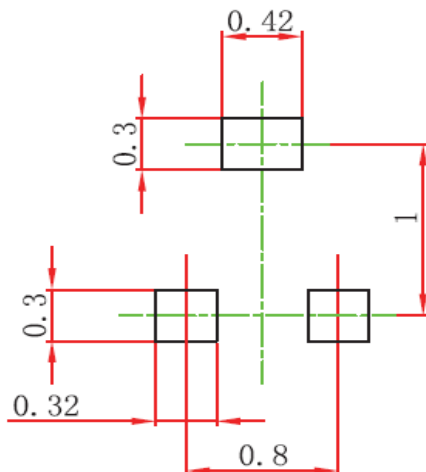
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Drain-to-Source Leakage Current	$I_{DS}$	$V_{DS} = 16V, V_{GS} = 0V$			1	$\mu A$
Gate-Body Leakage Current	$I_{GS}$	$V_{GS} = \pm 8V, V_{DS} = 0V$			$\pm 10$	$\mu A$
Gate Threshold Voltage (note 2)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.45	0.65	1	V
Static Drain-Source On-Resistance (note 2)	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 0.55A$		200	350	$m\Omega$
		$V_{GS} = 2.5V, I_D = 0.50A$		250	420	$m\Omega$
		$V_{GS} = 1.8V, I_D = 0.35A$		310	480	$m\Omega$
Body-diode forward voltage	$V_{SD}$	$I_S = 0.35A, V_{GS} = 0V$		0.9	1.5	V
Dynamic Characteristics (note 4)						
Total Gate Charge	$Q_g$	$V_{DS} = 10V$		1.15		nC
Gate-Source Charge	$Q_{gs}$	$I_D = 0.55A$		0.15		nC
Gate-Drain Charge	$Q_{gd}$	$V_{GS} = 4.5V$		0.23		nC
Input capacitance	$C_{iss}$	$V_{DS} = 10V$		50		pF
Output capacitance	$C_{oss}$	$V_{GS} = 0V$		13		pF
Reverse transfer capacitance	$C_{rss}$	$f = 100KHz$		8		pF
Turn-on delay time (note 3)	$t_{d(on)}$	$V_{GS} = 4.5V$		22		nS
Turn-on rise time (note 3)	$t_r$	$V_{DS} = 10V$		80		nS
Turn-off delay time (note 3)	$t_{d(off)}$	$I_D = 0.55A$		700		nS
Turn-off fall time (note 3)	$t_f$	$R_{GEN} = 6\Omega$		380		nS

**SOT723 - Package Outline Drawing**



Symbol	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.43	0.50	0.017	0.020
A1	0.00	0.05	0.000	0.002
b	0.17	0.27	0.007	0.011
b1	0.27	0.37	0.011	0.015
c	0.08	0.15	0.003	0.006
D	1.15	1.25	0.045	0.049
E	1.15	1.25	0.045	0.049
E1	0.75	0.85	0.03	0.033
e	0.8 typ		0.031 typ	
θ	7° REF		7° REF	

**Suggested Land Pattern**



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