1 SCOPE

1.1 CONTENT

This specification covers the requirements for application of the High Speed IO connector system. This connector-system interconnects a cable and a printed circuit board.

2 REFERENCE DOCUMENTATION

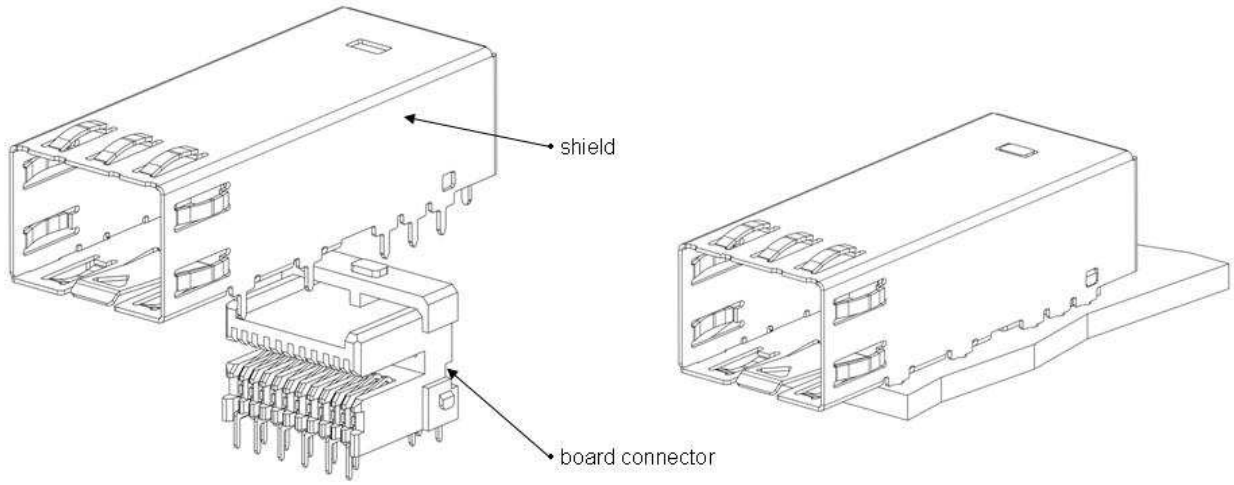
2.1 For the product specification of the High Speed IO connector system see:
Product Specification: 108-19376.

2.2 For configuration details see customer drawings:

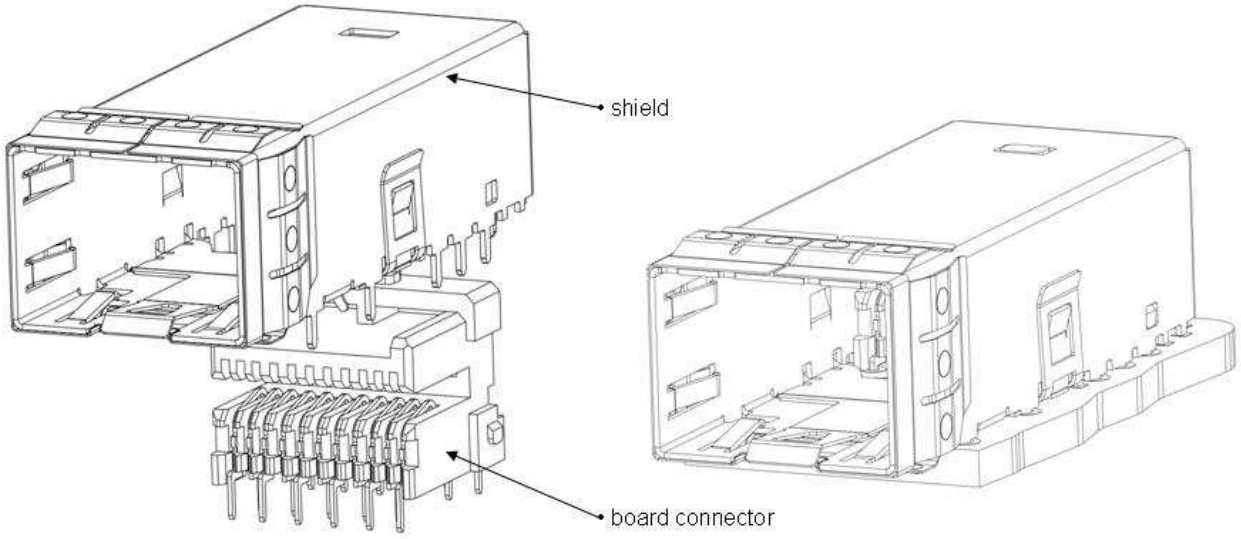
- C-2042853 Board Connector (version 1)
- C-1551967 Board Connector (version 2)
- C-2042847 Cable Plug
- C-2173775 Enhanced Cable Plug

3 NOMENCLATURE

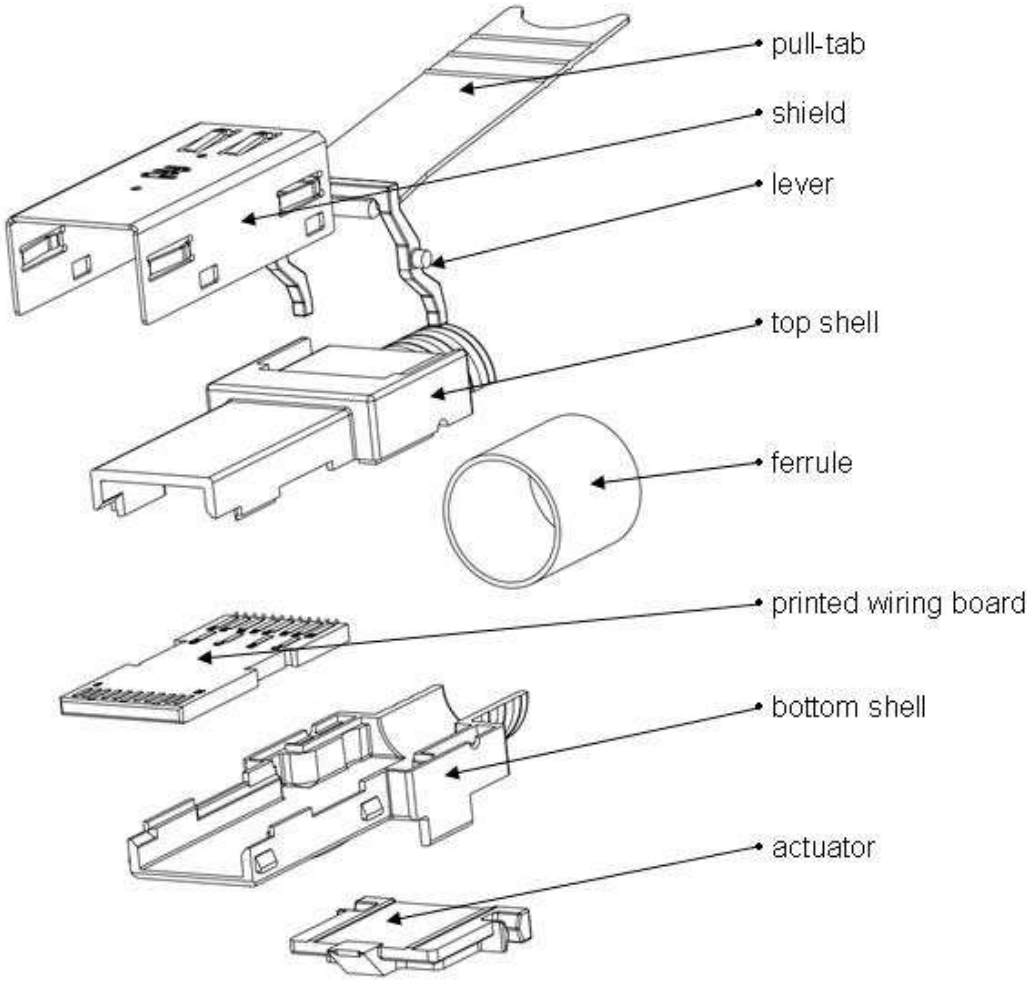
3.1 HSIO boardconnector v1

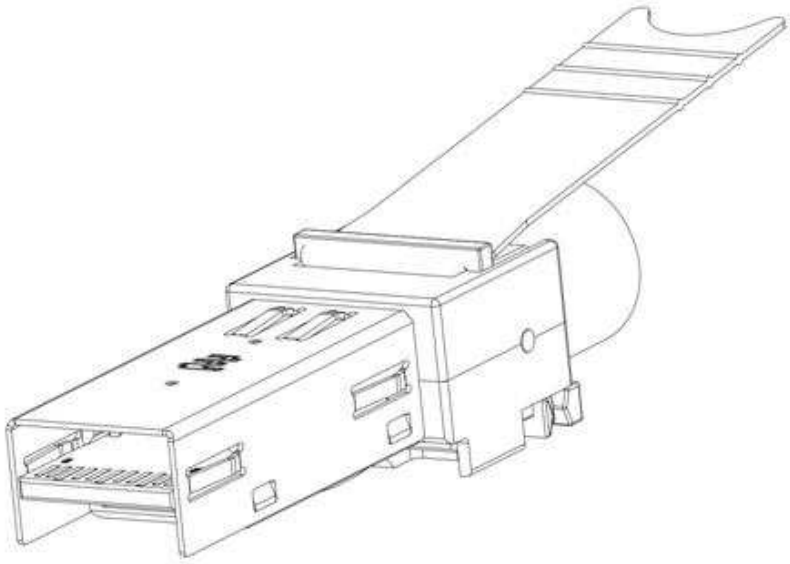


3.2 HSIO boardconnector v2

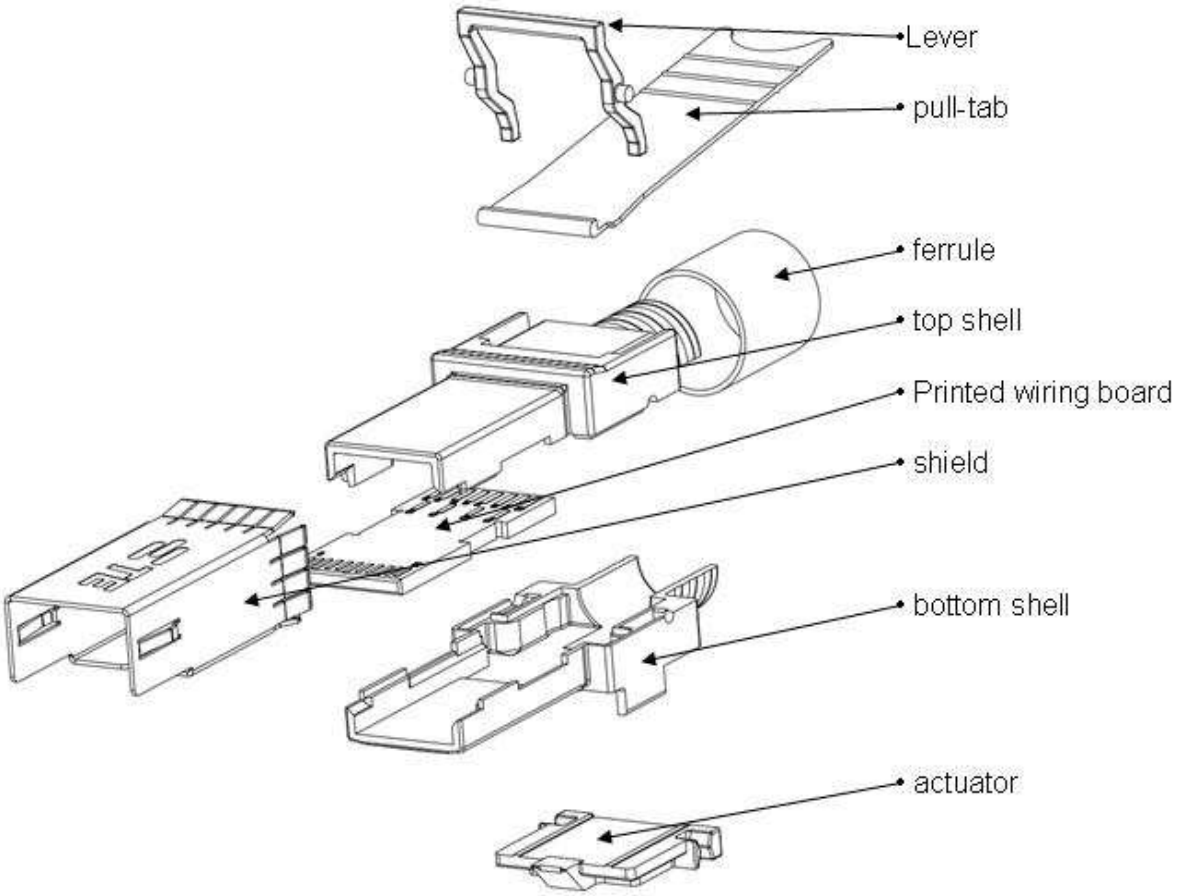


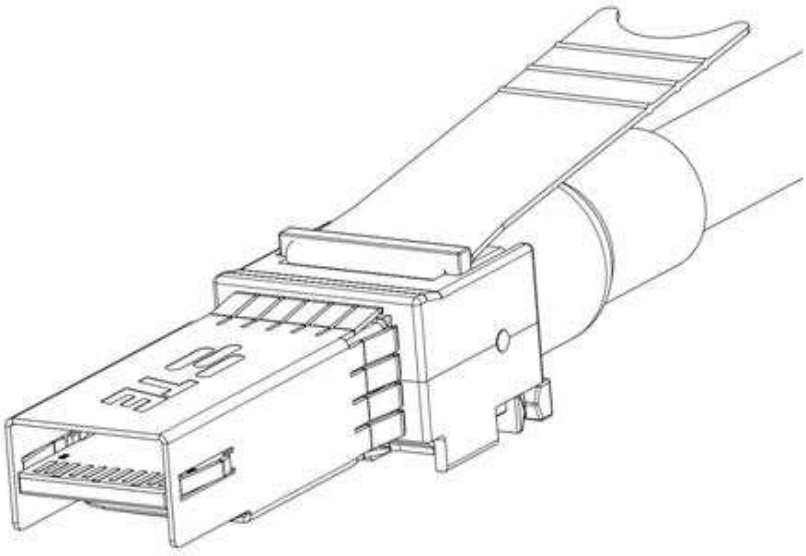
3.3 HSIO Cable Plug





3.4 HSIO Enhanced Cable Plug





4 ASSEMBLY

4.1 The board connector has to be extended for min 1 mm thru the front plate for proper working of the latch mechanism. See figure 2

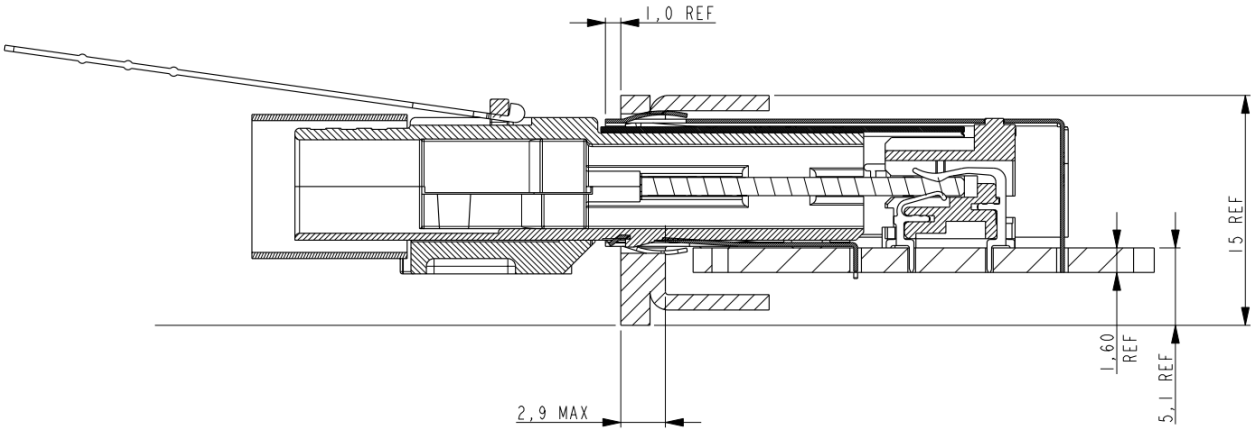


Figure 2

4.2 The cable connector will be released from the board connector by pulling the tab at top of the connector.

5 FRONT PANEL

5.1 CUTOUT

See figure 3 for the recommended bezel cutout (min pitch)

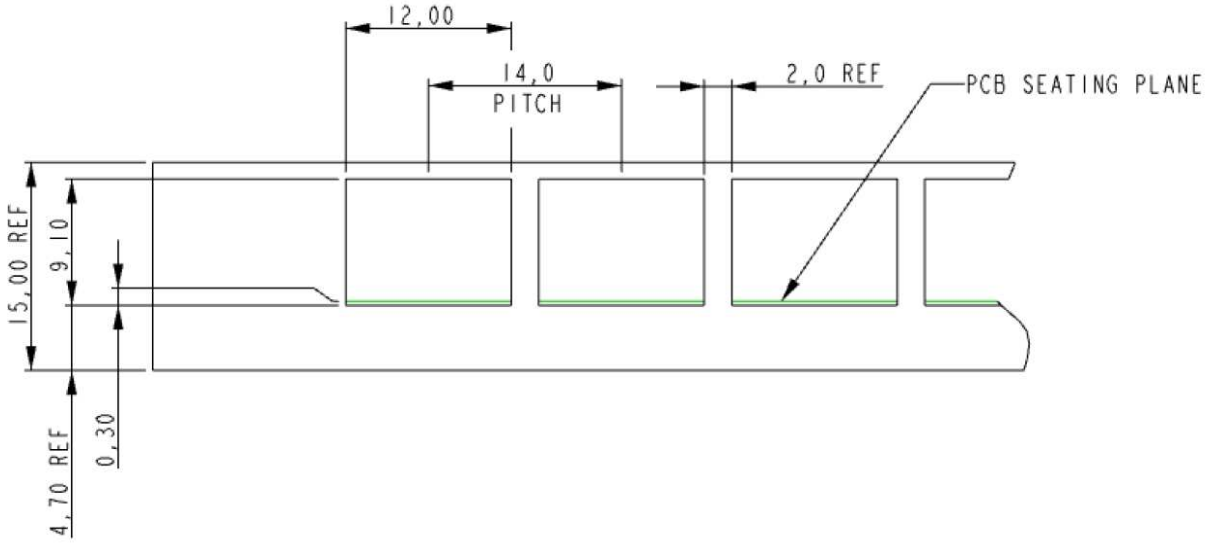


Figure 3

6 PC BOARD CONNECTOR FOOTPRINT

6.1 Pin-In-Paste technology is used to mount the connector on the board.

The footprint is according to the below drawing:

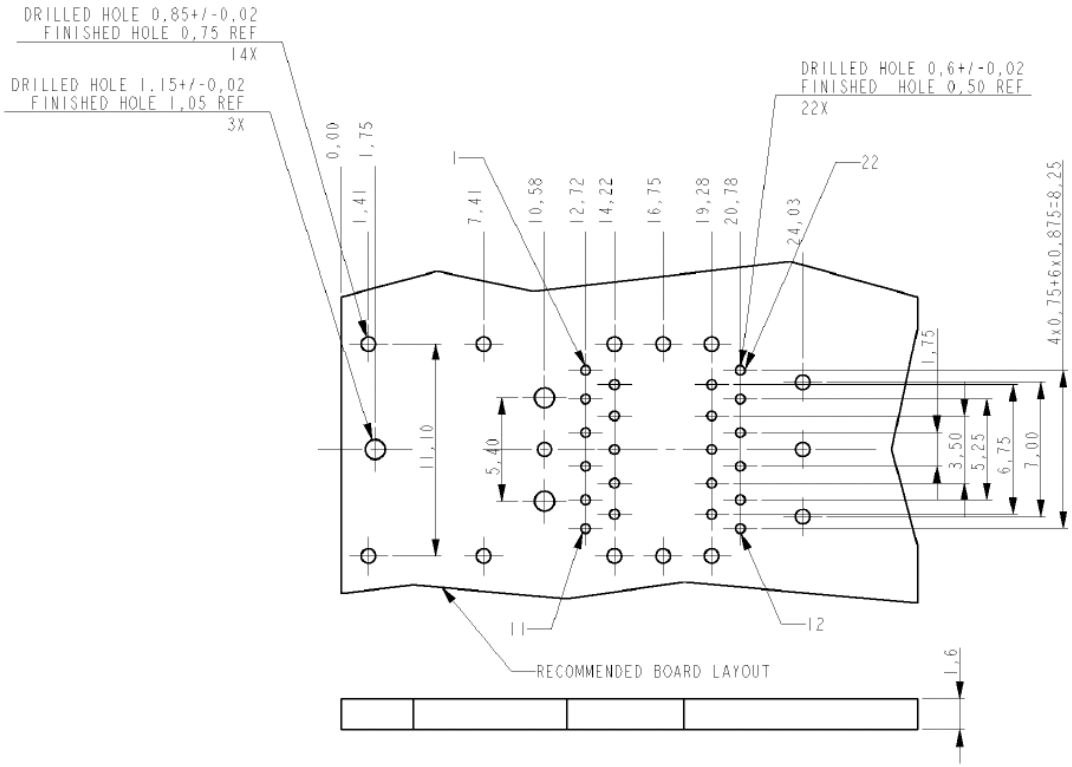


Figure 4. Recommended PCB layout

Horizontal signal pin pitch = 1.5 mm (rotation refer to above)
Vertical signal pin pitch = 1.75 mm (rotation refer to above)

Please refer to the customer drawing of board connector (C -2042853 for version 1, C-1551966 for version 2) for more details and the latest update of dimensions.

6.1 Pin Numbering and Signals

On the PCB the pin numbering and signals are defined according to below. This is the recommended configuration for maximum high speed performance and signal density.

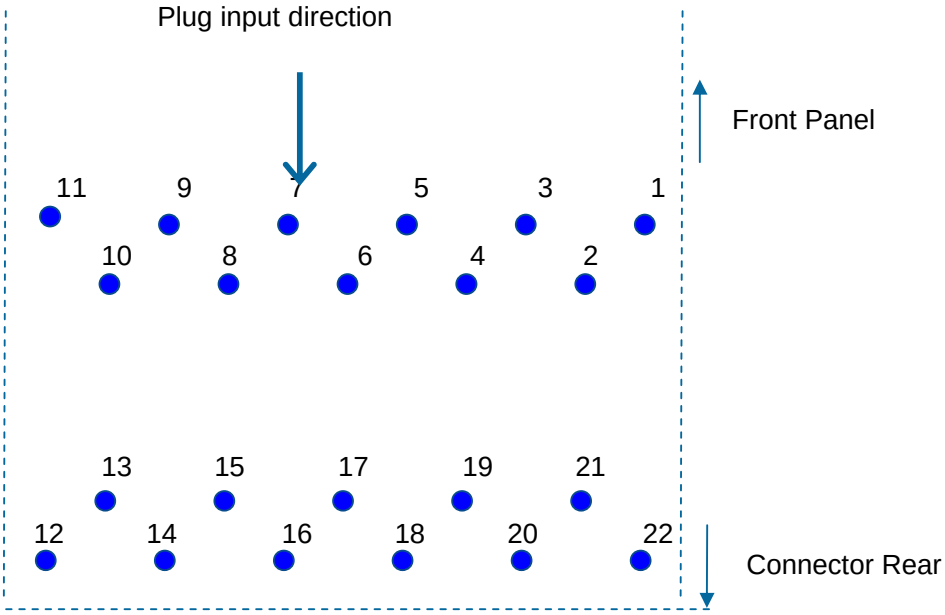


Figure 5. Signal numbering is seen from the top side of the PCB

Pin	Signal Name
1-2	100 Mbit/s
3	GND
4-5	1 Gbit/s
6	GND
7-8	1 Gbit/s
9	GND
10-11	100 Mbit/s
12-13	100 Mbit/s
14	GND
15-16	10 Gbit/s
17	GND
18-19	10 Gbit/s
20	GND
21-22	100 Mbit/s

Table 1. Pin configuration

6.2 Footprint

The hole placement of the HSIO footprint is designed to give optimal signal isolation but still keep a small total width of the connector with small pin-to-pin pitch.

For close connector-to-connector pitch, signal routing might require to route traces between the ground pins and the low speed signals on pin 12 and pin 22. The diagonal routing between the ground pins and pin 12 and 22 is detailed with minimum distances and minimum routing channels according to chapter 7.2.

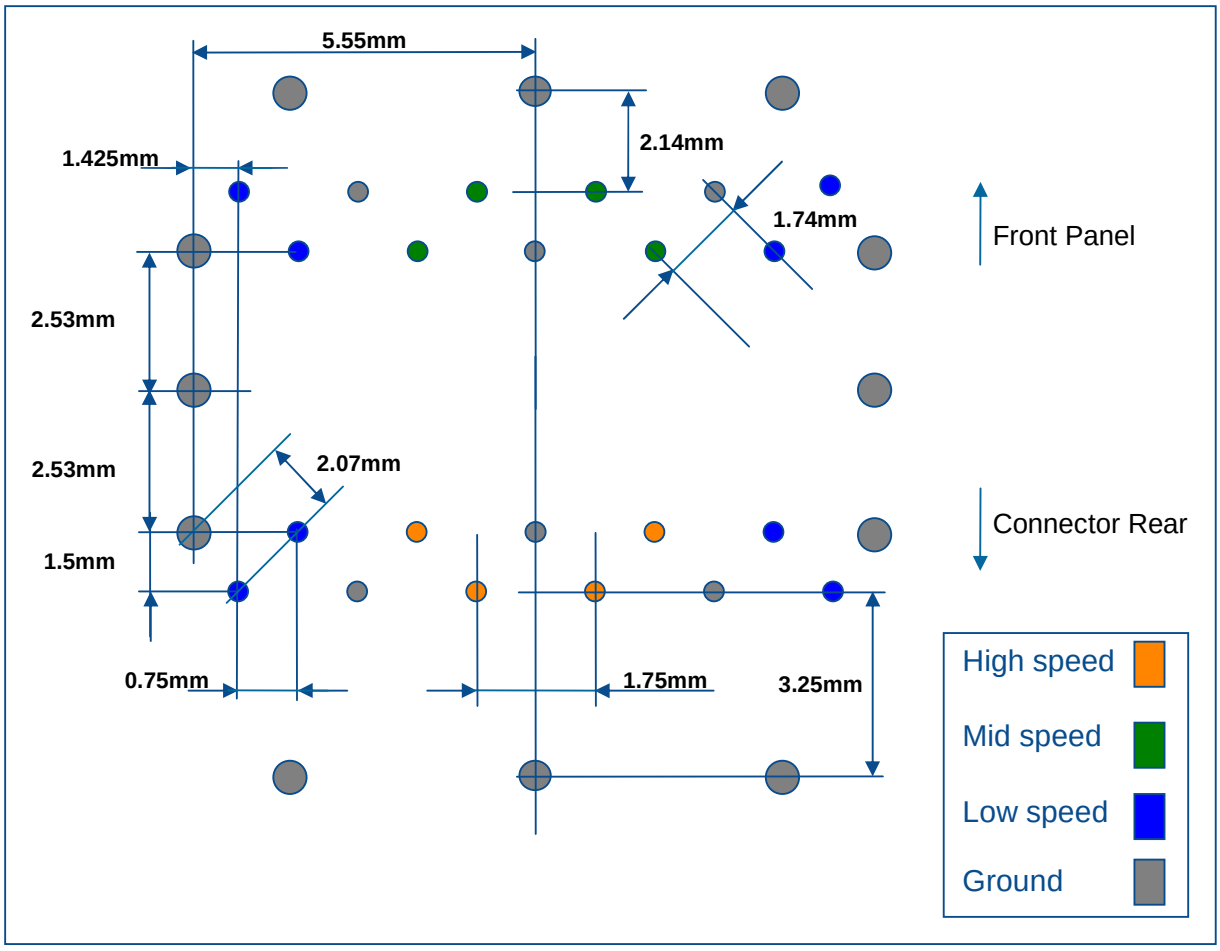


Figure 6. Top side view of the PCB.

6.3 Antipad design

The antipad design for the high speed differential pairs is important for impedance matching in high speed applications.

The antipad will decrease the capacitive coupling from the pads to the ground planes and will give a better 100 Ω impedance matching for the pads.

Two suggestions for the antipad design are shown below.

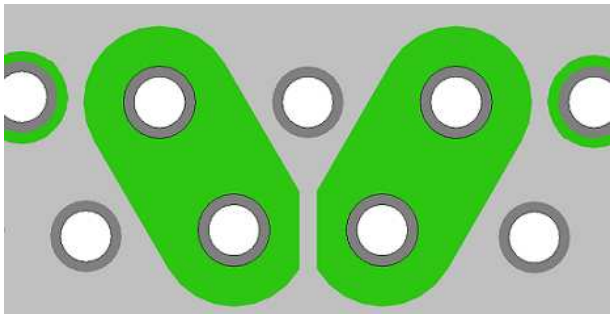


Figure 7. Oval shaped antipads

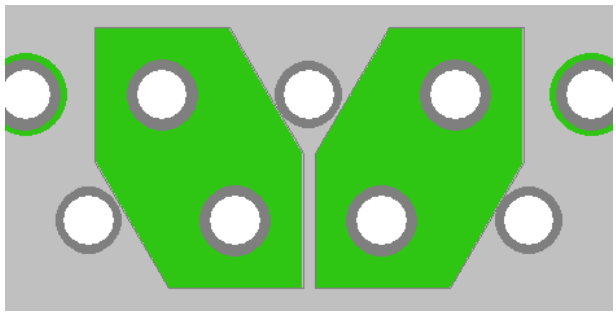


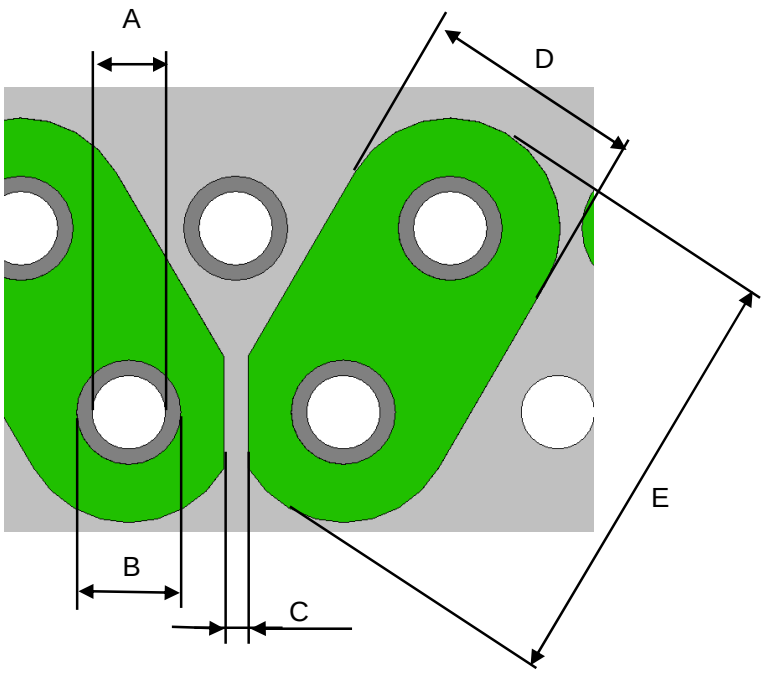
Figure 8. Polygon antipads

The ground shield plane between the antipads has been found to be sufficient with a width of 0.15 mm. However, increasing the ground plane when possible improves the isolation.

6.4 Dimensions

6.4.1 Dimensions of oval antipads

The dimensions of the suggested oval antipads are detailed below.



A : 0.65 mm (drill size)

B : 0.90 mm

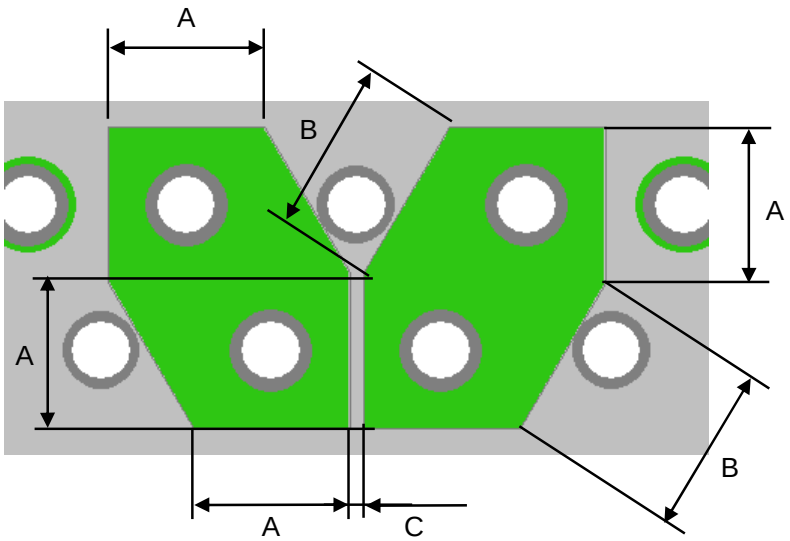
C : 0.15 mm

D : 1.60 mm

Figure 9. Dimensions of oval antipads

6.4.2 Dimensions of polygon antipads

The dimensions of the suggested polygon antipads are detailed below.



A : 1.60 mm

B : 2.48 mm

C : 0.15 mm

Figure 10. Dimensions of polygon antipads

7 ROUTING

It is recommended that the routing from the High Speed pairs is done on the bottom side or near bottom side of the PCB to minimize the via hole stub.

Ground planes should always be used between the different layers. This is important to get the required isolation so that the crosstalk noise is minimized.

7.1 Routing recommendation

The below suggested routing is based on a narrow connector to connector pitch. However, if there is space on each side of the connector or to the front, other solutions will be possible.

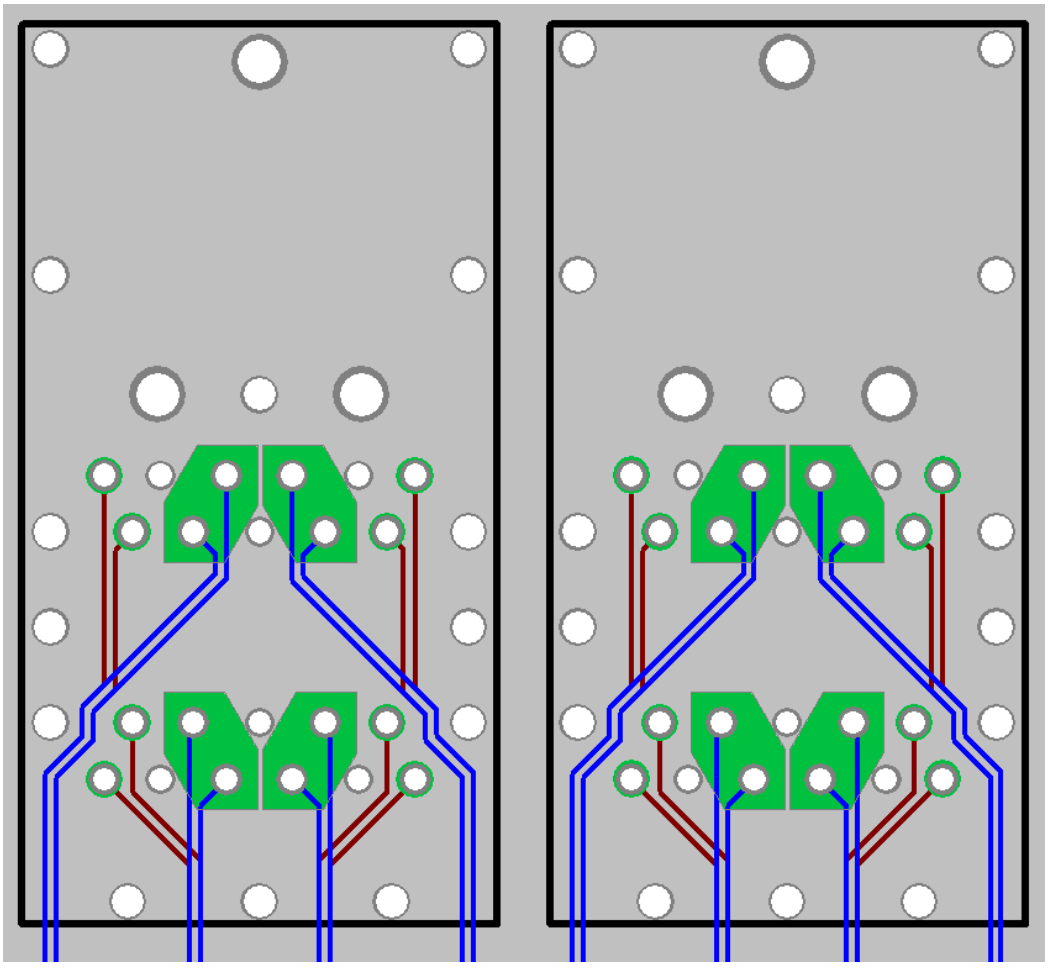


Figure 11. Routing recommendation, top side view of the PCB

7.2 Routing channel

In the suggested routing recommendation the routing channel with minimum distance is between the edge ground pins and the close by low speed signal pins, as detailed in the figure below. In the following the diagonal routing between the ground pins and pin 12 and 22 is detailed.

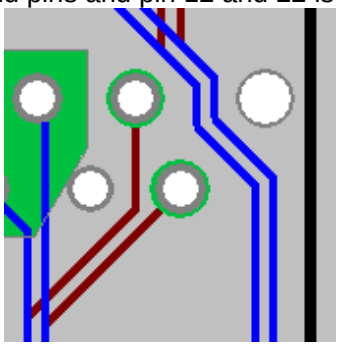
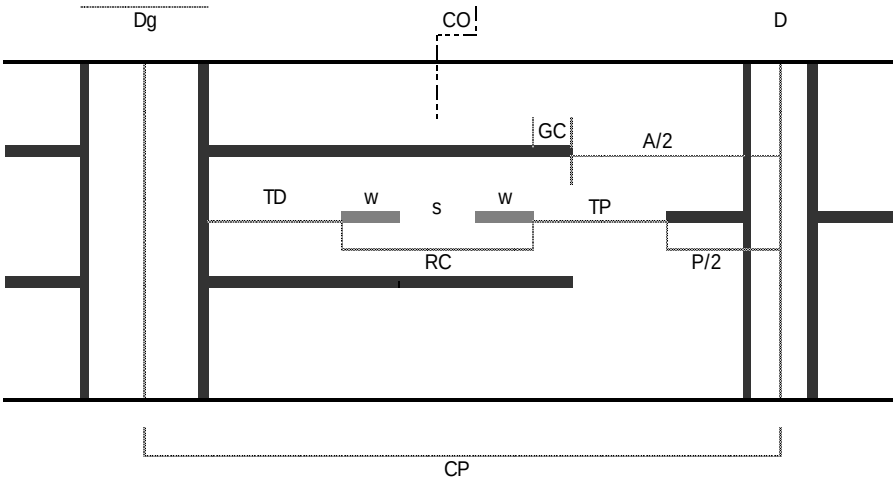


Figure 12. Minimum routing channel, routing recommendation

The routing channel in the inner layer will look similar to the figure below and the tables in 7.2.1 gives an overview of the possible routing channels. The calculated values in the table 2 and 3 in chapter 7.2.1 are based on certain values for pad, anti-pad and trace ground coverage.



CP	= Column Pitch	D	= Drill diameter
P	= Pad diameter	CO	= Centre line Offset
A	= Antipad diameter	RC	= Routing Channel
GC	= Ground Coverage	h	= dielectric height
TP	= Trace to Pad distance	w	= trace width
TD	= Trace to Drill distance	s	= trace separation
Dg	= Ground pad diameter		

RC = CP - A - 2GC + 2CO
TP = A/2 - P/2 + GC
TD = CP/2 -Dg/2 - RC/2 - CO

Figure 13. Routing channel distance overview

7.2.1 Routing channel calculation

General	Center Line Pitch **(CP)**	2,00	mm	
	Drill Diameter (signal) **(D)**	0,60	mm	
	Drill Diameter (GND) **(Dg)**	0,85	mm	
	Centre Line Offset **(CO)**	0	µm	

Property	Pad Technology	Pad Diameter **(P)**	Anti-Pad Diameter **(A)**	Ground Coverage **(GC)**	Trace-to-Pad **(TP)** (*)	Trace-to-Drill **(TD)** (*)	Routing Channel **(RC)**
Units		mm	mm	µm	mm	mm	mm
	D + 0.25mm (D + 10mil)	0,85	1,00	125	0,200	0,200	0,75
			1,05	100	0,200	0,200	0,75
			1,05	125	0,225	0,225	0,70
			1,20	75	0,250	0,250	0,65
			1,20	100	0,275	0,275	0,60
			1,20	125	0,300	0,300	0,55
	D + 0.30mm (D + 12mil)	0,90	1,05	125	0,200	0,225	0,70
			1,10	100	0,200	0,225	0,70
			1,10	125	0,225	0,250	0,65
			1,15	75	0,200	0,225	0,70
			1,15	100	0,225	0,250	0,65
			1,15	125	0,250	0,275	0,60
			1,20	75	0,225	0,250	0,65
			1,20	100	0,250	0,275	0,60
			1,20	125	0,275	0,300	0,55
			1,25	75	0,250	0,275	0,60
			1,25	100	0,275	0,300	0,55
			1,25	125	0,300	0,325	0,50
	D + 0.35mm (D + 14mil)	0,95	1,10	125	0,200	0,250	0,65
			1,15	100	0,200	0,250	0,65
			1,20	75	0,200	0,250	0,65
			1,20	100	0,225	0,275	0,60
			1,20	125	0,250	0,300	0,55
			1,25	75	0,225	0,275	0,60
			1,25	100	0,250	0,300	0,55
			1,25	125	0,275	0,325	0,50

- Configurations are shown for Ground Coverage (GC) values 75, 100 and 125 µm
- Configurations are shown for TP >= 0.20mm and TD>=0.20mm

(*) Assuming trace edge coincides with edge of routing channel

Table 2. Signal pin drill diameter 0.60 mm

General	Center Line Pitch **(CP)**	2,00	mm				
	Drill Diameter (signal) **(D)**	0,65	mm				
	Drill Diameter (GND) **(Dg)**	0,85	mm				
	Centre Line Offset **(CO)**	0	µm				
Property	Pad Technology	Pad Diameter **(P)**	Anti-Pad Diameter **(A)**	Ground Coverage **(GC)**	Trace-to-Pad **(TP)** (*)	Trace-to-Drill **(TD)** (*)	Routing Channel **(RC)**
Units		mm	mm	µm	mm	mm	mm
	D + 0.25mm (D + 10mil)	0,90	1,05	125	0,200	0,225	0,70
			1,10	100	0,200	0,225	0,70
			1,10	125	0,225	0,250	0,65
			1,20	75	0,225	0,250	0,65
			1,20	100	0,250	0,275	0,60
			1,20	125	0,275	0,300	0,55
	D + 0.30mm (D + 12mil)	0,95	1,10	125	0,200	0,250	0,65
			1,15	100	0,200	0,250	0,65
			1,15	125	0,225	0,275	0,60
			1,20	75	0,200	0,250	0,65
			1,20	100	0,225	0,275	0,60
			1,20	125	0,250	0,300	0,55
			1,25	75	0,225	0,275	0,60
			1,25	100	0,250	0,300	0,55
			1,25	125	0,275	0,325	0,50
	D + 0.35mm (D + 14mil)	1,00	1,15	125	0,200	0,275	0,60
			1,20	100	0,200	0,275	0,60
			1,20	125	0,225	0,300	0,55
			1,25	75	0,200	0,275	0,60
			1,25	100	0,225	0,300	0,55
			1,25	125	0,250	0,325	0,50
			1,30	75	0,225	0,300	0,55
			1,30	100	0,250	0,325	0,50
			1,30	125	0,275	0,350	0,45
	- Configurations are shown for Ground Coverage (GC) values 75, 100 and 125 µm						
	- Configurations are shown for TP >= 0.20mm and TD>=0.20mm						
	(*) Assuming trace edge coincides with edge of routing channel						

Table 3. Signal pin drill diameter 0.65 mm

8 IMPEDANCE

The impedance of the differential pairs in the cable and connector system is designed for 100 Ω. This impedance should be kept in the PCB trace routing and the legs of the differential pairs should always be routed together.

8.1 Footprint

The overall footprint design of the PCB connector might be a big contributor to return loss as the footprint often is more capacitive than the traces. Keep the vias and the pads as small as possible for best impedance matching.

In high speed applications the antipad design is important for the footprint impedance.

8.2 Trace width

The trace widths should be calculated for 100 Ω differential pair impedance. Take into account PCB manufactured normal process variations that can affect the trace impedance.

9 LAYER STACKUP

Bottom or near bottom layer routing is recommended with the HSIO connector.
It is not recommendable to use top layer routing with the HSIO connector for high speed applications.
The pin-in-paste via will result in a via stub which will have a negative effect on the footprint performance.

10 10 REQUIREMENTS

10.1 CONNECTOR PACKAGING , STORAGE AND HANDLING

The board connectors are packed in embossed tape and reel, shipped in a box. Boxes should remain unopened until ready for use to prevent contamination and damage to the connector parts. They should be used on a first-in/ first-out basis to prevent possible storage contamination.

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