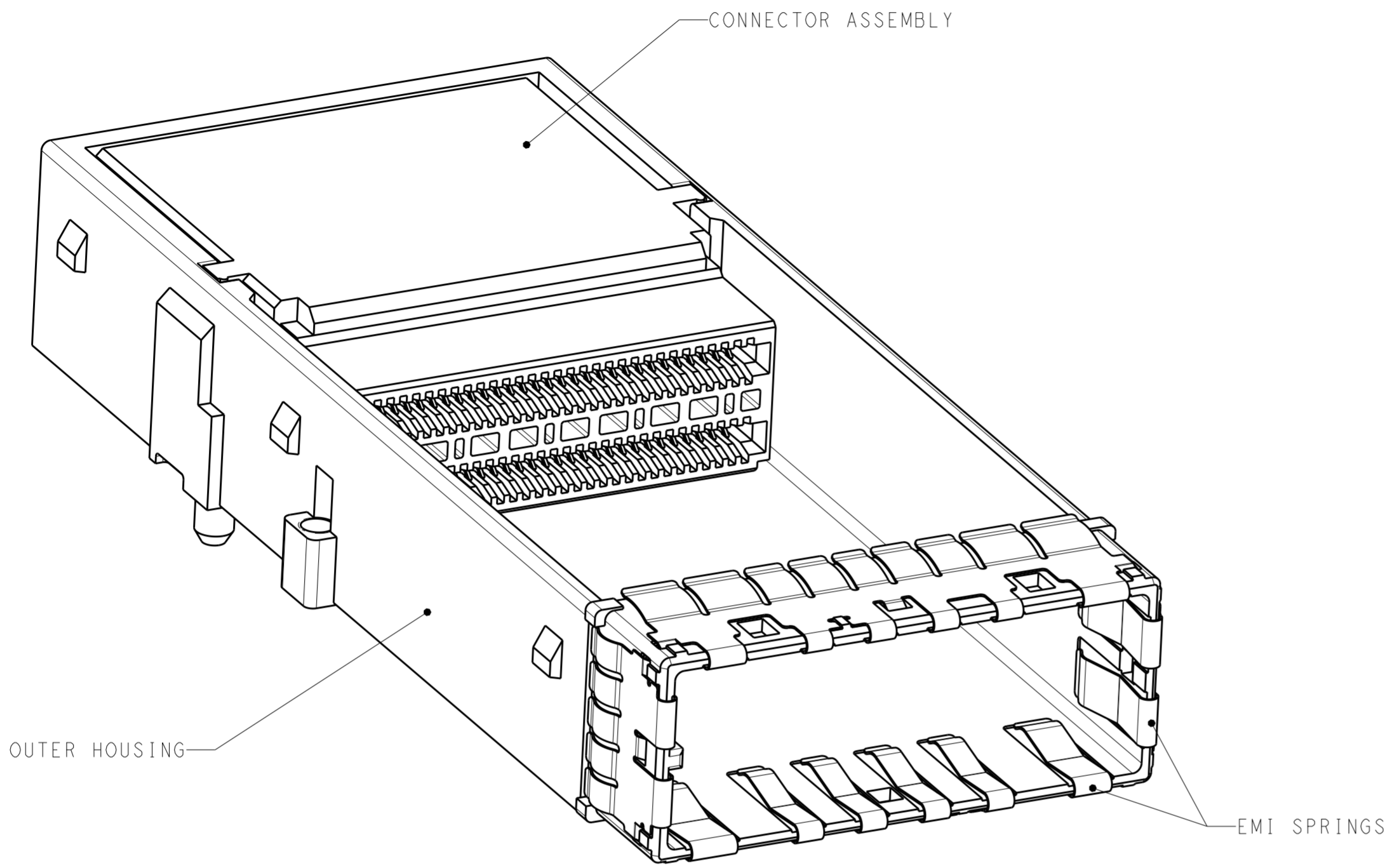



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REVISIONS				
P	LTR	DESCRIPTION	DATE	APVD
	A	RELEASED PER ECO-17-017419	28NOV2017	MS JW



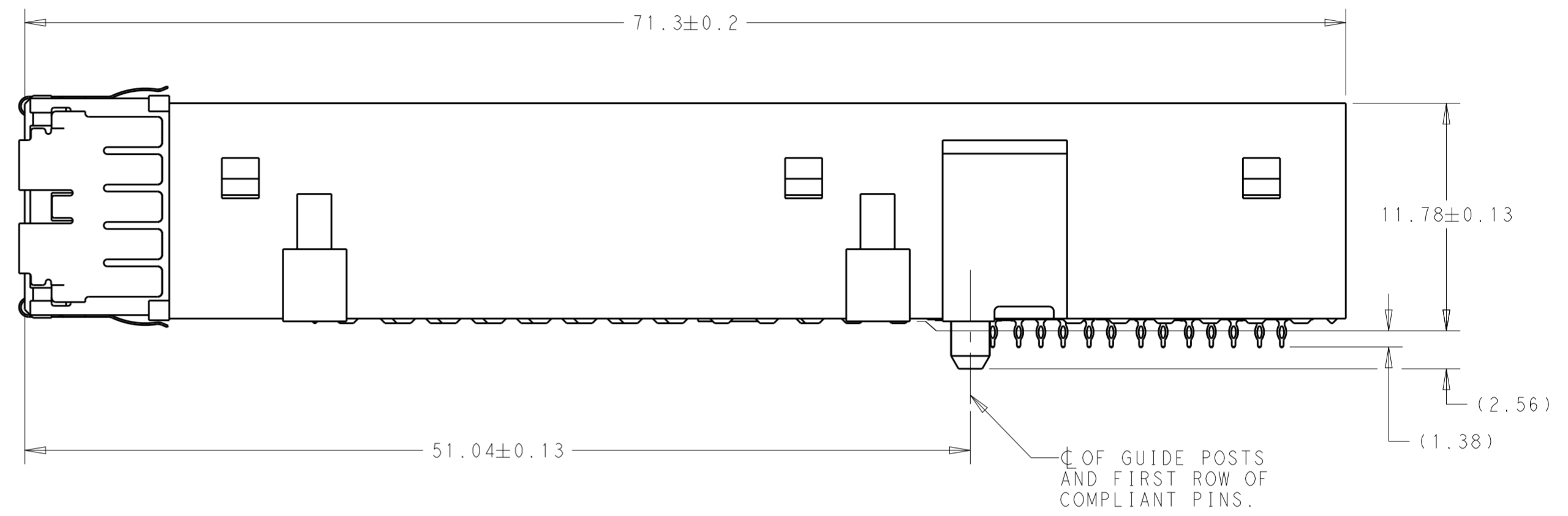
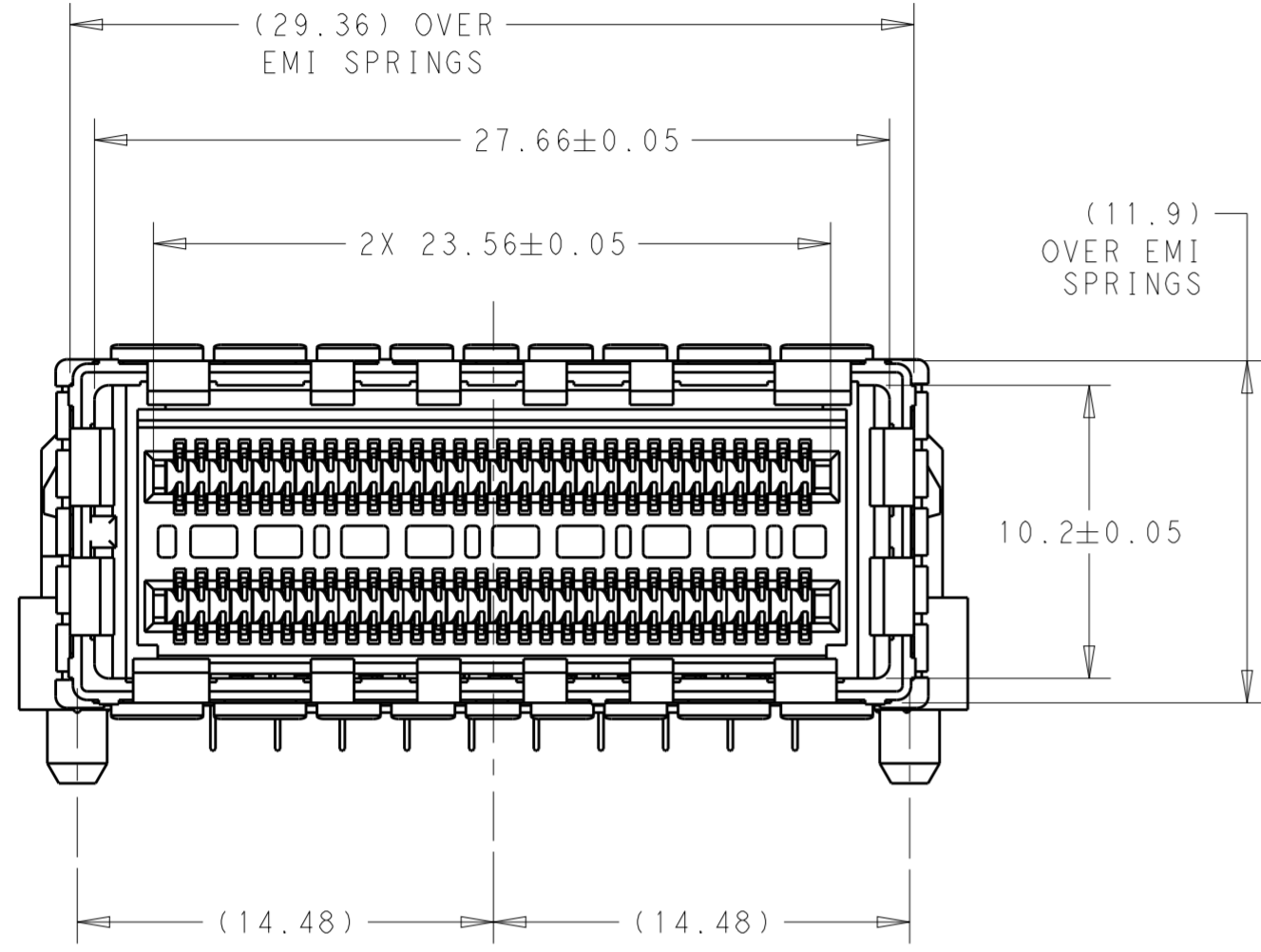
1. MATERIALS:
 OUTER HOUSING - NICKEL PLATED ZINC ALLOY PER ASTM B 240.
 CONNECTOR HOUSINGS - LCP, UL 94V-0 RATED.
 CHICKLETS - LCP, UL 94V-0 RATED.
 CONTACTS - PHOSPHOR BRONZE.
 EMI SPRINGS - COPPER ALLOY.
2. CONTACT FINISH:
 CONFORMS TO THE REQUIREMENTS OF TYCO ELECTRONICS PRODUCT SPECIFICATION 108-32065, BASED ON EIA/ECA-364-1000.01A, (CONTROLLED ENVIRONMENT APPLICATIONS) ON MATING INTERFACES. TIN ON COMPLIANT PINS.
3. PCB THICKNESS 1.57 MINIMUM.
4. FOR HOLE SIZE AND PLATINGS, SEE APPLICATION SPEC 114-32114.
5. CROSS HATCHED AREA INDICATES REQUIRED CONDUCTIVE AREA ON SURFACE OF PCB. NO COMPONENTS OR TOP SIDE SURFACE TRACES ALLOWED IN THIS AREA.
6. MOUNTING HARDWARE REQUIRED:
 3X M2X0.4 - SCREW LENGTH = PCB THICKNESS + (2 TO 4).

2311882-1
 PART NUMBER

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DIMENSIONS: mm		CHK J. WESTMAN 07NOV2016																
TOLERANCES UNLESS OTHERWISE SPECIFIED:		APVD J. WESTMAN 07NOV2016	NAME RECEPTACLE ASSEMBLY, PCIe OPTIMIZED, TYPE 2, CDFP															
<table border="0"> <tr> <td>0 PLC</td> <td>±0.1</td> </tr> <tr> <td>1 PLC</td> <td>±0.1</td> </tr> <tr> <td>2 PLC</td> <td>±0.1</td> </tr> <tr> <td>3 PLC</td> <td>±0.1</td> </tr> <tr> <td>4 PLC</td> <td>±0.1</td> </tr> <tr> <td>ANGLES</td> <td>±</td> </tr> <tr> <td>FINISH</td> <td></td> </tr> </table>		0 PLC	±0.1	1 PLC	±0.1	2 PLC	±0.1	3 PLC	±0.1	4 PLC	±0.1	ANGLES	±	FINISH		PRODUCT SPEC 108-32065	SIZE A2	
0 PLC	±0.1																	
1 PLC	±0.1																	
2 PLC	±0.1																	
3 PLC	±0.1																	
4 PLC	±0.1																	
ANGLES	±																	
FINISH																		
MATERIAL SEE NOTES		APPLICATION SPEC 114-32114	CAGE CODE -	DRAWING NO. C-2311882														
		WEIGHT -	RESTRICTED TO -															
		CUSTOMER DRAWING	SCALE 4:1	SHEET 1 OF 4														
			REV A															

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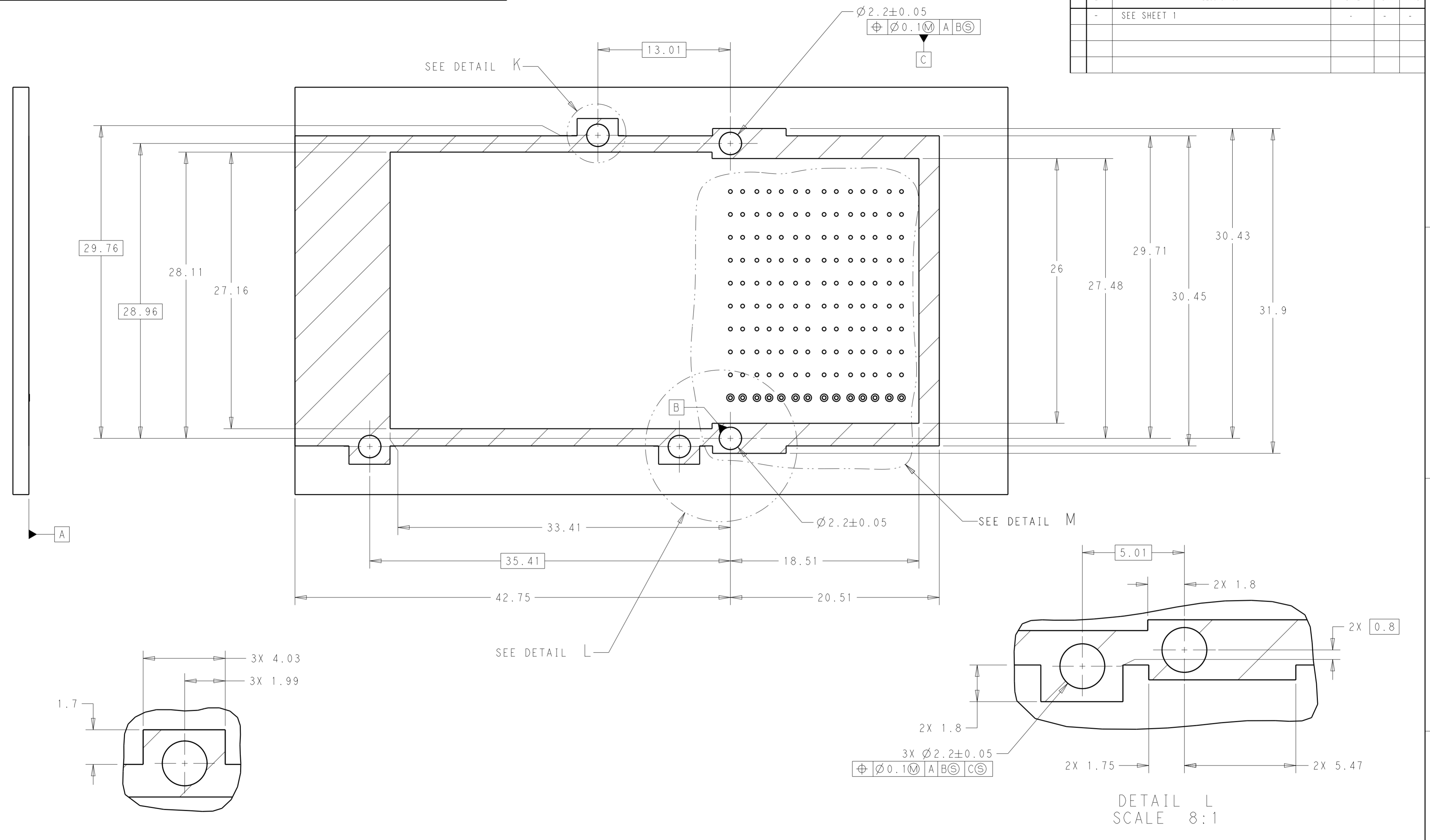
REVISIONS				
P	LTR	DESCRIPTION	DATE	APVD
-		SEE SHEET 1	-	-



THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN M. SHIRK 07NOV2016	STE TE Connectivity	
		CHK J. WESTMAN 07NOV2016		
		APVD J. WESTMAN 07NOV2016	NAME RECEPTACLE ASSEMBLY, PCIe OPTIMIZED, TYPE 2, CDFP	
DIMENSIONS: mm		PRODUCT SPEC 108-32065	SIZE A2	CAGE CODE -
TOLERANCES UNLESS OTHERWISE SPECIFIED: 0 PLC ±0.1 1 PLC ±0.1 2 PLC ±0.1 3 PLC ±0.1 4 PLC ±0.1 ANGLES ± FINISH		APPLICATION SPEC 114-32114	DRAWING NO C-2311882	RESTRICTED TO -
MATERIAL SEE NOTES		WEIGHT -	SCALE 4:1	SHEET 2 OF 4
		CUSTOMER DRAWING		REV A

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P	LTR	DESCRIPTION	DATE	APVD
-		SEE SHEET 1	-	-



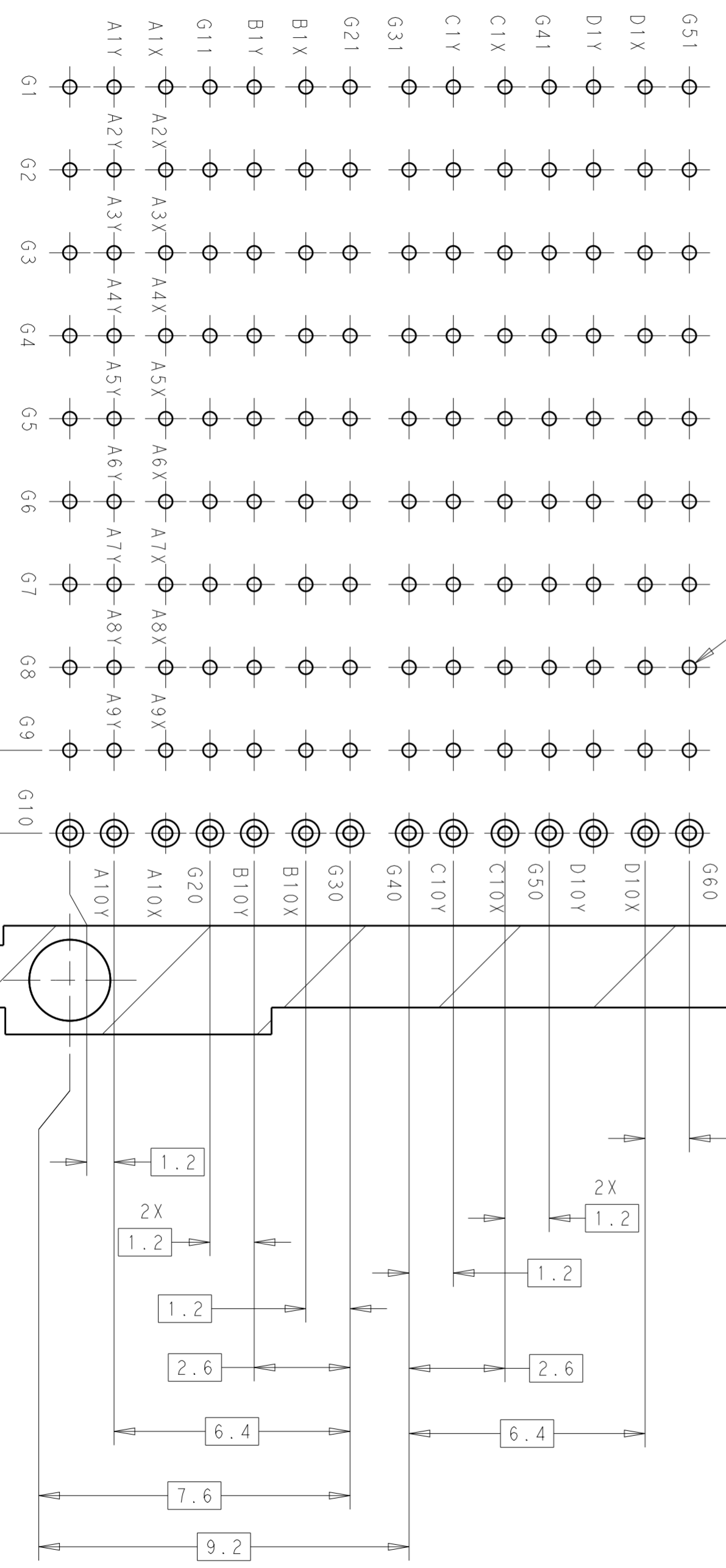
DETAIL K
SCALE 8:1

DETAIL L
SCALE 8:1

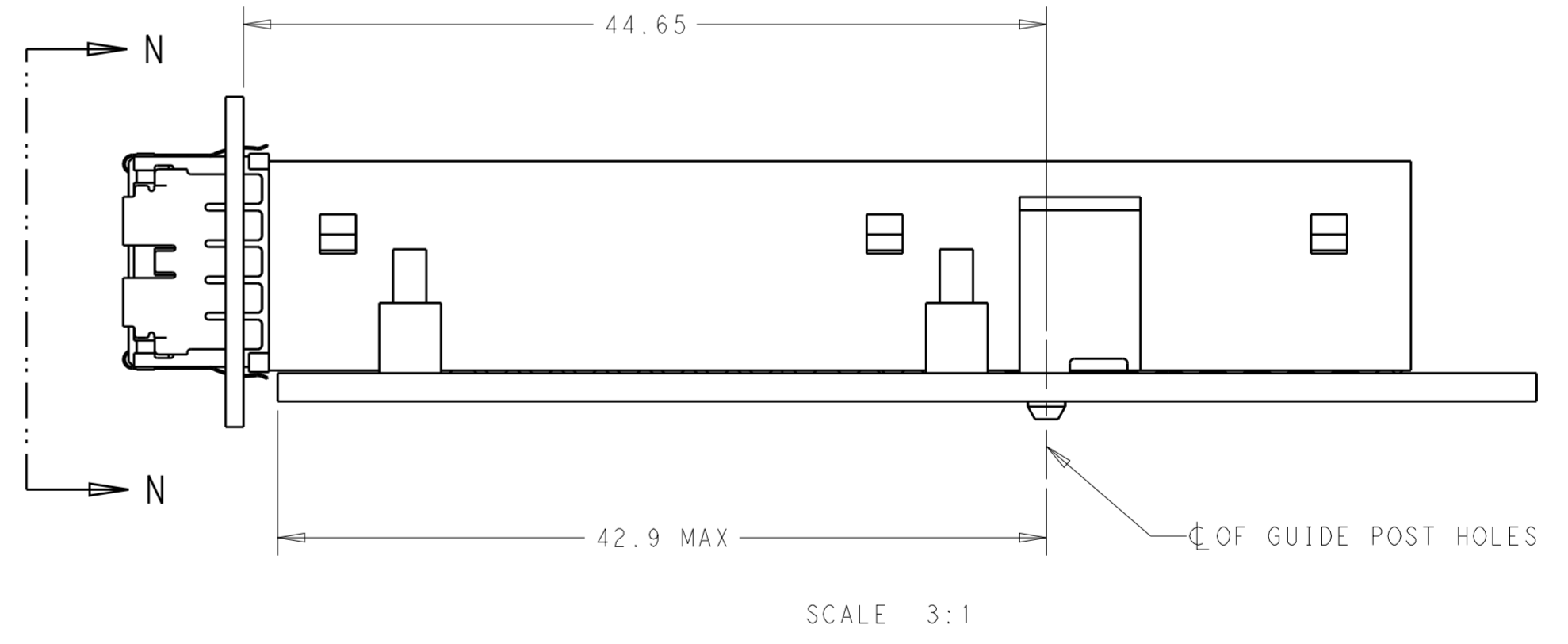
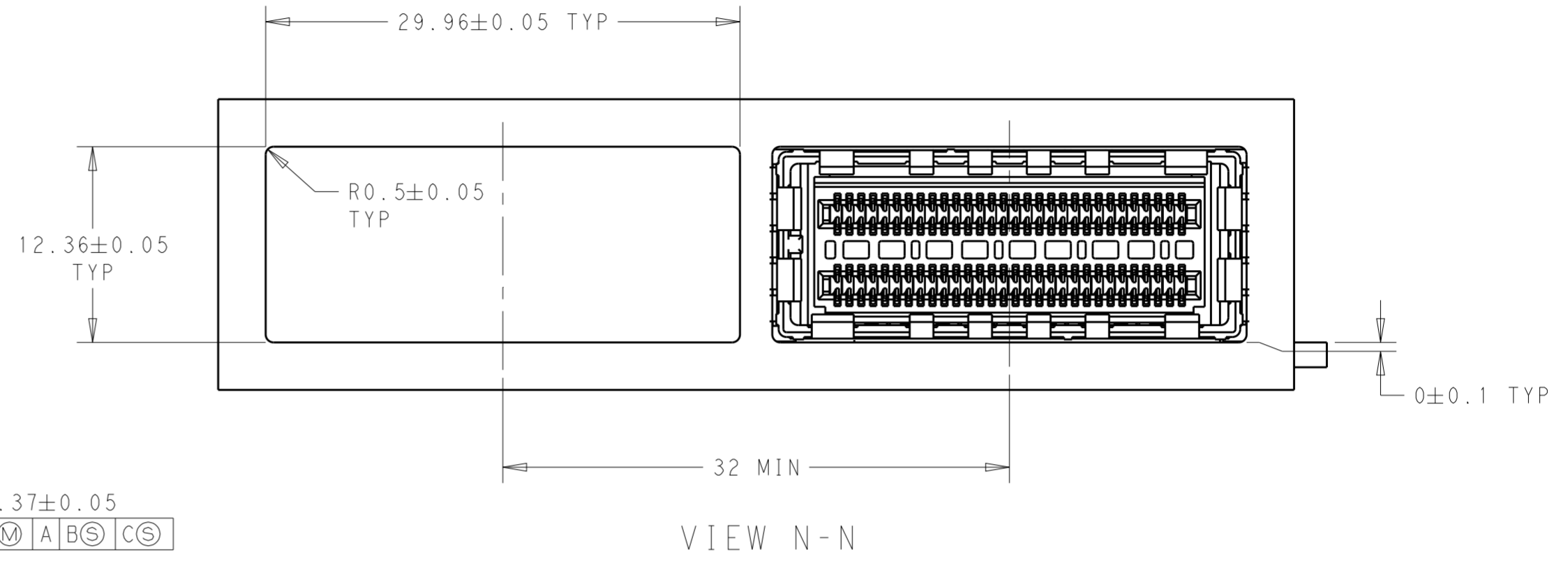
THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN M. SHIRK 07NOV2016	TE Connectivity	
DIMENSIONS: mm		CHK J. WESTMAN 07NOV2016		
TOLERANCES UNLESS OTHERWISE SPECIFIED:		APVD J. WESTMAN 07NOV2016	NAME RECEPTACLE ASSEMBLY, PCIE OPTIMIZED, TYPE 2, CDFP	
0 PLC ±0.1	1 PLC ±0.1	PRODUCT SPEC 108-32065	SIZE A2	CAGE CODE -
2 PLC ±0.1	3 PLC ±0.1	APPLICATION SPEC 114-32114	DRAWING NO C-2311882	RESTRICTED TO -
4 PLC ±0.1	ANGLES ±	WEIGHT -	SCALE 4:1	SHEET 3 OF 4
MATERIAL SEE NOTES	FINISH SEE NOTES	CUSTOMER DRAWING	REV A	

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REVISIONS				
P	LTR	DESCRIPTION	DATE	APVD
-	-	SEE SHEET 1	-	-



140X $\varnothing 0.37 \pm 0.05$
 $\varnothing 0.1$ M A B S C S



DETAIL M
 SCALE 8:1

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DIMENSIONS: mm		CHK J. WESTMAN 07NOV2016		
TOLERANCES UNLESS OTHERWISE SPECIFIED:		APVD J. WESTMAN 07NOV2016	NAME RECEPTACLE ASSEMBLY, PCIE OPTIMIZED, TYPE 2, CDFP	
0 PLC ±0.1 1 PLC ±0.1 2 PLC ±0.1 3 PLC ±0.1 4 PLC ±0.1 ANGLES ± FINISH		PRODUCT SPEC 108-32065	SIZE A2	
MATERIAL SEE NOTES		APPLICATION SPEC 114-32114	CAGE CODE -	DRAWING NO C-2311882
		WEIGHT -	RESTRICTED TO -	SCALE 4:1
		CUSTOMER DRAWING	SHEET 4 OF 4	REV A

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