Datasheet for Telink 2.4GHz RF System-On-Chip Solution TLSR8366

DS-TLSR8366-E18

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Keyword:

Features; Package; Pin layout; Working mode; Memory; MCU; RF Transceiver; Baseband; Clock; Timers; Interrupt; Interface; QDEC; Comparator; Electrical specification; Application

Brief:

This datasheet is dedicated for Telink high-performance 2.4GHz RF System-On-Chip (SoC) solution TLSR8366. In this datasheet, key features, working mode, main modules, electrical specification and application of the TLSR8366 are introduced.

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Revision History

Version	Major Changes	Date	Author
1.0	Initial release	2014/9	Cynthia
1.1	Added section 3.1.3.3; Updated section 1.2.1., Table 3-1, Table 3-3, and section 8.3	2015/1	Cynthia
1.2	Updated section 3.1	2015/1	S.G.J. Cynthia
1.21	Updated section 11.4	2015/3	Cynthia
1.22	Updated section 12.1	2015/3	L.X., Cynthia
1.2.3	Updated section 1	2015/5	Cynthia
1.2.4	Updated section 1.2.3, 11.2, 11.4	2015/6	L.Y., Cynthia
1.3.0	Added IO drive strength information	2015/7	L.Y., Cynthia
1.4.0	Deleted ESOP8 and DICE package information.	2016/5	X.S.J., Cynthia
1.5.0	Updated DC characteristics and ordering information.	2016/7	L.J.R., X.S.J., Cynthia
1.6.0	Deleted Telink SDK section.	2016/10	L.X., Cynthia
1.7.0	Updated ordering information.	2017/3	X.S.J., Cynthia
1.8.0	Updated the following sections: 1.2.2 RF Features and 11.4 AC characteristics, 5.1.3 HS divider clock, 8.1 GPIO.	2018/1	Y.C.Q., L.W.F., X.W.W, Cynthia
1.9.0	Updated section 1.2.2 RF Features, 1.2.3 Features of power management module, 1.4 Ordering information, 8.3 Pull-up/Pull-down resistor, 11.3 DC characteristics, 11.4 AC characteristics.	2018/8	LX, HZT, Cynthia
2.0.0	Updated section 11.4 AC characteristics.	2018/10	TJB, LX Cynthia
2.1.0	Updated section 11.4 AC characteristics.	2018/12	LX, Cynthia

Version	Major Changes	Date	Author
2.2.0	Updated section 11.3 DC characteristics and 11.4 AC characteristics.	2019/2	TJB, LX, Cynthia
2.3.0	Updated section 11.3 DC characteristics.	2019/2	LX, HZT, Cynthia

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1 Overview

As one member of the low-power, high-integration family of Telink wireless SoC solution, the TLSR8366 is dedicated to 2.4GHz RF System-On-Chip solutions such as wireless mouse, non-audio remote control, non-audio USB dongle, etc. It's completely RoHS-compliant and 100% lead (Pb)-free.

1.1 Block diagram

The TLSR8366 is designed to offer high integration, ultra-low power application capabilities. It integrates an advanced 2.4GHz RF transceiver, a powerful 32-bit MCU, 16KB on-chip OTP, 6KB on-chip SRAM, a quadrature decoder (QDEC), flexible I/O interfaces, and nearly all of the peripheral blocks needed to construct a powerful 2.4GHz RF System-On-Chip solution.

The system's block diagram is as shown in Figure 1-1:

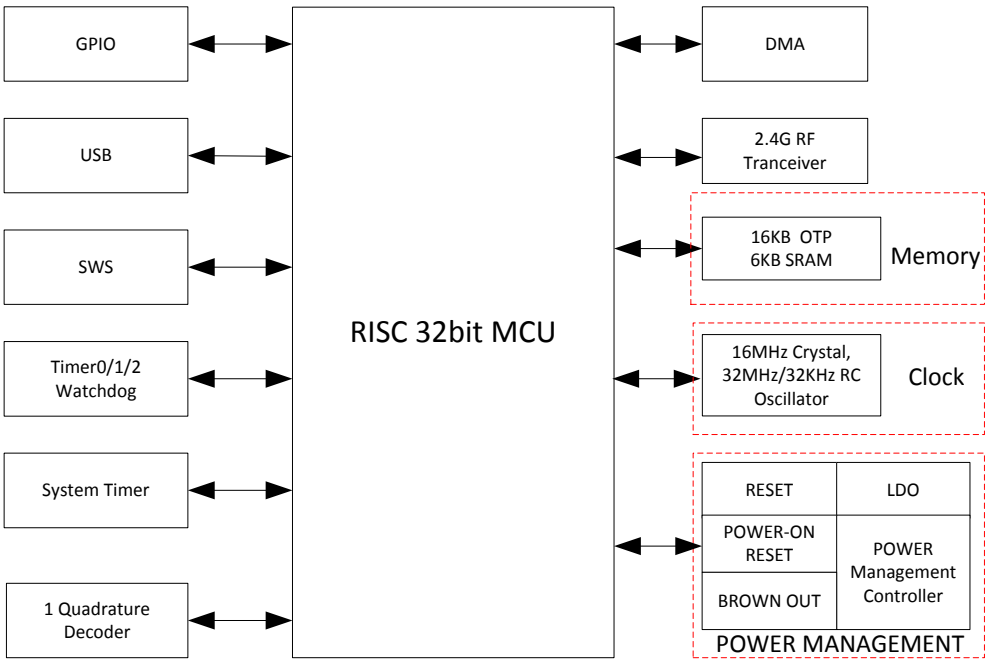


Figure 1- 1 Block diagram of the system

Based on the TLSR8366 with high-volume-assembly and high integration, few external components are needed to satisfy customers' ultra-low cost requirement.

1.2 Key features

1.2.1 General features

General features are as follows:

1) Embed 32-bit high performance MCU with clock up to 48MHz.
2) Program memory: 16KB on-chip OTP.
3) Data memory: 6KB on-chip SRAM.
4) 16MHz Crystal and 32KHz/32MHz embedded RC oscillator.
5) Abundant GPIO interfaces: Up to 18/12/9 GPIOs depending on package option.
6) Debug interface: SWS.
7) USB interface: DM, DP.
8) Embeds one quadrature decoder (QDEC).
9) Operating temperature: -40℃~+85℃ industrial temperature range.

1.2.2 RF Features

RF features include:

1) 2.4GHz RF transceiver embedded, working in worldwide 2.4GHz ISM band.
2) Adaptive frequency hopping.
3) RF link data rate: 2Mbps.
4) Rx Sensitivity: -87dBm at 2Mbps mode.
5) Tx output power: +7dBm.
6) Auto acknowledgement and retry.
7) Single-pin antenna interface.
8) RSSI monitoring.

1.2.3 Features of power management module

Features of power management module include:

1) Power supply of 1.9V~3.6V.
2) Embedded LDO.

3) Battery monitor: Supports low battery detection.
4) Multiple stage power management to minimize power consumption.
5) Low power consumption:
   - ✧ Transmitter mode current: 15mA @ 0dBm power, 23mA @ max power
   - ✧ Receiver mode current: 12.7mA
   - ✧ Suspend mode current: 10uA
   - ✧ Deep sleep mode current: 0.7uA

1.2.4 USB features

USB features include:

1) Compatible with USB2.0 Full speed mode
2) Supports 9 endpoints
3) Supports ISP (In-System Programming) via USB port
4) Composite device

1.3 Typical applications

Typical applications for the TLSR8366 are as follows:

- ✧ Wireless mouse
- ✧ Non-audio remote control
- ✧ Non-audio USB dongle

1.4 Ordering information

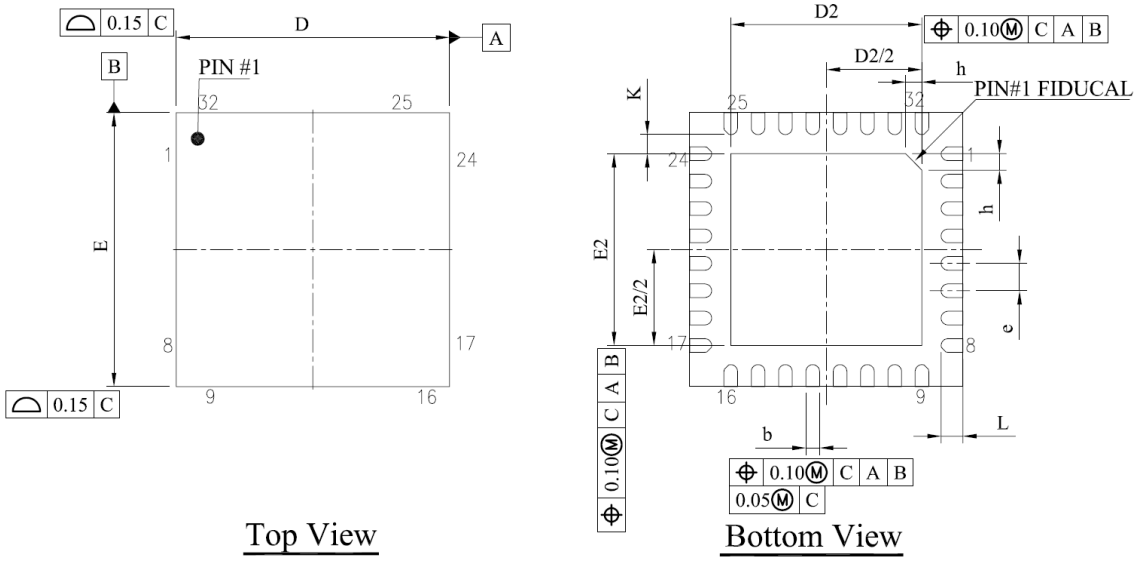
Table 1- 1 Ordering information of the TLSR8366

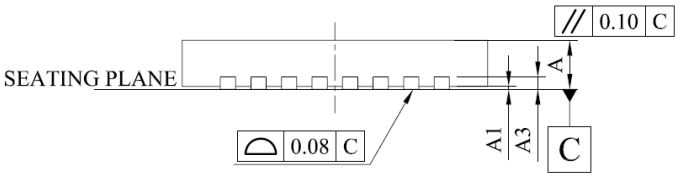
Product Series	Package Type	Temperature Range	Product Part No.	Packing Method	Minimum Order Quantity
TLSR8366	32-pin 5X5mm QFN	-40℃ ~ +85℃	TLSR8366ET32	TR	3000
	24-pin 4X4mm QFN	-40℃ ~ +85℃	TLSR8366ET24	TR	3000
	16-pin SOP16L_ 10X6 mm	-40℃ ~ +85℃	TLSR8366EP16	TR	3000

*Note: Packing method “TR” means tape and reel.

1.5 Package

Package dimension for the TLSR8366ET32, TLSR8366ET24 and TLSR8366EP16 are shown as Figure 1- 2, Figure 1- 3, and Figure 1- 4, respectively.

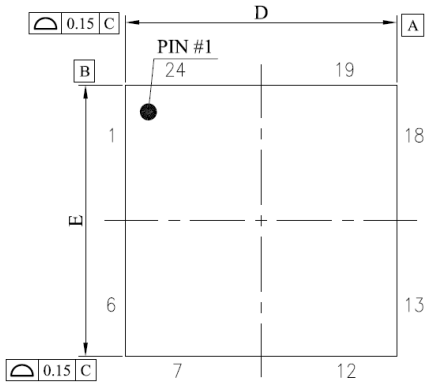




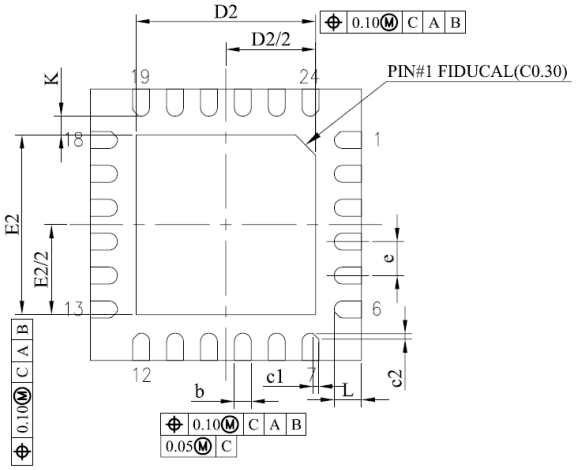
Side View

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.8	2.0
A3	---	0.20REF	---	---	7.9REF	---
b	0.18	0.25	0.30	7.1	9.8	11.8
D	4.90	5.00	5.10	192.9	196.9	200.8
D2	3.40	3.50	3.60	133.9	137.8	141.7
E	4.90	5.00	5.10	192.9	196.9	200.8
E2	3.40	3.50	3.60	133.9	137.8	141.7
e	---	0.50TYP	---	---	19.7TYP	---
K	0.20	---	---	7.9	---	---
L	0.35	0.40	0.45	13.8	15.7	17.7
h	0.30	0.35	0.40	11.8	13.8	15.7

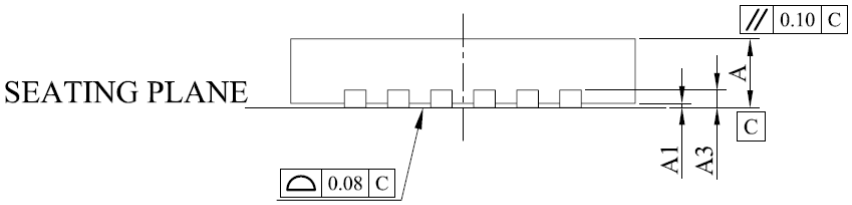
Figure 1- 2 Package dimension for the TLSR8366ET32 (Unit: mm)



Top View



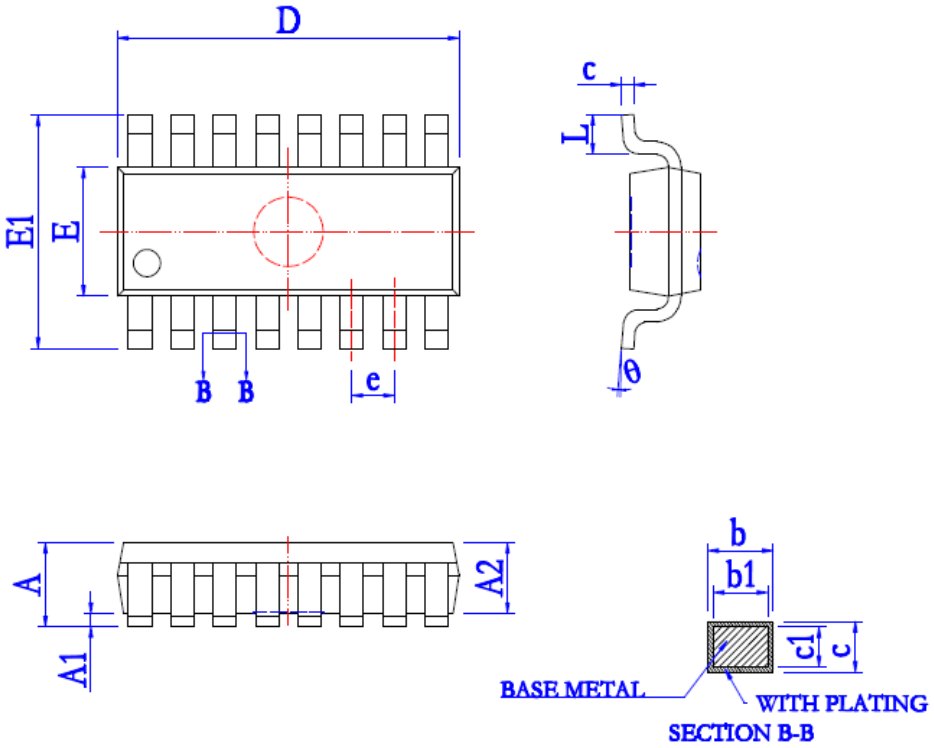
Bottom View



Side View

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.8	2.0
A3	---	0.20REF	---	---	7.9REF	---
b	0.18	0.25	0.30	7.1	9.8	11.8
D	3.90	4.00	4.10	153.5	157.5	161.4
D2	2.55	2.65	2.75	100.4	104.3	108.3
E	3.90	4.00	4.10	153.5	157.5	161.4
E2	2.55	2.65	2.75	100.4	104.3	108.3
e	---	0.50BSC	---	---	19.7BSC	---
K	0.20	---	---	7.9	---	---
L	0.35	0.40	0.45	13.8	15.7	17.7
c1	---	0.08	---	---	3.1	---
c2	---	0.08	---	---	3.1	---

Figure 1- 3 Package dimension for the TLSR8366ET24 (Unit: mm)



SYMBOL	MILIMETER	
	MIN	MAX
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
b1	0.320	0.500
c	0.170	0.250
c1	0.160	0.240
D	9.800	10.200
E	3.800	4.000
E1	5.800	6.200
e	1.270BSC	
L	0.400	0.800
θ	0°	8°
L/F Carrier Dimension (mil)	134*91	

Figure 1- 4 Package dimension for the TLSR8366EP16 (Unit: mm)

1.6 Pin layout

Pin assignment for the TLSR8366ET32 is as shown in Figure 1- 5:

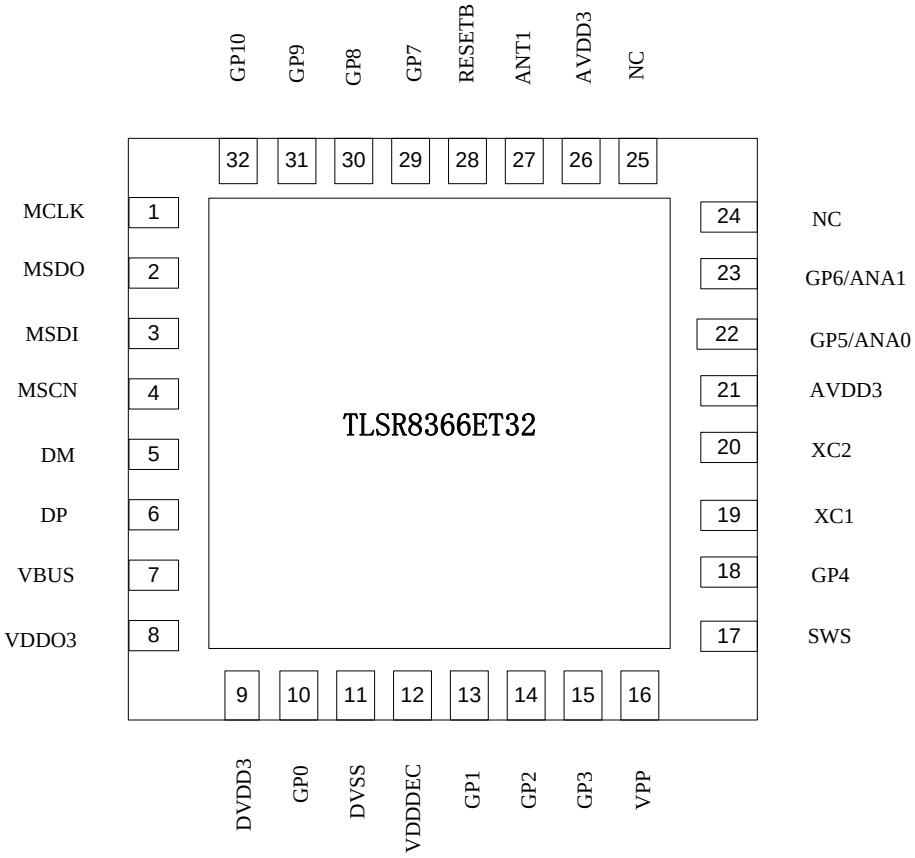


Figure 1- 5 Pin assignment for the TLSR8366ET32

Functions of 32 pins for the TLSR8366ET32 are described in Table 1-2:

Table 1- 2 Pin functions for the TLSR8366ET32

QFN32 5X5			
No.	**Pin Name**	**Type**	**Description**
1	**MCLK**	Digital I/O	memory spi clock
2	**MSDO ***	Digital I/O	memory spi data output
3	**MSDI ***	Digital I/O	memory spi data input
4	**MSCN**	Digital I/O	memory spi chip select. Active low
5	**DM**	Digital I/O	USB data minus
6	**DP**	Digital I/O	USB data positive

QFN32 5X5			
No.	**Pin Name**	**Type**	**Description**
7	VBUS	PWR	USB 5V supply
8	VDDO3	PWR	5V-to-3V LDO output
9	DVDD3	PWR	3.3V IO supply
10	**GP0 ***	Digital I/O	GPIO0
11	DVSS	GND	Digital LDO ground
12	VDDDEC	PWR	Digital LDO 1.8V output
13	**GP1 ***	Digital I/O	GPIO1
14	**GP2 ***	Digital I/O	GPIO2
15	**GP3 ***	Digital I/O	GPIO3
16	VPP	PWR	for OTP program 6.75V power supply
17	**SWS**	Digital I/O	single wire slave
18	**GP4 ***	Digital I/O	GPIO4
19	XC1	Analog I	16MHz crystal input+
20	XC2	Analog I	16MHz crystal input-
21	AVDD3	PWR	Analog 3.3V supply
22	**GP5/ANA0 ***	Digital I/O	GPIO5
23	**GP6/ANA1 ***	Digital I/O	GPIO6
24	NC	-	Not connected
25	NC	-	Not connected
26	AVDD3	PWR	RF 3.3V supply
27	ANT1	Analog I/O	RF input 1
28	RESETB	RESET	power on reset active low
29	**GP7 ***	Digital I/O	GPIO7
30	**GP8 ***	Digital I/O	GPIO8
31	**GP9 ***	Digital I/O	GPIO9
32	**GP10 ***	Digital I/O	GPIO10

*Note:

1) Pins with bold typeface can be used as GPIOS.

2) The GPIOs marked with an asterisk have configurable pull-up/pull-down resistor.

3) The GPIO pins including MCLK, MSDO, MSDI, MSCN, SWS, GP7~GP10 support drive strength of 4mA or 2mA (4mA when “DS”=1, 2mA when “DS”=0); the GPIO pins including GP0~GP6 support drive strength of 4mA or 0.7mA (4mA when “DS”=1, 0.7mA when “DS”=0); the GPIO pins including DM and DP support drive strength of

16mA or 12mA (16mA when “DS”=1, 12mA when “DS”=0). “DS” configuration will take effect when the pin is used as output. Please refer to **Section** 8.1 GPIO for corresponding “DS” register address and the default setting.

Pin assignment for the TLSR8366ET24 is as shown in Figure 1- 6:

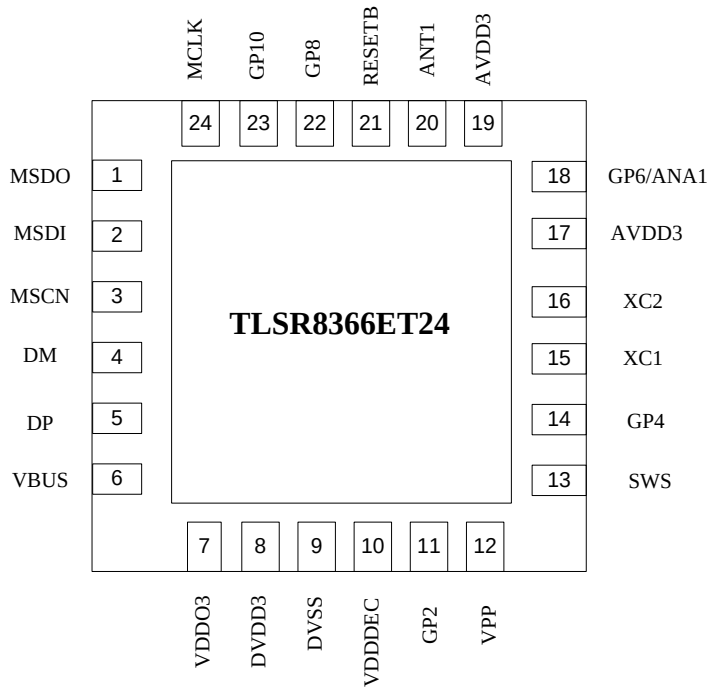


Figure 1- 6 Pin assignment for the TLSR8366ET24

Functions of 24 pins for the TLSR8366ET24 are described in Table 1-3:

Table 1- 3 Pin functions for the TLSR8366ET24

QFN24 4X4			
No.	**Pin Name**	**Type**	**Description**
1	**MSDO ***	Digital I/O	memory spi data output
2	**MSDI ***	Digital I/O	memory spi data input
3	**MSCN**	Digital I/O	memory spi chip select. Active low
4	**DM**	Digital I/O	USB data minus
5	**DP**	Digital I/O	USB data positive
6	VBUS	PWR	USB 5V supply
7	VDDO3	PWR	5V-to-3V LDO output
8	DVDD3	PWR	3.3V IO supply

QFN24 4X4			
No.	**Pin Name**	**Type**	**Description**
9	DVSS	GND	Digital LDO ground
10	VDDDEC	PWR	Digital LDO 1.8V output
11	**GP2 ***	Digital I/O	GPIO2
12	VPP	PWR	for OTP program 6.75V power supply
13	**SWS**	Digital I/O	single wire slave
14	**GP4 ***	Digital I/O	GPIO4
15	XC1	Analog I	16MHz crystal input+
16	XC2	Analog I	16MHz crystal input-
17	AVDD3	PWR	Analog 3.3V supply
18	**GP6/ANA1 ***	Digital I/O	GPIO6
19	AVDD3	PWR	RF 3.3V supply
20	ANT1	Analog I/O	RF input 1
21	RESETB	RESET	power on reset active low
22	**GP8 ***	Digital I/O	GPIO8
23	**GP10 ***	Digital I/O	GPIO10
24	**MCLK**	Digital I/O	memory spi clock

*Note:

1) Pins with bold typeface can be used as GPIOS.

2) The GPIOs marked with an asterisk have configurable pull-up/pull-down resistor.

3) The GPIO pins including MCLK, MSDO, MSDI, MSCN, SWS, GP8 and GP10 support drive strength of 4mA or 2mA (4mA when “DS”=1, 2mA when “DS”=0); the GPIO pins including GP2, GP4 and GP6 support drive strength of 4mA or 0.7mA (4mA when “DS”=1, 0.7mA when “DS”=0); the GPIO pins including DM and DP support drive strength of 16mA or 12mA (16mA when “DS”=1, 12mA when “DS”=0). “DS” configuration will take effect when the pin is used as output. Please refer to **Section** 8.1 GPIO for corresponding “DS” register address and the default setting.

Pin assignment for the TLSR8366EP16 is as shown in Figure 1- 7:

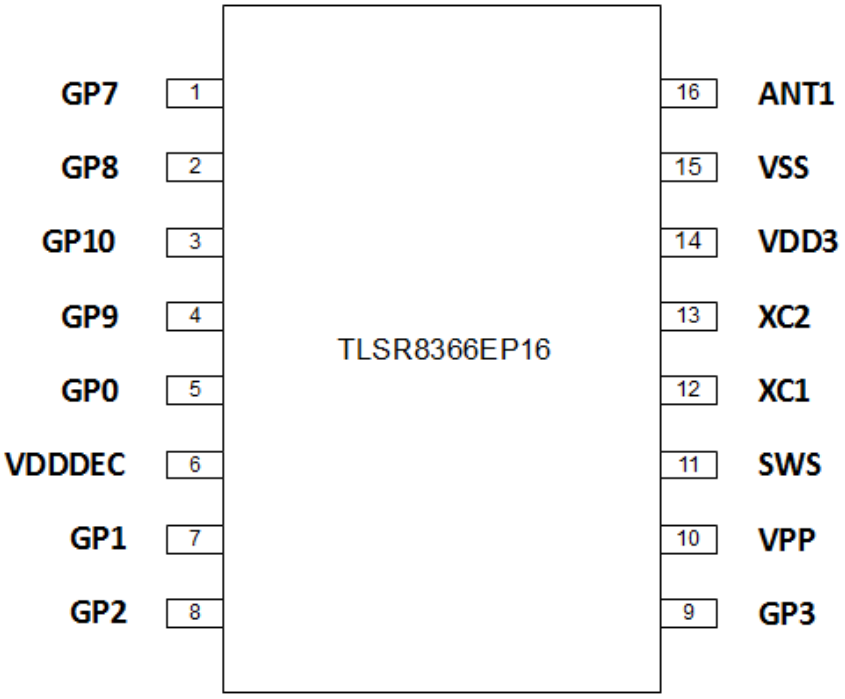


Figure 1- 7 Pin assignment for the TLSR8366EP16

Functions of 16 pins for the TLSR8366EP16 are described in Table 1-4:

Table 1- 4 Pin functions for the TLSR8366EP16

SOP16L_10X6			
No.	**Pin Name**	**Pin Type**	**Description**
1	**GP7 ***	Digital I/O	GPIO7
2	**GP8 ***	Digital I/O	GPIO8
3	**GP10 ***	Digital I/O	GPIO10
4	**GP9 ***	Digital I/O	GPIO9
5	**GP0 ***	Digital I/O	GPIO0
6	VDDDEC	PWR	Digital LDO 1.8V output
7	**GP1 ***	Digital I/O	GPIO1
8	**GP2 ***	Digital I/O	GPIO2
9	**GP3 ***	Digital I/O	GPIO3
10	VPP	PWR	for OTP program 6.75V power supply
11	**SWS**	Digital I/O	single wire slave

SOP16L_10X6			
No.	**Pin Name**	**Pin Type**	**Description**
12	XC1	Analog I	16MHz crystal input+
13	XC2	Analog I	16MHz crystal input-
14	VDD3	PWR	Analog 3.3V supply
15	VSS	GND	LNA ground
16	ANT1	Analog I/O	RF input 1

*Note:

1) Pins with bold typeface can be used as GPIOS.

2) The GPIOs marked with an asterisk have configurable pull-up/pull-down resistor.

3) The GPIO pins including SWS, GP7~GP10 support drive strength of 4mA or 2mA (4mA when “DS”=1, 2mA when “DS”=0); the GPIO pins including GP0~GP3 support drive strength of 4mA or 0.7mA (4mA when “DS”=1, 0.7mA when “DS”=0). “DS” configuration will take effect when the pin is used as output. Please refer to **Section** 8.1 GPIO for corresponding “DS” register address and the default setting.

2 Memory

The TLSR8366 embeds 6KB data memory (SRAM), and 16KB program memory (OTP).

SRAM/Register memory map is shown as follows:

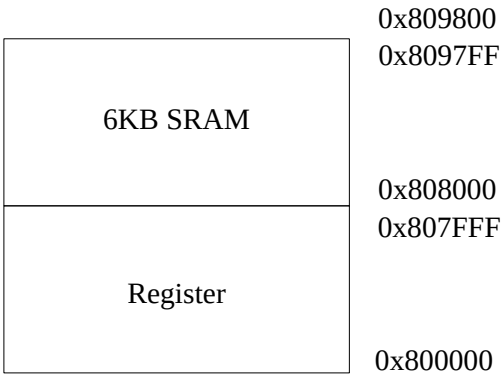


Figure 2- 1 Physical memory map

Register address: from 0x800000 to 0x807FFF;

6KB SRAM address: from 0x808000 to 0x809800.

Both register and 6KB SRAM address can be accessed via SWS interface.

OTP/External flash address mapping is configurable.

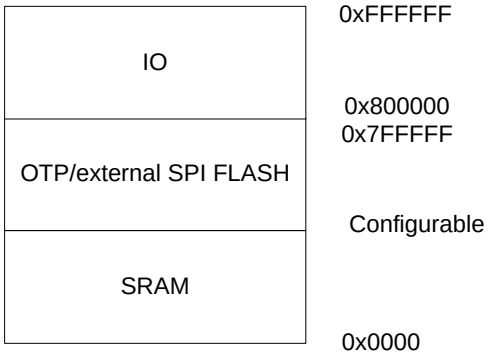


Figure 2- 2 MCU memory map

External FLASH address can be accessed via MSPI interface.

Address space starting from 0x800000 can be accessed via debug interface.

3 MCU

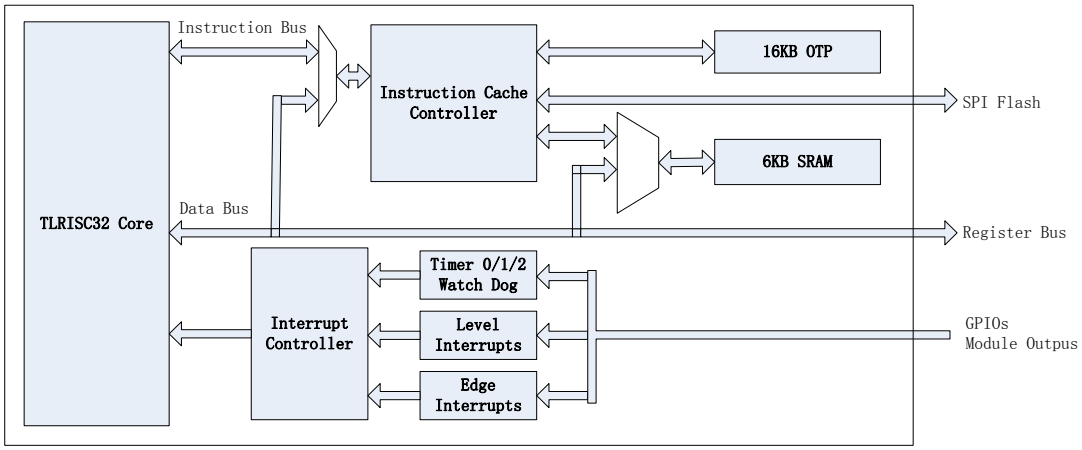


Figure 3- 1 Block diagram

The TLSR8366 integrates a powerful 32-bit MCU developed by Telink. The digital core is based on 32-bit RISC, and the length of instructions is 16 bits; four hardware breakpoints are supported.

3.1 Working modes

The TLSR8366 has four working modes: Active, Idle, Suspend and Deep Sleep. This section mainly gives the description of every working mode and mode transition.

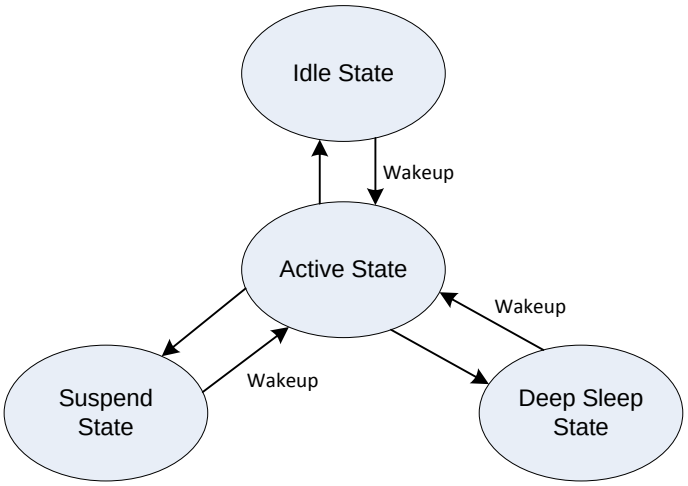


Figure 3- 2 Transition chart of working modes

3.1.1 Active mode

In active mode, the MCU block is at working state, and the TLSR8366 can transmit or receive data via its embedded RF transceiver. The RF transceiver can also

be powered down if no data transfer is needed.

3.1.2 Idle mode

In Idle mode, the MCU block stalls, and the RF transceiver can be at working state or be powered down. The time needed for the transition from Idle mode to Active mode is negligible.

3.1.3 Power-saving mode

3.1.3.1 Brief introduction

For the TLSR8366, there are two kinds of power-saving modes: suspend mode and deep sleep mode. The two modes have similar transition sequences but different register settings. For 1.8V digital core, it's still provided with the working power by 1.8V LDO in suspend mode; while in deep sleep mode, the 1.8V LDO will be turned off, and the digital core is powered down.

In suspend mode, the RF transceiver is powered down, and the clock of the MCU block is stopped. It only takes about 400us for the TLSR8366 to enter the active mode from suspend mode.

While in deep sleep mode, both the RF transceiver and the MCU block are powered down with only power management block being active. The transition time needed from deep sleep mode to active mode is 1ms, almost the same as power-up time.

3.1.3.2 Register configuration of power-saving mode

For the TLSR8366, power-saving mode related registers are configurable via digital core and 3.3V analog registers.

Table 3- 1 Registers in digital core

Address	Mnemonic	Type	Description	Reset value
0x6e	WAKEUPEN	R/W	Wakeup enable [0]: rsvd [1]: rsvd [2]: enable wakeup from usb [3]: enable wakeup from gpio or QDEC	00

Address	Mnemonic	Type	Description	Reset value
			wakeup [4]: rsvd System resume control [5]: enable GPIO remote wakeup [6]: if set to 1, system will issue USB resume signal on USB bus [7]: sleep wakeup reset system enable	
0x6f	PWDNEN	W	[0]: suspend enable [5]: rst all (act as power on reset) [6]: mcu low power mode [7]: stall mcu trig If bit[0] set 1, then system will go to suspend. Or only stall mcu	

Address 0x6e serves to enable various wakeup sources from power-saving mode.

Table 3- 2 3.3V analog registers (afe3V_reg05 ~ afe3V_reg06) (bit)

Address(bit)	Mnemonic	Reset value	Description
afe3V_reg05<0>	32K_rc_pd	0	Power down 32KHz RC oscillator 1: Power down 32KHz RC oscillator 0: Power up 32KHz RC oscillator
afe3V_reg05<1>	reserved	0	
afe3V_reg05<2>	32M_rc_pd	0	Power down of 32MHz RC oscillator 1: Power down 32MHz RC oscillator 0: Power up 32MHz RC oscillator
afe3V_reg05<3>	xtal_LDO_pd	0	Power down of 16MHz crystal oscillator 1: Power down 0: Power up
afe3V_reg05<4>	ldo_ana_pd	0	Power down of analog LDO 1: Power down

Address(bit)	Mnemonic	Reset value	Description
			0: Power up
afe3V_reg05<5>	reserved	1	
afe3V_reg05<6>	reserved	1	
afe3V_reg05<7>	BBPLL_LDO_pd_3V	0	Power down baseband pll LDO 1: Power down 0: Power up
afe3V_reg06<0>	comp_pd	1	Power down SAR ADC 1: Power down 0: Power up
afe3V_reg06<1>	rx_lnaLDO_pd	1	Power down LNA LDO in RF transceiver 1: Power down 0: Power up
afe3V_reg06<2>	rx_anaLDO_pd	1	Power down analog LDO in RF transceiver 1: Power down 0: Power up
afe3V_reg06<3>	rx_rfLDO_pd	1	Power down RF LDO in RF transceiver 1: Power down 0: Power up
afe3V_reg06<4>	pll_BG_pd	1	Power down Bandgap in PLL 1: Power down 0: Power up
afe3V_reg06<5>	reserved		
afe3V_reg06<6>	pll_vco_ldo_pd	1	Power down VCO LDO 1: Power down

Address(bit)	Mnemonic	Reset value	Description
			0: Power up
afe3V_reg06<7>	pll_cp_ldo_pd	1	Power down cp and prescaler analog circuit ldo 1: Power down 0: power up

Table 3- 3 3.3V analog registers (3v_reg14 ~ 3v_reg38)

Addr Dec	Addr Hex	Description	Default Value
r14	0x0e	buffer (watch dog will clean the buffer)	0x00
r15	0x0f	buffer (watch dog will clean the buffer)	0x00
r16	0x10	32k timer [7:0]	0x07
r17	0x11	32k timer [15:8]	0x00
r18	0x12[3:0]	32k timer [19:16]	0x00
	0x12[4]	32k timer mode, 1:continuous mode 0: single mode	
	0x12[7:5]	rsvd	
r19	0x13[6:0]	r_dly, power on delay (0x00 is the longest delay)	0x77
	0x13[7]	rsvd	
r20	0x14[2:0]	watch dog value, 0x01 means 500us,	0x02
	0x14[3]	watch dog enable	
	0x14[7:4]	pad polarity, bit[4] -->wkup_pad_en[1:0], bit[5]-->wkup_pad_en[3:2]……	
r21	0x15[3:0]	xtal_quick, 0xf means disable.	0x08
	0x15[5:4]	wake up source watch dog enable, bit[4], wkup dig , bit[5] wkup pad	
	0x15[7:6]	rsvd	

Addr Dec	Addr Hex	Description	Default Value
r22	0x16	wkup_pad_en,{p_gpio[10:7],p_gpio[4:1]}	0x00
r23	0x17[1:0]	wkupen, [0] wkup_dig, including wkup_usb, wkup_gpio and wkup qdec [1] wkup timer	0x00
	0x17[[2]	rsvd	
	0x17[3]	32k timer reset	
	0x17[4]	rsvd	
	0x17[5]	32k timer clock sel, [0] 32k rc, [1] 16m	
	0x17[6]	rsvd	
	0x17[7]	power down enable	
r24	0x18[0]	32k rc auto pwdn enable	0x00
	0x18[1]	rsvd	
	0x18[2]	16m xtal auto pwdn enable	
	0x18[3]	auto pwdn enable: ldo_ana, bbpll_ldo, comparator, rx_lna_ldo, rx_ana_ldo, rx_rfLDO, rx_rfldo,pll_bg, pll_vco_ldo, pll_cp_ldo	
	0x18[4]	rsvd	
	0x18[5]	power down low leakage ldo	
	0x18[6]	power down digital LDO enable	
	0x18[7]	isolation enable	
r25~r31		buffer(power on reset only)	0x00
r32	0x20	read only 32k timer value[7:0](one 32k clock will increase the value)	
r33	0x21	read only 32k timer value[15:8]	

Addr Dec	Addr Hex	Description	Default Value
r34	0x22	read only 32k timer value[23:16]	
r35	0x23[0]	rsvd	
	0x23[1]	timer wkup status write 1 will clean	
	0x23[2]	digital wkup status, write 1 will clean	
	0x23[3]	pad wkup status ,write 1 will clean	
	0x23[4]	watch dog status , write 1 will clean	
	0x23[5]	comparator value	
	0x23[6]	32k timer value[24]	
	0x23[7]	32k timer trig, write 1 to toggle this bit	
r36	0x24[0]	trk 32M manual en	0x00
	0x24[1]	trk 32M enable	
	0x24[2]	trk32k Manual en	
	0x24[3]	trk 32K enable	
	0x24[7:4]	rsvd	
r37	0x25[7:0]	32M manual cap	0x00
r38	0x26[6:0]	32K manual cap	0x00
	0x26[7]	rsvd	

3.1.3.3 Wakeup source

3.1.3.3.1 Wakeup source – USB

This wakeup source can only wake up the system from suspend mode.

First, set the digital core address 0x6e bit [2] to 1.

To activate this mode, 3V_reg23 bit[0] should also be set to 1.

Once USB host sends out resuming signal, the system will be wake up.

3.1.3.3.2 Wakeup source – GPIO

This wakeup source can only wake up the system from suspend mode.

First, set the right polarity of IO (address 0x594~0x595). Polarity 1 indicates corresponding IO is active low, while 0 indicates corresponding IO is active high.

Second, set the right mask (address 0x59c~0x59d). 1: enable this IO as wakeup source; 0: disable this IO.

Third, set both the digital core address 0x6e bit[3], 0x59e bit[7] and 3v_reg23 bit[0] to 1 so as to activate this mode.

Please refer to Table 8-1 for details about polarity and mask registers of each GPIO.

3.1.3.3.3 Wakeup source – 32K timer

This wakeup source is able to wake up the system from suspend mode or deep sleep mode.

Address 3V_reg23 bit[1] is the enabling bit for wakeup source from 32k timer.

3.1.3.3.4 Wakeup source – pad

This wakeup source is able to wake up the system from suspend mode or deep sleep mode.

3v_reg22 is enabling signal for pad wakeup sources: bit[7:4] -> [GP10, GP9, GP8, GP7], bit[3:0] -> [GP4, GP3, GP2, GP1]. 1: enable this IO as wakeup source; 0: disable this IO.

Polarity is controlled by 3v_reg20[7:4]: bit[7] controls polarity of GP10 and GP9, bit[6] controls polarity of GP8 and GP7, bit[5] controls polarity of GP4 and GP3, bit[4] controls polarity of GP2 and GP1. Polarity 1 indicates corresponding IO is active low,

while 0 indicates corresponding IO is active high.

3.1.3.3.5 Wakeup source – QDEC

This wakeup source can only wake up system from suspend mode. To enable this wakeup source, first enable QDEC clock, write 0x64[7] and 0x65[0] to 1, write 0x6e[3] to 1 and write 0xd7[1] to 1.

3.1.3.4 Transition sequence

First, enable the target wakeup source, and disable other wakeup sources.

NOTE: In deep sleep mode, the wakeup_dig (including wakeup source-USB, wakeup source-GPIO and wakeup source-QDEC, shown as Figure 3-3) can't be selected as wakeup source; the effective wakeup source is 32K timer or pad wakeup source.

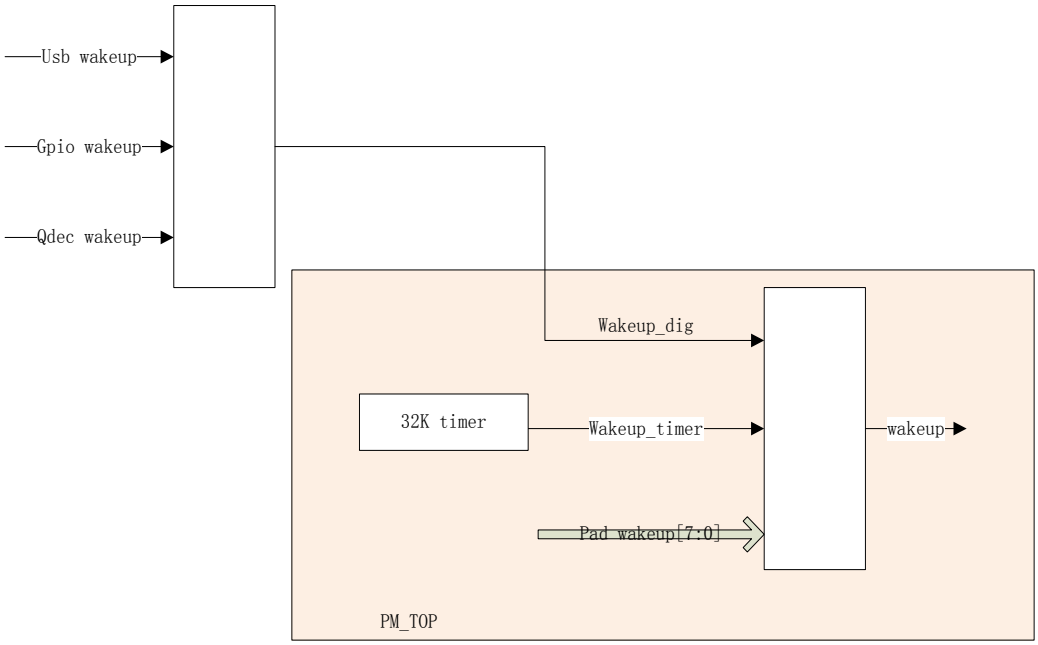


Figure 3- 3 Wakeup source

Second, select right power-saving mode: deep sleep mode or suspend mode. If deep sleep mode is to be selected, r24 bit[7] and bit[5] should be set to 1; r24 bit[7] and bit[5] should be cleared if suspend mode is to be selected.

Third, configure other enabling bits: set r23 bit[7] to 1; set r24 bits [3:0] to 1111, and also set r24 bit[6] to 1.

Fourth, Write data 0x81 to digital core address 0x6f to trigger the whole system. The system enters deep sleep mode or suspend mode (power-saving status depends on the setting of r24).

3.2 Reset

Except for power on reset, it is also feasible to carry out software reset for the whole chip or some modules. Setting address 0x6f[5] to 1b'1 is to reset the whole chip. Addresses 0x60~0x62 serve to reset individual modules: if some bit is set to logic "1", the corresponding module is reset.

Table 3- 4 Register configuration for reset, wakeup and power down enabling

Address	Mnemonic	Type	Description	Reset Value
0x60	RST0	R/W	Reset control, 1 for reset, 0 for clear [0] : mcu [1] : zb [2]: rsvd [3]: dma [4]: algm [5]: sws [6]: rsvd [7]: rsvd	00
0x61	RST1	R/W	[0] rsvd [1]rsvd [2]rsvd [3]rsvd [4]rsvd [5]rsvd [6]mspi [7]bbpll	df
0x62	RST2	R/W	[0]rsvd [1]algs [2]mcic [3]mcic auto reset at suspend [4]systimer [5]rsvd [6]rsvd [7] rsvd	00
0x6f	PWDNEN	W	[0]: suspend enable	

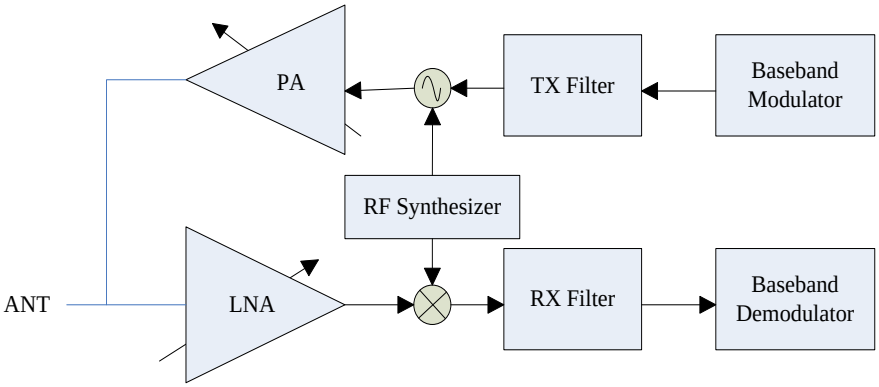
Address	Mnemonic	Type	Description	Reset Value
			[5]: rst all (act as power on reset) [6]: mcu low power mode [7]: stall mcu trig If bit[0] set 1, then system will go to suspend. Or only stall mcu	

4 2.4G RF Transceiver

4.1 Block diagram

The TLSR8366 integrates an advanced 2.4GHz RF transceiver. The RF transceiver works in the worldwide 2.4GHz ISM (Industrial Scientific Medical) band and contains an integrated balun with a single-ended RF Tx/Rx port pin. No matching components are needed.

The transceiver consists of a fully integrated frequency synthesizer, a power amplifier, a modulator and a receiver. The transceiver works in proprietary 2Mbps mode. All modes support FSK/GFSK modulations.



Block diagram of RF transceiver

The internal PA can deliver a typical 7dBm output power, avoiding the needs for an external RF PA.

4.2 Function description

Air interface data rate, the modulated signaling rate for RF transceiver when transmitting and receiving data, supports 2Mbps mode for the TLSR8366.

For the TLSR8366, RF transceiver can operate with frequency ranging from 2.400GHz to 2.4835GHz. The RF channel frequency setting determines the center of the channel.

4.3 Baseband

The baseband contains dedicated hardware logic to perform fast AGC control, access code correlation, CRC checking and frequency hopping logic.

The baseband supports all features required by 2Mbps specification.

4.3.1 Packet format

Packet format is shown as Table 4-1:

Table 4- 1 Packet Format

LSB MSB

Preamble (1 octet)	Access Address (Configurable: 3, 4 or 5 octets)	PDU (Configurable: 0 to 63 octets)	CRC (Configurable: 1 octet or 2 octets)

Packet length 40bits ~ 568bits (20~284us @ 2Mbps).

4.3.2 RSSI

The TLSR8366 provides accurate RSSI (Receiver Signal Strength Indicator) indication which can be read on per packet basis.

5 Clock

5.1 System clock

5.1.1 System clock sources

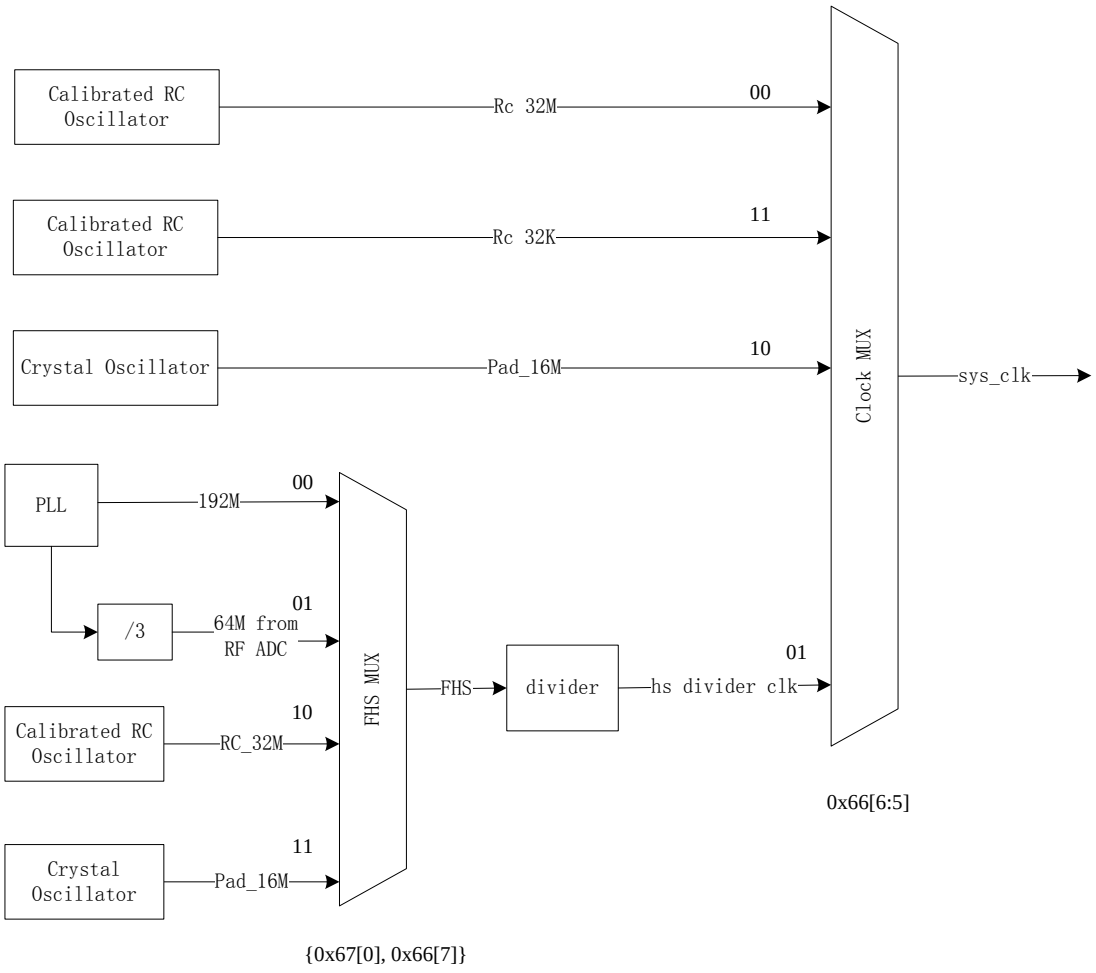


Figure 5- 1 Block diagram of system clock

There are four selectable clock sources for system clock, including: 32MHz RC oscillator, hs divider clock, 16MHz pad clock (external crystal oscillator) and 32KHz RC oscillator. Register CLKSEL (address 0x66[6:5]) is used to select system clock source.

Commonly a 16MHz crystal oscillator can be employed to generate a basic clock signal for the system. The maximum frequency tolerance of the crystal is ±60ppm. And a low-power RC oscillator can be used to generate a 32KHz clock signal for the wakeup timer.

5.1.2 FHS select

The high speed clock (FHS) is selectable via address {0x67[0], 0x66[7]} from the following sources: 192MHz clock from PLL, 64MHz clock from RF ADC, 32MHz clock from RC oscillator or 16MHz pad clock (external crystal oscillator).

5.1.3 HS divider clock

If address 0x66[6:5] is set to 2b'01 to select the HS divider clock as system clock source, system clock frequency is adjustable via address 0x66[4:0].

$F_{System\ clock}$ = F_{FHS} / (system clock divider value in address 0x66[4:0]).

5.2 Module clock

Registers CLKEN0~CLKEN2 (address 0x63~0x65) are used to enable or disable clock for various modules. By disable the clocks of unused modules, current consumption could be reduced.

5.2.1 DCDC clock

Address 0x71 bit[5] must be set to logic "1" to enable DCDC clock, while 0x71 bit[4:0] is used to configure frequency dividing factor (i.e. DCDC clock mod). DCDC clock is calculated according to the formula below:

$$F_{DCDC\ clock} = F_{FHS}/(\text{mod value in address } 0x71[4:0])$$

5.3 Register table

Table 5- 1 Register table for clock

Address	Mnemonic	Type	Description	Reset Value
0x63	CLKEN0	R/W	Clock enable control: 1 for enable; 0 for disable [0] : mcu [1] : zb [2]: rsvd [3]: dma [4]: algm [5]: sws [6]: rsvd	8c

Address	Mnemonic	Type	Description	Reset Value
			[7]: rsvd	
0x64	CLKEN1	R/W	[0]rsvd [1]rsvd [2]rsvd [3]rsvd [4]rsvd [5]rsvd [6]syst imer [7]qdec sysclk	00
0x65	CLKEN2	R/W	[0]32k for qdec [1]rsvd [2]rsvd [3]rsvd [4]rsvd [5]rsvd [6]rsvd [7]rsvd	00
0x66	CLKSEL	R/W	System clock select [4:0]: system clock divider: fhs/(CLKSEL[4:0]). Fhs refer to {0x67[0], 0x66[7]} FHS_sel [6:5] 2'b00:32m clock from rc 2'b01:hs divider clk 2'b10:16M clock from pad 2'b11:32k clk from rc [7] FHS sel (see 0x67 definition)	ff
0x67	FHS_sel	R/W	{0x67[0], 0x66[7]} fhs select 2'b00: 192M clock from pll 2'b01:64M 2'b10:32M clock from osc 2'b11:16M clock from pad	00
0x71	DC/DC clk mod	R/W	[4:0] dc/dc clk mod Dc/dc clk f = FHS/mod [5] clock enable [7:6] rsvd	

6 Timers

6.1 Timer0~Timer2

The TLSR8366 supports three timers: Timer0~ Timer2. The three timers all support four modes: Mode 0 (System Clock Mode), Mode 1 (GPIO Trigger Mode), Mode 2 (GPIO Pulse Width Mode) and Mode 3 (Tick Mode).

Timer 2 can also be configured as “watchdog” to monitor firmware running.

6.1.1 Register table

Table 6- 1 Register configuration for Timer0~Timer2

Address	Mnemonic	Type	Description	Reset Value
0x620	TMR_CTRL0	RW	[0]Timer0 enable [2:1] Timer0 mode. 0 using sclk, 1, using gpio, 2 count widht of gpi, 3 tick [3]Timer1 enable [5:4] Timer1 mode. [6]Timer2 enable [7]Bit of timer2 mode	00
0x621	TMR_CTRL1	RW	[0]Bit of timer2 mode [7:1]Low bits of watch dog capture	00
0x622	TMR_CTRL2	RW	[6:0]High bits of watch dog capture. It is compared with [31:18] of timer2 ticker [7]watch dog capture	00
0x623	TMR_STATUS	RW	[0] timer0 status, write 1 to clear [1] timer1 status, write 1 to clear [2] timer2 status, write 1 to clear [3] watch dog status, write 1 to clear	
0x624	TMR_CAPT0_0	RW	Byte 0 of timer0 capture	00

Address	Mnemonic	Type	Description	Reset Value
0x625	TMR_CAPT0_1	RW	Byte 1 of timer0 capture	00
0x626	TMR_CAPT0_2	RW	Byte 2 of timer0 capture	00
0x627	TMR_CAPT0_3	RW	Byte 3 of timer0 capture	00
0x628	TMR_CAPT1_0	RW	Byte 0 of timer1 capture	00
0x629	TMR_CAPT1_1	RW	Byte 1 of timer1 capture	00
0x62a	TMR_CAPT1_2	RW	Byte 2 of timer1 capture	00
0x62b	TMR_CAPT1_3	RW	Byte 3 of timer1 capture	00
0x62c	TMR_CAPT2_0	RW	Byte 0 of timer2 capture	00
0x62d	TMR_CAPT2_1	RW	Byte 1 of timer2 capture	00
0x62e	TMR_CAPT2_2	RW	Byte 2 of timer2 capture	00
0x62f	TMR_CAPT2_3	RW	Byte 3 of timer2 capture	00
0x630	TMR_TICK0_0	RW	Byte 0 of timer0 ticker	
0x631	TMR_TICK0_1	RW	Byte 1 of timer0 ticker	
0x632	TMR_TICK0_2	RW	Byte 2 of timer0 ticker	
0x633	TMR_TICK0_3	RW	Byte 3 of timer0 ticker	
0x634	TMR_TICK1_0	RW	Byte 0 of timer1 ticker	
0x635	TMR_TICK1_1	RW	Byte 1 of timer1 ticker	
0x636	TMR_TICK1_2	RW	Byte 2 of timer1 ticker	
0x637	TMR_TICK1_3	RW	Byte 3 of timer1 ticker	
0x638	TMR_TICK2_0	RW	Byte 0 of timer2 ticker	
0x639	TMR_TICK2_1	RW	Byte 1 of timer2 ticker	
0x63a	TMR_TICK2_2	RW	Byte 2 of timer2 ticker	
0x63b	TMR_TICK2_3	RW	Byte 3 of timer2 ticker	

6.1.2 Mode0 (System Clock Mode)

In Mode 0, system clock is employed as clock source.

After Timer is enabled, Timer Tick (i.e. counting value) is increased by 1 on each positive edge of system clock from preset initial Tick value. Generally the initial Tick value is set to 0.

Once current Timer Tick value matches the preset Timer Capture (i.e. timing value), an interrupt is generated, Timer stops counting and Timer status is updated.

Steps of setting Timer0 for Mode 0 is taken as an example.

1st: Set initial Tick value of Timer0

Set Initial value of Tick via registers TMR_TICK0_0~TMR_TICK0_3 (address 0x630~0x633). Address 0x630 is lowest byte and 0x633 is highest byte. It's recommended to clear initial Timer Tick value to 0.

2nd: Set Capture value of Timer0

Set registers TMR_CAPT0_0~TMR_CAPT0_3 (address 0x624~0x627). Address 0x624 is lowest byte and 0x627 is highest byte.

3rd: Set Timer0 to Mode 0 and enable Timer0

Set register TMR_CTRL0 (address 0x620) [2:1] to 2b'00 to select Mode 0; Meanwhile set address 0x620[0] to 1b'1 to enable Timer0. Timer0 starts counting upward, and Tick value is increased by 1 on each positive edge of system clock until it reaches Timer0 Capture value.

6.1.3 Mode1 (GPIO Trigger Mode)

In Mode 1, GPIO is employed as clock source.

After Timer is enabled, Timer Tick (i.e. counting value) is increased by 1 on each positive edge of GPIO from preset initial Tick value. Generally the initial Tick value is set to 0.

Once current Timer Tick value matches the preset Timer Capture (i.e. timing value), an interrupt is generated and timer stops counting.

Steps of setting Timer1 for Mode 1 is taken as an example.

1st: Set initial Tick value of Timer1

Set Initial value of Tick via registers TMR_TICK1_0~TMR_TICK1_3 (address 0x634~0x637). Address 0x634 is lowest byte and 0x637 is highest byte. It's recommended to clear initial Timer Tick value to 0.

2nd: Set Capture value of Timer1

Set registers TMR_CAPT1_0~TMR_CAPT1_3 (address 0x628~0x62b). Address 0x628 is lowest byte and 0x62b is highest byte.

3rd: Set Timer1 to Mode 1 and enable Timer1

Set address 0x620[5:4] to 2b'01 to select Mode 1; Meanwhile set address 0x620[3] to 1b'1 to enable Timer1. Timer1 starts counting upward, and Timer1 Tick value is increased by 1 on each positive edge of GPIO until it reaches Timer1 Capture value.

6.1.4 Mode2 (GPIO Pulse Width Mode)

In Mode 2, system clock is employed as the unit to measure the width of GPIO pulse.

After Timer is enabled, Timer Tick is triggered by a positive edge of GPIO pulse. Then Timer Tick (i.e. counting value) is increased by 1 on each positive edge of system clock from preset initial Tick value. Generally the initial Tick value is set to 0.

While a negative edge of GPIO pulse is detected, an interrupt is generated and timer stops counting. The GPIO pulse width could be calculated in terms of tick count and period of system clock.

Steps of setting Timer2 for Mode 2 is taken as an example.

1st: Set initial Timer2 Tick value

Set Initial value of Tick via registers TMR_TICK2_0~TMR_TICK2_3 (address 0x638~0x63b). Address 0x638 is lowest byte and 0x63b is highest byte. It's recommended to clear initial Timer Tick value to 0.

2nd: Set Timer2 to Mode 2 and enable Timer2

Set address 0x620[7:6] to 2b'01 and address 0x621 [0] to 1b'1.

Timer2 Tick is triggered by a positive edge of GPIO pulse. Timer2 starts counting upward and Timer2 Tick value is increased by 1 on each positive edge of system clock.

While a negative edge of GPIO pulse is detected, an interrupt is generated and Timer2 tick stops.

3rd: Read current Timer2 Tick value to calculate GPIO pulse width

Read current Timer2 Tick value from address 0x638~0x63b.

Then GPIO pulse width is calculated as follows:

$$\text{GPIO pulse width} = \text{System clock period} * (\text{current Timer2 Tick} - \text{intial Timer2 Tick})$$

For initial Timer2 Tick value set to the recommended value of 0, then:

$$\text{GPIO pulse width} = \text{System clock period} * \text{current Timer2 Tick}.$$

6.1.5 Mode3 (Tick Mode)

In Mode 3, system clock is employed.

After Timer is enabled, Timer Tick starts counting upward, and Timer Tick value is increased by 1 on each positive edge of system clock.

This mode could be used as time indicator. There will be no interrupt generated. Timer Tick keeps rolling from 0 to 0xffffffff. When Timer tick overflows, it returns to 0 and starts counting upward again.

Steps of setting Timer0 for Mode 3 is taken as an example.

1st: Set initial Tick value of Timer0

Set Initial value of Tick via address 0x630~0x633. Address 0x630 is lowest byte and address 0x633 is highest byte. It's recommended to clear initial Timer Tick value to 0.

2nd: Set Timer0 to Mode 3 and enable Timer0

Set address 0x620[2:1] to 2b'11 to select Mode 3, meanwhile set address 0x620[0] to 1b'1 to enable Timer0. Timer0 Tick starts to roll.

3rd: Read current Timer0 Tick value

Current Timer0 Tick value can be read from address 0x630~0x633.

6.1.6 Watchdog

Programmable watchdog could reset chip from unexpected hang up or malfunction.

Only Timer2 supports Watchdog.

Timer2 Tick has 32bits. Watchdog Capture has only 14bits, which consists of TMR_CTRL2 (address 0x622) [6:0] as higher bits and TMR_CTRL1 (address 0x621) [7:1] as lower bits. Chip will be reset when the Timer2 Tick[31:18] matches Watch dog capture.

1st: Clear Timer2 Tick value

Clear registers TMR_TICK2_0 ~TMR_TICK2_3 (address 0x638~0x63b). Address 0x638 is lowest byte and 0x63b is highest byte.

2nd: Enable Timer2

Set register TMR_CTRL0 (address 0x620) [6] to 1b'1 to enable Timer2.

3rd: Set 14-bit Watchdog Capture value and enable Watchdog

Set address 0x622[6:0] as higher bits of watchdog capture and 0x621[7:1] as lower bits. Meanwhile set address 0x622[7] to 1b'1 to enable Watchdog.

Then Timer2 Tick starts counting upwards from 0.

If bits[31:18] of Timer2 Tick value read from address 0x638~0x63b reaches watchdog capture, the chip will be reset.

6.2 System Timer

The TLSR8366 also supports a System Timer.

Table 6- 2 Register table for System Timer

Address	Mnemonic	R/W	Function	Default Value
0x740	Sys_timer[7:0]	R/W		00
0x741	Sys_timer[15:8]	R/W		00
0x742	Sys_timer[23:16]	R/W		00
0x743	Sys_timer[31:24]	R/W	System timer counter, write to set initial value. This is the sys timer counter	00

7 Interrupt System

7.1 Interrupt structure

The interrupting function is applied to manage dynamic program sequencing based on real-time events triggered by timers, pins and etc.

For the TLSR8366, there are 24 interrupt sources in all: 16 types are level-triggered interrupt sources and 8 types are edge-triggered interrupt sources.

When CPU receives an interrupt request (IRQ) from some interrupt source, it will decide whether to respond to the IRQ. If CPU decides to respond, it pauses current routine and starts to execute interrupt service subroutine. Program will jump to certain code address and execute IRQ commands. After finishing interrupt service subroutine, CPU returns to the breakpoint and continues to execute main function.

7.2 Register configuration

Table 7- 1 Register table for Interrupt system

Address	Mnemonic	Type	Description	Reset Value
0x640	MASK_0	RW	Byte 0 interrupt mask, level-triggered type [7]: irq_host_cmd | irq_qdec [6]: irq_uart [5]: irq_ks [4]: irq_dma [3]: usb_pwdn [2]: time2 [1]: time1 [0]: time0	00
0x641	MASK_1	RW	Byte 1 interrupt mask, level-triggered type [7]: an_irq [6]: irq_software | irq_pwm [5]: irq_zb_rt [4]: irq_udc[4] [3]: irq_udc[3] [2]: irq_udc[2] [1]: irq_udc[1] [0]: irq_udc [0]	00
0x642	MASK_2	RW	Byte 2 interrupt mask, edge-triggered type	00

Address	Mnemonic	Type	Description	Reset Value
			[7]: gpio2risc[2] [6]: gpio2risc[1] [5]: gpio2risc[0] [4]: irq_stimer [3]: pm_irq [2]: irq_gpio [1]: usb_reset [0]: usb_250us	
0x643	IRQMODE	RW	[0] interrupt enable [1] reserved (Multi-Address enable)	00
0x644	PRIO_0	RW	Byte 0 of priority 1: High priority; 0: Low priority	00
0x645	PRIO_1	RW	Byte 1 of priority	00
0x646	PRIO_2	RW	Byte 2 of priority	00
0x648	IRQSRC_0	R	Byte 0 of interrupt source	
0x649	IRQSRC_1	R	Byte 1 of interrupt source	
0x64a	IRQSRC_2	R	Byte 2 of interrupt source	

7.2.1 Enable/Mask interrupt sources

Various interrupt sources could be enabled or masked by registers MASK_0~MASK_2 (address 0x640~0x642).

7.2.2 Interrupt mode and priority

Interrupt mode is typically-used mode. Register IRQMODE (address 0x643)[0] should be set to 1b'1 to enable interrupt function.

IRQ tasks could be set as High or Low priority via registers PRIO_0~PRIO_2 (address 0x644~0x646). When more than one interrupt sources assert interrupt requests at the same time, CPU will respond depending on respective interrupt priority levels. It's recommended not to modify priority setting.

7.2.3 Interrupt source flag

Three bytes in registers IRQSRC_0~IRQSRC_2 (address 0x648~0x64a) serve to indicate IRQ sources. Once IRQ occurs from certain source, the corresponding IRQ source flag will be raised to "High". User could identify IRQ source by reading address

0x648~0x64a.

When handling edge-triggered type interrupt, the corresponding IRQ source flag needs to be cleared via address 0x64a. Take the interrupt source usb_250us for example: First enable the interrupt source by setting address 0x642[0] to 1; then set address 0x643 [0] to 1 to enable the interrupt. In interrupt handling function, 24-bit data is read from address 0x648~0x64a to determine which IRQ source is valid; if data bit[16] is 1, it means the usb_250us interrupt is valid. Clear this interrupt source by setting address 0x64a bit[0] to 1.

As for level-type interrupt, IRQ interrupt source status needs to be cleared via setting corresponding module status register. Take Timer0 IRQ interrupt source for example, register TMR_STATUS (address 0x623) [0] should be written with 1b'1 to clear Timer0 status (refer to section 6.1.1).

8 Interface

8.1 GPIO

The TLSR8366ET32, TLSR8366ET24 and TLSR8366EP16 support up to 18, 12 and 9 GPIOs respectively. Except for dedicated GPIOs, all digital IOs can be used as general purpose IOs. Please refer to section 1.6 for available GPIO resources.

The GPIOs with multiplexed function (MSPI, USB, SWS) are used as normal function by default. To use them as GPIOs, please refer to Table 8-1. First configure the function of the IO as GPIO function via related register in the “Act as GPIO” column. After GPIO function is enabled for some pin, if the pin is used as output, corresponding “OE” register should be set to set to 1b’1, and “IE” register should be cleared, then set “Output” register value; if the pin is used as input, corresponding “OE” register should be cleared, and “IE” register should be set to 1b’1, then input data can be read from “Input” register.

Table 8- 1 GPIO lookup table

PIN name	Normal Function (default)	GPIO Setting								
		Input	IE	OE	Output	DS (drive strength)	Act as GPIO	Polarity	Wakeup	m2
MSDO	MSDO	0x580[0]	0x590[0]	0x588[0]	0x584[0]	0x598[0]	0x58c[0]			
MSDI	MSDI	0x580[1]	0x590[1]	0x588[1]	0x584[1]	0x598[1]	0x58c[0]			
MCLK	MCLK	0x580[2]	0x590[2]	0x588[2]	0x584[2]	0x598[2]	0x58c[0]			
MSCN	MSCN	0x580[3]	0x590[3]	0x588[3]	0x584[3]	0x598[3]	0x58c[0]			
GP7	GPIO	0x580[4]	0x590[4]	0x588[4]	0x584[4]	0x598[4]		0x594[4]	0x59c[4]	0x5a8[4]
GP8	GPIO	0x580[5]	0x590[5]	0x588[5]	0x584[5]	0x598[5]		0x594[5]	0x59c[5]	0x5a8[5]
GP9	GPIO	0x580[6]	0x590[6]	0x588[6]	0x584[6]	0x598[6]		0x594[6]	0x59c[6]	0x5a8[6]
GP10	GPIO	0x580[7]	0x590[7]	0x588[7]	0x584[7]	0x598[7]		0x594[7]	0x59c[7]	0x5a8[7]
GP0	GPIO	0x581[0]	0x591[0]	0x589[0]	0x585[0]	0x599[0]		0x595[0]	0x59d[0]	0x5a9[0]
GP1	GPIO	0x581[1]	0x591[1]	0x589[1]	0x585[1]	0x599[1]		0x595[1]	0x59d[1]	0x5a9[1]
GP2	GPIO	0x581[2]	0x591[2]	0x589[2]	0x585[2]	0x599[2]		0x595[2]	0x59d[2]	0x5a9[2]
GP3	GPIO	0x581[3]	0x591[3]	0x589[3]	0x585[3]	0x599[3]		0x595[3]	0x59d[3]	0x5a9[3]
GP4	GPIO	0x581[4]	0x591[4]	0x589[4]	0x585[4]	0x599[4]		0x594[0]	0x59c[0]	0x5a8[0]
GP5	GPIO	0x581[5]	0x591[5]	0x589[5]	0x585[5]	0x599[5]		0x594[1]	0x59c[1]	0x5a8[1]
GP6	GPIO	0x581[6]	0x591[6]	0x589[6]	0x585[6]	0x599[6]		0x594[2]	0x59c[2]	0x5a8[2]

PIN name	Normal Function (default)	GPIO Setting								
		Input	IE	OE	Output	DS (drive strength)	Act as GPIO	Polarity	Wakeup	m2
SWS	SWS	0x581[7]	0x591[7]	0x589[7]	0x585[7]	0x599[7]	0x58c[5]	0x594[3]	0x59c[3]	0x5a8[3]
DM	DM	0x582[5]	0x592[5]	0x58a[5]	0x586[5]	0x59a[5]	0x58e[6]			
DP	DP	0x582[6]	0x592[6]	0x58a[6]	0x586[6]	0x59a[6]	0x58e[6]			

*Notes:
1) For OE, active high, 1: output enable.
2) For IE, 1: input enable, 0: input disable.
3) For all unused GPIOs, corresponding “IE” must be set as 0.
4) When SWS “IE” is set as 1, this pin must be fixed as pull-up/pull-down state (float state is not allowed).

In Table 8-1, the pins with bold typeface (including GP0~GP10 and SWS) support GPIO wakeup function from suspend mode, and also can be used to generate GPIO interrupt signal for interrupt system.

(1) GPIO interrupt request signal = | ((Input ^ Polarity) & m2).

- ✧ First enable GPIO function, IE, and disable OE;
- ✧ Select GPIO interrupt trigger edge (positive edge or negative edge) via configuring “Polarity”;
- ✧ Set corresponding GPIO interrupt enabling bit “m2”;
- ✧ User can read addresses 0x5b8~0x5bb to see which GPIO asserts GPIO interrupt request signal.

(2) GPIO Wakeup function:

- ✧ Set address 0x59e[7] to 1b’1 to enable GPIO wakeup;
- ✧ Set corresponding GPIO enabling bit “Wakeup”;
- ✧ Refer to **section 3.1.3.3.2** for other register configuration.

The registers in the “**DS**” column are used to configure corresponding pin’s driving strength: “1” indicates maximum drive level, while “0” indicates minimal drive level. The “DS” configuration will take effect when the pin is used as output. It’s set as

the strongest driving level by default. In actual applications, driving strength can be decreased to lower level if necessary.

Table 8-2 shows drive level for various GPIO pins.

- ✧ MSPI pins (MCLK, MSDO, MSDI, MSCN), SWS, GP7~GP10: maximum=4mA (“DS”=1), minimum=2mA (“DS”=0);
- ✧ GP0~GP6: maximum=4mA (“DS”=1), minimum=0.7mA (“DS”=0);
- ✧ USB pins (DM, DP): maximum=16mA (“DS”=1), minimum=12mA (“DS”=0).

Table 8- 2 IO drive strength

Pin Name	Drive Strength	
	“DS” = 0	“DS” = 1
MCLK	2mA	4mA
MSDO *	2mA	4mA
MSDI *	2mA	4mA
MSCN	2mA	4mA
DM	12mA	16mA
DP	12mA	16mA
GP0 *	0.7mA	4mA
GP1 *	0.7mA	4mA
GP2 *	0.7mA	4mA
GP3 *	0.7mA	4mA
SWS	2mA	4mA
GP4 *	0.7mA	4mA
GP5/ANA0 *	0.7mA	4mA
GP6/ANA1 *	0.7mA	4mA
GP7 *	2mA	4mA
GP8 *	2mA	4mA
GP9 *	2mA	4mA
GP10 *	2mA	4mA

8.2 SWS

The TLSR8366 supports SWS (Single Wire Slave) interface which represents the slave device of the single wire communication system developed by Telink. The maximum data rate can be up to 2Mbps.

8.3 Pull-up/Pull-down resistor

For the TLSR8366, the GPIOs including GP0~GP10, MSDI and MSDO support configurable 1MΩ / 10KΩ (except GP0) pull-up resistor or 100KΩ pull-down resistor. Related register configuration can be found in Table 8-3.

Take the GP1 for example: Setting analog register afe3V_reg08<1:0> to 2b'01/2b'10/2b'11 is to enable 1MΩ pull-up resistor/10KΩ pull-up resistor/100KΩ pull-down resistor respectively for GP1; Clearing the two bits disables pull-up and pull-down resistor for GP1.

Table 8- 3 3.3V analog registers related to Pull-up/Pull-down resistor

Address(bit)	Mnemonic	Reset value	Description
afe3V_reg08<1:0>	pullupdown_ctrl<1:0>	00	**GP1** Wake up mux input 0 pull up/down controls 00 -- No pull up/down resistor 01 -- 1MOhm pull-up resistor 10 – 10kOhm pull-up resistor 11 – 100kOhm pull-down resistor
afe3V_reg08<3:2>	pullupdown_ctrl<1:0>	00	**GP2** Wake up mux input 1 pull up/down controls 00 -- No pull up/down resistor 01 -- 1MOhm pull-up resistor 10 – 10kOhm pull-up resistor 11 – 100kOhm pull-down resistor

Address(bit)	Mnemonic	Reset value	Description
afe3V_reg08<5:4>	pullupdown_ctrl<1:0>	00	**GP3** Wake up mux input 2 pull up/down controls 00 -- No pull up/down resistor 01 -- 1MOhm pull-up resistor 10 – 10kOhm pull-up resistor 11 – 100kOhm pull-down resistor
afe3V_reg08<7:6>	pullupdown_ctrl<1:0>	00	**GP4** Wake up mux input 3 pull up/down controls 00 -- No pull up/down resistor 01 -- 1MOhm pull-up resistor 10 – 10kOhm pull-up resistor 11 – 100kOhm pull-down resistor
afe3V_reg09<1:0>	pullupdown_ctrl<1:0>	00	**GP7** Wake up mux input 4 pull up/down controls 00 -- No pull up/down resistor 01 -- 1MOhm pull-up resistor 10 – 10kOhm pull-up resistor 11 – 100kOhm pull-down resistor
afe3V_reg09<3:2>	pullupdown_ctrl<1:0>	00	**GP8** Wake up mux input 5 pull up/down controls 00 -- No pull up/down resistor 01 -- 1MOhm pull-up resistor 10 – 10kOhm pull-up resistor 11 – 100kOhm pull-down resistor
afe3V_reg09<5:4>	pullupdown_ctrl<1:0>	00	**GP9** Wake up mux input 6 pull up/down controls 00 -- No pull up/down resistor

Address(bit)	Mnemonic	Reset value	Description
			01 -- 1MOhm pull-up resistor 10 – 10kOhm pull-up resistor 11 – 100kOhm pull-down resistor
afe3V_reg09<7:6>	pullupdown_ctrl<1:0>	00	**GP10** Wake up mux input 7 pull up/down controls 00 -- No pull up/down resistor 01 -- 1MOhm pull-up resistor 10 – 10kOhm pull-up resistor 11 – 100kOhm pull-down resistor
afe3V_reg10<1:0>	pullupdown_ctrl<1:0>	00	**GP0** Wake up mux input 8 pull up/down controls 00/10 -- No pull up/down resistor 01 -- 1MOhm pull-up resistor 11 – 100kOhm pull-down resistor
afe3V_reg10<3:2>	pullupdown_ctrl<1:0>	00	**GP5** Wake up mux input 9 pull up/down controls 00 -- No pull up/down resistor 01 -- 1MOhm pull-up resistor 10 – 10kOhm pull-up resistor 11 – 100kOhm pull-down resistor
afe3V_reg10<5:4>	pullupdown_ctrl<1:0>	00	**GP6** Wake up mux input 10 pull up/down controls 00 -- No pull up/down resistor 01 -- 1MOhm pull-up resistor 10 – 10kOhm pull-up resistor 11 – 100kOhm pull-down resistor

9 Quadrature Decoder

The TLSR8366 embeds one quadrature decoder (QDEC) which is designed mainly for applications such as wheel. The QDEC implements debounce function to filter out jitter on the two phase inputs, and generates smooth square waves for the two phase.

9.1 Input pin selection

The QDEC supports two phase input; each input is selectable from the 11 dedicated GPIOs including GP0~GP10 via setting address 0xd2[4:0] (for channel a)/0xd3[4:0] (for channel b).

Table 9- 1 Input pin selection

Address 0xd2[4:0]/0xd3[4:0]	Pin
0	GP0
1	GP1
2	GP2
3	GP3
4	GP4
5	GP5
6	GP6
7	GP7
8	GP8
9	GP9
10	GP10

9.2 Common mode and double accuracy mode

The QDEC embeds an internal hardware counter, which is not connected with bus.

Address 0xd7[0] serves to select common mode or double accuracy mode.

For each wheel rolling step, two pulse edges (rising edge or falling edge) are generated.

If address 0xd7[0] is cleared to select common mode, the QDEC Counter value (real time counting value) is increased/decreased by 1 only when the same

rising/falling edges are detected from the two phase signals.

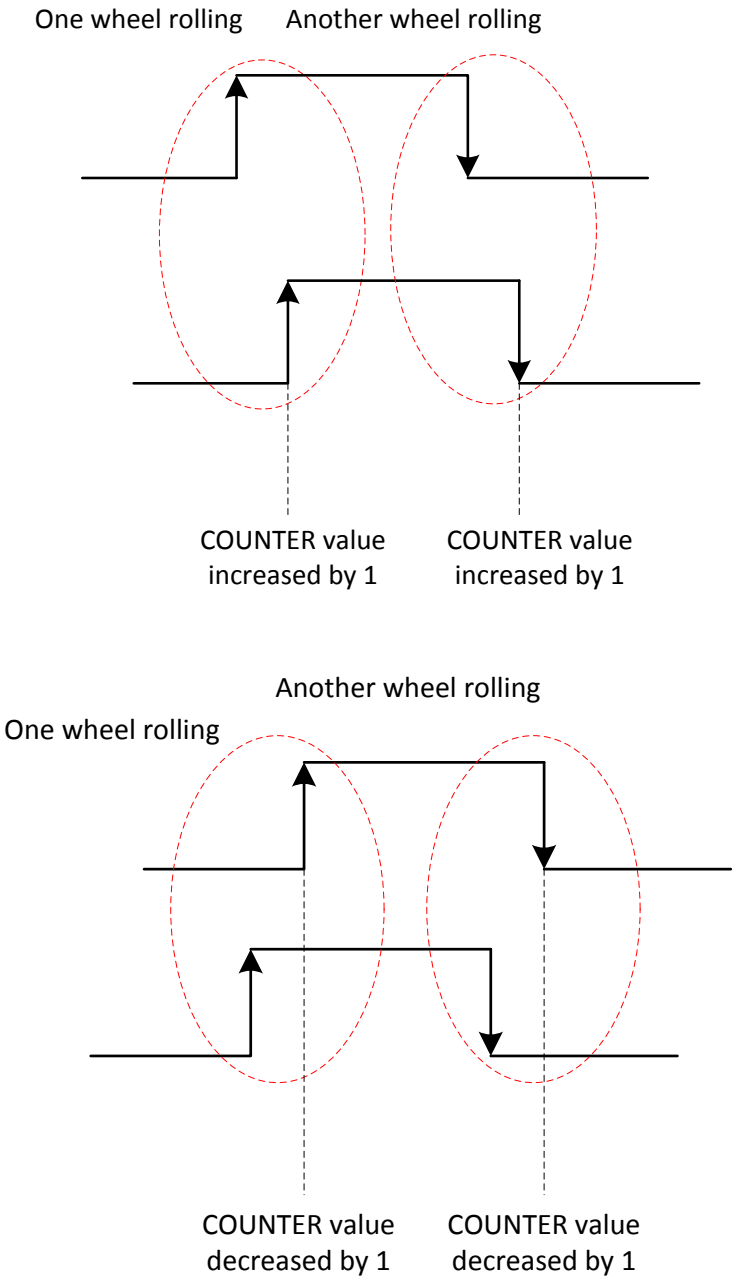


Figure 9- 1 Common mode

If address 0xd7[0] is set to 1b'1 to select double accuracy mode, the QDEC Counter value (real time counting value) is increased/decreased by 1 on each rising/falling edge of the two phase signals; the QDEC Counter value will be increased/decreased by 2 for one wheel rolling.

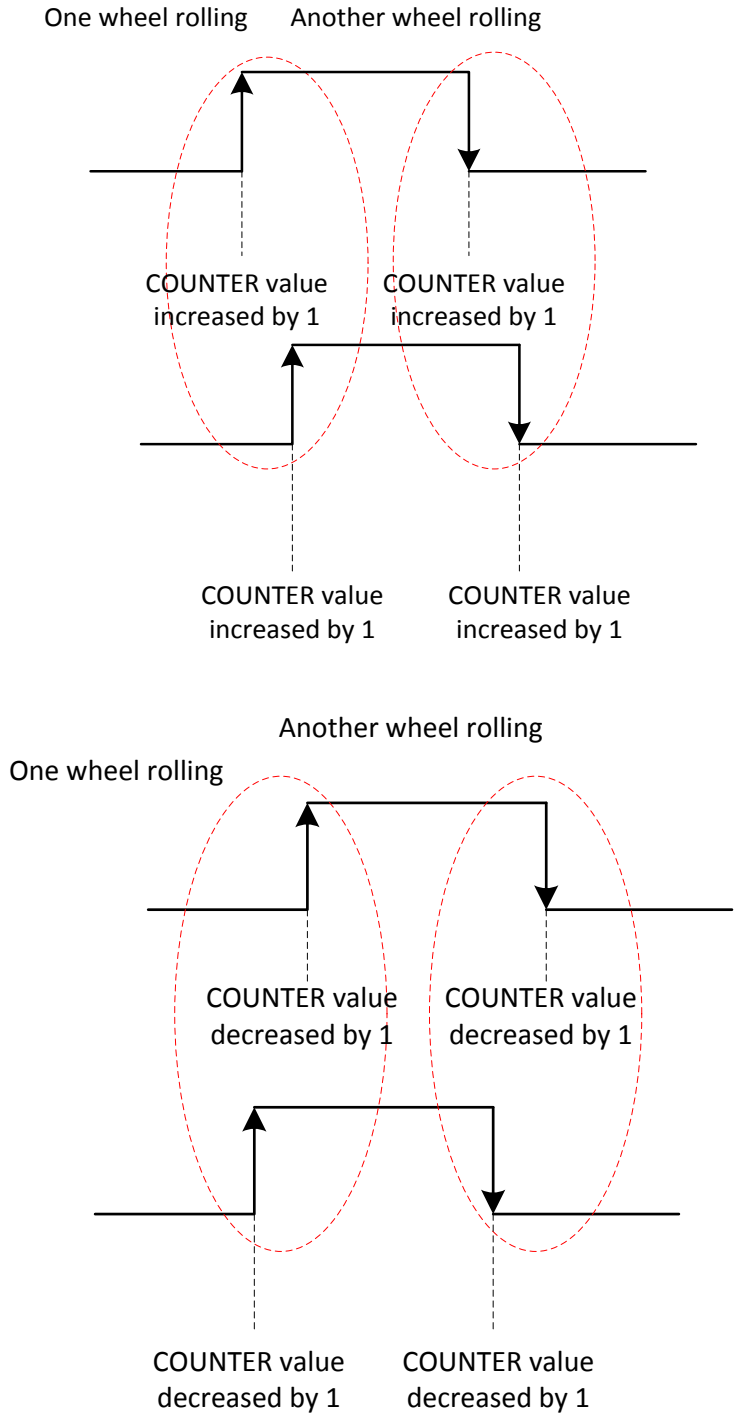


Figure 9- 2 Double accuracy mode

9.3 Read real time counting value

Neither can Hardware Counter value be read directly via software, nor can the counting value in address 0xd0 be updated automatically.

To read real time counting value, first write address 0xd8[0] with 1b'1 to load

Hardware Counter data into the QDEC_COUNT register, then read address 0xd0.

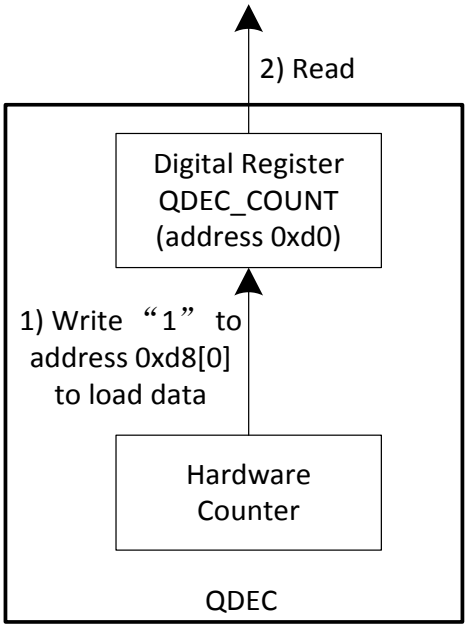


Figure 9- 3 Read real time counting value

9.4 QDEC interrupt

Address 0xd4[0] serves to enable or mask QDEC interrupt.

If address 0xd4[0] is set to 1b’1 to enable QDEC interrupt, whenever counter value changes, an QDEC IRQ is asserted and address 0xd5[0] is set to 1b’1 automatically. Writing 1b’1 to address 0xd5[0] can clear the interrupt flag bit.

9.5 QDEC reset

Address 0xd6[0] serves to reset the QDEC. The QDEC Counter value is cleared to zero.

9.6 Other configuration

The QDEC supports hardware debouncing. Address 0xd1[2:0] serves to set filtering window duration. All jitter with period less than the value will be filtered out and thus does not trigger count change.

Address 0xd1[4] serves to set input signal initial polarity.

Address 0xd1[5] serves to enable shuttle mode. Shuttle mode allows non-overlapping two phase signals as shown in the following figure.

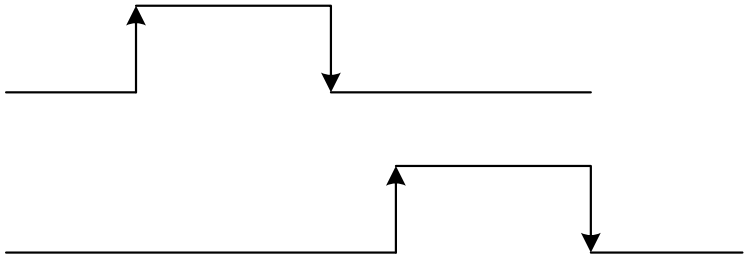


Figure 9- 4 Shuttle mode

Both address 0xd7[1] and 0x6e[5] should be set to 1b'1 to enable QDEC wakeup source.

9.7 Register table

Table 9- 2 Register table for QDEC

Address	Mnemonic	Type	Description	Reset value
0xd0	QDEC_COUNT	R	QDEC Counting value (read to clear): Pulse edge number	
0xd1	QDEC_CC	R/W	[2:0] : filter time (can filter 2^n *clk_32k*2 width de glitch) [4]: pola, input signal pola 0: no signal is low, 1: no signal is high [5]:shuttle mode 1 to enable shuttle mode	
0xd2	QDEC_CHNA0	R/W	[4:0] QDEC0 input pin select for channel a choose 1 of 11 pins for input channel a	0x00
0xd3	QDEC_CHNB0	R/W	[4:0] QDEC0 input pin select for channel b choose 1 of 11 pins for input channel b	0x01
0xd4	QDEC_MASK	R/W	[0]Interrupt mask 1: enable 0: mask	0x00
0xd5	QDEC_INT	R	[0]Interrupt flag Write 1 to clear	
0xd6	QDEC_RST	R/W	[0]Write 1 to reset QDEC	0x0

Address	Mnemonic	Type	Description	Reset value
0xd7	QDEC_DOUBLE	R/W	[0]Enable double accuracy mode [1]wakeup_en	0x0
0xd8	DATA_LOAD	R/W	[0]write 1 to load data when load completes it will be 0	

10 Comparator

10.1 Function description

The TLSR8366 embeds an internal comparator; its block diagram is shown as Figure 10-1:

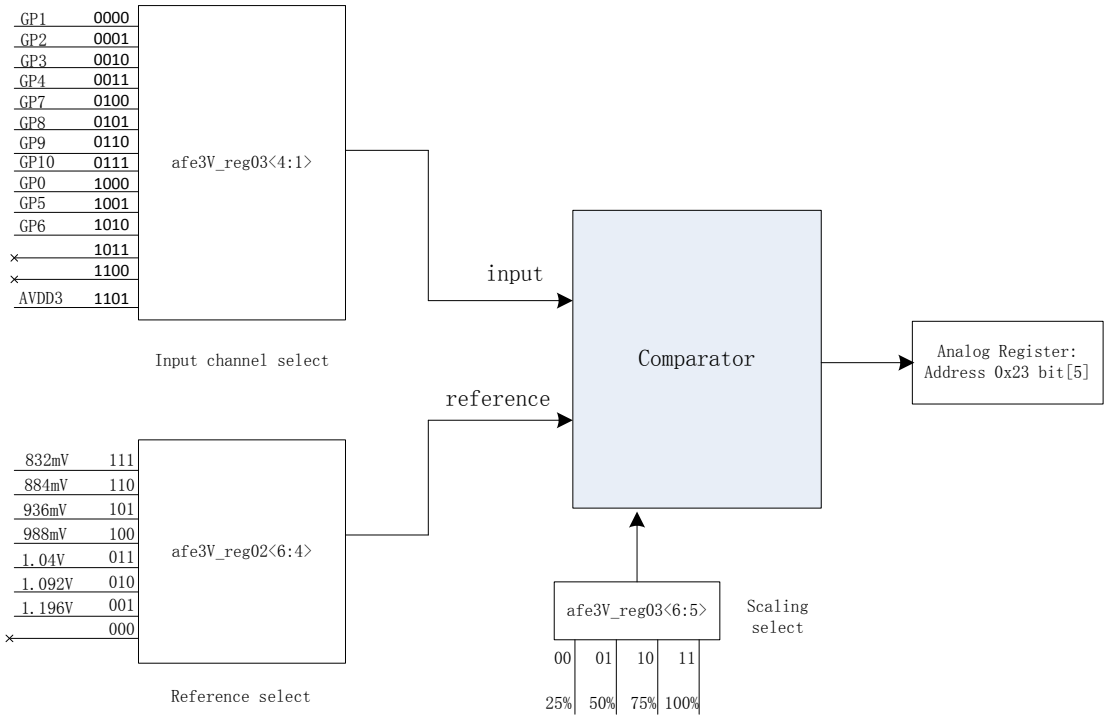


Figure 10- 1 Block diagram of comparator

The comparator is to compare the value of [input voltage *scaling] with reference voltage input.

As shown in Figure 10-1, analog register afe3V_reg03<4:1> is used to select one channel as input and register afe3V_reg02<6:4> is to select reference voltage input channel.

Analog register afe3V_reg03<6:5> is to select one of the four scaling options: 25%, 50%, 75% and 100%.

Please refer to Table 10-2 for concrete configuration.

If internal reference is used, we can detect 28 input voltage levels by setting the scaling factor. Table 10-1 shows the input voltage levels that can be detected. (Note:

Input voltage should not exceed the power supply of the ASIC.)

Table 10- 1 Input voltage levels

Internal reference（V）	Scaling factor	Equivalent reference（V）
0.832	100%	0.832
0.884	100%	0.884
0.936	100%	0.936
0.988	100%	0.988
1.04	100%	1.04
1.092	100%	1.092
1.196	100%	1.196
0.832	75%	1.109333
0.884	75%	1.178667
0.936	75%	1.248
0.988	75%	1.317333
1.04	75%	1.386667
1.092	75%	1.456
1.196	75%	1.594667
0.832	50%	1.664
0.884	50%	1.768
0.936	50%	1.872
0.988	50%	1.976
1.04	50%	2.08
1.092	50%	2.184
1.196	50%	2.392
0.832	25%	3.328
0.884	25%	3.536
0.936	25%	3.744
0.988	25%	3.952
1.04	25%	4.16
1.092	25%	4.368
1.196	25%	4.784

Distribution of the equivalent reference that can be set is shown in Figure 10-2.

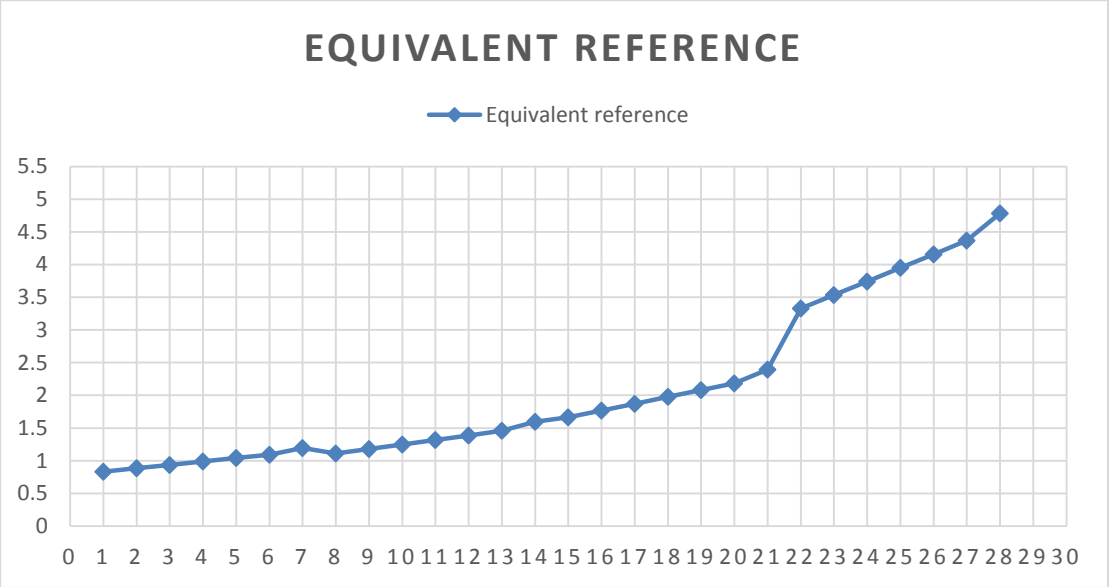


Figure 10- 2 Distribution of equivalent reference

The comparison principle is as follows: if the value of [input voltage *scaling] is larger than reference voltage input, the output will be low (“0”); and on the contrary, if the value of [input voltage *scaling] is lower than reference voltage input, the output will be high (“1”).

The user can read the register to get the result of comparison which is output to analog register with address 0x23 bit[5].

10.2 Register configuration

Table 10- 2 Analog register configuration related to comparator

Address	Name	Description	Default Value
afe3V_reg02<6:4>	comp_refsel<2:0>	Reference select: 111: 832mV reference 110: 884mV reference 101: 936mV reference 100: 988mV reference 011: 1.04V reference	000

Address	Name	Description	Default Value
		010: 1.092V reference 001: 1.196V reference 000: Float	
afe3V_reg03<0>	pd_I10u	Power down comparator reference generator 0: Power on 1: power down	0
afe3V_reg03<4:1>	comp_chsel<3:0>	Input Channel select: 0000: GP1 0001: GP2 0010: GP3 0011: GP4 0100: GP7 0101: GP8 0110: GP9 0111: GP10 1000: GP0 1001: GP5 1010: GP6 1011: NC 1100: NC 1101: AVDD3	1111
afe3V_reg03<6:5>	comp_refscale<1:0>	Reference voltage scaling: 00: 25% 01: 50% 10: 75% 11: 100%	01

11 Key Electrical Specifications

11.1 Absolute maximum ratings

Table 11- 1 Absolute Maximum Ratings

Characteristics	Sym.	Min.	Max	Unit	Test Condition
Supply Voltage	V_{Bus}	-0.5	6.5	V	Only VBUS pin is tested, and all VDD pins leave open
	VDD	-0.3	3.9	V	All AVDD and DVDD pin must have the same voltage
Voltage on Input Pin	V_{In}	-0.3	VDD +0.3	V	
Output Voltage	V_{Out}	0	VDD	V	
Storage temperature Range	T_{Str}	-65	150	°C	
Soldering Temperature	T_{Sld}		260	°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

11.2 Recommended operating condition

Table 11- 2 Recommended operation condition

Item	Sym.	Min	Typ.	Max	Unit	Condition
Power-supply voltage	VDD	1.9	3.3	3.6	V	
	V_{Bus}	4.5	5.0	5.5	V	
Operating Temperature Range	T_{Opr}	-40	27	85	°C	

11.3 DC characteristics

Table 11- 3 DC characteristics

Item	Sym.	Min	Typ.	Max	Unit	Condition
Tx current, only transmitter	I_{Tx1}	17	23	29	mA	Continuous Tx transmission @maximum output power, AVDD3=DVDD3=3.3V, Single tone signal
Tx current, whole chip	I_{Tx2}	21	28.7	36	mA	
Rx current, only receiver	I_{Rx1}	10	12.7	15	mA	Continuous Rx reception, AVDD3=DVDD3=3.3V
Rx current, whole chip	I_{Rx2}	15	18.8	23	mA	
Suspend current	I_{Susp}	-	10	20	uA	AVDD3=DVDD3=3.3V
		-	120	170	uA	VBUS=5V supply
Deep sleep current	I_{Deep}	-	0.7	5	uA	AVDD3=DVDD3=3.3V
		-	111	155	uA	VBUS=5V supply

*Note: All tests above are done at room temperature (T=25℃).

11.4 AC characteristics

Table 11- 4 AC Characteristics

Item	Sym.	Min	Typ.	Max	Unit	Condition
Digital inputs/outputs						
Input high voltage	VIH	0.7VDD		VDD	V	
Input low voltage	VIL	VSS		0.3VDD	V	
Output high voltage	VOH	VDD-0.3		VDD	V	
Output low voltage	VOL	VSS		0.3	V	
USB characteristics						
USB Output Signal Cross-over Voltage	V_{Crs}	1.3	-	2.0	V	
RF performance						
Item		**Min**	**Typ**	**Max**	**Unit**	
RF_Rx performance						
Sensitivity*[1]	2Mbps	-89	-87	-85	dBm	Tested on 4-layer board, PER (Packet Error Rate)≤1%
Frequency Offset Tolerance		-300		+300	KHz	
Co-channel rejection			-5		dB	

[1] Packet format to test sensitivity: Suppose payload length is 160 bits, the packet format should be Preamble (32bits) + Access code (32bits) + PIDF (9bits) + payload (160bits) + CRC (16bits) + padding (10bits).
The TLSR8366 SDK only uses the following channels (unit: MHz): 2402, 2403, 2404, 2405, 2406, 2407, 2408, 2411, 2413, 2414, 2418, 2446, 2450, 2455, 2456, 2457, 2458, 2459, 2460, 2461, 2466, 2467, 2468, 2469.

Item	Sym.	Min	Typ.	Max	Unit	Condition
In-band blocking rejection (Single Tone Interference)	±1 MHz offset		-9		dB	
	-2 MHz offset		20		dB	
	+2 MHz offset		5		dB	
	-3 MHz offset		20		dB	
	+3 MHz offset		18		dB	
	>4MHz offset		28		dB	
In-band blocking rejection (Equal Modulation Interference)	±1MHz offset		-9		dB	
	-2 MHz offset		-2		dB	
	+2 MHz offset		-3		dB	
	-3 MHz offset		12		dB	
	+3 MHz offset		9		dB	
	>4MHz offset		18		dB	
Image rejection			44		dB	
RF_Tx performance						
Output power			7		dBm	

Item	Sym.	Min	Typ.	Max	Unit	Condition
Modulation 20dB bandwidth			2.8		MHz	
Frequency Deviation		450	500	550	kHz	@2Mbps, modulation index=0.5
16MHz crystal						
Nominal frequency (parallel resonant)	f_{NOM}		16		MHz	
Frequency tolerance	f_{TOL}			±60	Ppm	
Load capacitance	C_L	5	12	18	pF	Programmable on chip load cap
Equivalent series resistance	ESR		50	100	ohm	
32MHz RC oscillator						
Nominal frequency	f_{NOM}		32		MHz	
Frequency tolerance	f_{TOL}		1		%	On chip calibration
32kHz RC oscillator						
Nominal frequency	f_{NOM}		32		kHz	
Frequency tolerance	f_{TOL}		1		%	On chip calibration
Calibration time			3		ms	

12 Applications

12.1 Application example for the TLSR8366ET32

12.1.1 Schematic

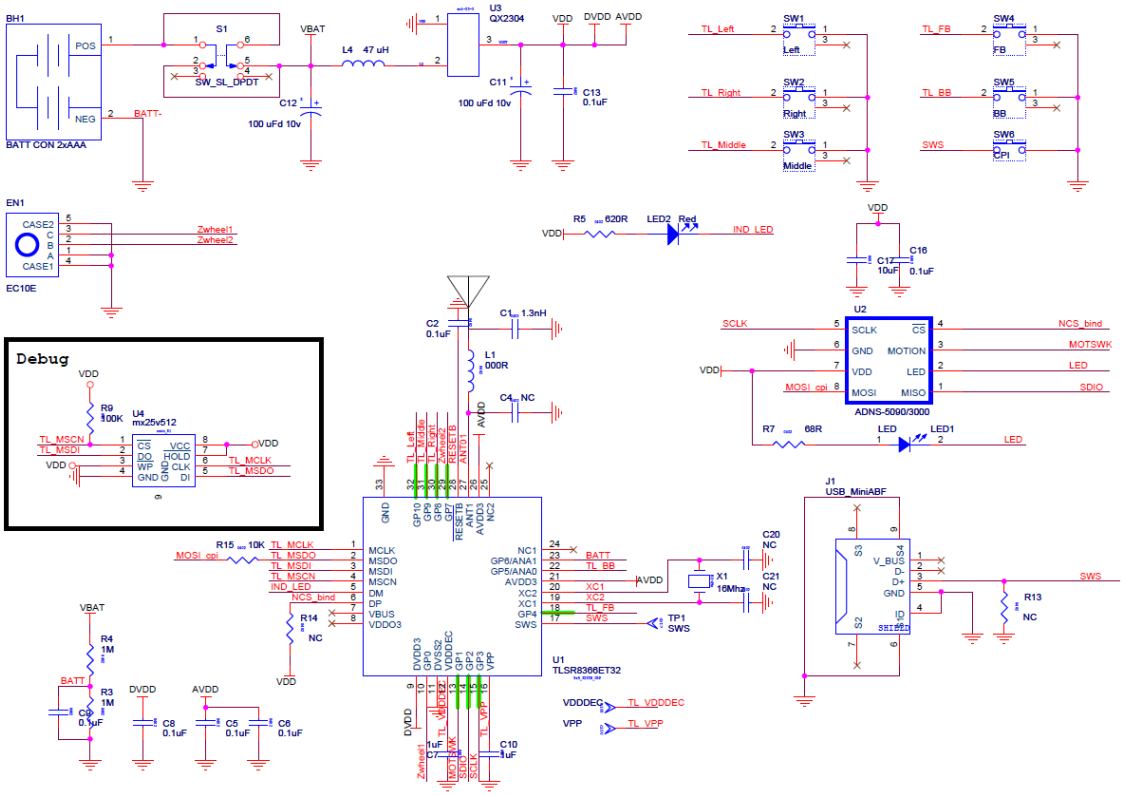


Figure 12- 1 Schematic for the TLSR8366ET32

12.1.2 Layout

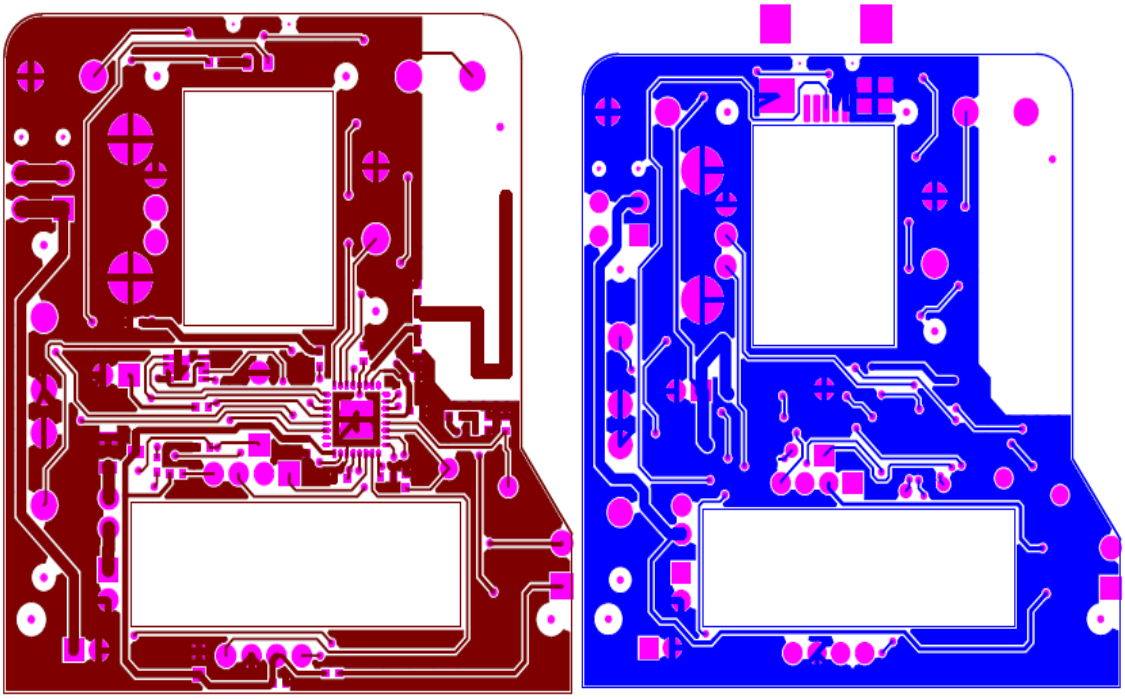


Figure 12- 2 Layout for the TLSR8366ET32

(Left: top view; Right: bottom view)

12.1.3 BOM (Bill of Material)

Table 12- 1 BOM table for the TLSR8366ET32

Quantity	Reference	Value
1	BH1	BATT CON 2xAAA
7	C2	0.1uF
	C5	0.1uF
	C6	0.1uF
	C8	0.1uF
	C9	0.1uF
	C13	0.1uF
	C16	0.1uF
2	C7	1uF
	C10	1uF
2	C11	100 uFd 10v
	C12	100 uFd 10v
1	C17	10uF
1	EN1	EC10E
1	J1	USB_MiniABF
1	LED1	LED

Quantity	Reference	Value
1	LED2	Red
1	L1	000R
1	L4	47 uH
2	R3	1M
	R4	1M
1	R5	620R
1	R7	68R
1	R9	100K
1	R15	10K
1	SW1	Left
1	SW2	Right
1	SW3	Middle
1	SW4	FB
1	SW5	BB
1	SW6	CPI
1	U1	TLSR8366ET32
1	U2	ADNS-5090/3000
1	U3	QX2304
1	U4	mx25v512
1	X1	16Mhz
1	C1	1.3nH

12.2 Application example for the TLSR8366ET24

12.2.1 Schematic

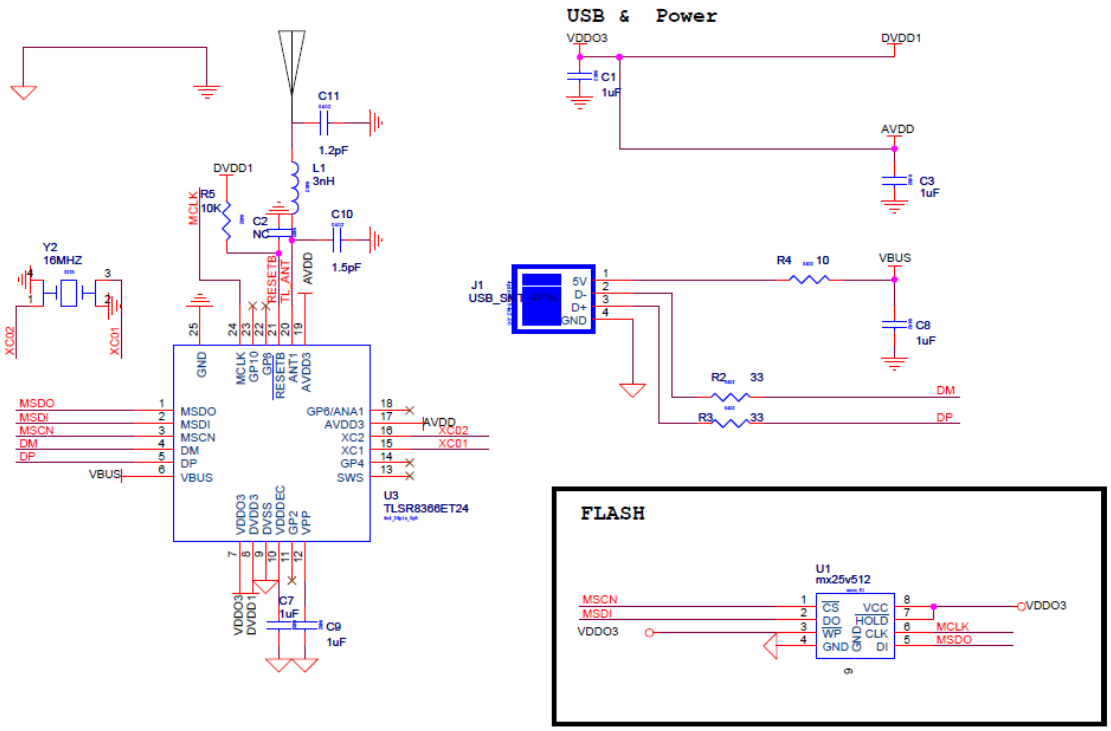


Figure 12- 3 Schematic for the TLSR8366ET24

12.2.2 Layout

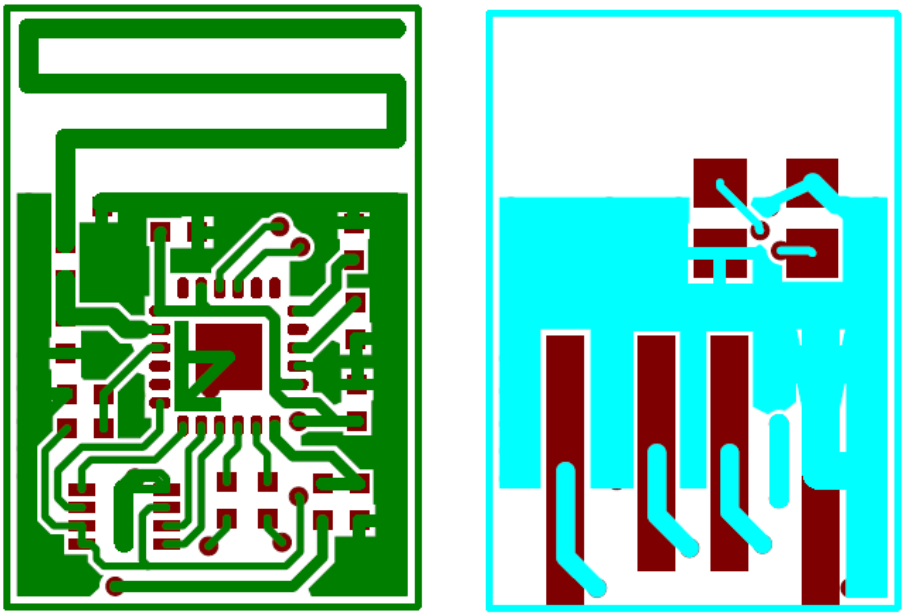


Figure 12- 4 Layout for the TLSR8366ET24

(Left: top view; Right: bottom view)

12.2.3 BOM (Bill of Material)

Table 12- 2 BOM table for the TLSR8366ET24

Quantity	Reference	Value
4	C1	1uF
	C7	1uF
	C8	1uF
	C9	1uF
1	C3	1uF
1	J1	USB_SMT_4PIN
1	C11	1.2pF
1	C10	1.5pF
1	L1	3nH
2	R2	33
	R3	33
1	R4	10
1	R5	10K
1	TP2	3V3
1	U1	mx25v512
1	U3	TLSR8366ET24
1	Y2	16MHZ

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