VEEK-MT-SoCKit

VEEK with Multi-touch Capacitive Panel

User Manual

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CONTENTS

Chapter 1

Introduction

The Video and Embedded Evaluation Kit - Multi-touch on SoCKit (VEEK-MT-SoCKit) is a comprehensive design platform with everything embedded developers need to create processing-based systems. VEEK-MT-SoCKit delivers an integrated system that includes hardware, design tools, intellectual property (IP) and reference designs for developing embedded software and hardware in a wide range of applications. The fully integrated kit allows developers to rapidly customize their processor and IP to best suit their specific application. The VEEK-MT-SoCKit features the SoC development board targeting Altera Cyclone® V SX SoC FPGA, as well as a capacitive LCD multimedia color touch panel, which natively supports multi-touch gestures. A 5-megapixel digital image sensor, ambient light sensor, and 3-axis accelerometer make up the rich feature set.

The all-in-one embedded solution offered on the VEEK-MT-SoCKit, a combination of LCD touch panel and digital image module, provides embedded developers the ideal platform for multimedia applications with parallel processing performance. Developers can benefit from the use of FPGA-based embedded processing system such as mitigating design risk and obsolescence, design reuse, reducing bill of material (BOM) costs by integrating powerful graphics engine within the FPGA, and lower cost.

For SoC Linux reference design for touch-screen display, please refer to the document “Programming Guide for Touch-Screen Display” in the CD for VEEK-MT-SoCKit.

Figure 1-1 shows the photo of VEEK-MT-SoCKit.

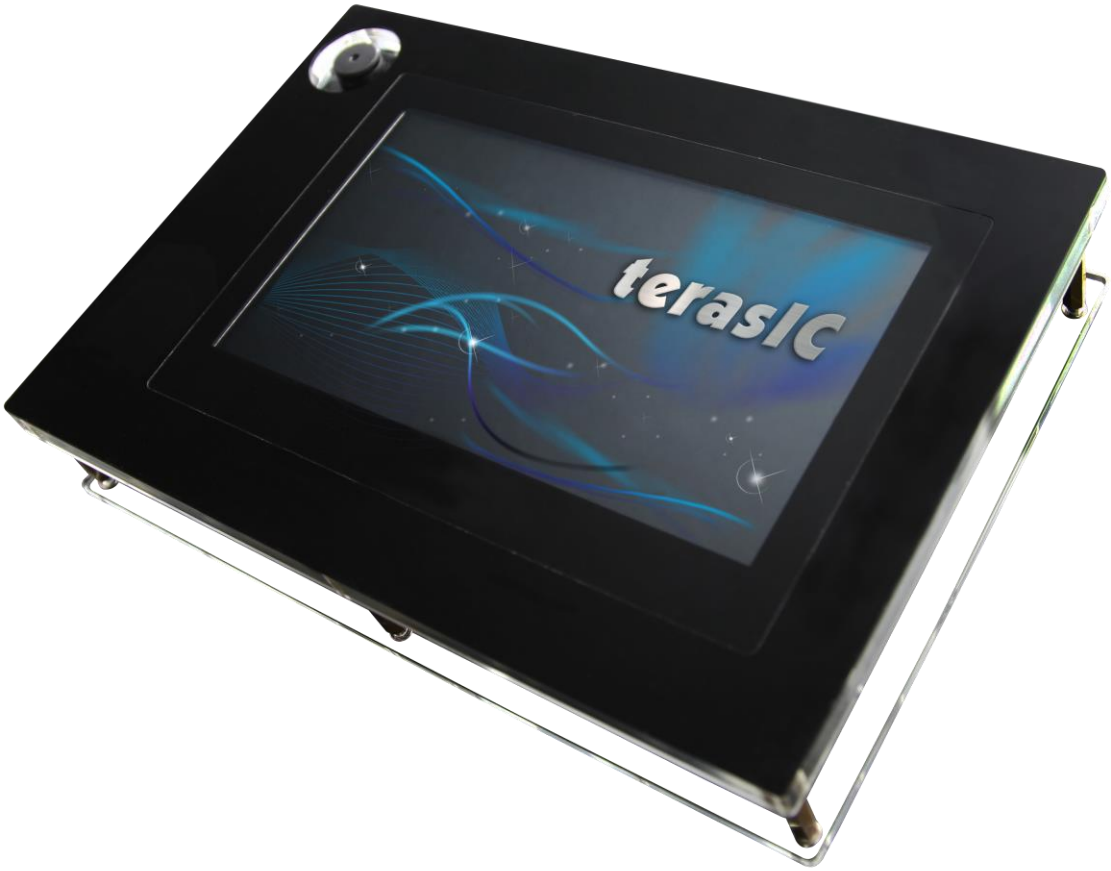

Figure 1-1 The VEEK-MT-SoCKit board

The key features are listed below:

1.1 Key Features

■ SoCKit Main Board

- Cyclone V SX SoC—5CSXFC6D6F31C6N
  - Dual-core ARM Cortex-A9 (HPS)
  - 110K LEs, 41509 ALMs
  - 5,140 M10K memory blocks
  - 224 18x18 Multiplier
  - 6 FPGA PLLs and 3 HPS PLLs.
  - 2 Hard Memory Controllers
  - 3.125G Transceivers

- Configuration Sources
  - Quad Serial Configuration device – EPCQ256 for FPGA
  - Onboard USB-Blaster II Controller

- Memory Devices
  - 1GB (2x256MBx16) DDR3 SDRAM for FPGA
  - 1GB (2x256MBx16) DDR3 SDRAM for HPS
  - 128MB QSPI Flash for HPS
  - MicroSD Card Socket for HPS
- Communication
  - USB 2.0 OTG (ULPI interface with micro USB type AB connector)
  - USB to UART (micro USB type B connector)
  - 10/100/1000 Ethernet

- Connectors
  - One HSMC (8-channel transceivers, configurable I/O standards 1.5/1.8/2.5/3.3V)
  - One LTC connector (One Serial Peripheral Interface (SPI) Master, one I2C, and one GPIO interface)

- Display
  - 24-bit VGA DAC
  - 128x64 dots LCD Module with backlight

- Audio
  - 24-bit CODEC, Line-in, Line-out, and Microphone-in jacks

- Switches, Buttons and LEDs
  - 8 User Keys (FPGA x4 ; HPS x 4)
  - 8 User Switches (FPGA x4 ; HPS x 4)
  - 8 User LEDs (FPGA x4 ; HPS x 4)
  - 2 HPS Reset Buttons (HPS_RSET_n and HPS_WARM_RST_n)

- Sensor
  - G-sensor for HPS
  - Temperature Sensor for FPGA

- Power
  - 12V DC Input

■ Capacitive LCD Touch Screen

- Equipped with a 7-inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module
- Module composed of LED backlight
- Support 24-bit parallel RGB interface
- Converting the X/Y coordination of touch point to its corresponding digital data via the Touch controller.

Table 1-1 shows the general physical specifications of the touch screen (Note*).

Table 1-1 General Physical Specifications of the LCD

Item	*Specification*	*Unit*
LCD size	7-inch (Diagonal)	-
Resolution	800 x3(RGB) x 480	dot
Dot pitch	0.1926(H) x0.1790 (V)	mm
Active area	154.08 (H) x 85.92 (V)	mm
Module size	164.9(H) x 100.0(V) x 5.7(D)	mm
Surface treatment	Glare	-
Color arrangement	RGB-stripe	-
Interface	Digital	-

■ 5-Megapixel Digital Image Sensor

- Superior low-light performance
- High frame rate
- Global reset release, which starts the exposure of all rows simultaneously
- Bulb exposure mode, for arbitrary exposure times
- Snapshot-mode to take frames on **demand**
- Horizontal and vertical mirror image
- Column and row skip modes to reduce image size without reducing field-of-view
- Column and row binning modes to improve image quality when resizing
- Simple two-wire serial interface
- Programmable controls: gain, frame rate, frame size, exposure

Table 1-2 shows the key parameters of the CMOS sensor (Note*).

Table 1-2 Key Performance Parameters of the CMOS Sensor

Parameter		*Value*
Active pixels		2592Hx1944V
Pixel size		2.2umx2.2um
Color filter array		RGB Bayer pattern
Shutter type		Global reset release(GRR)
Maximum data rate/master clock		96Mp/s at 96MHz
Frame rate	Full resolution	Programmable up to 15 fps
	VGA mode	Programmable up to 70 fps
ADC resolution		12-bit
Responsivity		1.4V/lux-sec(550nm)
Pixel dynamic range		70.1dB
SNRMAX		38.1dB
Supply voltage	Power	3.3V
	I/O	1.7V～3.1V

■ Digital Accelerometer

- Up to 13-bit resolution at +/- 16g
- SPI (3-wire and 4-wire) digital interface
- Flexible interrupts modes

■ Ambient Light Sensor

- Approximates human-eye response
- Precise luminance measurement under diverse lighting conditions
- Programmable interrupt function with user-defined upper and lower threshold settings
- 16-bit digital output with I2C fast-mode at 400 kHz
- Programmable analog gain and integration time
- 50/60-Hz lighting ripple rejection

Note: For more detailed information about the LCD touch panel and CMOS sensor module, please refer to their datasheets in the CD.

1.2 Setup License for Terasic Multi-touch IP

To utilize the multi-touch panel in a Quartus II project, a Terasic Multi-Touch IP is required. After the license file for Quartus II is installed, there is one more license file needed to implement Terasic's Multi-touch IP. Error messages will be displayed if the license file is not added before compiling projects using Terasic Multi-touch IP. The license file is located at:

VEEK-MT-SoCKit System CD\License\license_multi_touch.dat

There are two ways to install the License. The first one is to add the path of license file (license_multi_touch.dat) in Quartus II, as shown in **Figure 1-2**.

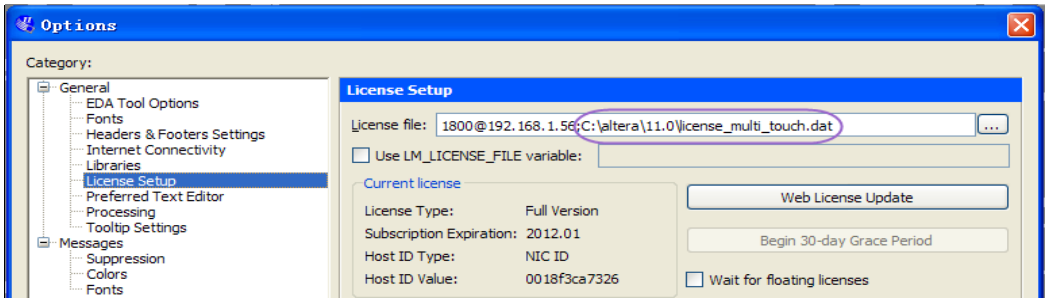

Figure 1-2 License setup

The other one is to add license content to the existing license file. The procedures are listed below:

1. Use Notepad or other text editing software to open the file license_multi_touch.dat.
2. The license contains the FEATURE lines required to license the IP Cores as shown in **Figure 1-3**.

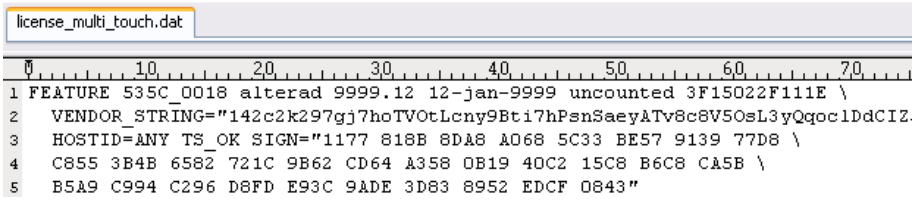

Figure 1-3 Contents of license_multi_touch.dat

3. Open your Quartus II license.dat file in a text editor.
4. Copy everything under the license_multi_touch.dat and paste it to your Quartus II license file. (Note: Do not delete any FEATURE lines from the Quartus II license file. Doing so will result in an unusable license file.) .
5. Save the Quartus II license file.

1.3 System CD

The VEEK-MT-SoCKit System CD containing documentations and supporting materials, including the User Manual, reference designs, touch-screen IP and its license, and device datasheets. Users can download this System CD form the link: http://cd-veek-mt-sockit.terasic.com. **Table 1-3** shows the content of System CD.

Table 1-3 Directory of the System CD

Folder Name	*Description*
Datasheet	**Datasheet for the major components on the kit.**
Demonstrations	**FPGA and SoC reference codes.**
IP	**touch-screen IP**
License	**License of touch-screen IP**
User_Manaual	**User Manual (this manual)**

1.4 Getting Help

Here is the contact information should you encounter any problem:

- Terasic Technologies
- Tel: +886-3-575-0880
- Email: support@terasic.com

Chapter 2

Architecture

This chapter describes the architecture of the VEEK-MT-SoCKit including block diagram and components.

2.1 Layout and Components

The picture of the VEEK-MT-SoCKit is shown in **Figure 2-1** and **Figure 2-2**. It depicts the layout of the board and indicates the locations of connectors and key components.

Figure 2-1 VEEK-MT-SoCKit PCB and component diagram (top view)

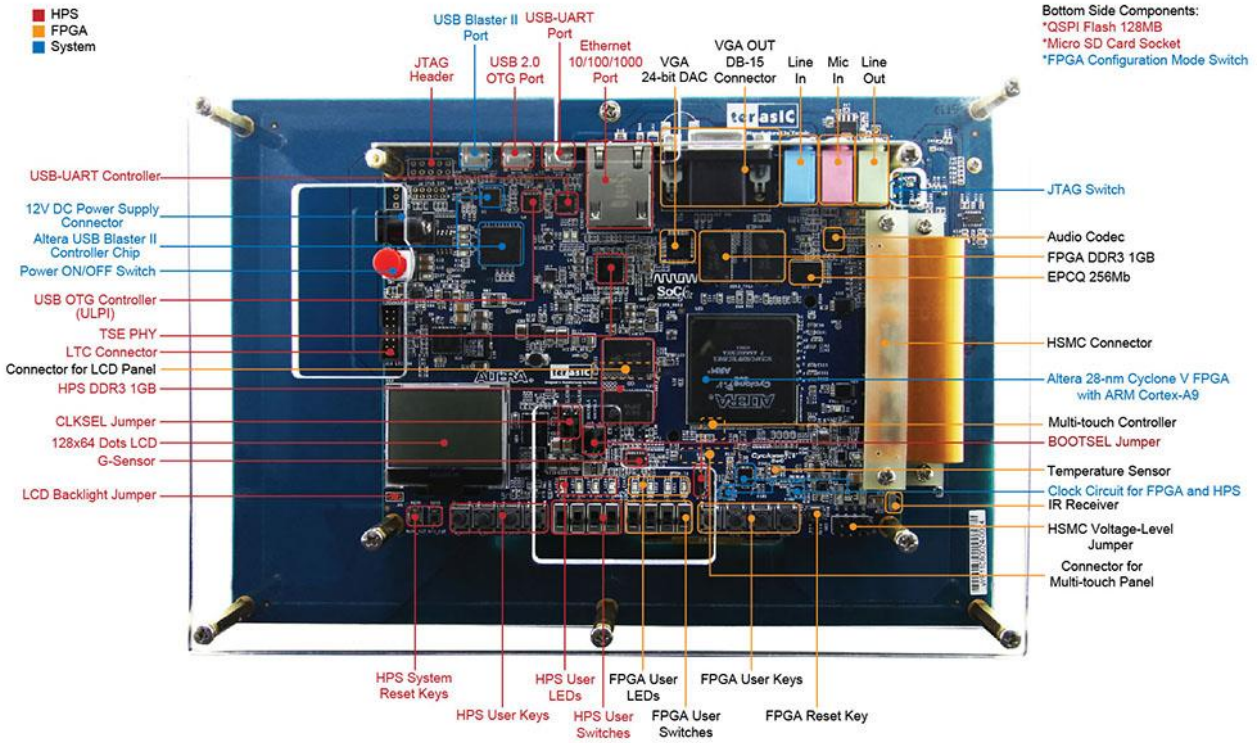

Figure 2-2 VEEK-MT-SoCKit PCB and component diagram (bottom view)

2.2 Block Diagram of the VEEK-MT-SoCKit

Figure 2-3 gives the block diagram of the VEEK-MT-SoCKit board. VEEK-MT-SoCKit is a combination of Cyclone V GX SoC development board and a Multi-touch LCD Camera Card (MTLC) connected via the HSMC connector. MTLC module is not only equipped with a 7"LCD screen, it also equips a 5-Megapixel digital image sensor module, G-sensor and Light sensor. All these sensors connect to the FPGA device via the HSMC connector, so they can be controlled and directly used by the FPGA device.

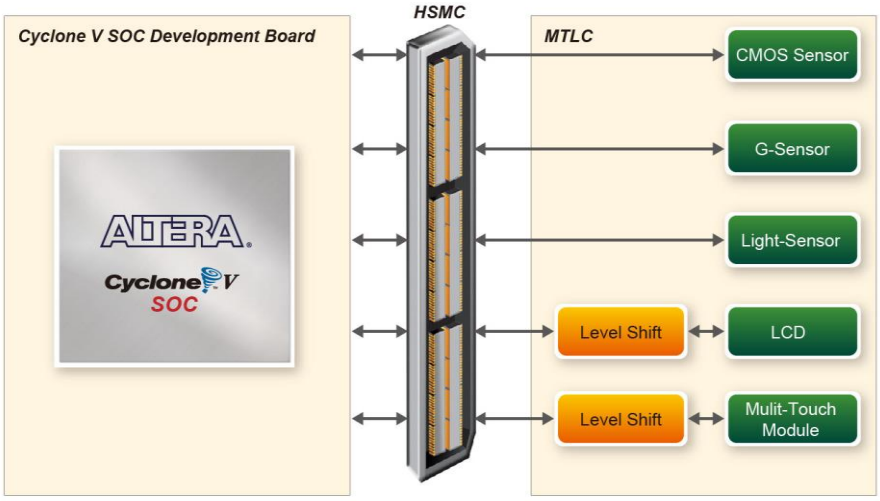

Figure 2-3 Block diagram of VEEK-MT-SoCKit

Chapter 3

Using VEEK-MT-SoCKit

This section describes the detailed information about the components, connectors, and pin assignments of the VEEK-MT-SoCKit.

3.1 Using the SoCKit Main Board

The VEEK-MT-SoCKit is composed of SoCKit SoC development board and 7" touch panel daughter card. The SoCKit SoC development board, which is equipped with the FPGA device, is considered as the majority part. The user manual and CD of SoCKit main board are available at: http://cd-sockit.terasic.com.

3.2 Using the 7” LCD Capacitive Touch Screen

The VEEK-MT-SoCKit features a 7-inch capacitive amorphous TFT-LCD panel. The LCD touch screen offers resolution of 800x480 to provide users the best display quality for developing applications. The LCD panel supports 24-bit parallel RGB data interface.

The VEEK-MT-SoCKit is also equipped with a Touch controller, which can read the coordinates of the touch points through the serial port interface of the Touch controller.

To display images on the LCD panel correctly, the RGB color data along with the data enable and clock signals must act according to the timing specification of the LCD touch panel, as shown in **Table 3-1. Table 3-2** gives the pin assignment information of the LCD touch panel.

Table 3-1 LCD Timing Specifications

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
DCLK	Dot Clock	1/tCLK		33		MHZ	
	DCLK pulse duty	Tcwh	40	50	60	%	
DE	Setup time	Tesu	8			ns	
	Hold time	Tehd	8			ns	
	Horizontal period	tH		1056		tCLK	

	Horizontal Valid	tHA		800		tCLK	
	Horizontal Blank	tHB		256		tCLK	
	Vertical Period	tV		525		tH	
	Vertical Valid	tVA		480		tH	
	Vertical Blank	tVB		45		tH	
SYNC	HSYNC setup time	Thst	8			ns	
	HSYNC hold time	Thhd	8			ns	
	VSYNC Setup Time	Tvst	8			ns	
	VSYNC Hold Time	Tvhd	8			ns	
	Horizontal Period	th		1056		tCLK	
	Horizontal Pulse Width	thpw		30		tCLK	thb+thpw=46DCLK is fixed
	Horizontal Back Porch	thb		16		tCLK	
	Horizontal Front Porch	thfp		210		tCLK	
	Horizontal Valid	thd		800		tCLK	
	Vertical Period	tv		525		th	
	Vertical Pulse Width	tvpw		13		th	tvpw + tvb = 23th is fixed
	Vertical Back Porch	tvb		10		th	
	Vertical Front Porch	tvfp		22		th	
	Vertical Valid	tvd		480		th	
DATA	Setup time	Tdsu	8			ns	
	Hold time	Tdsu	8			ns	

Table 3-2 Pin Assignment of the LCD Touch Panel

Signal Name	FPGA Pin No.	Description	I/O Standard
LCD_B0	C4	LCD blue data bus bit 0	2.5V
LCD_B1	D5	LCD blue data bus bit 1	2.5V
LCD_B2	A3	LCD blue data bus bit 2	2.5V
LCD_B3	A4	LCD blue data bus bit 3	2.5V
LCD_B4	E11	LCD blue data bus bit 4	2.5V
LCD_B5	F11	LCD blue data bus bit 5	2.5V
LCD_B6	F8	LCD blue data bus bit 6	2.5V
LCD_B7	F9	LCD blue data bus bit 7	2.5V
LCD_DCLK	E6	LCD Clock	2.5V
LCD_DE	C3	Data Enable signal	2.5V
LCD_DIM	F13	LCD backlight enable	2.5V
LCD_DITH	H8	Dithering setting	2.5V
LCD_G0	D12	LCD green data bus bit 0	2.5V

LCD_G1	E12	LCD green data bus bit 1	2.5V
LCD_G2	D10	LCD green data bus bit 2	2.5V
LCD_G3	D11	LCD green data bus bit 3	2.5V
LCD_G4	D9	LCD green data bus bit 4	2.5V
LCD_G5	E9	LCD green data bus bit 5	2.5V
LCD_G6	B5	LCD green data bus bit 6	2.5V
LCD_G7	B6	LCD green data bus bit 7	2.5V
LCD_HSD	C12	Horizontal sync input.	2.5V
LCD_MODE	G8	DE/SYNC mode select	2.5V
LCD_POWER_CTL	G10	LCD power control	2.5V
LCD_R0	A13	LCD red data bus bit 0	2.5V
LCD_R1	B13	LCD red data bus bit 1	2.5V
LCD_R2	C9	LCD red data bus bit 2	2.5V
LCD_R3	C10	LCD red data bus bit 3	2.5V
LCD_R4	B8	LCD red data bus bit 4	2.5V
LCD_R5	C8	LCD red data bus bit 5	2.5V
LCD_R6	A8	LCD red data bus bit 6	2.5V
LCD_R7	A9	LCD red data bus bit 7	2.5V
LCD_RSTB	B1	Global reset pin	2.5V
LCD_SHLR	B3	Left or Right Display Control	2.5V
LCD_UPDN	B2	Up / Down Display Control	2.5V
LCD_VSD	B11	Vertical sync input.	2.5V
TOUCH _I2C_SCL	F14	touch I2C clock	2.5V
TOUCH _I2C_SDA	F15	touch I2C data	2.5V
TOUCH _INT_n	B12	touch interrupt	2.5V

3.3 Using 5-megapixel Digital Image Sensor

The VEEK-MT-SoCKit is equipped with a 5-megapixel digital image sensor that provide an active imaging array of 2,592H x 1,944V. It features low-noise CMOS imaging technology that achieve CCD image quality. In addition, it incorporates sophisticated camera functions on-chip such as windowing, column and row skip mode, and snapshot mode.

The sensor can be operated in its default mode or programmed through a simple two-wire serial interface for frame size, exposure, gain settings, and other parameters. **Table 3-3** contains the pin names and descriptions of the image sensor module.

Table 3-3 Pin Assignment of the CMOS Sensor

Signal Name	FPGA Pin No.	Description	I/O Standard
CAMERA_PIXCLK	AG2	Pixel clock	2.5V
CAMERA_D0	H14	Pixel data bit 0	2.5V
CAMERA_D1	G13	Pixel data bit 1	2.5V
CAMERA_D2	K12	Pixel data bit 2	2.5V
CAMERA_D3	J12	Pixel data bit 3	2.5V
CAMERA_D4	J10	Pixel data bit 4	2.5V
CAMERA_D5	J9	Pixel data bit 5	2.5V
CAMERA_D6	K7	Pixel data bit 6	2.5V
CAMERA_D7	K8	Pixel data bit 7	2.5V
CAMERA_D8	G12	Pixel data bit 8	2.5V
CAMERA_D9	G11	Pixel data bit 9	2.5V
CAMERA_D10	J7	Pixel data bit 10	2.5V
CAMERA_D11	H7	Pixel data bit 11	2.5V
CAMERA_STROBE	D6	Snapshot strobe	2.5V
CAMERA_LVAL	D7	Line valid	2.5V
CAMERA_FVAL	E8	Frame valid	2.5V
CAMERA_RESET_n	E4	Image sensor reset	2.5V
CAMERA_SCLK	AF9	Serial clock	2.5V
CAMERA_TRIGGER	C5	Snapshot trigger	2.5V
CAMERA_SDATA	AG7	Serial data	2.5V
CAMERA_XCLKIN	AJ2	External input clock	2.5V

3.4 Using the Digital Accelerometer

The VEEK-MT-SoCKit is equipped with a digital accelerometer sensor module. The ADXL345 is a small, thin, and ultralow-power-consumption 3-axis accelerometer with high resolution measurement. Digitalized output is formatted as 16-bit in two's complement and could be accessed either using SPI interface or I2C interface. This chip uses the 3.3V CMOS signaling standard. Main applications include medical instrumentation, industrial instrumentation, personal electronic aid, and hard disk drive protection etc. Some of the key features of this device are listed below. For more detailed information about this chip, please refer to its datasheet, which is available on manufacturer's website or under the **datasheet** folder of the system CD.

Table 3-4 Pin Names and Descriptions of the G Sensor Module.

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
GSENSOR_INT1	E3	Interrupt 1 output	2.5V
GSENSOR_INT2	E2	Interrupt 2 output	2.5V
GSENSOR_CS_n	D4	Chip Select	2.5V
GSENSOR_ALT_ADDR	E1	I2C Address Select	2.5V
GSENSOR_SDA_SDI_SDIO	D1	Serial Data	2.5V
GSENSOR_SCL_SCLK	D2	Serial Communications Clock	2.5V

3.5 Using the Ambient Light Sensor

The APDS-9300 is a low-voltage digital ambient light sensor that convert light intensity to digital signal output and communicate in I2C protocol. Each device consists of one broadband photodiode (visible plus infrared) and one infrared photodiode. Two integrating ADCs convert the photodiode currents to a digital output, which represents the irradiance measured from each channel. This digital output is entered to a microprocessor where luminance (ambient light level) in lux is derived using an empirical formula to approximate the human-eye response. For more detailed information about this chip, please refer to its datasheet, which is available on manufacturer's website or under the **datasheet** folder of the system CD.

Table 3-5 Pin Names and Descriptions of the Ambient Light Sensor Module.

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
LSENSOR_ADDR_SEL	A6	Chip select	2.5V
LSENSOR_INT	B7	Interrupt output	2.5V
LSENSOR_SCL	A5	Serial Communications Clock	2.5V
LSENSOR_SDA	C7	Serial Data	2.5V

3.6 Using Terasic Multi-touch IP

Terasic Multi-touch IP is provided for developers to retrieve user inputs, including multi-touch gestures and single-touch. The file name of this IP is **i2c_touch_config** and it is encrypted. To compile projects with the IP, users need to install the IP license first. For license installation, please refer to section **1.2 Setup License for Terasic Multi-touch IP** in this document. The license file is located in the following directory:

VEEK-MT-SoCKit System CD\License\license_multi_touch.dat

The IP decodes I2C information and outputs coordinate and gesture information. The IP interface is shown below:

```
module i2c_touch_config  (
            // Host Side
            iCLK,
            iRSTN,
            iTRIG,
            oREADY,
            oREG_X1,
            oREG_Y1,
            oREG_X2,
            oREG_Y2,
            oREG_TOUCH_COUNT,
            oREG_GESTURE,
            // I2C Side
            I2C_SCLK,
            I2C_SDAT
);
```

The purpose of signals associated with the IP is described in **Table 3-6.** The IP requires a 50 MHz signal as a reference clock to the **iCLK** pin and system reset signal to **iRSTN**. The pins **iTRIG**, **I2C_SCLK**, and **IC2_SDAT** should be connected to TOUCH_INT_n, TOUCH_I2C_SCL, and TOUCH_I2C_SDA signals on the 2x20 GPIO header respectively. When **oREADY** rises, it means there is touch activity, and associated information is given in the oREG_X1, oREG_Y1, oREG_X2, oREG_Y2, oREG_TOUCH_COUNT, and oREG_GESTURE pins.

For the control application, when touch activity occurs, it should check whether the value of oREG_GESTURE matches a pre-defined gesture ID defined in **Table 3-7.** If it is not a gesture, it means a single-touch is occurred and the relative X/Y coordinates can be derived from oREG_X1 and oREG_Y1.

Table 3-6 Interface Definitions of Terasic Multi-touch IP

Pin Name	*Direction*	*Description*
iCLK	**Input**	**Connect to 50MHz Clock**
iRSTN	**Input**	**Connect to system reset signal**
iTRIG	**Input**	**Connect to Interrupt Pin of Touch IC**
oREADY	**Output**	**Rising Trigger when following six output data is valid**
oREG_X1	**Output**	**10-bits X coordinate of first touch point**
oREG_Y1	**Output**	**9-bits Y coordinate of first touch point**
oREG_X2	**Output**	**10-bits X coordinate of second touch point**
oREG_Y2	**Output**	**9-bits Y coordinate of second touch point**
oREG_TOUCH_COUNT	**Output**	**2-bits touch count. Valid value is 0, 1, or 2.**
oREG_GESTURE	**Output**	**8-bits gesture ID (See Table 3-7)**
I2C_SCLK	**Output**	**Connect to I2C Clock Pin of Touch IC**
I2C_SDAT	**Inout**	**Connect to I2C Data Pin of Touch IC**

The supported gestures and IDs are shown in **Table 3-7.**

Table 3-7 Gestures and Associated ID

Gesture	*ID (hex)*
One Point Gesture	
North	**0x10**
North-East	**0x12**
East	**0x14**
South-East	**0x16**
South	**0x18**
South-West	**0x1A**
West	**0x1C**
North-West	**0x1E**
Rotate Clockwise	**0x28**
Rotate Anti-clockwise	**0x29**
Click	**0x20**
Double Click	**0x22**
Two Points Gesture	
North	**0x30**
North-East	**0x32**
East	**0x34**
South-East	**0x36**
South	**0x38**
South-West	**0x3A**
West	**0x3C**
North-West	**0x3E**
Click	**0x40**
Zoom In	**0x48**
Zoom Out	**0x49**

Note: The Terasic Multi-touch IP can also be found under the "IP" folder from the system CD..

Chapter 4

VEEK-MT-SoCKit Demonstrations

This chapter gives detailed description of the exclusive demonstrations implemented on FPGA of VEEK-MT-SoCKit. These demonstrations are specifically developed for VEEK-MT-SoCKit. The goal is to show the potential of the kit and bring out the unique benefits of FPGA-based SOPC systems such as reducing BOM costs by integrating powerful graphics and video processing circuits within the FPGA.

For SoC Linux reference design for touch-screen display, please refer to the document "Programming Guide for Touch-Screen Display" in the System CD of VEEK-MT-SoCKit.

4.1 System Requirements

To run and recompile the demonstrations, you should:

- Install Altera Quartus II v13.0 and Nios II EDS v13.0 or later edition on the host computer
- Install the USB-Blaster II driver.
- Copy the entire folder with demonstrations from the VEEK-MT-SoCKit system CD to the host computer.

4.2 Painter Demonstration

This section shows how to control the LCD and the touch controller to run a demo based on Qsys and Altera VIP Suite. The demonstration also shows how multi-touch gestures and single-touch coordinates operate.

Figure 4-1 shows the block diagram of the hardware system for this demonstration. For LCD display processing, the reference design is developed based on the Video and Image Processing Suite (VIP) from Altera. The Frame Reader from the VIP is used for reading content to be displayed from the associated video memory, and the Video Out from the VIP is used to display the content on the LCD. The display content is filled by Nios II processor according to users' input.

For multi-touch processing, the Terasic Memory-Mapped IP is used to retrieve user input, including multi-touch gesture and single-touch resolution. This IP is encrypted, so the license included in the

system CD should be installed before compiling any Quartus II project. For more information about this IP, please refer to the section **3.6 Using Terasic Multi-touch IP** in this document.

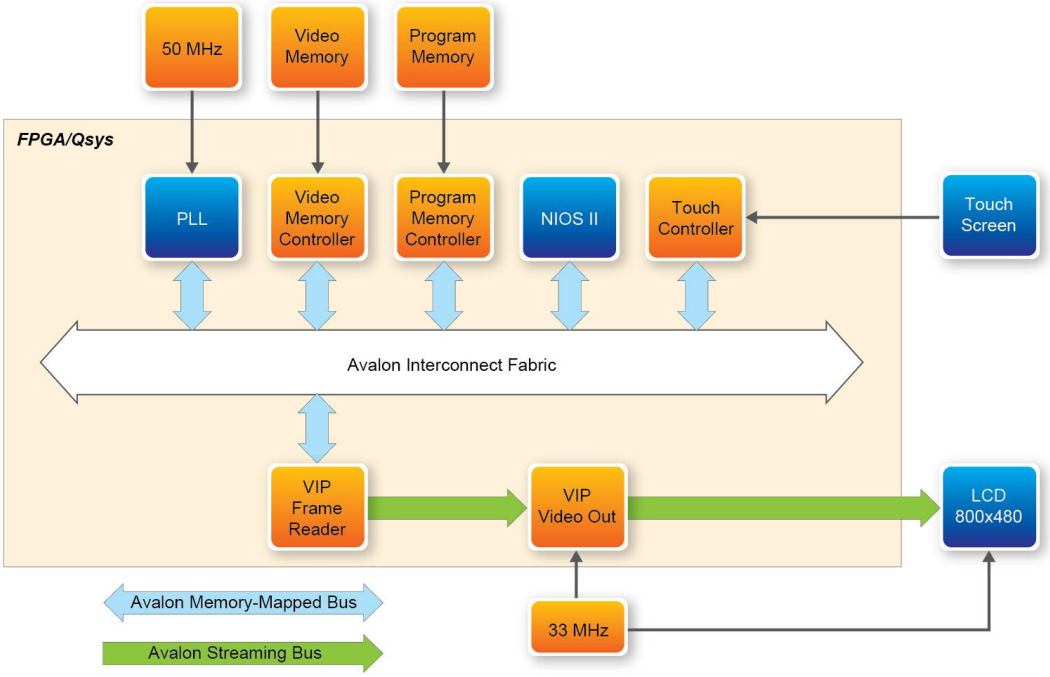

Figure 4-1 Block diagram of the Painter demonstration

■ Demonstration Source Code

- Project directory: System-CD\Demonstrations\FPGA\SoCKit_Painter
- Bit stream used: Painter.sof
- Nios II workspace: System-CD\Demonstrations\FPGA\SoCKit_Painter\software

■ Demonstration Batch File

Demo batch file directory: System-CD\Demonstrations\FPGA\SoCKit_Painter\demo_batch

The folder includes the following files:

- Batch file: test.bat and test_bashrc
- FPGA configuration file: SoCKit_Painter.sof
- Nios II program: SoCKit_MTLC_Painter.elf

■ Demonstration Setup

- Make sure both Quartus II and Nios II are installed on the host PC
- Power on the SoCKit board
- Connect a USB cable to the USB-Blaster port on the SoCKit board and install the USB-Blaster II driver if necessary.
- Configure the FPGA by executing the demo batch file "test.bat" from the directory "SoCKit_Painter\demo_batch" (Note*)
- After the programming is downloaded and executed successfully, you will see a painter GUI displayed on the LCD. **Figure 4-2** shows the GUI of the Painter demo**.**
- The GUI is classified into three areas: Palette, Canvas, and Gesture. Users can select pen color from the color palette and start painting in the Canvas area. If a gesture is detected, the associated gesture symbol is shown in the gesture area. Click the "Clear" button to To clean up the content in the Canvas area.
- **Figure 4-3** shows the photo when users paint in the canvas area. **Figure 4-4** shows the photo when counter-clockwise rotation gesture is detected. **Figure 4-5** shows the photo when zoom-in gesture is detected.

Figure 4-2 GUI of the Painter demo

Figure 4-3 Single touch painting

Figure 4-4 Counter-clockwise rotation gesture

Figure 4-5 Zoom-in gesture

Note: execute the test.bat from the folder SoCKit_Painter\demo_batch will automatically download the .sof and .elf files.

4.3 Camera Application

This demonstration shows a digital camera reference design using the 5-Megapixel CMOS sensor and 7-inch LCD module on the VEEK-MT-SoCKit. The CMOS sensor module sends raw image data to the FPGA, which handles image processing and converts the data to RGB format to display on the LCD module. The I2C Sensor Configuration module is used to configure the CMOS sensor module. **Figure 4-6** shows the block diagram of this demonstration.

After the configuration code is downloaded into the FPGA successfully, the I2C Sensor Configuration block will initiate the CMOS sensor via I2C interface. The CMOS sensor is configured as:

- Resolution: 800 * 480
- Exposure time: Adjustable
- Pix clock: MCLK*2 = 25*2 = 50MHz
- Readout mode: Binning
- Mirror mode: Line mirrored

According to the settings, the frame rate of the CMOS sensor output is approximately 44.4 **fps**.

After the configuration is complete, the CMOS sensor starts capturing and sending out image data stream. The CMOS Capture block extracts the valid pixel data stream based on the synchronous signals from the CMOS sensor. The data stream is generated in Bayer Color Pattern format. It is converted to RGB data stream within the RAW2RGB block.

The Multi-Port DDR3 SDRAM Controller then acquires the RGB data stream and writes it to the DDR3 SDRAM, which acts as a frame buffer. The Multi-Port DDR3 SDRAM Controller has two write ports and read ports with 128-bit data width each. The writing clock is same as the CMOS sensor pixel clock. The reading clock is provided by the LCD Controller, which is 33MHz.

Finally, the LCD controller fetches the RGB data from the buffer and displays it on the LCD panel continuously. Because the resolution and timing of the LCD is compatible with WVGA@800*480, the LCD controller generates the same timing, and the frame rate can achieve approximately 25 **fps**.

For better visual effect, the CMOS sensor is configured to enable the left right mirror mode. Users can disable this functionality by modifying the value of associated register written to the CMOS controller chip.

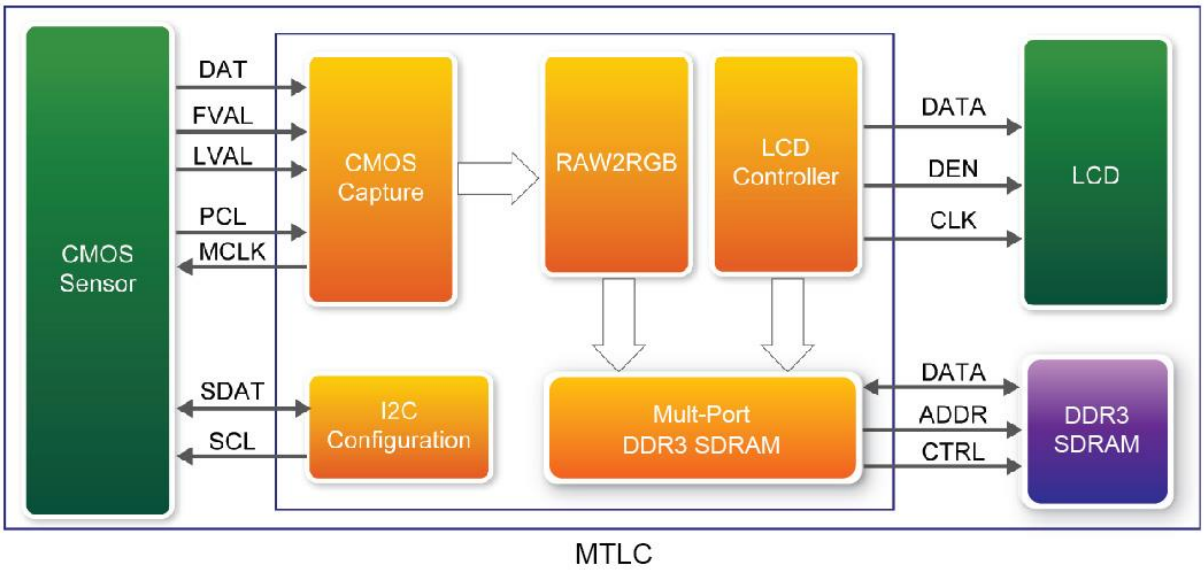

Figure 4-6 Block diagram of the digital camera design

■ Demonstration Source Code

- Project directory: System-CD\Demonstrations\FPGA\SoCKit_Camera
- Bit stream: SoCKit_Camera.sof

■ Demonstration Batch File

Demo batch file directory: System-CD\Demonstrations\FPGA\SoCKit_Camera\demo_batch

The folder includes the following files:

- Batch file: test.bat
- FPGA configuration file: SoCKit_Camera.sof

■ Demonstration Setup

- Configure the FPGA by executing the batch file 'test.bat' from the directory "SoCKit_Camera\demo_batch" (Note*)
- The system enters the FREE RUN mode automatically. Press **KEY0** on the SoCKit board to reset the circuit
- User can use the **SW0** and **KEY1** to set the exposure time for brightness adjustment of the image captured. When **SW0** is set to OFF, the brightness of image will be increased as **KEY1** is pressed. If **SW0** is set to ON, the brightness of image will be decreased as **KEY1** is pressed.
- User can use **SW3** to mirror lines of the image. Please remember to press **KEY0** to reset the circuit after **SW3** is toggled.

Note: execute the test.bat under the folder "SoCKit_Camera\demo_batch" will automatically download the .sof file.

Table 4-1 summarizes the functional keys of the digital camera demonstration and Figure 4-7 gives a photo of the demonstration.

Table 4-1 The Functional Keys of the Digital Camera Demonstration

Component	*Function Description*
KEY0	Reset circuit
KEY1	Set the new exposure time (use with SW0)
KEY2	Stop Run
KEY3	Switch to Free Run mode
SW0	Off: Extend the exposure time
	On: Shorten the exposure time
SW3	Mirror image (use with KEY0)

Figure 4-7 Screen shot of the VEEK-MT-SoCKit camera demonstration

4.4 Digital Accelerometer Demonstration

This demonstration shows a bubble level implementation based on a digital accelerometer. We use I^2C protocol to control the ADXL345 digital accelerometer, and the APDS-9300 Miniature Ambient Light Photo Sensor. The LCD displays the interface of our game. When tilting the VEEK-MT-SoCKit, the ADXL345 measures the static acceleration of gravity. In our Nios II software, we compute the change of angle in the x-axis and y-axis, and show the angle data on the LCD display. The value of light sensor will change as the brightness changes around the light-sensor.

Figure 4-8 shows the hardware system block diagram of this demonstration. The system is clocked by an external 50MHz oscillator. Through the internal PLL module, the generated 100MHz clock is used for Nios II processor and other components. Tere is also a 40MHz clock generated for low-speed peripherals.

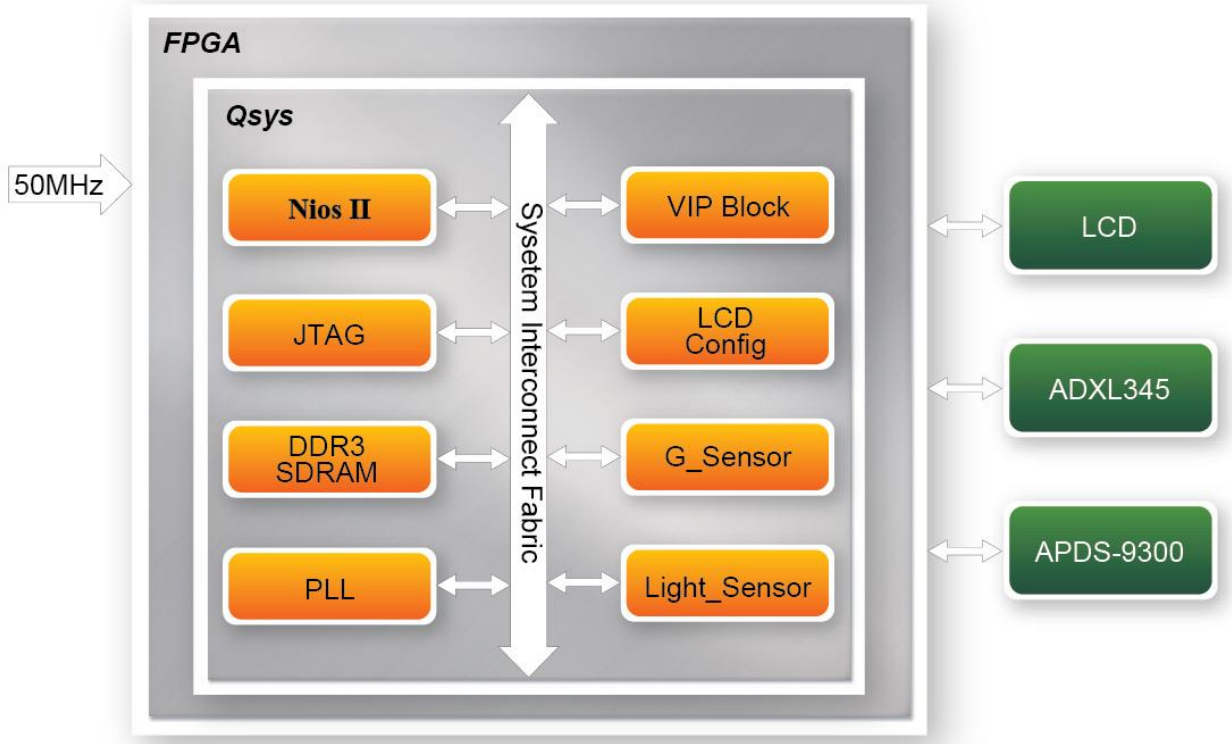

Figure 4-8 Block diagram of the digital accelerometer demonstration

■ Demonstration Source Code

- Project directory: System-CD\Demonstrations\FPGA\SoCKit_G_sensor
- Bit stream used: SoCKit_G_sensor.sof
- Nios II workspace: System-CD\Demonstrations\FPGA\SoCKit_G_sensor\software

■ Demonstration Batch File

Demo batch file directory: System-CD\Demonstrations\FPGA\SoCKit_G_sensor\demo_batch

The folder includes the following files:

- Batch file: G_sensor.bat, test_bashrc
- FPGA configuration file: SoCKit_G_sensor.sof
- Nios II program: G_sensor.elf

■ Demonstration Setup

- Configure the FPGA by executing the demo batch file “test.bat” from the batch file folder “SoCKit_Painter\demo_batch” (Note*)

- After the Nios II program is downloaded and executed successfully, a prompt message will be displayed in nios2-terminal: “its ADXL345’s ID = e5”.
- Tilt the VEEK-MT-SoCKit to all directions, and you will find the angle of G-sensor and the value of light sensor change accordingly. When turning the board from -80º to -10º and from 10º to 80º in Y-axis, or from 10ºto 80º and from -80º to -10º in Y-axis, the image will be inverted. **Figure 4-9** shows the photo when running the demonstration.

Figure 4-9 Digital accelerometer demonstration

Note: execute SoCKit_G_sensor\demo_batch\test.bat to download .sof and .elf files.

4.5 Video and Image Processing for Camera

The Video and Image Processing (VIP) for the Camera Example Design demonstrates dynamic scaling and clipping of a standard definition video stream in RGB format and picture-in-picture mixing with the background layer. The video stream is sent and displayed in high definition resolution (800×480) on the HSMC LTC daughter card (part of the VEEK).

The example design demonstrates a framework for rapid development of video and image processing systems using the parameterizable MegaCore® functions, which are available in the Video and Image Processing Suite. This demonstration needs the Quartus II license file includes the VIP suite feature.

A video source is sent from the CMOS sensor on VEEK, which generates a digital output in RGB format. A number of common video functions are performed on this input stream in the FPGA. These functions include clipping, chroma resampling, motion adaptive deinterlacing, color space conversion, picture-in-picture mixing, and polyphase scaling.

The input and output of video interfaces on the VEEK are configured and initialized by the software running on a Nios® II processor. The Nios II software demonstrates how to control the clocked video input, clocked video output, and mixer functions at run-time is also provided. The video system is implemented using the Qsys system design tool. This abstracted design tool provides an easy path to the system integration of video processing data path with NTSC or PAL video input, VGA output, and Nios II processor for configuration and control purposes. The Video and Image Processing Suite MegaCore functions have common open Avalon-ST data interfaces and Avalon Memory-Mapped (Avalon-MM) control interfaces to facilitate connection of a chain of video functions and video system modeling. In addition, video data is transmitted between the Video and Image Processing Suite functions using the Avalon-ST Video protocol, which facilitates building run-time controllable systems and error recovery.

Figure 4-9 shows the block diagram of Video and Image Processing.

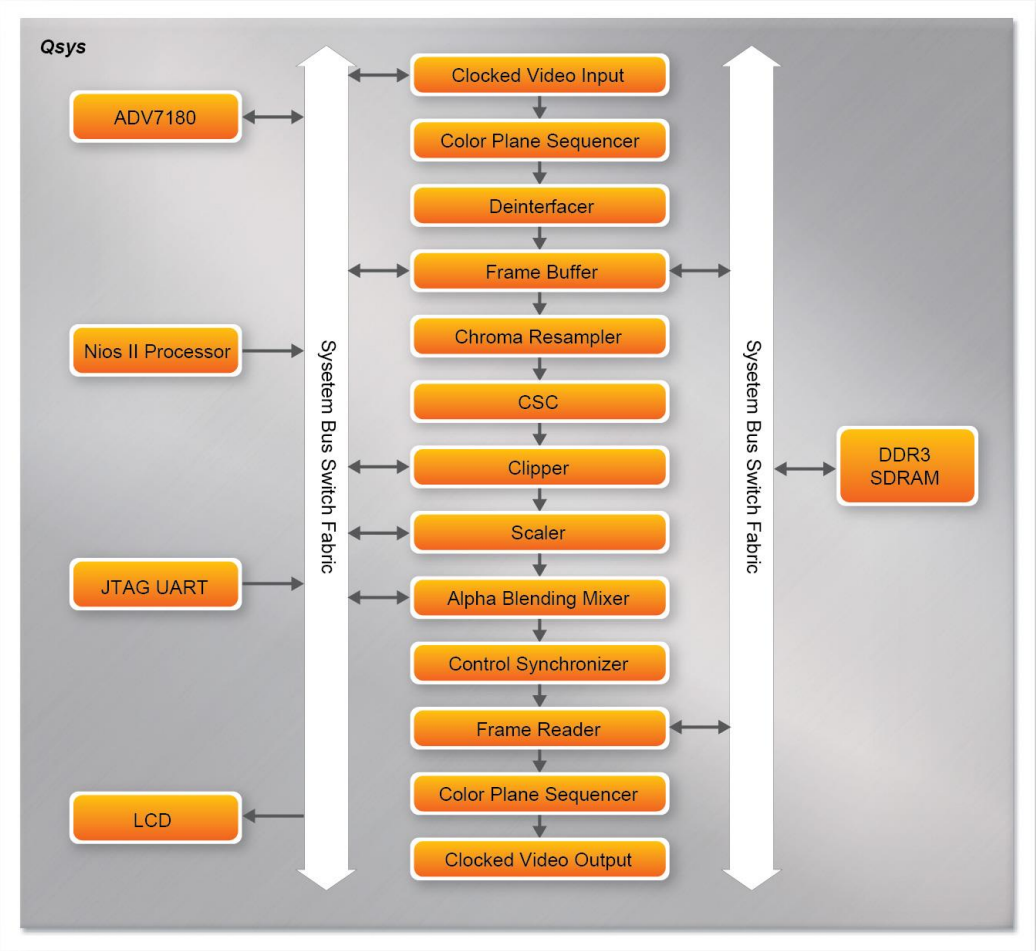

Figure 4-9 Block diagram of VIP camera example in Qsys with key components

■ Demonstration Source Code

- Project directory: System-CD\Demonstrations\FPGA\SoCKit_VIP_Camera
- Bit stream used: SoCKit _VIP_Camera.sof
- Nios II workspace: VEEK_VIP_Camera \software

■ Demonstration Batch File

Demo batch file directory: System-CD\Demonstrations\FPGA\SoCKit_VIP_Camera\demo_batch

The folder includes the following files:

- Batch file: VIP_Camera.bat, VIP_Camera _bashrc
- FPGA configuration file: SoCKit_VIP_Camera.sof
- Nios II program: VIP_Camera.elf

■ Demonstration Setup

- Connect the VGA output of the SoCKit board to a VGA monitor, as shown in **Figure 4-10**.
- (both LCD and CRT type of monitors should work)
- Configure the FPGA by executing the batch file "VIP_Camera.bat" from the folder "System-CD\Demonstrations\FPGA\SoCKit_VIP_Camera\demo_batch". (note *)
- The system enters the FREE RUN mode automatically. Press **KEY0** on the SoCKit board to reset the circuit
- Press **KEY2** to stop run; press **KEY3** again to switch back to FREE RUN mode and you should be able to see whatever the camera captures on the VGA display
- User can use **SW3** to mirror lines of the image. Please remember to press **KEY0** to reset the circuit after **SW3** is toggled.
- In the touch-screen, press and drag the video frame box will result in scaling the playing window to any size, as shown in **Figure 4-11**.

Note:

(1) Execute SoCKit_VIP_Camera\demo_batch\VIP_Camera.bat will download .sof and .elf files.

(2) You may need additional Altera VIP suite Megacore license features to recompile the project.

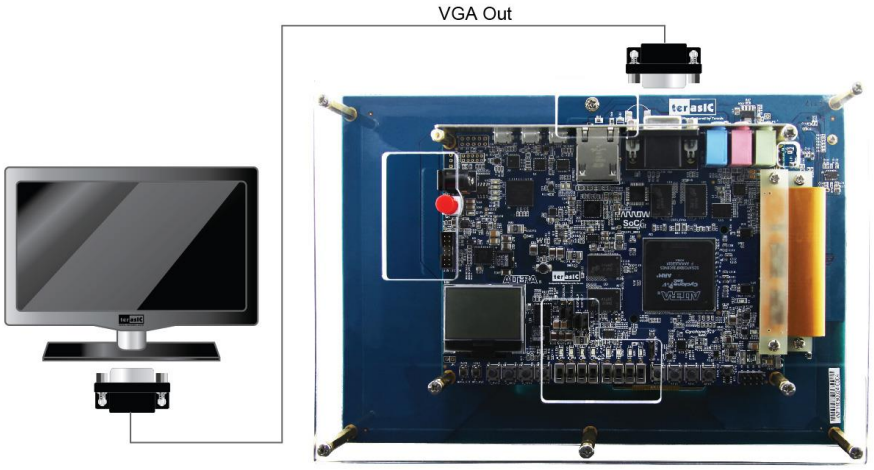

Figure 4-10 Setup for the VEEK VIP camera demonstration

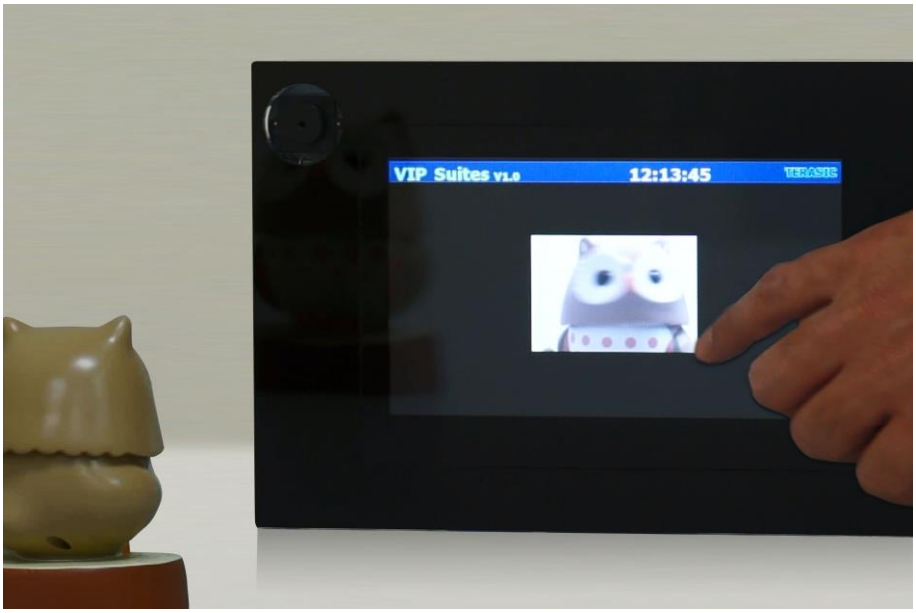

Figure 4-11 Screenshot of the VIP camera demonstration

Chapter 5

Appendix

5.1 Revision History

Version	*Change Log*
V1.0	**Initial Version**

5.2 Copyright Statement

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