24-Bit, Wide Bandwidth Analog-to-Digital Converter

FEATURES

- 105kSPS Data Rate
- AC Performance:
  - 51kHz Bandwidth
  - 109dB SNR (High-Resolution Mode)
  - −108dB THD
- DC Accuracy:
  - 1.8μV/°C Offset Drift
  - 2ppm/°C Gain Drift
- Selectable Operating Modes:
  - High-Speed: 105kSPS Data Rate
  - High-Resolution: 109dB SNR
  - Low-Power: 35mW Dissipation
- Power-Down Control
- Digital Filter:
  - Linear Phase Response
  - Passband Ripple: ±0.005dB
  - Stop Band Attenuation: 100dB
- Internal Offset Calibration On Command
- Selectable SPI™ or Frame Sync Serial Interface
- Designed for Multichannel Systems:
  - Daisy-Chainable Serial Interface
  - Easy Synchronization
- Simple Pin-Driven Control
- Modulator Output Option
- Specified from −40°C to +105°C
- Analog Supply: 5V
- Digital Supply: 1.8V to 3.3V

APPLICATIONS

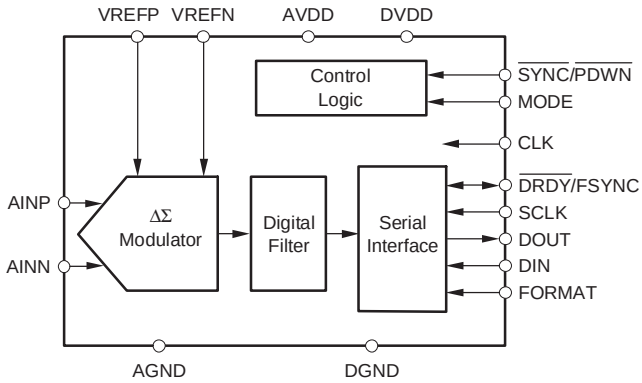
- Vibration/Modal Analysis
- Acoustics
- Dynamic Strain Gauges
- Pressure Sensors
- Test and Measurement

DESCRIPTION

The ADS1271 is a 24-bit, delta-sigma analog-to-digital converter (ADC) with a data rate up to 105kSPS. It offers a unique combination of excellent DC accuracy and outstanding AC performance. The high-order, chopper-stabilized modulator achieves very low drift with low in-band noise. The onboard decimation filter suppresses modulator and signal out-of-band noise. The ADS1271 provides a usable signal bandwidth up to 90% of the Nyquist rate with less than 0.005dB of ripple.

Traditionally, industrial delta-sigma ADCs offering good drift performance use digital filters with large passband droop. As a result, they have limited signal bandwidth and are mostly suited for DC measurements. High-resolution ADCs in audio applications offer larger usable bandwidths, but the offset and drift specification are significantly weaker than their industrial counterparts. The ADS1271 combines these converters, allowing high-precision industrial measurement with excellent DC and AC specifications ensured over an extended industrial temperature range.

Three operating modes allow for optimization of speed, resolution, and power. A selectable SPI or a frame-sync serial interface provides for convenient interfacing to microcontrollers or DSPs. The output from the modulator is accessible for external digital filter applications. All operations, including internal offset calibration, are controlled directly by pins; there are no registers to program.



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	ADS1271	UNIT
AVDD to AGND	−0.3 to +6.0	V
DVDD to DGND	−0.3 to +3.6	V
AGND to DGND	−0.3 to +0.3	V
Input Current	100, Momentary	mA
	10, Continuous	mA
Analog Input to AGND	−0.3 to AVDD + 0.3	V
Digital Input or Output to DGND	−0.3 to DVDD + 0.3	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	−40 to +105	°C
Storage Temperature Range	−60 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = −40°C to +105°C, AVDD = +5V, DVDD = +1.8V, f_{CLK} = 27MHz, VREFP = 2.5V, and VREFN = 0V, unless otherwise noted.

Specified values for ADS1271 and ADS1271B (high-grade version) are the same, except where shown in **BOLDFACE** type.

PARAMETER		TEST CONDITIONS	ADS1271			ADS1271B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Analog Inputs									
Full-scale input voltage (FSR(1))		V_{IN} = (AINP – AINN)		±V_{REF}			±V_{REF}		V
Absolute input voltage		AINP or AINN to AGND	AGND – 0.1		AVDD + 0.1	AGND – 0.1		AVDD + 0.1	V
Common-mode input voltage		V_{CM} = (AINP + AINN)/2		2.5			2.5		V
Differential input impedance	High-Speed mode			16.4			16.4		kΩ
	High-Resolution mode			16.4			16.4		kΩ
	Low-Power mode			32.8			32.8		kΩ
DC Performance									
Resolution		No missing codes	24			24			Bits
Data rate (f_{DATA})	High-Speed mode			105,469			105,469		SPS
	High-Resolution mode			52,734			52,734		SPS
	Low-Power mode			52,734			52,734		SPS
Integral nonlinearity (INL)		Differential input, V_{CM} = 2.5V		± 0.0006	± 0.0015		± 0.0006	± 0.0015	%FSR(1)
Offset error	High-Speed mode	Without calibration		0.150	1		0.150	1	mV
		With calibration	On the level of the noise						
Offset drift				1.8			1.8		µV/°C
Gain error				0.1	0.5		0.1	0.5	%FSR(1)
Gain error drift				2			2		ppm/°C
Noise	High-Speed mode	Shorted input		9.0	20		9.0	**16**	µV, rms
	High-Resolution mode			6.5			6.5	**12**	µV, rms
	Low-Power mode			9.0			9.0	**16**	µV, rms
Common-mode rejection		f_{CM} = 60Hz	90	100		**95**	**110**		dB
Power-supply rejection	AVDD	f = 60Hz		80			80		dB
	DVDD			80			80		dB
AC Performance									
Signal-to-noise ratio (SNR) (2) (unweighted)	High-Speed mode		99	106		**101**	106		dB
	High-Resolution mode			109		**103**	109		dB
	Low-Power mode			106		**101**	106		dB
Total harmonic distortion (THD)(3)		V_{IN} = 1kHz, −0.5dBFS		−105	−95		**−108**	**−100**	dB
Spurious-free dynamic range				−108			**−109**		dB
Passband ripple					±0.005			±0.005	dB
Passband				0.453 f_{DATA}			0.453 f_{DATA}		Hz
−3dB Bandwidth				0.49 f_{DATA}			0.49 f_{DATA}		Hz
Stop band attenuation			100			100			dB
Stop band	High-Speed mode		0.547 f_{DATA}		63.453 f_{DATA}	0.547 f_{DATA}		63.453 f_{DATA}	Hz
	High-Resolution mode		0.547 f_{DATA}		127.453 f_{DATA}	0.547 f_{DATA}		127.453 f_{DATA}	Hz
	Low-Power mode		0.547 f_{DATA}		63.453 f_{DATA}	0.547 f_{DATA}		63.453 f_{DATA}	Hz
Group delay	High-Speed and Low-Power modes			38/f_{DATA}			38/f_{DATA}		s
	High-Resolution mode			39/f_{DATA}			39/f_{DATA}		s
Settling time (latency)	High-Speed and Low-Power modes	Complete settling		76/f_{DATA}			76/f_{DATA}		s
	High-Resolution mode	Complete settling		78/f_{DATA}			78/f_{DATA}		s

(1) FSR = full-scale range = $2V_{REF}$.
(2) Minimum SNR is ensured by the limit of the *DC noise* specification.
(3) THD includes the first nine harmonics of the input signal.
(4) MODE and FORMAT pins excluded.
(5) See the text for more details on SCLK.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = −40°C to +105°C, AVDD = +5V, DVDD = +1.8V, f_{CLK} = 27MHz, VREFP = 2.5V, and VREFN = 0V, unless otherwise noted.

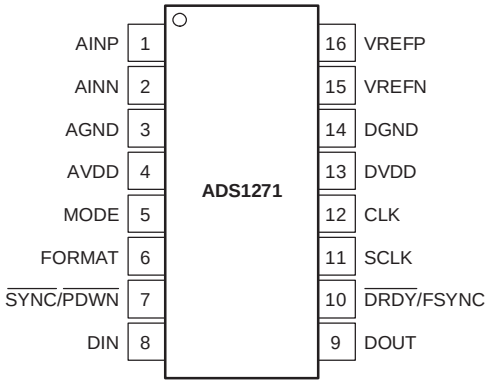
Specified values for ADS1271 and ADS1271B (high-grade version) are the same, except where shown in **BOLDFACE** type.

PARAMETER		TEST CONDITIONS	ADS1271			ADS1271B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Reference Inputs									
Reference input voltage (V_{REF})		V_{REF} = VREFP – VREFN	2.0	2.5	2.65	**0.5**	2.5	2.65	V
Negative reference input (VREFN)			AGND − 0.1		VREFP − 2.0	AGND − 0.1		**VREFP − 0.5**	V
Positive reference input (VREFP)			VREFN + 2.0		AVDD − 0.5	**VREFN + 0.5**		**AVDD + 0.1**	V
Reference Input impedance	High-Speed mode			4.2			4.2		kΩ
	High-Resolution mode			4.2			4.2		kΩ
	Low-Power mode			8.4			8.4		kΩ
Digital Input/Output									
V_{IH}			0.7 DVDD		DVDD	0.7 DVDD		DVDD	V
V_{IL}			DGND		0.3 DVDD	DGND		0.3 DVDD	V
V_{OH}		I_{OH} = 5mA	0.8 DVDD		DVDD	0.8 DVDD		DVDD	V
V_{OL}		I_{OL} = 5mA	DGND		0.2 DVDD	DGND		0.2 DVDD	V
Input leakage(4)		0 < $V_{IN\ DIGITAL}$ < DVDD			±10			±10	µA
Master clock rate (f_{CLK})			0.1		27	0.1		27	MHz
Serial clock rate (f_{SCLK})(5)	SPI format		24 f_{DATA}		f_{CLK}	24 f_{DATA}		f_{CLK}	MHz
	Frame-Sync format	High-Speed mode	64 f_{DATA}		64 f_{DATA}	64 f_{DATA}		64 f_{DATA}	MHz
		High-Resolution mode	128 f_{DATA}		128 f_{DATA}	128 f_{DATA}		128 f_{DATA}	MHz
		Low-Power mode	64 f_{DATA}		64 f_{DATA}	64 f_{DATA}		64 f_{DATA}	MHz
Power Supply									
AVDD			4.75	5	5.25	4.75	5	5.25	V
DVDD			1.65		3.6	1.65		3.6	V
AVDD current	High-Speed mode			17	25		17	25	mA
	High-Resolution mode			17	25		17	25	mA
	Low-Power mode			6.3	9.5		6.3	9.5	mA
	Power-Down mode	T > 85°C		1	70		1	70	µA
		T ≤ 85°C		1	10		1	10	µA
DVDD current	High-Speed mode			3.5	6		3.5	6	mA
	High-Resolution mode			2.5	5		2.5	5	mA
	Low-Power mode			1.8	3.5		1.8	3.5	mA
	Power-Down mode	T > 85°C, DVDD = 3.3V		1	70		1	70	µA
		T ≤ 85°C, DVDD = 3.3V		1	20		1	20	µA
Power dissipation	High-Speed mode			92	136		92	136	mW
	High-Resolution mode			90	134		90	134	mW
	Low-Power mode			35	54		35	54	mW
Temperature Range									
Specified			−40		+105	−40		+105	°C
Operating			−40		+105	−40		+105	°C
Storage			−60		+150	−60		+150	°C

(1) FSR = full-scale range = $2V_{REF}$.
(2) Minimum SNR is ensured by the limit of the *DC noise* specification.
(3) THD includes the first nine harmonics of the input signal.
(4) MODE and FORMAT pins excluded.
(5) See the text for more details on SCLK.

PIN ASSIGNMENTS

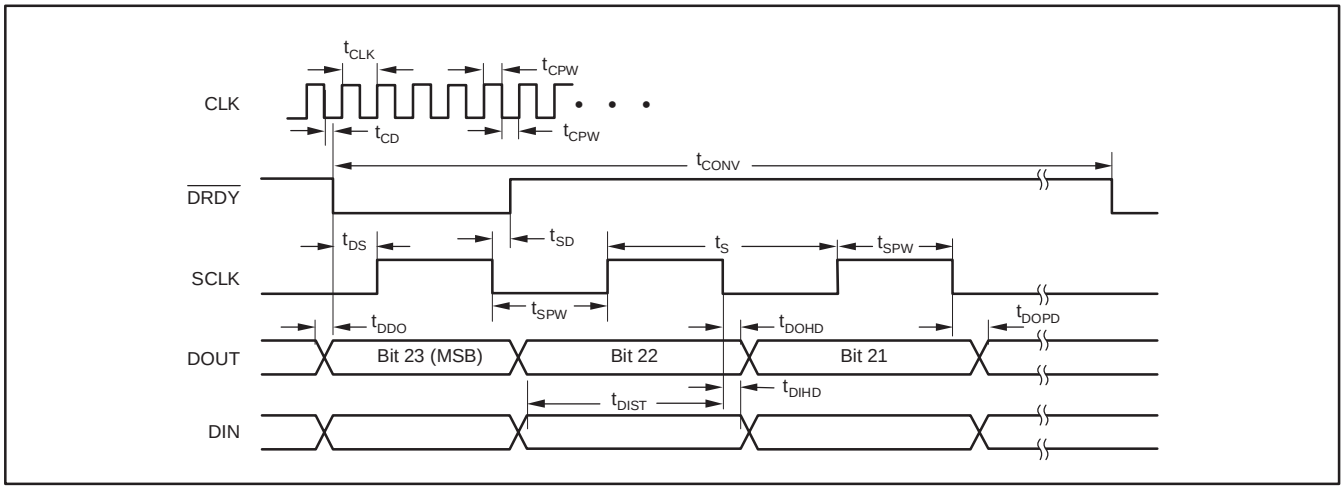
PW PACKAGE
TSSOP-16
(TOP VIEW)



Terminal Functions

PIN NAME	PIN NO.	FUNCTION	DESCRIPTION
AINP	1	Analog Input	Positive analog input
AINN	2	Analog Input	Negative analog input
AGND	3	Analog Input	Analog ground
AVDD	4	Analog Input	Analog supply
MODE	5	Digital Input	MODE = 0: High-Speed mode MODE = float: High-Resolution mode MODE = 1: Low-Power mode
FORMAT	6	Digital Input	FORMAT = 0: SPI FORMAT = float: Modulator output (ADS1271B only) FORMAT = 1: Frame-Sync
$\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$	7	Digital Input	Synchronize/Power-down input, active low
DIN	8	Digital Input	Data input for daisy-chain operation
DOUT	9	Digital Output	ADC data output, modulator output (modulator mode)
$\overline{\text{DRDY}}$/FSYNC	10	Digital Input/Output	If FORMAT = 0 (SPI), then pin 10 = $\overline{\text{DRDY}}$ output If FORMAT = 1 (Frame-Sync), then pin 10 = FSYNC input
SCLK	11	Digital Input	Serial clock for ADC data retrieval, modulator clock output (modulator mode)
CLK	12	Digital Input	Master clock
DVDD	13	Digital Input	Digital supply
DGND	14	Digital Input	Digital ground
VREFN	15	Analog Input	Negative reference input
VREFP	16	Analog Input	Positive reference input

TIMING CHARACTERISTICS: SPI FORMAT



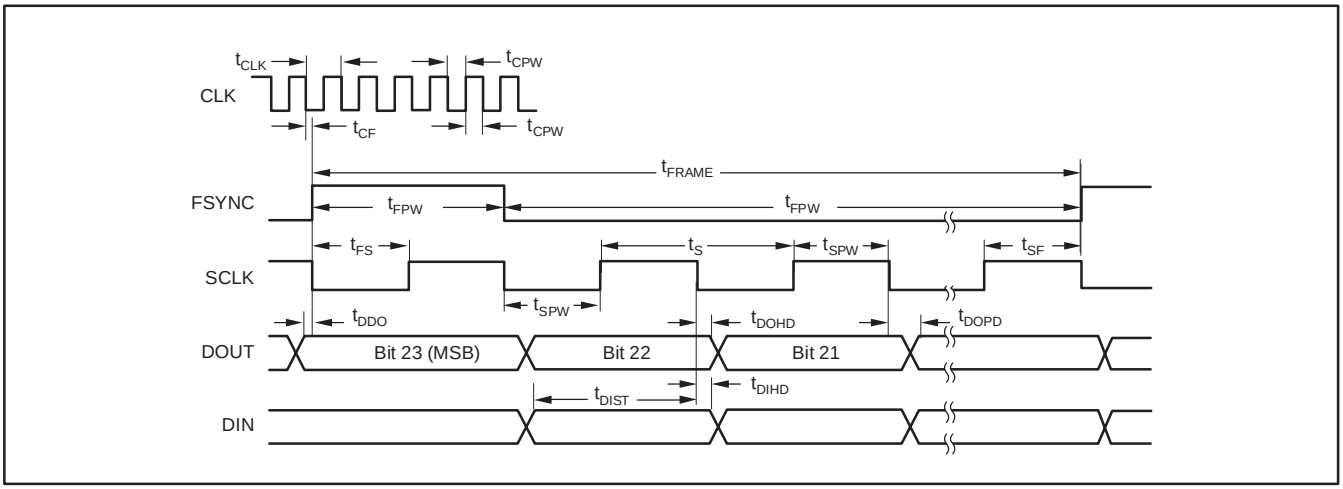
TIMING REQUIREMENTS: SPI FORMAT

For T_A = −40°C to +105°C and DVDD = 1.65V to 3.6V.

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$)		37		10,000	ns
t_{CPW}	CLK positive or negative pulse width		15			ns
t_{CONV}	Conversion period ($1/f_{DATA}$)	High-Speed mode		256		CLK periods
		High-Resolution mode		512		CLK periods
		Low-Power mode		512		CLK periods
t_{CD}(1)	Falling edge of CLK to falling edge of $\overline{DRDY}$			8		ns
t_{DS}(1)	Falling edge of $\overline{DRDY}$ to rising edge of first SCLK to retrieve data		5			ns
t_{DDO}(1)	Valid DOUT to falling edge of $\overline{DRDY}$		0			ns
t_{SD}(1)	Falling edge of SCLK to rising edge of $\overline{DRDY}$			8		ns
t_S(2)	SCLK period		t_{CLK}			ns
t_{SPW}	SCLK positive or negative pulse width		12			ns
t_{DOHD}(1)(3)	SCLK falling edge to old DOUT invalid (hold time)		5			ns
t_{DOPD}(1)	SCLK falling edge to new DOUT valid (propagation delay)				12	ns
t_{DIST}	New DIN valid to falling edge of SCLK (setup time)		6			ns
t_{DIHD}(3)	Old DIN valid to falling edge of SCLK (hold time)		6			ns

(1) Load on $\overline{DRDY}$ and DOUT = 20pF.
(2) For best performance, limit f_{SCLK}/f_{CLK} to ratios of 1, 1/2, 1/4, 1/8, etc.
(3) t_{DOHD} (DOUT hold time) and t_{DIHD} (DIN Hold time) are specified under opposite worst case conditions (digital supply voltage and ambient temperature). Under equal conditions, with DOUT connected directly to DIN, the timing margin is 4nS.

TIMING CHARACTERISTICS: FRAME-SYNC FORMAT



TIMING REQUIREMENTS: FRAME-SYNC FORMAT

for T_A = −40°C to +105°C and DVDD = 1.65V to 3.6V.

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$)		37		10,000	ns
t_{CPW}	CLK positive or negative pulse width		15			ns
t_{CF}	Falling edge of CLK to falling edge of SCLK		−0.35 t_{CLK}		0.35 t_{CLK}	ns
t_{FRAME}	Frame period ($1/f_{DATA}$)	High-Speed mode		256		CLK periods
		High-Resolution mode		256 or 512(1)		CLK periods
		Low-Power mode		256 or 512(1)		CLK periods
t_{FPW}	FSYNC positive or negative pulse width		1			SCLK periods
t_{FS}	Rising edge of FSYNC to rising edge of SCLK		5			ns
t_{SF}	Rising edge of SCLK to rising edge of FSYNC		5			ns
t_S	SCLK period (SCLK must be continuously running)	High-Speed mode		$\tau_{FRAME}/64$		τ_{FRAME} periods
		High-Resolution mode		$\tau_{FRAME}/128$		τ_{FRAME} periods
		Low-Power mode		$\tau_{FRAME}/64$		τ_{FRAME} periods
t_{SPW}	SCLK positive or negative pulse width		0.4t_{SCLK}		0.6t_{SCLK}	ns
t_{DOHD}(2)(3)	SCLK falling edge to old DOUT invalid (hold time)		5			ns
t_{DOPD}(2)	SCLK falling edge to new DOUT valid (propagation delay)				12	ns
t_{DDO}(2)	Valid DOUT to rising edge of FSYNC		0			ns
t_{DIST}	New DIN valid to falling edge of SCLK (setup time)		6			ns
t_{DIHD}(3)	Old DIN valid to falling edge of SCLK (hold time)		6			ns

(1) The ADS1271 automatically detects either frame period (only 256 or 512 allowed).
(2) Load on DOUT = 20pF.
(3) t_{DOHD} (DOUT hold time) and t_{DIHD} (DIN Hold time) are specified under opposite worst case conditions (digital supply voltage and ambient temperature). Under equal conditions, with DOUT connected directly to DIN, the timing margin is 4nS.

TYPICAL CHARACTERISTICS

T_A = 25°C, AVDD = 5V, DVDD = 1.8V, f_{CLK} = 27MHz, VREFP = 2.5V, VREFN = 0V, unless otherwise noted.

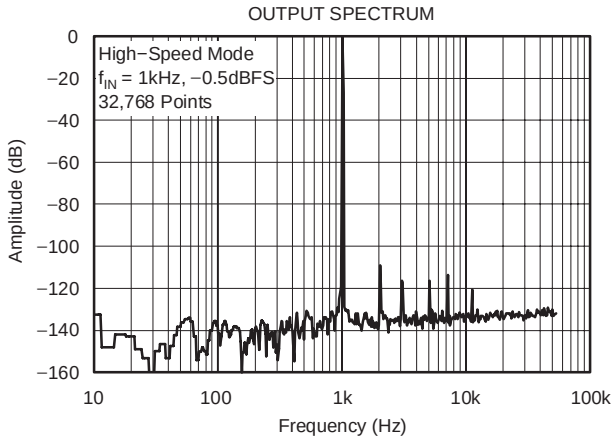


Figure 1

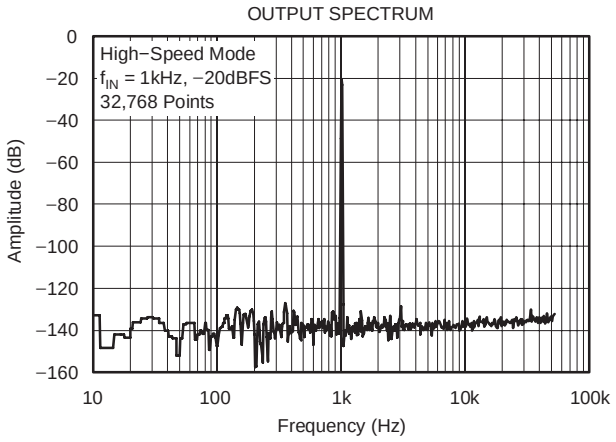


Figure 2

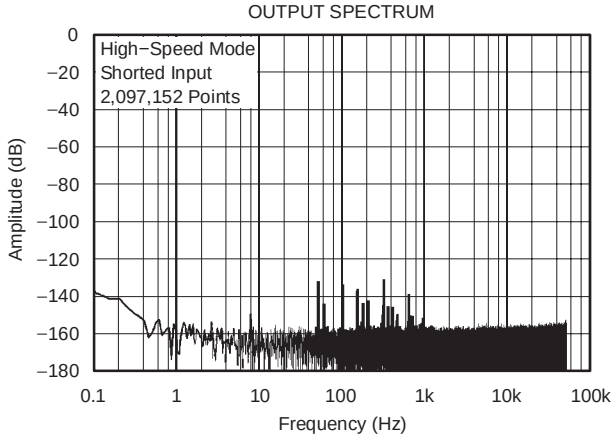


Figure 3

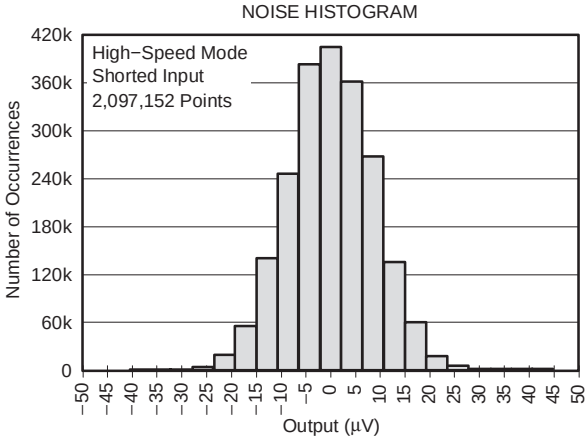


Figure 4

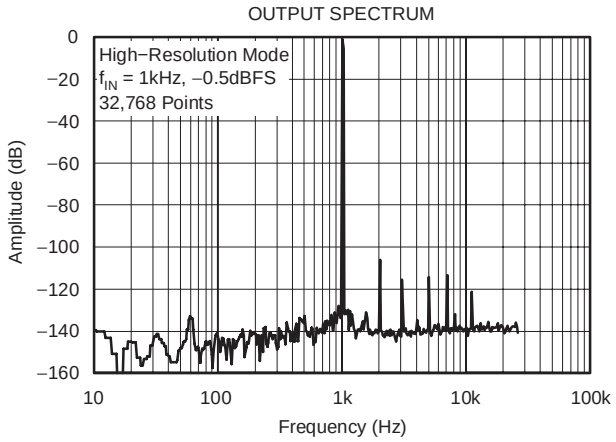


Figure 5

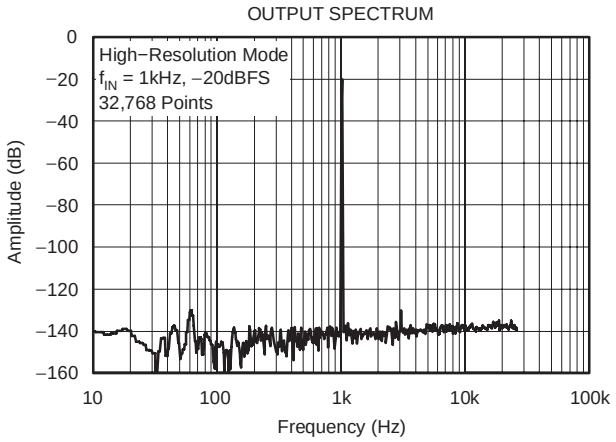


Figure 6

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, AVDD = 5V, DVDD = 1.8V, f_{CLK} = 27MHz, VREFP = 2.5V, VREFN = 0V, unless otherwise noted.

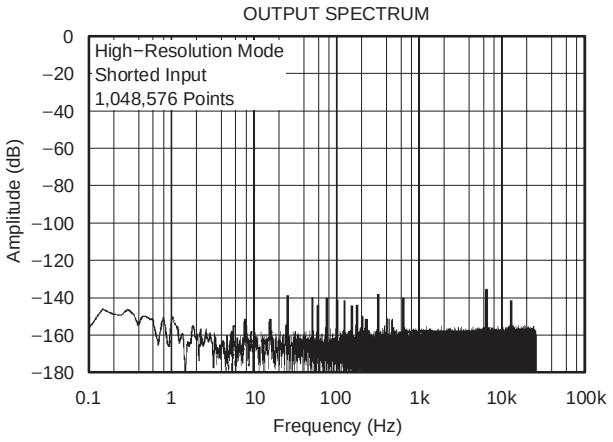


Figure 7

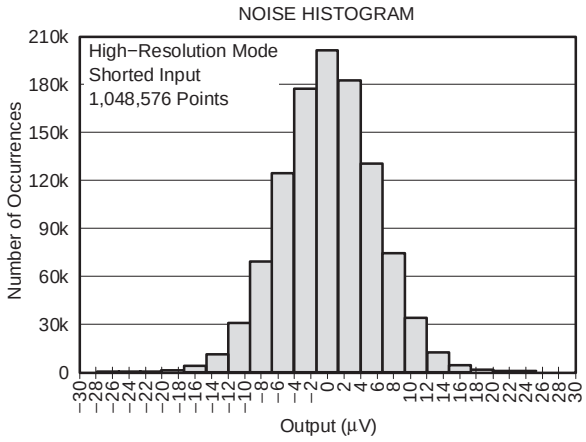


Figure 8

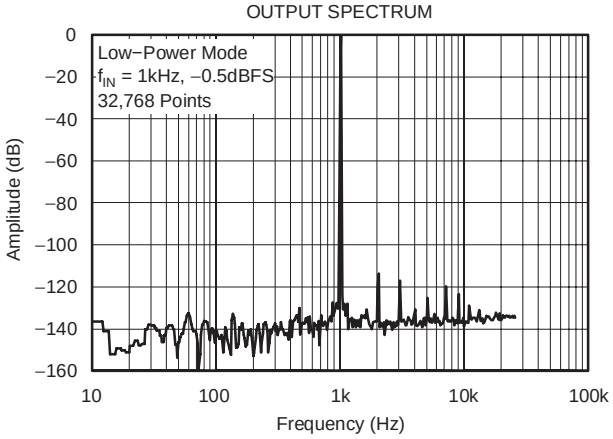


Figure 9

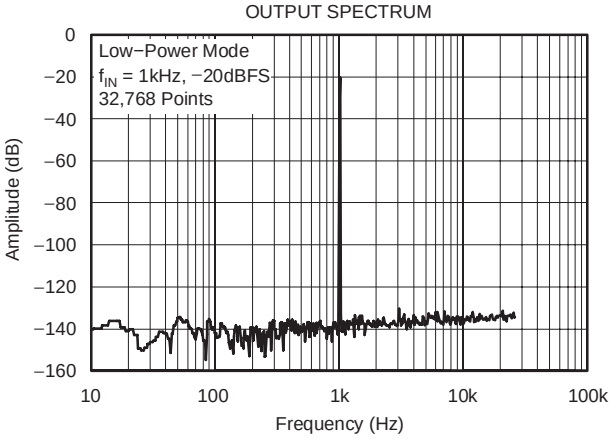


Figure 10

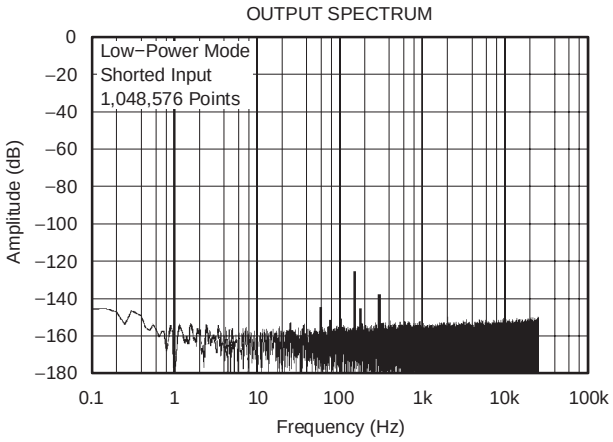


Figure 11

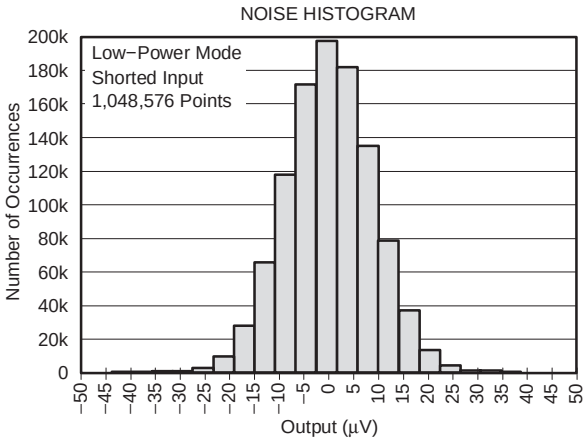


Figure 12

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, AVDD = 5V, DVDD = 1.8V, f_{CLK} = 27MHz, VREFP = 2.5V, VREFN = 0V, unless otherwise noted.

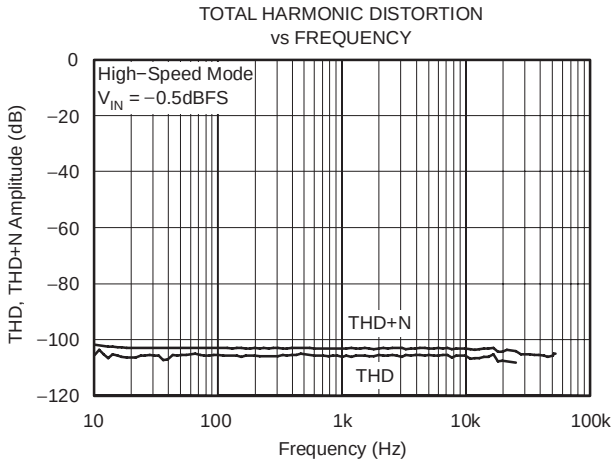


Figure 13

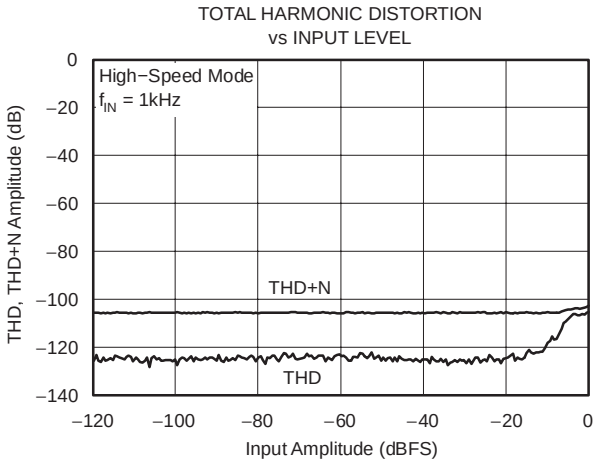


Figure 14

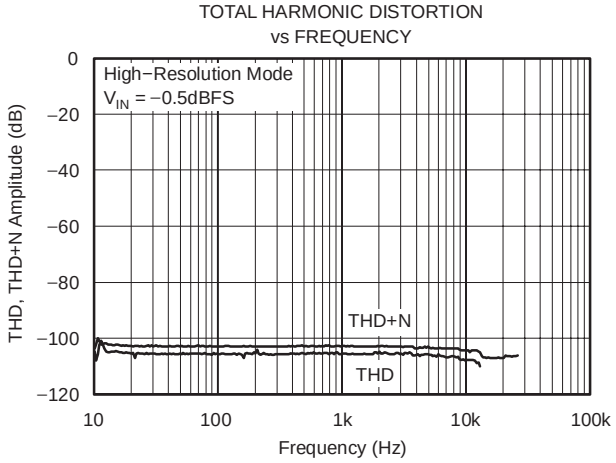


Figure 15

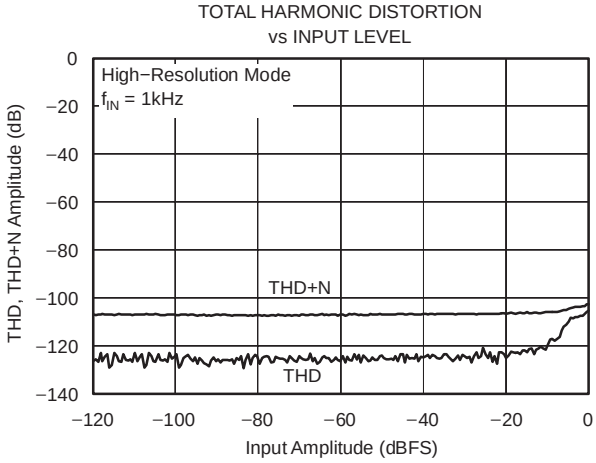


Figure 16

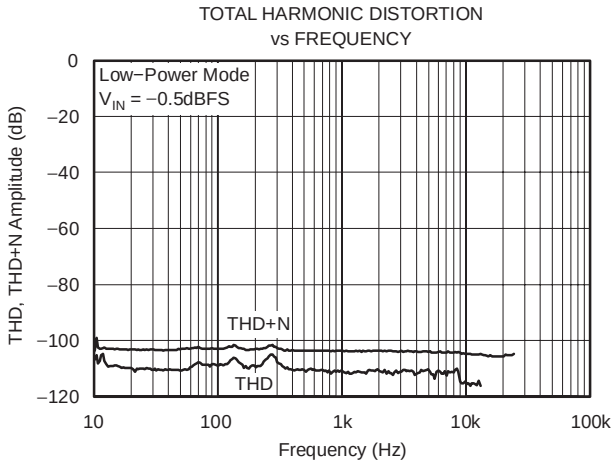


Figure 17

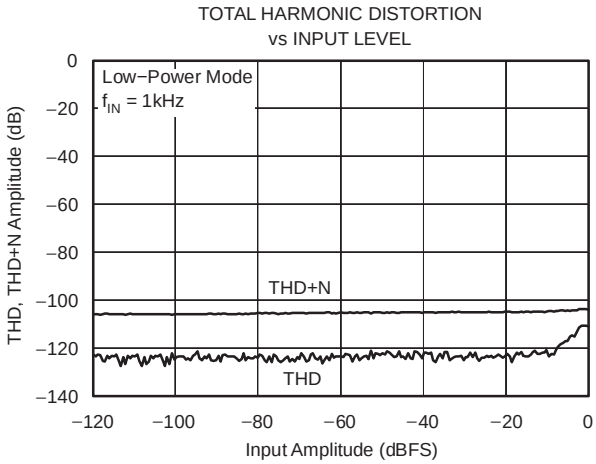


Figure 18

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, AVDD = 5V, DVDD = 1.8V, f_{CLK} = 27MHz, VREFP = 2.5V, VREFN = 0V, unless otherwise noted.

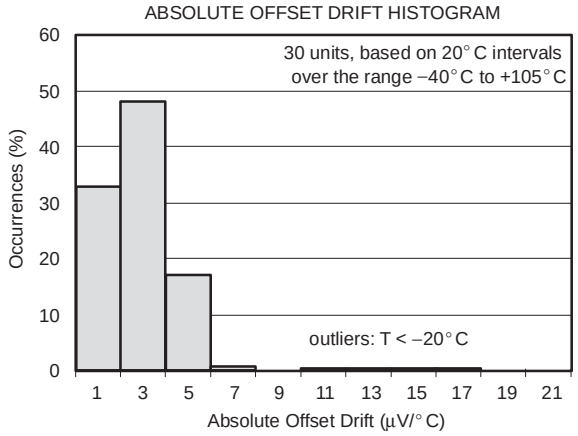


Figure 19

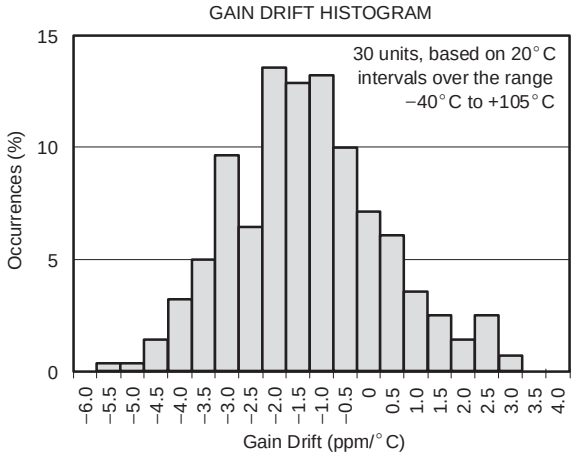


Figure 20

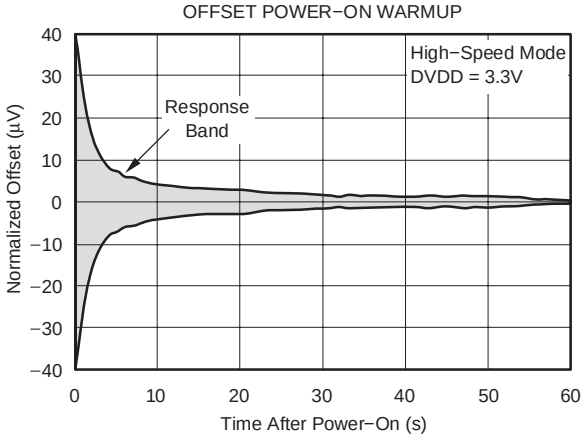


Figure 21

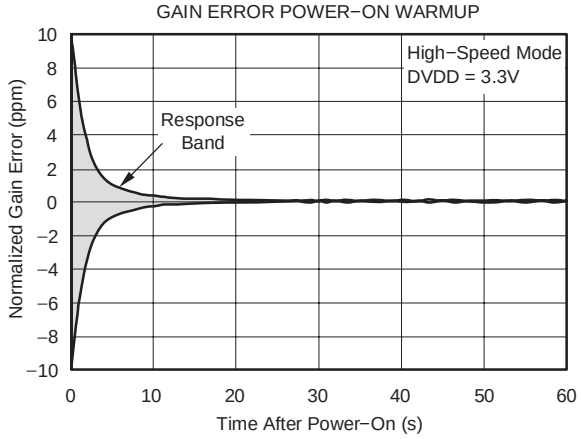


Figure 22

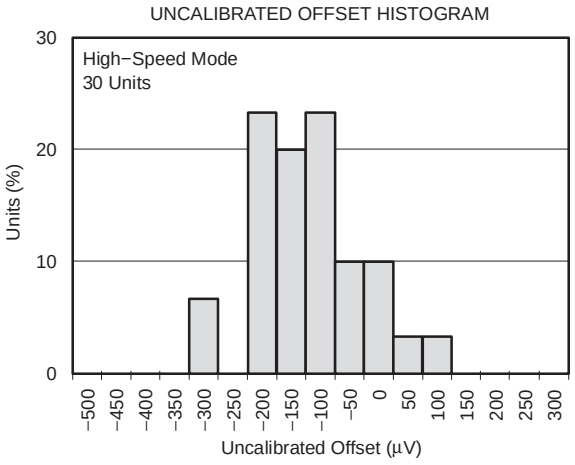


Figure 23

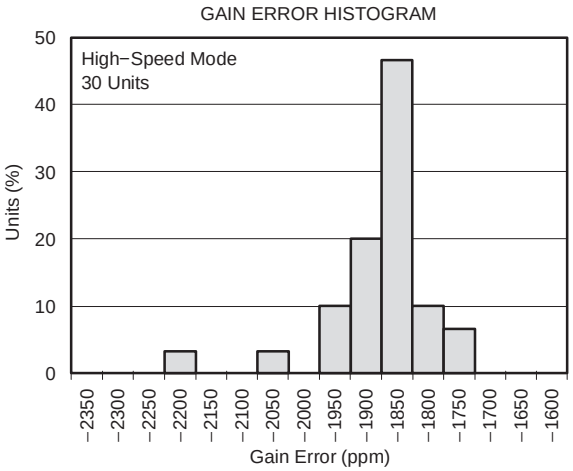


Figure 24

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, AVDD = 5V, DVDD = 1.8V, f_{CLK} = 27MHz, VREFP = 2.5V, VREFN = 0V, unless otherwise noted.

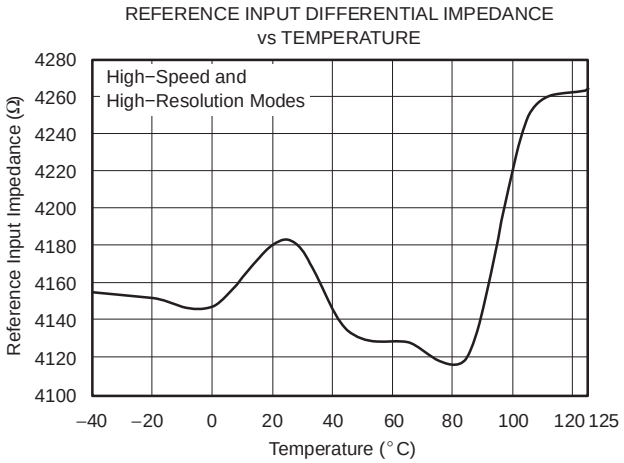


Figure 25

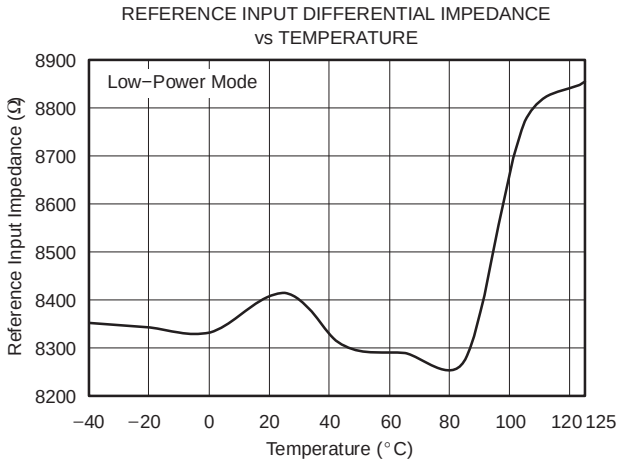


Figure 26

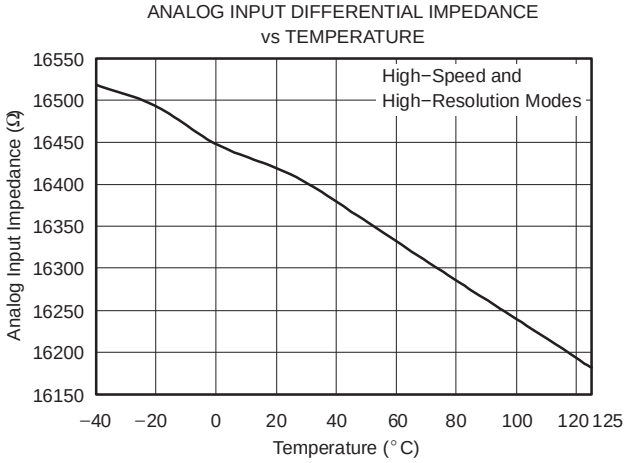


Figure 27

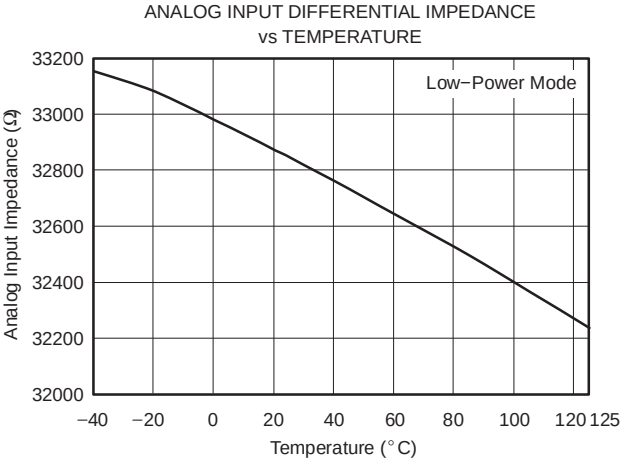


Figure 28

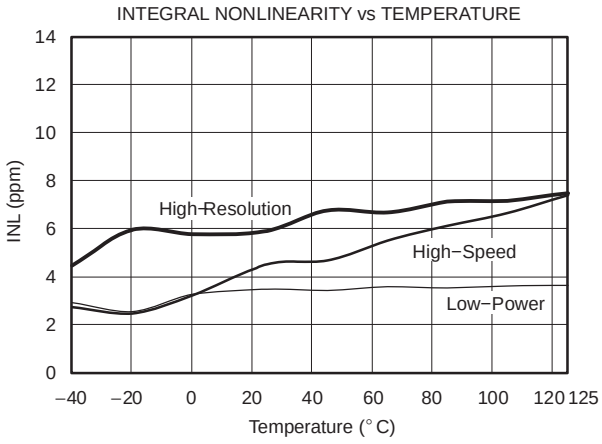


Figure 29

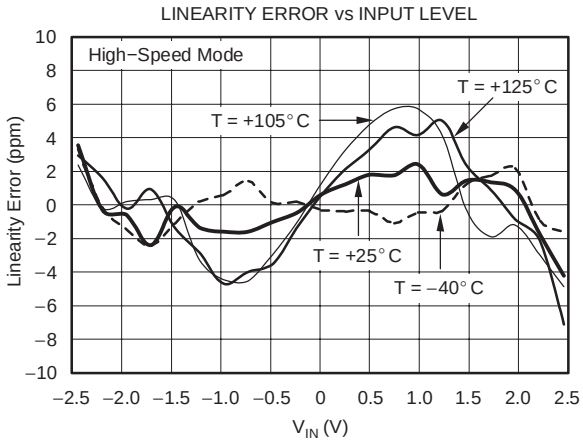


Figure 30

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, AVDD = 5V, DVDD = 1.8V, f_{CLK} = 27MHz, VREFP = 2.5V, VREFN = 0V, unless otherwise noted.

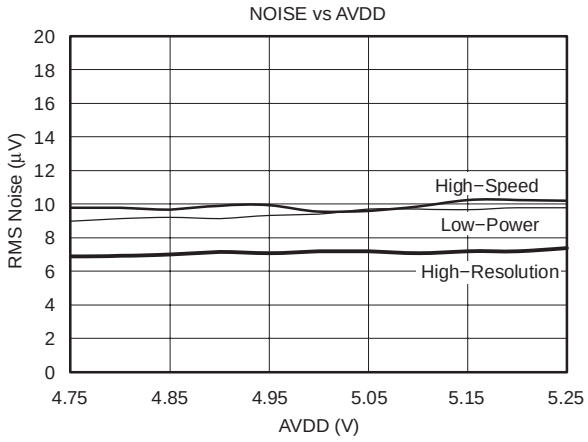


Figure 31

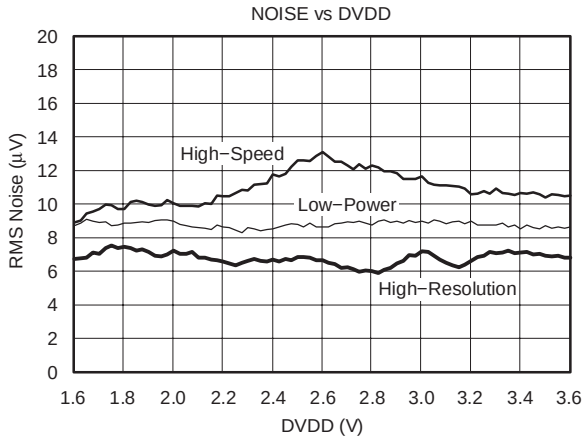


Figure 32

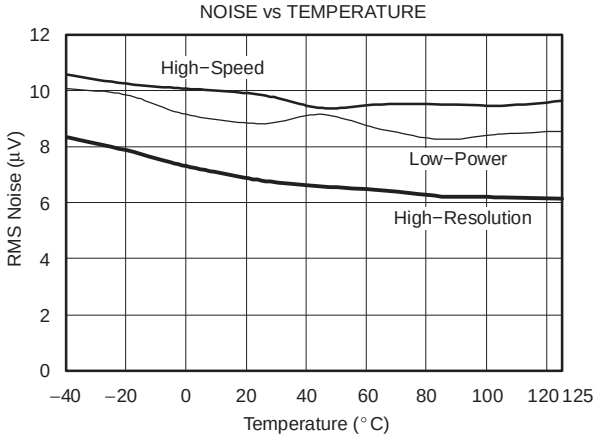


Figure 33

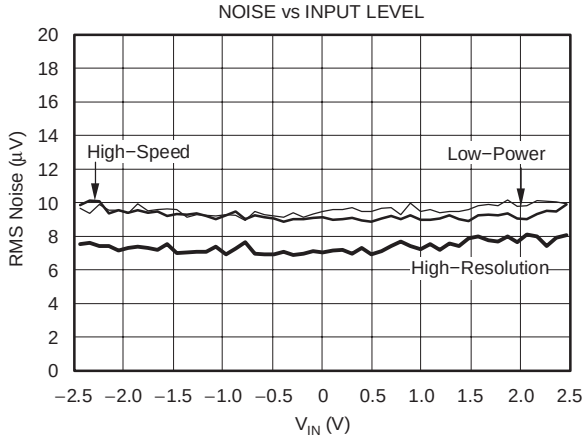


Figure 34

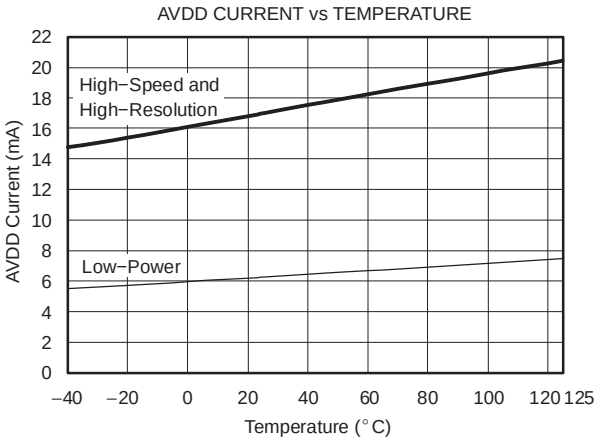


Figure 35

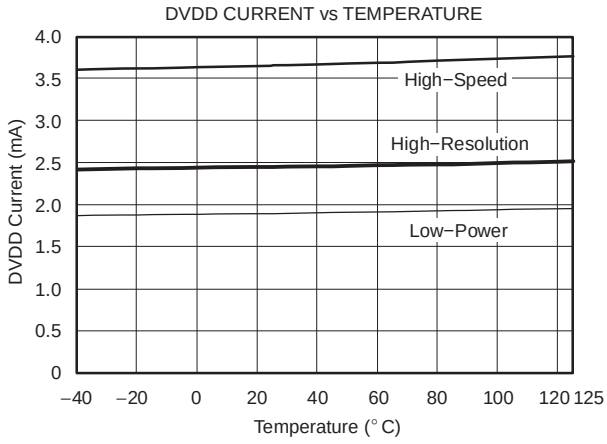


Figure 36

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, AVDD = 5V, DVDD = 1.8V, f_{CLK} = 27MHz, VREFP = 2.5V, VREFN = 0V, unless otherwise noted.

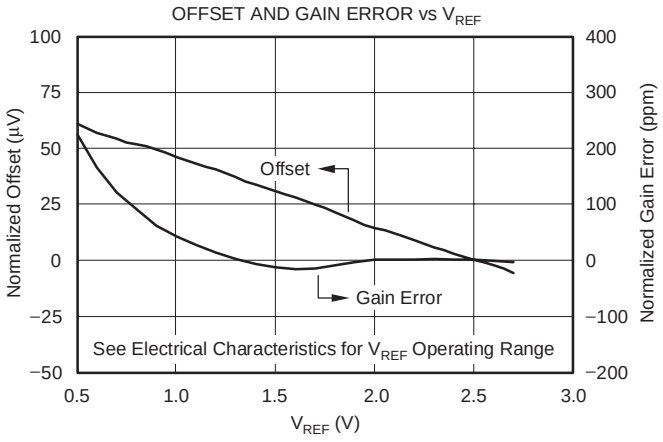


Figure 37

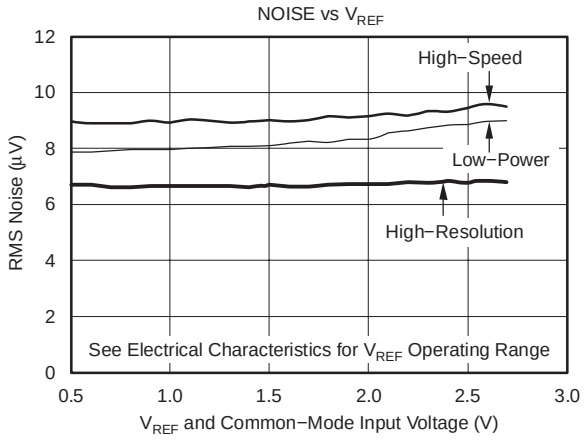


Figure 38

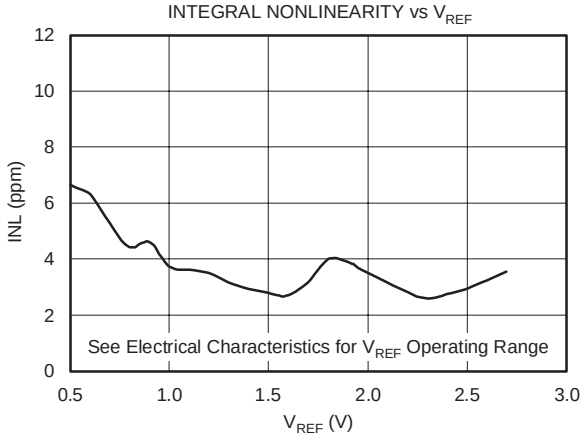


Figure 39

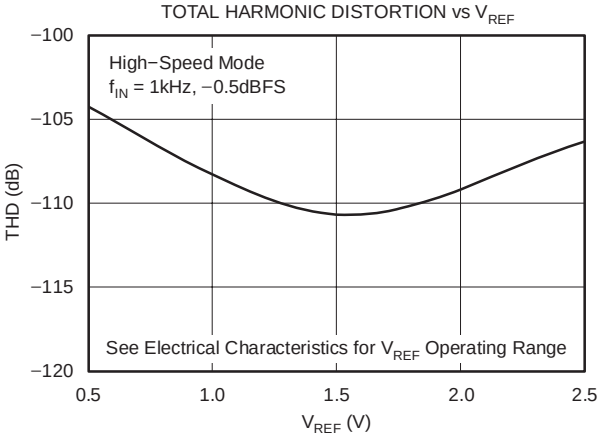


Figure 40

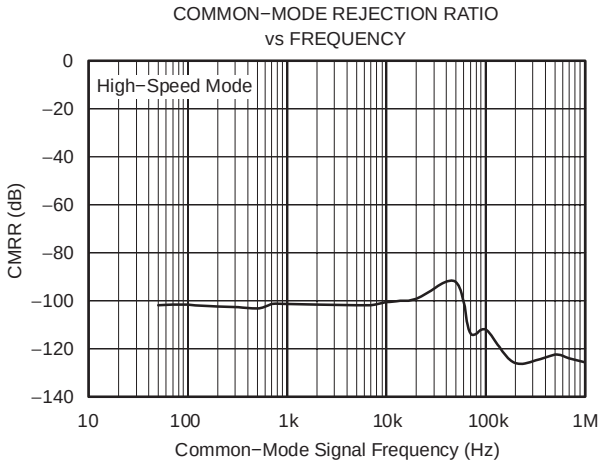


Figure 41

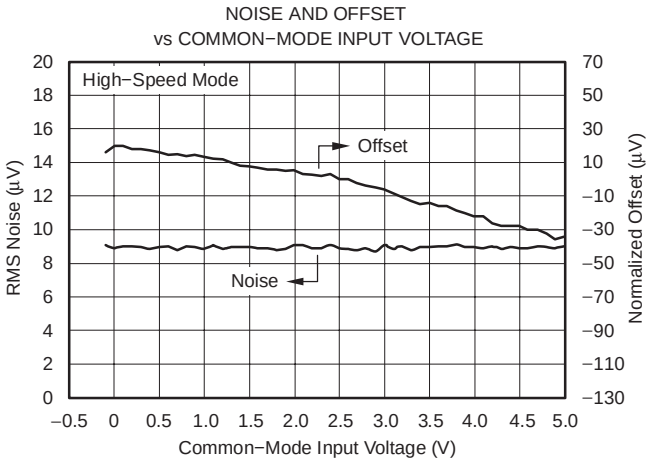


Figure 42

OVERVIEW

The ADS1271 is a 24-bit, delta-sigma ADC. It offers the combination of outstanding DC accuracy and superior AC performance. Figure 43 shows the block diagram for the ADS1271. The ADS1271 converter is comprised of an advanced, 6th-order, chopper-stabilized, delta-sigma modulator followed by a low-ripple, linear phase FIR filter. The modulator measures the differential input signal, V_{IN} = (AINP – AINN), against the differential reference, V_{REF} = (VREFP – VREFN). The digital filter receives the modulator signal and provides a low-noise digital output. To allow tradeoffs among speed, resolution, and power, three modes of operation are supported on the ADS1271: High-Speed, High-Resolution, and Low-Power. Table 1 summarizes the performance of each mode. In High-Speed mode, the data rate is 105kSPS; in High-Resolution mode, the SNR = 109dB; and in Low-Power mode, the power dissipation is only 35mW. The digital filter can be bypassed, enabling direct access to the modulator output.

The ADS1271 is configured by simply setting the appropriate IO pins—there are no registers to program. Data is retrieved over a serial interface that supports both SPI and Frame-Sync formats. The ADS1271 has a daisy-chainable output and the ability to synchronize externally, so it can be used conveniently in multichannel systems.

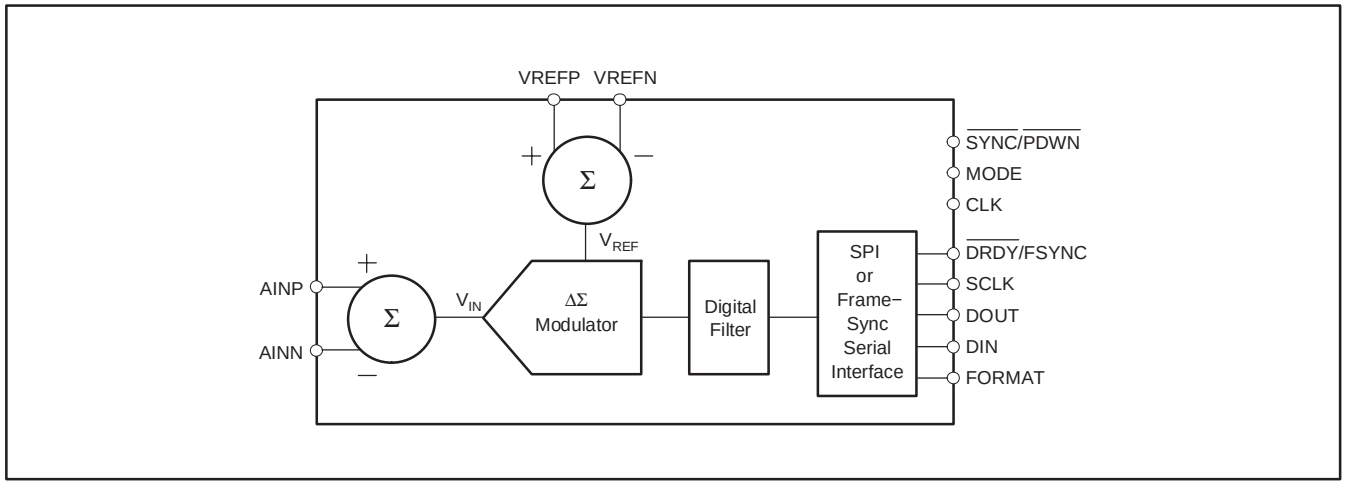


Figure 43. Block Diagram

Table 1. Operating Mode Performance Summary

MODE	DATA RATE (SPS)	PASSBAND (Hz)	SNR (dB)	NOISE (μV_{RMS})	POWER (mW)
High-Speed	105,469	47,777	106	9.0	92
High-Resolution	52,734	23,889	109	6.5	90
Low-Power	52,734	23,889	106	9.0	35

ANALOG INPUTS (AINP, AINN)

The ADS1271 measures the differential input signal V_{IN} = (AINP – AINN) against the differential reference V_{REF} = (VREFP – VREFN). The most positive measurable differential input is $+V_{REF}$, which produces the most positive digital output code of 7FFFFFh. Likewise, the most negative measurable differential input is $-V_{REF}$, which produces the most negative digital output code of 800000h.

While the ADS1271 measures the differential input signal, the absolute input voltage is also important. This is the voltage on either input (AINP or AINN) with respect to AGND. The range for this voltage is:

$$-0.1V < (AINN \text{ or } AINP) < AVDD + 0.1V$$

If either input is taken below –0.4V or above (AVDD + 0.4), ESD protection diodes on the inputs may turn on.

If these conditions are possible, external Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see *Absolute Maximum Ratings*).

The ADS1271 uses switched-capacitor circuitry to measure the input voltage. Internal capacitors are charged by the inputs and then discharged. Figure 44 shows a conceptual diagram of these circuits. Switch S2 represents the net effect of the modulator circuitry in discharging the sampling capacitor; the actual implementation is different. The timing for switches S1 and S2 is shown in Figure 45. The sampling time (t_{SAMPLE}) is the inverse of modulator sampling frequency (f_{MOD}) and is a function of the mode, format, and frequency of CLK, as shown in Table 2. When using the Frame-Sync format with High-Resolution or Low-Power modes, the ratio between f_{MOD} and f_{CLK} depends on the frame period that is set by the FSYNC input.

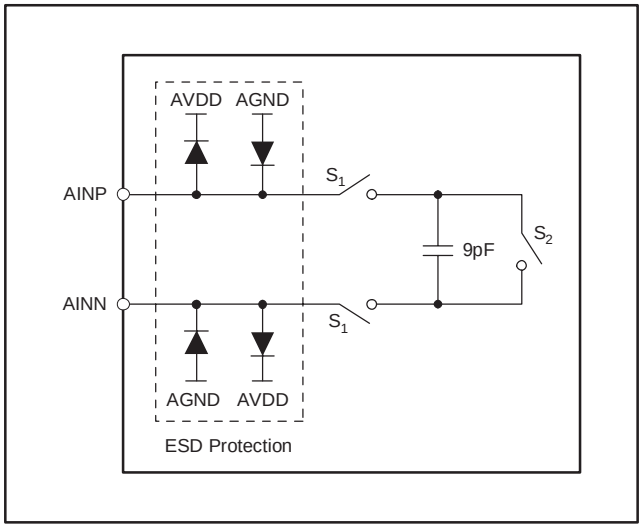


Figure 44. Equivalent Analog Input Circuitry

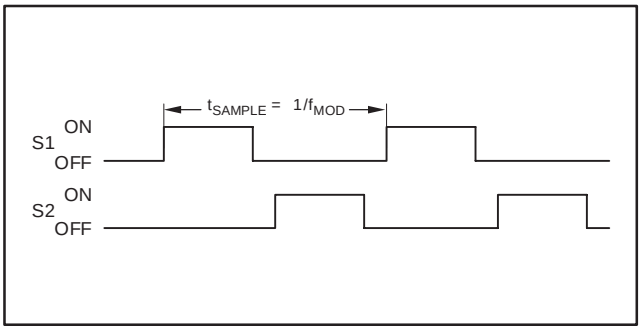


Figure 45. S1 and S2 Switch Timing for Figure 44

Table 2. Modulator Frequency for the Different Mode and Format Settings

MODE	INTERFACE FORMAT	f_{MOD}
High-Speed	SPI or Frame-Sync	$f_{CLK}/4$
High-Resolution	SPI	$f_{CLK}/4$
	Frame-Sync	$f_{CLK}/4$ or $f_{CLK}/2$
Low-Power	SPI	$f_{CLK}/8$
	Frame-Sync	$f_{CLK}/8$ or $f_{CLK}/4$

The average load presented by the switched capacitor input can be modeled with an effective differential impedance, as shown in Figure 46. Note that the effective impedance is a function of f_{MOD}.

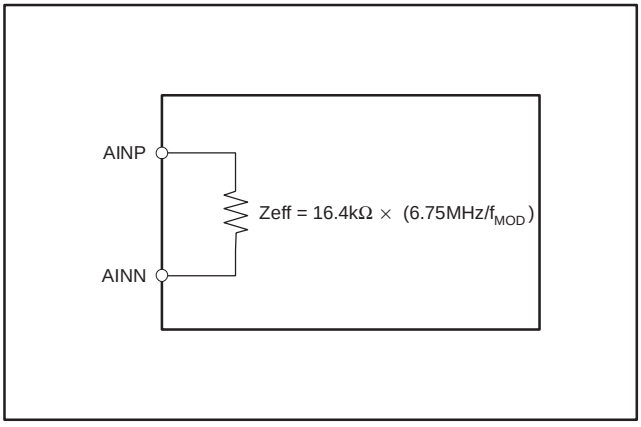


Figure 46. Effective Input Impedances

The ADS1271 is a very high-performance ADC. For optimum performance, it is critical that the appropriate circuitry be used to drive the ADS1271 inputs. See the *Application Information* section for the recommended circuits.

VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference for the ADS1271 ADC is the differential voltage between VREFP and VREFN: V_{REF} = (VREFP−VREFN). The reference inputs use a structure similar to that of the analog inputs with the equivalent circuitry on the reference inputs shown in Figure 47. As with the analog inputs, the load presented by the switched capacitor can be modeled with an effective impedance, as shown in Figure 48.

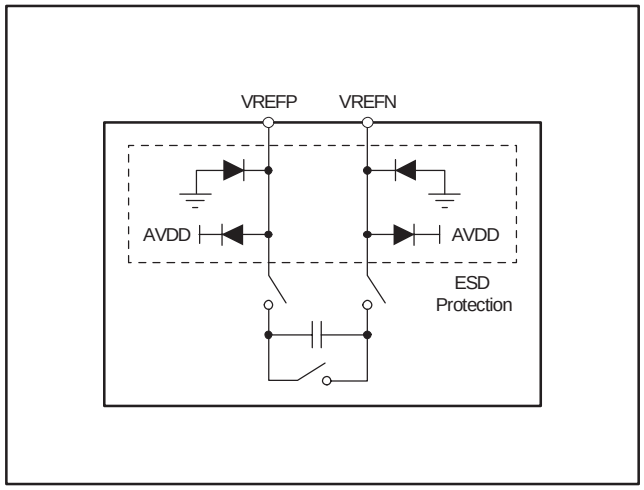


Figure 47. Equivalent Reference Input Circuitry

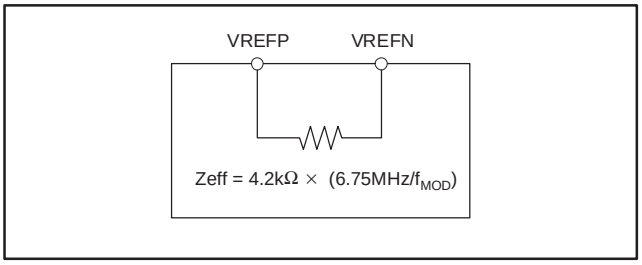


Figure 48. Effective Reference Impedance

ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AGND by more than 0.4V, and likewise do not exceed AVDD by 0.4V. If these conditions are possible, external Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see *Absolute Maximum Ratings*).

Note that the valid operating range of the reference inputs is limited to the following:

For the ADS1271:

$-0.1V \le VREFN \le VREFP - 2V$

$VREFN + 2V \le VREFP \le AVDD - 0.5V$

For the ADS1271B:

$-0.1V \le VREFN \le VREFP - 0.5V$

$VREFN + 0.5V \le VREFP \le AVDD + 0.1V$

A high-quality reference voltage with the appropriate drive strength is essential for achieving the best performance from the ADS1271. Noise and drift on the reference degrade overall system performance. See the *Application Information* section for example reference circuits.

CLOCK INPUT (CLK)

The ADS1271 requires an external clock signal to be applied to the CLK input pin. As with any high-speed data converter, a high-quality, low-jitter clock is essential for optimum performance. Crystal clock oscillators are the recommended clock source. Make sure to avoid excess ringing on the clock input; keeping the clock trace as short as possible using a 50Ω series resistor will help.

The ratio between the clock frequency and output data rate is a function of the mode and format. Table 3 shows the ratios when the SPI format is selected. Also included in this table is the typical CLK frequency and the corresponding data rate. When High-Speed mode is used, each conversion takes 256 CLK periods. When High-Resolution or Low-Power modes are selected, the conversions take 512 CLK periods.

Table 4 shows the ratios when the Frame-Sync format is selected. When using the Frame-Sync format in either High-Resolution or Low-Power mode, the f_{CLK}/f_{DATA} ratio can be 256 or 512. The ADS1271 automatically detects which ratio is being used. Using a ratio of 256 allows the CLK frequency to be reduced by a factor of two while maintaining the same data rate. The output data rate scales with the clock frequency. See the *Serial Interface* section for more details on the Frame-Sync operation.

Table 3. Clock Ratios for SPI Format

MODE SELECTION	f_{CLK}/f_{DATA}	TYPICAL f_{CLK} (MHz)	→	CORRESPONDING DATA RATE (SPS)
High-Speed	256	27	→	105,469
High-Resolution	512	27	→	52,734
Low-Power	512	27	→	52,734

Table 4. Clock Ratios for Frame-Sync Format

MODE SELECTION	f_{CLK}/f_{FRAME}	TYPICAL f_{CLK} (MHz)	→	CORRESPONDING DATA RATE (SPS)
High-Speed	256	27	→	105,469
High-Resolution	256	13.5	→	52,734
	512	27	→	52,734
Low-Power	256	13.5	→	52,734
	512	27	→	52,734

MODE SELECTION (MODE)

The ADS1271 supports three modes of operation: High-Speed, High-Resolution, and Low-Power. The mode selection is determined by the status of the digital input MODE pin, as shown in Table 5. A high impedance, or *floating,* condition allows the MODE pin to support a third state. The ADS1271 constantly monitors the status of the MODE pin during operation and responds to a change in status after 12,288 CLK periods. When floating the MODE pin, keep the total capacitance on the pin less than 100pF and the resistive loading greater than 10MΩ to ensure proper operation. Changing the mode clears the internal offset calibration value. If onboard offset calibration is being used, be sure to recalibrate after a mode change.

When daisy-chaining multiple ADS1271s together and operating in High-Resolution mode (MODE pin floating), the MODE pin of each device must be isolated from one another; this ensures proper device operation. The MODE pins can be tied together for High-Speed and Low-Power modes.

Table 5. Mode Selection

MODE PIN STATUS	MODE SELECTION
Logic Low (DGND)	High-Speed
Float(1)	High-Resolution
Logic High (DVDD)	Low-Power

(1) Load on MODE: C < 100pF, R > 10MΩ.

When using the SPI format, $\overline{\text{DRDY}}$ is held high after a mode change occurs until settled (or valid) data is ready, as shown in Figure 49.

In Frame-Sync format, the DOUT pin is held low after a mode change occurs until settled data is ready, as shown in Figure 49. Data can be read from the device to detect when DOUT changes to logic 1, indicating valid data.

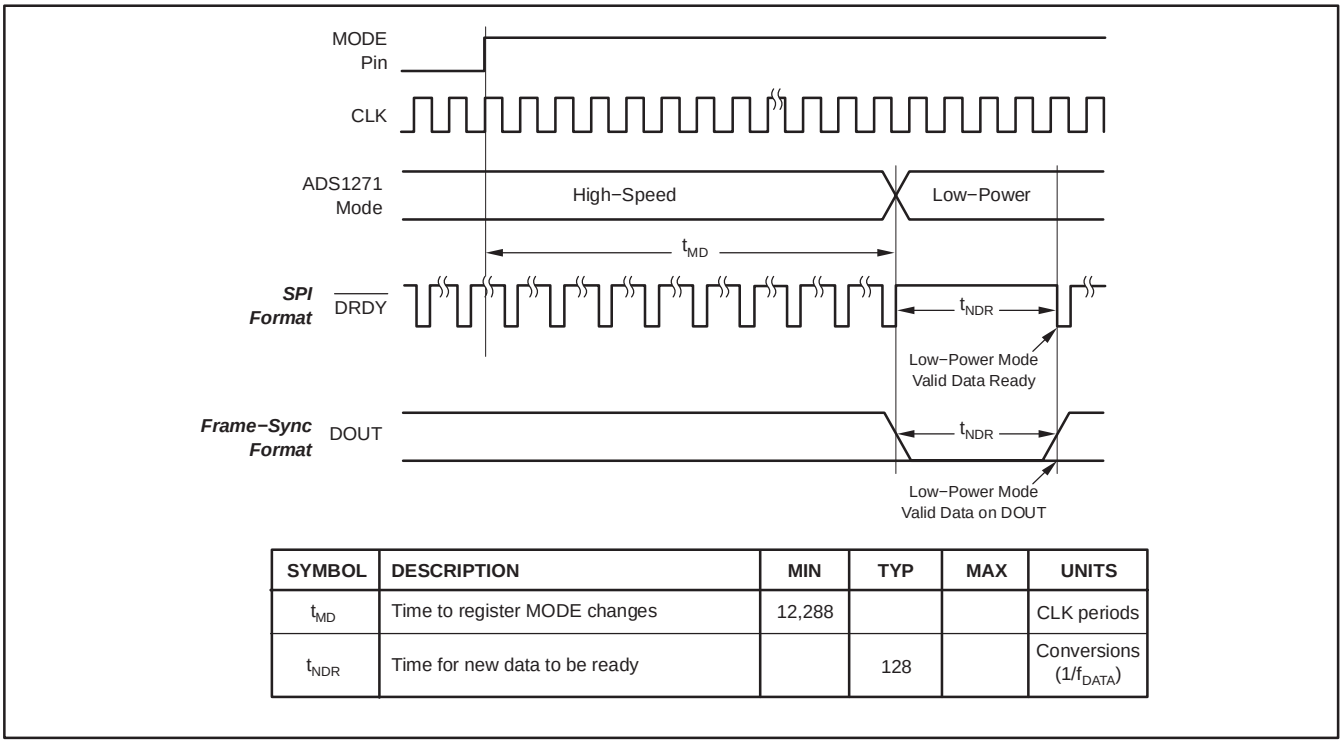
FORMAT SELECTION (FORMAT)

To help connect easily to either microcontrollers or DSPs, the ADS1271 supports two formats for the serial interface: an SPI-compatible interface and a Frame-Sync interface. The format is selected by the FORMAT pin, as shown in Table 6. If the status of this pin changes, perform a sync operation afterwards to ensure proper operation. The modulator output mode does not require a sync operation.

Table 6. Format Selection

FORMAT PIN STATUS	SERIAL INTERFACE FORMAT
Logic Low (DGND)	SPI
Float(1)	Modulator Output(2)
Logic High (DVDD)	Frame-Sync

(1) Load on FORMAT: C < 100pF, R > 10MΩ.
(2) See *Modulator Output* section.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{MD}	Time to register MODE changes	12,288			CLK periods
t_{NDR}	Time for new data to be ready		128		Conversions ($1/f_{DATA}$)

Figure 49. Mode Change Timing

SYNCHRONIZATION

The $\overline{\text{SYNC}}/\overline{\text{PDWN}}$ pin has two functions. When pulsed, it synchronizes the start of conversions and, if held low for more than 2^{19} CLK cycles (t_{SYN}), places the ADS1271 in Power-Down mode. The $\overline{\text{SYNC}}/\overline{\text{PDWN}}$ pin can be left high for continuous data acquisition. See the *Power-Down and Offset Calibration* section for more details.

The ADS1271 can be synchronized by pulsing the $\overline{\text{SYNC}}/\overline{\text{PDWN}}$ pin low and then returning the pin high. When the pin goes low, the conversion process is stopped, and the internal counters used by the digital filter are reset. When the $\overline{\text{SYNC}}/\overline{\text{PDWN}}$ pin is returned high, the conversion process is restarted. Synchronization allows the conversion to be aligned with an external event; for example, the changing of an external multiplexer on the analog inputs, or by a reference timing pulse.

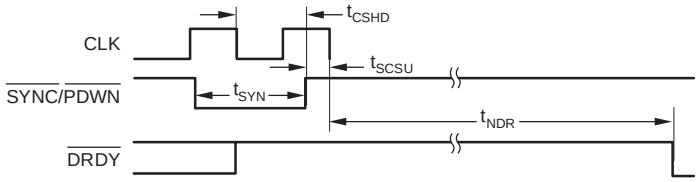
The $\overline{\text{SYNC}}/\overline{\text{PDWN}}$ pin is capable of synchronizing multiple ADS1271s to within the same CLK cycle. Figure 50 shows the timing requirement of $\overline{\text{SYNC}}/\overline{\text{PDWN}}$ and CLK in SPI format.

Figure 51 shows the timing requirement for Frame-Sync format.

After synchronization, indication of valid data depends on the whether SPI or Frame-Sync format was used.

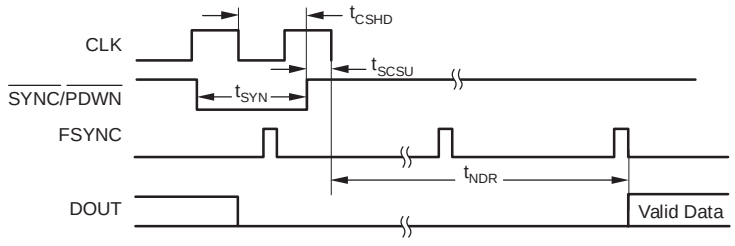
In the SPI format, $\overline{\text{DRDY}}$ goes high as soon as $\overline{\text{SYNC}}/\overline{\text{PDWN}}$ is taken low, as shown in Figure 50. After $\overline{\text{SYNC}}/\overline{\text{PDWN}}$ is returned high, $\overline{\text{DRDY}}$ stays high while the digital filter is settling. Once valid data is ready for retrieval, $\overline{\text{DRDY}}$ goes low.

In the Frame-Sync format, DOUT goes low as soon as $\overline{\text{SYNC}}/\overline{\text{PDWN}}$ is taken low, as shown in Figure 51. After $\overline{\text{SYNC}}/\overline{\text{PDWN}}$ is returned high, DOUT stays low while the digital filter is settling. Once valid data is ready for retrieval, DOUT begins to output valid data. For proper synchronization, FSYNC, SCLK, and CLK must be established before taking $\overline{\text{SYNC}}/\overline{\text{PDWN}}$ high, and must then remain running.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SCSU}	$\overline{\text{SYNC}}/\overline{\text{PWDN}}$ to CLK setup time	5			ns
t_{CSHD}	CLK to $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ hold time	10			ns
t_{SYN}	Synchronize pulse width	1		2^{18}	CLK periods
t_{NDR}	Time for new data to be ready		128		Conversions ($1/f_{DATA}$)

Figure 50. Synchronization Timing for SPI format



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SCSU}	$\overline{\text{SYNC}}/\overline{\text{PWDN}}$ to CLK setup time	5			ns
t_{CSHD}	CLK to $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ hold time	10			ns
t_{SYN}	Synchronize pulse width	1		2^{18}	CLK periods
t_{NDR}	Time for new data to be ready	128		129	Conversions ($1/f_{DATA}$)

Figure 51. Synchronization Timing for Frame-Sync Format

POWER-DOWN AND OFFSET CALIBRATION

In addition to controlling synchronization, the $\overline{SYNC}/\overline{PDWN}$ pin also serves as the control for Power-Down mode and offset calibration. To enter this mode, hold the $\overline{SYNC}/\overline{PDWN}$ pin low for at least 2^{19} CLK periods. While in Power-Down mode, both the analog and digital circuitry are completely deactivated. The digital inputs are internally disabled so that is not necessary to shut down CLK and SCLK. To exit Power-Down mode, return $\overline{SYNC}/\overline{PDWN}$ high on the rising edge of CLK.

The ADS1271 uses a chopper-stabilized modulator to provide inherently very low offset drift. To further minimize offset, the ADS1271 automatically performs an offset self-calibration when exiting Power-Down mode. When power down completes, the offset self-calibration begins with the inputs AINP and AINN automatically disconnected from the signal source and internally shorted together. There is no need to modify the signal source applied to the analog inputs during this calibration. *It is critical for the reference voltage to be stable when exiting Power-Down mode; otherwise, the calibration will be corrupted.*

The offset self-calibration only removes offset errors internal to the device, not offset errors due to external sources.

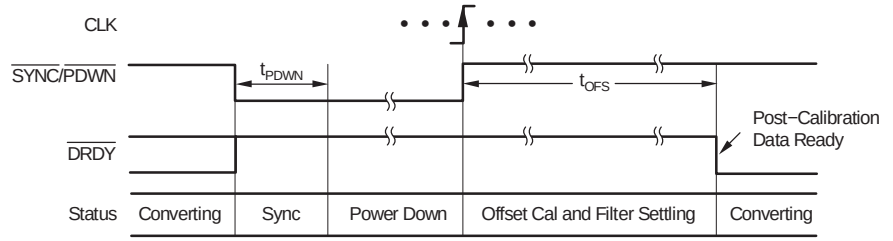
NOTE: When an offset self-calibration is performed, the resulting offset value will vary each time within the peak-to-peak noise range of the converter. In High-Speed mode, this is typically 178 LSBs.

The offset calibration value is cleared whenever the device mode is changed (for example, from High-Speed mode to High-Resolution mode).

When using the SPI format, $\overline{DRDY}$ will stay high after exiting Power-Down mode while the digital filter settles, as shown in Figure 52.

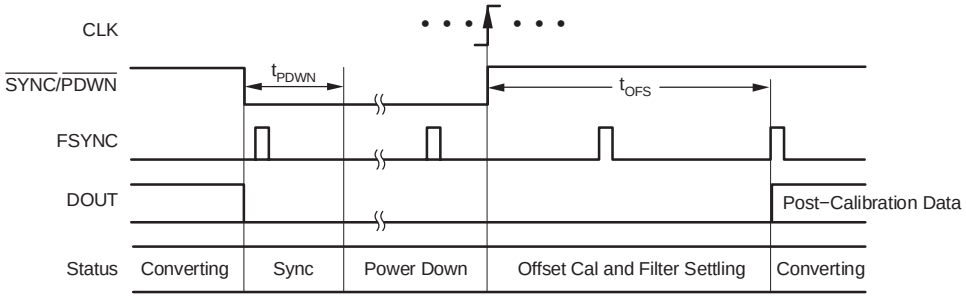
When using the Frame-Sync format, DOUT will stay low after exiting Power-Down mode while the digital filter settles, as shown in Figure 53.

NOTE: In Power-Down mode, the inputs of the ADS1271 must be driven (do not float) and the device drives the outputs driven to a DC level.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{PDWN}	$\overline{SYNC}/\overline{PDWN}$ pulse width to enter Power−Down mode	2^{19}			CLK periods
t_{OFS}	Time for offset calibration and filter settling		256		Conversions ($1/f_{DATA}$)

Figure 52. Power-Down Timing for SPI format



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{PDWN}	$\overline{SYNC}/\overline{PDWN}$ pulse width to enter Power−Down mode	2^{19}			CLK periods
t_{OFS}	Time for offset calibration and filter settling	256		257	Conversions ($1/f_{DATA}$)

Figure 53. Power-Down Timing for Frame-Sync Format

POWER-UP SEQUENCE

The analog and digital supplies should be applied before any analog or digital input is driven. The power supplies may be sequenced in any order. Once the supplies and the voltage reference inputs have stabilized, data can be read from the device.

FREQUENCY RESPONSE

The digital filter sets the overall frequency response. The filter uses a multi-stage FIR topology to provide linear phase with minimal passband ripple and high stopband attenuation. The oversampling ratio of the digital filter (that is, the ratio of the modulator sampling to the output data rate: f_{MOD}/f_{DATA}) is a function of the selected mode, as shown in Table 7. f_{MOD} is CLK/2, CLK/4, or CLK/8, depending on the mode.

Table 7. Oversampling Ratio versus Mode

MODE	OVERSAMPLING RATIO (f_{MOD}/f_{DATA})
High-Speed	64
High-Resolution	128
Low-Power	64

High-Speed and Low-Power Modes

The digital filter configuration is the same in both High-Speed and Low-Power modes with the oversampling ratio set to 64. Figure 54 shows the frequency response in High-Speed and Low-Power modes normalized to f_{DATA}. Figure 55 shows the passband ripple. The transition from passband to stop band is illustrated in Figure 56. The overall frequency response repeats at 64x multiples of the modulator frequency f_{MOD}, as shown in Figure 57. These image frequencies, if present in the signal and not externally filtered, will fold back (or alias) into the passband, causing errors. The stop-band of the ADS1271 provides 100dB attenuation of frequencies that begin just beyond the passband and continue out to f_{MOD}. Placing an antialiasing, low-pass filter in front of the ADS1271 inputs is recommended to limit possible high-amplitude out-of-band signals and noise.

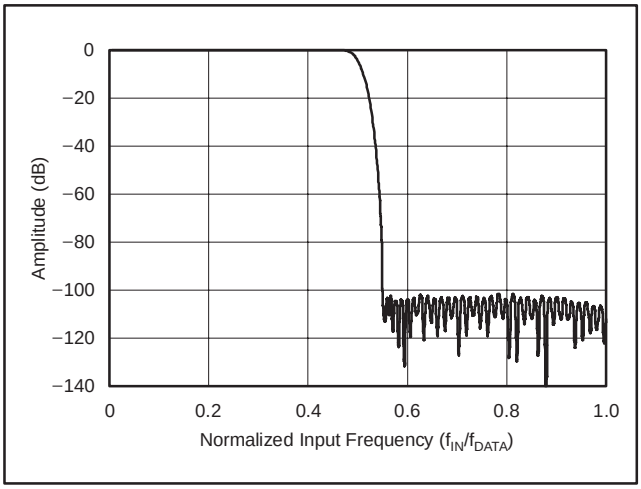


Figure 54. Frequency Response for High-Speed and Low-Power Modes

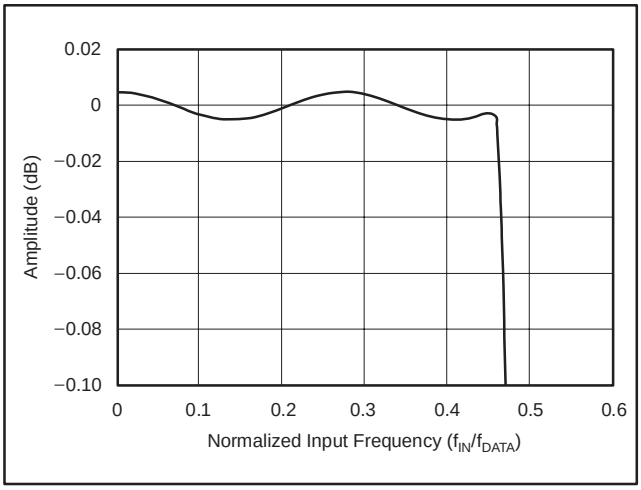


Figure 55. Passband Response for High-Speed and Low-Power Modes

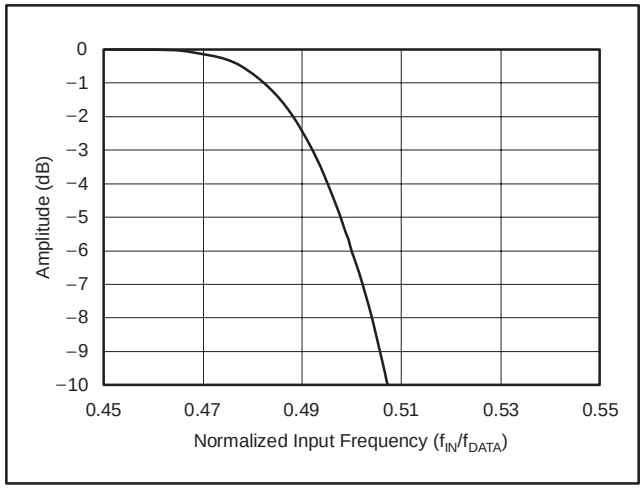


Figure 56. Transition Band Response for High-Speed and Low-Power Modes

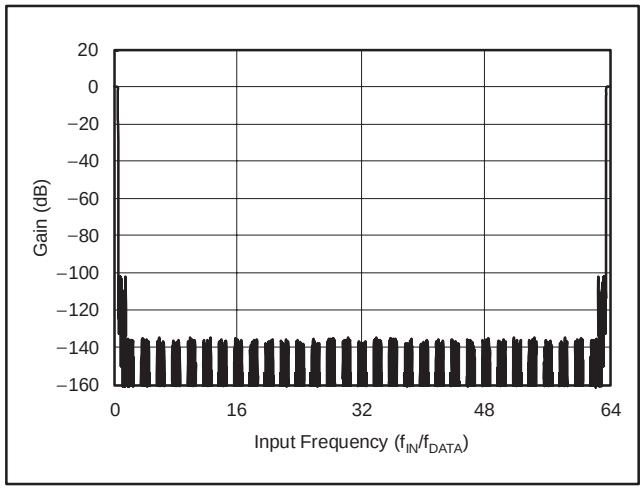


Figure 57. Frequency Response Out to f_{MOD} for High-Speed and Low-Power Modes

High-Resolution Mode

The oversampling ratio is 128 in High-Resolution mode. Figure 58 shows the frequency response in High-Resolution mode normalized to f_{DATA}. Figure 59 shows the passband ripple, and the transition from passband to stop band is illustrated in Figure 60. The overall frequency response repeats at multiples of the modulator frequency f_{MOD}, (128 × f_{DATA}), as shown in Figure 61. The stop band of the ADS1271 provides 100dB attenuation of frequencies that begin just beyond the passband and continue out to f_{MOD}. Placing an antialiasing, low-pass filter in front of the ADS1271 inputs is recommended to limit possible high-amplitude out-of-band signals and noise.

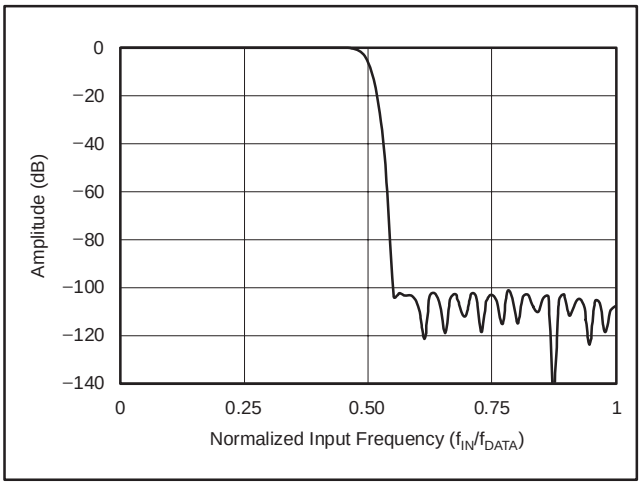


Figure 58. Frequency Response for High-Resolution Mode

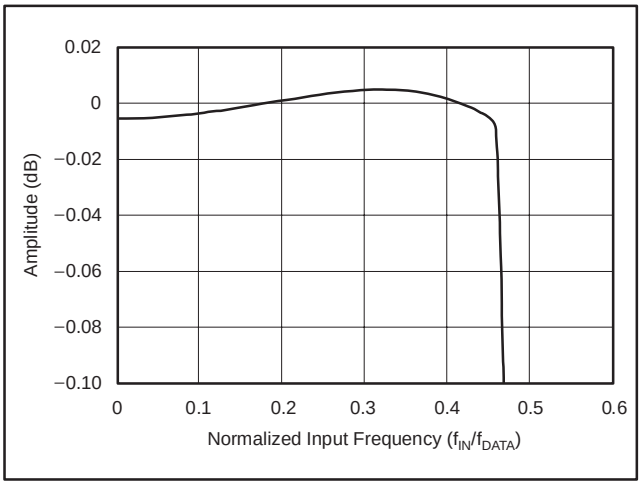


Figure 59. Passband Response for High-Resolution Mode

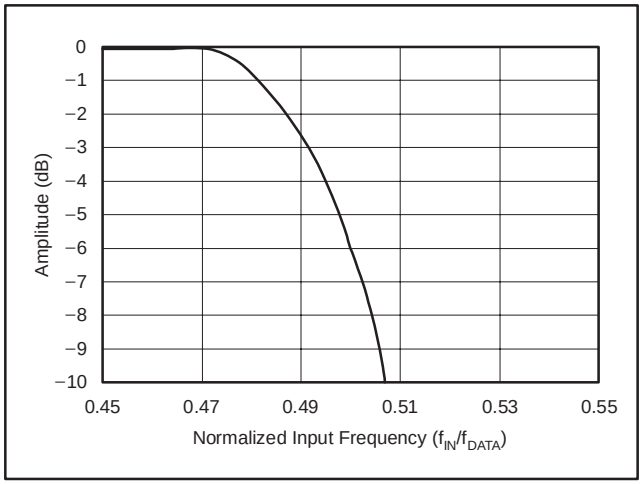


Figure 60. Transition Band Response for High-Resolution Mode

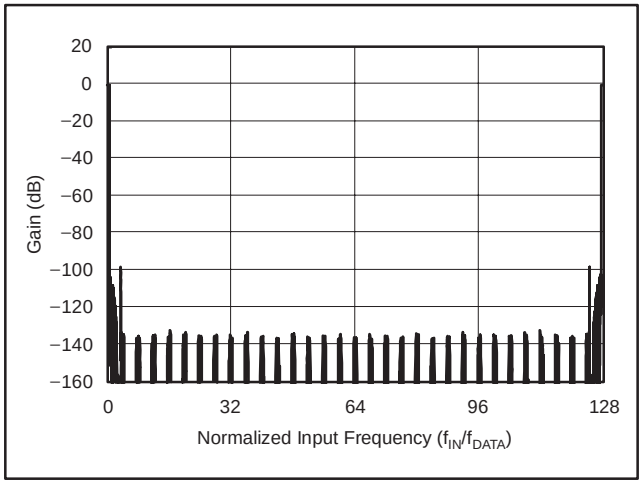


Figure 61. Frequency Response out to f_{MOD} for High-Resolution Mode

Table 8. Antialiasing Filter Order Image Rejection

ANTIALIASING FILTER ORDER	IMAGE REJECTION (dB) (f_{-3dB} at f_{DATA})	
	HS, LP	HR
1	39	45
2	75	87
3	111	129

PHASE RESPONSE

The ADS1271 incorporates a multiple stage, linear phase digital filter. Linear phase filters exhibit constant delay time versus input frequency (constant group delay). This means the time delay from any instant of the input signal to the same instant of the output data is constant and is independent of input signal frequency. This behavior results in essentially zero phase errors when analyzing multi-tone signals.

SETTLING TIME

As with frequency and phase response, the digital filter also determines settling time. Figure 62 shows the output settling behavior after a step change on the analog inputs normalized to conversion periods. The X axis is given in units of conversion. Note that after the step change on the input occurs, the output data changes very little prior to 30 conversion periods. The output data is fully settled after 76 conversion periods for High-Speed and Low-Power modes, and 78 conversions for High-Resolution mode.

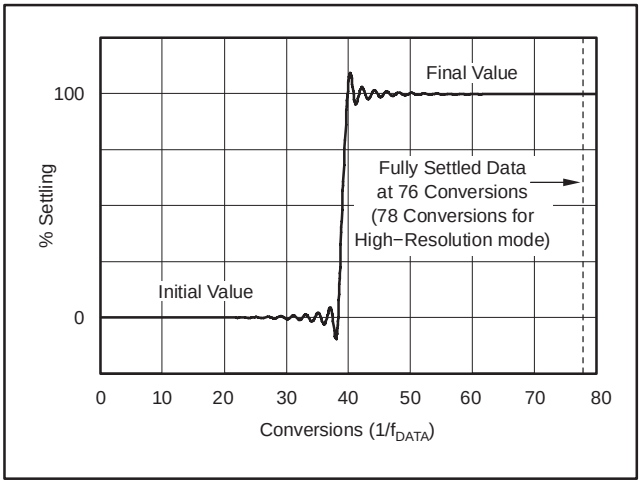


Figure 62. Settling Time for All Power Modes

DATA FORMAT

The ADS1271 outputs 24 bits of data in two's complement format.

A positive full-scale input produces an output code of 7FFFFFh, and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 9 summarizes the ideal output codes for different input signals.

Table 9. Ideal Output Code versus Input Signal

INPUT SIGNAL V_{IN} (AINP − AINN)	IDEAL OUTPUT CODE(1)
$\geq +V_{REF}$	7FFFFFh
$\frac{+V_{REF}}{2^{23} - 1}$	000001h
0	000000h
$\frac{-V_{REF}}{2^{23} - 1}$	FFFFFFh
$\leq -V_{REF}\left(\frac{2^{23}}{2^{23} - 1}\right)$	800000h

(1) Excludes effects of noise, INL, offset and gain errors.

SERIAL INTERFACE

Data is retrieved from the ADS1271 using the serial interface. To provide easy connection to either microcontrollers or DSPs, two formats are available for the interface: SPI and Frame-Sync. The FORMAT pin selects the interface. The same pins are used for both interfaces (SCLK, $\overline{\text{DRDY}}$/FSYNC, DOUT and DIN), though their respective functionality depends on the particular interface selected.

SPI SERIAL INTERFACE

The SPI-compatible format is a simple read-only interface. Data ready for retrieval is indicated by the $\overline{\text{DRDY}}$ output and is shifted out on the falling edge of SCLK, MSB first. The interface can be daisy-chained using the DIN input when using multiple ADS1271s. See the *Daisy-Chaining* section for more information.

SCLK (SPI Format)

The serial clock (SCLK) features a Schmitt-triggered input and shifts out data on DOUT on the falling edge. It also shifts in data on the falling edge on DIN when this pin is being used for daisy-chaining. The device shifts data out on the falling edge and the user shifts this data in on the rising edge. Even though the SCLK input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. SCLK should be held low after data retrieval. SCLK may be run as fast as the CLK frequency. SCLK may be either in free-running or stop-clock operation between conversions. For best performance, limit f_{SCLK}/f_{CLK} to ratios of 1, 1/2, 1/4, 1/8, etc. When the device is configured for modulator output, SCLK becomes the modulator clock output (see the *Modulator Output* section).

For the f_{SCLK}/f_{CLK} ratio of 1, care must be observed that these signals are not tied together. After Power On, SCLK remains an output until a few clocks have been received on the CLK input.

$\overline{\text{DRDY}}$/FSYNC

In the SPI format, this pin functions as the $\overline{\text{DRDY}}$ output. It goes low when data is ready for retrieval and then returns high on the falling edge of the first subsequent SCLK. If data is not retrieved (that is, SCLK is held low), $\overline{\text{DRDY}}$ will pulse high just before the next conversion data is ready, as shown in Figure 63. The new data is loaded within the ADS1271 one CLK cycle before $\overline{\text{DRDY}}$ goes low. All data must be shifted out before this time to avoid being overwritten.

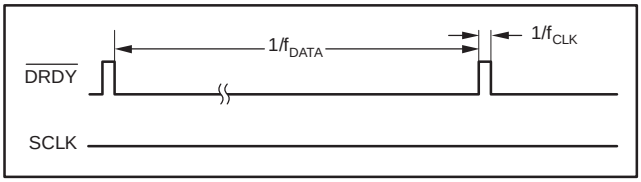


Figure 63. DRDY Timing with No Readback

DOUT

The conversion data is shifted out on DOUT. The MSB data is valid on DOUT when $\overline{\text{DRDY}}$ goes low. The subsequent bits are shifted out with each falling edge of SCLK. If daisy-chaining, the data shifted in using DIN will appear on DOUT after all 24 bits have been shifted out. When the device is configured for modulator output, DOUT becomes the modulator data output (see the *Modulator Output* section).

DIN

This input is used when multiple ADS1271s are to be daisy-chained together. The DOUT pin of the first device connects to the DIN pin of the next, etc. It can be used with either the SPI or Frame-Sync formats. Data is shifted in on the falling edge of SCLK. When using only one ADS1271, tie DIN low. See the *Daisy-Chaining* section for more information.

FRAME-SYNC SERIAL INTERFACE

Frame-Sync format is similar to the interface often used on audio ADCs. It operates in *slave* fashion—the user must supply framing signal FSYNC (similar to the *left/right clock* on stereo audio ADCs) and the serial clock SCLK (similar to the *bit clock* on audio ADCs). The data is output MSB first or *left-justified*. When using Frame-Sync format, the CLK, FSYNC and SCLK inputs must be synchronized together, as described in the following sub-sections.

SCLK (Frame-Sync Format)

The serial clock (SCLK) features a Schmitt-triggered input and shifts out data on DOUT on the falling edge. It also shifts in data on the falling edge on DIN when this pin is being used for daisy-chaining. Even though SCLK has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. When using Frame-Sync format, SCLK must run continuously. If it is shut down, the data readback will be corrupted. Frame-Sync format requires a specific relationship between SCLK and FSYNC, determined by the mode shown in Table 10. When the device is configured for modulator output, SCLK becomes the modulator clock output (see the *Modulator Output* section).

Table 10. SCLK Period When Using Frame-Sync Format

MODE	REQUIRED SCLK PERIOD
High-Speed	$\tau_{FRAME}/64$
High-Resolution	$\tau_{FRAME}/128$
Low-Power	$\tau_{FRAME}/64$

$\overline{\text{DRDY}}$/FSYNC

In Frame-Sync format, this pin is used as the FSYNC input. The frame-sync input (FSYNC) sets the frame period. The required FSYNC periods are shown in Table 11. For High-Speed mode, the FSYNC period must be 256 CLK periods. For both High-Resolution and Low-Power modes, the FSYNC period can be either 512 or 256 CLK periods; the ADS1271 will automatically detect which is being used. If the FSYNC period is not the proper value, data readback will be corrupted. It is recommended that FSYNC be aligned with the falling edge of SCLK.

Table 11. FSYNC Period

MODE	REQUIRED FSYNC PERIOD
High-Speed	256 CLK Periods
High-Resolution	256 or 512 CLK periods
Low-Power	256 or 512 CLK periods

DOUT

The conversion data is shifted out on DOUT. The MSB data becomes valid on DOUT on the CLK rising edge prior to FSYNC going high. The subsequent bits are shifted out with each falling edge of SCLK. If daisy-chaining, the data shifted in using DIN will appear on DOUT after all 24 bits have been shifted out. When the device is configured for modulator output, DOUT becomes the modulator data output (see the *Modulator Output* section).

DIN

This input is used when multiple ADS1271s are to be daisy-chained together. It can be used with either SPI or Frame-Sync formats. Data is shifted in on the falling edge of SCLK. When using only one ADS1271, tie DIN low.See the *Daisy-Chaining* section for more information.

DAISY-CHAINING

Multiple ADS1271s can be daisy-chained together to simplify the serial interface connections. The DOUT of one ADS1271 is connected to the DIN of the next ADS1271. The first DOUT provides the output data and the last DIN in the chain is connected to ground. A common SCLK is used for all the devices in the daisy chain. Figure 64 shows an example of a daisy chain with four ADS1271s. Figure 65 shows the timing diagram when reading back in the SPI format. It takes 96 SCLKs to shift out all the data.

In SPI format, it is recommended to tie all the $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ inputs together, which forces synchronization of all the devices. It is only necessary to monitor the $\overline{\text{DRDY}}$ output of one device when multiple devices are configured this way.

In Frame-Sync format, all of the devices are driven to synchronization by the FSYNC and SCLK inputs. However, to ensure synchronization to the same f_{CLK} cycle, it is recommended to tie all $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ inputs together.

The device clocks the $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ pin on the falling edge of f_{CLK}. To ensure exact synchronization, the $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ pin should transition on the rising edge of f_{CLK}

Since DOUT and DIN are both shifted on the falling edge of SCLK, the propagation delay on DOUT creates the setup time on DIN. Minimize the skew in SCLK to avoid timing violations. See *Mode Selection* section for MODE pin use when daisy-chaining.

The SPI format offers the most flexibility when daisy-chaining because there is more freedom in setting the SCLK frequency. The maximum number of ADS1271s that can be daisy-chained is determined by dividing the conversion time ($1/f_{DATA}$) by the time needed to read back all 24 bits ($24 \times 1/f_{SCLK}$).

Consider the case where:

f_{CLK} = 27MHz

mode = High-Resolution (52,734SPS)

format = SPI

f_{SCLK} = 27MHz

The maximum length of the daisy-chain is:

27MHz/(24 × 52,734SPS) = 21.3

Rounding down gives 21 as the maximum number of ADS1271s that can be daisy-chained.

Daisy-chaining also works in Frame-Sync format, but the maximum number of devices that can be daisy-chained is less than when using the SPI format. The ratio between the frame period and SCLK period is fixed, as shown in Table 10. Using these values, the maximum number of devices is two for High-Speed and Low-Power modes, and five for High-Resolution mode.

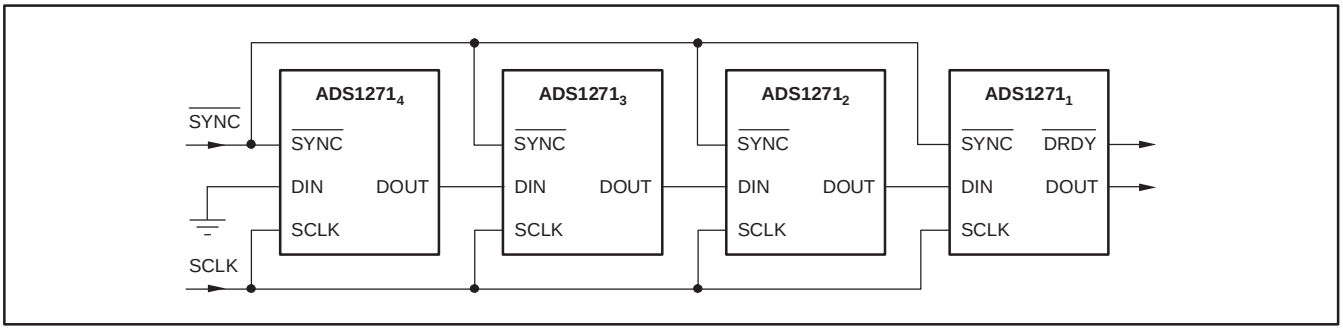


Figure 64. Example of SPI-Format, Daisy-Chain Connection for Multiple ADS1271s

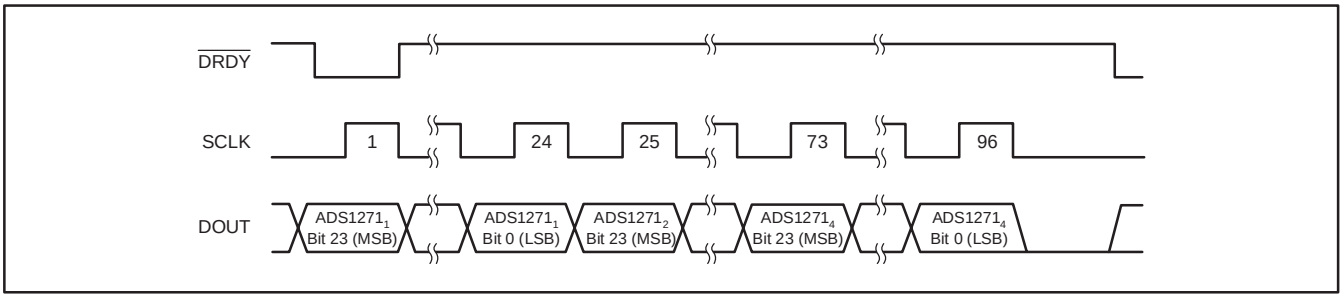


Figure 65. Timing Diagram for Example in Figure 64 (SPI Format)

MODULATOR OUTPUT

The ADS1271 incorporates a 6th-order, single-bit, chopper-stabilized modulator followed by a multi-stage digital filter, which yields the conversion results. The data stream output of the modulator is available directly, bypassing the internal digital filter. In this mode, an external digital filter implemented in an ASIC, FPGA, or similar device is required. To invoke the modulator output, float the FORMAT pin and tie DIN to DVDD. DOUT then becomes the modulator data stream output and SCLK becomes the modulator clock output. The $\overline{\text{DRDY}}$/FSYNC pin becomes an unused output and can be ignored. The normal operation of the Frame-Sync and SPI interfaces is disabled, and the functionality of SCLK changes from an input to an output, as shown in Figure 66. Note that modulator output mode is specified for the B grade device only.

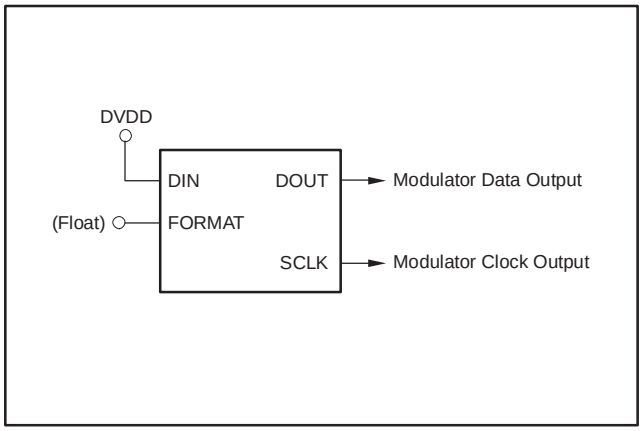


Figure 66. Modulator Output (B-Grade Device)

In modulator output mode, the frequency of the SCLK clock output depends on the mode selection of the ADS1271. Table 12 lists the modulator clock output frequency versus device mode.

Table 12. Modulator Output Clock Frequencies

MODE PIN	MODULATOR CLOCK OUTPUT (SCLK)
0	$f_{CLK}/4$
Float	$f_{CLK}/4$
1	$f_{CLK}/8$

Figure 67 shows the timing relationship of the modulator clock and data outputs.

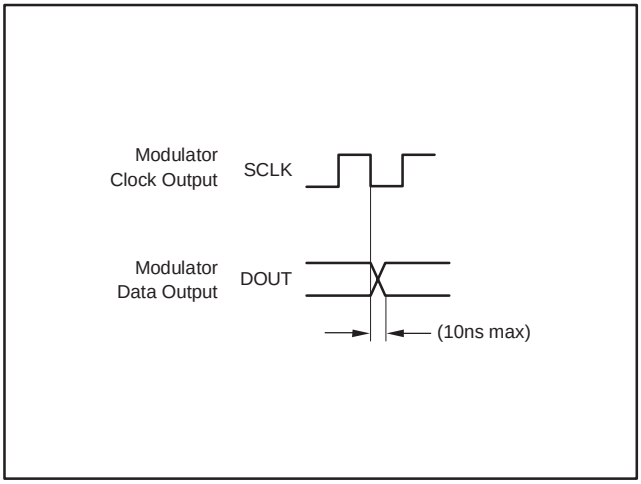


Figure 67. Modulator Output Timing

APPLICATION INFORMATION

To obtain the specified performance from the ADS1271, the following layout and component guidelines should be considered.

1. Power Supplies: The device requires two power supplies for operation: DVDD and AVDD. The allowed range for DVDD is 1.65V to 3.6V, and AVDD is restricted to 4.75V to 5.25V. Best performance is achieved when DVDD = 1.8V. For both supplies, use a 10μF tantalum capacitor, bypassed with a 0.1μF ceramic capacitor, placed close to the device pins. Alternatively, a single 10μF ceramic capacitor can be used. The supplies should be relatively free of noise and should not be shared with devices that produce voltage spikes (such as relays, LED display drivers, etc.). If a switching power supply source is used, the voltage ripple should be low (< 2mV). The power supplies may be sequenced in any order.

2. Ground Plane: A single ground plane connecting both AGND and DGND pins can be used. If separate digital and analog grounds are used, connect the grounds together at the converter.

3. Digital Inputs: It is recommended to source terminate the digital inputs to the device with 50Ω series resistors. The resistors should be placed close to the driving end of digital source (oscillator, logic gates, DSP, etc.) This helps to reduce ringing on the digital lines, which may lead to degraded ADC performance.

4. Analog/Digital Circuits: Place analog circuitry (input buffer, reference) and associated tracks together, keeping them away from digital circuitry (DSP, microcontroller, logic). Avoid crossing digital tracks across analog tracks to reduce noise coupling and crosstalk.

5. Reference Inputs: It is recommended to use a minimum 10μF tantalum with a 0.1μF ceramic capacitor directly across the reference inputs, VREFP and VREFN. The reference input should be driven by a low-impedance source. For best performance, the reference should have less than $3\mu V_{RMS}$ broadband noise. For references with noise higher than this, external reference filtering may be necessary.

6. Analog Inputs: The analog input pins must be driven differentially to achieve specified performance. A true differential driver or transformer (AC applications) can be used for this purpose. Route the analog inputs tracks (AINP, AINN) as a pair from the buffer to the converter using short, direct tracks and away from digital tracks.

   A 1nF to 10nF capacitor should be used directly across the analog input pins, AINP and AINN. A low-k dielectric (such as COG or film type) should be used to maintain low THD. Capacitors from each analog input to ground should be used. They should be no larger than 1/10 the size of the difference capacitor (typically 100pF) to preserve the AC common-mode performance.

7. Component Placement: Place the power supply, analog input, and reference input bypass capacitors as close as possible to the device pins. This is particularly important for the small-value ceramic capacitors. Surface-mount components are recommended to avoid the higher inductance of leaded components.

Figure 68 to Figure 70 illustrate basic connections and interfaces that can be used with the ADS1271.

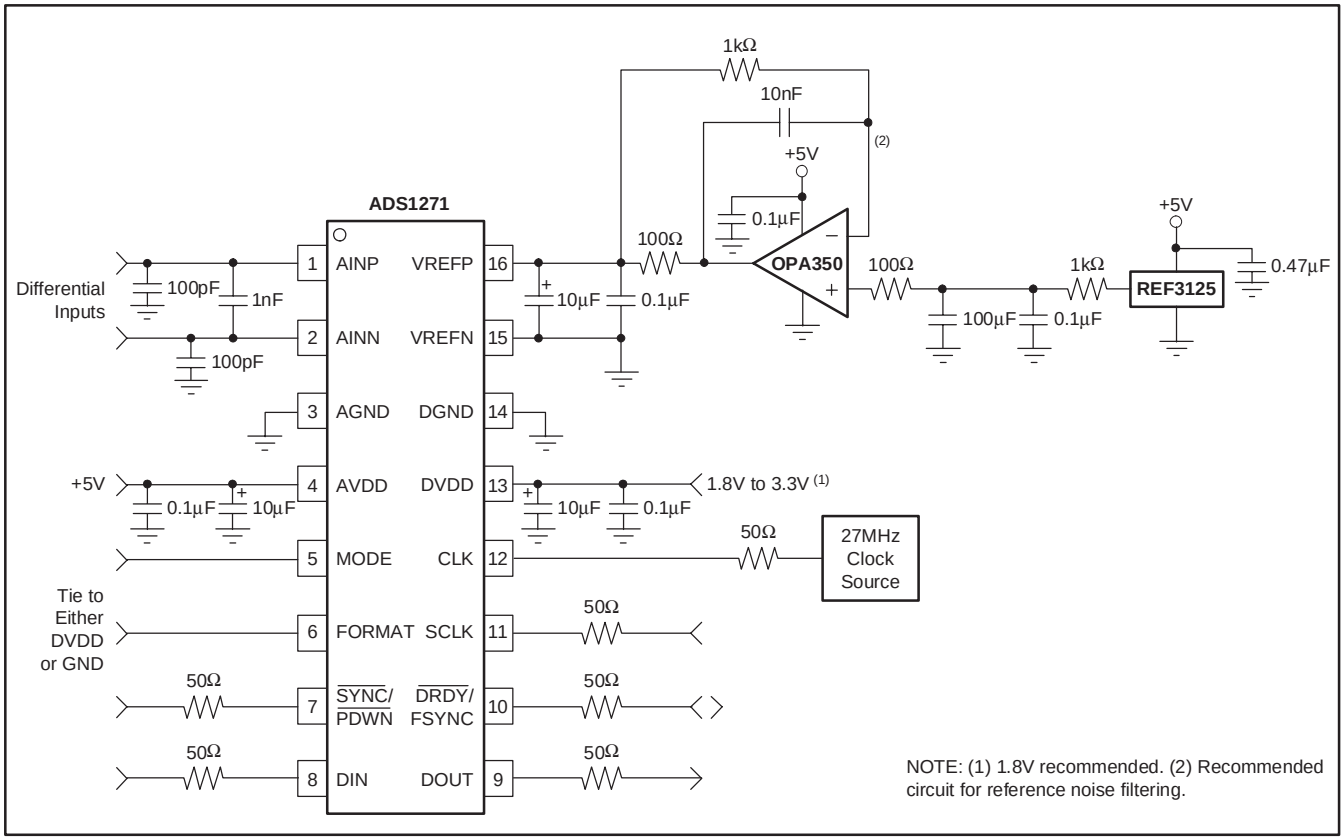


Figure 68. Basic Connection Drawing

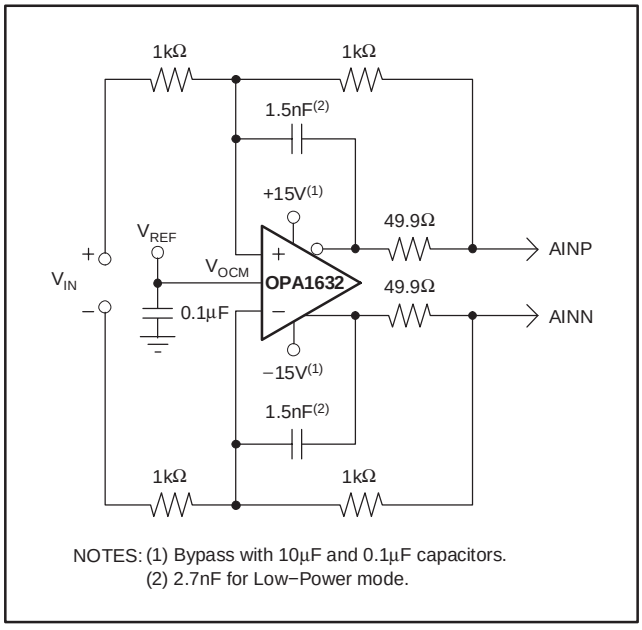


Figure 69. Basic Differential Input Signal Interface

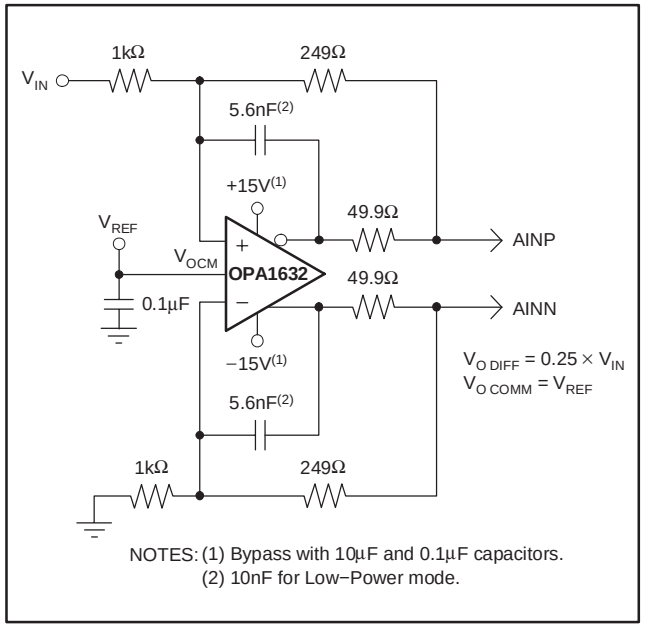


Figure 70. Basic Single-Ended Input Signal Interface

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
10/07	F	25	SCLK (SPI Format)	Added final paragraph to section.
9/07	E	20	Synchronization	Added sentence to 1st paragraph regarding $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ left high.
7/06	D	2	Absolute Maximum Ratings	Deleted lead temperature.
		7	Timing Characteristics: Frame-Sync Format	Changed t_{DDO} parameter from “falling edge” to “rising edge.”
				Added “(only 256 or 512 allowed)” to Note 1.
		16	Analog Inputs (AINP, AINN)	Changed “0.1V” to “0.4V” in 3rd paragraph
				Added 4th paragraph about clamp diode and series resistor requirements.
		17	Voltage ReferFence Inputs (VREFP, VREFN)	Changed “0.1V” to “0.4V” in 1st paragraph of right column.
				Added sentence about clamp diode and series resistor requirements.
		20	Synchronization	Changed text from 2nd paragraph through end of section.
				Changed Figure 50.
				Changed Figure 51.
		22	Frequency Response	Added “or CLK/8” to last sentence of 2nd paragraph.
		26	DOUT	Changed “SCLK” to “CLK” in 2nd sentence of 3rd paragraph.
		29	Application Information	Changed “REFP” to “VREFP” in part 5.
				Changed “REFN” to “VREFN” in part 5.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1271IBPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS 1271B	Samples
ADS1271IBPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS 1271B	Samples
ADS1271IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS 1271	Samples
ADS1271IPWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS 1271	Samples
ADS1271IPWR	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ADS 1271	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

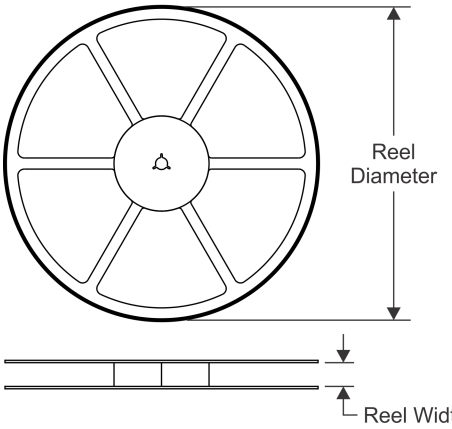
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

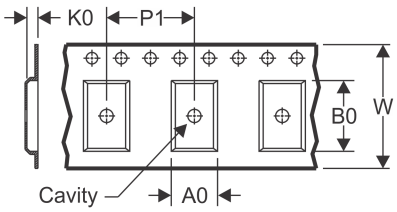
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

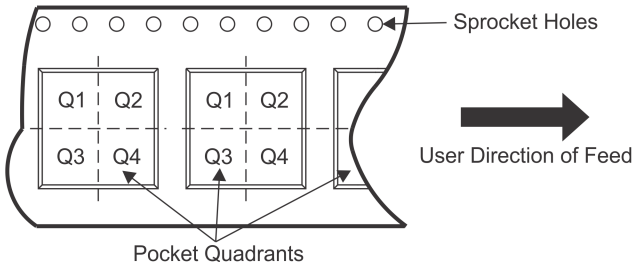


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

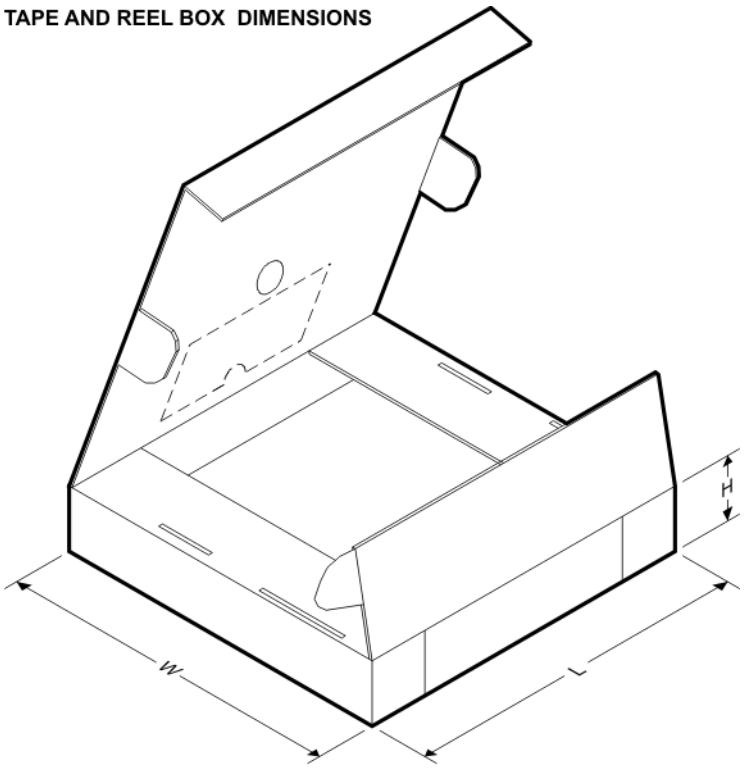
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1271IBPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS1271IPWR	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

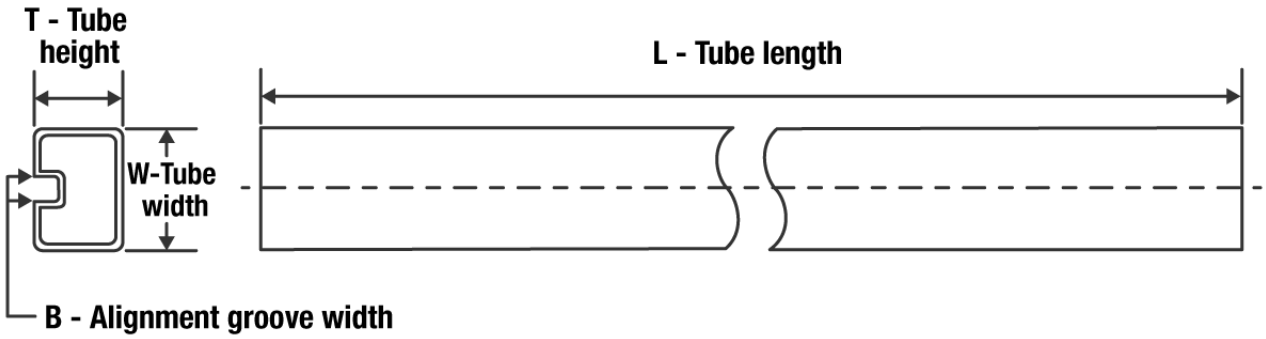
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1271IBPWR	TSSOP	PW	16	2000	350.0	350.0	43.0
ADS1271IPWR	TSSOP	PW	16	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

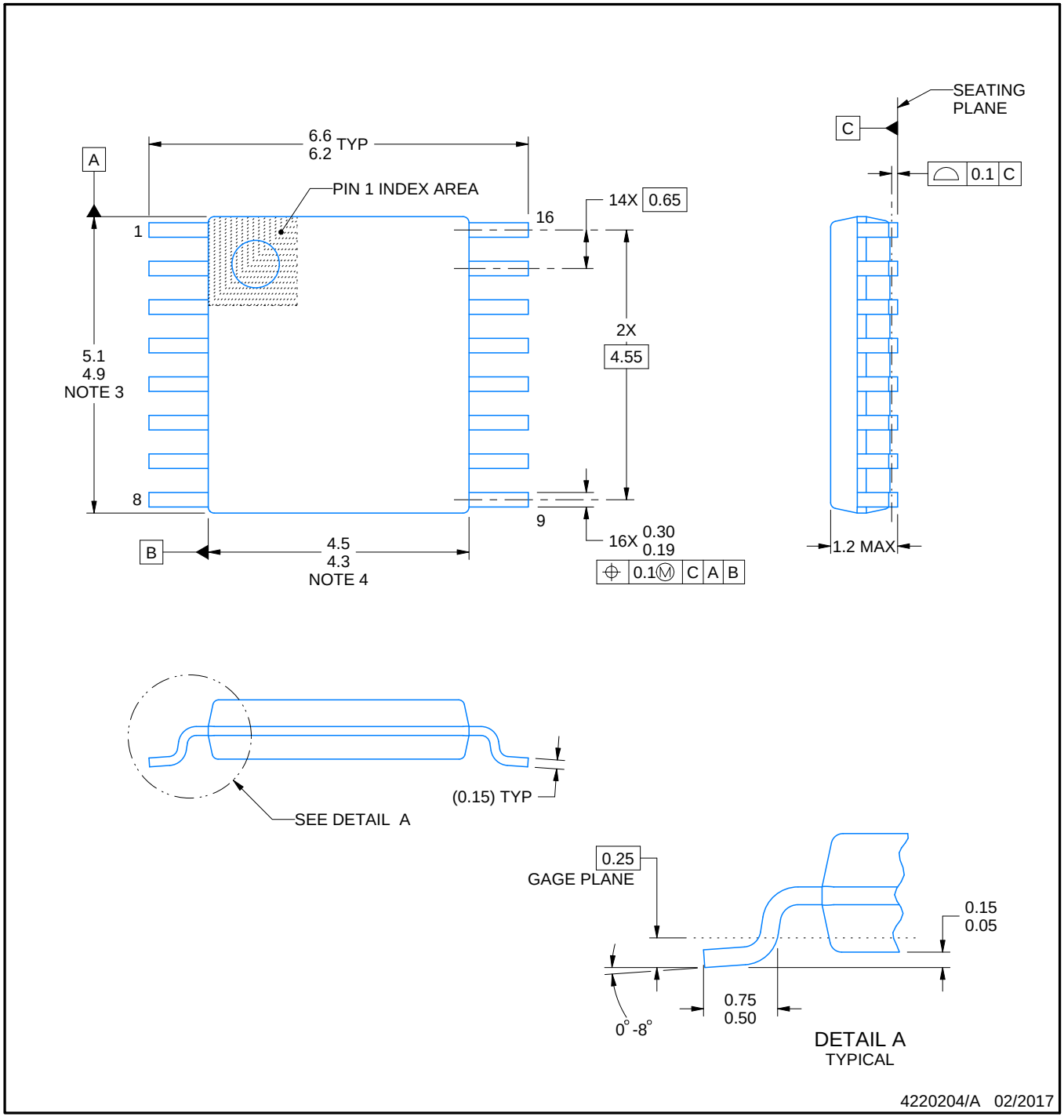
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS1271IBPW	PW	TSSOP	16	90	530	10.2	3600	3.5
ADS1271IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
ADS1271IPWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

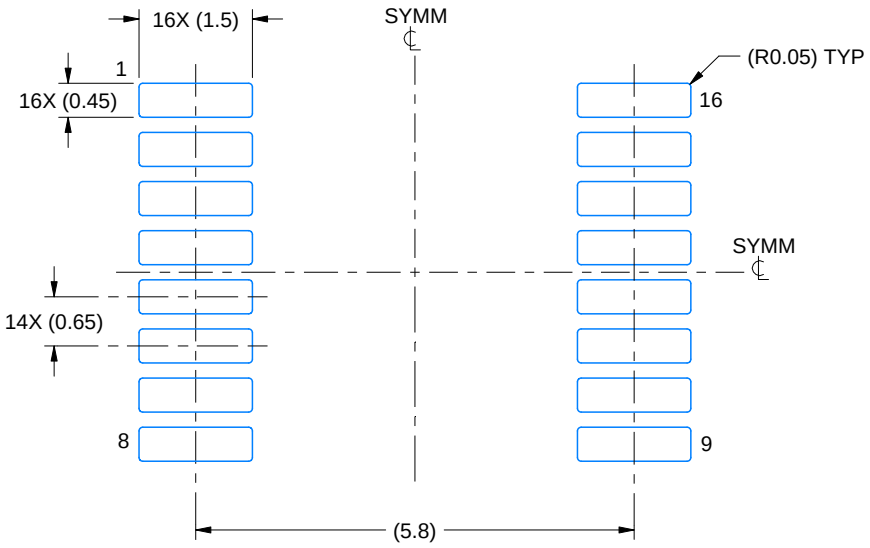
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

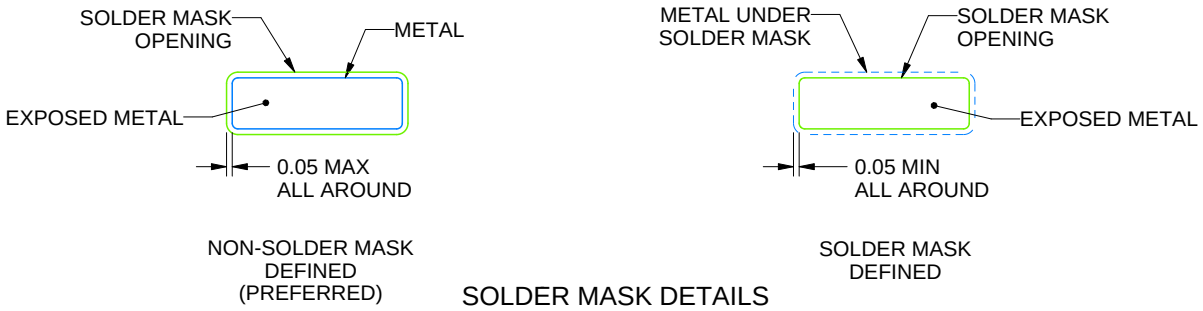


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

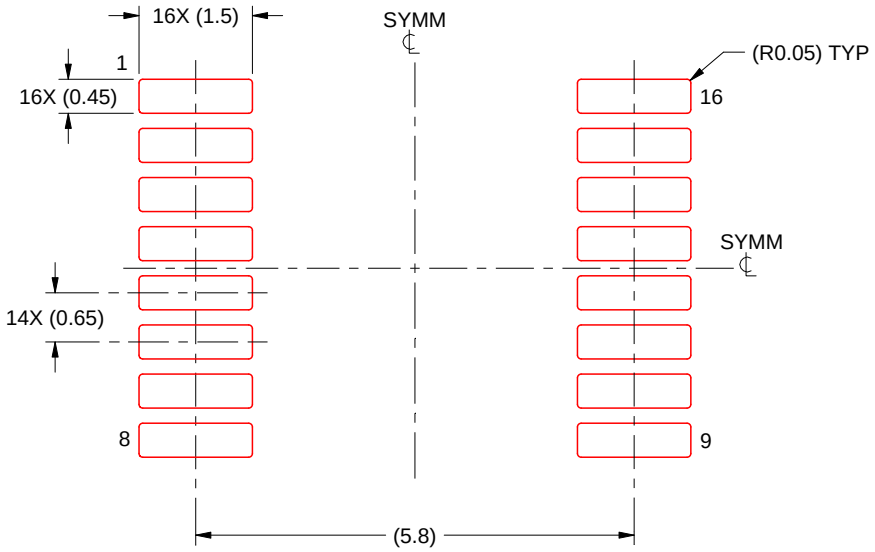


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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