ADS7054 14 位，1 MSPS，差分输入，小型低功耗 SAR ADC

1 特性

- 1 MSPS 吞吐量
- 封装尺寸小：
  - X2QFN-8 封装 (1.5mm × 1.5mm)
- 全差动输入范围：±AVDD
- 宽工作电压范围：
  - AVDD：1.65V 至 3.6V
  - DVDD：1.65V 至 3.6V（与 AVDD 无关）
  - 温度范围：-40°C 至 +125°C
- 性能优异：
  - 14 位 NMC DNL，±0.9-LSB INL
  - 79.5dB SINAD（2kHz 时）
  - 76.2dB SINAD（200kHz 时）
- 低功耗：
  - 1.5mW（1 MSPS，3.3V AVDD 时）
  - 170µW（100kSPS，3.3V AVDD 时）
  - 45µW（100kSPS，1.8V AVDD 时）
- 集成失调电压校准
- 与 SPI 兼容的串行接口：24MHz
- 符合 JESD8-7A 标准的数字 I/O

2 应用

- 光学编码器
- 声纳接收器
- 探鱼器
- I/Q 解调器
- 光线路卡和模块
- 热成像摄像机
- 超声波流量计
- 手持无线电

3 说明

ADS7054 器件属于引脚对引脚兼容的高速低功耗、单通道逐次逼近型寄存器 (SAR) 类型的模数转换器 (ADC) 系列。该器件系列包含多个分辨率、吞吐量和模拟输入型号（有关器件列表，请参阅 表格1）。

ADS7054 是一款 14 位 1 MSPS SAR ADC，支持± AVDD 范围内的全差分输入，AVDD 的范围为1.65V 至 3.6V。

内部失调电压校准功能在整个 AVDD 和工作温度范围内可保持优异的失调电压规格。

该器件支持由 $\overline{CS}$ 和 SCLK 信号控制的兼容 SPI 的串行接口。输入信号通过 $\overline{CS}$ 下降沿进行采样，而 SCLK 用于转换和串行数据输出。该器件支持宽数字电源范围（1.65V 至 3.6V），可直接连接到各种主机控制器。ADS7054 的标称 DVDD 范围（1.65V 至 1.95V）符合 JESD8-7A 标准。

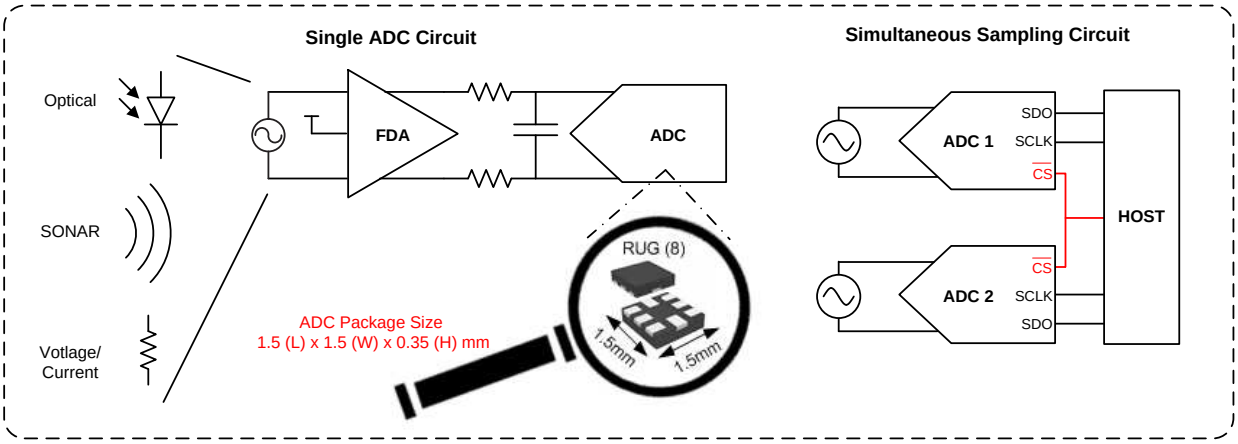
ADS7054 采用 8 引脚小型 X2QFN 封装，可以在广泛的工业温度范围（–40°C 至 +125°C）内正常工作。该器件体积小巧，功耗极低，非常适合需要高速高分辨率数据采集的空间受限型 电池供电 应用。

器件信息(1)

部件名称	封装	封装尺寸（标称值）
ADS7054	X2QFN (8)	1.50mm x 1.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

目录

4 修订历史记录

日期	修订版本	说明
2017 年 12 月	*	初始发行版

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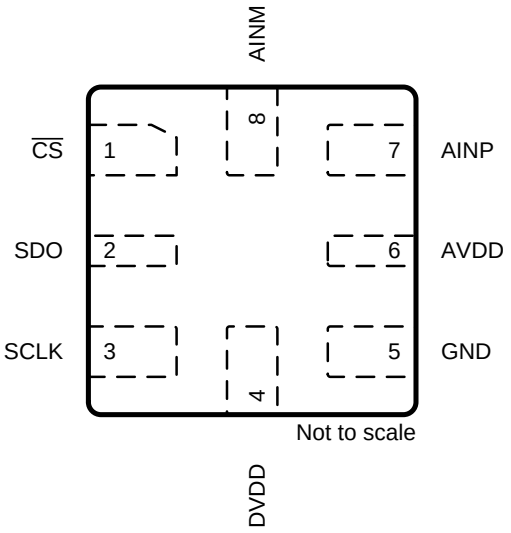
5 Pin Configuration and Functions

RUG Package
8-Pin X2QFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{CS}$	Digital input	Chip-select signal, active low
2	SDO	Digital output	Serial data out
3	SCLK	Digital input	Serial clock
4	DVDD	Supply	Digital I/O supply voltage
5	GND	Supply	Ground for power supply, all analog and digital signals are referred to this pin
6	AVDD	Supply	Analog power-supply input, also provides the reference voltage to the ADC
7	AINP	Analog input	Analog signal input, positive
8	AINM	Analog input	Analog signal input, negative

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6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
AVDD to GND	–0.3	3.9	V
DVDD to GND	–0.3	3.9	V
AINP to GND	–0.3	AVDD + 0.3	V
AINM to GND	–0.3	AVDD + 0.3	V
Input current to any pin except supply pins	–10	10	mA
Digital input voltage to GND	–0.3	DVDD + 0.3	V
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage range	1.65	3.3	3.6	V
DVDD	Digital supply voltage range	1.65	1.8	3.6	V
T_A	Operating free-air temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		ADS7054 RUG (X2QFN) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	177.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

at AVDD = 3.3 V, DVDD = 1.65 V to 3.6 V, f_{sample} = 1 MSPS, and V_{CM} = 1.65 V (unless otherwise noted); minimum and maximum values for T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input voltage span(1)		–AVDD		AVDD	V
	Absolute input voltage range	AINP to GND	–0.1		AVDD + 0.1	V
		AINM to GND	–0.1		AVDD + 0.1	
	Common-mode voltage	(AINP + AINM) / 2	(AVDD / 2) – 0.1		(AVDD / 2) + 0.1	V
C_S	Sampling capacitance			16		pF
SYSTEM PERFORMANCE						
	Resolution			14		Bits
NMC	No missing codes		14			Bits
INL(2)	Integral nonlinearity		–3	±0.9	3	LSB(3)
DNL	Differential nonlinearity		–0.99	±0.5	1	LSB
E_O(2)	Offset error	After calibration(4)	–6	±1	6	LSB
dV_{OS}/dT	Offset error drift with temperature			1.75		ppm/°C
E_G(2)	Gain error		–0.1	±0.01	0.1	%FS
	Gain error drift with temperature			0.5		ppm/°C
SAMPLING DYNAMICS						
t_{CONV}	Conversion time			18 × t_{SCLK}		ns
t_{ACQ}	Acquisition time		230			ns
f_{SAMPLE}	Maximum throughput rate	24-MHz SCLK, AVDD = 1.65 V to 3.6 V			1	MHz
	Aperture delay			3		ns
	Aperture jitter, RMS			12		ps
DYNAMIC CHARACTERISTICS						
SNR	Signal-to-noise ratio(5)	AVDD = 3.3 V, f_{IN} = 2 kHz	76	79.6		dB
		AVDD = 2.5 V, f_{IN} = 2 kHz		78.5		
THD	Total harmonic distortion(5)(6)	f_{IN} = 2 kHz		–92		dB
		f_{IN} = 100 kHz		–90.8		
		f_{IN} = 200 kHz		–90		
SINAD	Signal-to-noise and distortion(5)	f_{IN} = 2 kHz	76	79.4		dB
		f_{IN} = 100 kHz		78.7		
		f_{IN} = 200 kHz		78.5		
SFDR	Spurious-free dynamic range(5)	f_{IN} = 2 kHz		92		dB
		f_{IN} = 100 kHz		91.7		
		f_{IN} = 200 kHz		90		
$BW_{(fp)}$	Full-power bandwidth	At –3 dB		200		MHz

(1) Ideal input span; does not include gain or offset error.
(2) See Figure 31, Figure 29, and Figure 30 for statistical distribution data for INL, offset error, and gain error.
(3) LSB means least significant bit.
(4) See the *OFFCAL State* section for details.
(5) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise noted.
(6) Calculated on the first nine harmonics of the input frequency.

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Electrical Characteristics (continued)

at AVDD = 3.3 V, DVDD = 1.65 V to 3.6 V, f_{sample} = 1 MSPS, and V_{CM} = 1.65 V (unless otherwise noted); minimum and maximum values for T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT (CMOS Logic Family)						
V_{IH}	High-level input voltage(7)		0.65 DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage(7)		–0.3		0.35 DVDD	V
V_{OH}	High-level output voltage(7)	At I_{source} = 500 µA	0.8 DVDD		DVDD	V
		At I_{source} = 2 mA	DVDD – 0.45		DVDD	
V_{OL}	Low-level output voltage(7)	At I_{sink} = 500 µA	0		0.2 DVDD	V
		At I_{sink} = 2 mA	0		0.45	
POWER-SUPPLY REQUIREMENTS						
AVDD	Analog supply voltage		1.65	3	3.6	V
DVDD	Digital I/O supply voltage		1.65	3	3.6	V
I_{AVDD}	Analog supply current	AVDD = 3.3 V, f_{SAMPLE} = 1 MSPS		450	560	µA
		AVDD = 3.3 V, f_{SAMPLE} = 100 kSPS		47	55	
		AVDD = 3.3 V, f_{SAMPLE} = 10 kSPS		5		
		AVDD = 1.8 V, f_{SAMPLE} = 1 MSPS		230		
		Static current with $\overline{CS}$ and SCLK high		0.02		
I_{DVDD}	Digital supply current	DVDD = 1.8 V, CSDO = 20 pF, output code = 2AAAh(8)		250		µA
		DVDD = 1.8 V, static current with $\overline{CS}$ and SCLK high		0.01		

(7) Digital voltage levels comply with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V; see the *Parameter Measurement Information* section for details.
(8) See the *Estimating Digital Power Consumption* section for details.

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6.6 Timing Requirements

all specifications are at AVDD = 1.65 V to 3.6 V, DVDD = 1.65 V to 3.6 V, and $C_{LOAD-SDO}$ = 20 pF (unless otherwise noted); minimum and maximum values for T_A = –40°C to +125°C; typical values at T_A = 25°C

		MIN	TYP	MAX	UNIT
t_{CLK}	Time period of SCLK	41.66			ns
t_{su_CSCK}	Setup time: $\overline{CS}$ falling edge to SCLK falling edge	7			ns
t_{ht_CKCS}	Hold time: SCLK rising edge to $\overline{CS}$ rising edge	8			ns
t_{ph_CK}	SCLK high time	0.45		0.55	t_{SCLK}
t_{pl_CK}	SCLK low time	0.45		0.55	t_{SCLK}
t_{ph_CS}	$\overline{CS}$ high time	15			ns

6.7 Switching Characteristics

all specifications are at AVDD = 1.65 V to 3.6 V, DVDD = 1.65 V to 3.6 V, and $C_{LOAD-SDO}$ = 20 pF (unless otherwise noted); minimum and maximum values for T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CYCLE} (1)	Cycle time		1000			ns
t_{CONV}	Conversion time			18 × t_{SCLK}		ns
t_{den_CSDO}	Delay time: $\overline{CS}$ falling edge to data enable				6.5	ns
t_{d_CKDO}	Delay time: SCLK rising edge to (next) data valid on SDO				10	ns
t_{ht_CKDO}	SCLK rising edge to current data invalid		2.5			ns
t_{dz_CSDO}	Delay time: $\overline{CS}$ rising edge to SDO going to tri-state		5.5			ns

(1) $t_{CYCLE} = 1 / f_{SAMPLE}$.

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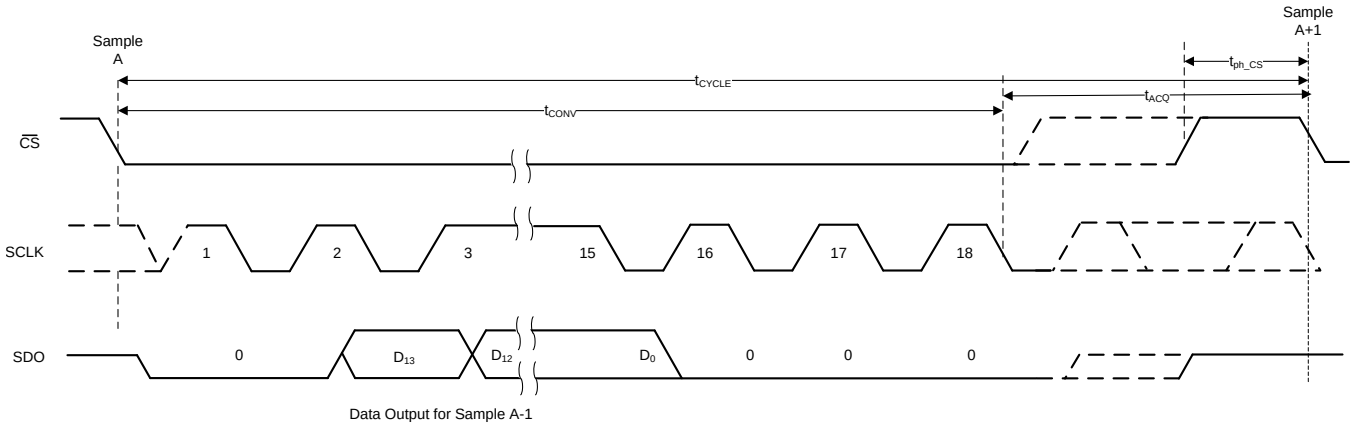

Figure 1. Serial Transfer Frame

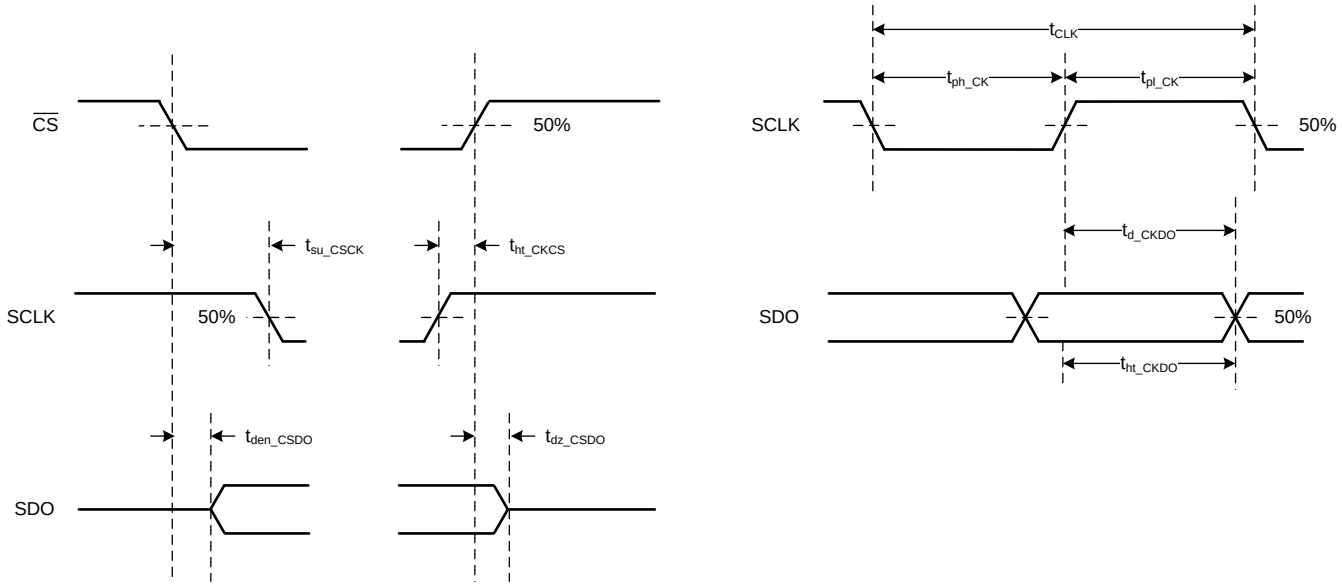

Figure 2. Timing Specifications

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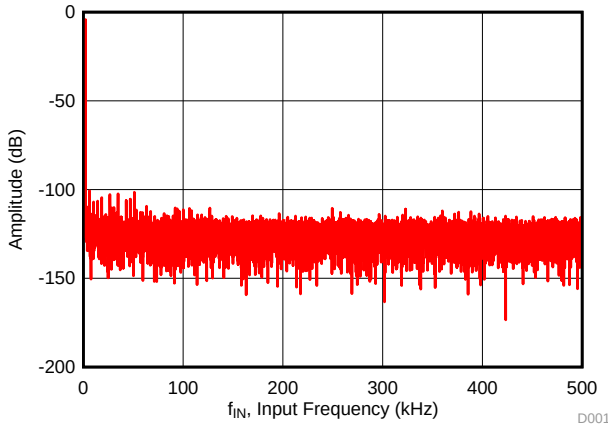
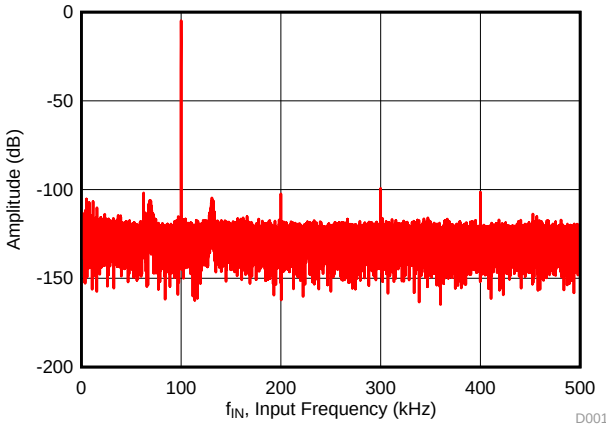
6.8 Typical Characteristics

at T_A = 25°C, AVDD = 3.3 V, DVDD = 1.8 V, f_{IN} = 2 kHz, and f_{sample} = 1 MSPS (unless otherwise noted)



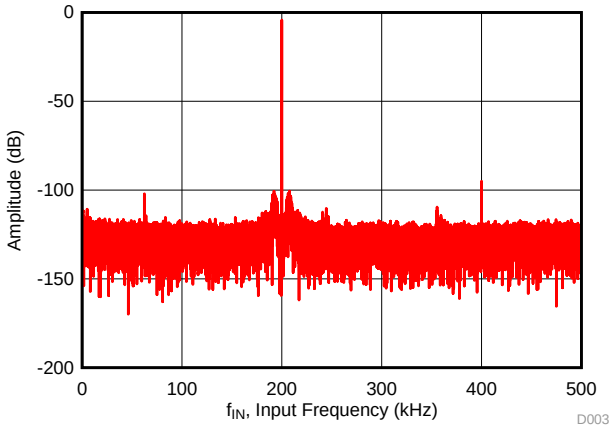
SNR = 80.6 dB, THD = –91.6 dB, ENOB = 13.0 bits

Figure 3. Typical FFT



SNR = 78.5 dB, THD = –89.5 dB, f_{IN} = 100 kHz

Figure 4. Typical FFT



SNR = 76.6dB, THD = –90.6 dB, f_{IN} = 200 kHz

Figure 5. Typical FFT

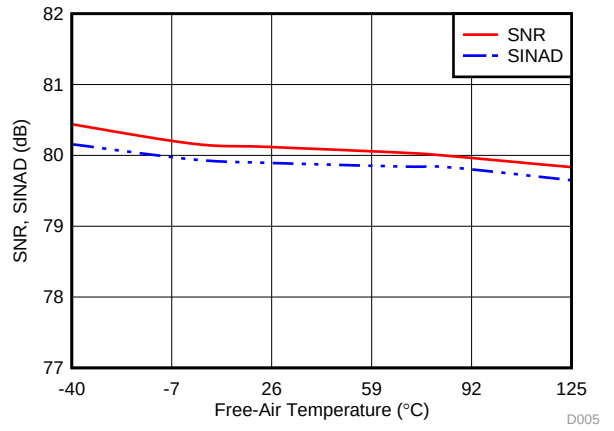


Figure 6. SNR and SINAD vs Temperature

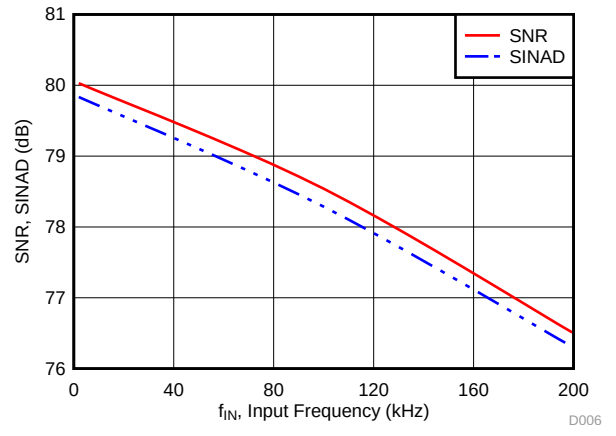


Figure 7. SNR and SINAD vs Input Frequency

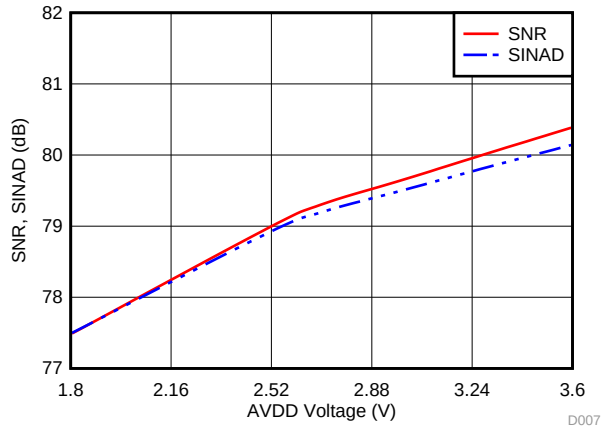


Figure 8. SNR and SINAD vs Reference Voltage (AVDD)

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, DVDD = 1.8 V, f_{IN} = 2 kHz, and f_{sample} = 1 MSPS (unless otherwise noted)

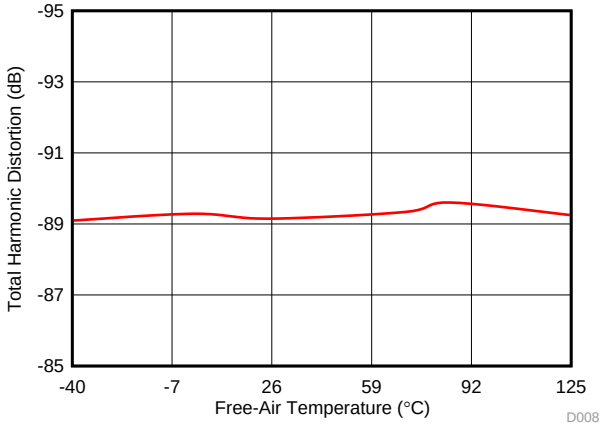

Figure 9. THD vs Temperature

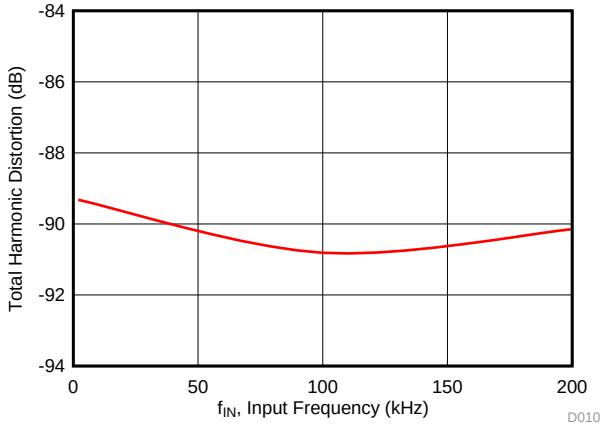

Figure 10. THD vs Input Frequency

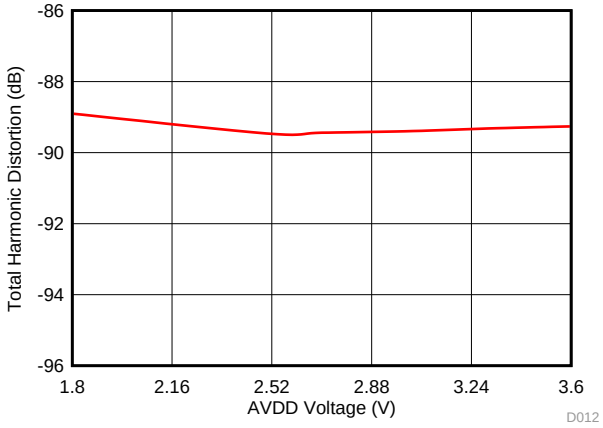

Figure 11. THD vs Reference Voltage (AVDD)

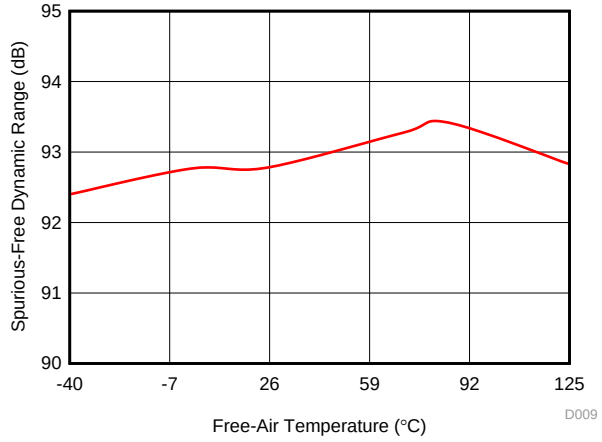

Figure 12. SFDR vs Temperature

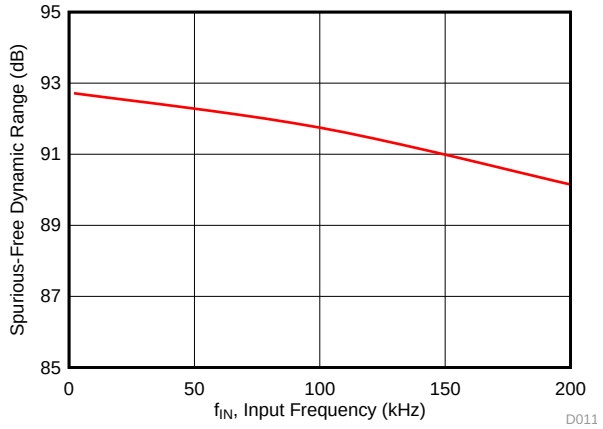

Figure 13. SFDR vs Input Frequency

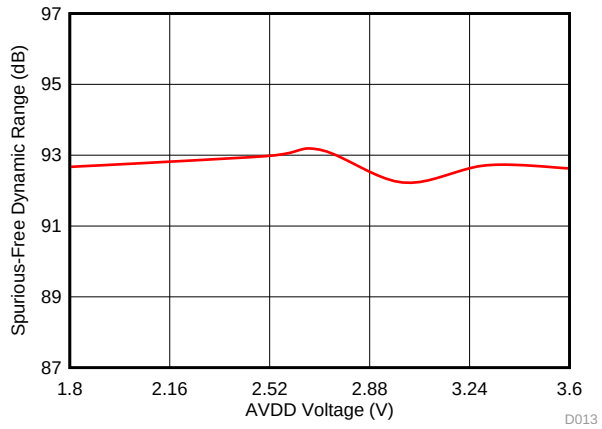

Figure 14. SFDR vs Reference Voltage (AVDD)

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, DVDD = 1.8 V, f_{IN} = 2 kHz, and f_{sample} = 1 MSPS (unless otherwise noted)

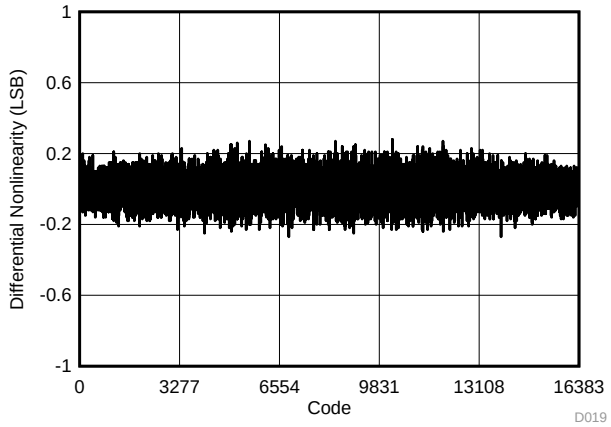

Figure 15. Typical DNL

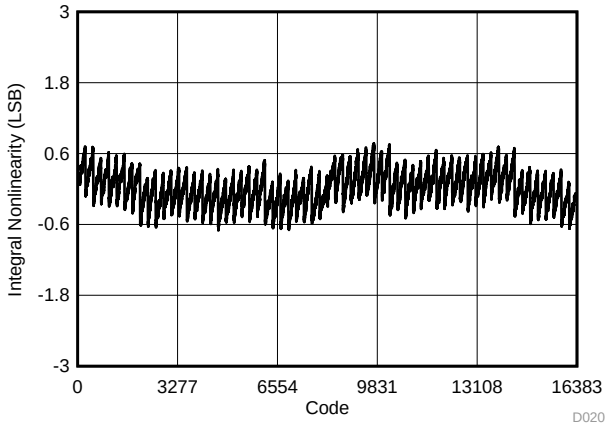

Figure 16. Typical INL

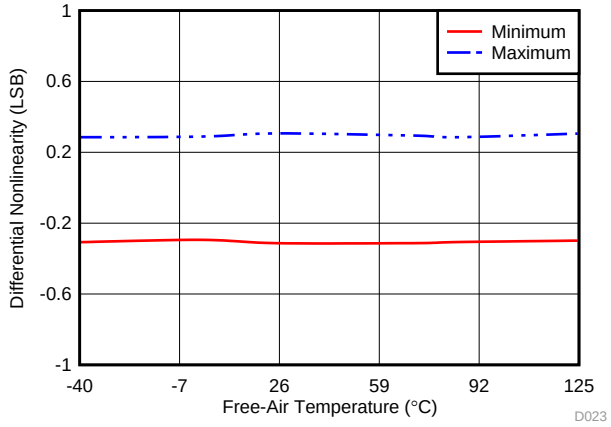

Figure 17. DNL vs Temperature

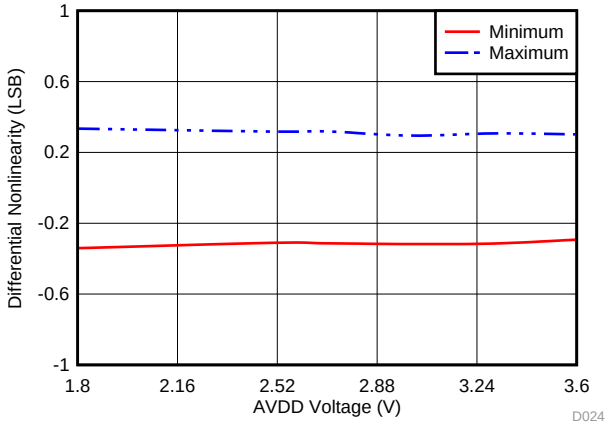

Figure 18. DNL vs Reference Voltage

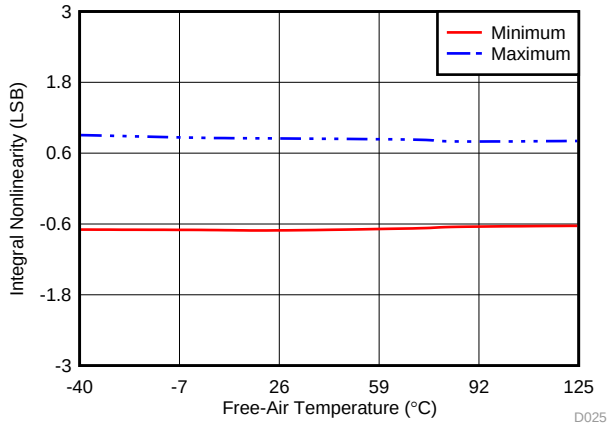

Figure 19. INL vs Temperature

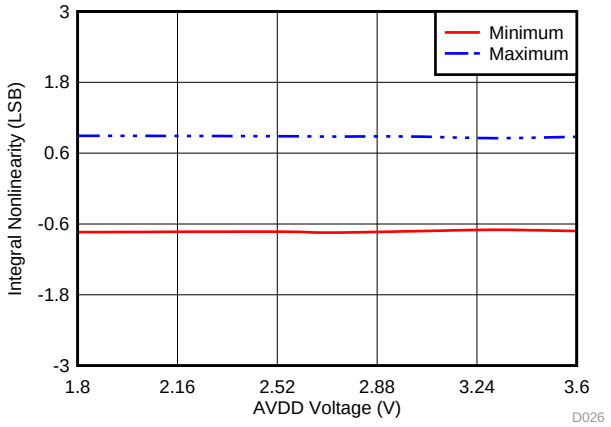

Figure 20. INL vs Reference Voltage

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, DVDD = 1.8 V, f_{IN} = 2 kHz, and f_{sample} = 1 MSPS (unless otherwise noted)

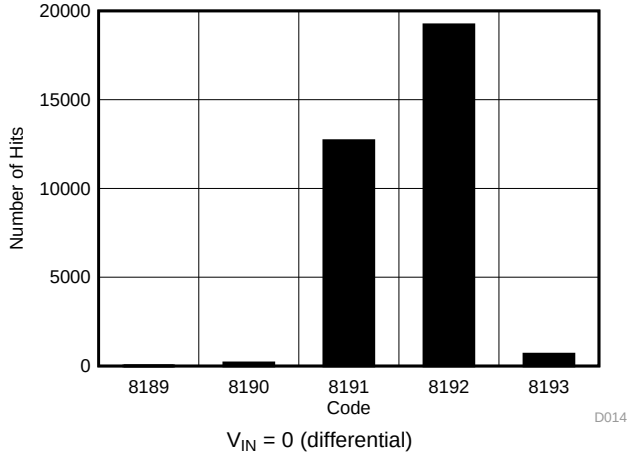

Figure 21. DC Input Histogram

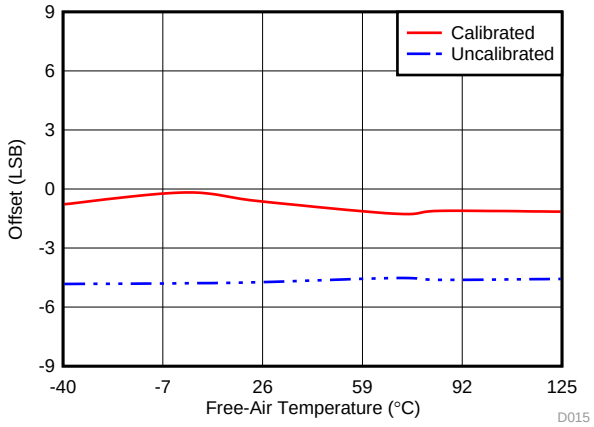

Figure 22. Offset vs Temperature

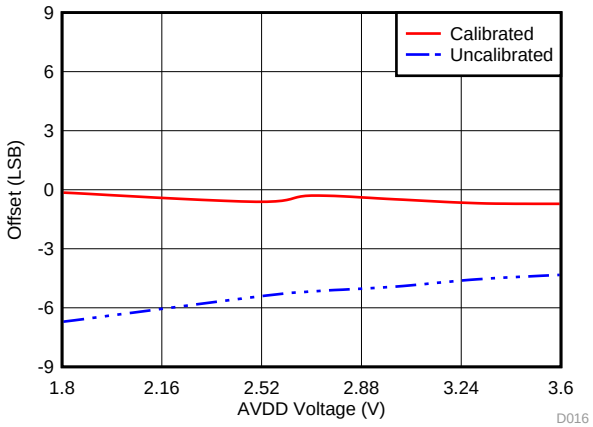

Figure 23. Offset vs Reference Voltage (AVDD)

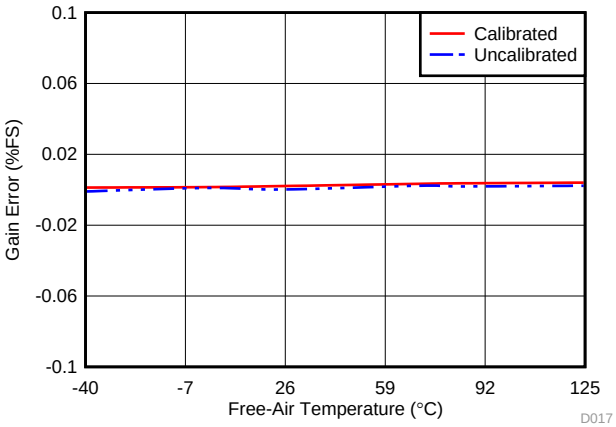

Figure 24. Gain Error vs Temperature

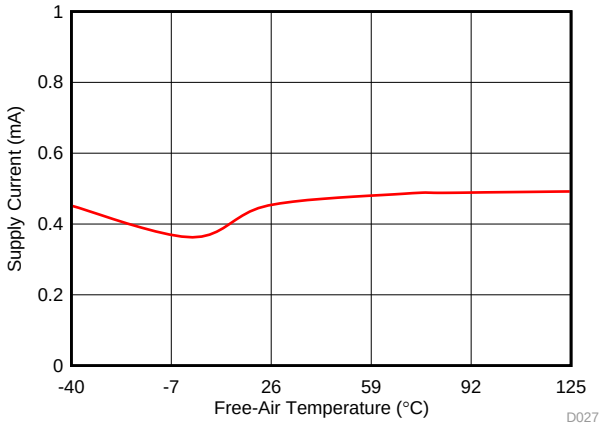

Figure 25. AVDD Current vs Temperature

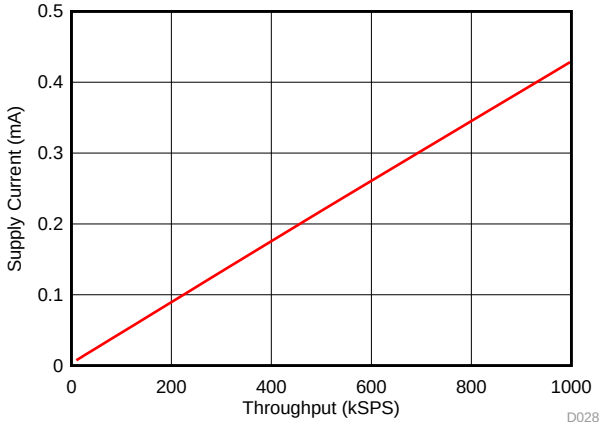

Figure 26. AVDD Current vs Throughput

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, DVDD = 1.8 V, f_{IN} = 2 kHz, and f_{sample} = 1 MSPS (unless otherwise noted)

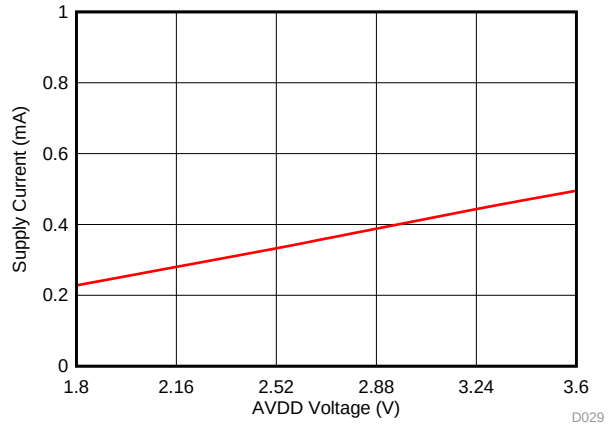

Figure 27. AVDD Current vs AVDD Voltage

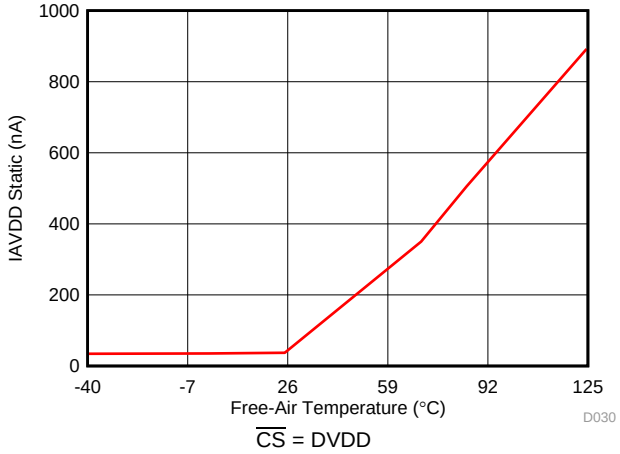

Figure 28. Static AVDD Current vs Temperature

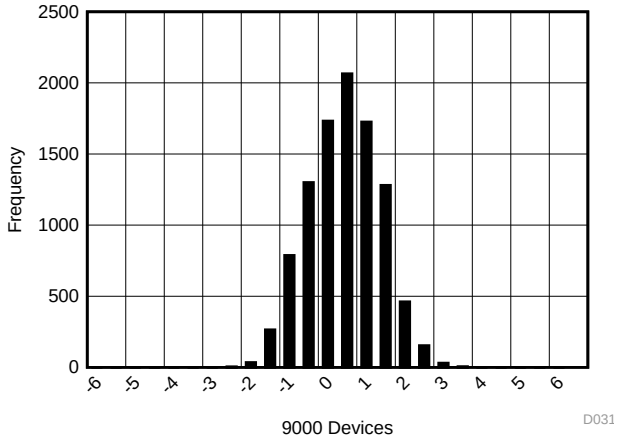

Figure 29. Typical Offset Error Distribution

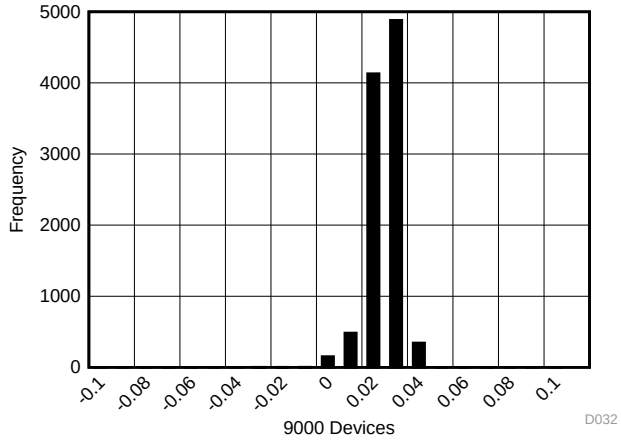

Figure 30. Typical Gain Error Distribution

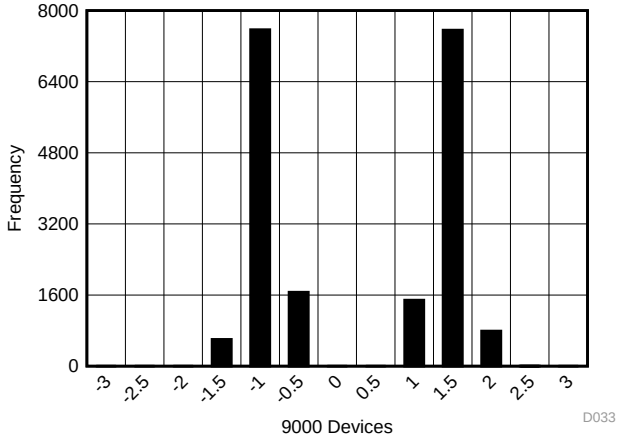

Figure 31. Typical INL Distribution

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7 Parameter Measurement Information

7.1 Digital Voltage Levels

The device complies with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V. Figure 32 shows voltage levels for the digital input and output pins.

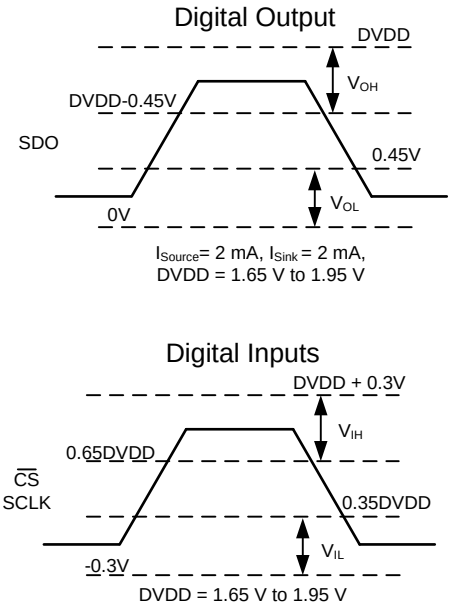

Figure 32. Digital Voltage Levels as per the JESD8-7A Standard

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8 Detailed Description

8.1 Overview

The ADS7054 device belongs to a family of pin-to-pin compatible, high-speed, low-power, single-channel successive-approximation register (SAR) type analog-to-digital converters (ADCs). The device family includes multiple resolutions, throughputs, and analog input variants (see Table 1 for a list of devices).

The ADS7054 is a 14-bit, 1-MSPS SAR ADC that supports fully-differential inputs in the range of ±AVDD, for AVDD in the range of 1.65 V to 3.6 V (see the *Analog Input* section for details on the analog input pins).

The internal offset calibration feature (see the *OFFCAL State* section) maintains excellent offset specifications over the entire AVDD and temperature operating range.

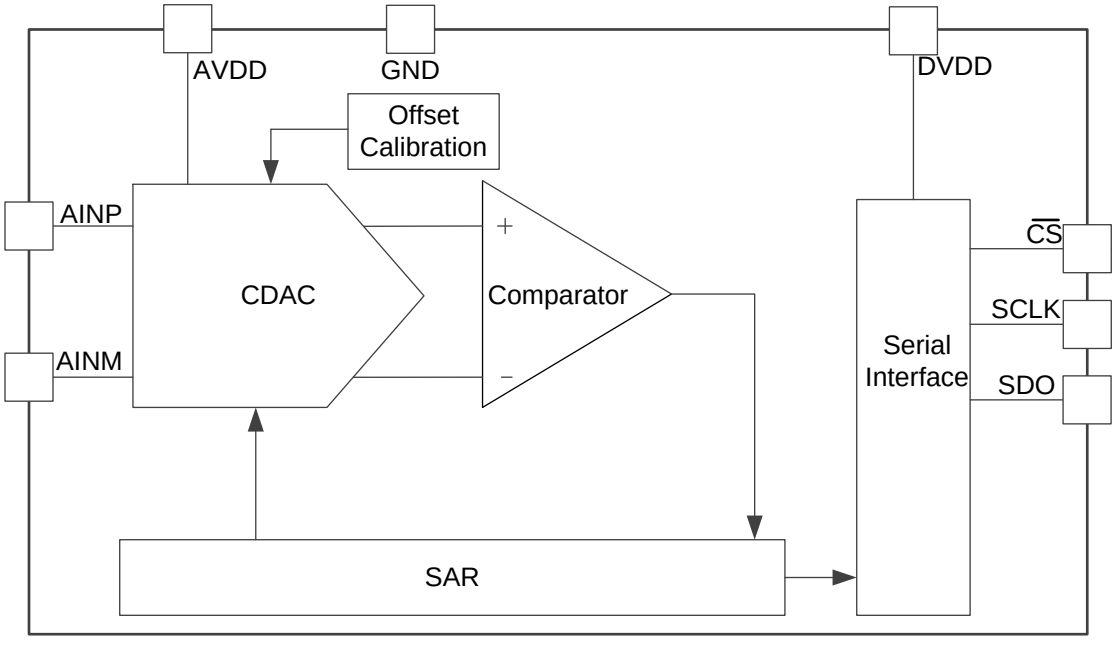
The device supports an SPI-compatible serial interface that is controlled by the $\overline{CS}$ and SCLK signals. The input signal is sampled with the $\overline{CS}$ falling edge and SCLK is used for both, conversion and serial data output (see the *Device Functional Modes* section, *Timing Requirements* table, and *Switching Characteristics* table).

The device supports a wide digital supply range (1.65 V to 3.6 V), enabling direct interfacing to a variety of host controllers. The ADS7054 complies with the JESD8-7A standard (see the *Digital Voltage Levels* section) for a normal DVDD range (1.65 V to 1.95 V).

The ADS7054 is available in an 8-pin, small, X2QFN package (see the *机械、封装和可订购信息* section for more details) and is specified over the extended industrial temperature range (–40°C to +125°C).

The small form-factor and extremely-low power consumption make this device suitable for space-constrained and battery-powered applications that require high-speed, high-resolution data acquisition (see the *Application Information* section).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Product Family

The devices listed in Table 1 are all part of the same pin-to-pin compatible, high-speed, low-power, single-channel SAR ADC family. This device family includes multiple different ADC resolutions, throughputs, and analog input types to allow for greater flexibility in the end system. Devices in the same package are pin-compatible to offer a scalable family of devices for varying levels of end-system performance. The ADCs with device numbers ending in *-Q1* are also AEC-Q100 qualified for automotive applications.

Table 1. Device Family Comparison

DEVICE NUMBER	RESOLUTION (Bits)	THROUGHPUT (MSPS)	INPUT TYPE	PACKAGES(1)
ADS7040	8	1	Single-ended	X2QFN (8): 1.5 mm × 1.5 mm VSSOP (8): 2.0 mm × 3.1 mm
ADS7041	10	1	Single-ended	X2QFN (8): 1.5 mm × 1.5 mm VSSOP (8): 2.0 mm × 3.1 mm
ADS7042	12	1	Single-ended	X2QFN (8): 1.5 mm × 1.5 mm VSSOP (8): 2.0 mm × 3.1 mm
ADS7043	12	1	Pseudo-differential	X2QFN (8): 1.5 mm × 1.5 mm VSSOP (8): 2.0 mm × 3.1 mm
ADS7044	12	1	Fully-differential	X2QFN (8): 1.5 mm × 1.5 mm VSSOP (8): 2.0 mm × 3.1 mm
ADS7029-Q1	8	2	Single-ended	VSSOP (8): 2.0 mm × 3.1 mm
ADS7039-Q1	10	2	Single-ended	VSSOP (8): 2.0 mm × 3.1 mm
ADS7049-Q1	12	2	Single-ended	VSSOP (8): 2.0 mm × 3.1 mm
ADS7046	12	3	Single-ended	X2QFN (8): 1.5 mm × 1.5 mm
ADS7047	12	3	Fully-differential	X2QFN (8): 1.5 mm × 1.5 mm
ADS7052	14	1	Single-ended	X2QFN (8): 1.5 mm × 1.5 mm
ADS7054	14	1	Fully-differential	X2QFN (8): 1.5 mm × 1.5 mm
ADS7056	14	2.5	Single-ended	X2QFN (8): 1.5 mm × 1.5 mm
ADS7057	14	2.5	Fully-differential	X2QFN (8): 1.5 mm × 1.5 mm

(1) Devices listed in the same package are pin-compatible.

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8.3.2 Analog Input

The device supports a unipolar, fully-differential analog input signal. Figure 33 shows a small-signal equivalent circuit of the sample-and-hold circuit. The sampling switch is represented by a resistance (R_{S1} and R_{S2}, typically 50 Ω) in series with an ideal switch (SW_1 and SW_2). The sampling capacitors, C_{S1} and C_{S2}, are typically 16 pF.

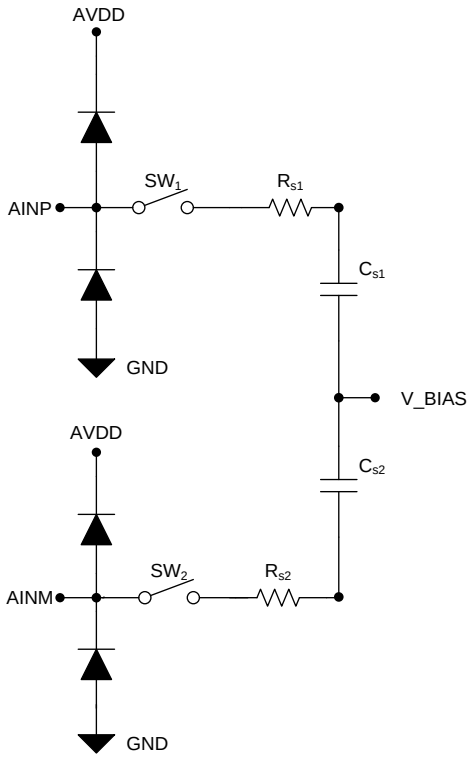

Figure 33. Equivalent Input Circuit for the Sampling Stage

During the acquisition process, both positive and negative inputs are individually sampled on C_{S1} and C_{S2}, respectively. During the conversion process, the device converts for the voltage difference between the two sampled values: $V_{AINP} – V_{AINM}$.

Each analog input pin has electrostatic discharge (ESD) protection diodes to AVDD and GND. Keep the analog inputs within the specified range to avoid turning the diodes on.

The full-scale analog input range (FSR) is V_{FSR} = –AVDD to AVDD and the common-mode input voltage is AVDD / 2 ± 0.1 V.

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8.3.3 Reference

The device uses the analog supply voltage (AVDD) as the reference voltage for the analog to digital conversion. During the conversion process, the internal capacitors are switched to the AVDD pin as per the successive approximation algorithm. A voltage reference must be selected with low temperature drift, high output current drive and low output impedance. TI recommends a 3.3-µF (C_{AVDD}), low equivalent series resistance (ESR) ceramic capacitor between the AVDD and GND pins. This decoupling capacitor provides the instantaneous charge required by the internal circuit during the conversion process and maintains a stable dc voltage on the AVDD pin.

See the *Power Supply Recommendations* and *Layout Example* sections for component recommendations and layout guidelines.

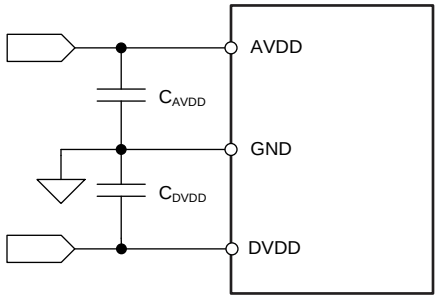

Figure 34. Reference for the Device

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8.3.4 ADC Transfer Function

The device supports a unipolar fully-differential analog input signal. The output is in two's compliment format. Figure 35 and Table 2 show the ideal transfer characteristics for the device.

The least significant bit for the device is given by:

$$1\ LSB = 2 \times V_{REF} / 2^{N} \quad (1)$$

where:

- V_{REF} = Voltage applied between the AVDD and GND pins
- N = 14

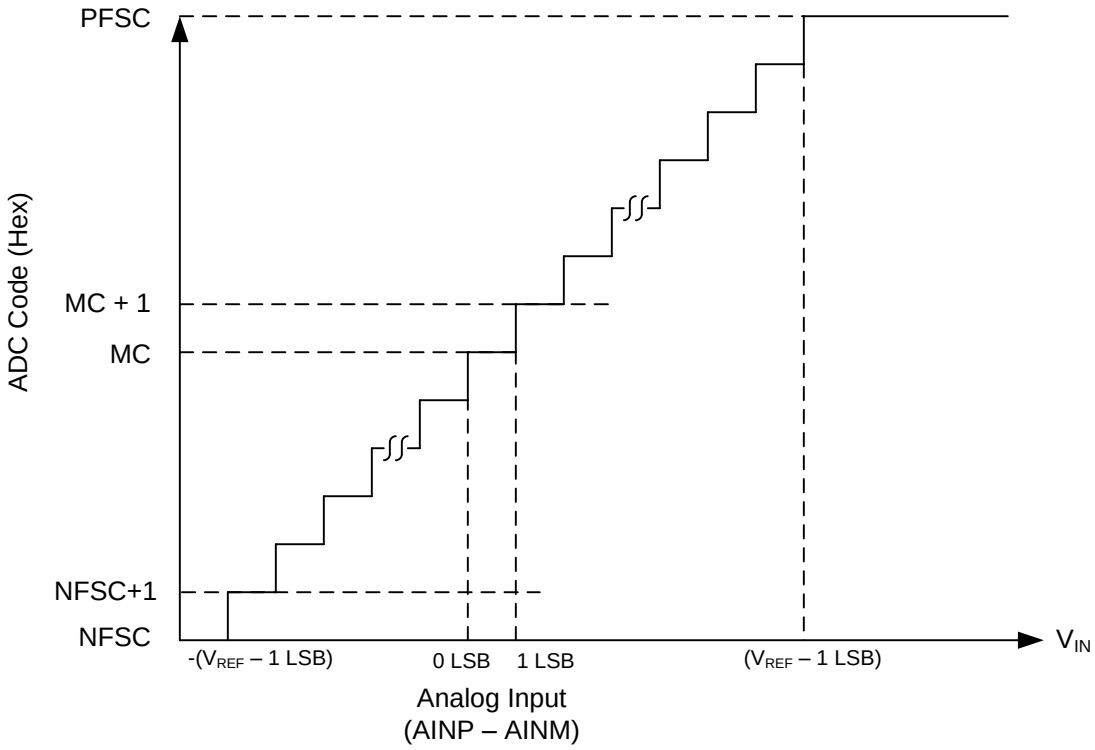

Figure 35. Ideal Transfer Characteristics

Table 2. Transfer Characteristics

INPUT VOLTAGE (AINP – AINM)	CODE	DESCRIPTION	IDEAL OUTPUT CODE (Hex)
≤ –(V_{REF} – 1 LSB)	NFSC	Negative full-scale code	2000
–(V_{REF} – 1 LSB) to –(V_{REF} – 2 LSB)	NFSC + 1	—	2001
0 LSB to 1 LSB	MC	Mid code	0000
1 LSB to 2 LSB	MC + 1	—	0001
≥ V_{REF} – 1 LSB	PFSC	Positive full-scale code	1FFF

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8.4 Device Functional Modes

The device supports a simple, SPI-compatible interface to the external host. On power-up, the device is in the ACQ state. The $\overline{CS}$ signal defines one conversion and serial data transfer frame. A frame starts with a $\overline{CS}$ falling edge and ends with a $\overline{CS}$ rising edge. The SDO pin is tri-stated when $\overline{CS}$ is high. With $\overline{CS}$ low, the clock provided on the SCLK pin is used for conversion and data transfer. Output data are available on the SDO pin.

As shown in Figure 36, the device supports three functional states: acquisition (ACQ), conversion (CNV), and offset calibration (OFFCAL). The device status depends on the $\overline{CS}$ and SCLK signals provided by the host controller.

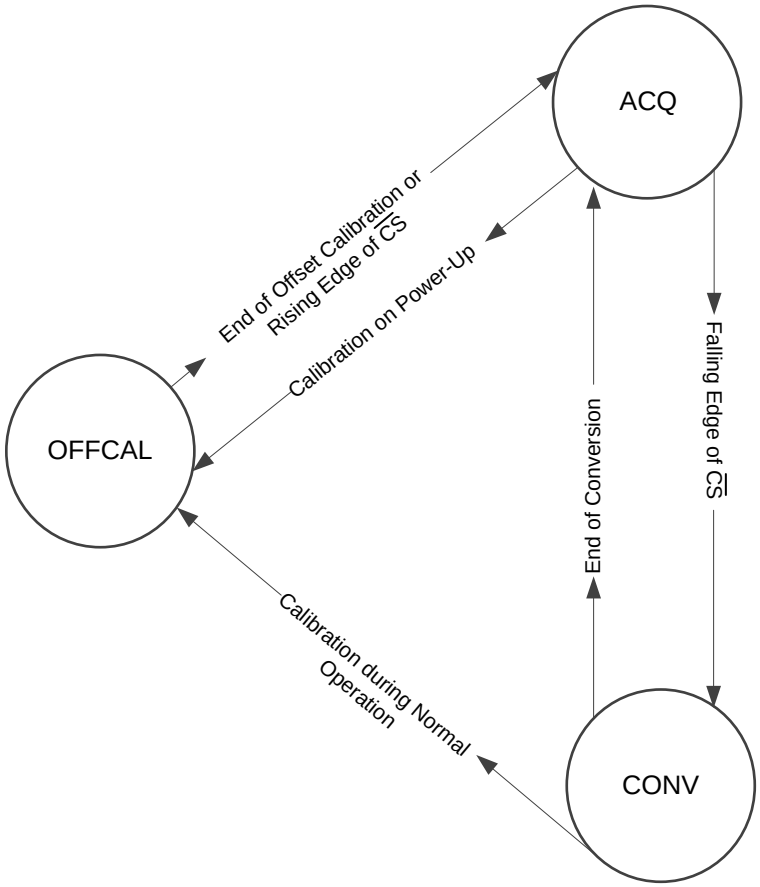

Figure 36. Functional State Diagram

8.4.1 ACQ State

In the ACQ state, switches SW_1 and SW_2 connected to the analog input pins close and the device acquires the analog input signal on C_{S1} and C_{S2}. The device enters ACQ state at power-up, at the end of every conversion, and after completing the offset calibration. A $\overline{CS}$ falling edge takes the device from the ACQ state to the CNV state.

The device consumes extremely low power from the AVDD and DVDD power supplies when in ACQ state.

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Device Functional Modes (continued)

8.4.2 CNV State

In the CNV state, the device uses the external clock to convert the sampled analog input signal to an equivalent digital code as per the transfer function illustrated in Figure 35. The conversion process requires a minimum of 18 SCLK falling edges to be provided within the frame. After the end of conversion process, the device automatically moves from the CNV state to the ACQ state. For acquisition of the next sample, a minimum time of t_{ACQ} must be provided.

Figure 37 shows a detailed timing diagram for the serial interface. In the first serial transfer frame after power-up, the device provides the first data as all zeros. In any frame, the clocks provided on the SCLK pin are also used to transfer the output data for the previous conversion. A leading 0 is output on the SDO pin on the $\overline{CS}$ falling edge. The most significant bit (MSB) of the output data is launched on the SDO pin on the rising edge after the first SCLK falling edge. Subsequent output bits are launched on the subsequent rising edges provided on SCLK. When all 14 output bits are shifted out, the device outputs 0's on the subsequent SCLK rising edges. The device enters the ACQ state after 18 clocks and a minimum time of t_{ACQ} must be provided for acquiring the next sample. If the device is provided with less than 18 SCLK falling edges in the present serial transfer frame, the device provides an invalid conversion result in the next serial transfer frame.

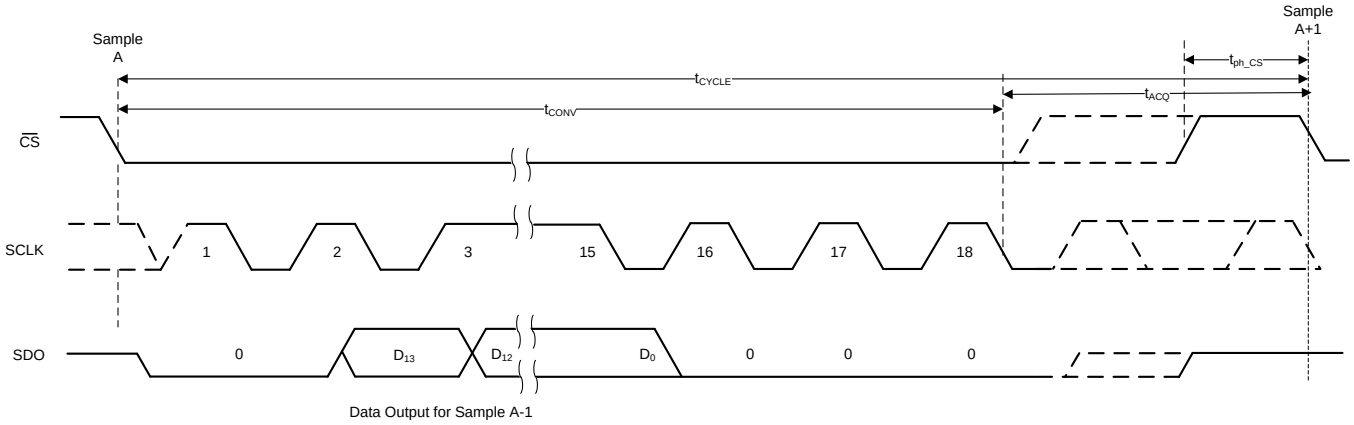

Figure 37. Serial Interface Timing Diagram

Device Functional Modes (continued)

8.4.3 OFFCAL State

In the offset calibration (OFFCAL) state, the sampling capacitors are disconnected from the analog input pins (AINP and AINM) and the device calibrates and corrects for any internal offset errors. The offset calibration is effective for all subsequent conversions until the device is powered off. An offset calibration cycle is recommended at power-up and whenever there is a significant change in the operating conditions for the device (such as in the AVDD voltage and operating temperature).

The host controller must provide a serial transfer frame as described in Figure 38 or in Figure 39 to enter the OFFCAL state.

8.4.3.1 Offset Calibration on Power-Up

On power-up, the host must provide 24 SCLKs in the first serial transfer to enter the OFFCAL state. The device provides 0's on SDO during offset calibration. For acquisition of the next sample, a minimum time of t_{ACQ} must be provided.

If the host controller starts the offset calibration process but then pulls the $\overline{CS}$ pin high before providing 24 SCLKs, then the offset calibration process is aborted and the device enters the ACQ state. Figure 38 and Table 3 provide the timing for offset calibration on power-up.

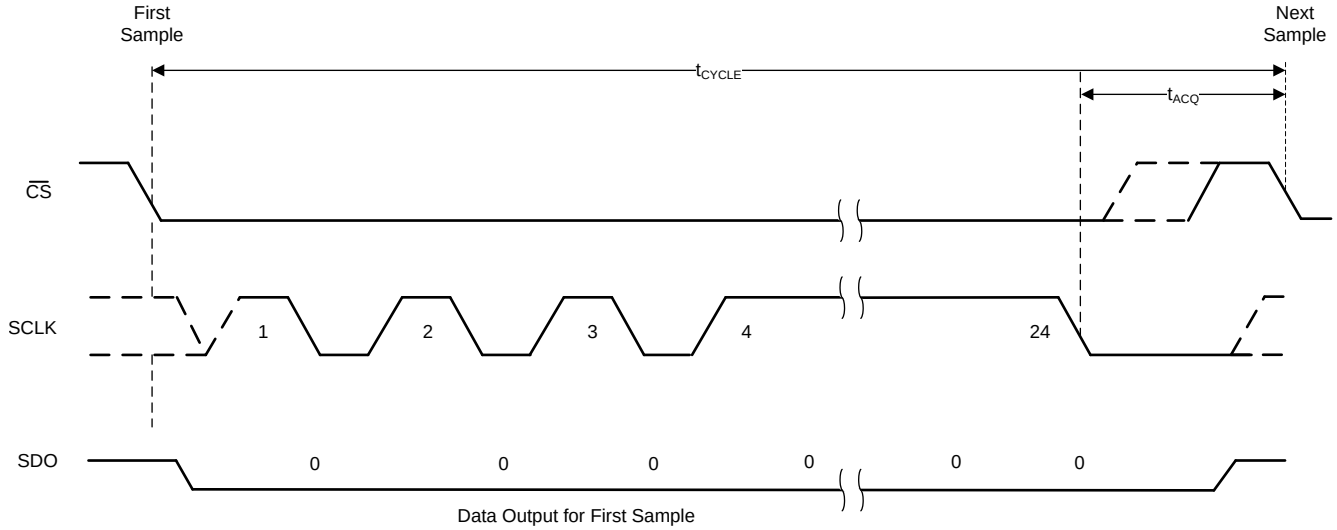

Figure 38. Timing for Offset Calibration on Power-Up

Table 3. Timing Specifications for Offset Calibration on Power-Up(1)

		MIN	TYP	MAX	UNIT
t_{cycle}	Cycle time for offset calibration on power-up	24 × t_{CLK} + t_{ACQ}			ns
t_{ACQ}	Acquisition time	230			ns
f_{SCLK}	Frequency of SCLK			24	MHz

(1) In addition to the timing specifications of Figure 38 and Table 3, the timing specifications described in Figure 2 and the *Timing Requirements* table are also applicable for offset calibration on power-up.

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8.4.3.2 Offset Calibration During Normal Operation

During normal operation, the host must provide 64 SCLKs in the serial transfer frame to enter the OFFCAL state. The device provides the conversion result for the previous sample during the first 18 SCLKs and 0's on SDO for the rest of the SCLKs in the serial transfer frame. For acquisition of the next sample, a minimum time of t_{ACQ} must be provided.

If the host controller provides more than 18 SCLKs but pulls the $\overline{CS}$ high before providing 64 SCLKs, then the offset calibration process is aborted and the device enters the ACQ state. Figure 39 and Table 4 provide the timing for offset calibration during normal operation.

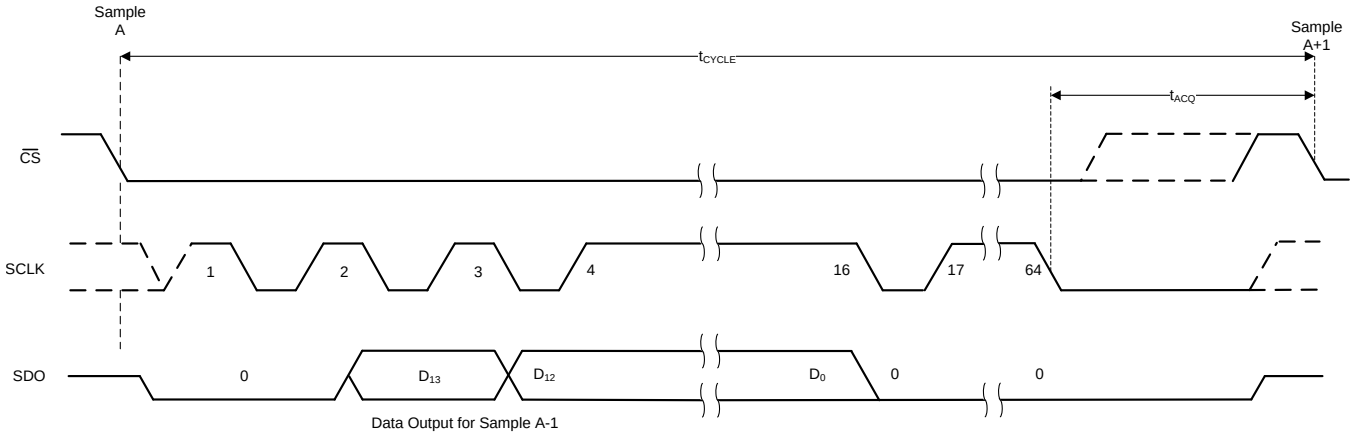

Figure 39. Timing for Offset Calibration During Normal Operation

Table 4. Timing Specifications for Offset Calibration During Normal Operation(1)

		MIN	TYP	MAX	UNIT
t_{cycle}	Cycle time for offset calibration on power-up	64 × t_{CLK} + t_{ACQ}			ns
t_{ACQ}	Acquisition time	230			ns
f_{SCLK}	Frequency of SCLK			24	MHz

(1) In addition to the timing specifications of Figure 39 and Table 4, the timing specifications described in Figure 2 and the *Timing Requirements* table are also applicable for offset calibration during normal operation.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The two primary supporting circuits required to maximize the performance of a high-precision, successive approximation register (SAR) analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides typical application circuits designed for the device.

9.2 Typical Applications

9.2.1 2-Channel, Simultaneous Sampling Data Acquisition Using the ADS7054

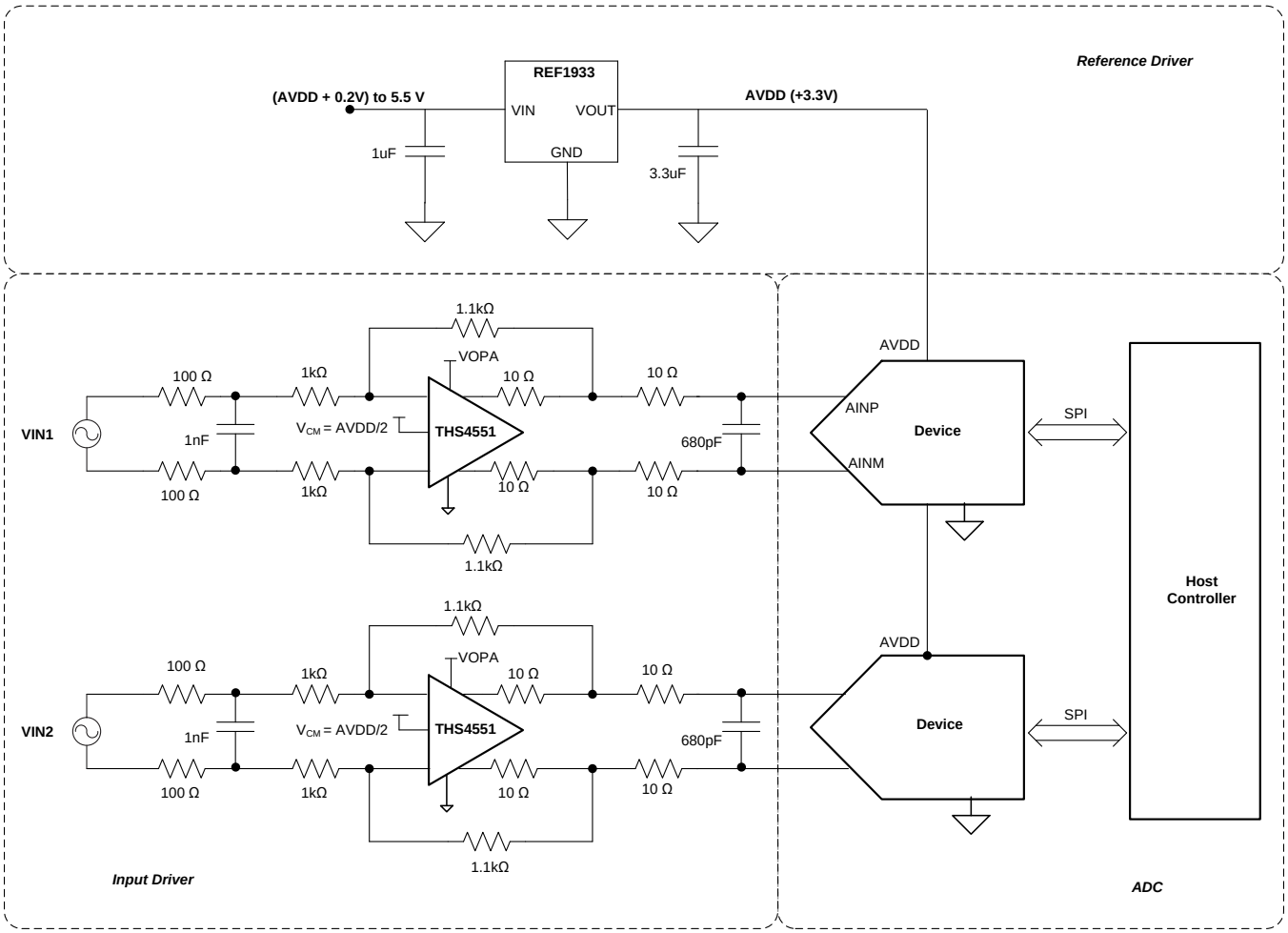

Figure 40. 2-Channel, Simultaneous-Sampling Data Acquisition (DAQ) Circuit Using the ADS7054

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Typical Applications (continued)

9.2.1.1 Design Requirements

The goal of the circuit shown in Figure 40 is to design a two-channel, simultaneous-sampling data acquisition (DAQ) circuit based on the ADS7054 with an SNR greater than 79 dB and a THD less than –85 dB for input frequencies from 2 kHz to 50 kHz at a throughput of 1 MSPS. This simultaneous-sampling scheme is typically used in motor sine and cosine (sin-cos) encoders, resolvers, fish finders, sonar, and I-Q demodulation.

9.2.1.2 Detailed Design Procedure

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and charge kickback filter. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

9.2.1.2.1 Low Distortion Charge Kickback Filter Design

Figure 41 shows the input circuit of a typical SAR ADC. During the acquisition phase, the SW switch closes and connects the sampling capacitor (C_{SH}) to the input driver circuit. This action introduces a transient on the input pins of the SAR ADC. An ideal amplifier with 0 Ω of output impedance and infinite current drive can settle this transient in zero time. For a real amplifier with non-zero output impedance and finite drive strength, this switched capacitor load can create stability issues.

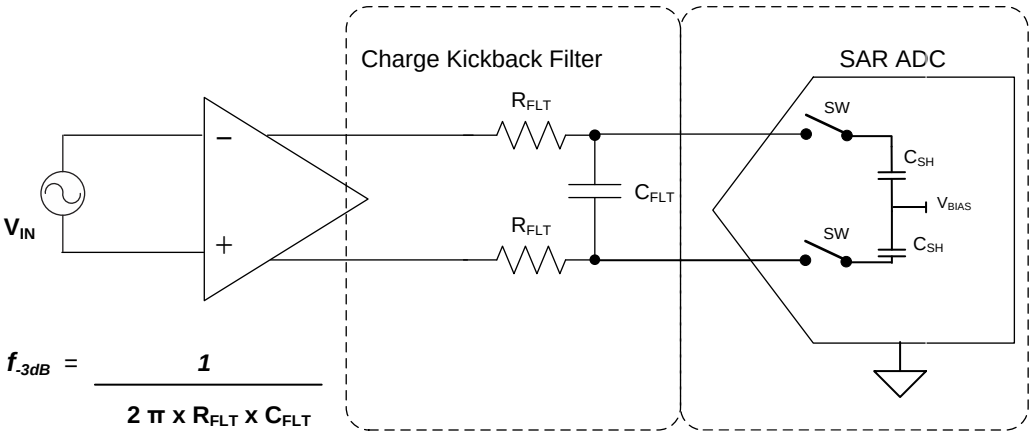

Figure 41. Input Sample-and-Hold Circuit for a Typical SAR ADC

For ac signals, the filter bandwidth must be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system. Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected across the ADC inputs. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor is at least 20 times the specified value of the ADC sampling capacitance. For this device, the input sampling capacitance is equal to 16 pF. Thus, the value of C_{FLT} is greater than 320 pF. Select a COG- or NPO-type capacitor because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design.

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Typical Applications (continued)

9.2.1.2.2 Input Amplifier Selection

The input amplifier bandwidth is typically much higher than the cutoff frequency of the charge kickback filter. Thus, TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers can require more bandwidth than others to drive similar filters. To learn more about the SAR ADC input driver design, see the TI Precision Labs training video series.

The THS4551 is selected for its high bandwidth (135 MHz), low total harmonic distortion of –90 dBc at 100 kHz, and ultra-low noise of (3.2 nV/√Hz). The THS4551 is powered up from the power supply (VDD = 5 V and VSS = GND).

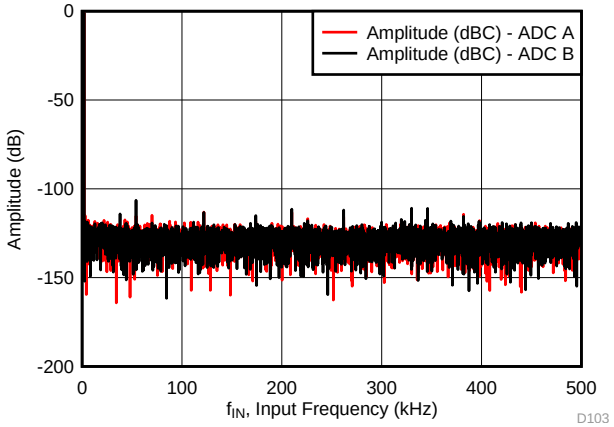
9.2.1.2.3 Reference Circuit

The ADS70xx uses the analog supply voltage (AVDD) as the reference voltage for the analog-to-digital conversion. During the conversion process, the internal capacitors are switched to the level of the AVDD pin as per the successive approximation algorithm. A voltage reference must be selected with low temperature drift, high output current drive, and low output impedance. For this application, the REF1933 was selected as the voltage reference and analog power supply for the ADC. The REF1933 has excellent temperature drift performance (25 ppm/°C), good initial accuracy (0.1%), high output drive capability (25 mA), and low quiescent current (360 µA). The REF1933 also provides a bias voltage output of half the reference voltage (V_{REF} / 2) that can be used as the common-mode input for the amplifier.

TI recommends a 3.3-µF (C_{AVDD}), low equivalent series resistance (ESR) ceramic capacitor between the AVDD and GND pins. This decoupling capacitor provides the instantaneous charge required by the internal circuit during the conversion process and maintains a stable dc voltage on the AVDD pin.

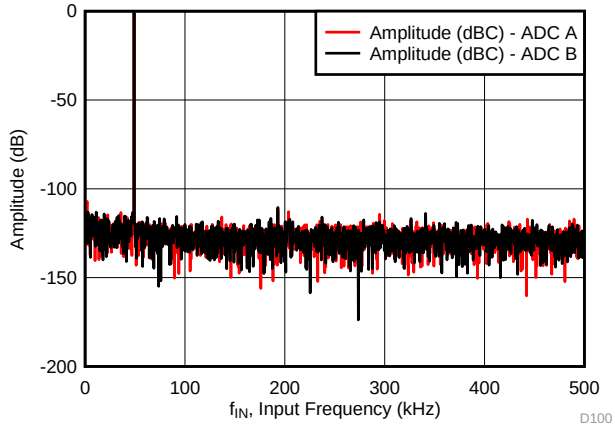
9.2.1.3 Application Curves

Figure 42 and Figure 43 provide the measurement results for the circuit described in Figure 40.



Device 1 SNR = 80.3 dB, THD = –93 dB, SINAD = 79.6 dB
Device 2 SNR = 79.8 dB, THD = –92 dB, SINAD = 79.3 dB

Figure 42. Test Results for the ADS7054 and THS4551 for a 2-kHz input



Device 1 SNR = 79.2 dB, THD = –94 dB, SINAD = 78.9 dB
Device 2 SNR = 78.9 dB, THD = –92 dB, SINAD = 78.6 dB

Figure 43. Test Results for the ADS7054 and THS4551 for a 50-kHz input

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Typical Applications (continued)

9.2.2 Improving Precision of Single-Ended Signal Source Measurements Using the ADS7054

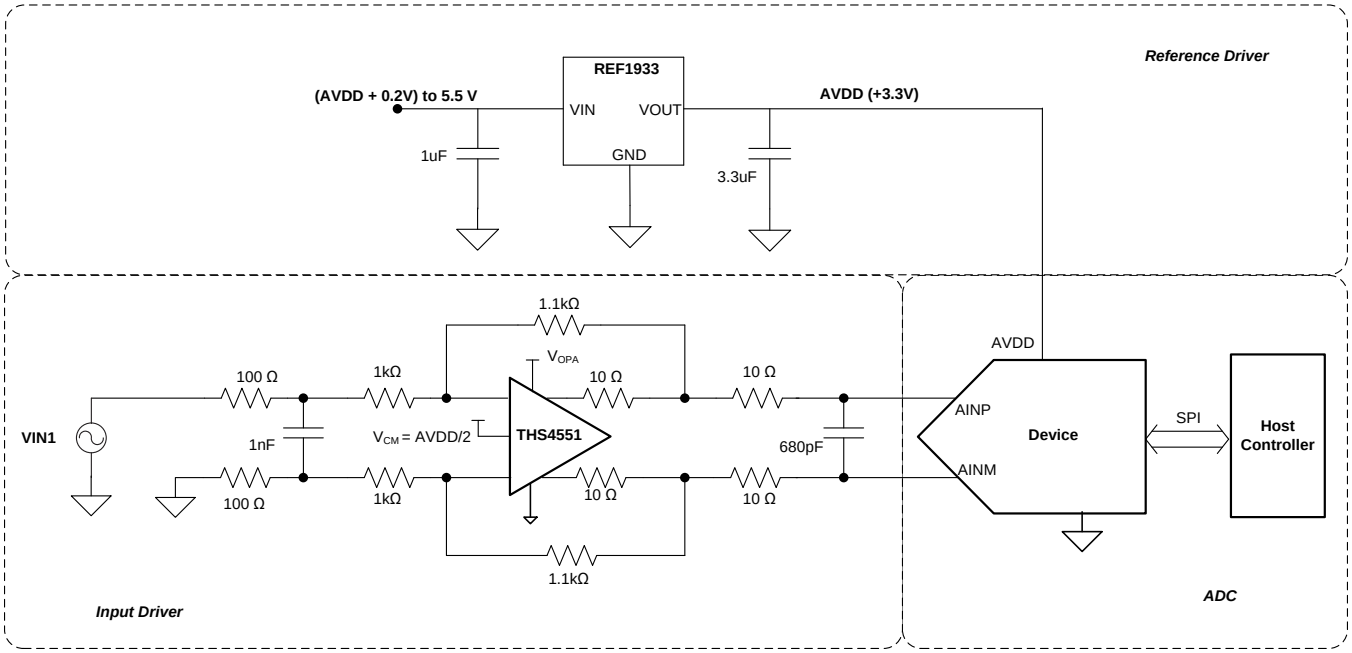

Figure 44. Interfacing Single-Ended Signals with the ADS7054 Using a Single-Ended to Differential Front-End

9.2.2.1 Design Requirements

Some applications have sensor or signal inputs that are single ended. In order to increase the dynamic range, linearity, and precision of the system, such single-ended signals are often required to be interfaced with a differential input ADC. The goal of the design shown in Figure 44 is to interface a single-ended input source with the ADS7054 using a single-ended to differential front-end amplifier to achieve an SNR greater than 79 dB and a THD less than –85 dB for input frequencies up to 10 kHz at a throughput of 1 MSPS.

9.2.2.2 Detailed Design Procedure

To achieve a SNR greater than 79 dB, the operational amplifier must have high bandwidth in order to settle the input signal within the acquisition time of the ADC. The operational amplifier must have low noise to keep the total system noise below 20% of the input-referred noise of the ADC. For the application circuit shown in Figure 44, the THS4551 is selected for its high bandwidth (135 MHz), low total harmonic distortion of –90 dBc at 100 kHz, and ultra-low noise of (3.2 nV/$\sqrt{\text{Hz}}$). The THS4551 is powered up from the power supply (VDD = 5 V and VSS = GND).

The THS4551 can be used in a single-ended to differential configuration as shown in Figure 44 without any performance degradation. This configuration enables single-ended input signals to be interfaced with differential input SAR ADCs (such as the ADS7054) to achieve higher system-level precision.

For this application, the REF1933 was selected as the voltage reference and analog power supply for the ADC. The REF1933 has excellent temperature drift performance (25 ppm/°C), good initial accuracy (0.1%), high output drive capability (25 mA), and low quiescent current (360 µA). The REF1933 also provides a bias voltage output of half the reference voltage (V_{REF} / 2) that can be used as the common-mode input for the amplifier.

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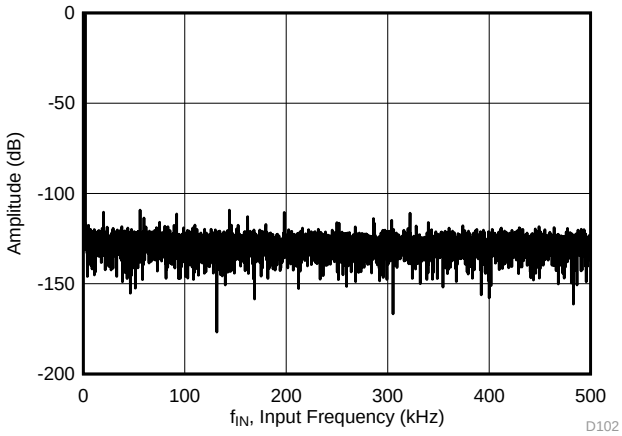
Typical Applications (continued)

9.2.2.3 Application Curve

Figure 45 shows the FFT plot for the ADS7054 with a 2-kHz, single-ended input signal used for the circuit in Figure 44.



SNR = 79.8 dB, THD = –92 dB, SINAD = 79.1 dB

Figure 45. Test Results for the ADS7054 With a 2-kHz, Single-Ended Input

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10 Power Supply Recommendations

10.1 AVDD and DVDD Supply Recommendations

The device has two separate power supplies: AVDD and DVDD.

AVDD powers the analog blocks and is also used as the reference voltage for the analog-to-digital conversion. Use a low-noise, low-dropout regulator (LDO) or a discrete reference to supply AVDD (see the *Reference* and *Application Information* sections). Always set the AVDD supply to be greater than or equal to the maximum input signal to avoid code saturation. Decouple the AVDD pin to the GND pin with a 3.3-µF ceramic decoupling capacitor.

DVDD is used for the interface circuits. Decouple the DVDD pin to the GND pin with a 1-µF ceramic decoupling capacitor. 图 46 shows the decoupling recommendations.

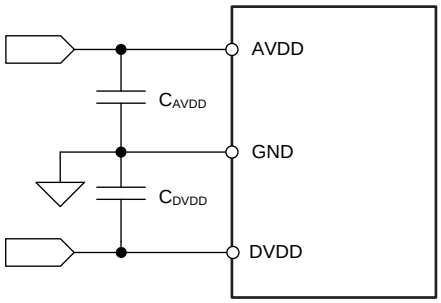

图 46. Power-Supply Decoupling

10.2 Optimizing Power Consumed by the Device

In order to best optimize the power consumed by the device, use the following design considerations:

- Keep the analog supply voltage (AVDD) in the specified operating range and equal to the maximum analog input voltage.
- Keep the digital supply voltage (DVDD) in the specified operating range and at the lowest value supported by the host controller.
- Reduce the load capacitance on the SDO output.
- Run the device at the optimum throughput. Power consumption reduces proportionally with the throughput.

10.2.1 Estimating Digital Power Consumption

The current consumption from the DVDD supply depends on the DVDD voltage, the load capacitance on the SDO pin ($C_{LOAD\text{-}SDO}$), and the output code, and can be calculated as:

$$I_{DVDD} = C_{LOAD\text{-}SDO} \times V \times f \quad (2)$$

where:

- $C_{LOAD\text{-}SDO}$ = Load capacitance on the SDO pin
- V = DVDD supply voltage
- f = Frequency of transitions on the SDO output

The number of transitions on the SDO output depends on the output code, and thus changes with the analog input. The maximum value of f occurs when data output on the SDO change on every SCLK (that is, for output codes of 2AAAh or 1555h). With an output code of 2AAAh or 1555h, f = 7 MHz and when $C_{LOAD\text{-}SDO}$ = 20 pF and DVDD = 1.8 V, I_{DVDD} = 250 µA.

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11 Layout

11.1 Layout Guidelines

图 47 shows a typical connection diagram for the ADS7054.

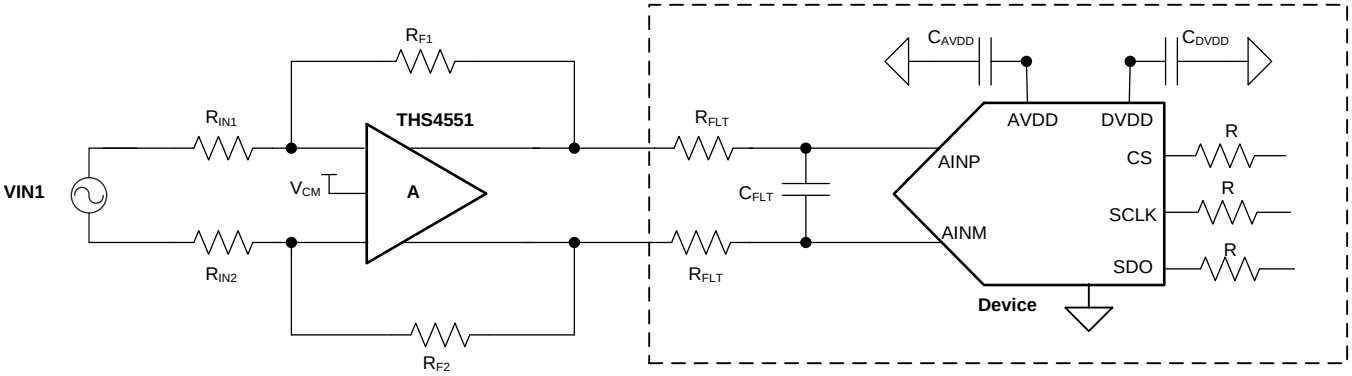

图 47. Typical Connection Diagram

图 48 depicts a board layout example for the device for the typical connection diagram in 图 47. The key considerations for layout are:

- Use a solid ground plane underneath the device and partition the PCB into analog and digital sections
- Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources.
- The power sources to the device must be clean and well-bypassed. Use C_{AVDD} decoupling capacitors in close proximity to the analog (AVDD) power-supply pin.
- Use a C_{DVDD} decoupling capacitor close to the digital (DVDD) power-supply pin.
- Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors.
- Connect the ground pin to the ground plane using a short, low-impedance path.
- Place the charge kickback filter components close to the device.

Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors are recommended because these components provide the most stable electrical properties over voltage, frequency, and temperature changes.

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11.2 Layout Example

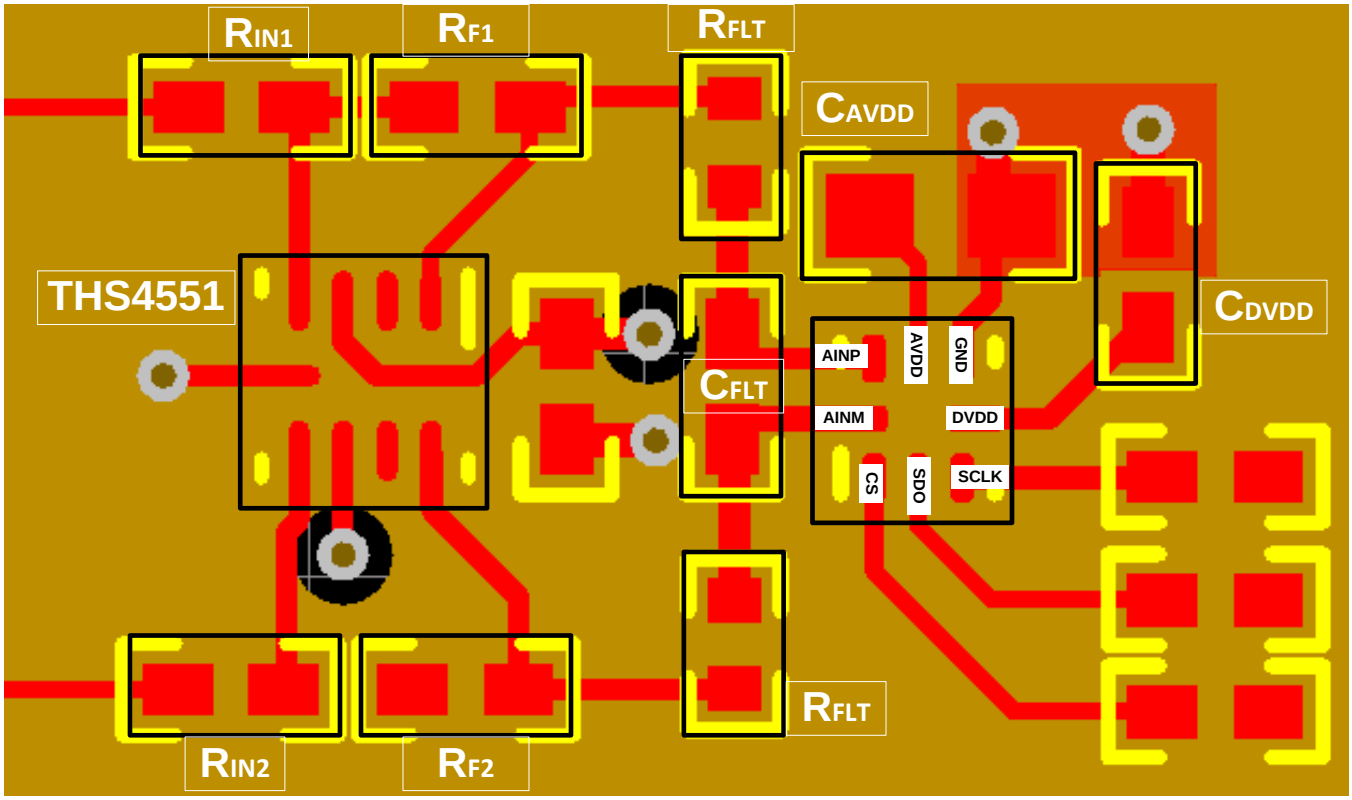

图 48. Example Layout

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

TI 高精度实验室培训视频系列

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

输入驱动器放大器（单端输入）：

- *《OPAx836 极低功耗、轨至轨输出、负轨输入、电压反馈运算放大器》*
- *THS403x 100MHz 低噪声高速放大器*
- *《OPAx365 50MHz、零交叉、低失真、高 CMRR、RRI/O、单电源运算放大器》*

输入驱动器放大器（全差分输入）：

- *THS4551 低噪声 150MHz 全差分精密放大器*
- *《OPAx836 极低功耗、轨至轨输出、负轨输入、电压反馈运算放大器》*

基准驱动器：

- *《REF19xx 低漂移、低功率、双路输出、V_{REF} 和 V_{REF}/2 电压基准》*
- *《具有集成 ADC 驱动器缓冲器的 REF61xx 高精度电压基准》*

类似器件：

- *《ADS7042 超低功耗、超小尺寸、12 位、1MSPS、SAR ADC》*
- *《ADS7049-Q1 小型低功耗 12 位、2MSPS SAR ADC》*

参考设计：

- TI 设计：*采用 73dB SNR、7.5MSPS 时间交织 SAR ADC 且适用于成像应用的模拟前端参考设计*
- *针对双极信号采用运算放大器和 FDA 的单端到差分*

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

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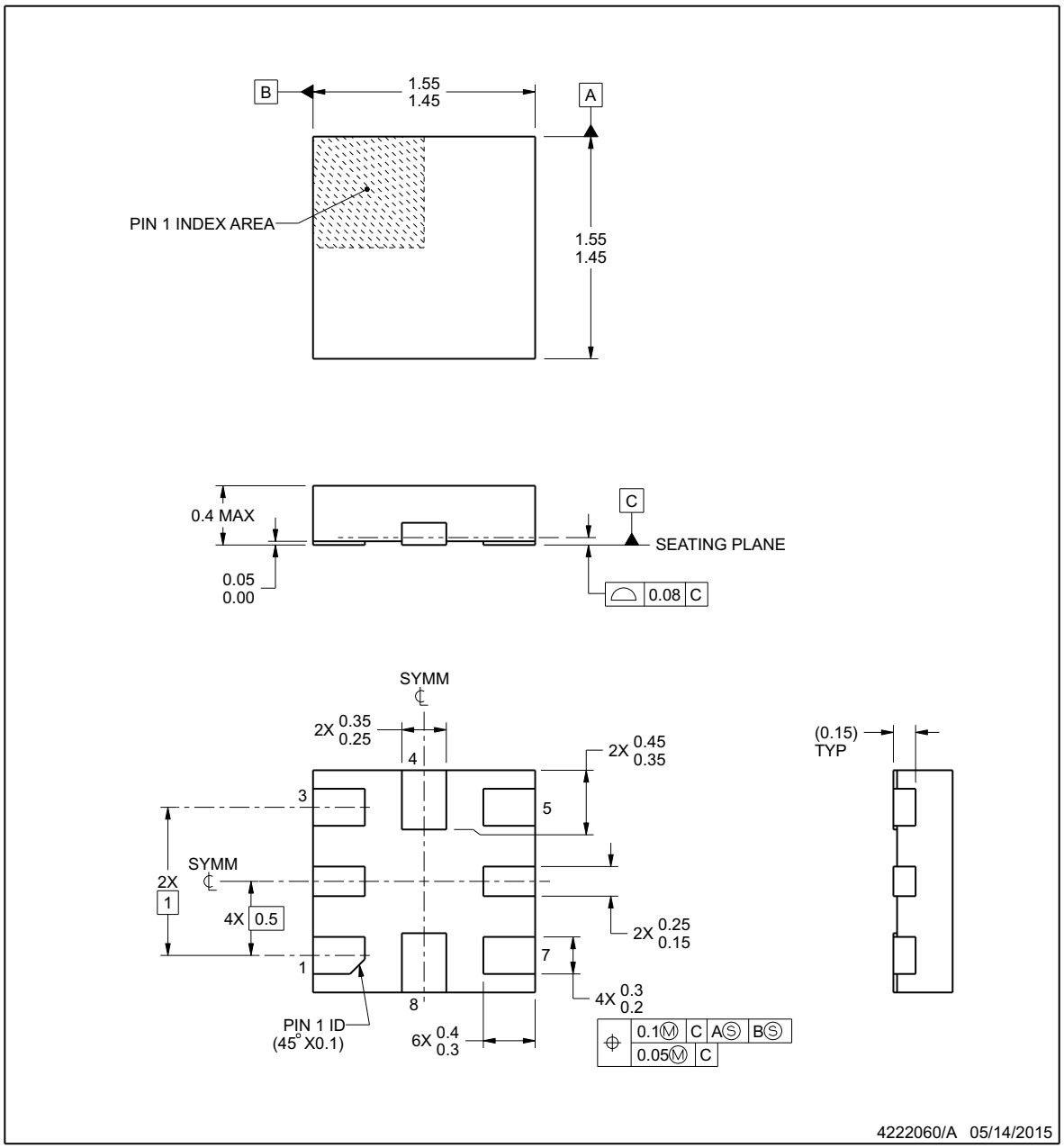
PACKAGE OUTLINE

RUG0008A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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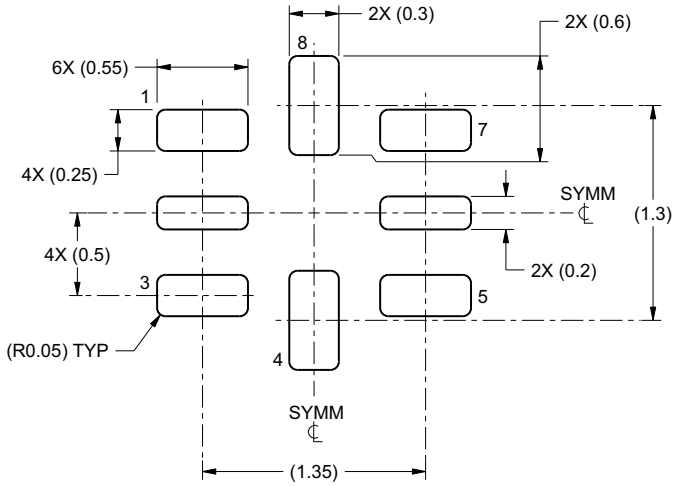
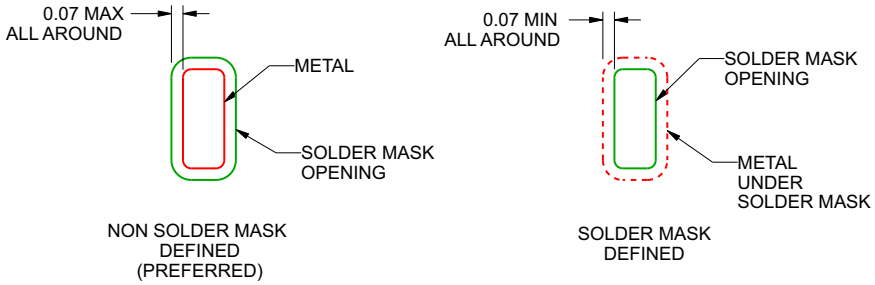
EXAMPLE BOARD LAYOUT

RUG0008A — **X2QFN - 0.4 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

4222060/A 05/14/2015

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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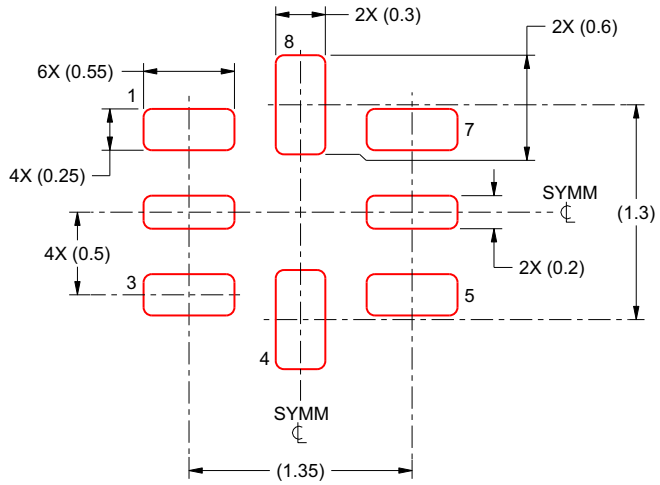
EXAMPLE STENCIL DESIGN

RUG0008A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE:25X

4222060/A 05/14/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7054IRUGR	ACTIVE	X2QFN	RUG	8	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	9Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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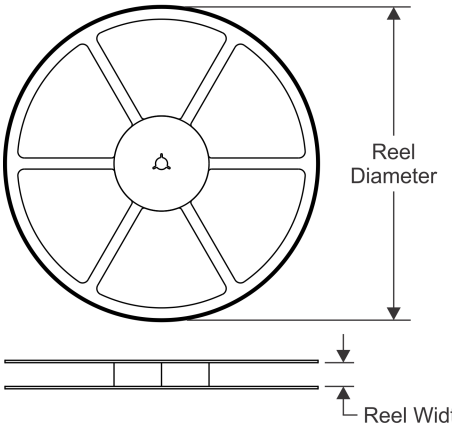
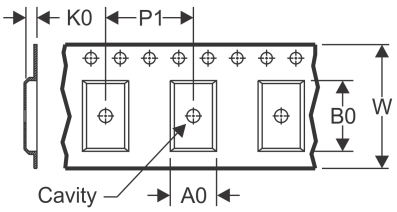
TAPE AND REEL INFORMATION

REEL DIMENSIONS

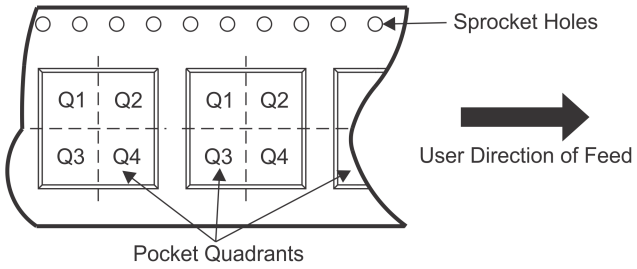


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

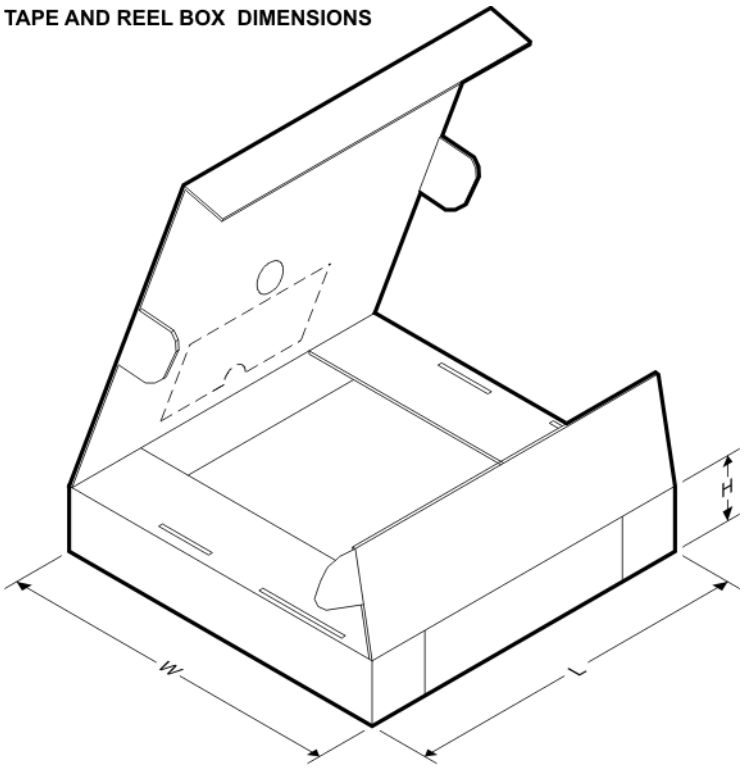
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7054IRUGR	X2QFN	RUG	8	3000	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2

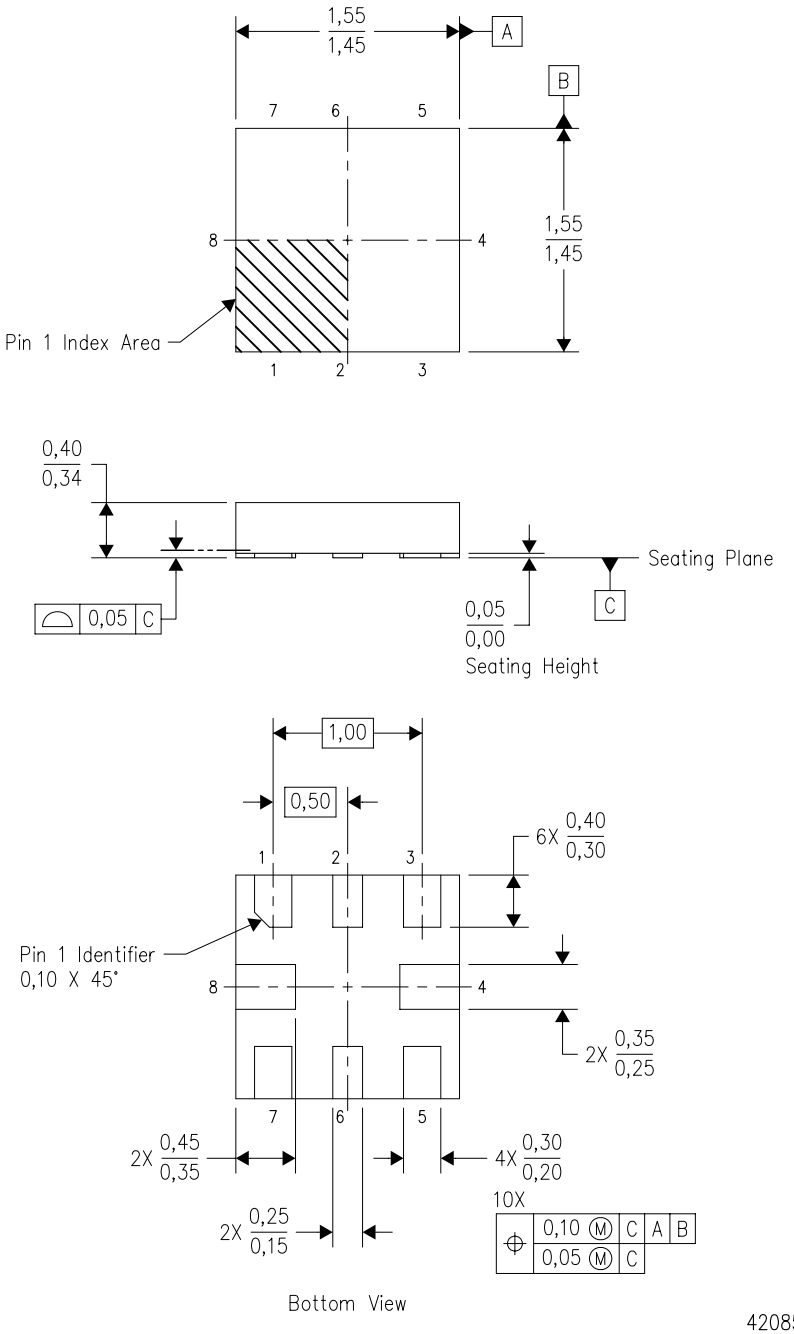
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7054IRUGR	X2QFN	RUG	8	3000	183.0	183.0	20.0

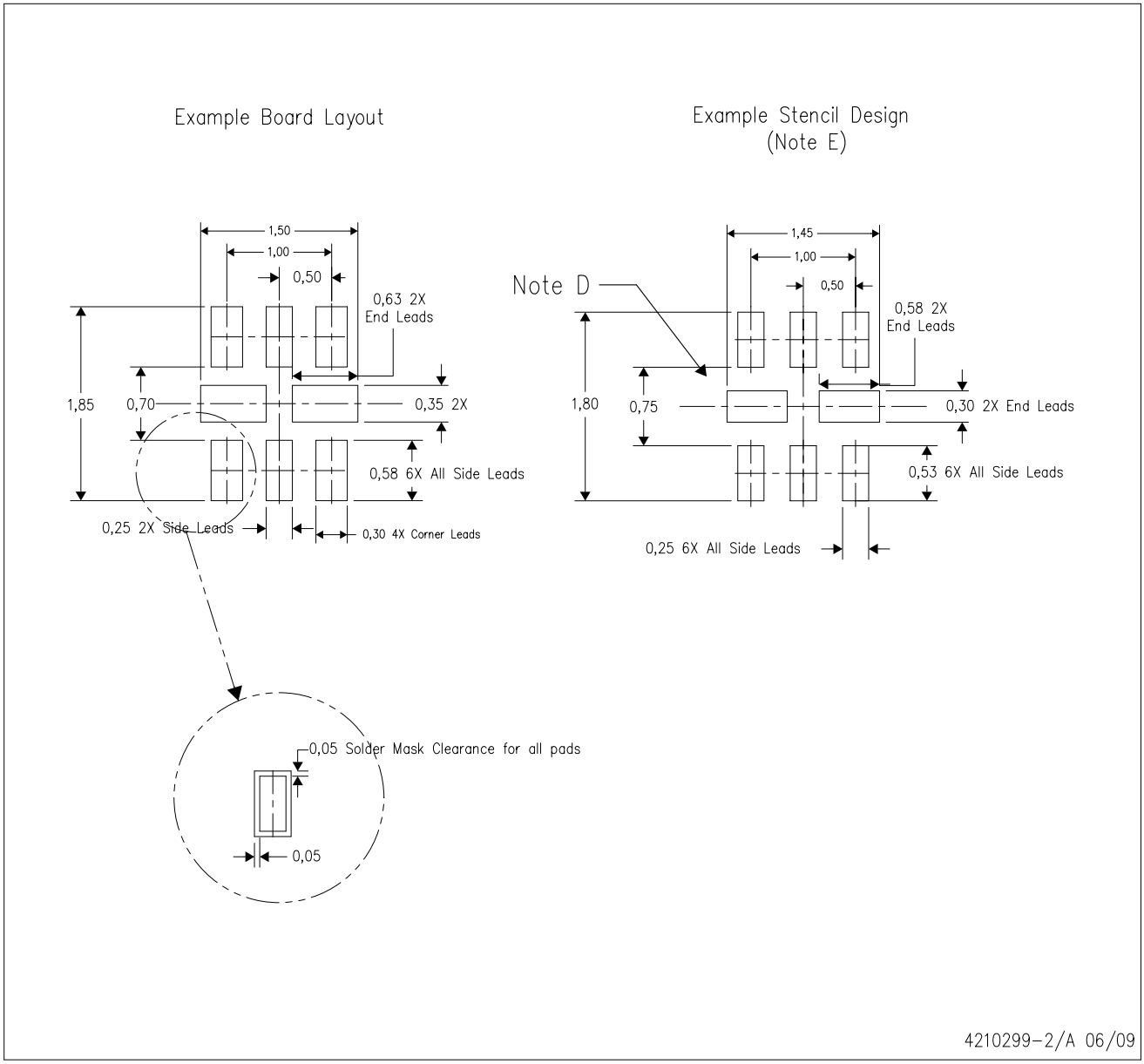
RUG (S–PQFP–N8) PLASTIC QUAD FLATPACK



4208528–2/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2ECD.

RUG (R–PQFP–N8)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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Click to view products by Texas Instruments ***manufacturer:***

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