14-位, 2 MSPS, 双通道, 差分/单端，超低功耗模数转换器

查询样品: ADS7945, ADS7946

特性

- 取样率: 2 MSPS
- 14-位, 与 8/10/12-位 ADS7947/8/9 系列产品 (ADS7946)引脚兼容
- 突出的性能:
  - SNR: 84 dB (ADS7945)
  - 无丢码
  - INL: 1.5 LSB (最大) (ADS7945)
- 低功耗:
  - 在 2 MSPS 运行模式下，11.6 mW
  - 低速状态下自动动率降低:
    - 在 500 kSPS模式下 7.2 mW
    - 在 100 kSPS模式下 1.4 mW
    - 在 20 kSPS 模式下 0.3 mW
- 宽电源范围:
  - 模拟: 2.7 V 至 5.25 V
  - 数字: 1.65 V 至 AVDD
- 简单串口 (SPI)
- 完全指定温度范围从 –40°C 到 +125°C
- 微笑器件封装: 3 mm × 3 mm QFN

应用范围

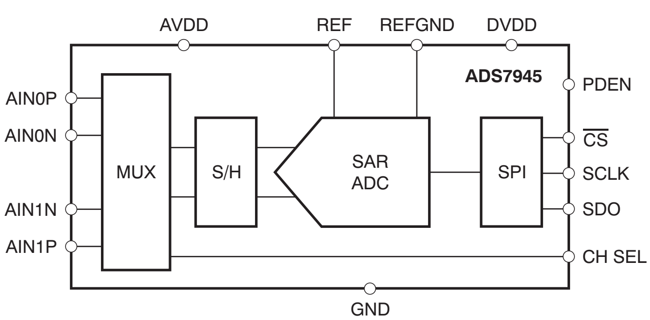
- 光纤网络
- 医疗仪表
- 电池供电设备
- 数据采集系统

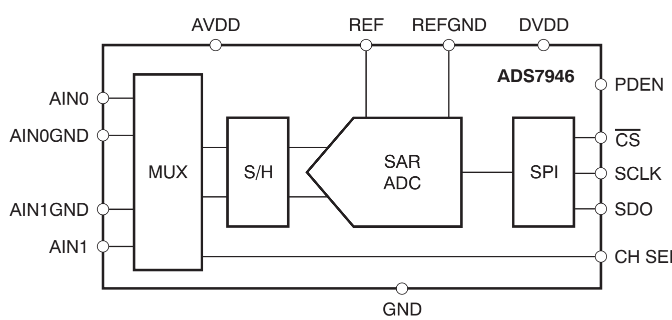
说明

ADS7945/6 是 14-为, 2 MSPS 模数转换器 (ADCs), 它们分别具有差分和单端输入。 此设备 运行在 2 MSPS 具有一个标准16时钟数据帧的采样速率。 此设备特有突出的dc精度和出色的动态性能；ADS7946与 8/10/12-位ADS7947/8/9 设备引脚兼容。 此设备包含一个2通道输入复用器和一个低功率逐次逼近寄存器（SAR），此寄存器具有一个固有的取样保持输入级。

ADS7945/6 支持较宽的模拟供电范围，允许的全尺寸输入范围已拓展到 ±5 V 差分或者 5 V 单端范围。 一个简单的 SPI™, 具有数字供电，能在低至1.65V的电压下运行，能很容易的与多种数字控制器建立端口连接。 当运行在较低速度时，自动掉电可被启用以大幅减少功率消耗。

封装方式为微小 3 mm × 3 mm QFN, ADS7945/6 完全额定工作温度范围从 –40°C 至 +125°C 并适合多种数据采集应用，在这里，高性能，低功耗和小封装尺寸是关键。





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English Data Sheet: SBAS539B

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FAMILY AND ORDERING INFORMATION(1)

PRODUCT	RESOLUTION (Bits)	INPUT
ADS7945	14	Unipolar, differential
ADS7946	14	Unipolar, single-ended
ADS7947	12	Unipolar, single-ended
ADS7948	10	Unipolar, single-ended
ADS7949	8	Unipolar, single-ended

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
AINxP to GND or AINxN to GND (ADS7945)		–0.3 to AVDD + 0.3	V
AINx to GND (ADS7946)		–0.3 to AVDD + 0.3	V
AINxGND to GND (ADS7946)		–0.3 to +0.3	V
AVDD to GND or DVDD to GND		–0.3 to 7	V
Digital input voltage to GND		–0.3 to DVDD + 0.3	V
Digital output to GND		–0.3 to DVDD + 0.3	V
Operating temperature range		–40 to +125	°C
Storage temperature range		–65 to +150	°C
ESD ratings	Human body model (HBM)	2000	V
	Charged device model (CDM)	500	V
	Machine model (MM)	200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *electrical characteristics* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: ADS7945 (Differential)

Minimum/maximum specifications at T_A = –40°C to +125°C, AVDD = 2.7 V to 5.25 V, DVDD = 1.65 V to AVDD, input common-mode = V_{REF}/2 ± 0.2, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.
Typical specifications at T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, input common-mode = V_{REF}/2 ± 0.2, and f_{SAMPLE} = 2 MSPS.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT					
Full-scale input span(1)	AINxP – AINxN	$-V_{REF}$		V_{REF}	V
Absolute input range	AIN0P, AIN1P	–0.2		AVDD + 0.2	V
	AIN0N, AIN1N	–0.2		AVDD + 0.2	V
Input common-mode range(2)	(AINxP + AINxN)/2		V_{REF}/2 ± 0.2		V
Input capacitance(3)			32		pF
Input leakage current	At +125°C		1.5		nA
SYSTEM PERFORMANCE					
Resolution			14		Bits
No missing codes		14			Bits
Integral linearity		–1.5	±0.8	1.5	LSB(4)
Differential linearity		–1	±0.8	1.5	LSB
Offset error(5)		–4	±1.5	4	LSB
Gain error		–4	±1.5	4	LSB
Transition noise				25	μV_{RMS}
Power-supply rejection	With 500 Hz sine wave on AVDD		60		dB
SAMPLING DYNAMICS					
Conversion time				16	SCLK
Acquisition time		80			ns
Maximum sample rate (throughput rate)	40 MHz SCLK with a 16-clock frame			2	MSPS
Aperture delay(6)				10	ns
Aperture jitter(6)			10		ps
Step response(6)(3)			80		ns
DYNAMIC CHARACTERISTICS					
Total harmonic distortion (THD)(7)	20 kHz, V_{REF} = 4.0 V		–92		dB
Signal-to-noise ratio (SNR)	20 kHz, V_{REF} = 4.0 V	82	84		dB
	100 kHz, V_{REF} = 4.0 V		83		dB
Signal-to-noise and distorion ratio (SINAD)	20 kHz, V_{REF} = 4.0 V		83.5		dB
Spurious-free dynamic range (SFDR)	20 kHz, V_{REF} = 4.0 V		94		dB
Full-power bandwidth(8)	At –3 dB		15		MHz

(1) Ideal input span; does not include gain or offset error.
(2) Refer to the *Input Common-Mode Range* section in Application Information.
(3) Refer to Figure 76 for sampling circuit details.
(4) LSB means least significant bit.
(5) Measured relative to an ideal full-scale input.
(6) Ensured by simulation.
(7) Calculated on the first nine harmonics of the input frequency.
(8) Indicates signal bandwidth for undersampling applications.

ELECTRICAL CHARACTERISTICS: ADS7945 (Differential) (continued)

Minimum/maximum specifications at T_A = –40°C to +125°C, AVDD = 2.7 V to 5.25 V, DVDD = 1.65 V to AVDD, input common-mode = $V_{REF}/2$ ± 0.2, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.
Typical specifications at T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, input common-mode = $V_{REF}/2$ ± 0.2, and f_{SAMPLE} = 2 MSPS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7DVDD			V
	V_{IL}				0.3DVDD	V
	V_{OH}	SDO load 20 pF	0.8DVDD			V
	V_{OL}	SDO load 20 pF			0.2DVDD	V
Input leakage current	I_{IH}, I_{IL}	0 < V_{IN} < DVDD		±20		nA
External reference			2.5		AVDD	V
POWER-SUPPLY REQUIREMENTS						
AVDD			2.7	3.3	5.25	V
DVDD			1.65	3.3	AVDD	V
AVDD supply current	$I_{DYNAMIC}$	AVDD = 3.3 V, f_{SAMPLE} = 2 MSPS		3.5	4	mA
		AVDD = 5 V, f_{SAMPLE} = 2 MSPS		4	5	mA
	I_{STATIC}	AVDD = 3.3 V, SCLK off		2.3		mA
		AVDD = 5 V, SCLK off		2.5	3	mA
DVDD supply current(9)		DVDD = 3.3 V, f_{SAMPLE} = 2 MSPS, SDO load 20 pF		750		µA
Power-down state AVDD supply current	$I_{PD\text{-}DYNAMIC}$	SCLK = 40 MHz			550	µA
	$I_{PD\text{-}STATIC}$	SCLK off			2.5	µA
Power-up time		From power-down state using PDEN pin			1	µs
TEMPERATURE RANGE						
Specified performance			–40		+125	°C

(9) DVDD consumes only dynamic current. $I_{DVDD} = C_{LOAD}$ × DVDD × number of 0→1 transitions in SDO × f_{SAMPLE}. This is a load-dependent current and there is no DVDD current when the output is not toggling.

ELECTRICAL CHARACTERISTICS: ADS7946 (Single-Ended)

Minimum/maximum specifications at T_A = –40°C to +125°C, AVDD = 2.7 V to 5.25 V, DVDD = 1.65 V to AVDD, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.
Typical specifications at T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, and f_{SAMPLE} = 2 MSPS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Full-scale input span[1]		AINx – AINxGND	0		V_{REF}	V
Absolute input range		AIN0, AIN1	–0.2		AVDD + 0.2	V
		AIN0GND, AIN1GND	–0.2		0.2	V
Input capacitance[2]				32		pF
Input leakage current		At +125°C		1.5		nA
SYSTEM PERFORMANCE						
Resolution				14		Bits
No missing codes			14			Bits
Integral linearity			–2.5	±1.25	2.5	LSB[3]
Differential linearity			–1	±0.8	2.0	LSB
Offset error[4]			–4	±1.5	4	LSB
Gain error			–4	±1.5	4	LSB
Transition noise					25	μV_{RMS}
Power-supply rejection		With 500 Hz sine wave on AVDD		60		dB
SAMPLING DYNAMICS						
Conversion time					16	SCLK
Acquisition time			80			ns
Maximum sample rate (throughput rate)		40 MHz SCLK with a 16-clock frame			2	MSPS
Aperture delay[5]					10	ns
Aperture jitter[5]				10		ps
Step response[5][2]				80		ns
DYNAMIC CHARACTERISTICS						
Total harmonic distortion (THD)[6]		20 kHz, V_{REF} = 4.0 V		–85		dB
Signal-to-noise ratio (SNR)		20 kHz, V_{REF} = 4.0 V	79	82		dB
		100 kHz, V_{REF} = 4.0 V		80		dB
Signal-to-noise and distortion ratio (SINAD)		20 kHz, V_{REF} = 4.0 V		78.8		dB
Spurious-free dynamic range (SFDR)		20 kHz, V_{REF} = 4.0 V		86		dB
Full-power bandwidth[7]		At –3 dB		15		MHz
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7DVDD			V
	V_{IL}				0.3DVDD	V
	V_{OH}	SDO load 20 pF	0.8DVDD			V
	V_{OL}	SDO load 20 pF			0.2DVDD	V
Input leakage current	I_{IH}, I_{IL}	0 < V_{IN} < DVDD		±20		nA
External reference			2.5		AVDD	V

(1) Ideal input span; does not include gain or offset error.
(2) Refer to Figure 76 for sampling circuit details.
(3) LSB means least significant bit.
(4) Measured relative to an ideal full-scale input.
(5) Ensured by simulation.
(6) Calculated on the first nine harmonics of the input frequency.
(7) Indicates signal bandwidth for undersampling applications.

ELECTRICAL CHARACTERISTICS: ADS7946 (Single-Ended) (continued)

Minimum/maximum specifications at T_A = –40°C to +125°C, AVDD = 2.7 V to 5.25 V, DVDD = 1.65 V to AVDD, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.
Typical specifications at T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, and f_{SAMPLE} = 2 MSPS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY REQUIREMENTS						
AVDD			2.7	3.3	5.25	V
DVDD			1.65	3.3	AVDD	V
AVDD supply current	$I_{DYNAMIC}$	AVDD = 3.3 V, f_{SAMPLE} = 2 MSPS		3.5	4	mA
		AVDD = 5 V, f_{SAMPLE} = 2 MSPS		4	5	mA
	I_{STATIC}	AVDD = 3.3 V, SCLK off		2.3		mA
		AVDD = 5 V, SCLK off		2.5	3	mA
DVDD supply current(8)		DVDD = 3.3 V, f_{SAMPLE} = 2 MSPS, SDO load 20 pF		750		µA
Power-down state AVDD supply current	$I_{PD-DYNAMIC}$	SCLK = 40 MHz			550	µA
	$I_{PD-STATIC}$	SCLK off			2.5	µA
Power-up time		From power-down state using PDEN pin			1	µs
TEMPERATURE RANGE						
Specified performance			–40		+125	°C

(8) DVDD consumes only dynamic current. $I_{DVDD} = C_{LOAD} \times DVDD \times$ number of 0→1 transitions in SDO × f_{SAMPLE}. This is a load-dependent current and there is no DVDD current when the output is not toggling.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS7945/6 RTE 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	54.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	53.7	
θ_{JB}	Junction-to-board thermal resistance	19.2	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	14.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	5.2	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 SPRA953。

PARAMETER MEASUREMENT INFORMATION

TIMING DIAGRAM: ADS7945, ADS7946

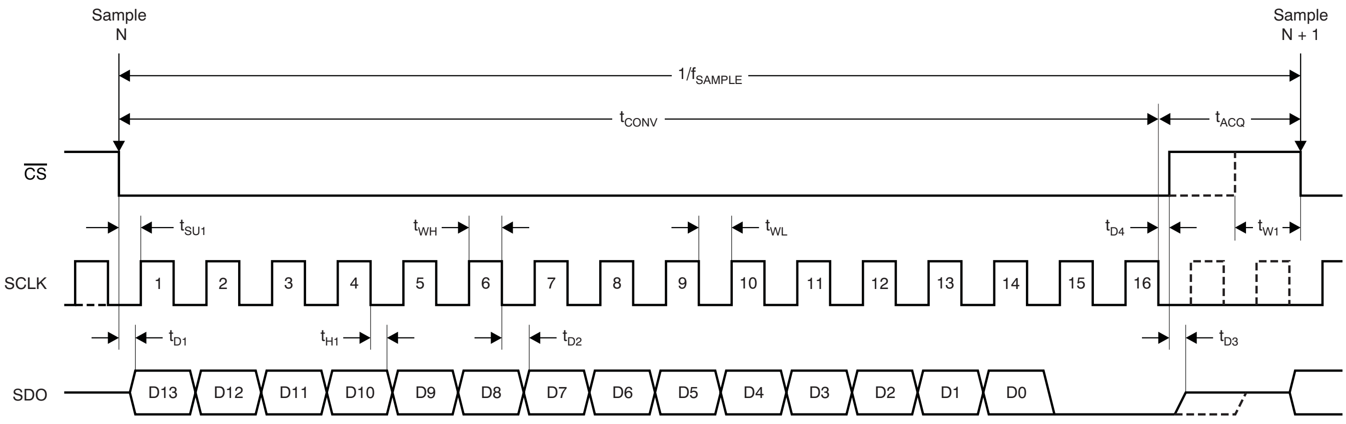


Table 1. TIMING REQUIREMENTS: ADS7945, ADS7946(1)(2)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time				16	SCLK
t_{ACQ}	Acquisition time		80			ns
f_{SAMPLE}	Sample rate (throughput rate)	SCLK = 40 MHz, 16-clock frame			2	MSPS
t_{W1}	Pulse width $\overline{CS}$ high		25			ns
t_{D1}	Delay time, $\overline{CS}$ low to first data (D0-15) out	DVDD = 1.8 V			14.5	ns
		DVDD = 3 V			12.5	ns
		DVDD = 5 V			8.5	ns
t_{SU1}	Setup time, $\overline{CS}$ low to first rising edge of SCLK	DVDD = 1.8 V	3.5			ns
		DVDD = 3 V	3.5			ns
		DVDD = 5 V	3.5			ns
t_{D2}(3)	Delay time, SCLK falling to SDO	DVDD = 1.8 V			11	ns
		DVDD = 3 V			9	ns
		DVDD = 5 V			7.1	ns
t_{H1}	Hold time, SCLK falling to data valid	DVDD = 1.8 V	4			ns
		DVDD = 3 V	3			ns
		DVDD = 5 V	2			ns
t_{D3}	Delay time, $\overline{CS}$ high to SDO 3-state	DVDD = 1.8 V			15	ns
		DVDD = 3 V			12.5	ns
		DVDD = 5 V			8.5	ns
t_{D4}	Delay time $\overline{CS}$ rising edge from conversion end (refer to the t_{CONV} specification for conversion time)		10			ns
t_{WH}	Pulse duration, SCLK high		8			ns
t_{WL}	Pulse duration, SCLK low		8			ns
	SCLK frequency				40	MHz
t_{PDSU}	Setup time, PDEN high to $\overline{CS}$ rising edge (refer to Figure 84 and Figure 85)		2			ns
t_{PDH}	Hold time, $\overline{CS}$ rising edge to PDEN falling edge (refer to Figure 84)		20			ns

(1) All specifications are ensured by simulations at T_A = –40°C to +125°C, and DVDD = 1.65 V to AVDD, unless otherwise noted.
(2) 1.8 V specifications apply from 1.65 V to 2 V; 3 V specifications apply form 2.7 V to 3.6 V; 5 V specifications apply from 4.75 V to 5.25 V.
(3) With 20 pF load.

PIN CONFIGURATION ADS7945 (DIFFERENTIAL)

**RTE PACKAGE
QFN-16
(TOP VIEW)**

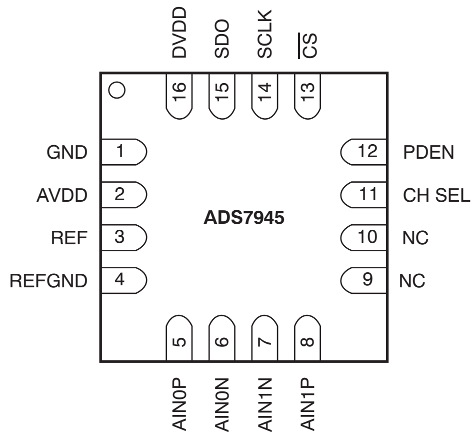


Table 2. PIN FUNCTIONS

PIN NO.	PIN NAME	FUNCTION	DESCRIPTION
1	GND	Analog/digital	Power supply ground; all analog and digital signals are referred with respect to this pin
2	AVDD	Analog	ADC power supply
3	REF	Analog	ADC positive reference input; decouple this pin with REFGND
4	REFGND	Analog	Reference return; short to analog ground plane
5	AIN0P	Analog input	Positive analog input, channel 0
6	AIN0N	Analog input	Negative analog input, channel 0
7	AIN1N	Analog input	Negative analog input, channel 1
8	AIN1P	Analog input	Positive analog input, channel 1
9	NC	—	Not connected internally, it is recommended to externally short this pin to GND
10	NC	—	Not connected internally, it is recommended to externally short this pin to GND
11	CH SEL	Digital input	This pin selects the analog input channel. Low = Channel 0 High = Channel 1 It is recommended to change the channel within a window of one clock; from half a clock after the $\overline{CS}$ falling edge. This change ensures the settling on the multiplexer output before the sample start.
12	PDEN	Digital input	This pin enables a power-down feature if it is high at the $\overline{CS}$ rising edge
13	$\overline{CS}$	Digital input	Chip select signal; active low
14	SCLK	Digital input	Serial SPI clock
15	SDO	Digital output	Serial data out
16	DVDD	Digital	Digital I/O supply

PIN CONFIGURATION ADS7946 (SINGLE-ENDED)

**RTE PACKAGE
QFN-16
(TOP VIEW)**

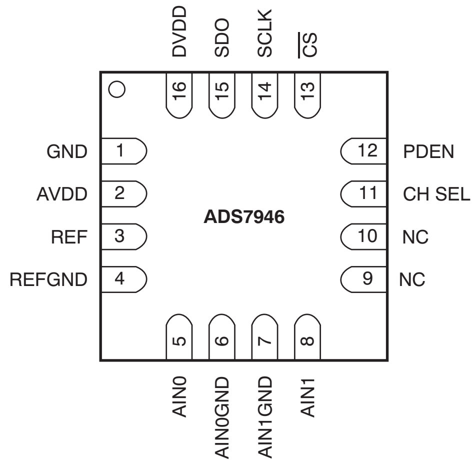


Table 3. PIN FUNCTIONS

PIN NO.	PIN NAME	FUNCTION	DESCRIPTION
1	GND	Analog/digital	Power supply ground; all analog and digital signals are referred with respect to this pin
2	AVDD	Analog	ADC power supply
3	REF	Analog	ADC positive reference input; decouple this pin with REFGND
4	REFGND	Analog	Reference return; short to analog ground plane
5	AIN0	Analog input	Positive analog input, channel 0
6	AIN0GND	Analog input	Ground sense analog input, channel 0
7	AIN1GND	Analog input	Ground sense analog input, channel 1
8	AIN1	Analog input	Positive analog input, channel 1
9	NC	—	Not connected internally, it is recommended to externally short this pin to GND
10	NC	—	Not connected internally, it is recommended to externally short this pin to GND
11	CH SEL	Digital input	This pin selects the analog input channel. Low = Channel 0 High = Channel 1 It is recommended to change the channel within a window of one clock; from half a clock after the $\overline{CS}$ falling edge. This change ensures the settling on the multiplexer output before the sample start.
12	PDEN	Digital input	This pin enables a power-down feature if it is high at the $\overline{CS}$ rising edge
13	$\overline{CS}$	Digital input	Chip select signal; active low
14	SCLK	Digital input	Serial SPI clock
15	SDO	Digital output	Serial data out
16	DVDD	Digital	Digital I/O supply

TYPICAL CHARACTERISTICS: ADS7945

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

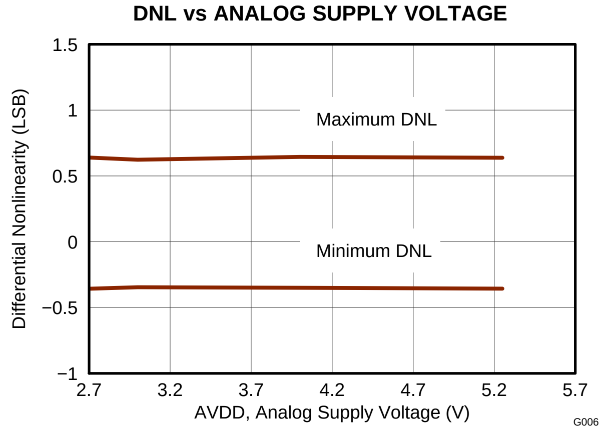


Figure 1.

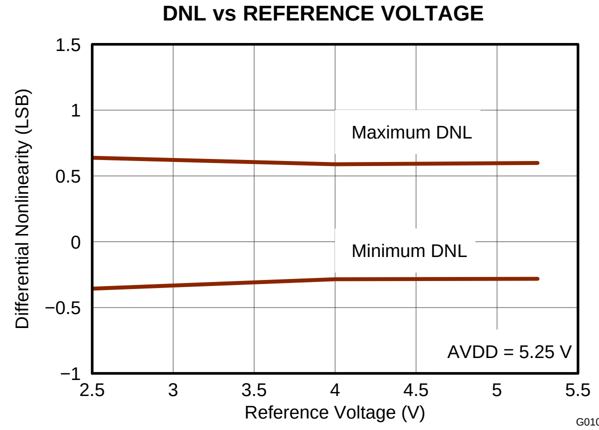


Figure 2.

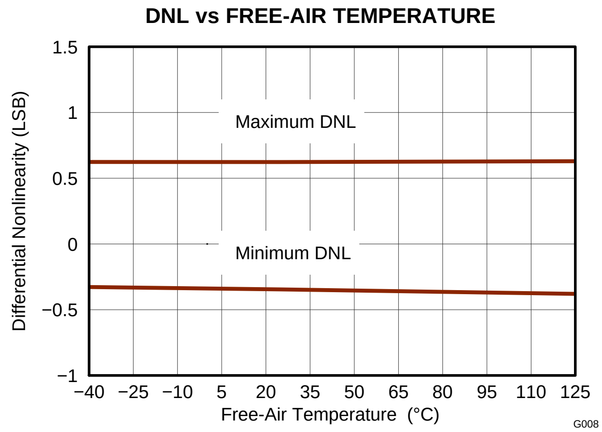


Figure 3.

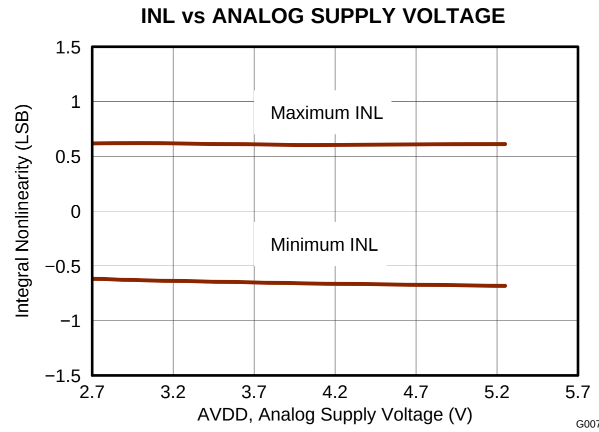


Figure 4.

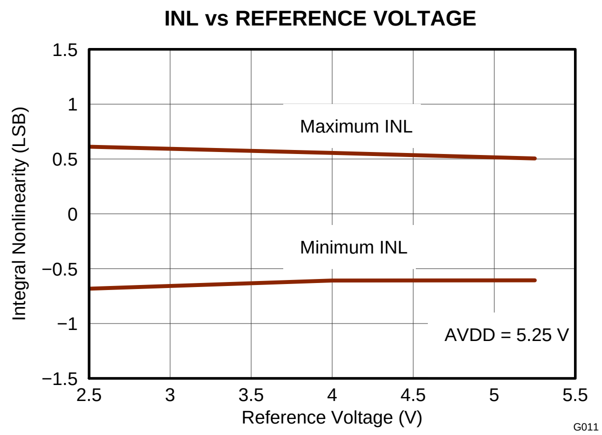


Figure 5.

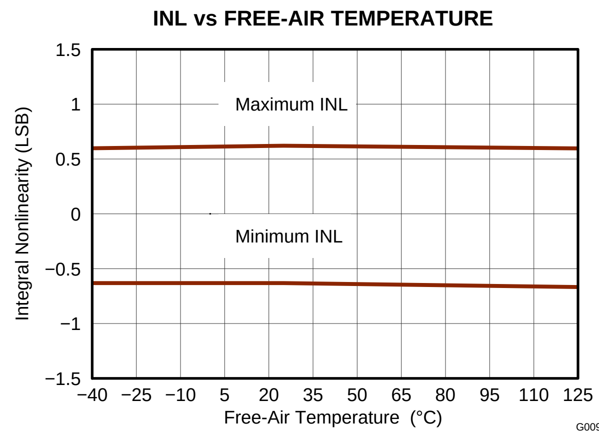


Figure 6.

TYPICAL CHARACTERISTICS: ADS7945 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

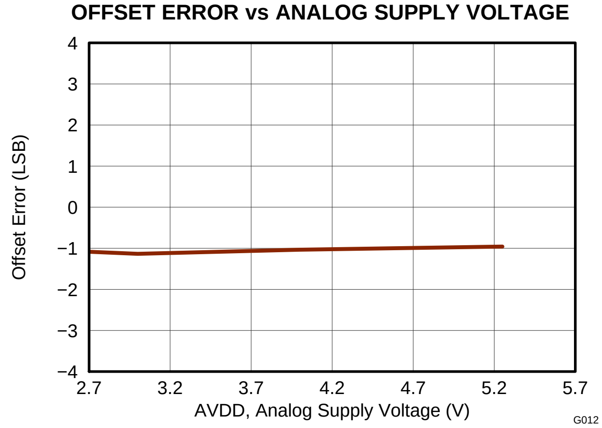


Figure 7.

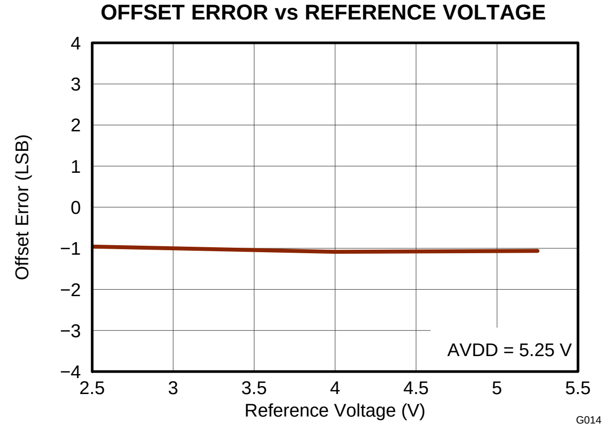


Figure 8.

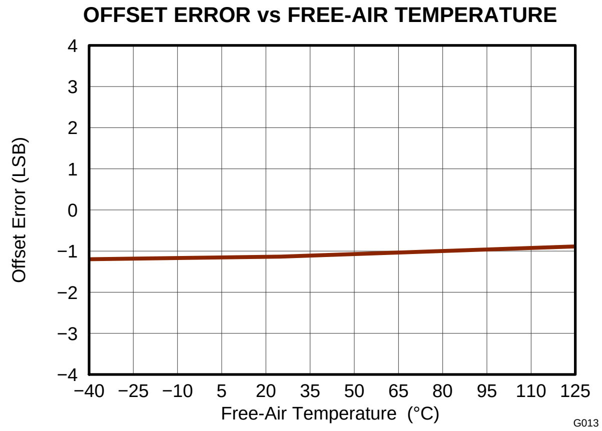
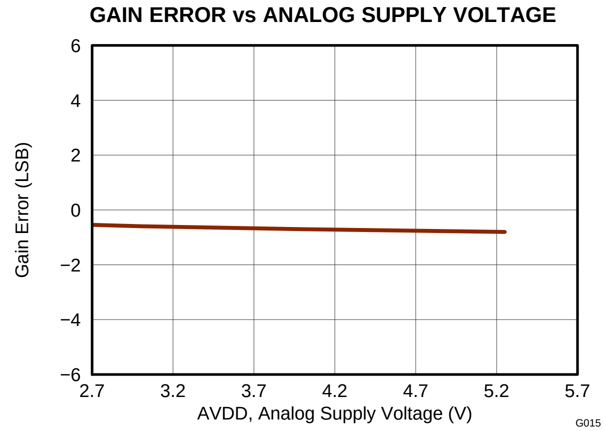


Figure 9.



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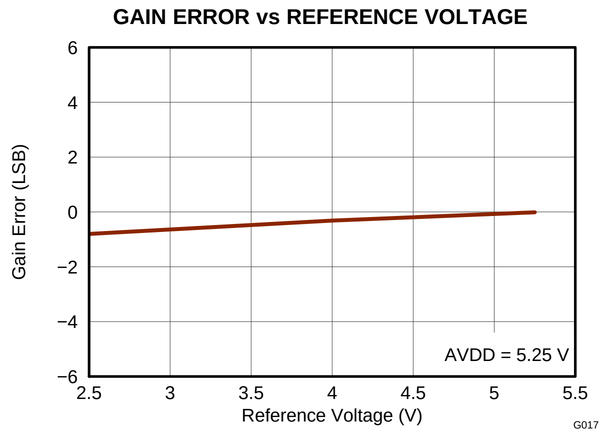


Figure 11.

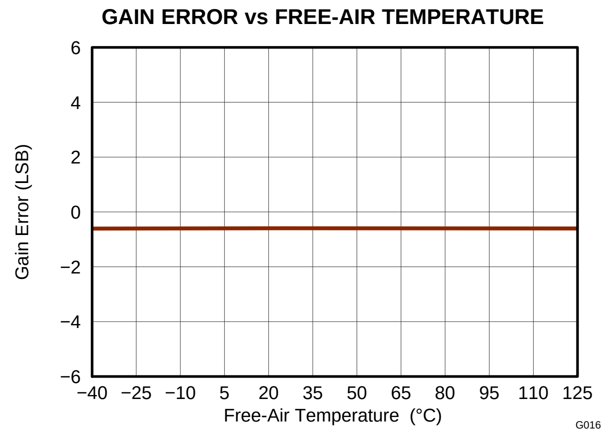


Figure 12.

TYPICAL CHARACTERISTICS: ADS7945 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

SNR vs ANALOG SUPPLY VOLTAGE

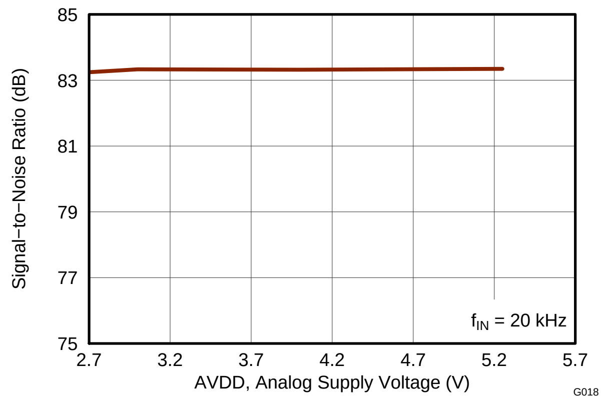


Figure 13.

SNR vs REFERENCE VOLTAGE

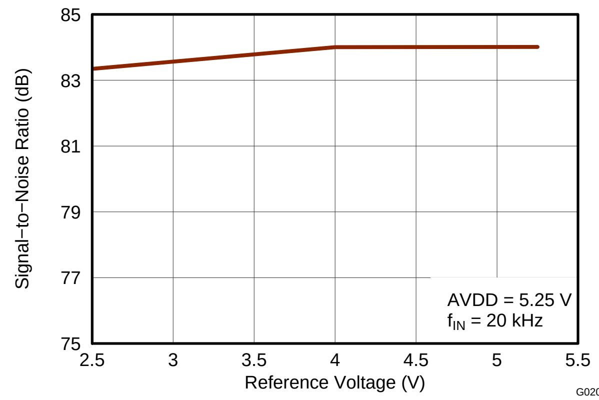


Figure 14.

SNR vs FREE-AIR TEMPERATURE

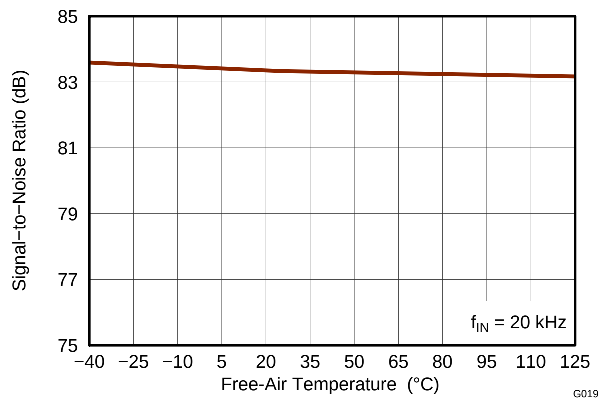


Figure 15.

SNR vs INPUT FREQUENCY

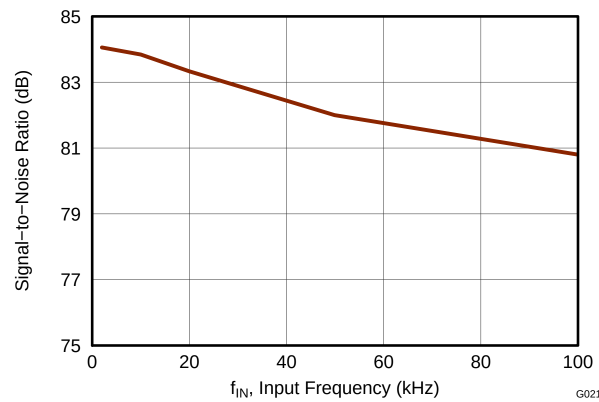


Figure 16.

SINAD vs ANALOG SUPPLY VOLTAGE

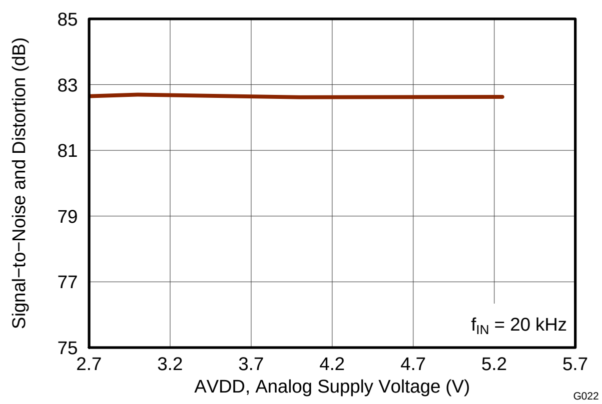


Figure 17.

SINAD vs REFERENCE VOLTAGE

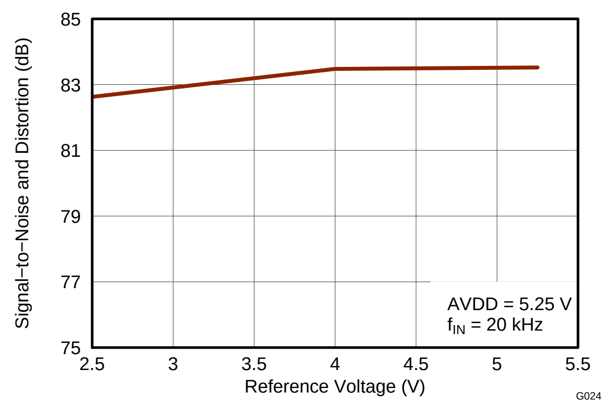


Figure 18.

TYPICAL CHARACTERISTICS: ADS7945 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

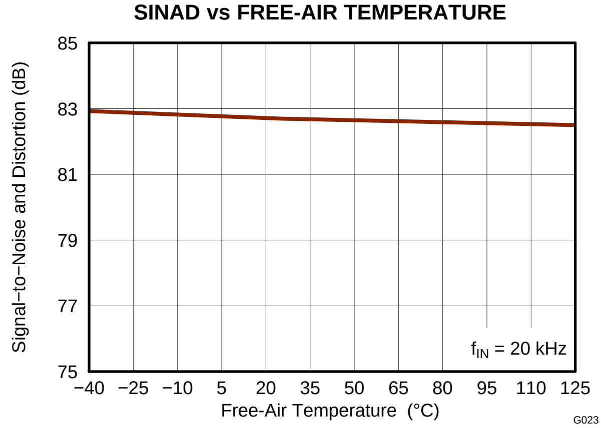


Figure 19.

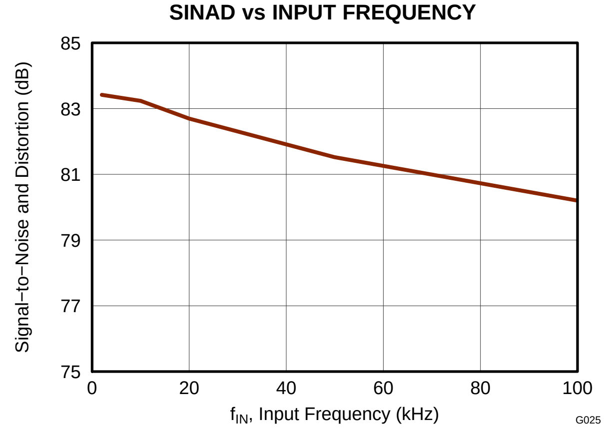


Figure 20.

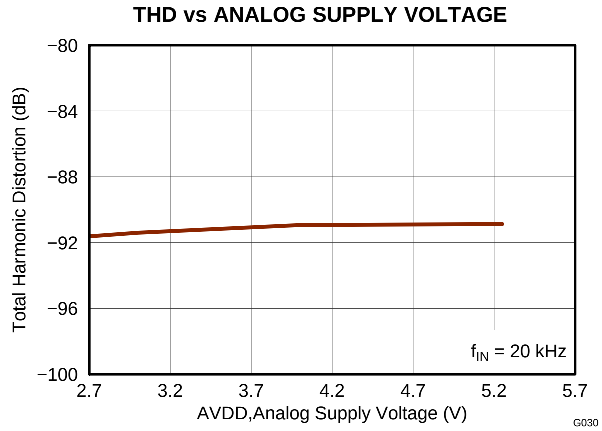


Figure 21.

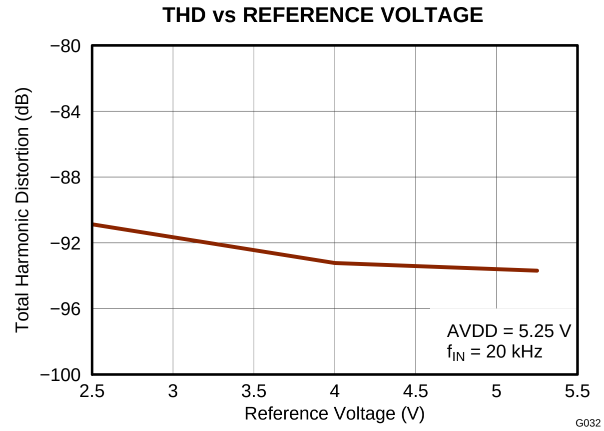


Figure 22.

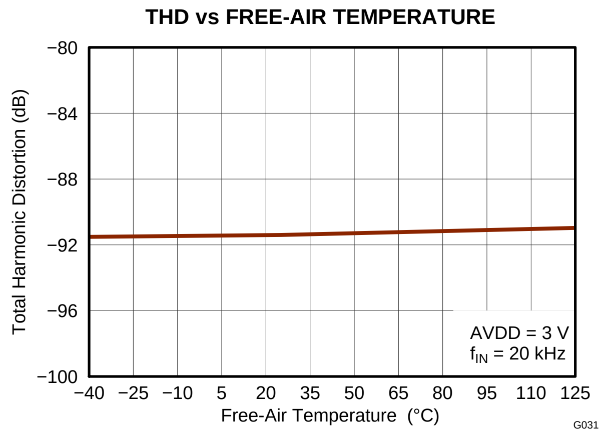


Figure 23.

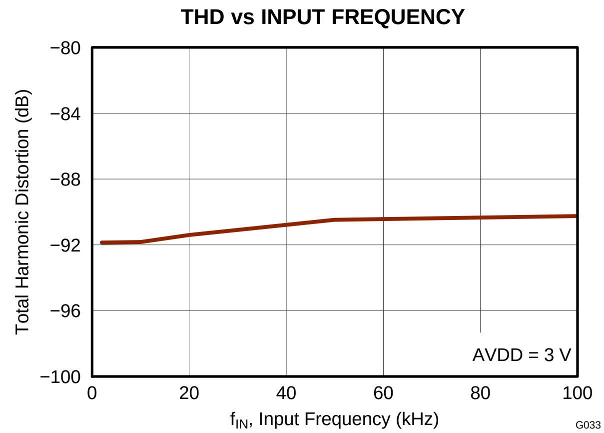


Figure 24.

TYPICAL CHARACTERISTICS: ADS7945 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

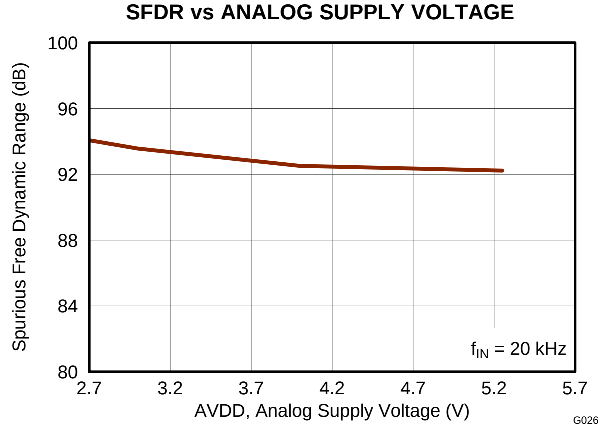


Figure 25.

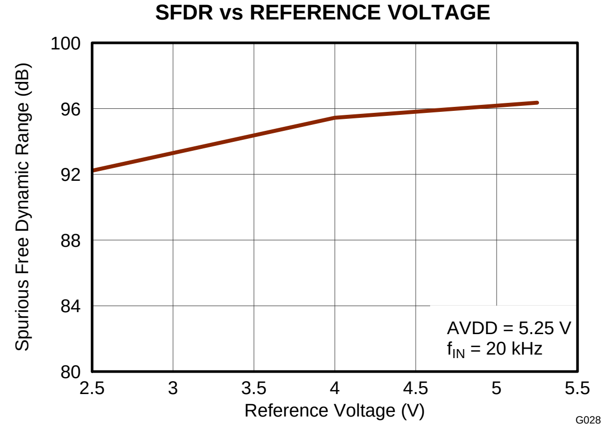


Figure 26.

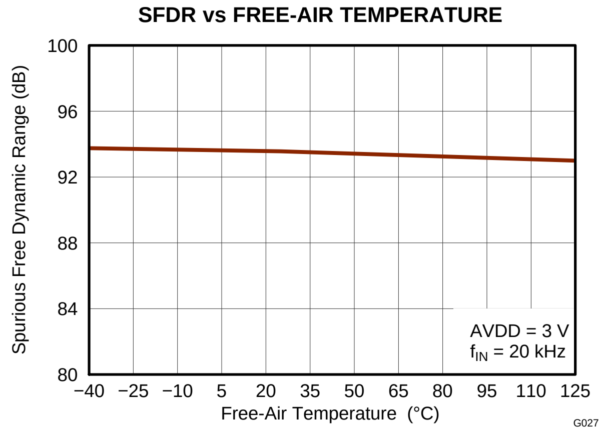


Figure 27.

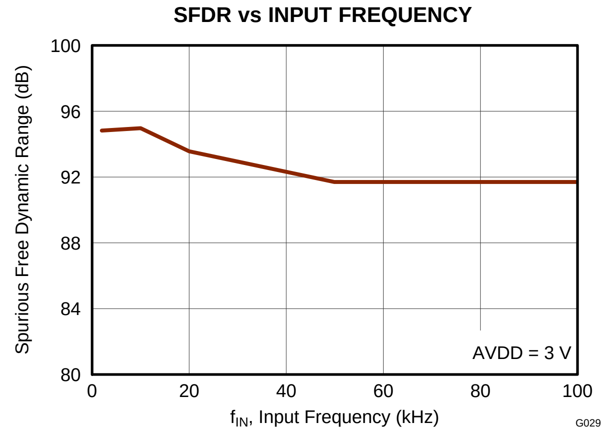


Figure 28.

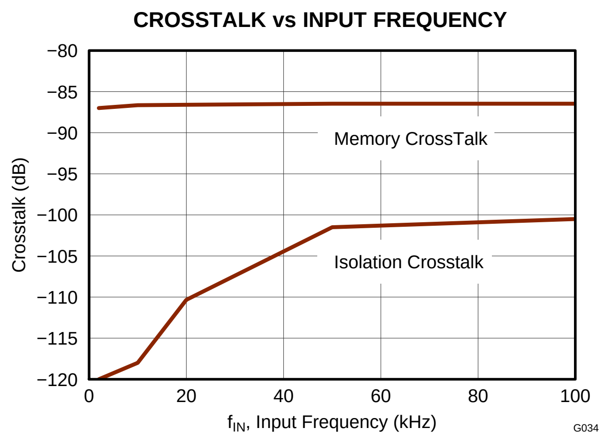


Figure 29.

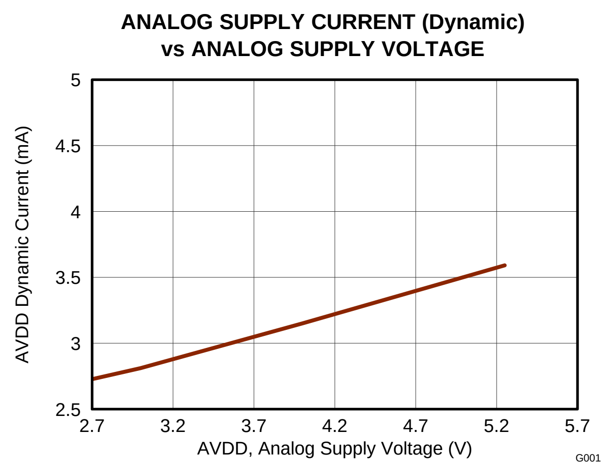


Figure 30.

TYPICAL CHARACTERISTICS: ADS7945 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

ANALOG SUPPLY CURRENT (Dynamic) vs FREE-AIR TEMPERATURE

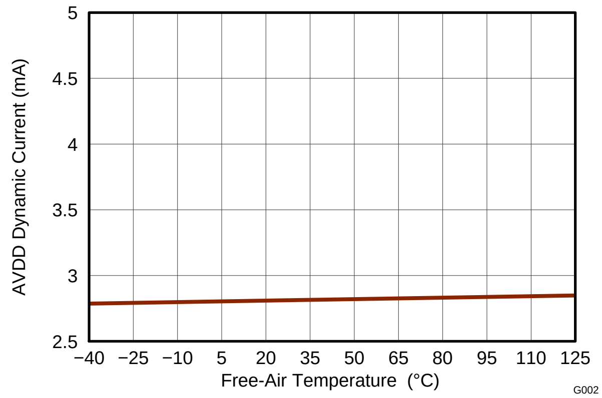


Figure 31.

ANALOG SUPPLY CURRENT (Dynamic) vs SAMPLE RATE

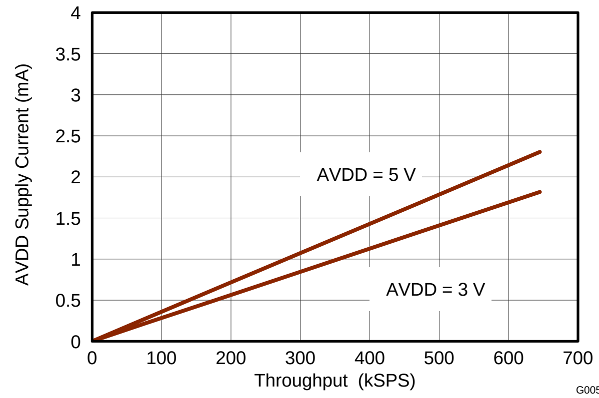


Figure 32.

ANALOG SUPPLY CURRENT (Static) vs ANALOG SUPPLY VOLTAGE

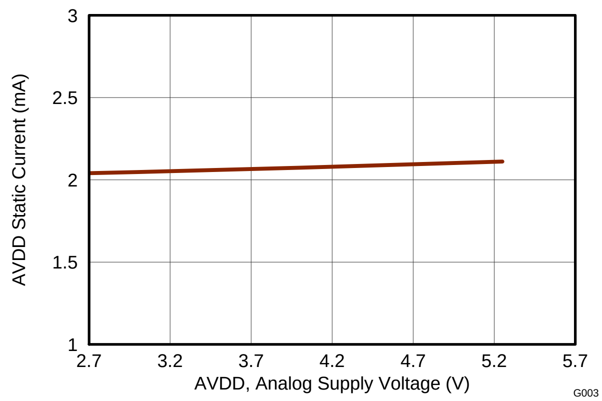


Figure 33.

ANALOG SUPPLY CURRENT (Static) vs FREE-AIR TEMPERATURE

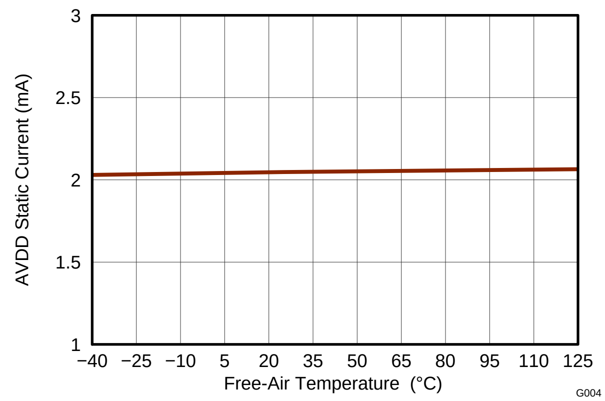


Figure 34.

DNL

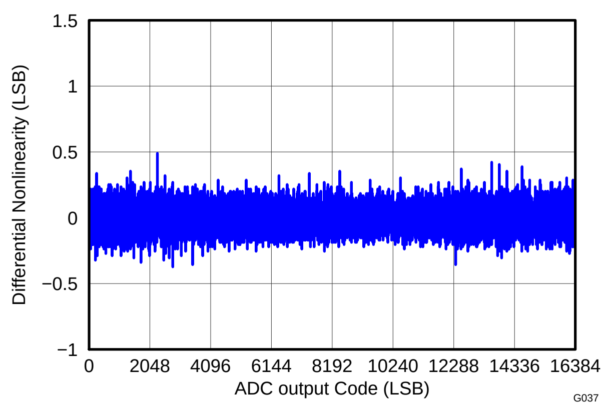


Figure 35.

INL

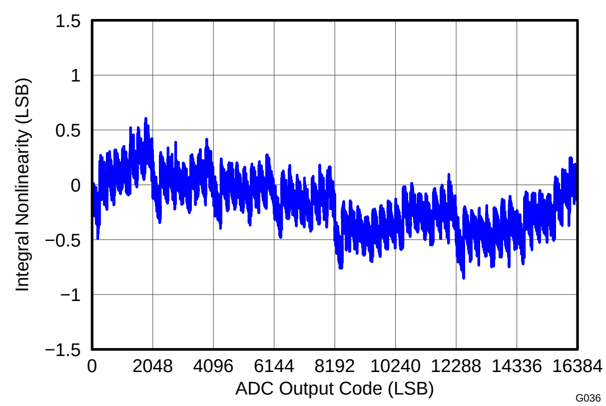


Figure 36.

TYPICAL CHARACTERISTICS: ADS7945 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

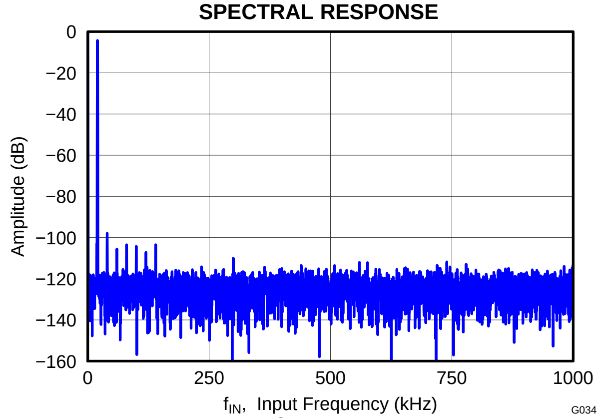


Figure 37.

TYPICAL CHARACTERISTICS: ADS7946

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

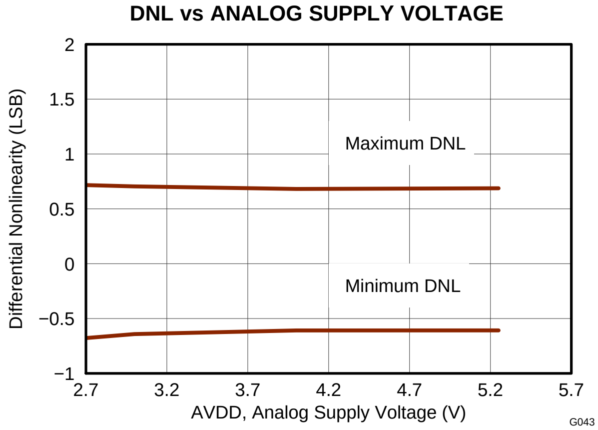


Figure 38.

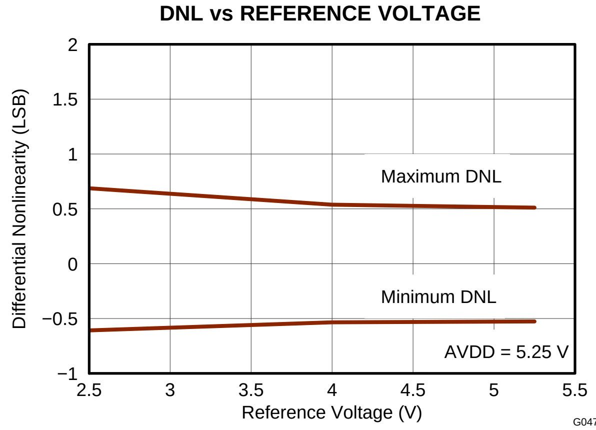


Figure 39.

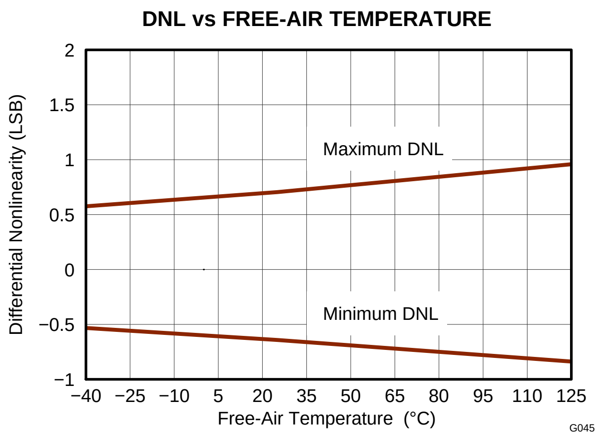
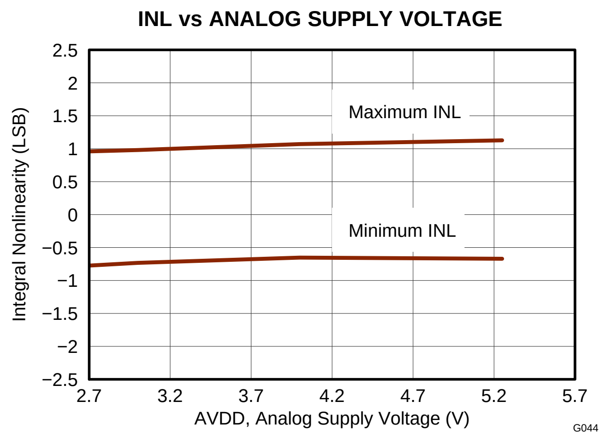


Figure 40.



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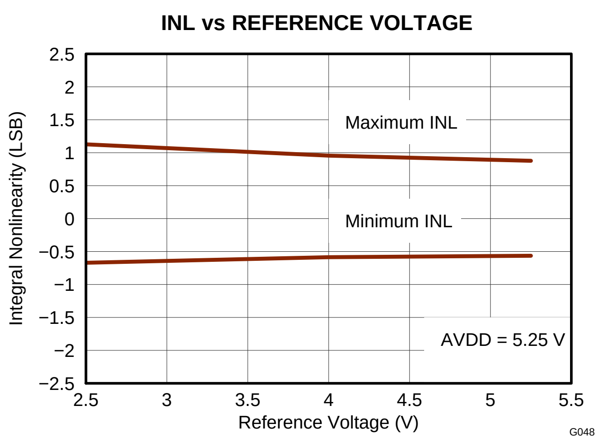


Figure 42.

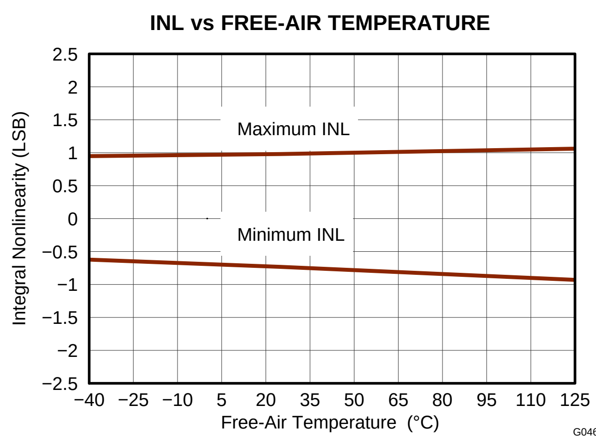
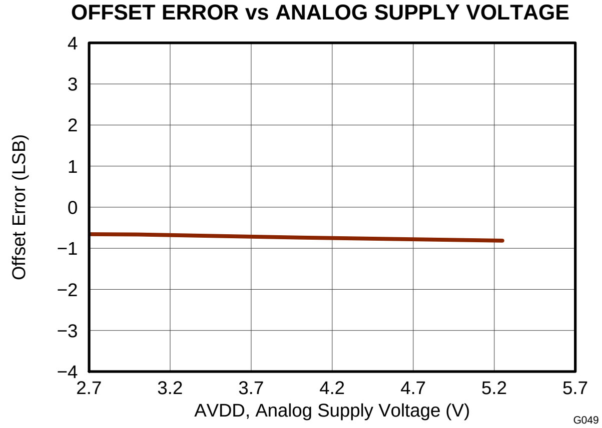


Figure 43.

TYPICAL CHARACTERISTICS: ADS7946 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.



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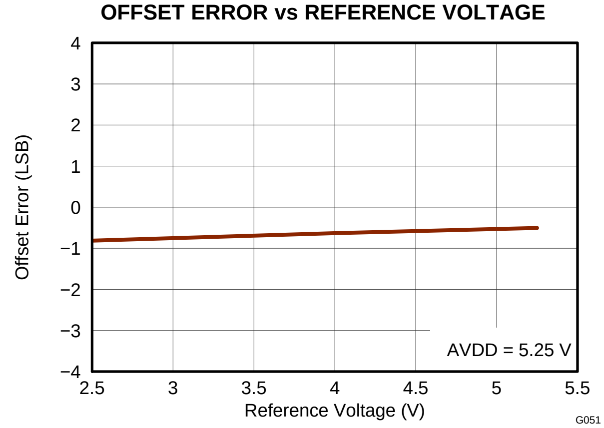


Figure 45.

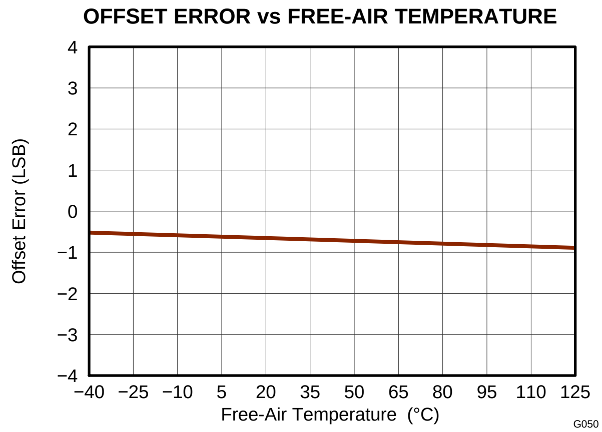


Figure 46.

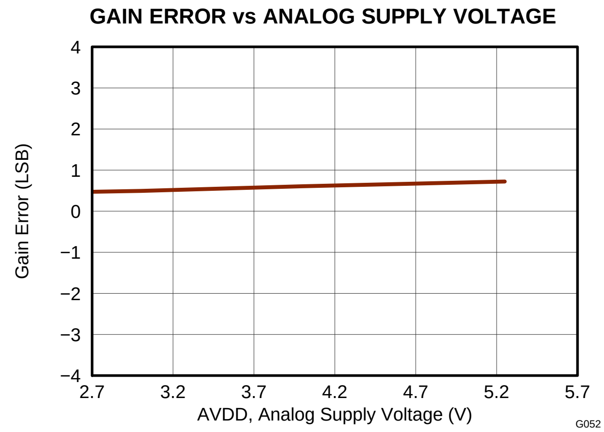


Figure 47.

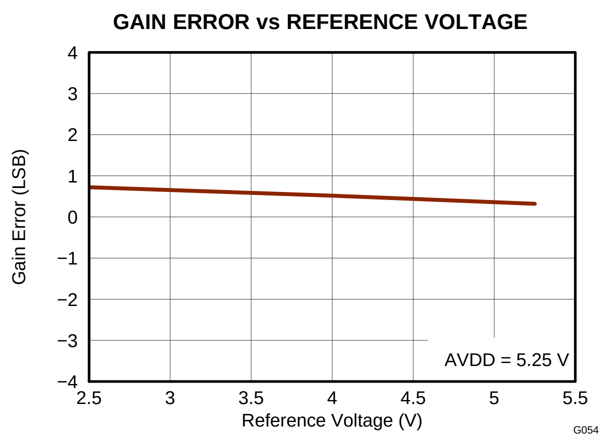


Figure 48.

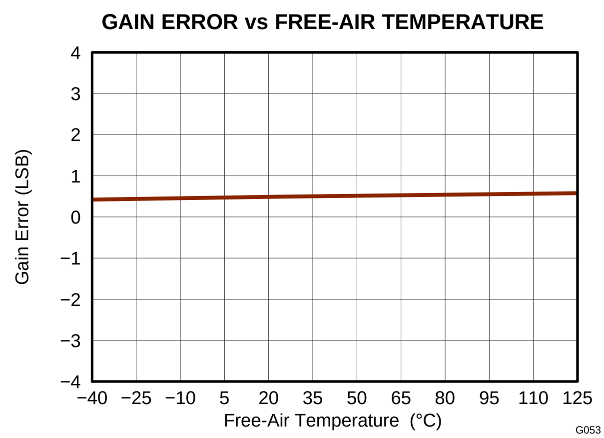


Figure 49.

TYPICAL CHARACTERISTICS: ADS7946 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

SNR vs ANALOG SUPPLY VOLTAGE

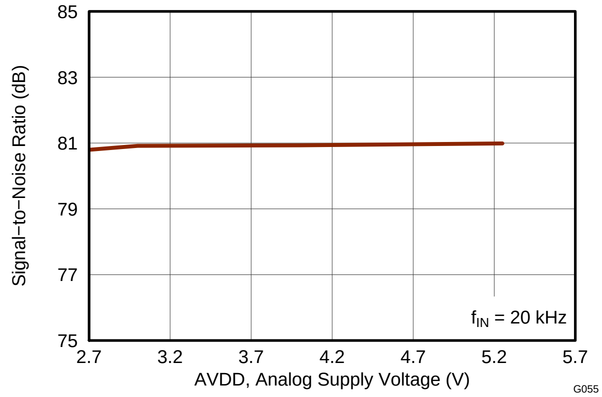


Figure 50.

SNR vs REFERENCE VOLTAGE

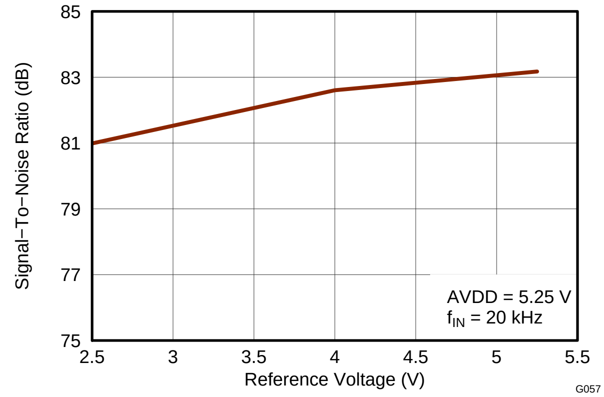


Figure 51.

SNR vs FREE-AIR TEMPERATURE

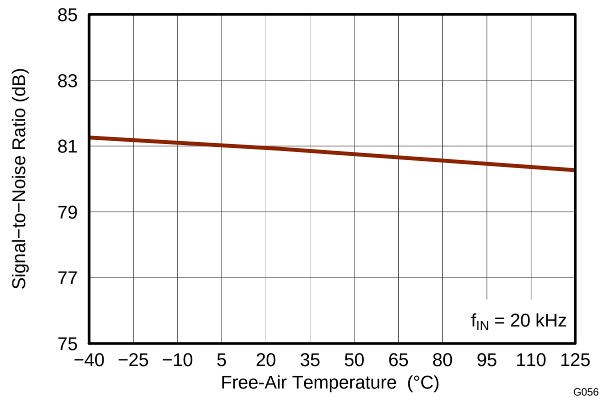


Figure 52.

SNR vs INPUT FREQUENCY

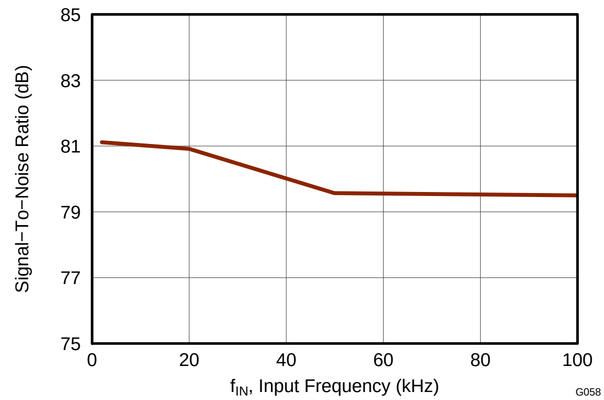


Figure 53.

SINAD vs ANALOG SUPPLY VOLTAGE

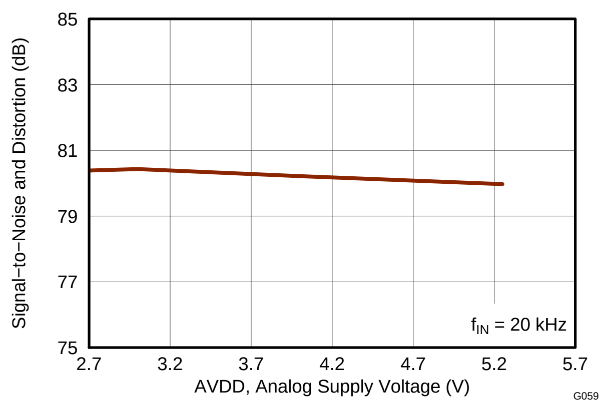


Figure 54.

SINAD vs REFERENCE VOLTAGE

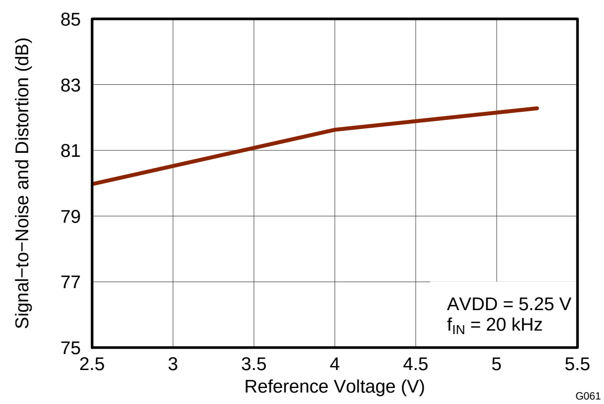


Figure 55.

TYPICAL CHARACTERISTICS: ADS7946 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

SINAD vs FREE-AIR TEMPERATURE

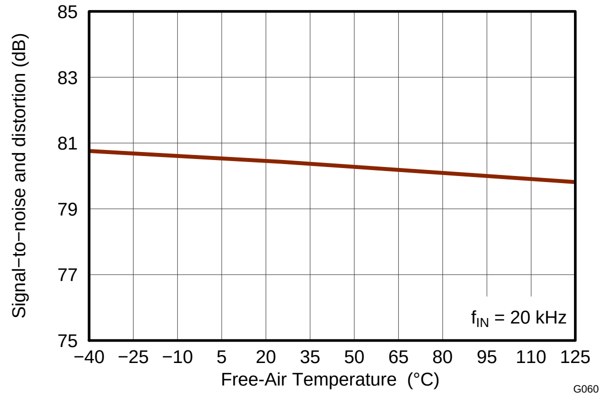


Figure 56.

SINAD vs INPUT FREQUENCY

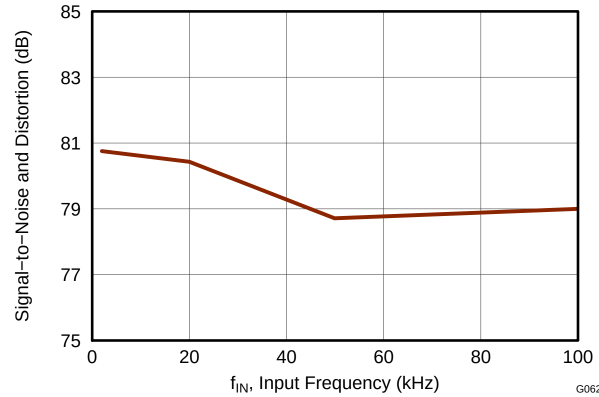


Figure 57.

THD vs ANALOG SUPPLY VOLTAGE

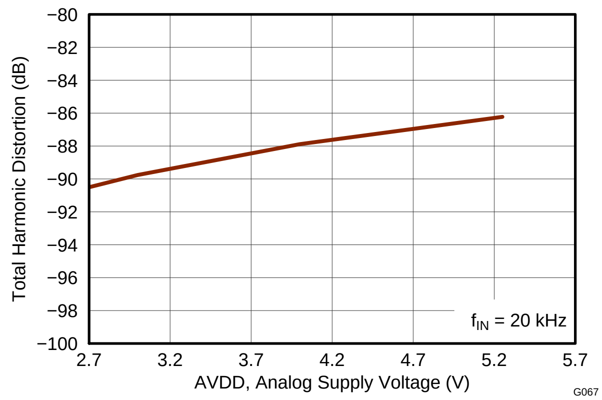


Figure 58.

THD vs REFERENCE VOLTAGE

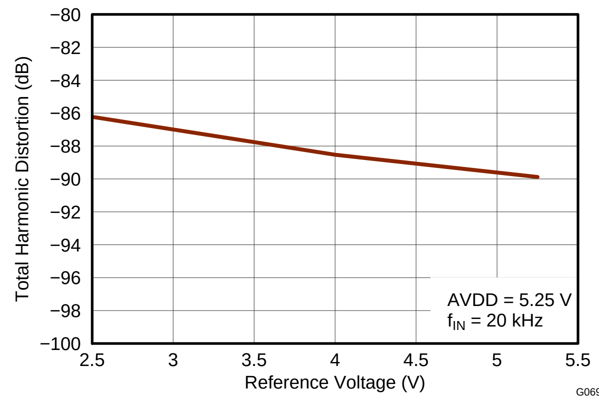


Figure 59.

THD vs FREE-AIR TEMPERATURE

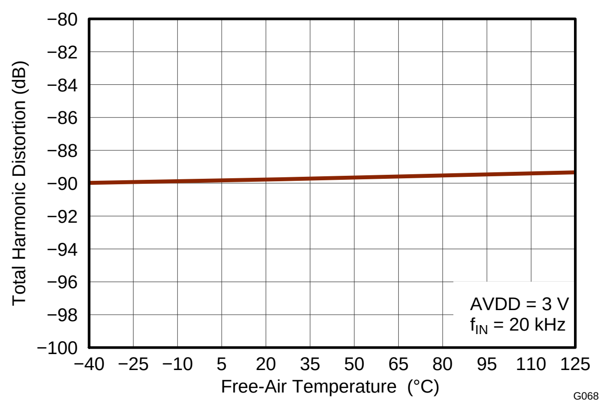


Figure 60.

THD vs INPUT FREQUENCY

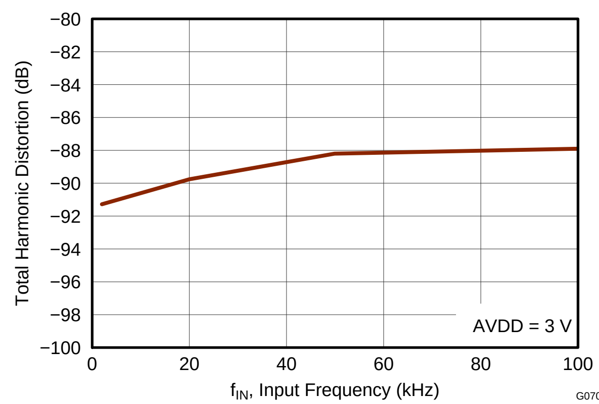


Figure 61.

TYPICAL CHARACTERISTICS: ADS7946 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

SFDR vs ANALOG SUPPLY VOLTAGE

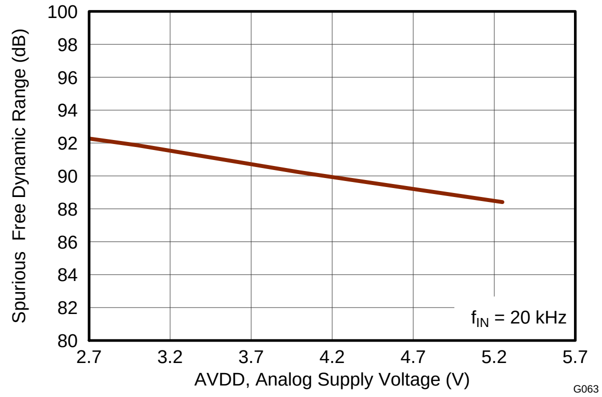


Figure 62.

SFDR vs REFERENCE VOLTAGE

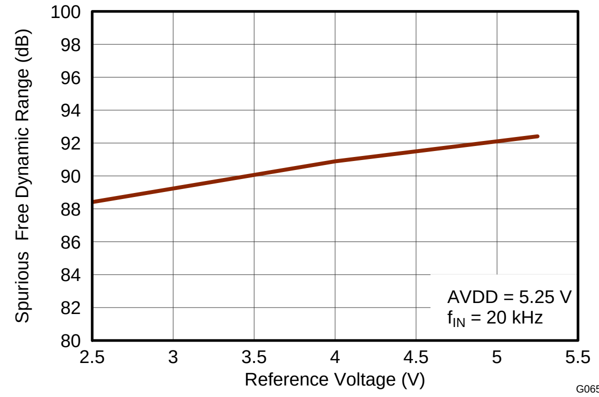


Figure 63.

SFDR vs FREE-AIR TEMPERATURE

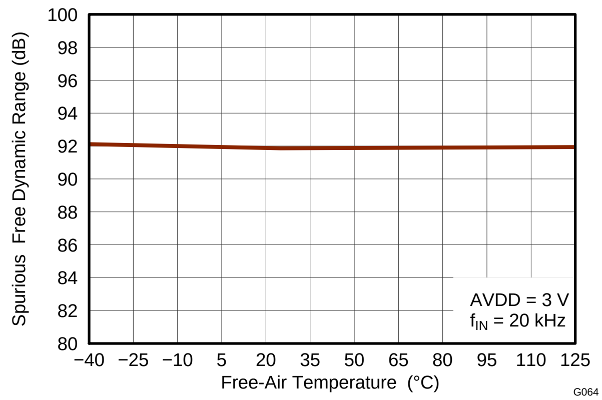


Figure 64.

SFDR vs INPUT FREQUENCY

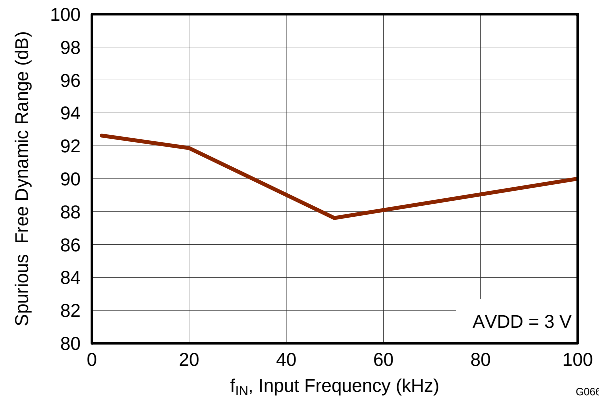


Figure 65.

CROSSTALK vs INPUT FREQUENCY

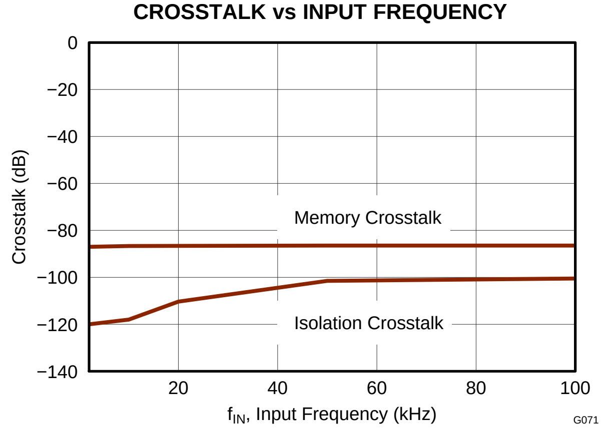


Figure 66.

ANALOG SUPPLY CURRENT (Dynamic) vs ANALOG SUPPLY VOLTAGE

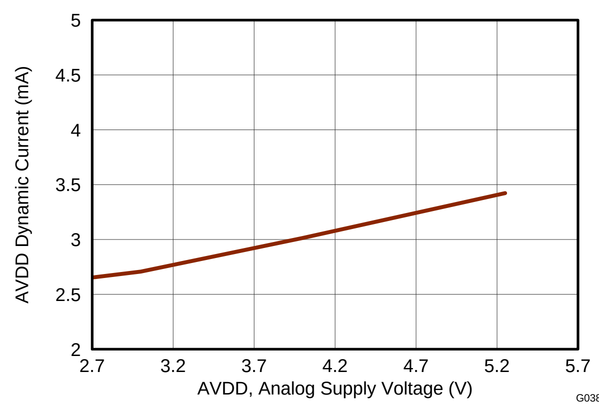


Figure 67.

TYPICAL CHARACTERISTICS: ADS7946 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

ANALOG SUPPLY CURRENT (Dynamic) vs FREE-AIR TEMPERATURE

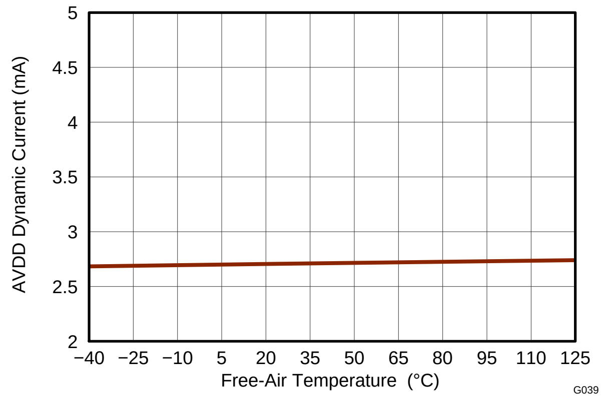


Figure 68.

ANALOG SUPPLY CURRENT (Dynamic) vs SAMPLE RATE

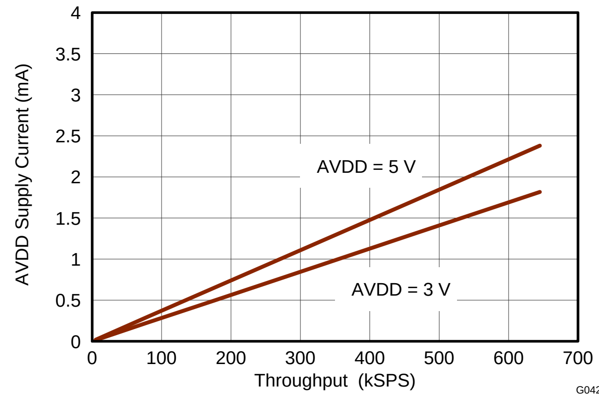


Figure 69.

ANALOG SUPPLY CURRENT (Static) vs ANALOG SUPPLY VOLTAGE

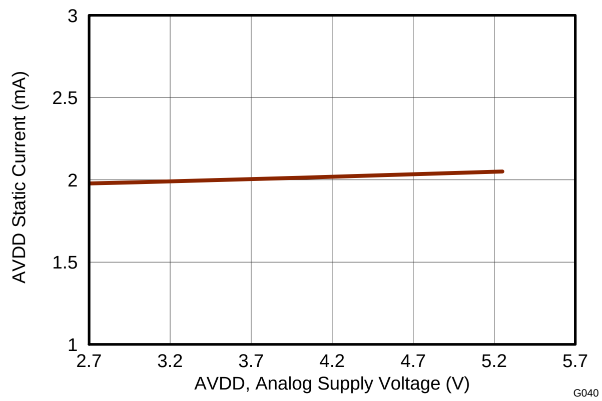


Figure 70.

ANALOG SUPPLY CURRENT (Static) vs FREE-AIR TEMPERATURE

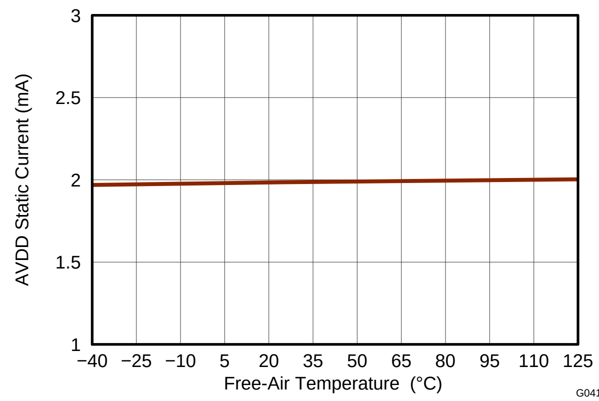


Figure 71.

DNL

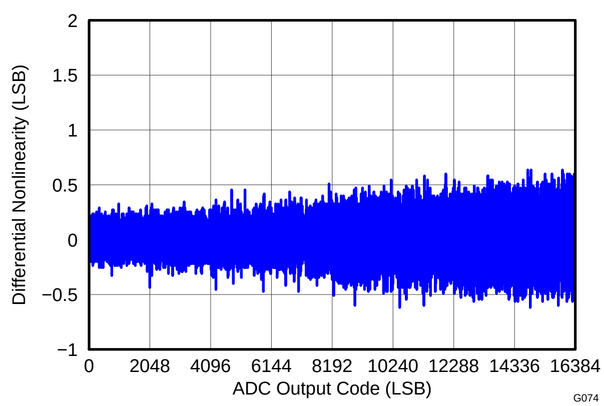


Figure 72.

INL

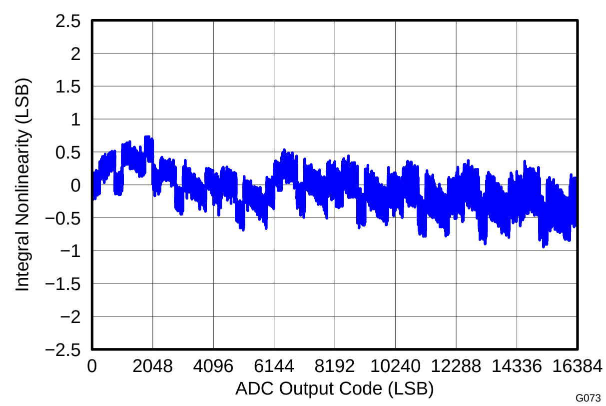


Figure 73.

TYPICAL CHARACTERISTICS: ADS7946 (continued)

At T_A = +25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and f_{SAMPLE} = 2 MSPS, unless otherwise noted.

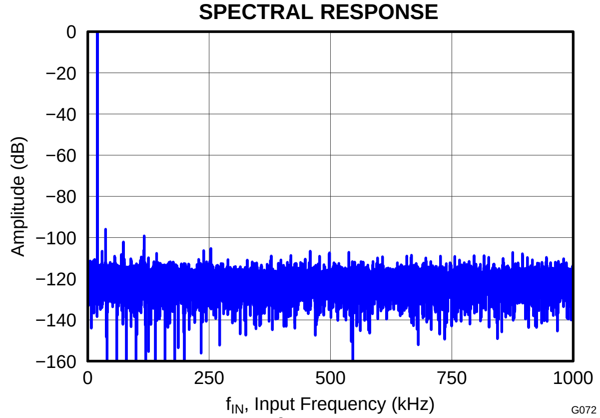


Figure 74.

OVERVIEW

The ADS7945 and ADS7946 are 14-bit, miniature, dual-channel, low-power SAR ADCs. The ADS7945 is a differential input device and the ADS7946 is a single-ended device with ground sensing input. These devices feature very low power consumption at rated speed. The PDEN pin enables an auto power-down mode that further reduces power consumption at lower speeds.

MULTIPLEXER AND ADC INPUT

The ADS7945/46 devices feature differential/single-ended inputs respectively with a double-pole, double-throw multiplexer. The analog input circuit shown in Figure 75 is similar for for ADS7945 and ADS7946.

The ADS7945 features a differential input. Each of the positive (AINxP) and negative (AINxN) inputs can swing from –V_{REF}/2 to +V_{REF}/2 around the common-mode voltage (AINxP + AINxN)/2 so that AINxP and AINxN swing in opposite directions equally from common-mode voltage (differential input swing V_{AINxP} – V_{AINxN} ranges from –V_{REF} to +V_{REF}). The ADC converts the difference in voltage: V_{AINxP} – V_{AINxN}. This feature allows the devices to reject the common-mode noise in the input signal.

For the ADS7946, the ground sense inputs (AINxGND) can accept swings of ±0.2 V whereas the inputs (AINx) allow signals in the range of 0 V to V_{REF} over the ground sense input. The ADC converts the difference in voltage: V_{AINx} – $V_{AINxGND}$. This feature can be used in multiple ways. For example, two signals can be connected from different sensors with unequal ground potentials (within ±0.2 V) to a single ADC. The ADC rejects the common-mode offset and noise. This feature also allows the use of a single-supply op amp. The signal and the AINxGND input can be offset by +0.2 V, which provides the ground clearance required for a single-supply op amp.

Figure 75 shows the electrostatic discharge (ESD) diodes to supply and ground at every analog input. Make sure that these diodes do not turn on by keeping the supply voltage within the specified input range.

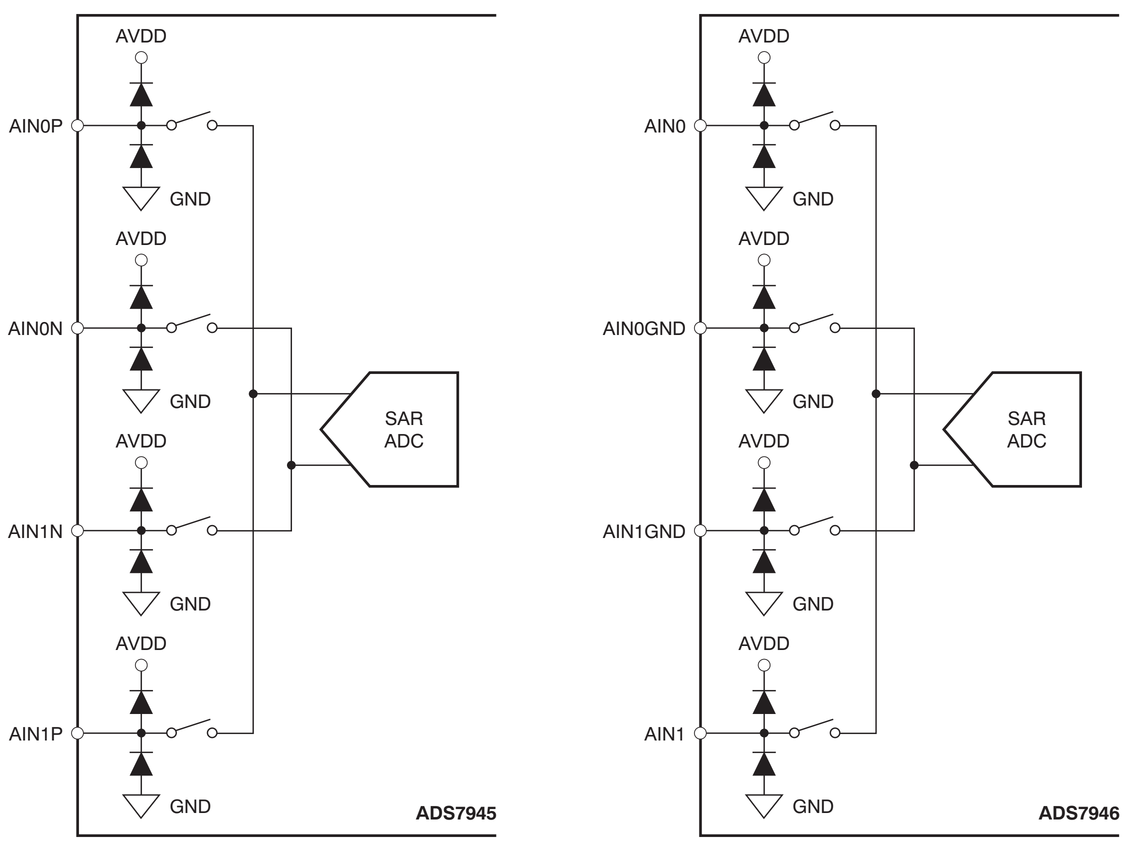


Figure 75. Analog Inputs

Figure 76 shows an equivalent circuit of the multiplexer and ADC sampling stage. See the *Application Information* section for details on the driving circuit. The positive and negative/ground sense inputs are separately sampled on 32 pF sampling capacitors. The multiplexer and sampling switches are represented by an ideal switch in series with a 12 Ω resistance. Note that this is dc resistance and can be used for step-settling calculations (do not use the RC values shown in Figure 76 for 3 dB bandwidth calculations for undersampling applications). During sampling, the devices connect the 32 pF sampling capacitor to the ADC driver. This connection creates a glitch at the device input. It is recommended to connect a capacitor across the AINxP and AINxN terminals or AINx and AINxGND terminals to reduce this glitch for the ADS7945 or ADS7946, respectively. A driving circuit must have sufficient bandwidth to settle this glitch within the acquisition time.

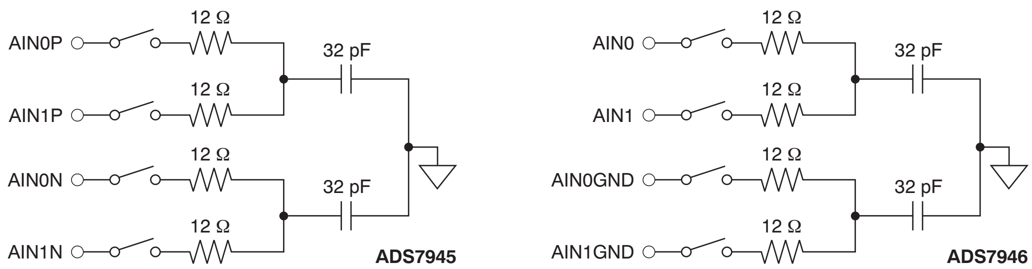


Figure 76. Input Sampling Stage Equivalent Circuit

Figure 77 shows a timing diagram for the ADC analog input channel selection. As shown in Figure 77, the CH SEL signal selects the analog input channel to the ADC. CH SEL = 0 selects channel 0 and CH SEL = 1 selects channel 1. It is recommended not to toggle the CH SEL signal during an ADC acquisition phase until the device sees the first valid SCLK rising edge after the device samples the analog input. If CH SEL is toggled during this period, it can cause erroneous output code because the device might see unsettled analog input.

CH SEL can be toggled at any time during the window specified in Figure 77; however, it is recommended to select the desired channel after the first SCLK rising edge and before the second SCLK rising edge. This timing ensures that the multiplexer output is settled before the ADC starts acquisition of the analog input.

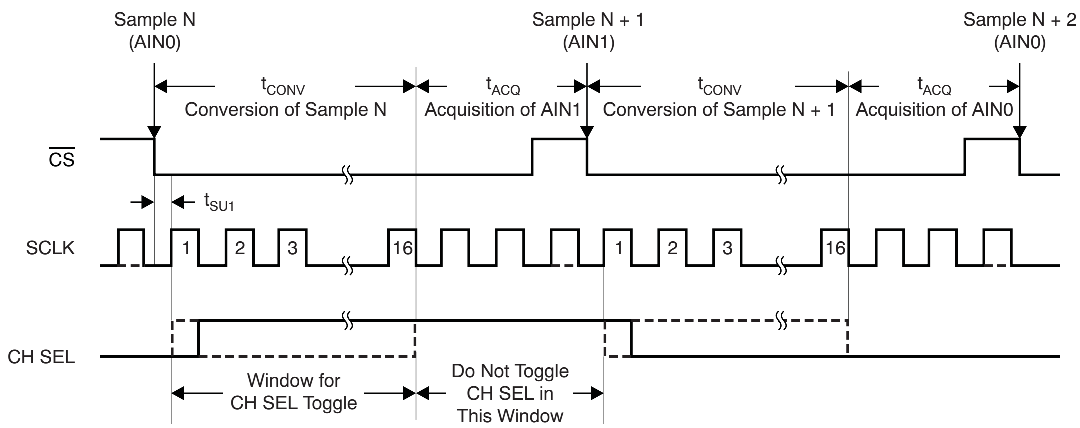
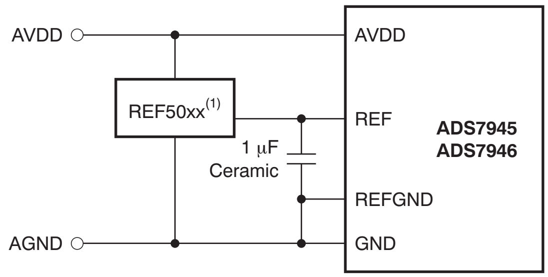


Figure 77. ADC Analog Input Channel Selection

REFERENCE

The ADS7945/6 use an external reference voltage during the conversion of a sampled signal. The devices switch the capacitors used in the conversion process to the reference terminal during conversion. The switching frequency is the same as the SCLK frequency. It is necessary to decouple the REF terminal to REFGND with a 1 μF ceramic capacitor in order to get the best noise performance from the device. The capacitor must be placed closest to these pins. The reference input can be driven with the REF50xx series precision references from TI. Figure 78 shows a typical reference driving circuit.

Sometimes it is convenient to use AVDD as a reference. The ADS7945/6 allow reference ranges up to AVDD. However, make sure that AVDD is well-bypassed and that there is a separate bypass capacitor between REF and REFGND.



(1) Select the appropriate device as described by the required reference value. For example, select the REF5040 for a 4 V reference, the REF5030 for a 3 V reference, and the REF5025 for a 2.5 V reference. Ensure that (AVDD – REF) > 0.2 V so that the REF50xx functions properly.

Figure 78. Typical Reference Driving Circuit

CLOCK

The ADS7945/6 use SCLK for conversions (typically 40 MHz). A lower frequency SCLK can be used for applications that require sample rates less than 2 MSPS. However, it is better to use a 40 MHz SCLK and slow down the device speed by choosing a lower frequency for $\overline{CS}$, which allows more acquisition time. This configuration relaxes constraints on the output impedance of the driving circuit. Refer to the *Application Information* section for calculation of the driving circuit output impedance.

ADC TRANSFER FUNCTION

The ADS7945 is a differential input device and the ADS7946 is a single-ended input device. This section describes the transfer characteristics for both devices.

The ADS7945 output is in twos compliment format. Figure 79 shows the ideal transfer characteristics for these devices. Here, full-scale range for the ADC input (AINxP – AINxN) is equal to twice the reference input voltage to the ADC 2 × (V_{REF}). 1 LSB is equal to 2 × ($V_{REF}/2^N$), where N is the resolution of the ADC (N = 14 for the ADS7945). The differential input of the ADC is bipolar around the common-mode voltage (AINxP + AINxN)/2 and has a range of positive FSR (+V_{REF}) to negative FSR (–V_{REF}).

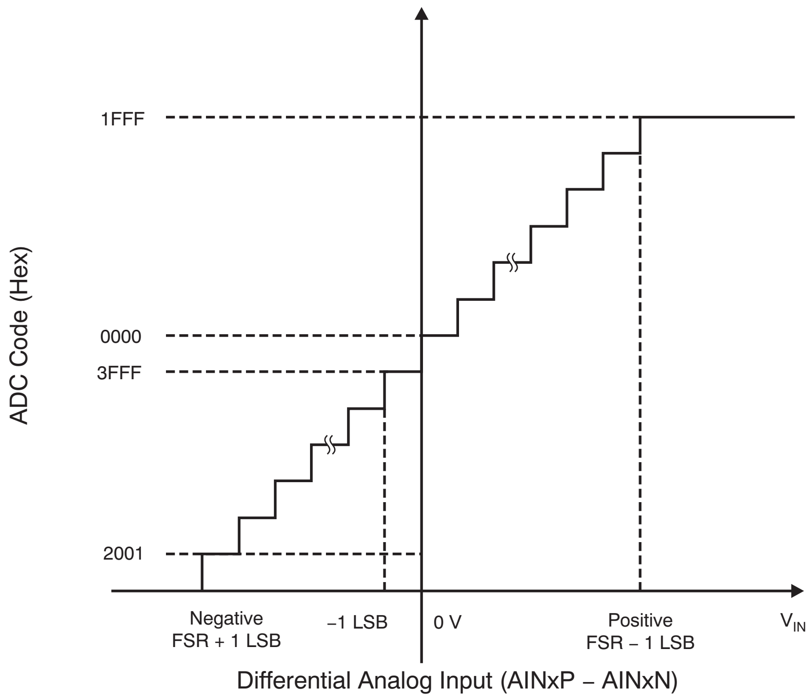


Figure 79. ADS7945 Transfer Characteristics

The ADS7946 output is in straight binary format. Figure 80 shows ideal transfer characteristics for this device. Here, FSR is the full-scale range for the ADC input (AINx – AINxGND) and is equal to the reference input voltage to the ADC (V_{REF}). 1 LSB is equal to ($V_{REF}/2^N$), where *N* is the resolution of the ADC (N = 14 for the ADS7946).

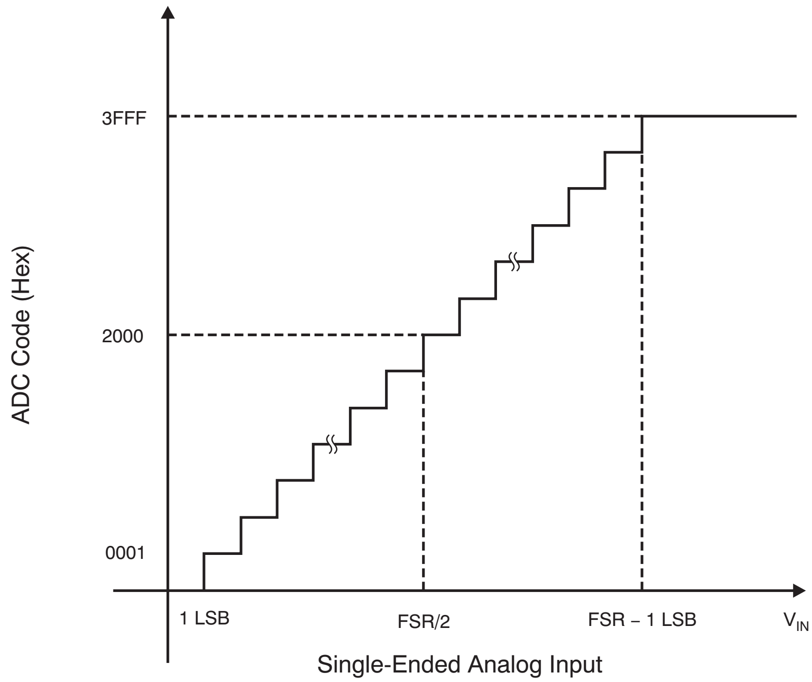


Figure 80. ADS7946 Transfer Characteristics

DEVICE OPERATION

The ADS7945/6 operate with either a 16-clock frame or 32-clock frame for ease of interfacing with the host processor.

16-CLOCK FRAME

Figure 81 shows the devices operating in 16-clock mode. This mode is the fastest mode for device operation. In this mode, the devices output data from previous conversions while converting the recently sampled signal.

As shown in Figure 81, the ADS7945/6 start acquisition of the analog input from the 16th falling edge of SCLK. The device samples the input signal on the $\overline{\text{CS}}$ falling edge. SDO comes out of 3-state and the device outputs the MSB on the $\overline{\text{CS}}$ falling edge. The device outputs the next lower SDO bits on every SCLK falling edge after it has first seen the SCLK rising edge. The data correspond to the sample and conversion completed in the previous frame. During a $\overline{\text{CS}}$ low period, the device converts the recently sampled signal. It uses SCLK for conversions. Conversion is complete on the 16th SCLK falling edge. $\overline{\text{CS}}$ can be high at any time after the 16th SCLK falling edge (see the *Parameter Measurement Information* for more details). The $\overline{\text{CS}}$ rising edge after the 16th SCLK falling edge and before the 29th SCLK falling edge keeps the device in the 16-clock data frame. The device output goes to 3-state when $\overline{\text{CS}}$ is high. It is also permissible to stop SCLK after the device has seen the 16th SCLK falling edge.

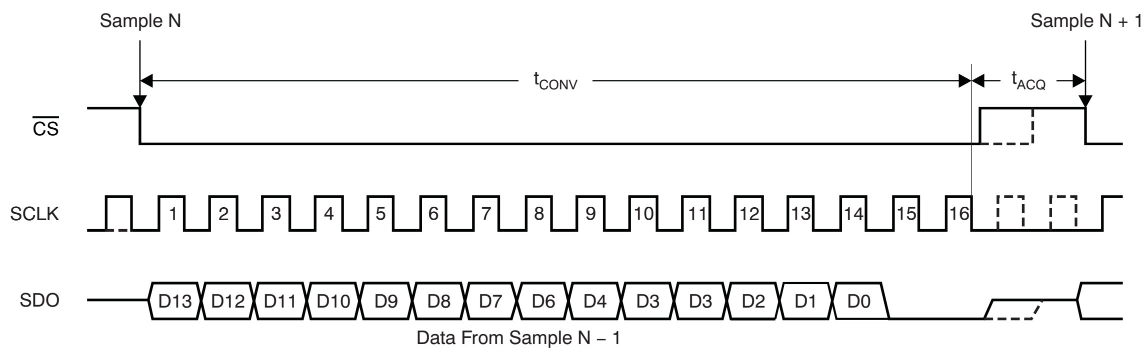


Figure 81. ADS7945/6 Operating in 16-Clock Mode without Power-Down (PDEN = 0)

32-CLOCK FRAME

Figure 82 shows the devices operating in 32-clock mode. In this mode, the devices convert and output the data from the most recent sample before taking the next sample.

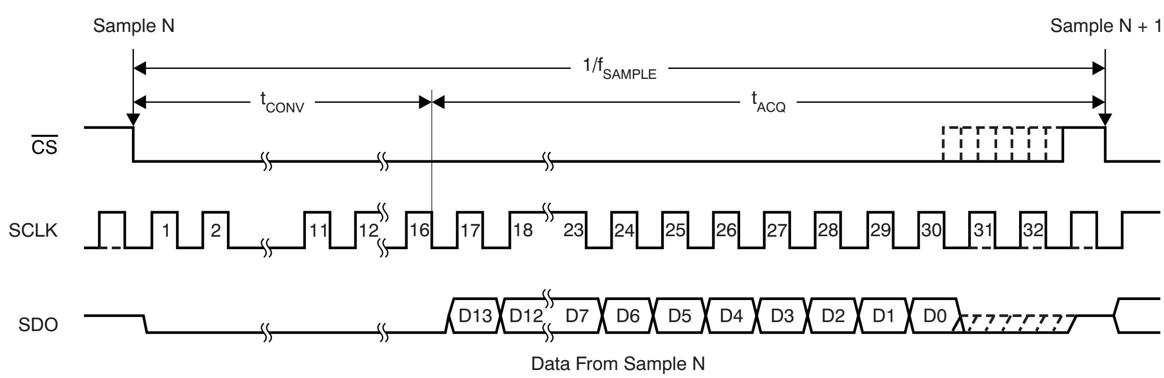


Figure 82. ADS7945/6 Operation in 32-Clock Frame without Power-Down (PDEN = 0)

$\overline{CS}$ can be held low past the 16th falling edge of SCLK. The devices continue to output recently converted data starting with the 16th SCLK falling edge. If $\overline{CS}$ is held low until the 30th SCLK falling edge, then the devices detect 32-clock mode. Note that the device data from recent conversions are already output with no latency before the 30th SCLK falling edge. Once 32-clock mode is detected, the device outputs 16 zeros during the next conversion (in fact, for the first 16 clocks), unlike 16-clock mode where the devices output the previous conversion result. SCLK can be stopped after the devices have seen the 30th falling edge with $\overline{CS}$ low.

CONVERSION ABORT

For some event triggered applications such as latching position of absolute position sensor on marker or homing pulse, it is essential to abort ongoing conversion on event and quickly start fresh acquisition. ADS794X features conversion abort function. $\overline{CS}$ high during conversion (during first 16 clocks) will abort ongoing conversion and start fresh acquisition. Device will sample acquired signal during $\overline{CS}$ high period on falling edge of $\overline{CS}$ and will start conversion normally, however data on SDO (conversion results from aborted frame) will not be valid.

For example if conversion is aborted during 'n^{th}' frame and (n+1) is first valid frame after conversion abort. SDO data during frame number (n+1) (corresponding to n^{th} conversion) will not be valid. Conversion results for sample and conversion during frame number (n+1) will be available in frame number (n+2).

POWER-DOWN

The ADS7945/6 devices offer an easy-to-use power-down feature available through a dedicated PDEN pin (pin 12). A high level on PDEN at the $\overline{CS}$ rising edge enables the power-down mode for that particular cycle. Figure 83 to Figure 85 illustrate device operation with power-down in both 32-clock and 16-clock mode.

Many applications must slow device operation. For speeds below approximately 500 kSPS, it is convenient to use 32-clock mode with power-down. This configuration results in considerable power savings.

As shown in Figure 83, PDEN is held at a logic '1' level. Note that the device looks at the PDEN status only at the $\overline{CS}$ rising edge; however, for continuous low-speed operation, it is convenient to continuously hold PDEN = 1. The devices detect power-down mode on the $\overline{CS}$ rising edge with PDEN = 1.

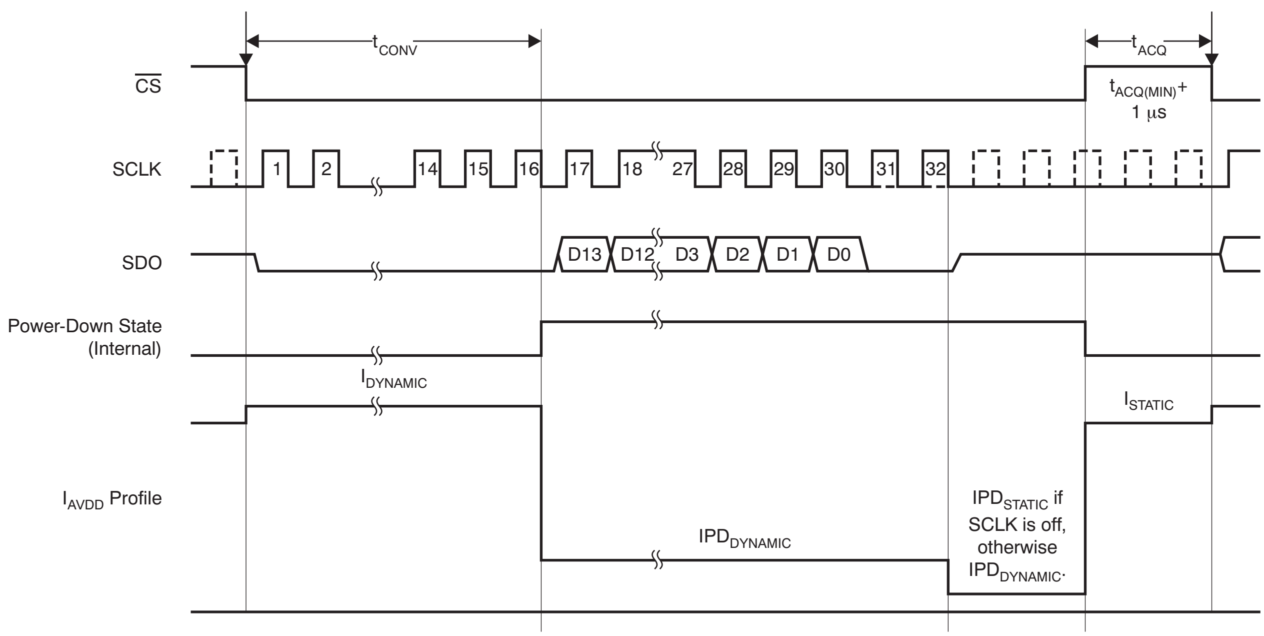


Figure 83. Operation with a 32-Clock Frame in Power-Down Mode (PDEN = 1)

On the $\overline{CS}$ falling edge, the devices start normal operation as previously described. The devices complete conversions on the 16th SCLK falling edge. The devices enter the power-down state immediately after conversions complete. However, the devices can still output data as per the timings described previously. The devices consume dynamic power-down current ($I_{PD\text{-}DYNAMIC}$) during data out operations. It is recommended to stop the clock after the 32nd SCLK falling edge to further save power down to the *static power-down current* level ($I_{PD\text{-}STATIC}$). The devices power up again on the SCLK rising edge. However, they require an extra 1 μs to power up completely. $\overline{CS}$ must be high for the 1 μs + t_{ACQ} (min) period.

In some applications, data collection is accomplished in burst mode. The system powers down after data collection. 16-clock mode is convenient for these applications. Figure 84 and Figure 85 detail power saving in 16-clock burst mode.

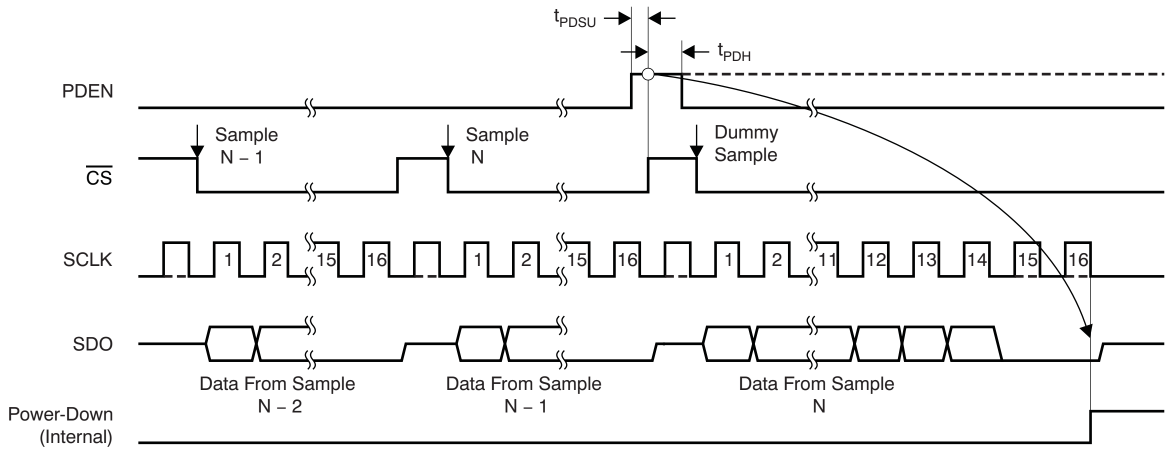


Figure 84. Entry Into Power-Down with 16-Clock Burst Mode

As shown in Figure 84, the two frames capturing the *N–1* and *Nth* samples are normal 16-clock frames. Keeping PDEN = 1 before the $\overline{CS}$ rising edge in the next frame ensures that the devices detect the power-down mode. Data from the Nth sample are read during this frame. It is expected that the Nth sample represents the last data of interest in the burst of conversions. The devices enter the power-down state after the end of conversions. This is the 16th SCLK falling edge. It is recommended to stop the clock after the 16th SCLK falling edge. Note that it is mandatory not to have more than 29 SCLK falling edges during the $\overline{CS}$ low period. This limitation ensures that the devices remain in 16-clock mode.

The devices remain in a power-down state as long as $\overline{CS}$ is low. A $\overline{CS}$ rising edge with PDEN = 0 brings the devices out of the power-down state. It is necessary to ensure that the $\overline{CS}$ high time for the first sample after power up is more than 1 μs + t_{ACQ} (min).

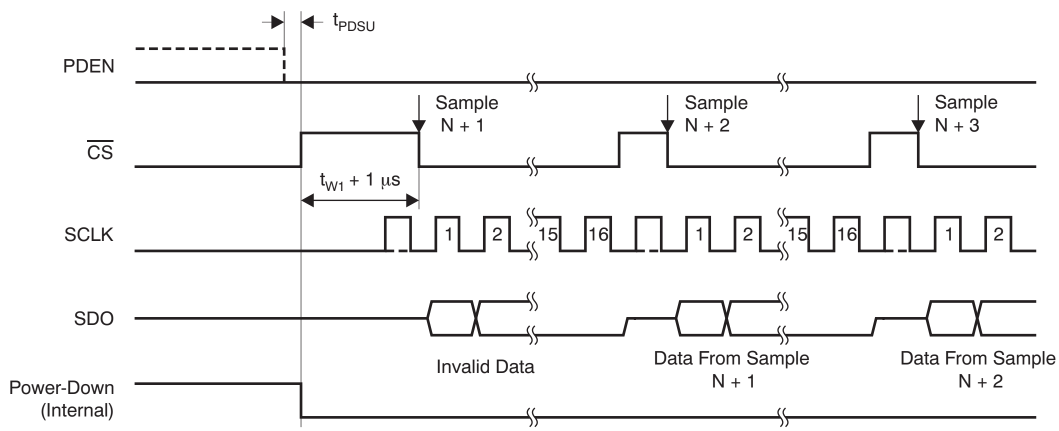


Figure 85. Exit From Power-Down with 16-Clock Burst Mode

APPLICATION INFORMATION: ADS7945

The ADS7945 employs a sample-and-hold stage at the input; see Figure 76 for a typical equivalent circuit of a sample-and-hold stage. The device connects a 32 pF sampling capacitor during sampling. This configuration results in a glitch at the input terminals of the device at the start of the sample. The external circuit must be designed in such a way that the input can settle to the required accuracy during the sampling time chosen. Figure 86 shows a typical driving circuit for the analog inputs.

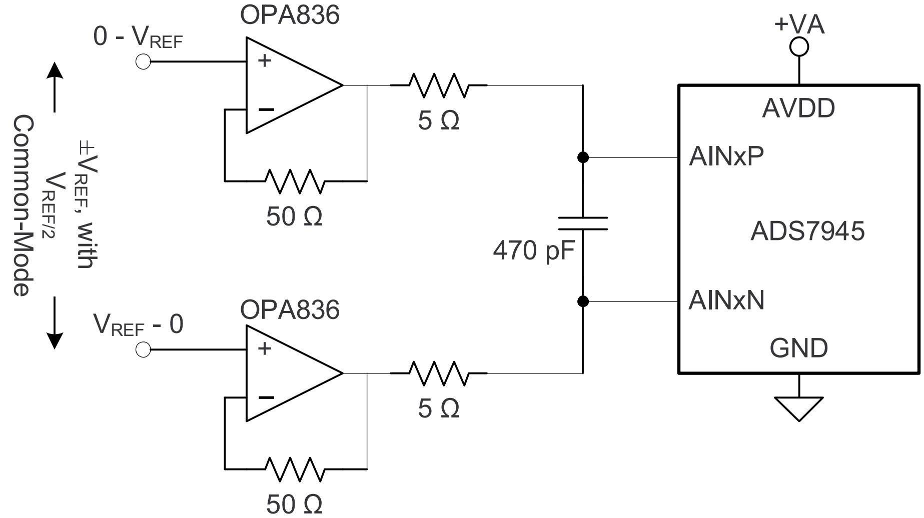


Figure 86. Typical Input Driving Circuit for the ADS7945

The 470 pF capacitor across the AINxP and AINxN terminals decouples the driving op amp from the sampling glitch. It is recommended to split the series resistance of the input filter in two equal values as shown in Figure 86. It is recommended that both input terminals see the same impedance from the external circuit. The low-pass filter at the input limits noise bandwidth of the driving op amps. Select the filter bandwidth so that the full-scale step at the input can settle to the required accuracy during the sampling time. Equation 1, Equation 2, and Equation 3 are useful for filter component selection.

$$\text{Filter Time Constant } (t_{AU}) = \frac{\text{Sampling Time}}{\text{Settling Resolution} \times \ln(2)}$$

Where:

Settling resolution is the accuracy in LSB to which the input needs to settle. A typical settling resolution for the 14-bit device is 15 or 16. (1)

$$\text{Filter Time Constant } (t_{AU}) = R \times C \quad (2)$$

$$\text{Filter Bandwidth} = \frac{1}{2 \times \pi \times t_{AU}} \quad (3)$$

Also, make sure the driving op amp bandwidth does not limit the signal bandwidth below filter bandwidth. In many applications, signal bandwidth may be much lower than filter bandwidth. In this case, an additional low-pass filter may be used at the input of the driving op amp. This signal filter bandwidth can be selected in accordance with the input signal bandwidth.

INPUT COMMON-MODE RANGE

The AIN+ and AIN– inputs to the ADS7945 should typically vary between 0 V and V_{REF} with a common-mode of $V_{REF}/2$. The ADS7945 offers excellent CMRR which makes it possible to achieve close to the rated performance of the converter even in cases where the common-mode input is not well-controlled. The device can accept a ±200 mV variation in the common-mode voltage at any VDD/V_{REF} combination allowing use of the entire ADC signal range (–V_{REF} to +V_{REF} differentially).

DRIVING AN ADC WITHOUT A DRIVING OP AMP

For some low input signal bandwidth applications, such as battery power monitoring or mains monitoring, it is not required to operate an ADC at high sampling rates. In fact, it is desirable to avoid using a driving op amp from a cost perspective. In these cases, the ADC input sees the impedance of the signal source (such as a battery or mains transformer). This section elaborates the effects of source impedance on sampling frequency.

Equation 1 can be rewritten as Equation 4:

Sampling Time = Filter Time Constant × Settling Resolution × ln(2) (4)

As shown in Figure 87, it is recommended to use a bypass capacitor across the positive and negative ADC input terminals.

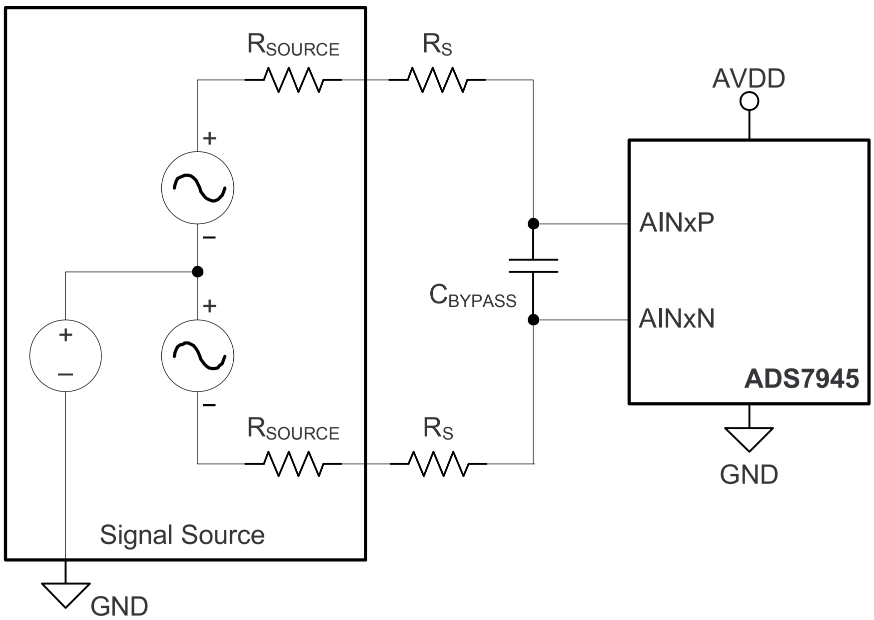


Figure 87. Driving an ADS7945 ADC Without a Driving Op Amp

Source impedance (2 × R_{SOURCE} + 2 × R_S) with (C_{BYPASS} + C_{SAMPLE}) acts as a low-pass filter with Equation 5:

Filter Time Constant = 2 × (R_{SOURCE} + R_S) × (C_{BYPASS} + C_{SAMPLE})

where:

C_{SAMPLE} is the internal sampling capacitance of the ADC (equal to 32 pF). (5)

Table 4 lists the recommended bypass capacitor values and the filter time constant for different source resistances. It is recommended to use a 10 pF bypass capacitor, at minimum. Table 4 assumes R_S = 5 Ω; however, depending on the application, R_S can be chosen to be 0 Ω. In this case, there is an extra margin of 5 Ω for R_{SOURCE}.

Table 4. Filter Time Constant versus Source Resistance

2 × R_{SOURCE} (Ω)	2 × (R_{SOURCE} + R_S)	APPROXIMATE C_{BYPASS} (pF)	C_{BYPASS} + C_{SAMPLE} (pF)	FILTER TIME CONSTANT (ns)
18	28	220	252	7.2
44	54	100	132	7.2
81	91	47	79	7.2
161	171	10	42	7.2
500	510	10	42	21
1000	1010	10	42	42
5000	5010	10	42	210

Typically, settling resolution is selected as (ADC resolution + 2). For the ADS7945 (14-bit) the ideal settling resolution is 16. Using Equation 2 and Equation 3, the sampling time can be easily determined for a given source impedance and allows 80 ns of sampling time for a 14-bit ADC with 7.2 ns of filter time constant, which matches the ADS7945 specifications. For net source impedance (2 × (R_{SOURCE} + R_S)) above 171 Ω, the filter time constant continues to increase beyond the 7.2 ns required for an 80 ns sampling time. This increment increases the minimum permissible sampling time for 14-bit settling and the device must be operated at a lower sampling rate.

The device sampling rate can be maximized by using a 40 MHz clock even for lower throughputs. Table 5 shows typical calculations for the ADS7945.

Table 5. Sampling Frequency versus Source Impedance for the ADS7945 (14-Bit)

2 × R_{SOURCE} (Ω)	C_{BYPASS} (pF)	SAMPLING TIME, t_{ACQ} (ns)	CONVERSION TIME, t_{CONV} (ns)	CYCLE TIME, t_{ACQ} + t_{CONV} (ns)	SAMPLING RATE (MSPS)
161	10	80	420 (with 40 MHz clock)	500	2
500	10	235	420 (with 40 MHz clock)	655	1.5
1000	10	468	420 (with 40 MHz clock)	888	1.1
5000	10	2331	420 (with 40 MHz clock)	2751	0.4

It is necessary to allow 1000 ns additional sampling time over what is shown in Table 5 if PDEN (pin 12) is set high.

APPLICATION INFORMATION: ADS7946

The ADS7946 employs a sample-and-hold stage at the input; see Figure 76 for a typical equivalent circuit of a sample-and-hold stage. The device connects a 32 pF sampling capacitor during sampling. This configuration results in a glitch at the input terminals of the device at the start of the sample. The external circuit must be designed in such a way that the input can settle to the required accuracy during the sampling time chosen. Figure 88 shows a typical driving circuit for the analog inputs.

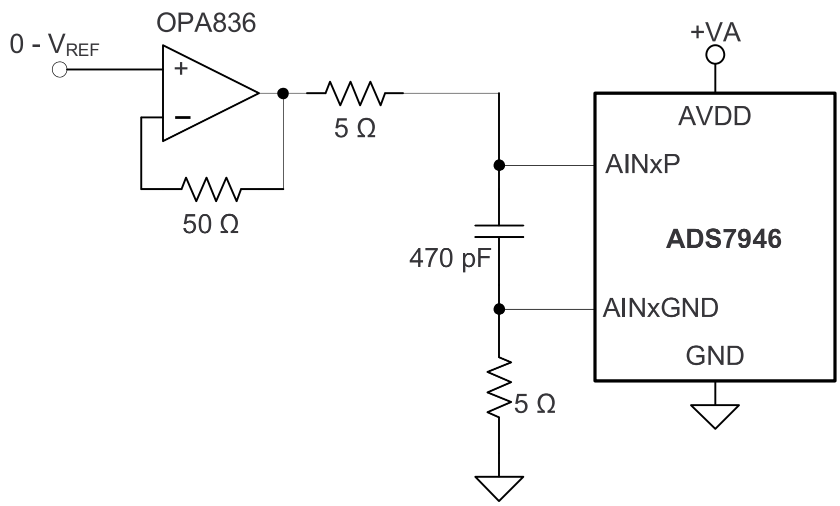


Figure 88. Typical Input Driving Circuit For the ADS7946

The 470 pF capacitor across the AINx and AINxGND terminals decouples the driving op amp from the sampling glitch. It is recommended to split the series resistance of the input filter in two equal values, as shown in Figure 88. It is recommended that both input terminals see the same impedance from the external circuit. The low-pass filter at the input limits noise bandwidth of the driving op amp. Select the filter bandwidth so that the full-scale step at the input can settle to the required accuracy during the sampling time. Equation 6, Equation 7, and Equation 8 are useful for filter component selection.

$$\text{Filter Time Constant } (t_{AU}) = \frac{\text{Sampling Time}}{\text{Settling Resolution} \times \ln(2)}$$

where:

Settling resolution is the accuracy in LSB to which the input must settle. A typical settling resolution for the 14-bit device is 15 or 16. (6)

$$\text{Filter Time Constant } (t_{AU}) = R \times C \tag{7}$$

$$\text{Filter Bandwidth} = \frac{1}{2 \times \pi \times t_{AU}} \tag{8}$$

Also, make sure the driving op amp bandwidth does not limit the signal bandwidth below filter bandwidth. In many applications, signal bandwidth may be much lower than filter bandwidth. In this case, an additional low-pass filter may be used at the input of the driving op amp. This signal filter bandwidth can be selected in accordance with the input signal bandwidth.

DRIVING AN ADC WITHOUT A DRIVING OP AMP

For some low input signal bandwidth applications, such as battery power monitoring or mains monitoring, it is not required to operate an ADC at high sampling rates. In fact, it is desirable to avoid using a driving op amp from a cost perspective. In this case, the ADC input sees the impedance of the signal Equation 4 source (such as a battery or mains transformer). This section elaborates the effects of source impedance on sampling frequency.

Equation 6 can be rewritten as Equation 9:

Sampling Time = Filter Time Constant × Settling Resolution × ln(2) (9)

As shown in Figure 89, it is recommended to use a bypass capacitor across the positive and negative ADC input terminals.

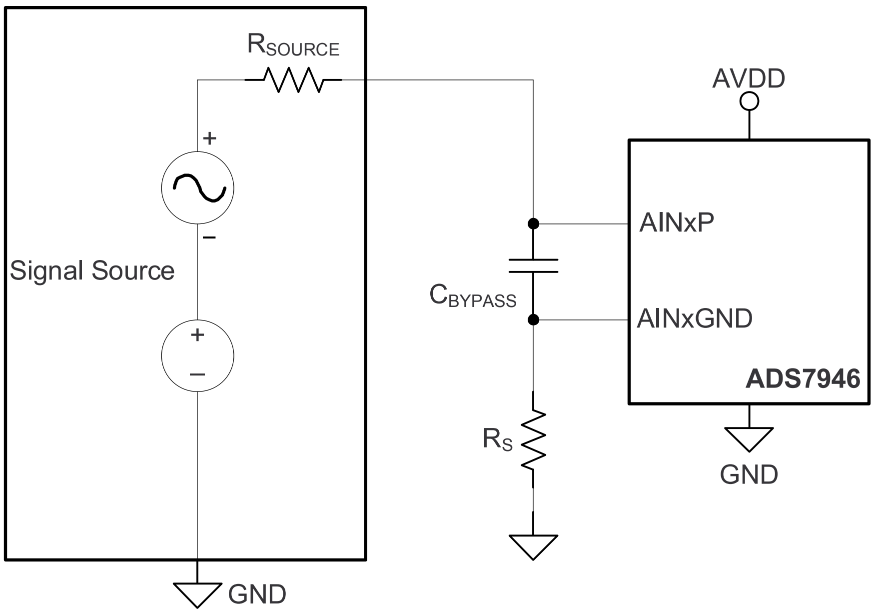


Figure 89. Driving an ADS7946 ADC Without a Driving Op Amp

Source impedance (R_{SOURCE} + R_S) with (C_{BYPASS} + C_{SAMPLE}) acts as a low-pass filter with Equation 10:

Filter Time Constant = (R_{SOURCE} + R_S) × (C_{BYPASS} + C_{SAMPLE})

Where:

C_{SAMPLE} is the internal sampling capacitance of the ADC (equal to 32 pF). (10)

Table 6 lists the recommended bypass capacitor values and the filter time constant for different source resistances. It is recommended to use a 10 pF bypass capacitor (minimum).

Table 6. Filter Time Constant versus Source Resistance

R_{SOURCE} (Ω)	$R_{SOURCE} + R_S$	APPROXIMATE C_{BYPASS} (pF)	$C_{BYPASS} + C_{SAMPLE}$ (pF)	FILTER TIME CONSTANT (ns)
23	28	220	252	7.2
49	54	100	132	7.2
86	91	47	79	7.2
166	171	10	42	7.2
500	505	10	42	21
1000	1005	10	42	42
5000	5005	10	42	210

Typically, settling resolution is selected as (ADC resolution + 2). For the ADS7946 (14-bit) the ideal settling resolution is 16. Using equations Equation 7 and Equation 8, the sampling time can be easily determined for a given source impedance and allows 80 ns of sampling time for a 14-bit ADC with 7.2 ns of filter time constant, which matches the ADS7946 specifications. For source impedance above 166 Ω, the filter time constant continues to increase beyond the 7.2 ns required for an 80 ns sampling time. This increment increases the minimum permissible sampling time for 14-bit settling and the device must be operated at a lower sampling rate.

The device sampling rate can be maximized by using a 40 MHz clock even for lower throughputs. Table 7 shows typical calculations for the ADS7946.

Table 7. Sampling Frequency versus Source Impedance for the ADS7946 (14-Bit)

R_{SOURCE} (Ω)	C_{BYPASS} (pF)	SAMPLING TIME, t_{ACQ} (ns)	CONVERSION TIME, t_{CONV} (ns)	CYCLE TIME, $t_{ACQ} + t_{CONV}$ (ns)	SAMPLING RATE (MSPS)
166	10	80	420 (with 40 MHz clock)	500	2
500	10	235	420 (with 40 MHz clock)	655	1.5
1000	10	468	420 (with 40 MHz clock)	888	1.1
5000	10	2331	420 (with 40 MHz clock)	2751	0.4

It is necessary to allow 1000 ns additional sampling time over what is shown in Table 7 if PDEN (pin 12) is set high.

PCB LAYOUT/SCHEMATIC GUIDELINES: ADS7945

The ADS7945 is a mixed-signal device. For maximum performance, proper decoupling, grounding, and proper termination of digital signals are essential. Figure 90 shows the essential components around the ADC. All capacitors shown are ceramic. These decoupling capacitors must be placed close to the respective signal pins.

There is a 47 Ω *source series termination* resistor shown on the SDO signal. This resistor must be placed as close to pin 15 as possible. Series terminations for SCLK and $\overline{CS}$ must be placed close to the host.

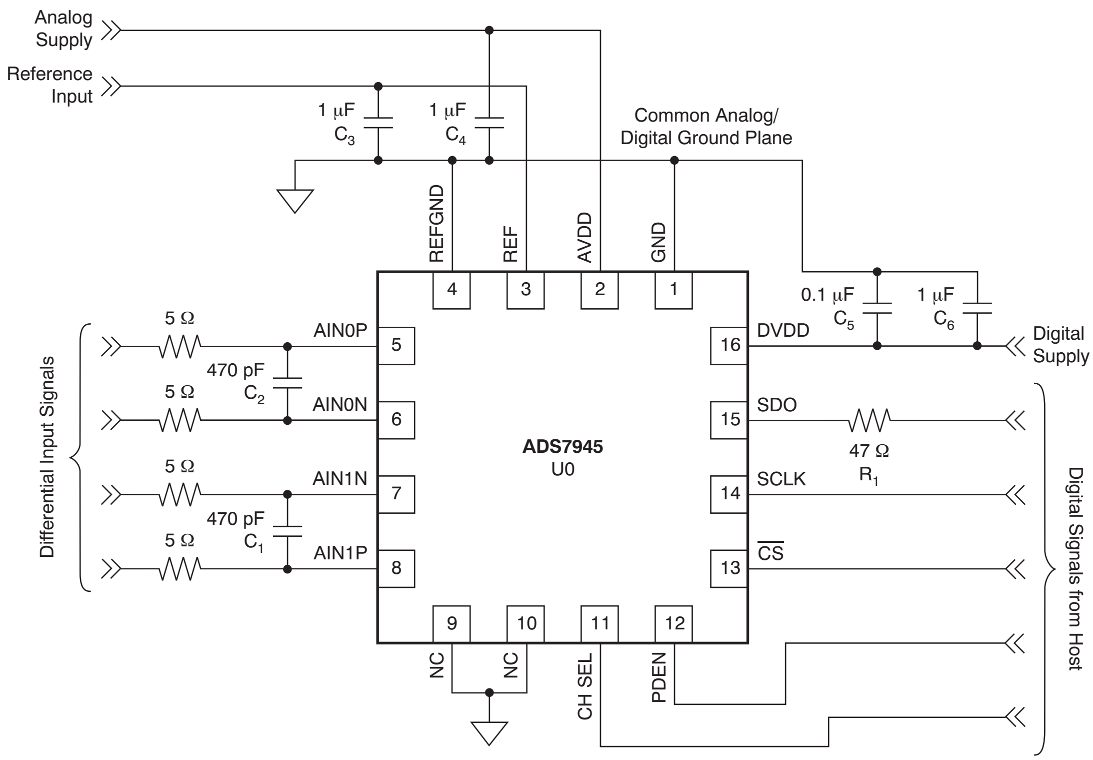


Figure 90. Recommended ADS7945 ADC Schematic

A common ground plane for both analog and digital often enables better results. Typically, the second PCB layer is the ground plane. The ADC ground pins are returned to the ground plane through multiple vias (PTH). It is a good practice to place analog components on one side and digital components on other side of the ADC (or ADCs). All signals must be routed, assuming there is a split ground plane for analog and digital. Furthermore, it is better to split the ground initially during layout. Route all analog and digital traces so that the traces see the respective ground all along the second layer. Then short both grounds to form a common ground plane. Figure 91 shows a typical layout around the ADC.

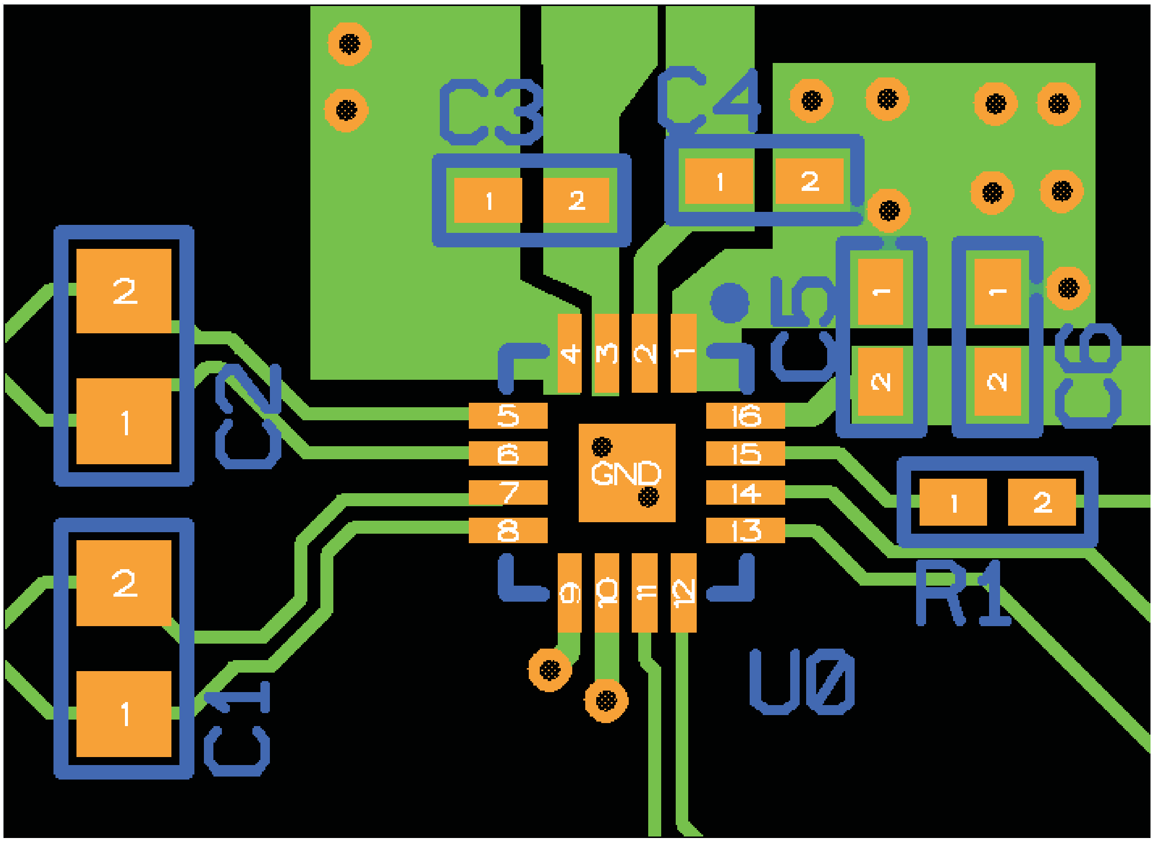


Figure 91. Recommended ADS7945 ADC Layout
(Only top layer is shown; second layer is common ground for analog and digital)

PCB LAYOUT/SCHEMATIC GUIDELINES: ADS7946

The ADS7946 is a mixed-signal device. For maximum performance, proper decoupling, grounding, and proper termination of digital signals are essential. Figure 92 shows the essential components around the ADC. All capacitors shown are ceramic. These decoupling capacitors must be placed close to the respective signal pins.

There is a 47 Ω *source series termination* resistor shown on the SDO signal. This resistor must be placed as close to pin 15 as possible. Series terminations for SCLK and CS must be placed close to the host.

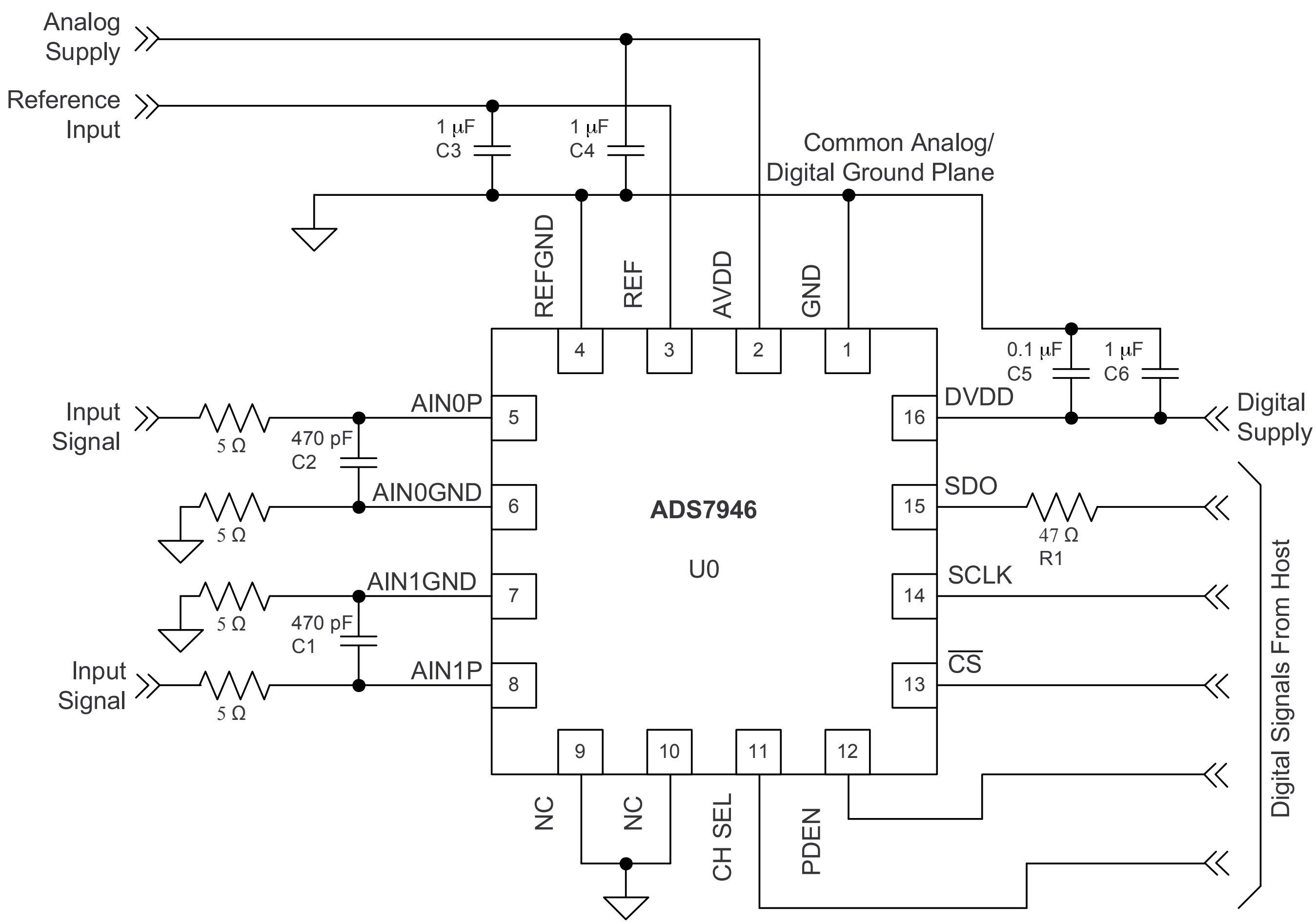


Figure 92. Recommended ADS7946 ADC Schematic

A common ground plane for both analog and digital often enables better results. Typically, the second PCB layer is the ground plane. The ADC ground pins are returned to the ground plane through multiple vias (PTH). It is a good practice to place analog components on one side and digital components on other side of the ADC (or ADCs). All signals must be routed, assuming there is a split ground plane for analog and digital. Furthermore, it is better to split the ground initially during layout. Route all analog and digital traces so that the traces see the respective ground all along the second layer. Then short both grounds to form a common ground plane. Figure 93 shows a typical layout around the ADC.

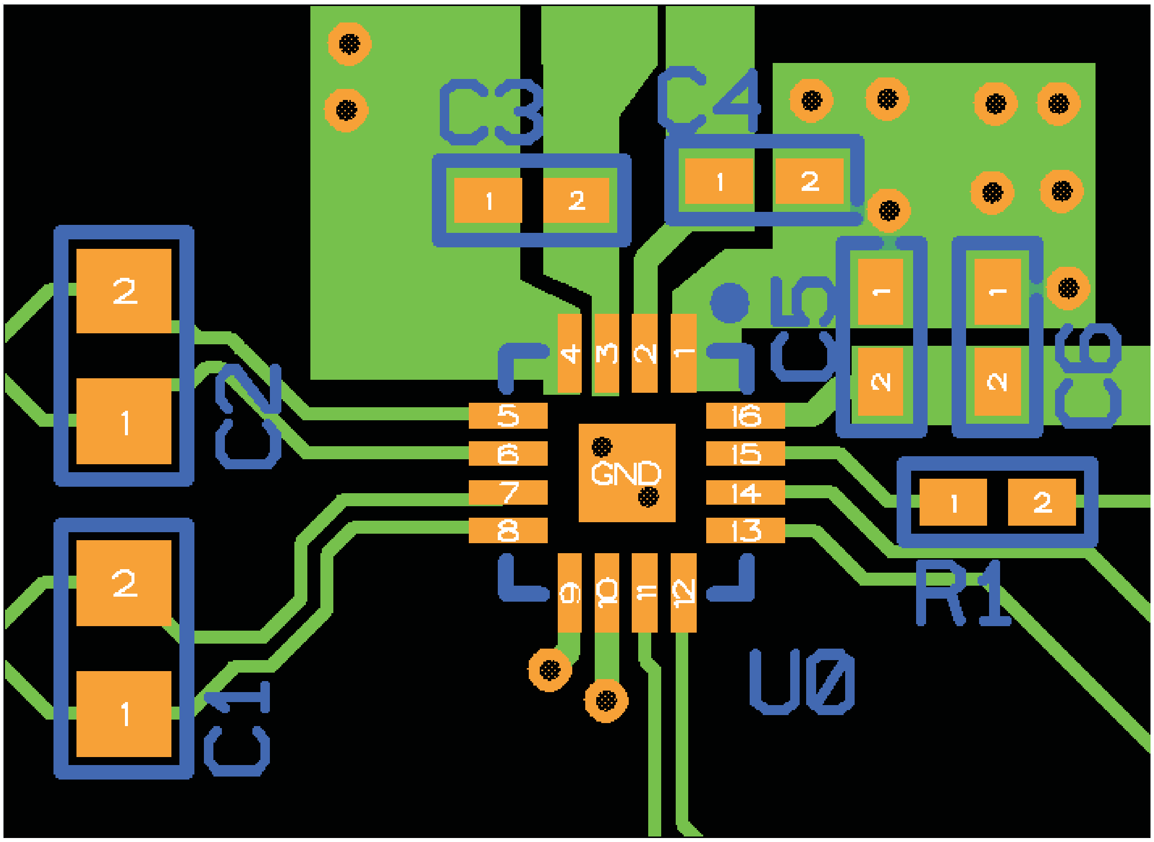


Figure 93. Recommended ADS7946 ADC Layout
(Only top layer is shown; second layer is common ground for analog and digital)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7945SRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7945	Samples
ADS7945SRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7945	Samples
ADS7946SRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7946	Samples
ADS7946SRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7946	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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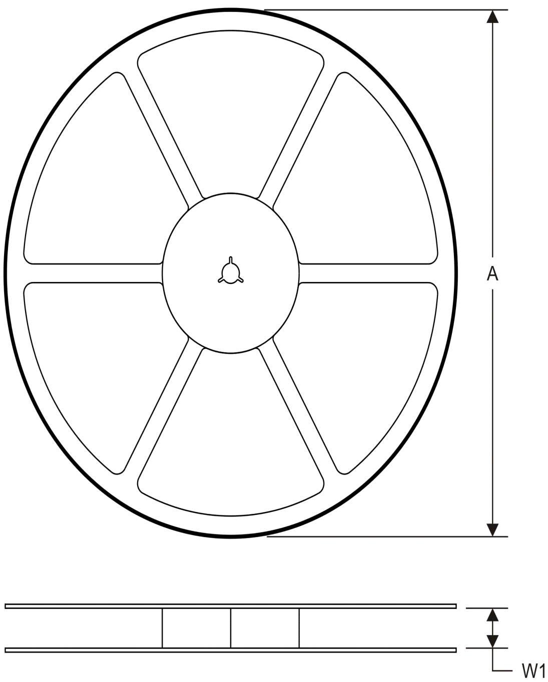
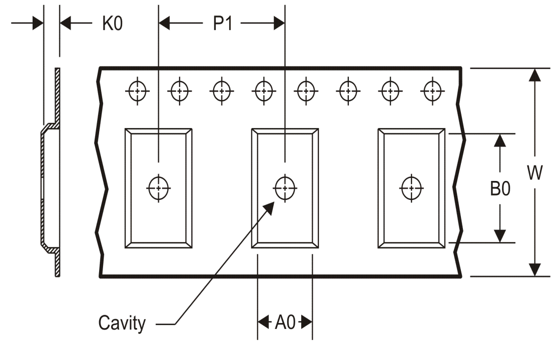
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



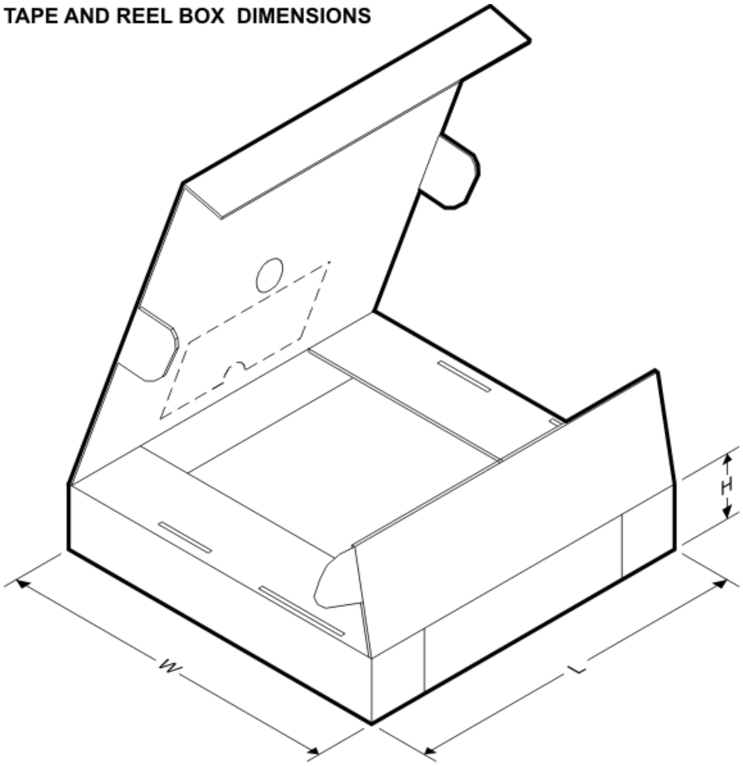
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7945SRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7945SRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7946SRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7946SRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7945SRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7945SRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS7946SRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7946SRTET	WQFN	RTE	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

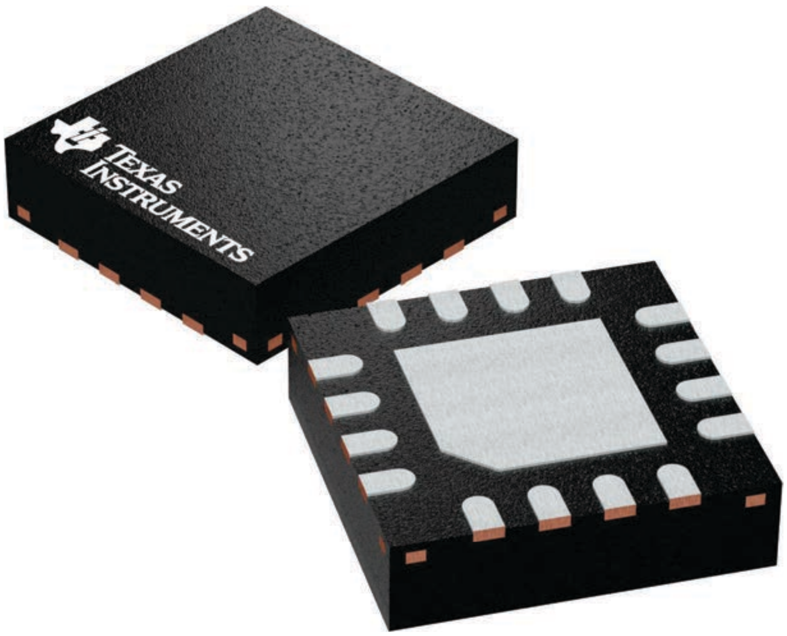
RTE 16

WQFN - 0.8 mm max height

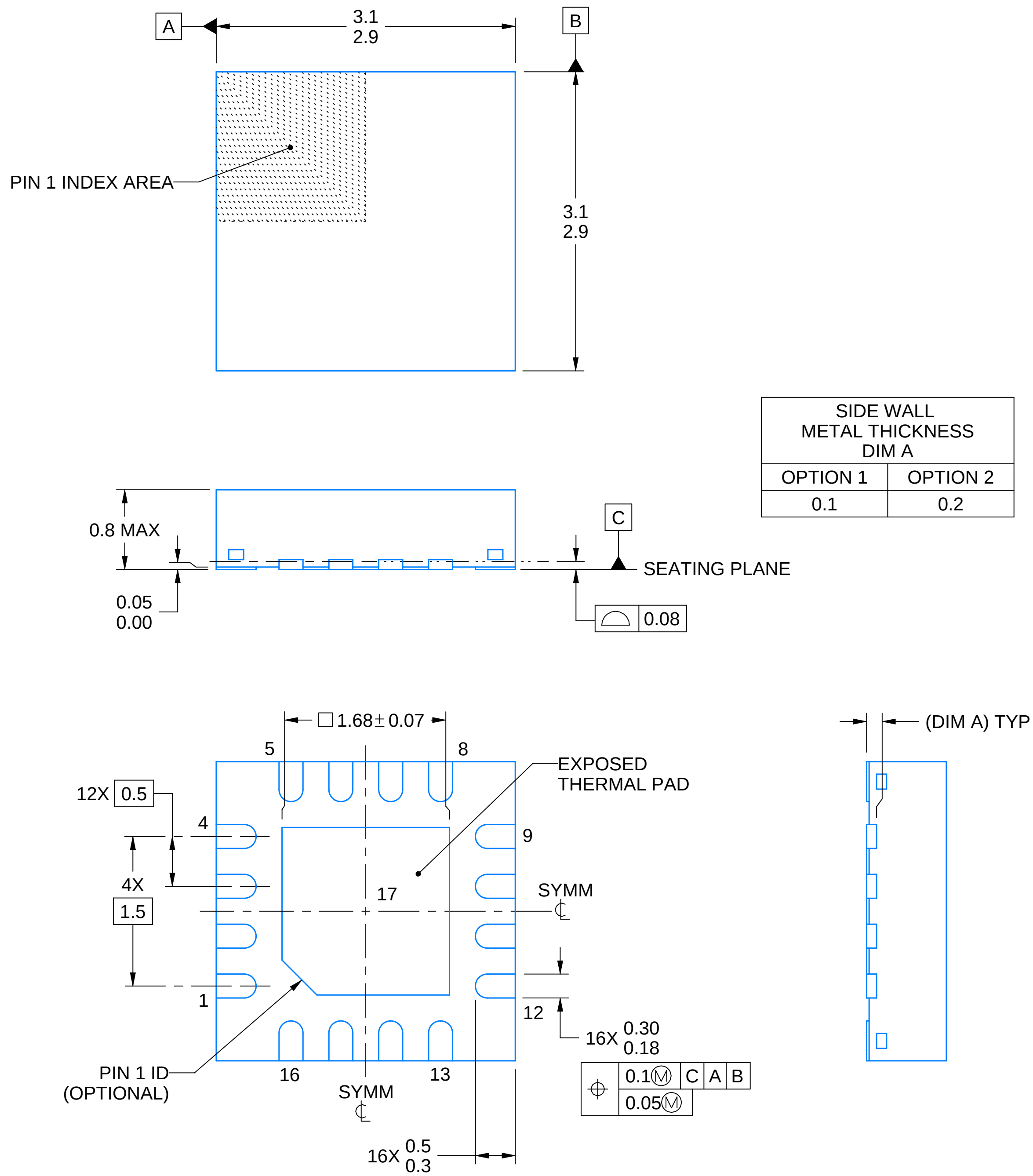
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

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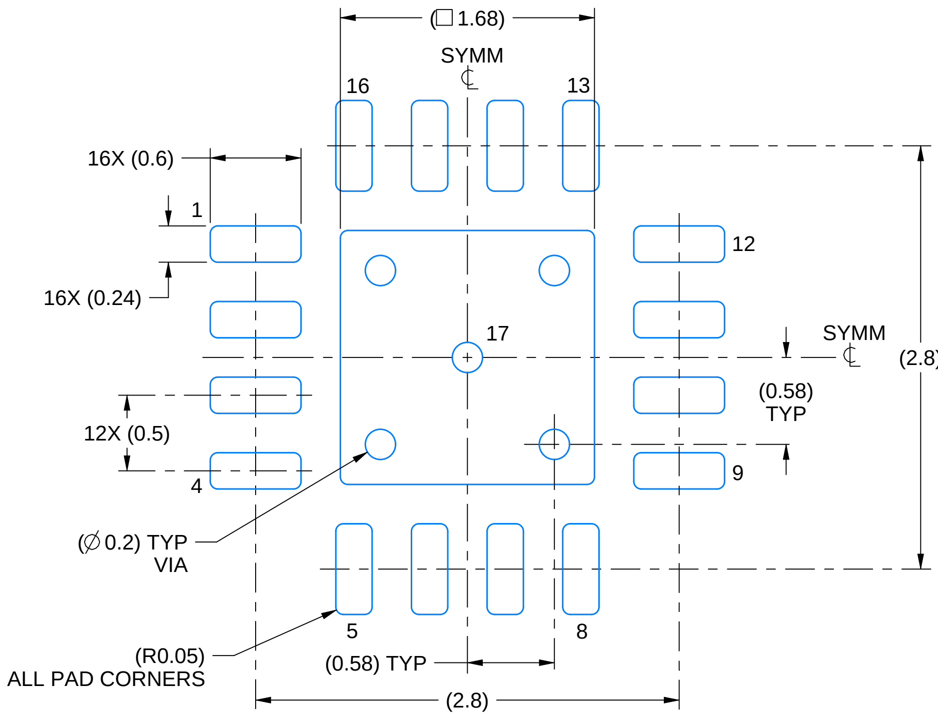
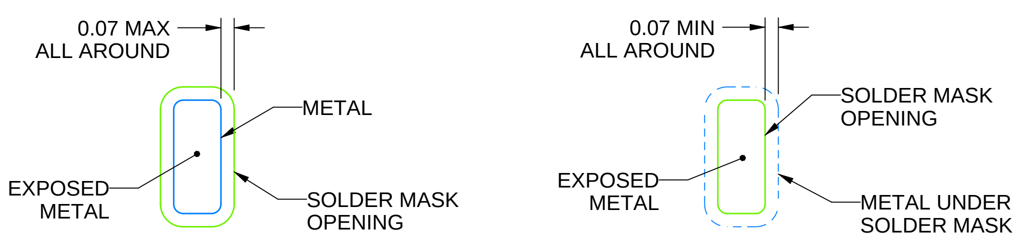
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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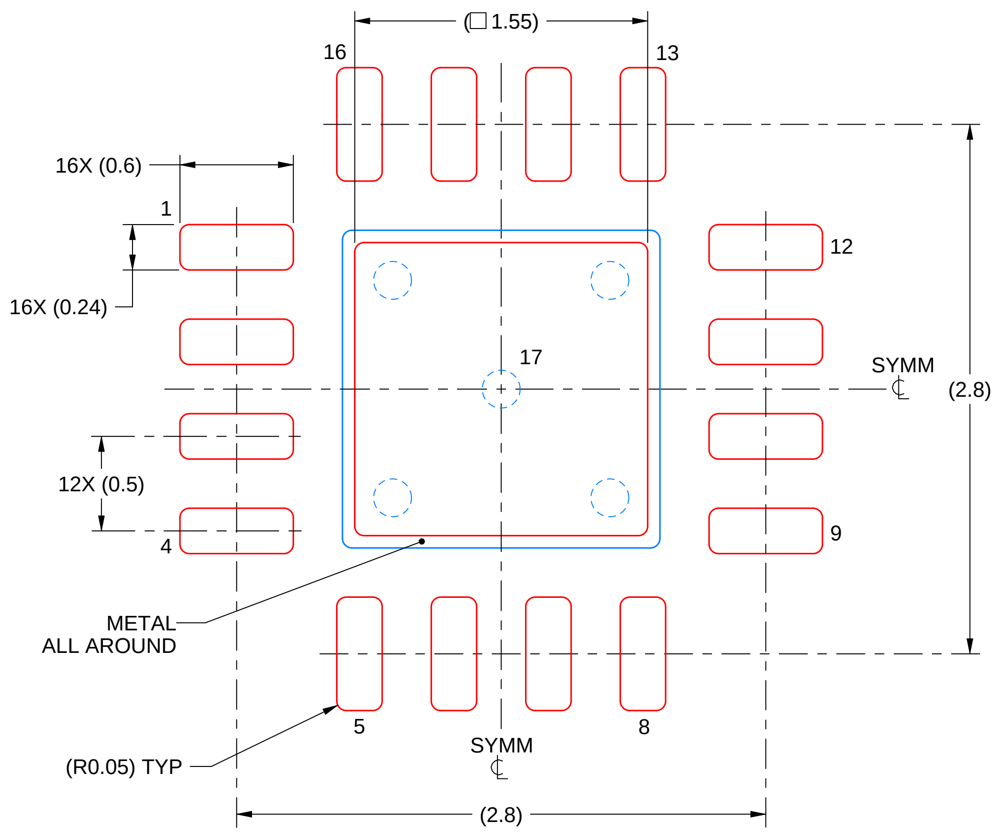
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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