

1A SINGLE-CHIP Li-Ion/Li-Pol CHARGE MANAGEMENT IC WITH THERMAL REGULATION

FEATURES

- Ideal for Low-Dropout Designs for Single-Cell Li-Ion or Li-Pol Packs in Space Limited Applications
- Integrated Power FET and Current Sensor for up to 1-A Charge Applications
- Reverse Leakage Protection Prevents Battery Drainage
- $\pm 0.5\%$ Voltage Regulation Accuracy
- Thermal Regulation Maximizes Charge Rate
- Charge Termination by Minimum Current and Time
- Precharge Conditioning With Safety Timer
- Status Outputs for LED or System Interface Indicate Charge, Fault, and Power Good Outputs
- Short-Circuit and Thermal Protection
- Automatic Sleep Mode for Low Power Consumption
- Small 3×3 mm MLP Package
- Selectable Battery Insertion and Battery Absent Detection
- Input Overvoltage Protection
– 6.5 V and 10.5 V Options

APPLICATIONS

- PDA, MP3 Players, Digital Cameras
- Internet Appliances and Handheld Devices

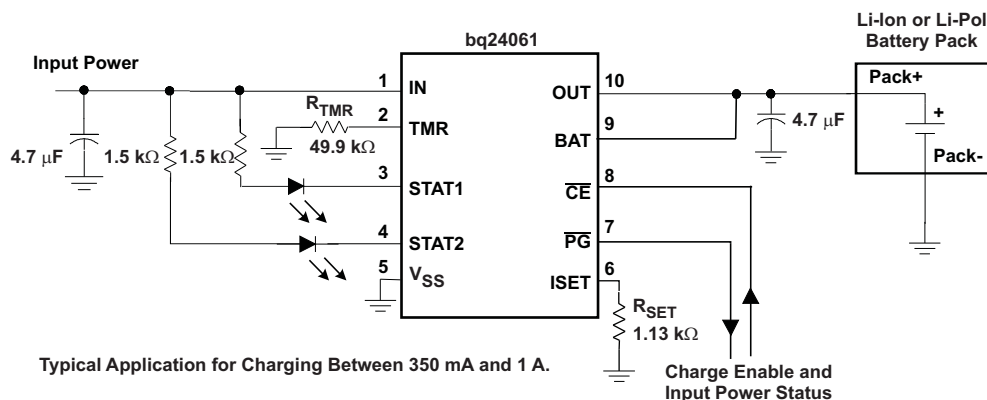
DESCRIPTION

The bq2406x series are highly integrated Li-Ion and Li-Pol linear chargers, targeted at space-limited portable applications. The bq2406x series offers a variety of safety features and functional options, while still implementing a complete charging system in a small package. The battery is charged in three phases: conditioning, constant or thermally regulated current, and constant voltage. Charge is terminated based on minimum current. An internal programmable charge timer provides a backup safety feature for charge termination and is dynamically adjusted during the thermal regulation phase. The bq2406x automatically re-starts the charge if the battery voltage falls below an internal threshold; sleep mode is set when the external input supply is removed. Multiple versions of this device family enable easy design of the bq2406x in cradle chargers or in the end equipment, while using low cost or high-end AC adapters.

Pin Out
(Top View)



TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

| Charge Voltage | Input Over Voltage | Termination Enable | Safety Timer Enable | Power Good Status | IC Enable | Pack Temp | Pack Voltage Detection (Absent) | Devices ⁽¹⁾⁽²⁾⁽³⁾ | Marking |
|----------------|--------------------|---------------------|---------------------|---------------------|---------------------|-----------|---------------------------------|------------------------------|---------|
| 4.2 V | 6.5 V | TMR pin | TMR pin | \overline{PG} pin | No | TS pin | With timer enabled | bq24060 | BPG |
| 4.2 V | 6.5 V | TMR pin | TMR pin | \overline{PG} pin | \overline{CE} pin | No | With timer enabled | bq24061 | BPH |
| 4.2 V | 6.5 V | \overline{TE} pin | TMR pin | No | \overline{CE} pin | No | With termination enabled | bq24063 | Preview |
| 4.2 V | 10.5 V | TMR pin | TMR pin | \overline{PG} pin | No | TS pin | With timer enabled | bq24064 | BSA |

- (1) The bq2406x are only available taped and reeled. Add suffix R to the part number for quantities of 3,000 devices per reel (e.g., bq24060BPGR). Add suffix T to the part number for quantities of 250 devices per reel (e.g., bq24060DRCT).
- (2) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.
- (3) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | | bq2406x |
|------------------|---|-------------------------------|
| | Supply voltage (IN with respect to Vss) | –0.3 V to 18 V ⁽²⁾ |
| | Input voltage on IN, STATx, \overline{PG} , TS, \overline{CE} , \overline{TE} , TMR (all with respect to Vss) | –0.3 V to V(IN) |
| | Input voltage on OUT, BAT, ISET (all with respect to Vss) | –0.3 V to 7 V |
| | Output sink current (STATx) + PG | 15 mA |
| | Output current (OUT pin) | 1.5 A |
| T _A | Operating free-air temperature range | –40°C to 155°C |
| T _{stg} | Storage temperature range | –65°C to 150°C |
| T _J | Junction temperature range | –40°C to 150°C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) The bq2406x device can withstand up to 26 V for a maximum of 87 hours.

RECOMMENDED OPERATING CONDITIONS

| | | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------------|---|------|-----|------|------|
| V _(IN) | Supply voltage range | Battery absent detection not functional | 3.5 | | 4.35 | V |
| V _(IN) | Supply voltage range | Battery absent detection functional | 4.35 | | 16.5 | V |
| T _J | Junction temperature | | 0 | | 125 | °C |
| R _{TMR} | 33K ≤ R _{TMR} ≤ 100K | | | | | |

DISSIPATION RATINGS⁽¹⁾

| PACKAGE | θ _{JC} (°C/W) | θ _{JA} (°C/W) |
|------------|------------------------|------------------------|
| 10-pin DRC | 3.21 | 46.87 |

- (1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a 2x3 via matrix.

ELECTRICAL CHARACTERISTICS

over recommended operating, $T_j = 0 - 125^\circ\text{C}$ range, See the Application Circuits section, typical values at $T_j = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|---|---|----------------------------|------|------|------------------|---|
| POWER DOWN THRESHOLD – UNDERVOLTAGE LOCKOUT | | | | | | | |
| $V_{(UVLO)}$ | Power down threshold | $V_{(IN)} = 0\text{ V}$, increase $V_{(OUT)}$: $0 \rightarrow 3\text{ V}$ OR $V_{(OUT)} = 0\text{ V}$, increase $V_{(IN)}$: $0 \rightarrow 3\text{ V}$, $\overline{CE} = \text{LO}$ ⁽¹⁾ | 1.5 | | 3.0 | V | |
| INPUT POWER DETECTION, $\overline{CE} = \text{HI}$ or LOW, $V_{(IN)} > 3.5\text{ V}$ | | | | | | | |
| $V_{(INDT)}$ | Input power detection threshold | $V_{(IN)}$ detected at $[V_{(IN)} - V_{(OUT)}] > V_{(INDT)}$ | | | 130 | mV | |
| $V_{(HYS(INDT))}$ | Input power detection hysteresis | Input power not detected at $[V_{(IN)} - V_{(OUT)}] < [V_{(INDT)} - V_{(HYS(INDT))}]$ | 30 | | | mV | |
| $T_{(DGL(INDT1))}$ | Deglintch time, input power detected status | \overline{PG} : HI \rightarrow LO, Thermal regulation loop not active, $R_{(TMR)} = 50\text{ K}\Omega$ or $V_{(TMR)} = \text{OPEN}$ | 1.5 | | 3.5 | ms | |
| $T_{(DGL(NOIN))}$ | Delay time, input power not detected status | \overline{PG} : LO \rightarrow HI after $T_{(DGL(NOIN))}$ | | | 10 | μs | |
| $T_{(DLY(CHGOFF))}$ | Charger off delay | Charger turned off after $T_{(DLY(CHGOFF))}$, Measured from \overline{PG} : LO \rightarrow HI; Timer reset after $T_{(DLY(CHGOFF))}$ | 28 | | 32 | ms | |
| INPUT OVERVOLTAGE PROTECTION | | | | | | | |
| $V_{(OVP)}$ | Input overvoltage detection threshold | $V_{(IN)}$ increasing | bq24060/61/63 | 6.2 | 6.5 | 7.0 | V |
| | | | bq24064 | 10.2 | 10.5 | 11.7 | |
| $V_{(HYS(OVP))}$ | Input overvoltage hysteresis | $V_{(IN)}$ decreasing | bq24060/61/63 | 0.1 | | 0.2 | V |
| | | | bq24064 | 0.3 | | 0.5 | |
| $T_{(DGL(OVDET))}$ | Input overvoltage detection delay | $\overline{CE} = \text{HI}$ or LO , Measured from $V_{(IN)} > V_{(OVP)}$ to \overline{PG} : LO \rightarrow HI; $V_{(IN)}$ increasing | 10 | | 100 | μs | |
| $T_{(DGL(OVNDT))}$ | Input overvoltage not detected delay | $\overline{CE} = \text{HI}$ or LO , Measured from $V_{(IN)} < V_{(OVP)}$ to \overline{PG} : HI \rightarrow LO; $V_{(IN)}$ decreasing | 10 | | 100 | μs | |
| QUIESCENT CURRENT | | | | | | | |
| $I_{(CC(CHGOFF))}$ | IN pin quiescent current, charger off | Input power detected, $\overline{CE} = \text{HI}$ | $V_{(IN)} = 6\text{ V}$ | 100 | 200 | μA | |
| | | | $V_{(IN)} = 16.5\text{ V}$ | 300 | | | |
| $I_{(CC(CHGON))}$ | IN pin quiescent current, charger on | Input power detected, $\overline{CE} = \text{LO}$, $V_{(BAT)} = 4.5\text{ V}$ | | 4 | 6 | mA | |
| $I_{(BAT(DONE))}$ | Battery leakage current after termination into IC | Input power detected, charge terminated, $\overline{CE} = \text{LO}$ | | 1 | 5 | μA | |
| $I_{(BAT(CHGOFF))}$ | Battery leakage current into IC, charger off | Input power detected, $\overline{CE} = \text{HI}$ OR input power not detected, $\overline{CE} = \text{LO}$ | | 1 | 5 | μA | |
| TS PIN COMPARATOR | | | | | | | |
| $V_{(TS1)}$ | Lower voltage temperature threshold | Hot detected at $V_{(TS)} < V_{(TS1)}$; NTC thermistor | 29 | 30 | 31 | % $V_{(IN)}$ | |
| $V_{(TS2)}$ | Upper voltage temperature threshold | Cold detected at $V_{(TS)} > V_{(TS2)}$; NTC thermistor | 60 | 61 | 62 | % $V_{(IN)}$ | |
| $V_{(HYS(TS))}$ | Hysteresis | Temp OK at $V_{(TS)} > [V_{(TS1)} + V_{(HYS(TS))}]$ OR $V_{(TS)} < [V_{(TS2)} - V_{(HYS(TS))}]$ | | 2 | | % $V_{(IN)}$ | |
| \overline{CE} INPUT | | | | | | | |
| $V_{(IL)}$ | Input (low) voltage | $V_{(\overline{CE})}$ increasing | 0 | | 1 | V | |
| $V_{(IH)}$ | Input (high) voltage | $V_{(\overline{CE})}$ decreasing | 2.0 | | | V | |
| STAT1, STAT2 AND \overline{PG} OUTPUTS, $V_{(IN)} \geq V_{(O(REG))} + V_{(DO-MAX)}$ | | | | | | | |
| $V_{(OL)}$ | Output (low) saturation voltage | Ioutput = 5 mA (sink) | | | 0.5 | V | |
| THERMAL SHUTDOWN | | | | | | | |
| $T_{(SHUT)}$ | Temperature trip | Junction temperature, temp rising | | 155 | | $^\circ\text{C}$ | |
| $T_{(SHUTHYS)}$ | Thermal hysteresis | Junction temperature | | 20 | | $^\circ\text{C}$ | |

(1) Specified by design, not production tested.

ELECTRICAL CHARACTERISTICS (Continued)

over recommended operating, $T_j = 0-125^{\circ}\text{C}$ range, See the Application Circuits section, typical values at $T_j = 25^{\circ}\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---|---|---|--|------|------|--------------------|-----|
| VOLTAGE REGULATION, $V(\text{IN}) \geq V_{\text{O(REG)}} + V_{\text{(DO-MAX)}}$, $I_{\text{(TERM)}} < I_{\text{(OUT)}} < I_{\text{O(OUT)}}$, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED | | | | | | | |
| $V_{\text{O(REG)}}$ | Output voltage | bq24060/61/63/64 | | 4.20 | | V | |
| $V_{\text{O(TOL)}}$ | Voltage regulation accuracy | $T_A = 25^{\circ}\text{C}$ | -0.5% | | 0.5% | | |
| | | | -1% | | 1% | | |
| $V_{\text{(DO)}}$ | Dropout voltage, $V(\text{IN}) - V(\text{OUT})$ | $I_{\text{O(OUT)}} = 1 \text{ A}$ | | | 750 | mV | |
| CURRENT REGULATION, $V(\text{IN}) > V(\text{OUT}) > V_{\text{(DO-MAX)}}$, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED | | | | | | | |
| $I_{\text{O(OUT)}}$ | Output current range | $V_{\text{(BAT)}} > V_{\text{(LOWV)}}$, $I_{\text{O(OUT)}} = I_{\text{(OUT)}} = K_{\text{(SET)}} \times \frac{V_{\text{(SET)}}}{R_{\text{SET}}}$ | 100 | | 1000 | mA | |
| $V_{\text{(SET)}}$ | Output current set voltage | $V(\text{ISET}) = V_{\text{(SET)}}$, $V_{\text{(LOWV)}} < V(\text{BAT}) \leq V_{\text{O(REG)}}$ | 2.45 | 2.50 | 2.55 | V | |
| $K_{\text{(SET)}}$ | Output current set factor | $100 \text{ mA} \leq I_{\text{O(OUT)}} \leq 1000 \text{ mA}$ | $\frac{\text{mA} \times \text{k}\Omega}{\text{Volts}}$ | | 315 | 335 | 355 |
| | | $10 \text{ mA} \leq I_{\text{O(OUT)}} < 100 \text{ mA}$ | | | 315 | 372 | 430 |
| R_{ISET} | External resistor range | Resistor connected to ISET pin | 0.7 | | 10 | k Ω | |
| VOLTAGE AND CURRENT REGULATION TIMING, $V(\text{IN}) > V(\text{OUT}) + V_{\text{(DO-MAX)}}$, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED, $R_{\text{TMR}} = 50\text{K}$ or $V(\text{TMR}) = \text{OPEN}$; Thermal regulation loop not active | | | | | | | |
| $T_{\text{PWRUP(CHG)}}$ | Input power detection to full charge current time delay | Measured from $\overline{\text{PG}}:\text{HI} \rightarrow \text{LO}$ to $I(\text{OUT}) > 100 \text{ mA}$, $\overline{\text{CE}} = \text{LO}$, $I_{\text{O(OUT)}} = 1 \text{ A}$, $V(\text{BAT}) = 3.5 \text{ V}$ | | 25 | 35 | ms | |
| $T_{\text{PWRUP(EN)}}$ | Charge enable to full charge current delay | Measured from $\overline{\text{CE}}:\text{HI} \rightarrow \text{LO}$ to $I(\text{OUT}) > 100 \text{ mA}$, $I_{\text{O(OUT)}} = 1 \text{ A}$, $V_{\text{(BAT)}} = 3.5 \text{ V}$, $V_{\text{(IN)}} = 4.5 \text{ V}$, Input power detected | | 25 | 35 | ms | |
| $T_{\text{PWRUP(LDO)}}$ | Input power detection to voltage regulation delay, LDO mode set, no battery or load connected | Measured from $\overline{\text{PG}}:\text{HI} \rightarrow \text{LO}$ to $V(\text{OUT}) > 90\%$ of charge voltage regulation; $V_{\text{(TMR)}} = \text{OPEN}$, LDO mode set, no battery and no load at OUT pin, $\overline{\text{CE}} = \text{LO}$ | | 25 | 35 | ms | |
| PRECHARGE AND OUTPUT SHORT-CIRCUIT CURRENT REGULATION, $V(\text{IN}) - V(\text{OUT}) > V_{\text{(DO-MAX)}}$, $V(\text{IN}) \geq 4.5\text{V}$, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED, $R_{\text{TMR}} = 50\text{K}$ or $V(\text{TMR}) = \text{OPEN}$; Thermal regulation loop not active | | | | | | | |
| $V_{\text{(LOWV)}}$ | Precharge to fast-charge transition threshold | $V_{\text{(BAT)}}$ increasing | 2.8 | 2.95 | 3.15 | V | |
| $V_{\text{(SC)}}$ | Precharge to short-circuit transition threshold | $V_{\text{(BAT)}}$ decreasing | 1.2 | 1.4 | 1.6 | V | |
| $V_{\text{(SCIND)}}$ | Short-circuit indication | $V_{\text{(BAT)}}$ decreasing | 1.6 | 1.8 | 2.0 | | |
| $I_{\text{O(PRECHG)}}$ | Precharge current range | $V_{\text{(SC)}} < V_{\text{(BAT)}} < V_{\text{(LOWV)}}$, $t < T_{\text{(PRECHG)}}$ $I_{\text{O(PRECHG)}} = K_{\text{(SET)}} \times \frac{V_{\text{(PRECHG)}}}{R_{\text{(ISET)}}$ | 10 | | 100 | mA | |
| $V_{\text{(PRECHG)}}$ | Precharge set voltage | $V_{\text{(ISET)}} = V_{\text{(PRECHG)}}$, $V_{\text{(SC)}} < V_{\text{(BAT)}} < V_{\text{(LOWV)}}$, $t < T_{\text{(PRECHG)}}$ | 225 | 250 | 280 | mV | |
| $I_{\text{O(SHORT)}}$ | Output shorted regulation current | $V_{\text{SS}} \leq V_{\text{(BAT)}} \leq V_{\text{(SC)}}$, $I_{\text{O(SHORT)}} = I_{\text{(OUT)}}$, $V_{\text{(BAT)}} = V_{\text{SS}}$, Internal pullup resistor | $V_{\text{POR}} < V_{\text{IN}} < 6.0 \text{ V}$ | 15 | 22 | 30 | mA |
| | | | $6.0 \text{ V} < V_{\text{IN}} < V_{\text{OVP}}$ | | 25 | | |
| TEMPERATURE REGULATION (Thermal regulation™), CHARGER ENABLED, NO FAULT CONDITIONS DETECTED | | | | | | | |
| $T_{\text{J(REG)}}$ | Temperature regulation limit | $V(\text{IN}) = 5.5 \text{ V}$, $V(\text{BAT}) = 3.2 \text{ V}$, Fast charge current set to 1A | 101 | 112 | 125 | $^{\circ}\text{C}$ | |
| $I_{\text{(MIN_TJ(REG))}}$ | Minimum current in thermal regulation | $V_{\text{(LOWV)}} < V(\text{BAT}) < V_{\text{O(REG)}}$, $0.7\text{k}\Omega < R_{\text{ISET}} < 3.5\text{k}\Omega$ | | 200 | 250 | mA | |

ELECTRICAL CHARACTERISTICS (Continued)

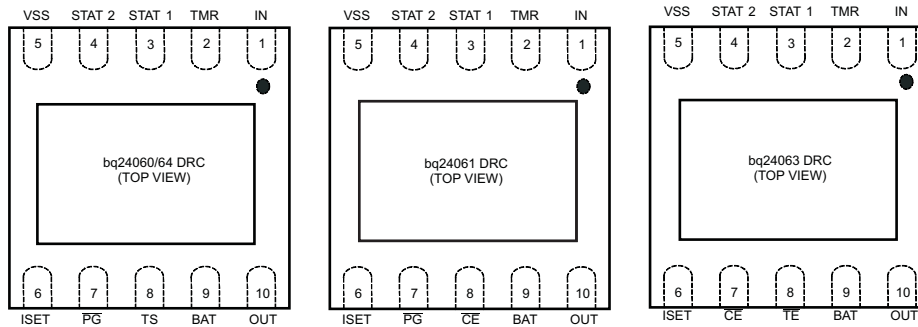
over recommended operating, $T_j = 0\text{--}125^\circ\text{C}$ range, See the Application Circuits section, typical values at $T_j = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|---|---|--|-----------------|-----|------|---------------|-----|---|
| CHARGE TERMINATION DETECTION, $V_{O(REG)} = 4.2\text{ V}$, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED, Thermal regulation LOOP NOT ACTIVE, $R_{TMR} = 50\text{K}$ or TMR pin OPEN | | | | | | | | |
| $I_{(TERM)}$ | Termination detection current range | $V_{(BAT)} > V_{(RCH)}$, $I_{(TERM)} = K_{(SET)} \times V_{(TERM)} / R_{ISET}$ | 10 | | 100 | mA | | |
| $V_{(TERM)}$ | Charge termination detection set voltage ⁽¹⁾ | $V_{(BAT)} > V_{(RCH)}$ | 225 | 250 | 275 | mV | | |
| $T_{DGL(TERM)}$ | Deglintch time, termination detected | $V_{(ISET)}$ decreasing | 15 | 25 | 35 | ms | | |
| BATTERY RECHARGE THRESHOLD | | | | | | | | |
| $V_{(RCH)}$ | Recharge threshold detection | $[V_{O(REG)} - V_{(BAT)}] > V_{(RCH)}$ | 75 | 100 | 135 | mV | | |
| $T_{DGL(RCH)}$ | Deglintch time, recharge detection | $V_{(BAT)}$ decreasing | 15 | 25 | 35 | ms | | |
| TIMERS, $\overline{CE} = \text{LO}$, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED, $V(TMR) < 3\text{ V}$, TIMERS ENABLED | | | | | | | | |
| $T_{(CHG)}$ | Charge safety timer range | $T_{(CHG)} = K_{(CHG)} \times R_{TMR}$; thermal loop not active | 3 | | 10 | hours | | |
| $K_{(CHG)}$ | Charge safety timer constant | $V_{(BAT)} > V_{(LOWV)}$ | 0.08 | 0.1 | 0.12 | hr/k Ω | | |
| $T_{(PCHG)}$ | Pre-charge safety timer range | $T_{(PCHG)} = K_{(PCHG)} \times T_{(CHG)}$; Thermal regulation loop not active | 1080 | | 3600 | sec | | |
| $K_{(PCHG)}$ | Pre-charge safety timer constant | $V_{(BAT)} < V_{(LOWV)}$ | 0.08 | 0.1 | 0.12 | | | |
| $V_{TMR(OFF)}$ | Charge timer and termination enable threshold | [Charge timer AND termination disabled] at $V_{(TMR)} > V_{TMR(OFF)}$ | bq24060/61/64 | | 2.5 | 3.0 | 3.5 | V |
| | Charge timer enable threshold | [Charge timer disabled] at $V_{(TMR)} > V_{TMR(OFF)}$ | bq24063 | | | | | |
| I_{TMR} | TMR pin source current | $V_{(TMR)} = 3.5\text{ V}$, $V_{(IN)} = 4.5\text{ V}$ | 1 | | 6 | μA | | |
| BATTERY DETECTION THRESHOLDS | | | | | | | | |
| $I_{DET(DOWN)}$ | Battery detection current (sink) | $2\text{ V} < V_{(BAT)} < V_{O(REG)}$ | 1 | 2 | 3.2 | mA | | |
| $I_{DET(UP)}$ | Battery detection current (source) | $2\text{ V} < V_{(BAT)} < V_{O(REG)}$ | $I_{O(PRECHG)}$ | | | | | |
| $T_{(DETECT)}$ | Battery detection time | $2\text{ V} < V_{(BAT)} < V_{O(REG)}$, Thermal regulation loop not active; $R_{TMR} = 50\text{ k}\Omega$, $I_{DET(down)}$ or $I_{DET(UP)}$ | 85 | 120 | 150 | ms | | |
| TIMER FAULT RECOVERY | | | | | | | | |
| $I_{(FAULT)}$ | Fault Current (source) | $V_{(OUT)} < V_{(RCH)}$ | -12 | -10 | -8 | mA | | |
| CHARGE OVERCURRENT DETECTION, $V(IN) \geq 4.5\text{ V}$, CHARGER ENABLED | | | | | | | | |
| $I_{CH(OI)}$ | Charge overcurrent detection threshold | $V_{(ISET)} = VSS$ | 2 | | | A | | |
| $T_{DGL(OI)}$ | Overcurrent detection delay time | Measured from $V_{(ISET)} = VSS$ to $I_{O(OUT)} = 0$ | 100 | | | μs | | |

(1) The voltage on the ISET pin is compared to the $V_{(TERM)}$ voltage to determine when the termination should occur.

DEVICE INFORMATION

PIN ASSIGNMENT



TERMINAL FUNCTIONS, REQUIRED COMPONENTS

| NAME | TERMINAL NO. | | | I/O | DESCRIPTION AND REQUIRED COMPONENTS |
|---------------------|--------------|---------|---------|-----|---|
| | bq24060/64 | bq24061 | bq24063 | | |
| IN | 1 | 1 | 1 | I | Charge Input Voltage and internal supply. Connect a 1- μ F (minimum) capacitor from IN to VSS. $C_{IN} \geq C_{OUT}$ |
| TMR | 2 | 2 | 2 | I | Safety Timer Program Input, timer disabled if floating. Connect a resistor to VSS pin to program safety timer timeout value |
| STAT1 | 3 | 3 | 3 | O | Charge Status Output 1 (open-collector, see Table 3) |
| STAT2 | 4 | 4 | 4 | O | Charge Status Output 2 (open-collector, see Table 3) |
| VSS | 5 | 5 | 5 | I | Ground |
| ISET | 6 | 6 | 6 | O | Charge current set point, resistor connected from ISET to VSS sets charge current value. Connect a 0.47- μ F capacitor from BAT to ISET. |
| \overline{PG} | 7 | 7 | — | O | Power Good status output (open-collector), active low |
| \overline{CE} | — | 8 | 7 | I | Charge enable Input. \overline{CE} = LO enables charger. \overline{CE} = HI disables charger. |
| \overline{TE} | — | — | 8 | I | Termination enable Input. \overline{TE} = LO enables termination detection and battery absent detection. \overline{TE} = HI disables termination detection and battery absent detection. |
| TS | 8 | — | — | I | Temperature Sense Input, connect to battery pack thermistor. Connect an external resistive divider to program temperature thresholds. |
| BAT | 9 | 9 | 9 | I | Battery Voltage Sense Input. Connect to the battery positive terminal. Connect a 200- Ω resistor from BAT to OUT. |
| OUT | 10 | 10 | 10 | O | Charge current output. Connect to the battery positive terminal. Connect a 1- μ F (minimum) capacitor from OUT to VSS. |
| Exposed Thermal Pad | Pad | Pad | Pad | | There is an internal electrical connection between the exposed thermal pad and Vss pin of the IC. The exposed thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the IC. VSS pin must be connected to ground at all times. |

TYPICAL OPERATING CHARACTERISTICS

Measured using the typical application circuit shown previously.

THERMAL LOOP OPERATION WITH POWERPAD ATTACHED

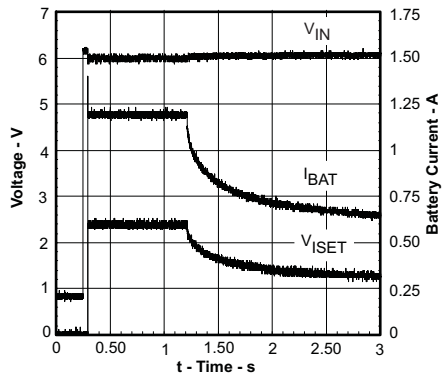


Figure 1.

THERMAL LOOP AND DTC OPERATION

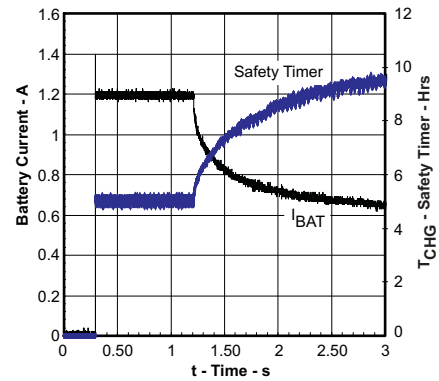


Figure 2.

PACK REMOVAL TRANSIENT

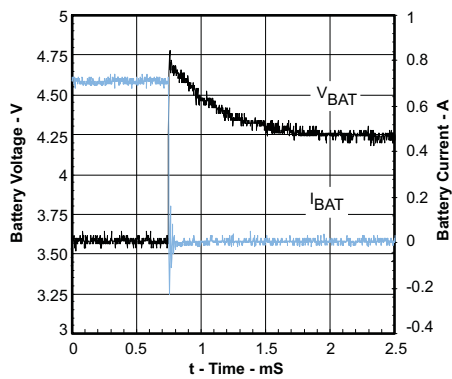


Figure 3.

INPUT OVP RECOVERY TRANSIENTS

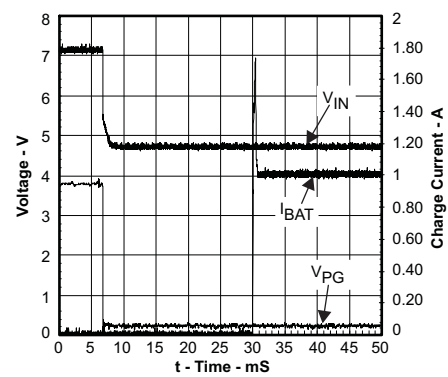


Figure 4.

PG DEGLITCH TIME

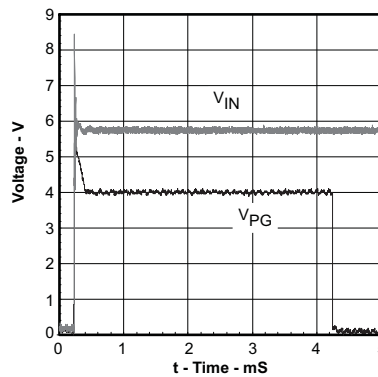


Figure 5.

TYPICAL OPERATING CHARACTERISTICS (continued)

Measured using the typical application circuit shown previously.

**PRE-CHARGE CURRENT
vs
BATTERY VOLTAGE**

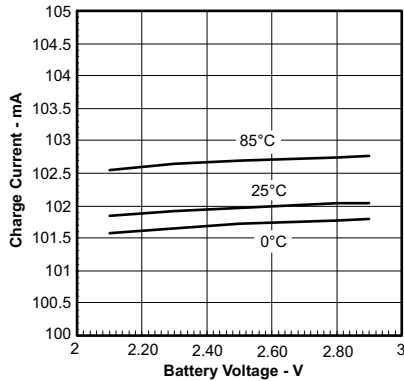


Figure 6. HIGH CHARGE RATE

**FAST-CHARGE CURRENT
vs
BATTERY VOLTAGE**

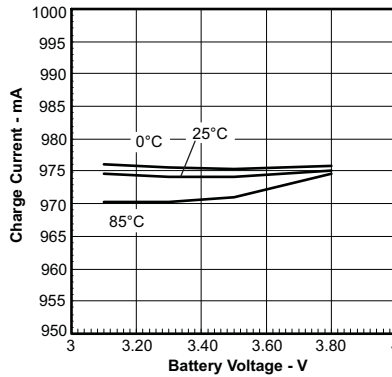


Figure 7. HIGH CHARGE RATE

**FAST-CHARGE CURRENT
vs
BATTERY VOLTAGE**

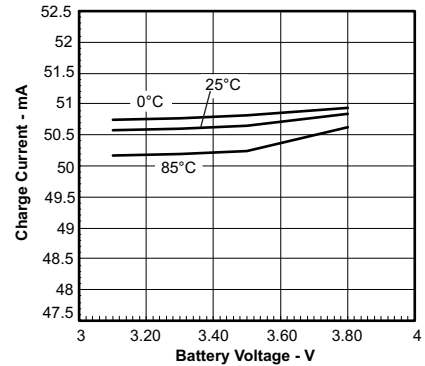


Figure 8. LOW CHARGE RATE

**KSET LINEARITY
vs
CHARGE CURRENT**

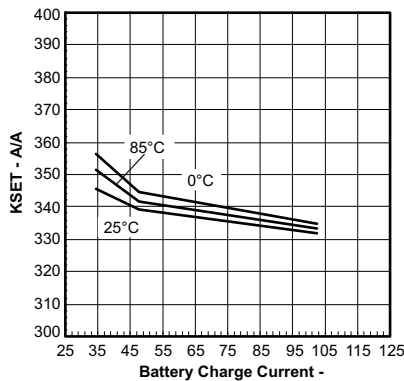


Figure 9. $2.0 < V_{(BAT)} < 3.0$ V

**KSET LINEARITY
vs
CHARGE CURRENT**

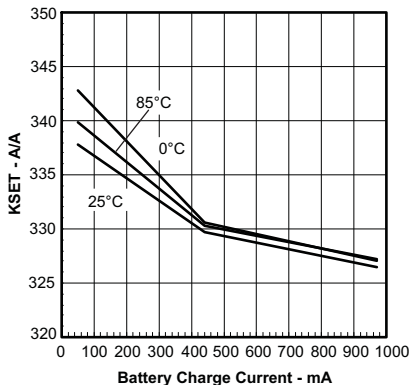


Figure 10. $3.0 < V_{(BAT)} < 4.0$ V

**BATTERY REGULATION VOLTAGE
vs
INPUT VOLTAGE**

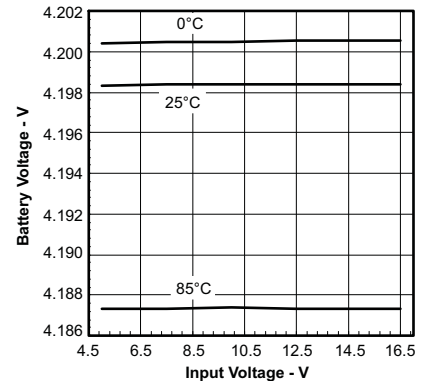


Figure 11.

**DROPOUT VOLTAGE
vs
TEMPERATURE**

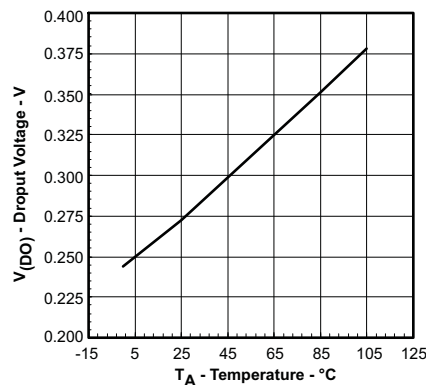


Figure 12.

FUNCTIONAL DESCRIPTION

The charge current is programmable using external components (R_{ISET} resistor). The charge process starts when an external input power is connected to the system, the charger is enabled by $\overline{CE} = LO$ and the battery voltage is below the recharge threshold, $V(BAT) < V_{(RCH)}$. When the charge cycle starts a safety timer is activated, if the safety timer function is enabled. The safety timer timeout value is set by an external resistor connected to TMR pin.

When the charger is enabled two control loops modulate the battery switch drain to source impedance to limit the BAT pin current to the programmed charge current value (charge current loop) or to regulate the BAT pin voltage to the programmed charge voltage value (charge voltage loop). If $V(BAT) < V_{(LOWV)}$ (3 V typical) the BAT pin current is internally set to 10% of the programmed charge current value.

A typical charge profile is shown below, for an operation condition that does not cause the IC junction temperature to exceed $T_{J(REG)}$, (112°C typical).

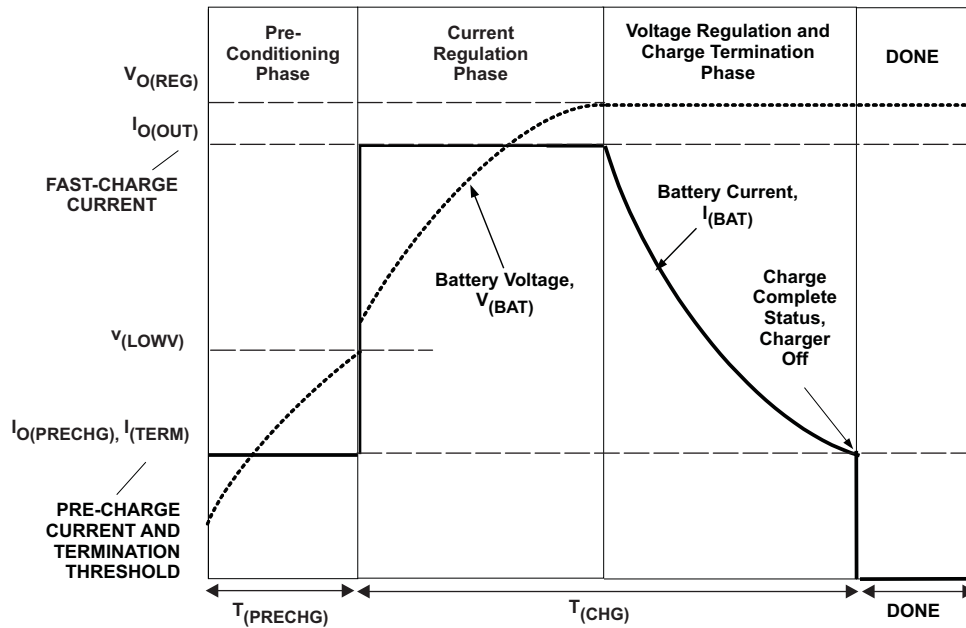


Figure 13. Charging Profile With $T_{J(REG)}$

If the operating conditions cause the IC junction temperature to exceed $T_{J(REG)}$, the charge cycle is modified, with the activation of the integrated thermal control loop. The thermal control loop is activated when an internal voltage reference, which is inversely proportional to the IC junction temperature, is lower than a fixed, temperature stable internal voltage. The thermal loop overrides the other charger control loops and reduces the charge current until the IC junction temperature returns to $T_{J(REG)}$, effectively regulating the IC junction temperature.

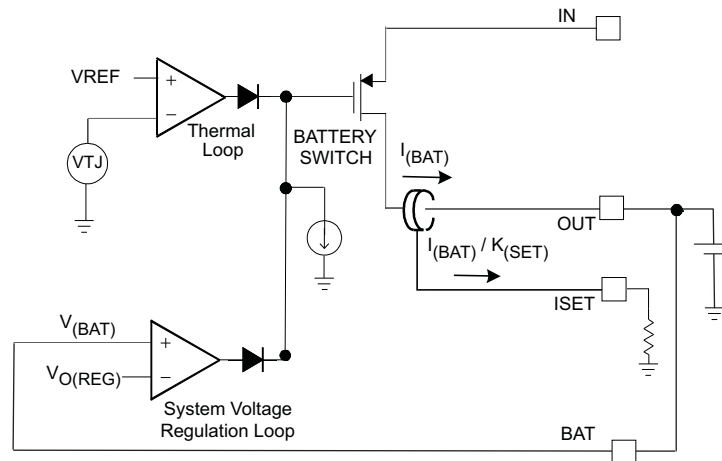


Figure 14. Thermal Regulation Circuit

A modified charge cycle, with the thermal loop active, is shown in Figure 15.

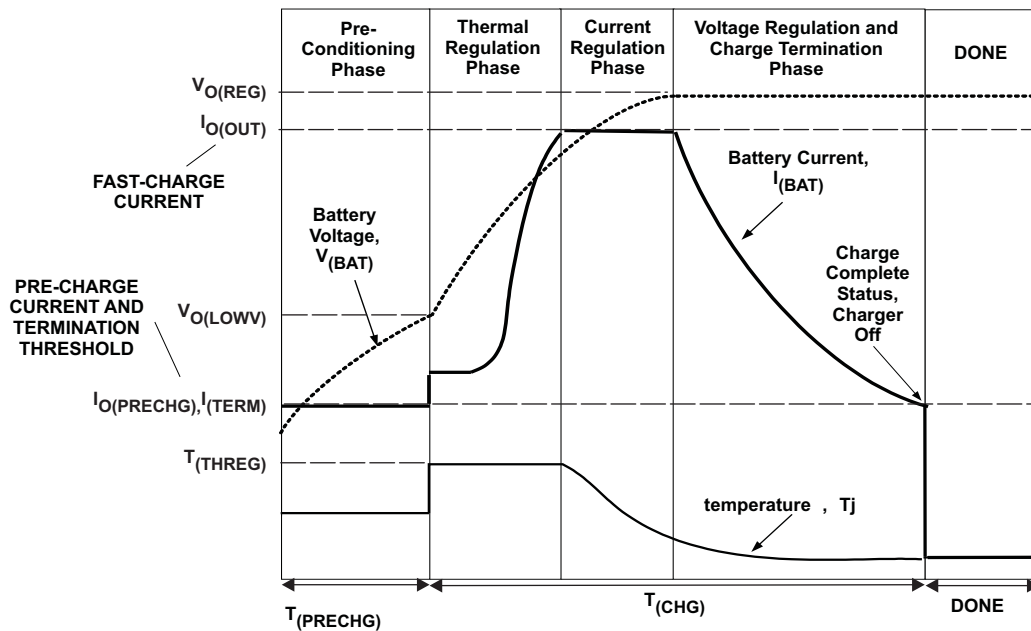
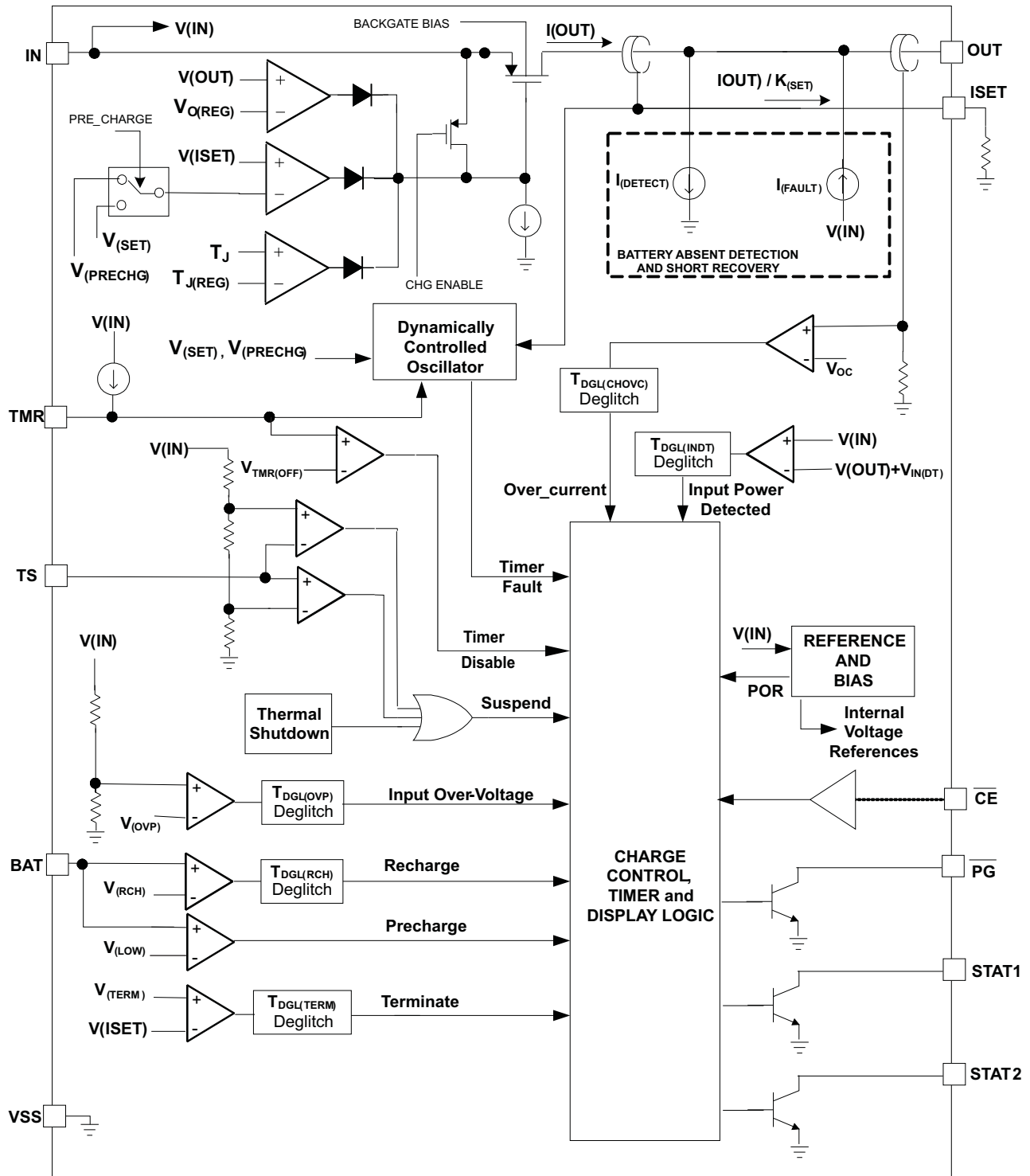


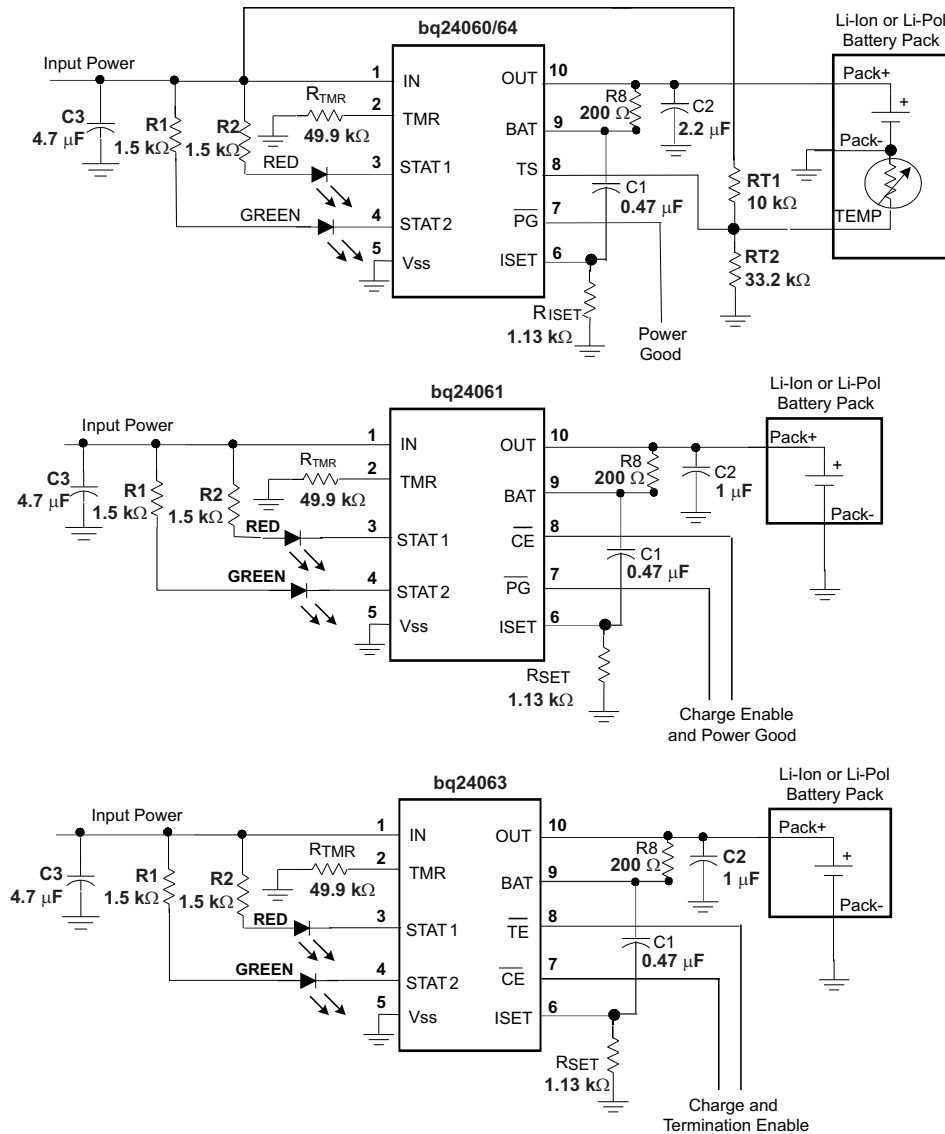
Figure 15. Charge Profile, Thermal Loop Active

FUNCTIONAL BLOCK DIAGRAM



APPLICATION CIRCUITS

The typical application diagrams shown here are configured for 750 mA fast charge current, 75 mA pre-charge current, 5 hour safety timer and 30 min pre-charge timer.



NOTE: Temp window set between 0°C and 45°C for application w/TS pin.

Figure 16. Application Circuits

OPERATING MODES

Power Down

The bq2406x family is in a power-down mode when the input power voltage (IN) is below the power-down threshold $V_{(PDWN)}$. During the power down mode all IC functions are off, and the host commands at the control pins are not interpreted. The integrated power mosfet connected between IN and OUT pins is off, the status output pins STAT1 and STAT2 are set to high impedance mode and PG output is set to the high impedance state.

Sleep Mode

The bq2406x enters the sleep mode when the input power voltage (IN) is above the power down threshold $V(\text{PDWN})$ but still lower than the input power detection threshold, $V(\text{IN}) < V(\text{OUT}) + V_{\text{IN}(\text{DT})}$.

During the sleep mode the charger is off, and the host commands at the control pins are not interpreted. The integrated power mosfet connected between IN and OUT pins is off, the status output pins STAT1 and STAT2 are set to the high impedance state and the $\overline{\text{PG}}$ output indicates input power not detected.

The sleep mode is entered from any other state, if the input power (IN) is not detected.

Overvoltage Lockout

The input power is detected when the input voltage $V(\text{IN}) > V(\text{OUT}) + V_{\text{IN}(\text{DT})}$. When the input power is detected the bq2406x transitions from the sleep mode to the power-on-reset mode. In this mode of operation an internal timer $T_{(\text{POR})}$ is started and internal blocks are reset (power-on-reset). Until the timer expires the STAT1 and STAT2 outputs indicate charger OFF, and the $\overline{\text{PG}}$ output indicates the input power status as not detected.

At the end of the power-on-reset delay the internal comparators are enabled, and the STAT1, STAT2 and $\overline{\text{PG}}$ pins are active.

Stand-By Mode

In the bq24061/63 the stand-by mode is started at the end of the power-on-reset phase, if the input power is detected and $\overline{\text{CE}} = \text{HI}$. In the stand-by mode selected blocks in the IC are operational, and the control logic monitors system status and control pins to define if the charger will set to on or off mode. The quiescent current required in stand-by mode is 100 μA typical.

If the $\overline{\text{CE}}$ pin is not available the bq2406x enters the begin charge mode at the end of the power-on-reset phase.

Begin Charge Mode

All blocks in the IC are powered up, and the bq2406x is ready to start charging the battery pack. A new charge cycle is started when the control logic decides that all conditions required to enable a new charge cycle are met. During the begin charge phase all timers are reset, after that the IC enters the charging mode.

Charging Mode

When the charging mode is active the bq2406x executes the charging algorithm, as described in the operational flow chart, [Figure 17](#).

Suspend Mode

The suspend mode is entered when the pack temperature is not within the valid temperature range. During the suspend mode the charger is set to off, but the timers are not reset.

The normal charging mode resumes when the pack temperature is within range.

LDO Mode Operation

The *LDO Mode* (TMR pin open circuit) disables the charging termination circuit, disables the battery detect routine and holds the safety timer clock in reset. This is often used for operation without a battery or in production testing. This mode is different than a typical LDO since it has different modes of operation, and delivers less current at lower output voltages. See [Figure 24](#) for the output current versus the output voltage. Note that a load on the output prior to powering the device may keep the part in short-circuit mode. Also, during normal operation, exceeding the programmed fast charge level causes the output to drop, further restricting the output power, and soon ends up in short-circuit mode. Operation with a battery or keeping the average load current below the programmed current level prevents this type of latch up. The out pin current can be monitored via the ISET pin. If in LDO mode without a battery present, It is recommended that a 200- Ω feedback resistor, R8, be used, see [Figure 16](#).

STATE MACHINE DIAGRAM

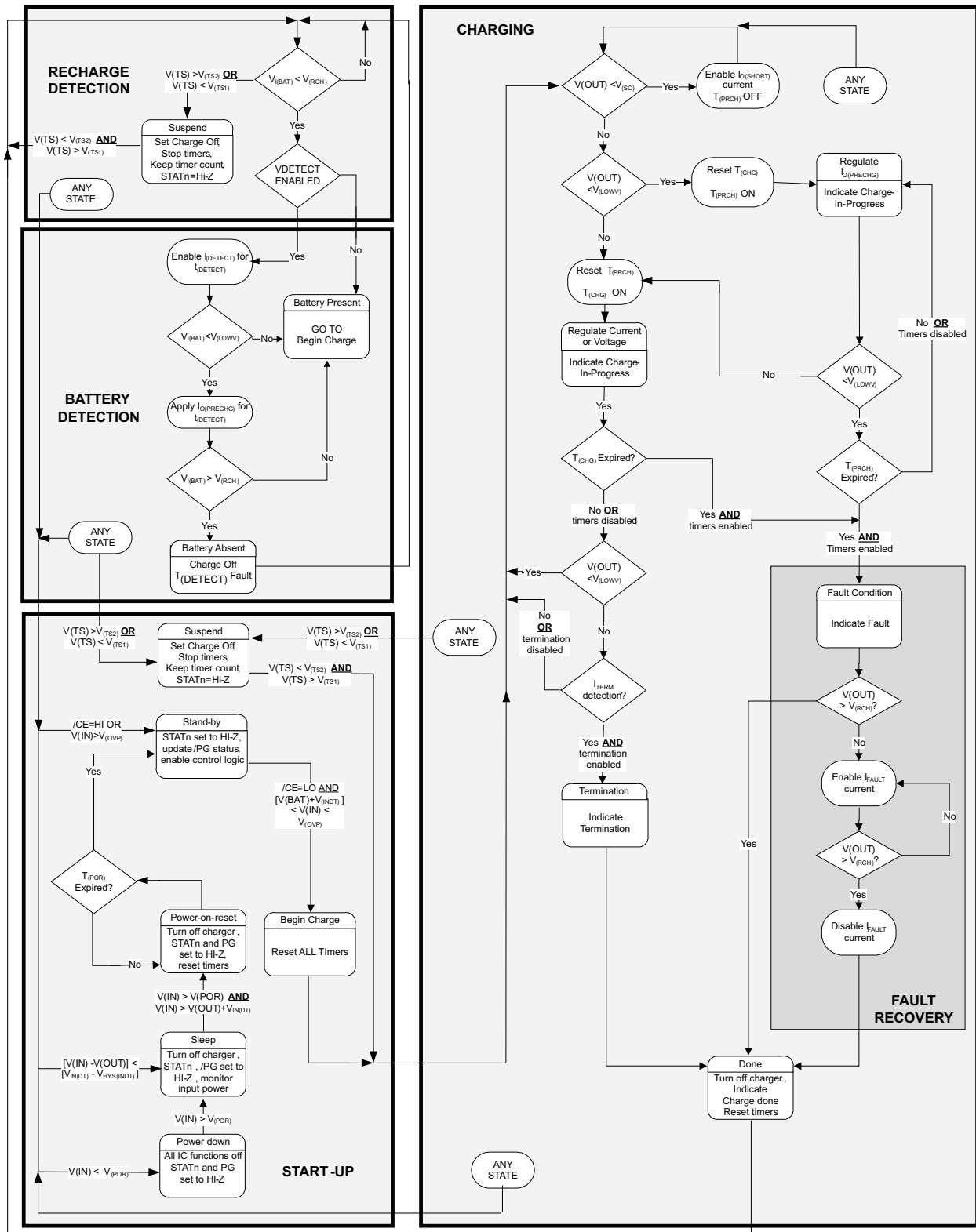


Figure 17. Operational Flow Chart

CONTROL LOGIC OVERVIEW

An external host can enable or disable the charging process using a dedicated control pin, \overline{CE} . A low-level signal on this pin enables the charge, and a high-level signal disables the charge. The bq2406x is in stand-by mode with $\overline{CE} = HI$. When the charger function is enabled ($\overline{CE} = LO$) a new charge is initiated.

Table 1 describes the charger control logic operation, in bq2406x versions without the TS pin the pack temp status is internally set to OK.

Table 1. Control Logic Functionality

| bq2406X OPERATION MODE | \overline{CE} | INPUT POWER | TIMER FAULT (latched) | OUTPUT SHORT CIRCUIT | TERMINATION (latched) | PACK TEMP | THERMAL SHUTDOWN | POWER DOWN | CHARGER POWER STAGE |
|--------------------------|-----------------|--------------|-----------------------|----------------------|-----------------------|-------------|------------------|------------|---------------------|
| POWER DOWN | LO | Low | X | X | X | X | X | Yes | OFF |
| SLEEP | X | Not Detected | X | X | X | X | X | No | OFF |
| STANDBY | HI | Detected | X | X | X | X | X | No | OFF |
| SEE STATE DIAGRAM | LO | Detected | X | Yes | X | X | X | No | |
| | LO | Detected | No | No | Yes | X | X | No | OFF |
| | LO | Detected | Yes | No | No | X | X | No | IFAULT |
| | LO | Detected | No | No | Yes | Absent | $T_J < T_{SHUT}$ | No | IDTECT |
| | LO | Detected | No | No | No | Hot or Cold | $T_J < T_{SHUT}$ | No | OFF |
| | LO | Detected | No | No | No | Ok | $T_J < T_{SHUT}$ | No | OFF |
| | LO | Over Voltage | No | No | No | Ok | $T_J < T_{SHUT}$ | No | OFF |
| CHARGING | LO | Detected | No | No | No | Ok | $T_J < T_{SHUT}$ | No | ON |

In both STANDBY and SUSPEND modes the charge process is disabled. In the STANDBY mode all timers are reset; in SUSPEND mode the timers are held at the count stored when the suspend mode was set.

The timer fault, termination and output short circuit variables shown in the control logic table are latched in the detection circuits, outside the control logic. Refer to the timers, termination and short circuit protection sections for additional details on how those latched variables are reset.

TEMPERATURE QUALIFICATION (Applies only to versions with TS pin option)

The bq2406x devices continuously monitor the battery temperature by measuring the voltage between the TS and VSS pins. The IC compares the voltage on the TS pin against the internal $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to determine if charging is allowed. Once a temperature outside the $V_{(TS1)}$ and $V_{(TS2)}$ thresholds is detected the IC immediately suspends the charge. The IC suspends charge by turning off the power FET and holding the timer value (i.e., timers are NOT reset). Charge is resumed when the temperature returns to the normal range.

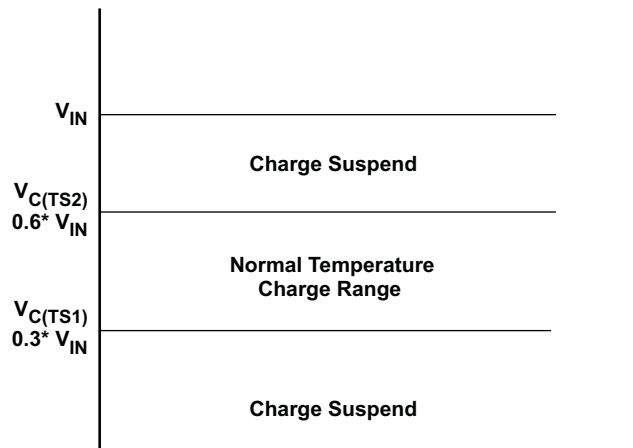


Figure 18. Battery Temperature Qualification With NTC Thermistor

The external resistors R_{T1} and R_{T2} (see application diagram) enable selecting a temperature window. If R_{TC} and R_{TH} are the thermistor impedances for the Cold and Hot thresholds the values for R_{T1} and R_{T2} can be calculated as follows, for a NTC (negative temperature coefficient) thermistor. Solve for R_{T2} first and substitute into R_{T1} equation.

$$R_{T2} = \frac{2.5 R_{TC} R_{TH}}{R_{TC} - 3.5 R_{TH}} \tag{1}$$

$$R_{T1} = \frac{7 R_{TH} R_{T2}}{3 [R_{TH} + R_{T2}]} \tag{2}$$

Applying a fixed voltage, 1/2 V_{in} (50% resistor divider from V_{in} to ground), to the TS pin to disable the temperature sensing feature.

INPUT OVERVOLTAGE DETECTION, POWER GOOD STATUS OUTPUT

The input power detection status for pin IN is shown at the open collector output pin \overline{PG} .

Table 2. Input Power Detection Status

| INPUT POWER DETECTION (IN) | \overline{PG} STATE |
|----------------------------|-----------------------|
| NOT DETECTED | High impedance |
| DETECTED, NO OVERVOLTAGE | LO |
| DETECTED, OVERVOLTAGE | High impedance |

The bq2406x detects an input overvoltage when $V(IN) > V_{(OVP)}$. When an overvoltage protection is detected the charger function is turned off and the bq2460x is set to standby mode of operation. The OVP detection is not latched, and the IC returns to normal operation when the fault condition is removed.

CHARGE STATUS OUTPUTS

The open-collector STAT1 and STAT2 outputs indicate various charger operations as shown in Table 3. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-collector transistor is turned off. When termination is disabled (TMR pin floating or $\overline{TE} = Hi$, bq24063) the Done state is not available; the status LEDs indicate fast charge if $V_{BAT} > V_{LOWV}$ and precharge if $V_{BAT} < V_{LOWV}$. The available output current is a function of the OUT pin voltage, See Figure 24.

Table 3. Charge Status⁽¹⁾

| Charge State | STAT1 | STAT2 |
|---|-------|-------|
| Precharge in progress | ON | ON |
| Fast charge in progress | ON | OFF |
| Done (termination enabled only) | OFF | ON |
| Charge Suspend (temperature) | OFF | OFF |
| Timer Fault | | |
| Charger off | | |
| Selected Input power overvoltage detected | | |
| Battery absent | | |
| Batterys short | | |

(1) Pulse loading on the OUT pin may cause the IC to cycle between Done and charging states (LEDs *Flashing*)

BATTERY CHARGING: CONSTANT CURRENT PHASE

The bq2406x family offers on-chip current regulation. The current regulation is defined by the value of the resistor connected to ISET pin.

During a charge cycle the fast charge current $I_{O(OUT)}$ is applied to the battery if the battery voltage is above the $V_{(LOWV)}$ threshold (2.95 V typical):

$$I(OUT) = I_{O(OUT)} = \frac{V_{(SET)} \times K_{SET}}{R_{ISET}} \quad (3)$$

Where $K_{(SET)}$ is the output current set factor and $V_{(SET)}$ is the output current set voltage.

During a charge cycle if the battery voltage is below the $V_{(LOWV)}$ threshold a pre-charge current $I_{(PRECHG)}$ is applied to the battery. This feature revives deeply discharged cells.

$$I(OUT) = I_{(PRECHG)} = \frac{V_{(PRECHG)} \times K_{SET}}{R_{ISET}} \sim \frac{I_{O(OUT)}}{10} \quad (4)$$

Where $K_{(SET)}$ is the output current set factor and $V_{(PRECHG)}$ is the precharge set voltage.

At low constant current charge currents, less than 350 mA, it is recommended that a 0.47- μ F capacitor be placed between the ISET and BAT pins to insure stability, see [Figure 16](#).

CHARGE CURRENT TRANSLATOR

When the charge function is enabled internal circuits generate a current proportional to the charge current at the ISET pin. This current, when applied to the external charge current programming resistor R_{ISET} generates an analog voltage that can be monitored by an external host to calculate the current sourced from the OUT pin.

$$V(ISET) = I(OUT) \times \frac{R_{ISET}}{K_{(SET)}} \quad (5)$$

BATTERY VOLTAGE REGULATION

The battery pack voltage is sensed through the BAT pin, which is tied directly to the positive side of the battery pack. The bq2406x monitors the battery pack voltage between the BAT and VSS pins. When the battery voltage rises to $V_{O(REG)}$ threshold the voltage regulation phase begins and the charging current begins to taper down. The voltage regulation threshold $V_{O(REG)}$ is fixed by an internal IC voltage reference.

PRE-CHARGE TIMER

The bq2406x family activates an internal safety timer during the battery pre-conditioning phase. The charge safety timer time-out value is set by the external resistor connected to TMR pin, R_{TMR} and the timeout constants $K_{(PCHG)}$ and $T_{(CHG)}$:

$$T_{(PCHG)} = K_{(PCHG)} \times T_{(CHG)}$$

The pre-charge timer operation is detailed in [Table 4](#).

Table 4. Pre-Charge Timer Operational Modes

| bq2460X MODE | V(OUT) > V _(LOWV) | PRE-CHARGE TIMER MODE |
|---|------------------------------|---|
| STANDBY ($\overline{CE} = \text{Hi}$) | X | RESET |
| CHARGING | Yes | RESET |
| SUSPEND (TS out of range) | Yes | RESET |
| SUSPEND (TS out of range) | No | Hold |
| CHARGING, TMR PIN NOT OPEN | No | COUNTING, EXTERNAL PROGRAMMED RATE |
| CHARGING, TMR PIN OPEN | X | RESET |

In SUSPEND mode the pre-charge timer is put on hold (i.e., pre-charge timer is not reset), normal operation resumes when the timer returns to the normal operating mode (COUNTING). If V(BAT) does not reach the internal voltage threshold $V_{(LOWV)}$ within the pre-charge timer period a fault condition is detected, the charger is turned off and the pre-charge safety timer fault condition is latched.

When the pre-charge timer fault latch is set the charger is turned off. Under those conditions a small current I_{FAULT} is applied to the OUT pin, as long as input power (IN) is detected **AND** $V(\text{OUT}) < V_{(LOWV)}$, as part of a timer fault recovery protocol. This current allows the output voltage to rise above the pre-charge threshold $V_{(LOWV)}$, resetting the pre-charge timer fault latch when the pack is removed. [Table 5](#) further details the pre-charge timer fault latch operation.

Table 5. Pre-Charge Timer Latch Functionality

| PRE-CHARGE TIMER FAULT ENTERED WHEN | PRE-CHARGE TIMER FAULT LATCH RESET AT |
|--|---|
| Pre-charge timer timeout AND $V(\text{OUT}) > V_{(LOWV)}$ | \overline{CE} rising edge or OVP detected |
| | Input power removed (not detected) |
| | Timer function disabled |

THERMAL PROTECTION LOOP

An internal control loop monitors the bq2406x junction temperature (T_J) to ensure safe operation during high power dissipations and or increased ambient temperatures. This loop monitors the bq2406x junction temperature and reduces the charge current as necessary to keep the junction temperature from exceeding, $T_{J(REG)}$, (112°C, typical).

The bq2406x's thermal loop control can reduce the charging current down to ~200mA if needed. If the junction temperature continues to rise, the IC will enter thermal shutdown.

THERMAL SHUTDOWN AND PROTECTION

Internal circuits monitor the junction temperature, T_J , of the die and suspends charging if T_J exceeds an internal threshold $T_{(SHUT)}$ (155°C typical). Charging resumes when T_J falls below the internal threshold $T_{(SHUT)}$ by approximately 20°C.

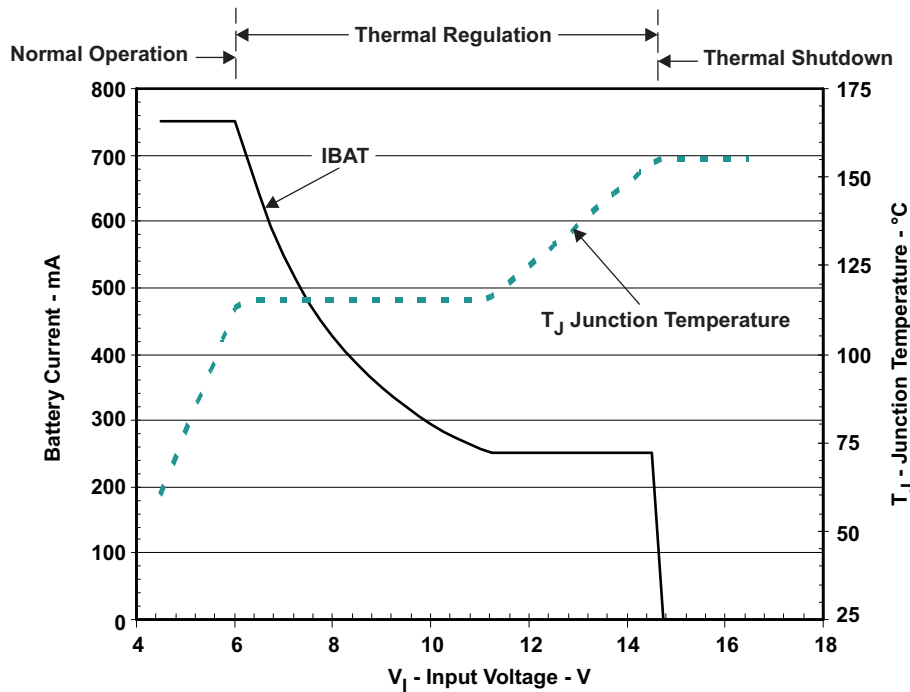


Figure 19. Thermal Regulation Loop Performance and Thermal Shutdown

DYNAMIC TIMER FUNCTION

The charge and pre-charge safety timers are programmed by the user to detect a fault condition if the charge cycle duration exceeds the total time expected under normal conditions. The expected charge time is usually calculated based on the fast charge current rate.

When the thermal loop is activated the charge current is reduced, and bq2406x activates the dynamic timer control, an internal circuit that slows down the safety timer's clock frequency. The dynamic timer control circuit effectively extends the safety time duration for either the precharge or fast charge timer modes. This minimizes the chance of a safety timer fault due to thermal regulation.

The bq2406x dynamic timer control (DTC) monitors the voltage at pin ISET during pre-charge and fast charge, and if in thermal regulation slows the clock frequency proportionately to the change in charge current. The time duration is based on a 2^{24} ripple counter, so slowing the clock frequency is a real time correction. The DTC circuit changes the safety timers clock period based on the $V_{(SET)}/V_{(ISET)}$ ratio (fast charge) or $V_{(PRECHG)}/V_{(SET)}$ ratio (pre-charge). Typical safety timer multiplier values relative to the $V_{(SET)}/V_{(ISET)}$ ratio is shown in Figure 20 and Figure 21.

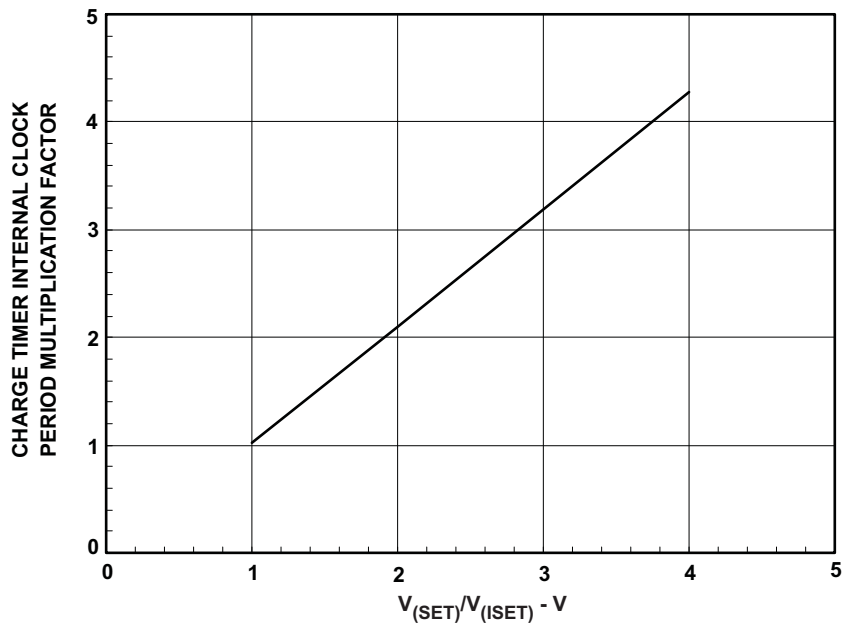


Figure 20. Safety Timer Linearity
Internal Clock Period Multiplication Factor

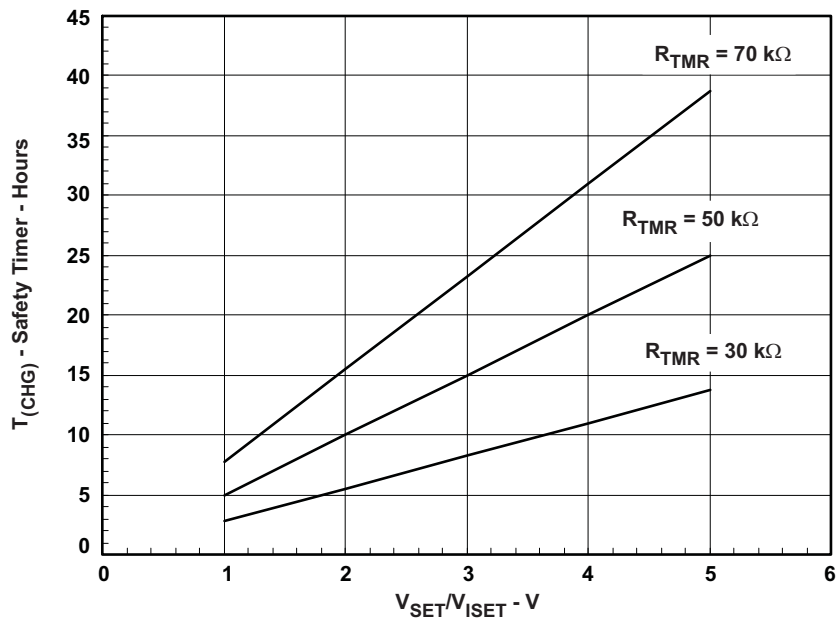


Figure 21. bq2406x Safety Timer Linearity for R_{TMR} Values

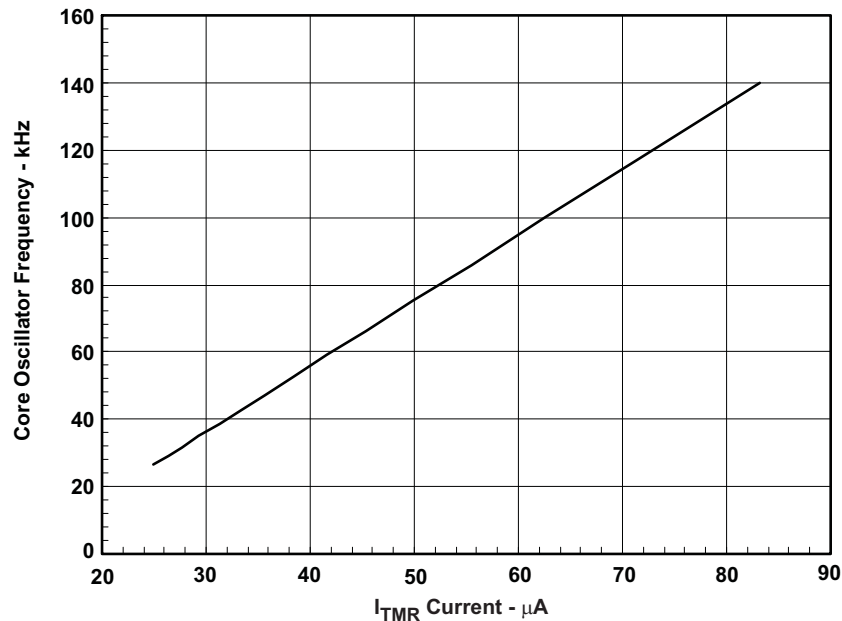


Figure 22. bq2406x Oscillator Linearity vs I_{TMR}
R_{TMR} 30 KΩ – 100 KΩ

CHARGE TERMINATION DETECTION AND RECHARGE

The charging current is monitored during the voltage regulation phase. Charge termination is indicated at the STATx pins (STAT1 = Hi-Z; STAT2 = Low) once the charge current falls below the termination current threshold I_(TERM). A deglitch period T_{DGL(TERM)} is added to avoid false termination indication during transient events.

Charge termination is not detected if the charge current falls below the termination threshold as a result of the thermal loop activation. Termination is also not detected when charger enters the suspend mode, due to detection of invalid pack temperature or internal thermal shutdown.

Table 6 describes the termination latch functionality.

Table 6. Termination Latch Functionality

| TERMINATION DETECTED LATCHED WHEN | TERMINATION LATCH RESET AT |
|---|---|
| I(OUT) < I _(TERM) AND t > T _{DGL(TERM)} AND V(OUT) > V _(RCH) | \overline{CE} rising edge or OVP detected |
| | New charging cycle started; see state diagram |
| | Termination disabled |

The termination function is DISABLED:

- In bq24060/61/64 the termination is disabled when the TMR pin is left open (floating).
- In bq24063 leaving TMR pin open (floating) does NOT disable the termination. The only way to disable termination in the bq24063 is to set \overline{TE} = HIGH.

BATTERY ABSENT DETECTION – VOLTAGE MODE ALGORITHM

The bq2406x provides a battery absent detection scheme to reliably detect insertion and/or removal of battery packs. The detection circuit applies an internal current to the battery terminal, and detects battery presence based on the terminal voltage behavior. Figure 23 has a typical waveform of the output voltage when the battery absent detection is enabled and no battery is connected:

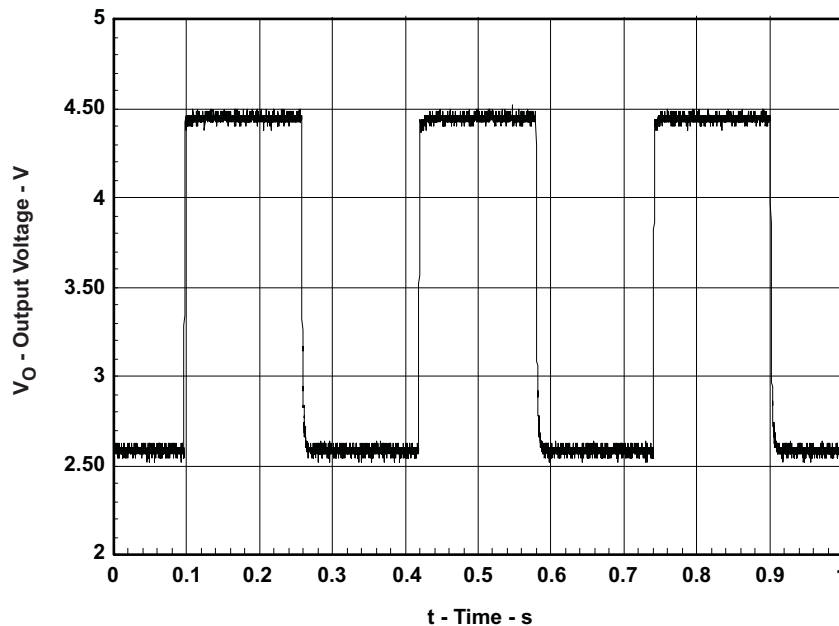


Figure 23. Battery-Absent Detection Waveforms

The battery absent detection function is disabled if the voltage at the BAT pin is held above the battery recharge threshold, $V_{(RCH)}$, after termination detection. When the voltage at the BAT pin falls to the recharge threshold, either by connection of a load to the battery or due to battery removal, the bq2406x begins a battery absent detection test. This test involves enabling a detection current, $I_{DET(DOWN)}$, for a period of $T_{(DETECT)}$ and checking to see if the battery voltage is below the pre-charge threshold, $V_{(LOWV)}$. Following this, the precharge current, $I_{DET(UP)}$ is applied for a period of $T_{(DETECT)}$ and the battery voltage checked again to be above the recharge threshold.

Passing both of the discharge and charging tests (battery terminal voltage being below the pre-charge and above the recharge thresholds on the battery detection test) indicates a battery absent fault at the STAT1 and STAT2 pins. Failure of either test starts a new charge cycle. For the absent battery condition the voltage on the BAT pin rises and falls between the $V_{(LOWV)}$ and $V_{O(REG)}$ thresholds indefinitely. See the operation flowchart for more details on this algorithm. If it is desired to power a system load without a battery, it is recommended to float the TMR pin which puts the charger in *LDD mode* (disables termination).

The battery absent detection function is disabled when the termination is disabled.

The bq2406x provides a small battery leakage current, $I_{BAT(DONE)}$ (1 μ A typical), after termination to pull down the BAT pin voltage in the event of battery removal. If the leakage on the OUT pin is higher than this pulldown current, then the voltage at the pin remains above termination and a battery-absent state will not be detected. This problem is fixed with the addition of a pulldown resistor of 2 M Ω to 4 M Ω from the OUT pin to VSS. A resistor too large (< 2 M Ω) can cause the OUT pin voltage to drop below the $V_{(LOWV)}$ threshold before the recharge deglitch (typical 25 ms) expires, causing a fault condition. In this case the bq2406x provides a fault current (typical 750 μ A) to pull the pin above the termination threshold.

CHARGE SAFETY TIMER

As a safety mechanism the bq2406x has a user-programmable timer that monitors the total fast charge time. This timer (charge safety timer) is started at the beginning of the fast charge period. The safety charge timeout value is set by the value of an external resistor connected to the TMR pin (R_{TMR}); if pin TMR is left open (floating) the charge safety timer is disabled.

The charge safety timer time-out value is calculated as follows:

$$T_{(CHG)} = [K_{(CHG)} \times R_{(TMR)}]$$

The safety timer operation modes are shown in [Table 7](#)

Table 7. Charge Safety Timer Operational Modes

| bq2460X | V(OUT) > V _(LOWV) | CHARGE SAFETY TIMER MODE |
|----------------------------|------------------------------|--------------------------|
| STANDBY | X | RESET |
| CHARGING | No | RESET |
| SUSPEND | No | RESET |
| SUSPEND | Yes | SUSPEND |
| CHARGING, TMR PIN NOT OPEN | Yes | COUNTING |
| CHARGING, TMR PIN OPEN | X | RESET |

In SUSPEND mode the charge safety timer is put on hold (i.e., charge safety timer is not reset), normal operation resumes when the TS fault is removed and the timer returns to the normal operating mode (COUNTING). If charge termination is not reached within the timer period a fault condition is detected. Under those circumstances the LED status is updated to indicate a fault condition and the charger is turned off.

When the charge safety timer fault latch is set and the charger is turned off a small current I_{FAULT} is applied to the OUT pin, as long as input power (IN) is detected **AND** V(OUT) < V_(RCHG), as part of a timer fault recovery protocol. This current allows the output voltage to rise above the recharge threshold V_(RCHG) if the pack is removed, and assures that the charge safety timer fault latch is reset if the pack is removed and re-inserted. [Table 8](#) further details the charge safety timer fault latch operation.

Table 8. Charge Safety Timer Latch Functionality

| CHARGE SAFETY TIMER FAULT ENTERED | CHARGE SAFETY TIMER FAULT LATCH RESET AT |
|-----------------------------------|---|
| V(OUT) > V _(LOW V) | CE rising edge, or OVP detected |
| | Input power removed (not detected) |
| | New charging cycle started; see state diagram |

SHORT CIRCUIT PROTECTION

The internal comparators monitor the battery voltage and detect when a short circuit is applied to the battery terminal. If the voltage at the BAT pin is less than the internal threshold V_(scind) (1.8 V typical), the STAT pins indicate a fault condition (STAT1 = STAT2 = Hi-Z). When the voltage at the BAT pin falls below a second internal threshold V_(sc) (1.4 V typical), the charger power stage is turned off. A recovery current, I_(short) (22 mA typical), is applied to the BAT pin, enabling detection of the short circuit removal. The battery output current versus battery voltage is shown in the graph, [Figure 24](#)

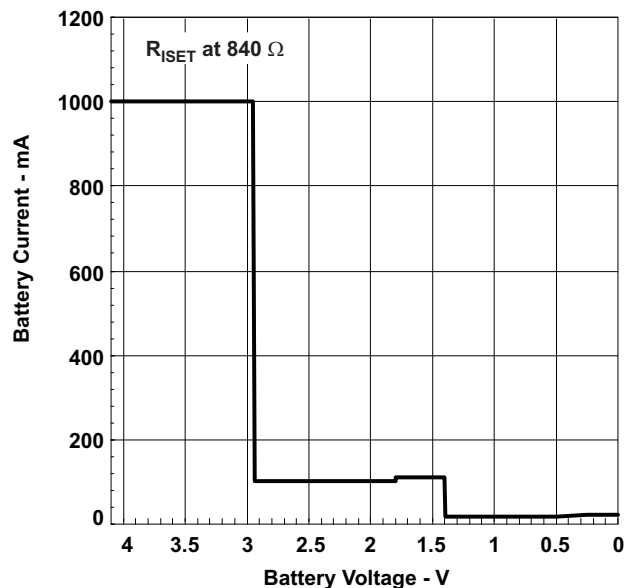


Figure 24. bq2406x Short Circuit Behavior

See the application section for additional details on start-up operation with $V(\text{BAT}) < V_{(\text{SC})}$.

STARTUP WITH DEEPLY DEPLETED BATTERY CONNECTED

The bq2406x charger furnishes the programmed charge current if a battery is detected. If no battery is connected the bq2406x operates as follows:

- The output current is limited to 22 mA (typical), if the voltage at BAT pin is below the short circuit detection threshold $V_{(\text{SC})}$, 1.8 V typical.
- The output current is regulated to the programmed pre-charge current if $V_{(\text{SC})} < V(\text{BAT}) < V_{(\text{LOWV})}$.
- The output current is regulated to the programmed fast charge current If $V(\text{BAT}) > V_{(\text{LOWV})}$ **AND** voltage regulation is not reached.

The output voltage collapses if no battery is present and the end equipment requires a bias current larger than the available charge current.

APPLICATION INFORMATION

SELECTING INPUT AND OUTPUT CAPACITOR

In most applications, all that is needed is a high-frequency decoupling capacitor on the input power pin. A 1- μ F ceramic capacitor, placed in close proximity to the IN pin and GND pad, works fine. In some applications, depending on the power supply characteristics and cable length, it may be necessary to increase the input filter capacitor to avoid exceeding the IN pin maximum voltage rating during adapter hot plug events.

The bq2406x only requires a small output capacitor for loop stability. A 0.47 μ F ceramic capacitor placed between the BAT and ISET pad is typically sufficient.

bq2406x CHARGER DESIGN EXAMPLE

Requirements

- Supply voltage = 5 V
- Safety timer duration of 5 hours for fast charge
- Fast charge current of approximately 750 mA
- Battery temp sense is not used

Calculations

Program the charge current for 750 mA:

$$R_{\text{ISET}} = [V_{\text{(SET)}} \times K_{\text{(SET)}} / I_{\text{(OUT)}}]$$

from electrical characteristics table. . . $V_{\text{(SET)}} = 2.5 \text{ V}$

from electrical characteristics table. . . $K_{\text{(SET)}} = 335$

$$R_{\text{ISET}} = [2.5 \text{ V} \times 335 / 0.75 \text{ A}] = 1.12 \text{ k}\Omega$$

Selecting the closest standard value, use a 1.13 k Ω resistor connected between ISET (pin 6) and ground.

Program 5-hour safety timer timeout:

$$R_{\text{(TMR)}} = [T_{\text{(CHG)}} / K_{\text{(CHG)}}]$$

from the electrical characteristics table. . . $K_{\text{(CHG)}} = 0.1 \text{ hr} / \text{k}\Omega$

$$K_{\text{(TMR)}} = [5 \text{ hrs} / (0.1 \text{ hr} / \text{k}\Omega)] = 50 \text{ k}\Omega$$

Selecting the closest standard value, use a 49.9 k Ω resistor connected between TMR (pin 2) and ground.

Disable the temp sense function:

A constant voltage between V_{TS1} and V_{TS2} on the TS input disables the temp sense function.

from electrical characteristics table. . . $V_{\text{(TS1)}} = 30\% \times V_{\text{IN}}$

from electrical characteristics table. . . $V_{\text{(TS2)}} = 61\% \times V_{\text{IN}}$

A constant voltage of $50\% \times V_{\text{in}}$ disables the temp sense function, so a divide-by-2 resistor divider connected between V_{in} and ground can be used. Two 1-m Ω resistors keeps the power dissipated in this divider to a minimum.

For a 0–45°C range with a Semitec 103AT thermistor, the thermistor values are 4912 at 450°C and 2728k at 0°C. RT1 (top resistor) and RT2 (bottom resistor) are calculated as follows:

APPLICATION INFORMATION (continued)

$$R_{T2} = \frac{2.5 R_{TC} R_{TH}}{R_{TC} - 3.5 R_{TH}} = \frac{2.5 (27.28k) (4.912k)}{27.28k - 3.5(4.912k)} = 33.2k;$$

$$R_{T1} = \frac{7 R_{TH} R_{T2}}{3 [R_{TH} + R_{T2}]} = \frac{7 (4.921k) (33.2k)}{3 [4.921k + 33.2k]} = 10k$$

(6)

| PIN | COMPONENTS |
|-----------------------------|---|
| IN | In most applications, the minimum input capacitance needed is a 0.1 μ F ceramic decoupling capacitor near the input pin connected to ground (preferably to a ground plane through vias). The recommended amount of input capacitance is 1 μ F or at least as much as on the output pin. This added capacitance helps with hot plug transients, input inductance and initial charge transients. |
| OUT | There is no minimum value for capacitance for this output, but it is recommended to connect a 1 μ F ceramic capacitor between OUT and ground. This capacitance helps with termination, and cycling frequency between <i>charge done</i> and refresh charge when no battery is present. It also helps cancel out any battery lead inductance for long leaded battery packs. It is recommended to put as much ceramic capacitance on the input as the output so as not to cause a drop out of the input when charging is initiated. |
| ISET/BAT | For stability reasons, it may be necessary to put a 0.47- μ F capacitor between the ISET and BAT pin.. |
| STAT1/2 and \overline{PG} | Optional (LED STATUS – See below, Processor Monitored; or no status) |
| STAT1 | Connect the cathode of a red LED to the open-collector STAT1 output, and connect the anode of the red LED to the input supply through a 1.5 k Ω resistor that limits the current. |
| STAT2 | Connect the cathode of a green LED to the open-collector STAT2 output, and connect the anode of the green LED to the input supply through a 1.5 k Ω resistor that limits the current. |
| \overline{PG} | Connect the cathode of an LED to the open-collector \overline{PG} output, and connect the anode of the LED to the input supply through a 1.5 k Ω resistor to limit the current. |

THERMAL CONSIDERATIONS

The bq2406x family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note (SLUA271)*.

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta(JA) = \frac{T_J - T_A}{P}$$

(7)

Where:

T_J = chip junction temperature

T_A = ambient temperature

P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow

APPLICATION INFORMATION (continued)

- Whether other surfaces are in close proximity to the device being tested

The device power dissipation, P , is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged :

$$P = [V(IN) - V(OUT)] \times I(OUT)$$

Due to the charge profile of Li-Ion batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See the charging profile, [Figure 13](#) .

If the board thermal design is not adequate the programmed fast charge rate current may not be achieved under maximum input voltage and minimum battery voltage, as the thermal loop can be active effectively reducing the charge current to avoid excessive IC junction temperature.

USING ADAPTERS WITH LARGE OUTPUT VOLTAGE RIPPLE

Some low cost adapters implement a half rectifier topology, which causes the adapter output voltage to fall below the battery voltage during part of the cycle. To enable operation with low cost adapters under those conditions the bq2406x family keeps the charger on for at least 30 msec (typical) after the input power puts the part in sleep mode. This feature enables use of external low cost adapters using 50 Hz networks.

The backgate control circuit prevents any reverse current flowing from the battery to the adapter terminal during the charger off delay time.

Note that the \overline{PG} pin is not deglitched, and it indicates input power loss immediately after the input voltage falls below the output voltage. If the input source frequently drops below the output voltage and recovers, a small capacitor can be used from \overline{PG} to VSS to prevent \overline{PG} flashing events.

PCB LAYOUT CONSIDERATIONS

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq2406x, with short trace runs to both IN, OUT and GND (thermal pad).
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bq2406x family are packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note (SLUA271)*.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| BQ24060DRCCR | ACTIVE | VSON | DRC | 10 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BPG | Samples |
| BQ24060DRCT | ACTIVE | VSON | DRC | 10 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BPG | Samples |
| BQ24061DRCCR | ACTIVE | VSON | DRC | 10 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BPH | Samples |
| BQ24061DRCT | ACTIVE | VSON | DRC | 10 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BPH | Samples |
| BQ24064DRCCR | ACTIVE | VSON | DRC | 10 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BSA | Samples |
| BQ24064DRCT | ACTIVE | VSON | DRC | 10 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BSA | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ24060DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24060DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24060DRCT | VSON | DRC | 10 | 250 | 180.0 | 12.5 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24060DRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24061DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24061DRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24064DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24064DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24064DRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24064DRCT | VSON | DRC | 10 | 250 | 180.0 | 12.5 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ24060DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ24060DRCR | VSON | DRC | 10 | 3000 | 338.0 | 355.0 | 50.0 |
| BQ24060DRCT | VSON | DRC | 10 | 250 | 338.0 | 355.0 | 50.0 |
| BQ24060DRCT | VSON | DRC | 10 | 250 | 210.0 | 185.0 | 35.0 |
| BQ24061DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ24061DRCT | VSON | DRC | 10 | 250 | 210.0 | 185.0 | 35.0 |
| BQ24064DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ24064DRCR | VSON | DRC | 10 | 3000 | 338.0 | 355.0 | 50.0 |
| BQ24064DRCT | VSON | DRC | 10 | 250 | 210.0 | 185.0 | 35.0 |
| BQ24064DRCT | VSON | DRC | 10 | 250 | 338.0 | 355.0 | 50.0 |

GENERIC PACKAGE VIEW

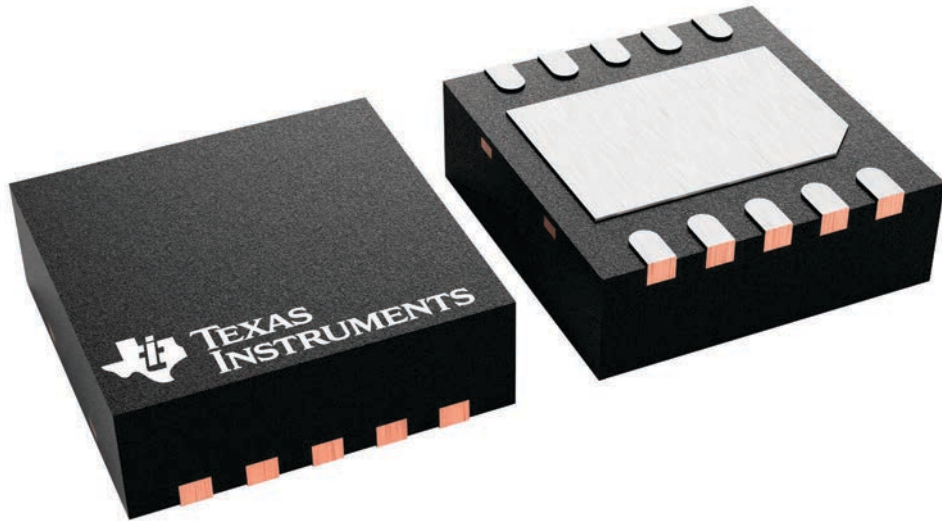
DRC 10

VSON - 1 mm max height

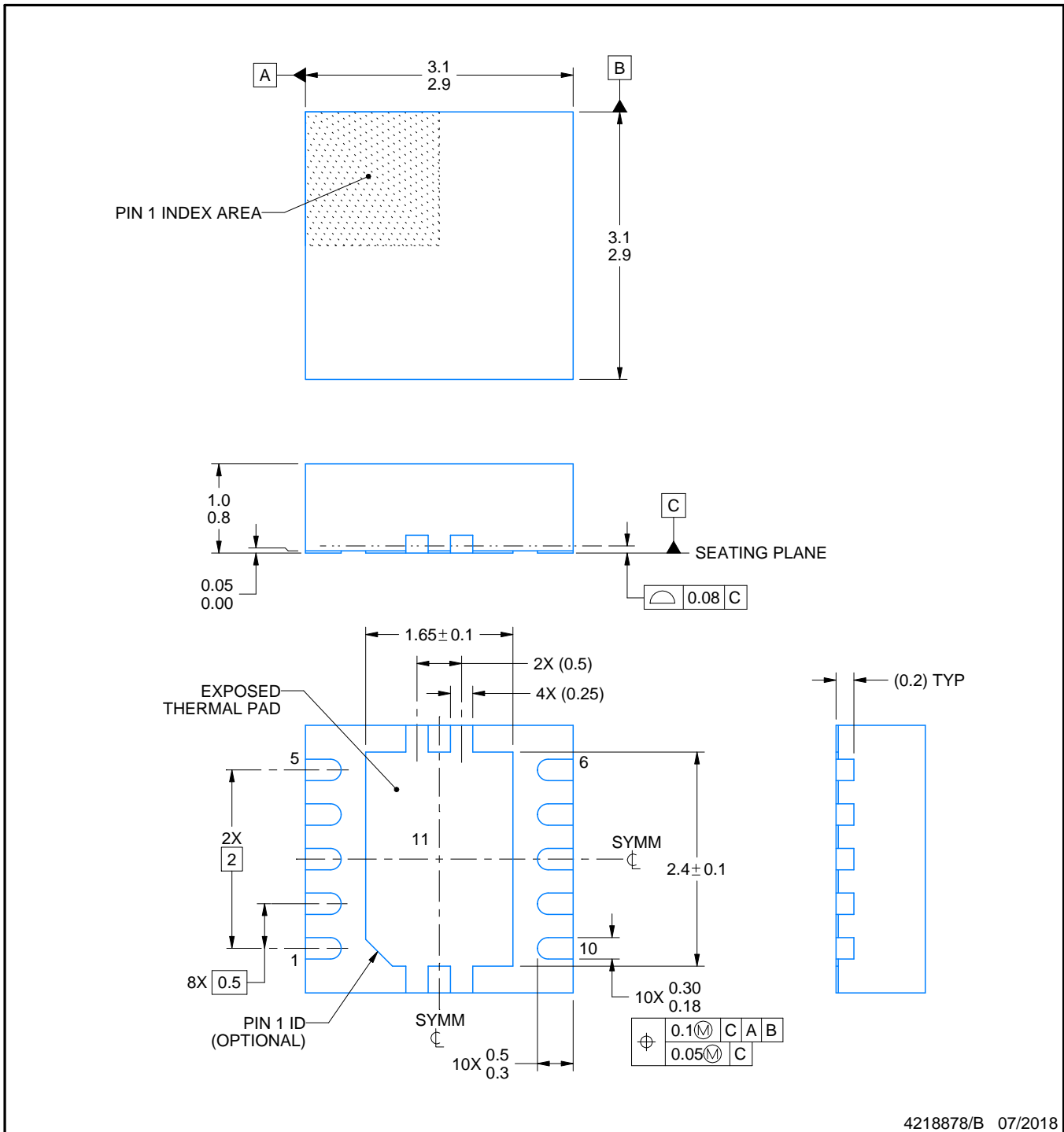
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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