具有 NTC 监控和电源路径且符合汽车标准的 bq24079QW-Q1 4.1V 电池电压锂离子电池充电器

1 特性

- 符合汽车类应用的 应用
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4A
- 完全符合 USB 充电器标准
  - 最大输入电流可选 100mA 和 500mA
  - 100mA 最大电流限制可确保充电符合 USB-IF 标准
  - 基于输入的动态电源管理 (V_{IN}-DPM)，用于保护免受不良 USB 电源损害
- 28V 输入额定值，具有过压保护
- 4.1V 电池稳压电压
- 集成动态电源路径管理 (DPPM) 功能可同时独立进行系统供电和对电池充电
- 具有用于进行电流监控的输出 (ISET)，可支持高达 1.5A 的充电电流
- 针对墙式充电器的高达 1.5A 的可编程输入电流限制
- 带有 SYSOFF 输入的电池断开功能。
- 可编程预充电和快速充电安全计时器
- 反向电流、短路和热保护
- 负温度系数 (NTC) 热敏电阻输入
- 私有启动序列限制涌入电流
- 状态指示 - 充电中/已完成、电源正常
- 具有可湿性的小型 3mm × 3mm 16 引线 VQFN 封装

2 应用

- 汽车远程信息处理
- 车队管理
- 显示密钥/智能密钥

3 说明

bq24079QW-Q1 是一款集成型锂离子线性充电器和系统电源路径管理器件，适用于空间受限的汽车 应用，例如远程信息处理/eCall。此器件可通过 4.35V 到 6.4V 电压的运行，最高支持 1.5A 的充电电流。它们在输入电压范围内具有输入电压保护功能，因此支持非稳压适配器。bq24079QW-Q1 的 USB 输入电流限制精度和启动序列使得这款器件能够符合 USB-IF 涌入电流规范。此外，输入动态电源管理 (V_{IN}-DPM) 可防止系统负载损毁错误配置的 USB 源。

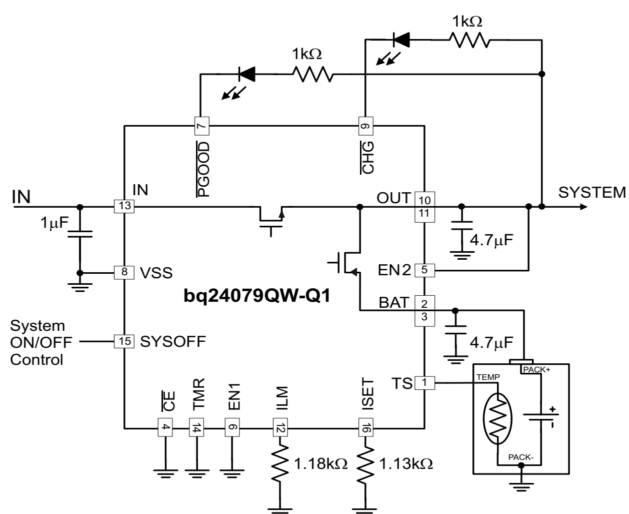
bq24079QW-Q1 具有 动态电源路径管理 (DPPM) 功能，可在为系统供电的同时独立为电池充电。当输入电流限制引起系统输出降至 DPPM 阈值时，DPPM 电路将减少充电电流；因此，可在为系统负载供电的同时单独监测充电电流。此特性以及 4.1V 电池稳压电压有助于减少电池的充放电次数，实现正常充电终止，并让系统能够在电池组故障或缺失的情况下运行，从而延长电池寿命。

器件信息(1)

器件编号	封装	封装尺寸（标称值）
bq24079QW-Q1	VQFN (16)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (November 2017) to Revision B — **Page**

- 已更改 将特性中的 HBM ESD 分类等级从 H1C 更改为 2 ... 1
- Changed ESD Ratings HBM to All pins value ±2000 V ... 5

Changes from Original (October 2017) to Revision A — **Page**

- 已更改 标题 ... 1
- Changed Standby current into IN pin MAX from 50 to 55 µA ... 6

5 （说明 （续））

此外，该系列充电器可提供经稳压的系统输入，即使在电池完全放电的情况下，也可使系统在连接电源后实现瞬间开启。此电源路径管理架构还允许在适配器不能够发送峰值系统电流时补偿系统电流需求，从而使得能够使用较小的适配器。

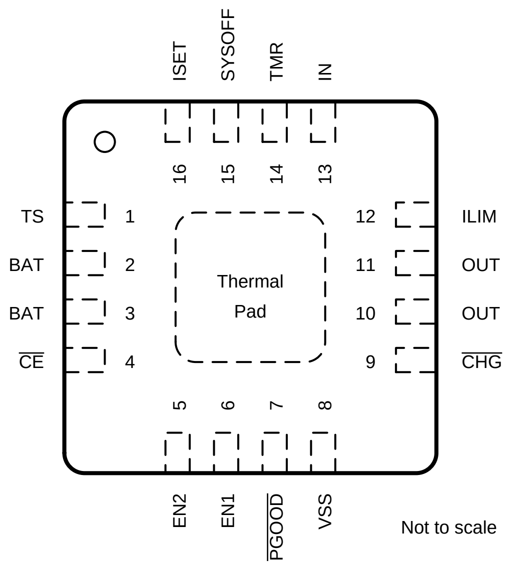
电池充电发生于以下三个阶段：调节、恒定电流和恒定电压。在所有的充电阶段，一个内部控制环路监测 IC 结温并且如果超过此内部温度阈值则减少充电电流。充电器功率级和充电电流感应功能完全集成在了一起。该充电器具高精度电流和电压调节环路、充电状态显示和充电终止功能。输入电流限制和充电电流可使用外部电阻编程设定。

6 Device Comparison Table

DEVICE	V_{OVP}	$V_{BAT(REG)}$	$V_{OUT(REG)}$	V_{DPPM}	OPTIONAL FUNCTION
bq24079QW-Q1	6.6 V	4.1 V	5.5 V	4.3 V	SYSOFF

7 Pin Configuration and Functions

**RGT Package
16 Pin VQFN
Top View**



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
TS	1	I	External NTC Thermistor Input. Connect the TS input to the NTC thermistor in the battery pack. TS monitors a 10-kΩ NTC thermistor. For applications that do not utilize the TS function, connect a 10-kΩ fixed resistor from TS to VSS to maintain a valid voltage level on TS. Do not leave TS pin floating.
BAT	2, 3	I/O	Charger Power Stage Output and Battery Voltage Sense Input. Connect BAT to the positive terminal of the battery. Bypass BAT to VSS with a 4.7-μF to 47-μF ceramic capacitor.
$\overline{\text{CE}}$	4	I	Charge Enable Active-Low Input. Connect $\overline{\text{CE}}$ to a high logic level to suspend charging. When $\overline{\text{CE}}$ is high, OUT is active and battery supplement mode is still available. Connect $\overline{\text{CE}}$ to a low logic level to enable the battery charger. $\overline{\text{CE}}$ is internally pulled down with ~285 kΩ. Do not leave $\overline{\text{CE}}$ unconnected to ensure proper operation.
EN2	5	I	Input Current Limit Configuration Inputs. Use EN1 and EN2 control the maximum input current and enable USB compliance. See EN1/EN2 Settings table for the description of the operation states. EN1 and EN2 are internally pulled down with ∓285 kΩ. Do not leave EN1 or EN2 unconnected to ensure proper operation.
EN1	6	I	
$\overline{\text{PGOOD}}$	7	O	Open-drain Power Good Status Indication Output. $\overline{\text{PGOOD}}$ pulls to VSS when a valid input source is detected. $\overline{\text{PGOOD}}$ is high-impedance when the input power is not within specified limits. Connect $\overline{\text{PGOOD}}$ to the desired logic voltage rail using a 1-kΩ to 100-kΩ resistor, or use with an LED for visual indication.
VSS	8	–	Ground. Connect to the thermal pad and to the ground rail of the circuit.
$\overline{\text{CHG}}$	9	O	Open-Drain Charging Status Indication Output. $\overline{\text{CHG}}$ pulls to VSS when the battery is charging. $\overline{\text{CHG}}$ is high impedance when charging is complete and when charger is disabled. Connect $\overline{\text{CHG}}$ to the desired logic voltage rail using a 1-kΩ to 100-kΩ resistor, or use with an LED for visual indication.
OUT	10, 11	O	System Supply Output. OUT provides a regulated output when the input is below the OVP threshold and above the regulation voltage. When the input is out of the operation range, OUT is connected to V_{BAT} except when SYSOFF is high. Connect OUT to the system load. Bypass OUT to VSS with a 4.7-μF to 47-μF ceramic capacitor.
ILIM	12	I	Adjustable Current Limit Programming Input. Connect a 1100-Ω to 8-kΩ resistor from ILIM to VSS to program the maximum input current (EN2 = 1, EN1 = 0). The input current includes the system load and the battery charge current. Leaving ILIM unconnected disables all charging.
IN	13	I	Input Power Connection. Connect IN to the external DC supply (AC adapter or USB port). The input operating range is 4.35 V to 6.6 V. The input can accept voltages up to 26 V without damage but operation is suspended. Connect bypass capacitor 1 μF to 10 μF to VSS.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
TMR	14	I	Timer Programming Input. TMR controls the pre-charge and fast-charge safety timers. Connect TMR to VSS to disable all safety timers. Connect a 18-kΩ to 72-kΩ resistor between TMR and VSS to program the timers a desired length. Leave TMR unconnected to set the timers to the default values.
SYSOFF	15	I	System Enable Input. Connect SYSOFF high to turn off the FET connecting the battery to the system output. When an adapter is connected, charging is also disabled. Connect SYSOFF low for normal operation. SYSOFF is internally pulled up to V_{BAT} through a large resistor (~5 MΩ). Do not leave SYSOFF unconnected to ensure proper operation.
ISET	16	I/O	Fast Charge Current Programming Input. Connect a 590-Ω to 8.9-kΩ resistor from ISET to VSS to program the fast charge current level. Charging is disabled if ISET is left unconnected. While charging, the voltage at ISET reflects the actual charging current and can be used to monitor charge current. See the *Charge Current Translator* section for more details.
Thermal Pad	–	–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

8 Specifications

8.1 Absolute Maximum Ratings[(1)]

over the -40°C to 125°C operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage, V_I	IN (with respect to VSS)	–0.3	28	V
	BAT (with respect to VSS)	–0.3	5	V
	OUT, EN1, EN2, $\overline{CE}$, TS, ISET, $\overline{PGOOD}$, $\overline{CHG}$, ILIM, TMR, SYSOFF	–0.3	7	V
Input current, I_I	IN		1.6	A
Output current (Continuous), I_O	OUT		5	A
	BAT (Discharge mode)		5	A
	BAT (Charging mode)		1.5[(2)]	A
Output sink current	$\overline{CHG}$, $\overline{PGOOD}$		15	mA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) The IC operational charging life is reduced to 20,000 hours, when charging at 1.5A and 125°C. The thermal regulation feature reduces charge current if the IC's junction temperature reaches 125°C; thus without a good thermal design the maximum programmed charge current may not be reached.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge[(1)]	Human-body model (HBM), per AEC Q100-002[(2)]	All pins	±2000	V
		Charged-device model (CDM), per AEC Q100-011		±500	

(1) Electrostatic discharge (ESD) measures device sensitivity and immunity to damage caused by assembly line electrostatic discharges.
(2) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_I	IN voltage range	4.35	26	V
	IN operating voltage range	4.35	6.4	V
I_{IN}	Input current, IN pin		1.5	A
I_{OUT}	Current, OUT pin		4.5	A
I_{BAT}	Current, BAT pin (Discharging)		4.5	A

Recommended Operating Conditions (continued)

		MIN	MAX	UNIT
I_{CHG}	Current, BAT pin (Charging)		1.5[(1)]	A
R_{ILIM}	Maximum input current programming resistor	1100	8000	Ω
R_{ISET}	Fast-charge current programming resistor [(2)]	590	8900	Ω
R_{ITERM}	Termination current programming resistor	0	15	kΩ
R_{TMR}	Timer programming resistor	18	72	kΩ

(1) The IC operational charging life is reduced to 20,000 hours, when charging at 1.5A and 125°C. The thermal regulation feature reduces charge current if the IC's junction temperature reaches 125°C; thus without a good thermal design the maximum programmed charge current may not be reached.
(2) Use a 1% tolerance resistor for R_{ISET} to avoid issues with the R_{ISET} short test when using the maximum charge current setting.

8.4 Thermal Information

THERMAL METRIC[(1)]		bq24079QW-Q1 RGT (VQFN) 16 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

Over ambient temperature range (–40°C ≤ T_A ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Undervoltage lock-out	V_{IN}: 0 V → 4 V	3.2	3.3	3.4	V
V_{hys}	Hysteresis on UVLO	V_{IN}: 4 V → 0 V	200		300	mV
$V_{IN(DT)}$	Input power detection threshold	Input power detected when $V_{IN} > V_{BAT} + V_{IN(DT)}$ V_{BAT} = 3.6 V, V_{IN}: 3.5 V → 4 V	50	80	135	mV
V_{hys}	Hysteresis on $V_{IN(DT)}$	V_{BAT} = 3.6 V, V_{IN}: 4 V → 3.5 V	20			mV
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	Time measured from V_{IN}: 0 V → 5 V with 1-µs rise time to $\overline{PGOOD}$ = LO		1.2		ms
V_{OVP}	Input overvoltage protection threshold	V_{IN}: 5 V → 7 V	6.4	6.6	6.8	V
V_{hys}	Hysteresis on OVP	V_{IN}: 7 V → 5V		110		mV
$t_{DGL(OVP)}$	Input overvoltage blanking time (OVP fault deglitch)			50		µs
t_{REC}	Input overvoltage recovery time	Time measured from V_{IN}: 11 V → 5 V with 1-µs fall time to $\overline{PGOOD}$ = LO		1.2		ms
ILIM, ISET SHORT CIRCUIT DETECTION (CHECKED DURING STARTUP)						
I_{SC}	Current source	V_{IN} > UVLO and $V_{IN} > V_{BAT} + V_{IN(DT)}$		1.3		mA
V_{SC}		V_{IN} > UVLO and $V_{IN} > V_{BAT} + V_{IN(DT)}$		520		mV
QUIESCENT CURRENT						
$I_{BAT(PDWN)}$	Sleep current into BAT pin	$\overline{CE}$ = LO or HI, Input power not detected, No load on OUT pin, T_A ≤ 125°C		4.4	13	µA
I_{IN}	Standby current into IN pin	EN1 = HI, EN2 = HI, V_{IN} = 6 V, T_A ≤ 125°C		38.8	55	µA
		EN1 = HI, EN2 = HI, V_{IN} = 10 V, T_A ≤ 125°C		90.2	200	
I_{CC}	Active supply current, IN pin	$\overline{CE}$ = LO, V_{IN} = 6 V, No load on OUT pin, $V_{BAT} > V_{BAT(REG)}$, (EN1, EN2) ≠ (HI, HI)			1.5	mA

Electrical Characteristics (continued)

Over ambient temperature range (–40°C ≤ T_A ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER PATH						
$V_{DO(IN-OUT)}$	$V_{IN} – V_{OUT}$	V_{IN} = 4.3 V, I_{IN} = 1 A, V_{BAT} = 4.1 V		300	475	mV
$V_{DO(BAT-OUT)}$	$V_{BAT} – V_{OUT}$	I_{OUT} = 1 A, V_{IN} = 0 V, V_{BAT} > 3 V		50	100	mV
$V_{O(REG)}$	OUT pin voltage regulation	$V_{IN} > V_{OUT} + V_{DO(IN-OUT)}$	5.4	5.5	5.65	V
$I_{IN}max$	Maximum input current	EN1 = LO, EN2 = LO	90	95	101	mA
		EN1 = HI, EN2 = LO	440	475	500	mA
		EN2 = HI, EN1 = LO		K_{ILIM}/R_{ILIM}		A
K_{ILIM}	Maximum input current factor	I_{LIM} = 500 mA to 1.5 A	1500	1610	1720	AΩ
		I_{LIM} = 200 mA to 500 mA	1300	1525	1770	AΩ
$I_{IN}max$	Programmable input current limit range	EN2 = HI, EN1 = LO, R_{ILIM} = 8 kΩ to 1.1 kΩ	200		1500	mA
V_{IN-DPM}	Input voltage threshold when input current is reduced	EN2 = LO, EN1 = X	4.35	4.5	4.63	V
V_{DPPM}	Output voltage threshold when charging current is reduced		4.2	4.3	4.4	V
V_{BSUP1}	Enter battery supplement mode	V_{BAT} = 3.6 V, R_{ILIM} = 1.5 kΩ, R_{LOAD} = 10 Ω → 2 Ω		$V_{OUT} \le V_{BAT}$ –40mV		V
V_{BSUP2}	Exit battery supplement mode	V_{BAT} = 3.6 V, R_{ILIM} = 1.5 kΩ, R_{LOAD} = 2 Ω → 10 Ω		$V_{OUT} \ge V_{BAT}$–20mV		V
$V_{O(SC1)}$	Output short-circuit detection threshold, power-on	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$	0.8	0.9	1	V
$V_{O(SC2)}$	Output short-circuit detection threshold, supplement mode $V_{BAT} – V_{OUT} > V_{O(SC2)}$ indicates short-circuit	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$	200	250	300	mV
$t_{DGL(SC2)}$	Deglitch time, supplement mode short circuit			250		µs
$t_{REC(SC2)}$	Recovery time, supplement mode short circuit			60		ms
BATTERY CHARGER						
I_{BAT}	Source current for BAT pin short-circuit detection	V_{BAT} = 1.5 V	4	7.5	11	mA
$V_{BAT(SC)}$	BAT pin short-circuit detection threshold	V_{BAT} rising	1.6	1.8	2	V
$V_{BAT(REG)}$	Battery charge voltage		4.059	4.100	4.141	V
V_{LOWV}	Pre-charge to fast-charge transition threshold	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$	2.9	3	3.1	V
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			25		ms
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			25		ms
I_{CHG}	Battery fast charge current range	$V_{BAT(REG)} > V_{BAT} > V_{LOWV}$, V_{IN} = 5 V, $\overline{CE}$ = LO, EN1 = LO, EN2 = HI	100		1500	mA
	Battery fast charge current	$\overline{CE}$ = LO, EN1= LO, EN2 = HI, $V_{BAT} > V_{LOWV}$, V_{IN} = 5 V, $I_{IN}max > I_{CHG}$, No load on OUT pin, Thermal loop and DPPM loop not active		K_{ISET}/R_{ISET}		A
K_{ISET}	Fast charge current factor		797	890	975	AΩ
I_{PRECHG}	Pre-charge current			K_{PRECHG}/R_{ISET}		A
K_{PRECHG}	Pre-charge current factor		55	88	118	AΩ
I_{TERM}	Termination comparator detection threshold (internally set)	$\overline{CE}$ = LO, (EN1, EN2) ≠ (LO, LO), $V_{BAT} > V_{RCH}$, t < t_{MAXCH}, V_{IN} = 5 V, DPPM loop and thermal loop not active	0.09×I_{CHG}	0.1×I_{CHG}	0.11×I_{CHG}	A
		$\overline{CE}$ = LO, (EN1, EN2) = (LO, LO), $V_{BAT} > V_{RCH}$, t < t_{MAXCH}, V_{IN} = 5 V, DPPM loop and thermal loop not active	0.027×I_{CHG}	0.033×I_{CHG}	0.040×I_{CHG}	A
$t_{DGL(TERM)}$	Deglitch time, termination detected			25		ms
V_{RCH}	Recharge detection threshold	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$	50	100	145	mV
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected			62.5		ms

Electrical Characteristics (continued)

Over ambient temperature range (–40°C ≤ T_A ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DGL(NO-IN)}$	Delay time, input power loss to OUT LDO turn-off	V_{BAT} = 3.6 V. Time measured from V_{IN}: 5 V → 3 V, 1-µs fall time		20		ms
$I_{BAT(DET)}$	Sink current for battery detection	V_{BAT} = 2.5 V	5	7.5	10	mA
t_{DET}	Battery detection timer	BAT high or low		250		ms
BATTERY CHARGING TIMERS						
t_{PRECHG}	Pre-charge safety timer value	TMR = floating	1440	1800	2160	s
t_{MAXCHG}	Charge safety timer value	TMR = floating	14400	18000	21600	s
t_{PRECHG}	Pre-charge safety timer value	18 kΩ < R_{TMR} < 72 kΩ		R_{TMR} × K_{TMR}		s
t_{MAXCHG}	Charge safety timer value	18 kΩ < R_{TMR} < 72 kΩ		10×R_{TMR} ×K_{TMR}		s
K_{TMR}	Timer factor		36	48	60	s/kΩ
BATTERY-PACK NTC MONITOR(1)						
I_{NTC}	NTC bias current	V_{IN} > UVLO and V_{IN} > V_{BAT} + $V_{IN(DT)}$	71	75	80	µA
V_{HOT}	High temperature trip point	Battery charging, V_{TS} Falling	270	300	330	mV
$V_{HYS(HOT)}$	Hysteresis on high trip point	Battery charging, V_{TS} Rising from V_{HOT}		30		mV
V_{COLD}	Low temperature trip point	Battery charging, V_{TS} Rising	2000	2100	2200	mV
$V_{HYS(COLD)}$	Hysteresis on low trip point	Battery charging, V_{TS} Falling from V_{COLD}		300		mV
$t_{DGL(TS)}$	Deglitch time, pack temperature fault detection	TS fault detected to charger disable		50		ms
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature	T_J Rising		155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON EN1, EN2, $\overline{CE}$, SYSOFF						
V_{IL}	Logic LOW input voltage		0		0.4	V
V_{IH}	Logic HIGH input voltage		1.4		6	V
I_{IL}	Input sink current	V_{IL}= 0 V			1	µA
I_{IH}	Input source current	V_{IH}= 1.4 V			10	µA
LOGIC LEVELS ON $\overline{PGOOD}$, $\overline{CHG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.4	V

(1) These numbers set trip points of 0°C and 50°C while charging, with 3°C hysteresis on the trip points, with a Vishay Type 2 curve NTC with an R25 of 10 kΩ.

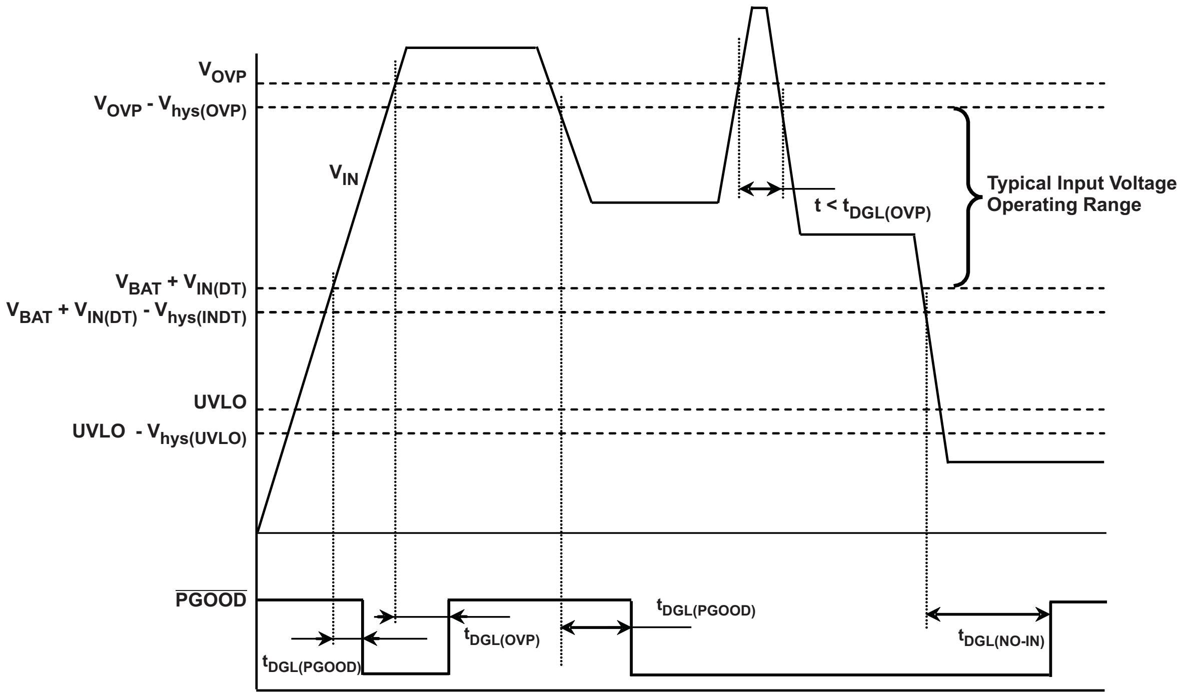


图 1. Power-Up, Power-Down, Power Good Indication

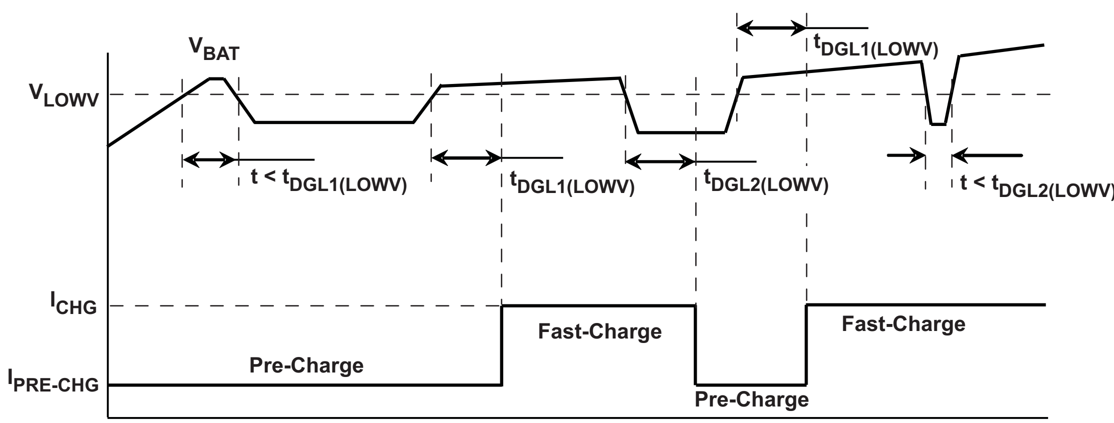


图 2. Pre- to Fast-Charge, Fast- to Pre-Charge Transition – $t_{DGL1(LOWV)}$, $t_{DGL2(LOWV)}$

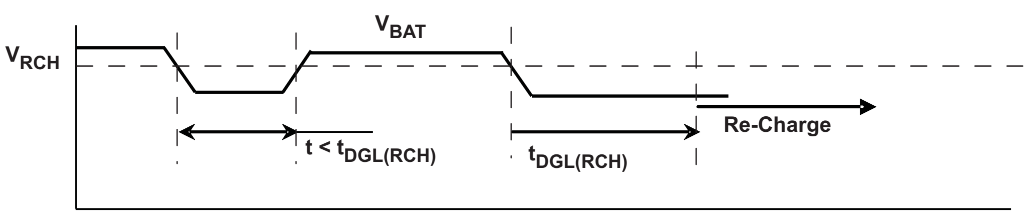


图 3. Recharge – $t_{DGL(RCH)}$

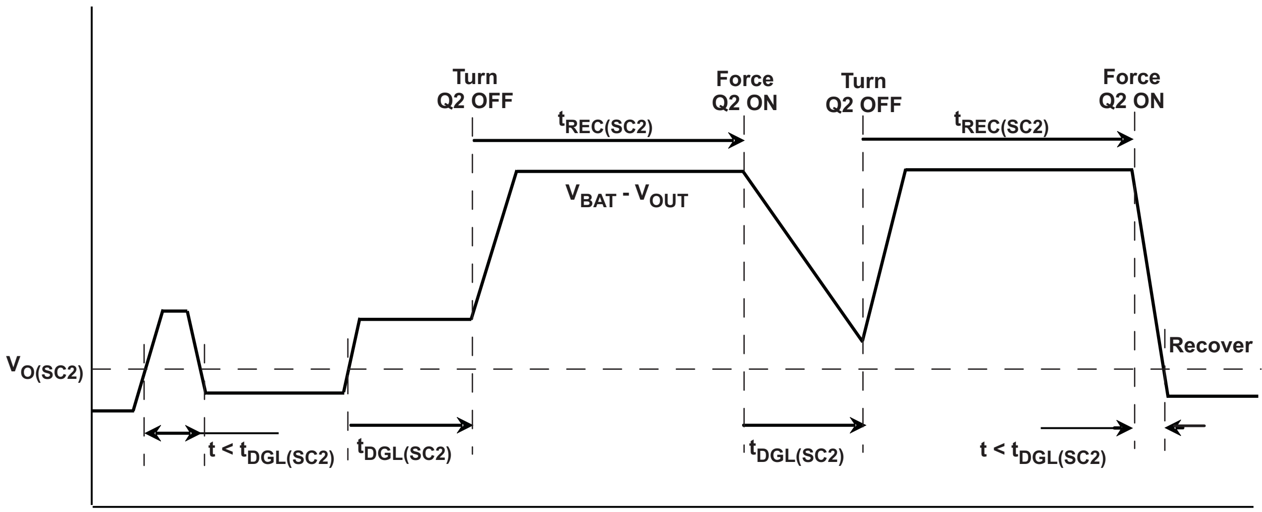


图 4. OUT Short-Circuit – Supplement Mode

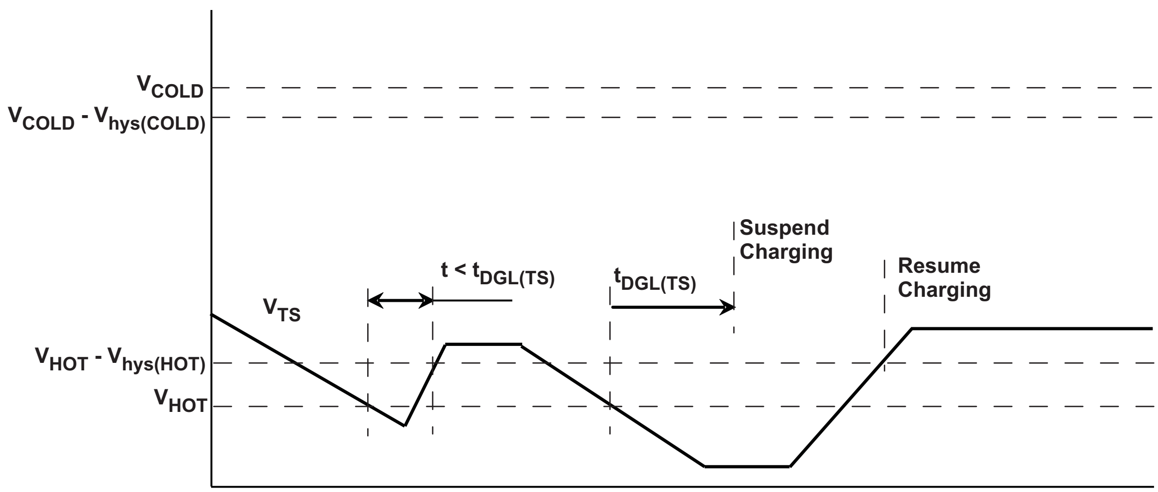


图 5. Battery Pack Temperature Sensing – TS Pin. Battery Temperature Increasing

8.6 Typical Characteristics

V_{IN} = 6 V, EN1 = 1, EN2 = 0, T_A = 25°C, unless otherwise noted.

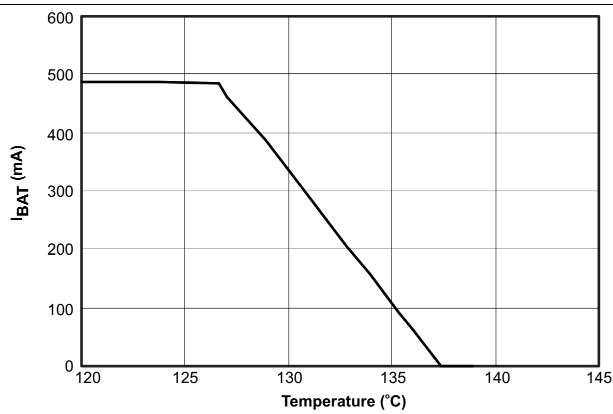
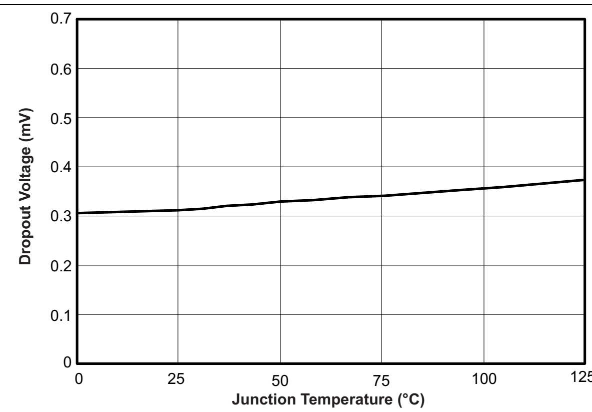
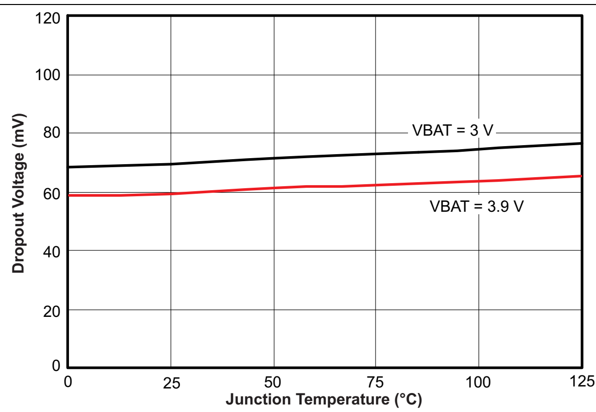


图 6. Thermal Regulation



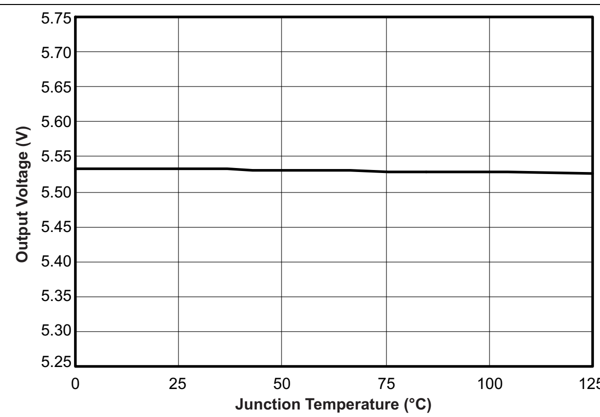
I_L = 1 A

图 7. Dropout Voltage vs Temperature



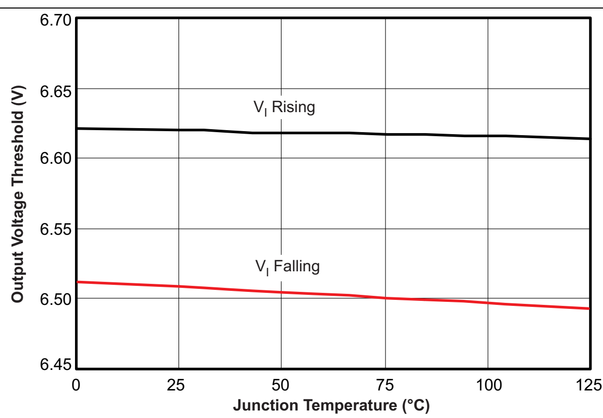
I_L = 1 A, No Input Supply

图 8. Dropout Voltage vs Temperature



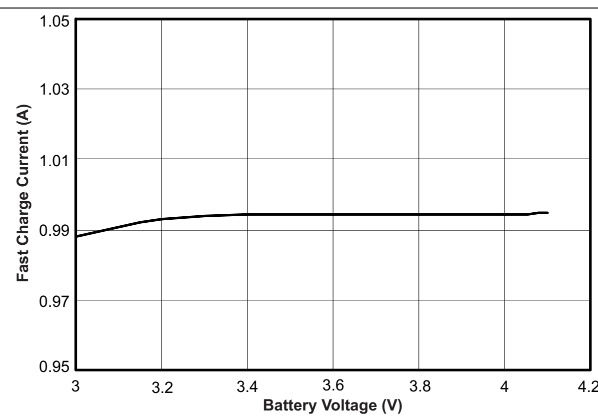
V_{IN} = 6 V, I_L = 1 A

图 9. Output Regulation Voltage vs Temperature - bq24079QW-Q1



6.6 V

图 10. Overvoltage Protection Threshold vs Temperature

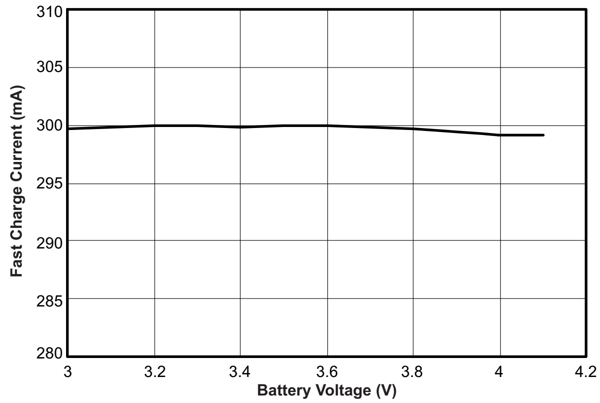


R_{ISET} = 900 Ω

图 11. Fastcharge Current vs Battery Voltage

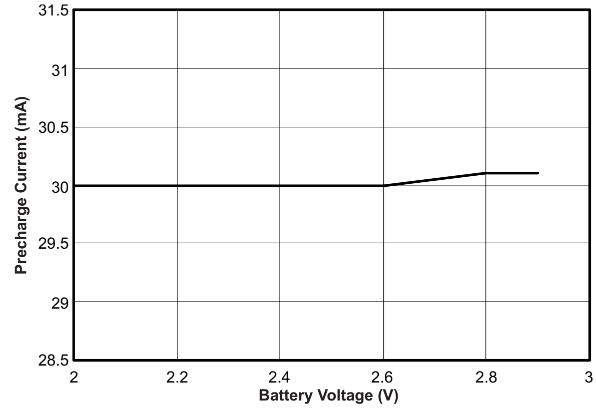
Typical Characteristics (接下页)

V_{IN} = 6 V, EN1 = 1, EN2 = 0, T_A = 25°C, unless otherwise noted.



R_{ISET} = 3 kΩ

图 12. Fastcharge Current vs Battery Voltage



R_{ISET} = 3 kΩ

图 13. Precharge Current vs Battery Voltage

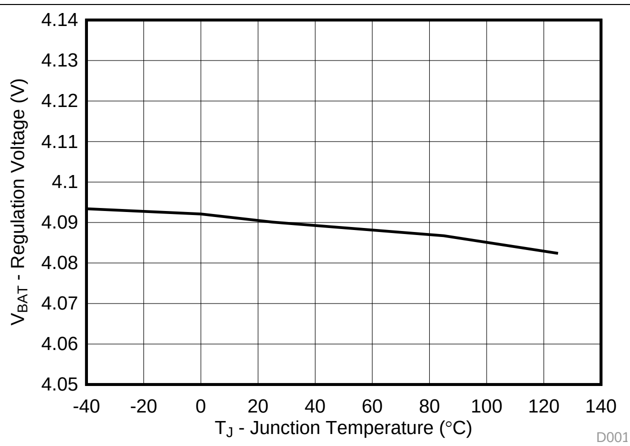


图 14. BAT Regulation Voltage vs Temperature

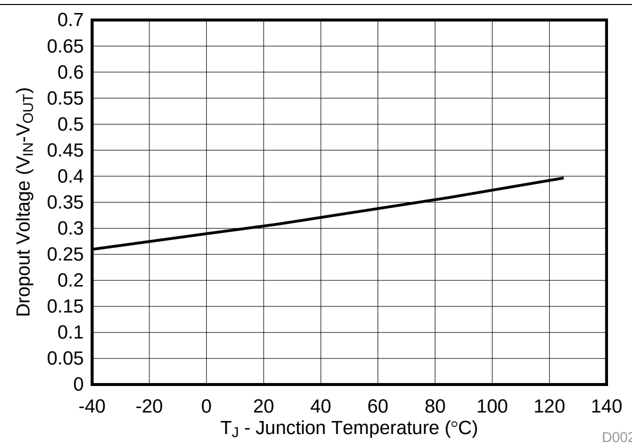
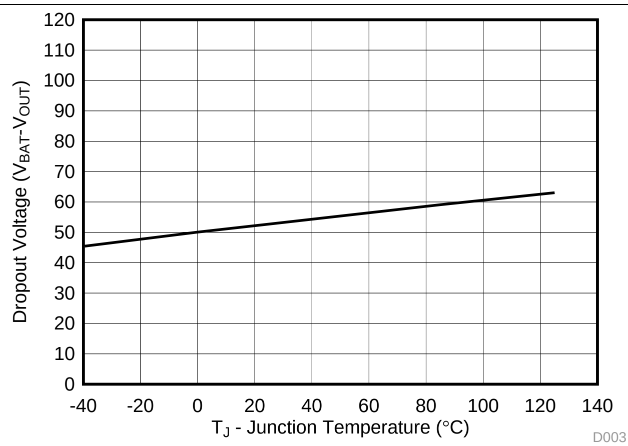


图 15. Dropout Voltage vs Temperature



I_L = 1 A

图 16. Dropout Voltage vs Temperature

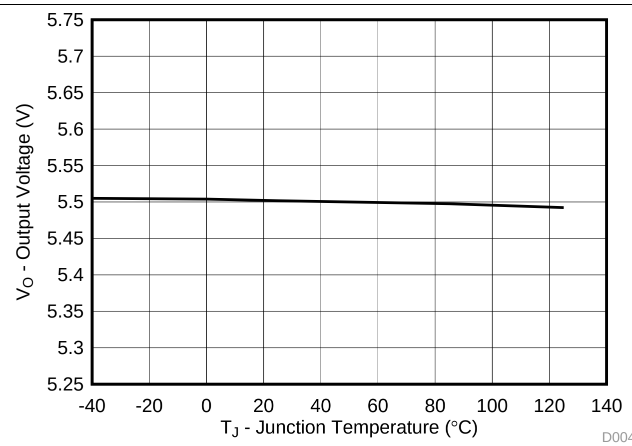


图 17. Output Regulation Voltage vs Temperature

Typical Characteristics (接下页)

V_{IN} = 6 V, EN1 = 1, EN2 = 0, T_A = 25°C, unless otherwise noted.

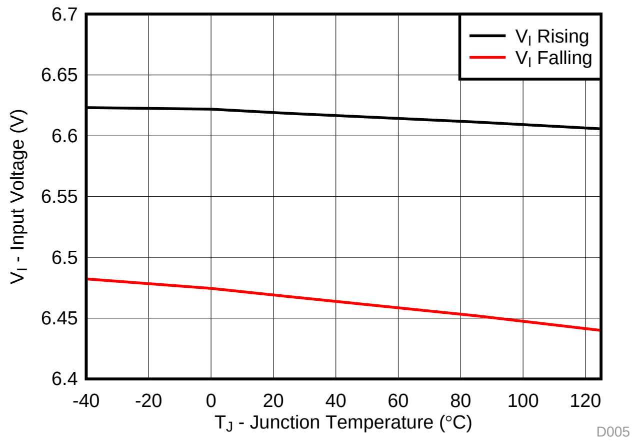


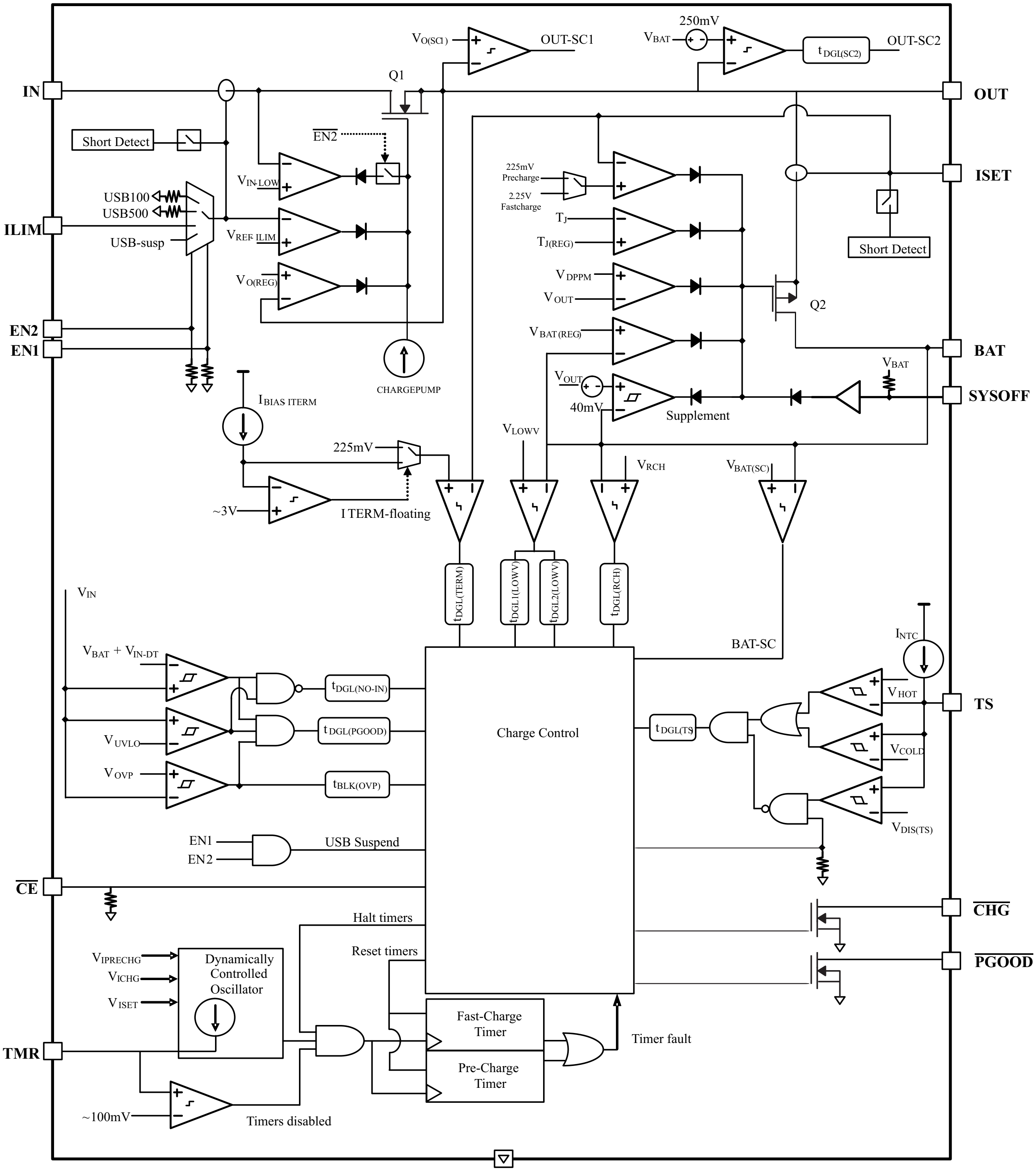
图 18. Input Voltage vs Temperature

9 Detailed Description

9.1 Overview

The bq24079QW-Q1 device is an integrated Li-Ion linear charger and system power path management device targeted at space-limited portable applications. The device powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack. It also allows instant system turn-on even with a totally discharged battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port. The device features Dynamic Power Path Management (DPPM), which shares the source current between the system and battery charging, and automatically reduces the charging current if the system load increases. When charging from a USB port, the input dynamic power management (V_{IN}-DPM) circuit reduces the input current if the input voltage falls below a threshold, preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Undervoltage Lockout (UVLO)

The bq24079QW-Q1 remains in power down mode when the input voltage at the IN pin is below the undervoltage threshold (UVLO).

During the power down mode, the host commands at the control inputs ($\overline{\text{CE}}$, EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{\text{CHG}}$ and $\overline{\text{PGOOD}}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. (If SYSOFF is high, Q2 is off). During power down mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

9.3.2 Power On

When V_{IN} exceeds the UVLO threshold, the bq24079QW-Q1 powers up. While V_{IN} is below $V_{BAT} + V_{IN(DT)}$, the host commands at the control inputs ($\overline{\text{CE}}$, EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{\text{CHG}}$ and $\overline{\text{PGOOD}}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. (If SYSOFF is high, Q2 is off). During this mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

Once V_{IN} rises above $V_{BAT} + V_{IN(DT)}$, $\overline{\text{PGOOD}}$ is driven low to indicate the valid power status and the $\overline{\text{CE}}$, EN1, and EN2 inputs are read. The device enters standby mode if (EN1 = EN2 = HI) or if an input overvoltage condition occurs. In standby mode, Q1 is OFF and Q2 is ON so OUT is connected to the battery input. (If SYSOFF is high, FET Q2 is off). During this mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

When the input voltage at IN is within the valid range: V_{IN} > UVLO ***AND*** $V_{IN} > V_{BAT} + V_{IN(DT)}$ ***AND*** $V_{IN} < V_{OVP}$, and the EN1 and EN2 pins indicate that the USB suspend mode is not enabled [(EN1, EN2) ≠ (HI, HI)], all internal timers and other circuit blocks are activated. The device then checks for short-circuits at the ISET and ILIM pins. If no short conditions exists, the device switches on the input FET Q1 with a 100mA current limit to checks for a short circuit at OUT. When V_{OUT} is above $V_{O(SC1)}$, the FET Q1 switches to the current limit threshold set by EN1, EN2 and R_{ILIM} and the device enters into the normal operation. During normal operation, the system is powered by the input source (Q1 is regulating), and the device continuously monitors the status of $\overline{\text{CE}}$, EN1 and EN2 as well as the input voltage conditions.

Feature Description (接下页)

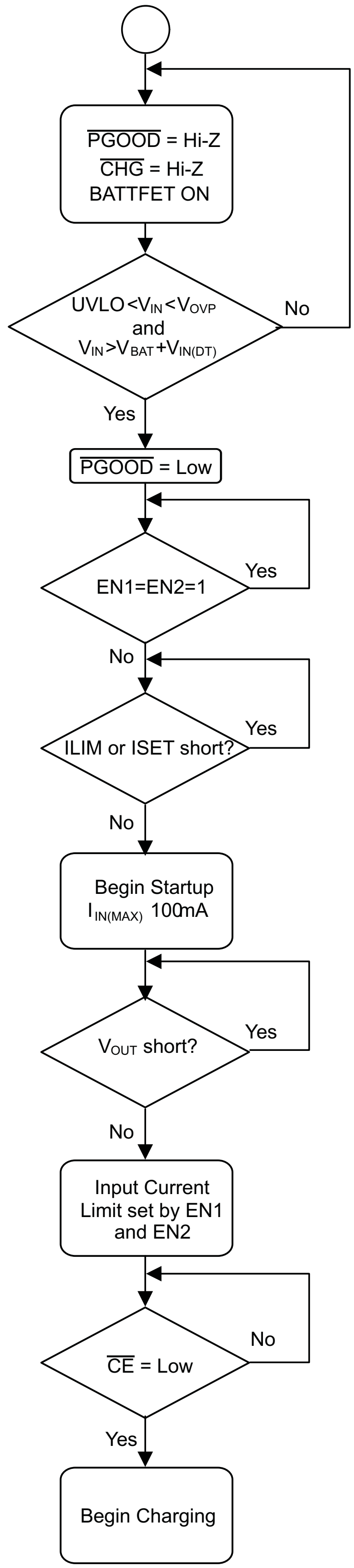


图 19. Startup Flow Diagram

Feature Description (接下页)

9.3.3 Overvoltage Protection (OVP)

The bq24079QW-Q1 accepts inputs up to 28 V without damage. Additionally, an overvoltage protection (OVP) circuit is implemented that shuts off the internal LDO and discontinues charging when $V_{IN} > V_{OVP}$ for a period long than $t_{DGL(OVP)}$. When in OVP, the system output (OUT) is connected to the battery and $\overline{PGOOD}$ is high impedance. Once the OVP condition is removed, a new power on sequence starts (See the *Power On* section). The safety timers are reset and a new charge cycle will be indicated by the $\overline{CHG}$ output.

9.3.4 Dynamic Power-path Management

The bq24079QW-Q1 features an OUT output that powers the external load connected to the battery. This output is active whenever a source is connected to IN or BAT when SYSOFF is low. The following sections discuss the behavior of OUT with a source connected to IN to charge the battery and a battery source only.

9.3.4.1 Input Source Connected (Adapter or USB)

With a source connected, the dynamic power-path management (DPPM) circuitry of the bq24079QW-Q1 monitors the input current continuously. The OUT output for the bq24079QW-Q1 is regulated to a fixed voltage ($V_{O(REG)}$). The current into IN is shared between charging the battery and powering the system load at OUT. The bq24079QW-Q1 has internal selectable current limits of 100 mA (USB100) and 500 mA (USB500) for charging from USB ports, as well as a resistor-programmable input current limit.

The bq24079QW-Q1 is USB IF compliant for the inrush current testing. The USB spec allows up to 10 µF to be hard started, which establishes 50 µC as the maximum inrush charge value when exceeding 100 mA. The input current limit for the bq24079QW-Q1 prevents the input current from exceeding this limit, even with system capacitances greater than 10 µF. Note that the input capacitance to the device must be selected small enough to prevent a violation (<10 µF), as this current is not limited. 图 20 demonstrates the startup of the bq24079QW-Q1 and compares it to the USB-IF specification.

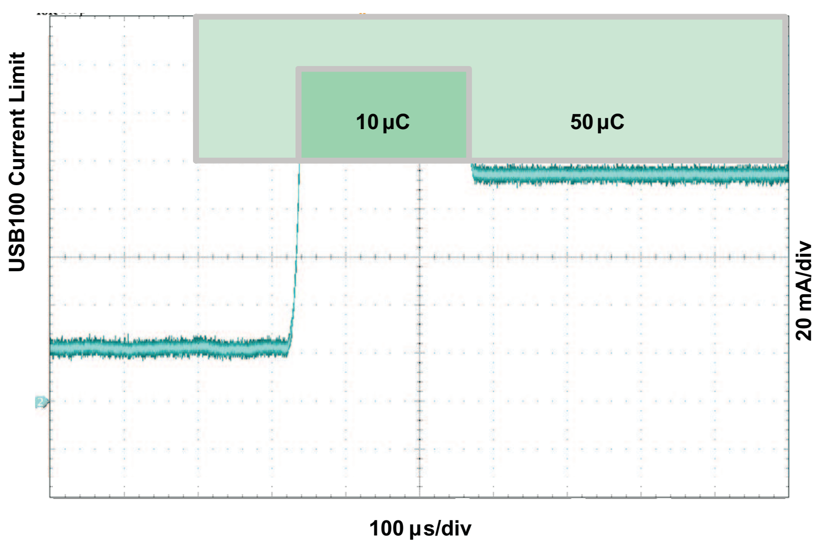


图 20. USB-IF Inrush Current Test

The input current limit selection is controlled by the state of the EN1 and EN2 pins. When using the resistor-programmable current limit, the input current limit is set by the value of the resistor connected from the ILIM pin to VSS, and is given by the equation:

$$I_{IN\text{-}MAX} = K_{ILIM}/R_{ILIM} \quad (1)$$

The input current limit is adjustable up to 1.5 A. The valid resistor range is 1.1 kΩ to 8 kΩ.

When the IN source is connected, priority is given to the system load. The DPPM and Battery Supplement modes are used to maintain the system load. These modes are explained in detail in the following sections.

Feature Description (接下页)

9.3.4.1.1 Input DPM Mode (V_{IN}-DPM)

The bq24079QW-Q1 uses the V_{IN}-DPM mode for operation from current-limited USB ports. When EN1 and EN2 are configured for USB100 (EN2 = 0, EN1 = 0) or USB500 (EN2 = 0, EN2 = 1) modes, the input voltage is monitored. If V_{IN} falls to $V_{IN\text{-}DPM}$, the input current limit is reduced to prevent the input voltage from falling further. This prevents the bq24079QW-Q1 from crashing poorly designed or incorrectly configured USB sources. 图 21 shows the V_{IN}-DPM behavior to a current limited source. In this figure, the input source has a 400-mA current limit and the device is in USB500 mode (EN1 = 1, EN2 = 0).

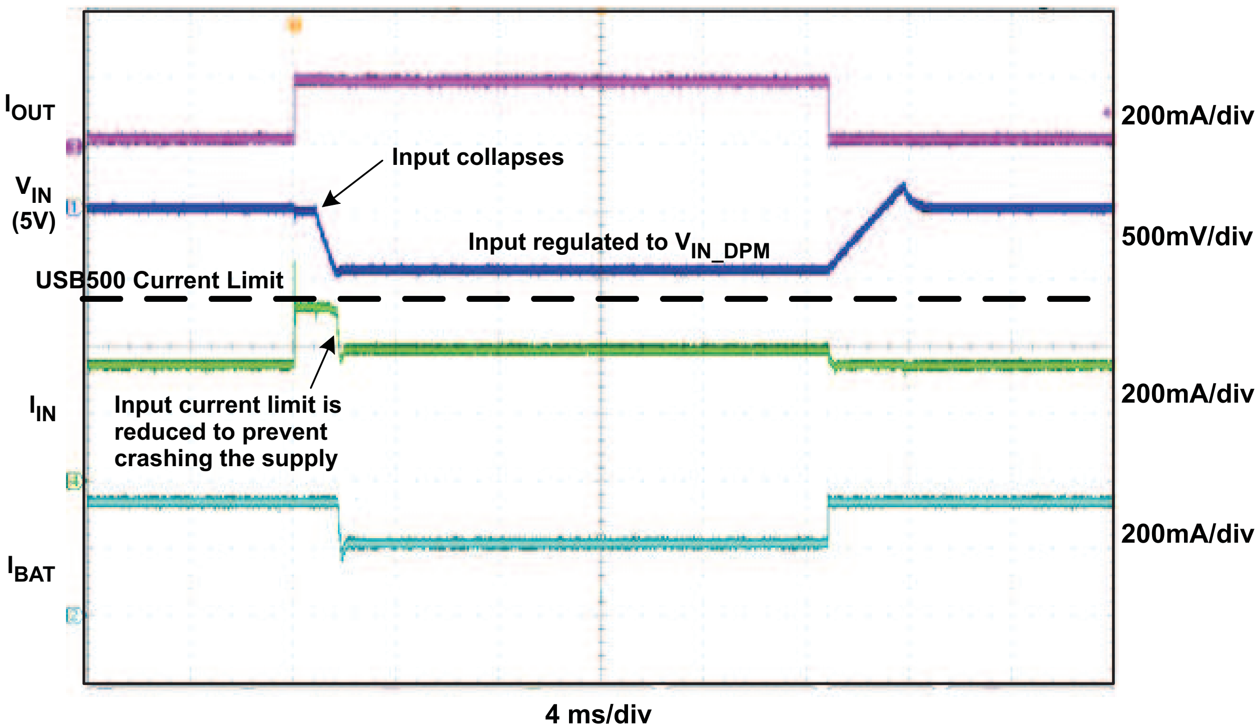


图 21. V_{IN}-DPM Waveform

9.3.4.1.2 DPPM Mode

When the sum of the charging and system load currents exceeds the maximum input current (programmed with EN1, EN2, and ILIM pins), the voltage at OUT decreases. Once the voltage on the OUT pin falls to V_{DPPM}, the bq24079QW-Q1 enters DPPM mode. In this mode, the charging current is reduced as the OUT current increases in order to maintain the system output. Battery termination is disabled while in DPPM mode.

9.3.4.1.3 Battery Supplement Mode

While in DPPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at OUT reduces further. When the OUT voltage drops below the V_{BSUP1} threshold, the battery supplements the system load. The battery stops supplementing the system load when the voltage at OUT rises above the V_{BSUP2} threshold.

During supplement mode, the battery supplement current is not regulated (BAT-FET is fully on). However, there is a short circuit protection circuit built in. If the voltage at OUT drops $V_{O(SC2)}$ below the BAT voltage during battery supplement mode, the OUT output is turned off if the overload exists after $t_{DGL(SC2)}$. The short circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. Battery termination is disabled while in supplement mode.

Feature Description (接下页)

9.3.4.2 Input Source Not Connected

When no source is connected to the IN input, OUT is powered strictly from the battery. During this mode, the current into OUT is not regulated, similar to *Battery Supplement Mode*. However, the short circuit circuitry is active. If the OUT voltage falls below the BAT voltage by 250 mV for longer than $t_{DGL(SC2)}$, OUT is turned off. The short circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. This ON/OFF cycle continues until the overload condition is removed.

9.3.5 Battery Charging

Set $\overline{CE}$ low to initiate battery charging. First, the device checks for a short-circuit on the BAT pin by sourcing $I_{BAT(SC)}$ to the battery and monitoring the voltage. When the BAT voltage exceeds $V_{BAT(SC)}$, the battery charging continues. The battery is charged in three phases: conditioning pre-charge, constant current fast charge (current regulation) and a constant voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

图 22 illustrates a normal Li-Ion charge cycle using the bq24079QW-Q1:

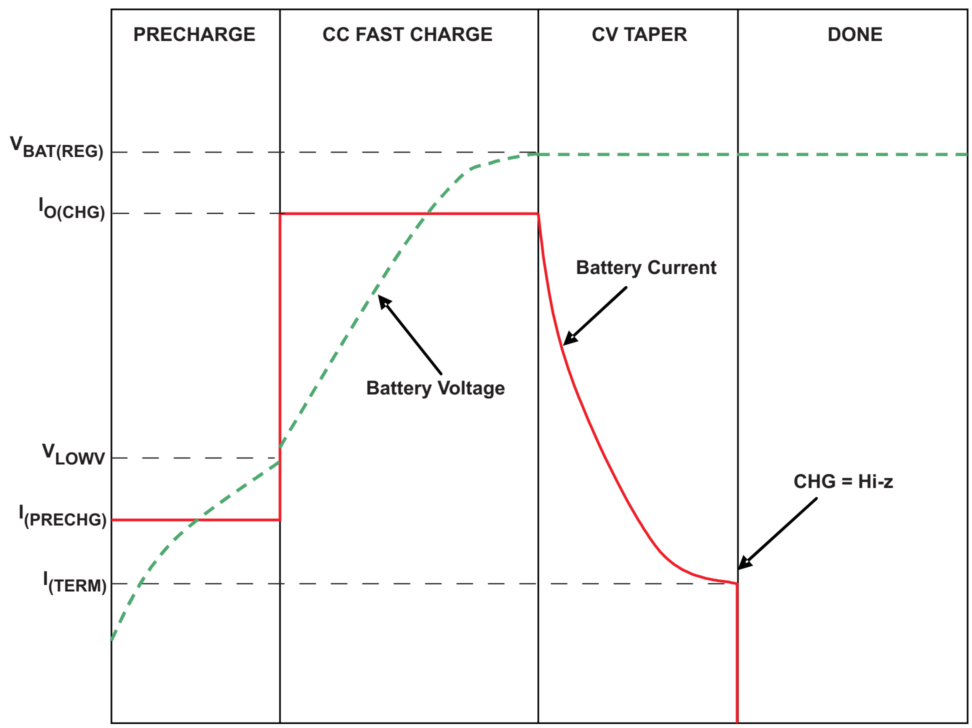


图 22. Typical Charge Cycle

In the pre-charge phase, the battery is charged with the pre-charge current (I_{PRECHG}). Once the battery voltage crosses the V_{LOWV} threshold, the battery is charged with the fast-charge current (I_{CHG}). As the battery voltage reaches $V_{BAT(REG)}$, the battery is held at a constant voltage of $V_{BAT(REG)}$ and the charge current tapers off as the battery approaches full charge. When the battery current reaches I_{TERM}, the $\overline{CHG}$ pin indicates *charging done* by going high-impedance.

Note that termination detection is disabled whenever the charge rate is reduced because of the actions of the thermal loop, the DPPM loop or the $V_{IN(LOW)}$ loop.

The value of the fast-charge current is set by the resistor connected from the ISET pin to VSS, and is given by the equation:

$$I_{CHG} = K_{ISET}/R_{ISET} \quad (2)$$

Feature Description (接下页)

The charge current limit is adjustable up to 1.5 A. The recommended valid resistor range is 590 Ω to 8.9 kΩ. Note that if I_{CHG} is programmed as greater than the input current limit, the battery will not charge at the rate of I_{CHG}, but at the slower rate of $I_{IN(MAX)}$ (minus the load current on the OUT pin, if any). In this case, the charger timers will be proportionately slowed down.

9.3.5.1 Charge Current Translator

When the charger is enabled, internal circuits generate a current proportional to the charge current at the ISET input. The current out of ISET is 1/400 (±10%) of the charge current. This current, when applied to the external charge current programming resistor, R_{ISET}, generates an analog voltage that can be monitored by an external host to calculate the current sourced from BAT.

$$V_{ISET} = I_{CHARGE} / 400 \times R_{ISET} \quad (3)$$

Feature Description (接下页)

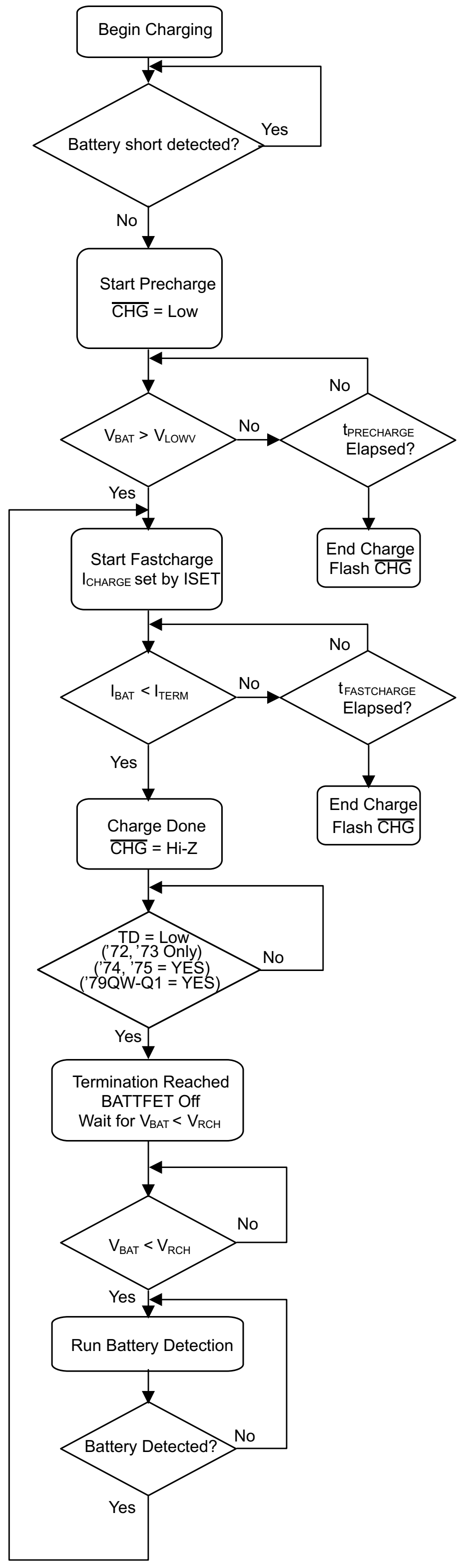


图 23. Battery Charging Flow Diagram

Feature Description (接下页)

9.3.5.2 Battery Detection And Recharge

The bq24079QW-Q1 automatically detects if a battery is connected or removed. Once a charge cycle is complete, the battery voltage is monitored. When the battery voltage falls below V_{RCH}, the battery detection routine is run. During battery detection, current ($I_{BAT(DET)}$) is pulled from the battery for a duration t_{DET} to see if the voltage on BAT falls below V_{LOWV}. If not, charging begins. If it does, then it indicates that the battery is missing or the protector is open. Next, the precharge current is applied for t_{DET} to close the protector if possible. If $V_{BAT} < V_{RCH}$, then the protector closed and charging is initiated. If $V_{BAT} > V_{RCH}$, then the battery is determined to be missing and the detection routine continues.

9.3.5.3 Battery Disconnect (SYSOFF Input)

The bq24079QW-Q1 features a SYSOFF input that allows the user to turn the FET Q2 off and disconnect the battery from the OUT pin. This is useful for disconnecting the system load from the battery, factory programming where the battery is not installed or for host side impedance track fuel gauging, such as bq27500, where the battery open circuit voltage level must be detected before the battery charges or discharges. The $\overline{CHG}$ output remains low when SYSOFF is high. Connect SYSOFF to VSS, to turn Q2 on for normal operation. SYSOFF is internally pulled to VBAT through ~5 MΩ resistor.

9.3.5.4 Dynamic Charge Timers (TMR Input)

The bq24079QW-Q1 device contains internal safety timers for the pre-charge and fast-charge phases to prevent potential damage to the battery and the system. The timers begin at the start of the respective charge cycles. The timer values are programmed by connecting a resistor from TMR to VSS. The resistor value is calculated using the following equation:

$$t_{PRECHG} = K_{TMR} \times R_{TMR} \quad (4)$$

$$t_{MAXCHG} = 10 \times K_{TMR} \times R_{TMR} \quad (5)$$

Leave TMR unconnected to select the internal default timers. Disable the timers by connecting TMR to VSS.

Note that timers are suspended when the device is in thermal shutdown, and the timers are slowed proportionally to the charge current when the device enters thermal regulation.

During the fast charge phase, several events increase the timer durations.

A. The system load current activates the DPPM loop which reduces the available charging current
B. The input current is reduced because the input voltage has fallen to $V_{IN(LOW)}$
C. The device has entered thermal regulation because the IC junction temperature has exceeded $T_{J(REG)}$

During each of these events, the internal timers are slowed down proportionately to the reduction in charging current. For example, if the charging current is reduced by half, the timer clock is reduced to half the frequency, and the counter counts half as fast.

If the pre charge timer expires before the battery voltage reaches V_{LOWV}, the bq24079QW-Q1 indicates a fault condition. Additionally, if the battery current does not fall to I_{TERM} before the fast charge timer expires, a fault is indicated. The $\overline{CHG}$ output flashes at approximately 2 Hz to indicate a fault condition. The fault condition is cleared by toggling $\overline{CE}$ or the input power, entering/ exiting USB suspend mode, or an OVP event.

9.3.5.5 Status Indicators ($\overline{PGOOD}$, $\overline{CHG}$)

The bq24079QW-Q1 contains two open-drain outputs that signal its status. The $\overline{PGOOD}$ output signals when a valid input source is connected. $\overline{PGOOD}$ is low when $(V_{BAT} + V_{IN(DT)}) < V_{IN} < V_{OVP}$. When the input voltage is outside of this range, $\overline{PGOOD}$ is high impedance.

The charge cycle after power-up, $\overline{CE}$ going low or exiting OVP is indicated with the $\overline{CHG}$ pin on (low - LED on), whereas all refresh (subsequent) charges will result in the $\overline{CHG}$ pin off (open - LED off). In addition, the $\overline{CHG}$ signals timer faults by flashing at approximately 2 Hz.

Feature Description (接下页)

表 1. $\overline{\text{PGOOD}}$ Status Indicator

INPUT STATE	$\overline{\text{PGOOD}}$ OUTPUT
$V_{IN} < V_{UVLO}$	Hi impedance
$V_{UVLO} < V_{IN} < V_{BAT} + V_{IN(DT)}$	Hi impedance
$V_{BAT} + V_{IN(DT)} < V_{IN} < V_{OVP}$	Low
$V_{IN} > V_{OVP}$	Hi impedance

表 2. $\overline{\text{CHG}}$ Status Indicator

CHARGE STATE	$\overline{\text{CHG}}$ OUTPUT
Charging	Low (for first charge cycle)
Charging suspended by thermal loop	
Safety timers expired	Flashing at 2Hz
Charging done	Hi impedance
Recharging after termination	
IC disabled or no valid input power	
Battery absent	

9.3.5.6 Thermal Regulation And Thermal Shutdown

The bq24079QW-Q1 contain a thermal regulation loop that monitors the die temperature. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high VIN and heavy OUT system load conditions. Under these conditions, if the die temperature increases to $T_{J(OFF)}$, the input FET Q1 is turned OFF. FET Q2 is turned ON to ensure that the battery still powers the load on OUT. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the input FET Q1 is turned on and the device returns to thermal regulation. Continuous overtemperature conditions result in a "hiccup" mode. During thermal regulation, the safety timers are slowed down proportionately to the reduction in current limit.

Note that this feature monitors the die temperature of the bq24079QW-Q1. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm and the LDO associated with OUT. A modified charge cycle with the thermal loop active is shown in 图 24. Battery termination is disabled during thermal regulation.

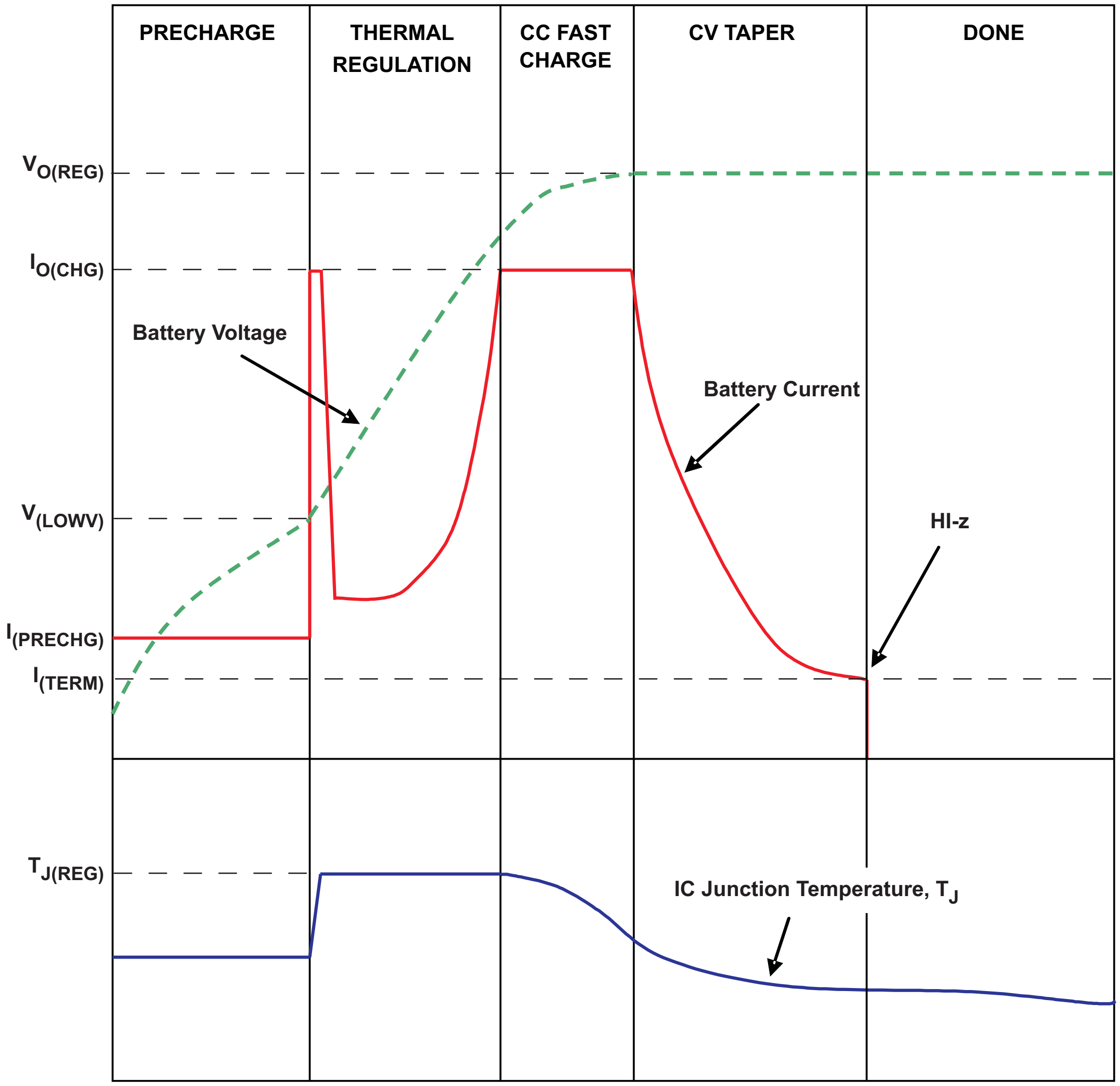


图 24. Charge Cycle Modified by Thermal Loop

9.3.6 Battery Pack Temperature Monitoring

The bq24079QW-Q1 features an external battery pack temperature monitoring input. The TS input connects to the NTC thermistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions. During charging, I_{NTC} is sourced to TS and the voltage at TS is continuously monitored. If, at any time, the voltage at TS is outside of the operating range (V_{COLD} to V_{HOT}), charging is suspended. The timers maintain their values but suspend counting. When the voltage measured at TS returns to within the operation window, charging is resumed and the timers continue counting. When charging is suspended due to a battery pack temperature fault, the $\overline{CHG}$ pin remains low and continues to indicate *charging*.

For applications that do not require the TS monitoring function, connect a 10 kΩ resistor from TS to VSS to set the TS voltage at a valid level and maintain charging.

The allowed temperature range for 103AT-2 type thermistor is 0°C to 50°C. However, the user may increase the range by adding two external resistors. See 图 25 for the circuit details. The values for Rs and Rp are calculated using the following equations:

$$Rs = \frac{-(R_{TH} + R_{TC}) \pm \sqrt{\left((R_{TH}+R_{TC})^2 - 4\left\{R_{TH} \times R_{TC} + \frac{V_H \times V_C}{(V_H - V_C) \times I_{TS}} \times (R_{TC} - R_{TH})\right\}\right)}}{2} \quad (6)$$

$$Rp = \frac{V_H \times (R_{TH} + R_S)}{I_{TS} \times (R_{TH} + R_S) - V_H} \quad (7)$$

Where:

R_{TH}: Thermistor Hot Trip Value found in thermistor data sheet
R_{TC}: Thermistor Cold Trip Value found in thermistor data sheet
V_H: IC's Hot Trip Threshold = 0.3 V nominal
V_C: IC's Cold Trip Threshold = 2.1 V nominal
I_{TS}: IC's Output Current Bias = 75 µA nominal
NTC Thermsitor Semitec 103AT-4

Rs and Rp 1% values were chosen closest to calculated values

COLD TEMP RESISTANCE AND TRIP THRESHOLD, Ω (°C)	HOT TEMP RESISTANCE AND TRIP THRESHOLD, Ω (°C)	EXTERNAL BIAS RESISTOR, Rs (Ω)	EXTERNAL BIAS RESISTOR, Rp (Ω)
28000 (–0.6)	4000 (51)	0	∞
28480 (–1)	3536 (55)	487	845000
28480 (–1)	3021 (60)	1000	549000
33890 (–5)	4026 (51)	76.8	158000
33890 (–5)	3536 (55)	576	150000
33890 (–5)	3021 (60)	1100	140000

RHOT and RCOLD are the thermistor resistance at the desired hot and cold temperatures, respectively.

注

Note that the temperature window cannot be tightened more than using only the thermistor connected to TS, it can only be extended.

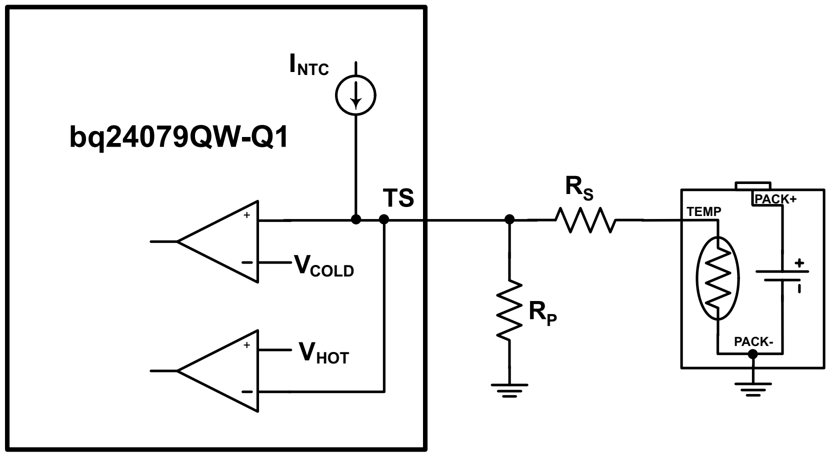


图 25. Extended TS Pin Thresholds

9.3.7 Half-Wave Adaptors

Some adapters implement a half rectifier topology, which causes the adapter output voltage to fall below the battery voltage during part of the cycle. To enable operation with adapters under those conditions, the bq24079QW-Q1 keeps the charger on for at least 20 msec (typical) after the input power puts the part in sleep mode. This feature enables use of external adapters using 50-Hz networks. The input must not drop below the UVLO voltage for the charger to work properly. Thus, the battery voltage should be above the UVLO to help prevent the input from dropping out. Additional input capacitance may be needed.

9.4 Device Functional Modes

9.4.1 Sleep Mode

When the input is between UVLO and $V_{IN(DT)}$, the device enters sleep mode. After entering sleep mode for >20 ms, the internal FET connection between the IN and OUT pin is disabled, and pulling the input to ground will not discharge the battery other than the leakage on the BAT pin. If one has a full 1000-mAHr battery and the leakage is 10 µA, then it would take 1000 mAHr/10 µA = 100000 hours (11.4 years) to discharge the battery. The battery's self discharge is typically 5 times higher than this.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The bq24079QW-Q1 devices power the system while simultaneously and independently charging the battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port. The devices feature dynamic power-path management (DPPM), which shares the source current between the system and battery charging and automatically reduces the charging current if the system load increases. When charging from a USB port, the input dynamic power management (VIN-DPM) circuit reduces the input current limit if the input voltage falls below a threshold, preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. The bq24079QW-Q1 is configurable to be host controlled for selecting different input current limits based on the input source connected, or a fully stand alone device for applications that do not support multiple types of input sources.

10.2 Typical Application – bq24079QW-Q1 Charger Design Example

See 图 26 for Schematics of the Design Example.

V_{IN} = UVLO to V_{OVP}, $I_{FASTCHG}$ = 800 mA, $I_{IN(MAX)}$ = 1.3 A, Battery Temperature Charge Range = 0°C to 50°C, 6.25 hour Fastcharge Safety Timer

V_{IN} = UVLO to V_{OVP}, $I_{FASTCHG}$ = 800 mA, $I_{IN(MAX)}$ = 1.3 A, I_{TERM} = 110 mA, Battery Temperature Charge Range = 0°C to 50°C, Safety Timers disabled

V_{IN} = UVLO to V_{OVP}, $I_{FASTCHG}$ = 800 mA, $I_{IN(MAX)}$ = 1.3 A, Battery Temperature Charge Range = 0°C to 50°C, 6.25 hour Fastcharge Safety Timer

Typical Application – bq24079QW-Q1 Charger Design Example (接下页)

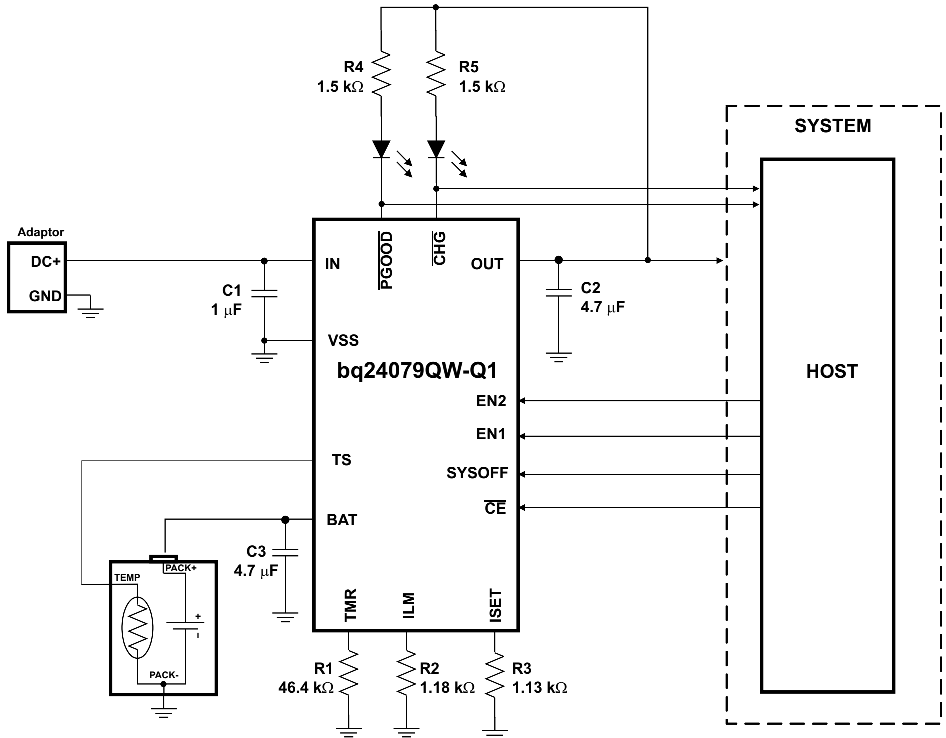


图 26. Using bq24079QW-Q1 to Disconnect the Battery from the System

Typical Application – bq24079QW-Q1 Charger Design Example (接下页)

10.2.1 Design Requirements

- Supply voltage = 5 V
- Fast charge current of approximately 800 mA; ISET - pin 16
- Input Current Limit =1.3 A; ILIM - pin 12
- Termination Current Threshold = 110 mA
- Safety timer duration, Fast-Charge = 6.25 hours; TMR – pin 14
- TS – Battery Temperature Sense = 10-kΩ NTC (103AT-2)

10.2.2 Detailed Design Procedure

10.2.2.1 Calculations

10.2.2.1.1 Program the Fast Charge Current (ISET):

$R_{ISET} = K_{ISET} / I_{CHG}$

K_{ISET} = 890 AΩ from the electrical characteristics table.

R_{ISET} = 890 AΩ/0.8 A = 1.1125 kΩ

Select the closest standard value, which for this case is 1.13 kΩ. Connect this resistor between ISET (pin 16) and V_{SS}.

10.2.2.1.2 Program the Input Current Limit (ILIM)

$R_{ILIM} = K_{ILIM} / I_{I\_MAX}$

K_{ILIM} = 1550 AΩ from the electrical characteristics table.

R_{ISET} = 1550 AΩ / 1.3 A = 1.192 kΩ

Select the closest standard value, which for this case is 1.18 kΩ. Connect this resistor between ILIM (pin 12) and V_{SS}.

10.2.2.1.3 Program 6.25-hour Fast-Charge Safety Timer (TMR)

$R_{TMR} = t_{MAXCHG} / (10 \times K_{TMR})$

K_{TMR} = 48 s/kΩ from the electrical characteristics table.

R_{TMR} = (6.25 hr × 3600 s/hr) / (10 × 48 s/kΩ) = 46.8 kΩ

Select the closest standard value, which for this case is 46.4 kΩ. Connect this resistor between TMR (pin 2) and V_{SS}.

10.2.2.2 TS Function

Use a 10-kΩ NTC thermistor in the battery pack (103AT-2). For applications that do not require the TS monitoring function, connect a 10-kΩ resistor from TS to VSS to set the TS voltage at a valid level and maintain charging.

Typical Application – bq24079QW-Q1 Charger Design Example (接下页)

10.2.2.3 $\overline{CHG}$ and $\overline{PGOOD}$

LED Status: connect a 1.5-kΩ resistor in series with a LED between OUT and $\overline{CHG}$ to indicate charging status. Connect a 1.5-kΩ resistor in series with a LED between OUT and $\overline{PGOOD}$ to indicate when a valid input source is connected.

Processor Monitoring Status: connect a pullup resistor (on the order of 100 kΩ) between the processor's power rail and $\overline{CHG}$ and $\overline{PGOOD}$

10.2.2.4 System ON/OFF (SYSOFF)

Connect SYSOFF high to disconnect the battery from the system load. Connect SYSOFF low for normal operation

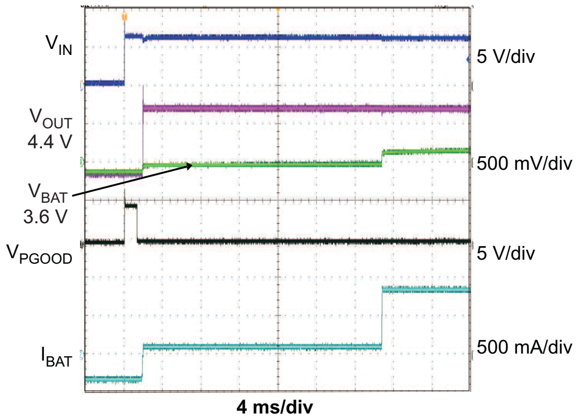
10.2.2.5 Selecting In, Out And Bat Pin Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power pin, input, output and battery pins. Using the values shown on the application diagram, is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast high amplitude pulsed load applications. Note if designed high input voltage sources (bad adaptors or wrong adaptors), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16-V capacitor may be adequate for a 30-V transient (verify tested rating with capacitor manufacturer).

Typical Application – bq24079QW-Q1 Charger Design Example (接下页)

10.2.3 Application Curves

V_{IN} = 6 V, EN1 = 1, EN2 = 0, T_A = 25°C, unless otherwise noted.



R_{LOAD} = 10 Ω

图 27. Adapter Plug-in Battery Connected

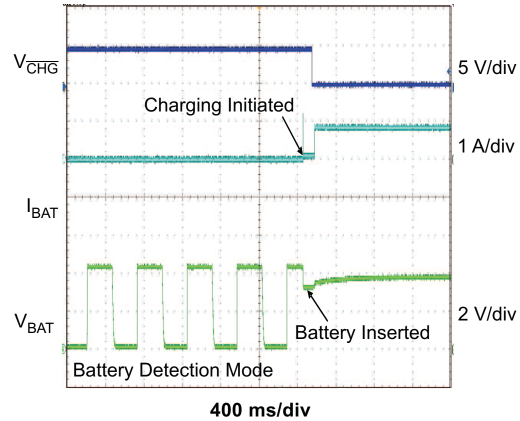


图 28. Battery Detection Battery Inserted

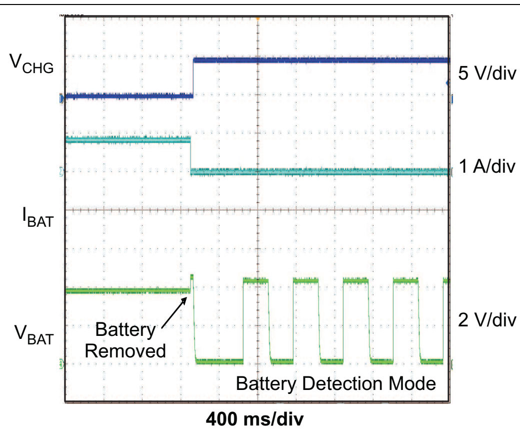
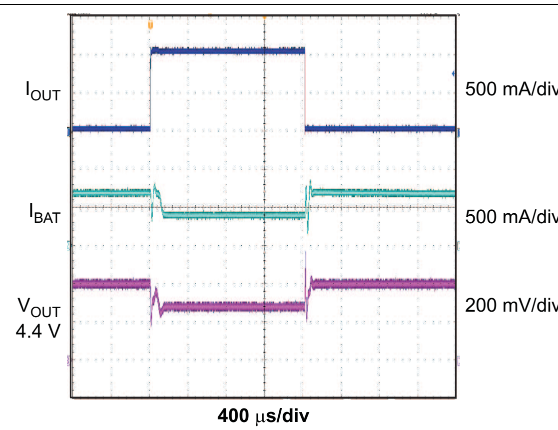


图 29. Battery Detection Battery Removed



R_{LOAD} = 20 Ω to 9 Ω

图 30. Entering And Exiting DPPM Mode

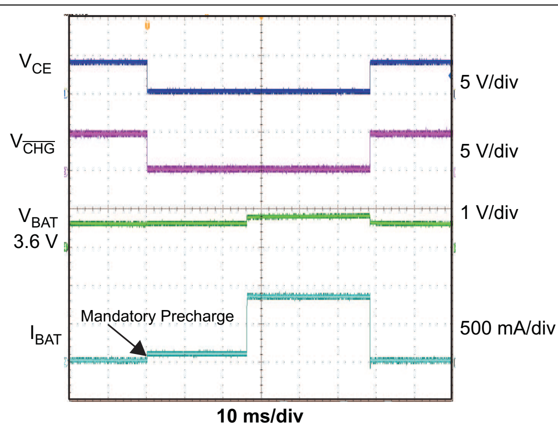
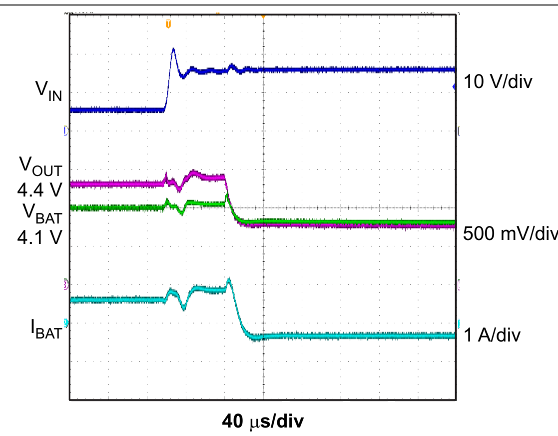


图 31. Charger ON/OF Using $\overline{CE}$

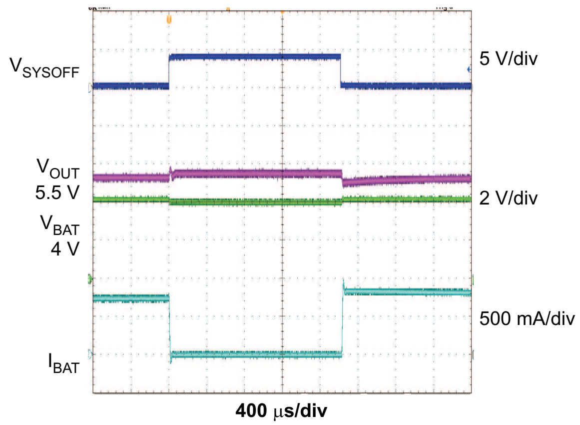


V_{IN} = 6 V to 15 V R_{LOAD} = 10 Ω

图 32. OVP Fault

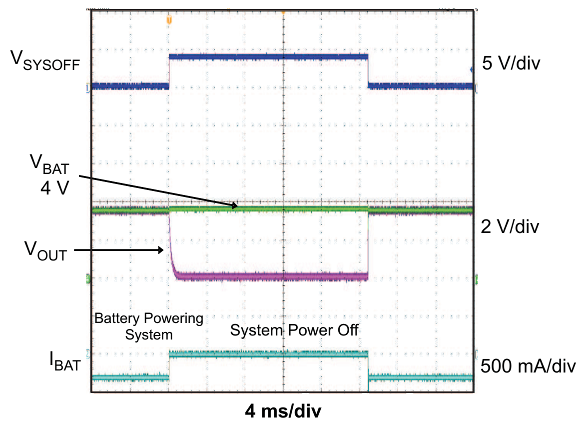
Typical Application – bq24079QW-Q1 Charger Design Example (接下页)

V_{IN} = 6 V, EN1 = 1, EN2 = 0, T_A = 25°C, unless otherwise noted.



V_{IN} = 6 V

图 33. System On/off With Input Connected - bq24079QW-Q1



V_{IN} = 0 V

图 34. System On/off With Input Not Connected - bq24079QW-Q1

11 Power Supply Recommendations

Some adapters implement a half rectifier topology, which causes the adapter output voltage to fall below the battery voltage during part of the cycle. To enable operation with adapters under those conditions, the bq24079QW-Q1 keeps the charger on for at least 20 msec (typical) after the input power puts the part in sleep mode. This feature enables use of external adapters using 50-Hz networks. The input must not drop below the UVLO voltage for the charger to work properly. Thus, the battery voltage should be above the UVLO to help prevent the input from dropping out. Additional input capacitance may be needed.

12 Layout

12.1 Layout Guidelines

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq24079QW-Q1, with short trace runs to both IN, OUT and GND (thermal pad).
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces
- The bq24079QW-Q1 is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application note entitled: QFN/SON PCB Attachment Application Note (SLUA271).

12.2 Layout Example

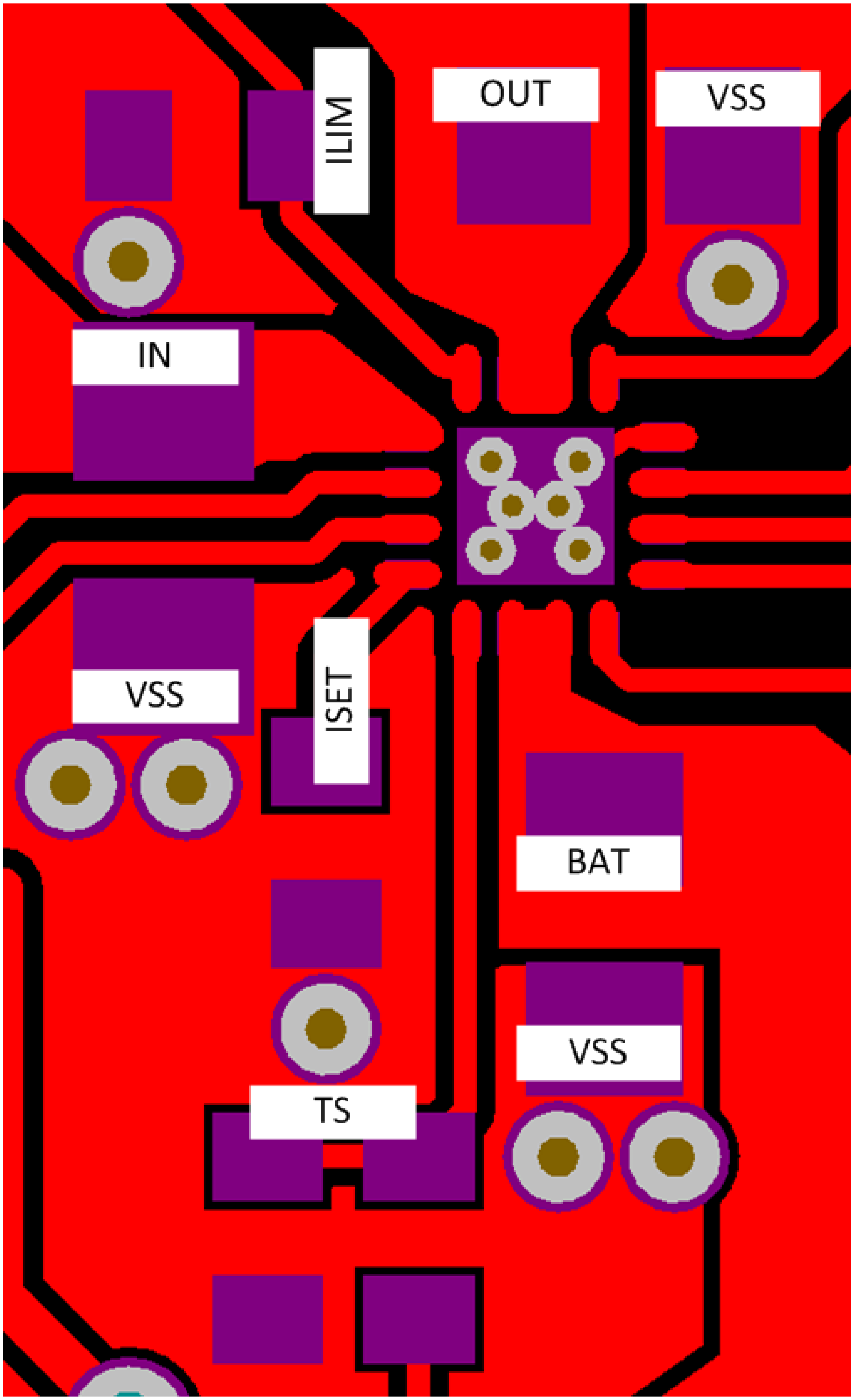


图 35.

12.3 Thermal Package

The bq24079QW-Q1 is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). The power pad should be directly connected to the V_{SS} pin. Full PCB design guidelines for this package are provided in the application note entitled: QFN/SON PCB Attachment Application Note (SLUA271). The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$\theta_{JA} = (T_J - T) / P$

Where:

T_J = chip junction temperature

T = ambient temperature

P = device power dissipation

Factors that can influence the measurement and calculation of θ_{JA} include:

1. Whether or not the device is board mounted
2. Trace size, composition, thickness, and geometry
3. Orientation of the device (horizontal or vertical)
4. Volume of the ambient air surrounding the device under test and airflow
5. Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-Ion batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to ≊3.4 V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4 V is a good minimum voltage to use. This is verified, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad should have multiple vias), the charge current and the battery voltage as a function of time. The fast charge current will start to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged :

$$P = [V_{(IN)} – V_{(OUT)}] \times I_{(OUT)} + [V_{(OUT)} – V_{(BAT)}] \times I_{(BAT)} \quad (7)$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for non typical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

13 器件和文档支持

13.1 器件支持

13.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

13.2 文档支持

13.2.1 相关文档

请参阅如下相关文档：

- 《QFN/SON PCB 连接应用手册》(SLUA271)

13.3 接收文档更新通知

要接收文档更新通知，请转至 TI.com.cn 上您的器件的产品文件夹。请在右上角单击*通知我* 按钮进行注册，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查看任意已修订文档的修订历史记录。

13.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区*。**此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

13.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24079QWRGTRQ1	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1COC	Samples
BQ24079QWRGTTQ1	ACTIVE	VQFN	RGT	16	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1COC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

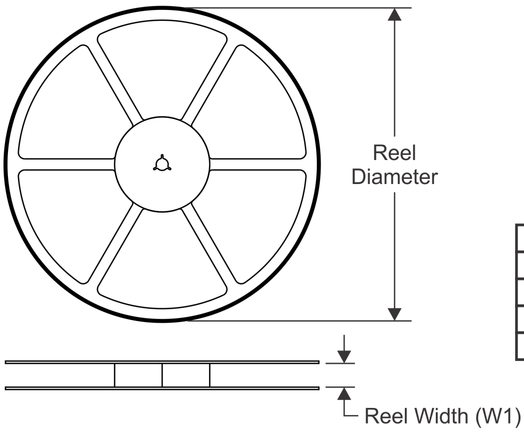
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

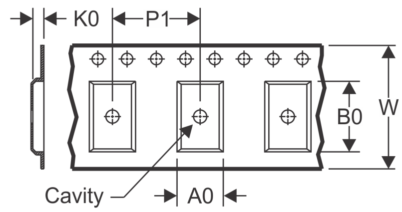
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

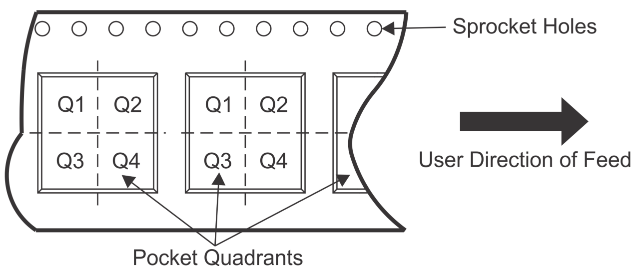


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

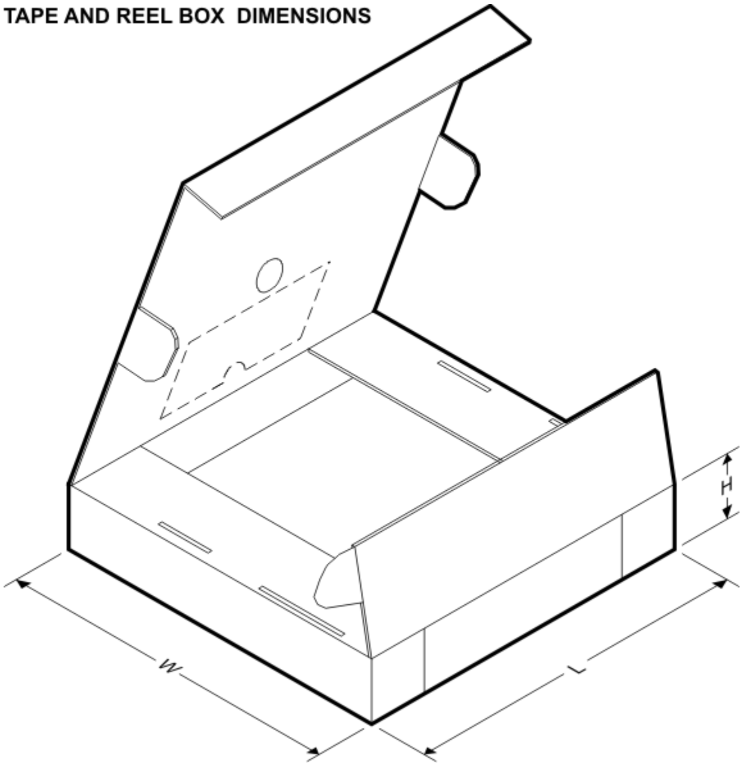
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

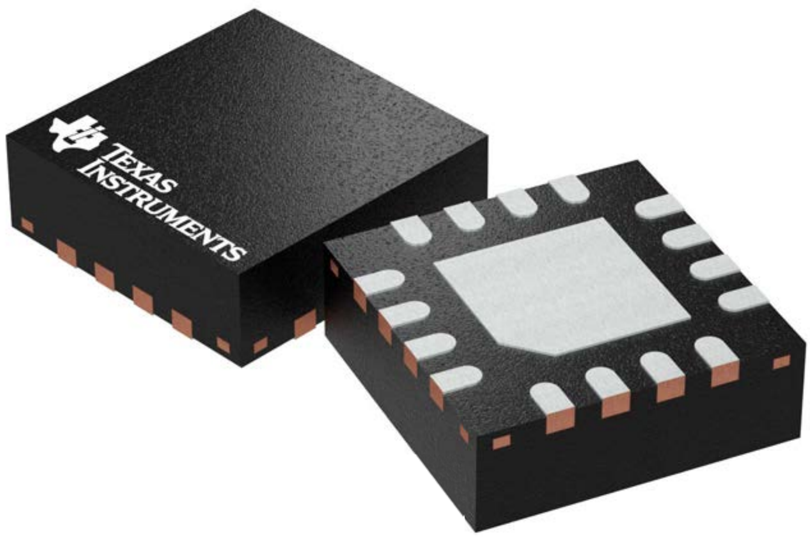
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24079QWRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
BQ24079QWRGTTQ1	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

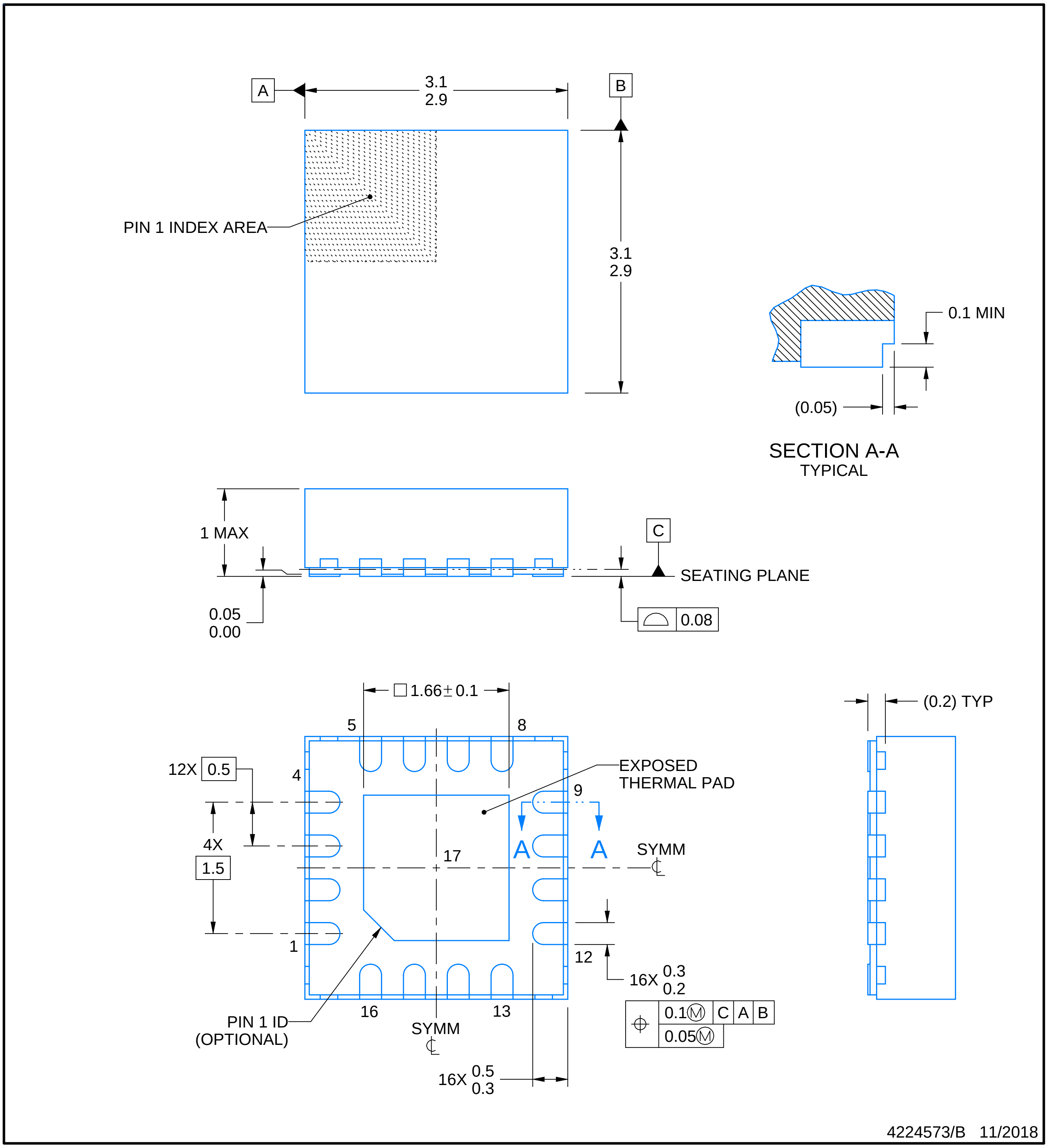


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24079QWRGTRQ1	VQFN	RGT	16	3000	367.0	367.0	38.0
BQ24079QWRGTTQ1	VQFN	RGT	16	250	213.0	191.0	35.0

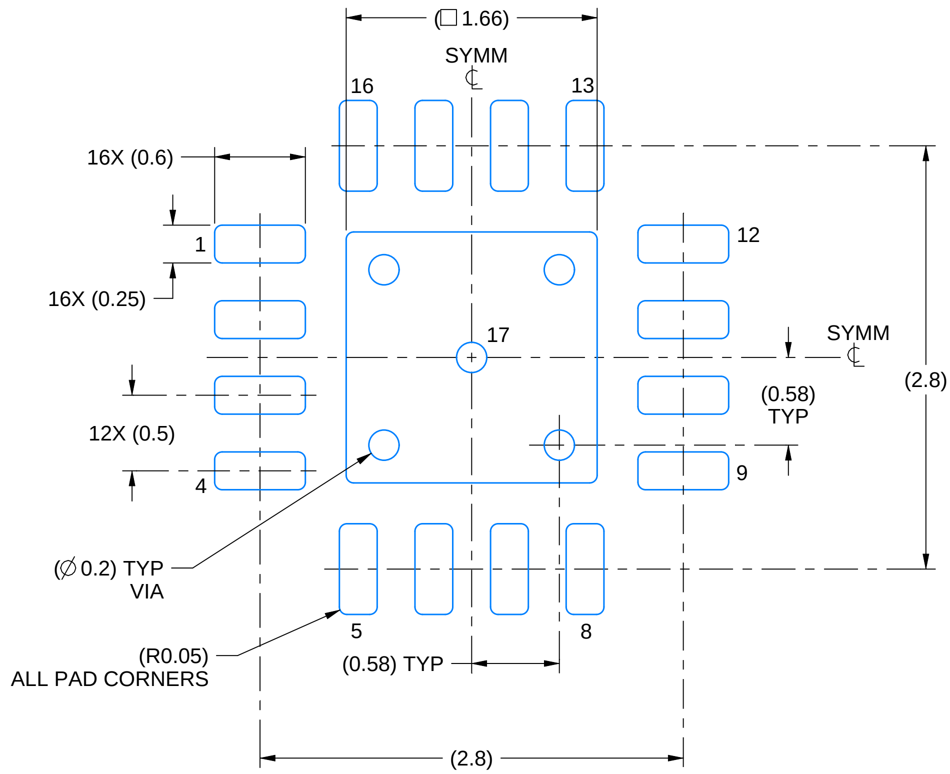


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

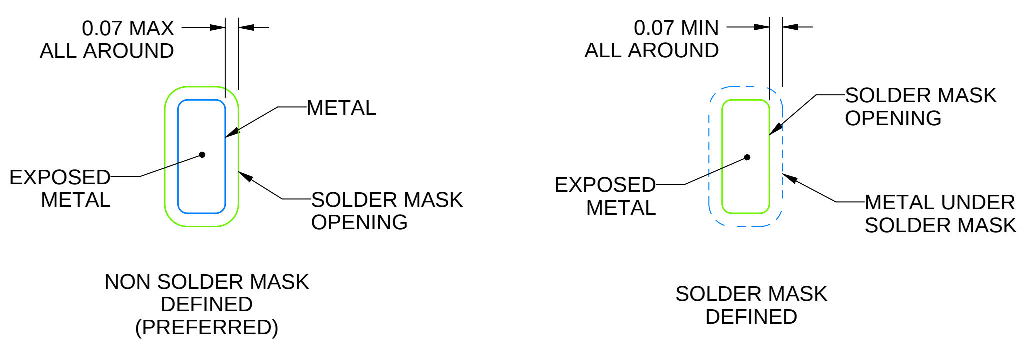


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

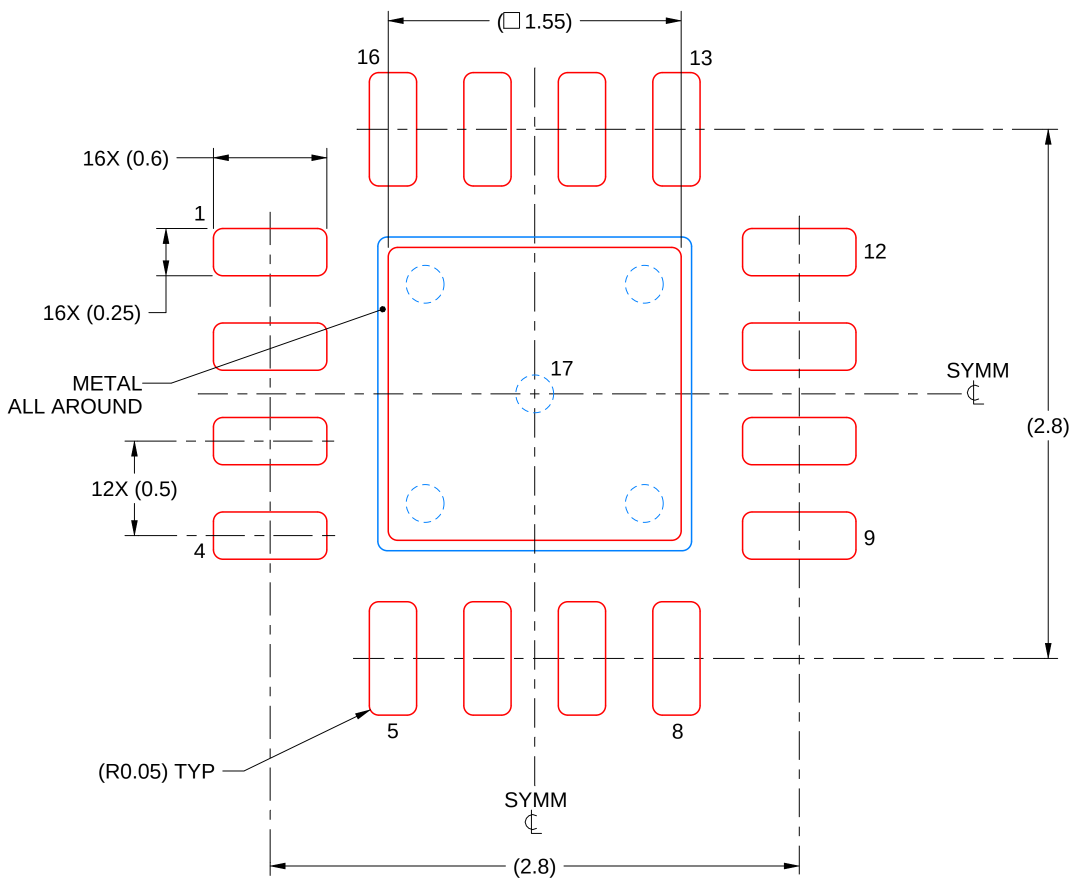


SOLDER MASK DETAILS

4224573/B 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

THERMAL PAD 17:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224573/B 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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