

## bq2408x-Q1 1A 单芯片锂离子和锂聚合物汽车充电器

### 1 特性

- 集成功率 FET 和电流传感器，适用于高达 1A 的充电应用 由交流适配器供电
- 采用安全定时器实现预充电调节
- 充电和电源正常状态输出
- 自动休眠模式，可降低功耗
- 集成了充电电流监视器
- 固定 7 小时快速充电安全定时器
- 非常适合空间受限型便携式应用中的单节锂离子电 池或锂聚合物电池组的低压降充电器设计
- 3mm x 3mm 小外形尺寸无引线 (SON) 封装

### 2 应用

- 汽车用线性充电器
- 紧急呼叫/备用呼叫电池
- 车用信息娱乐系统
- 汽车遥控钥匙

### 3 说明

bq24080-Q1 和 bq24081-Q1 是针对空间受限型充电器应用的高度集成且灵活的锂离子线性充电器件。它们在单片器件中集成了功率 FET 和电流传感器、高精度电流和电压调节、充电状态以及充电终止功能。可通过一个外部电阻设置充电电流幅值。

器件分三个阶段对电池进行充电：调节、恒流和恒压。当达到最低电流时将终止充电。内置的充电定时器针对充电终止提供了备用的安全性机制。如果电池电压低于内部阈值，器件将自动重新启动充电。移除交流适配器后，器件将自动进入休眠模式。

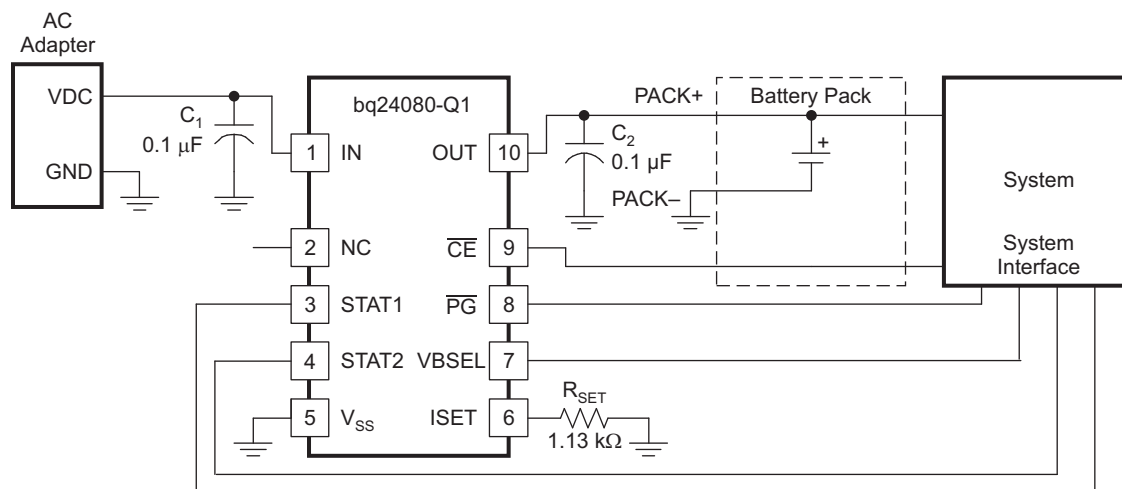
器件信息(1)

器件型号	封装	封装尺寸 (标称值)
bq24080-Q1 <sup>(2)</sup>	VSON (10)	3.00mm x 3.00mm
bq24081-Q1		

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

(2) 产品预览

简化原理图



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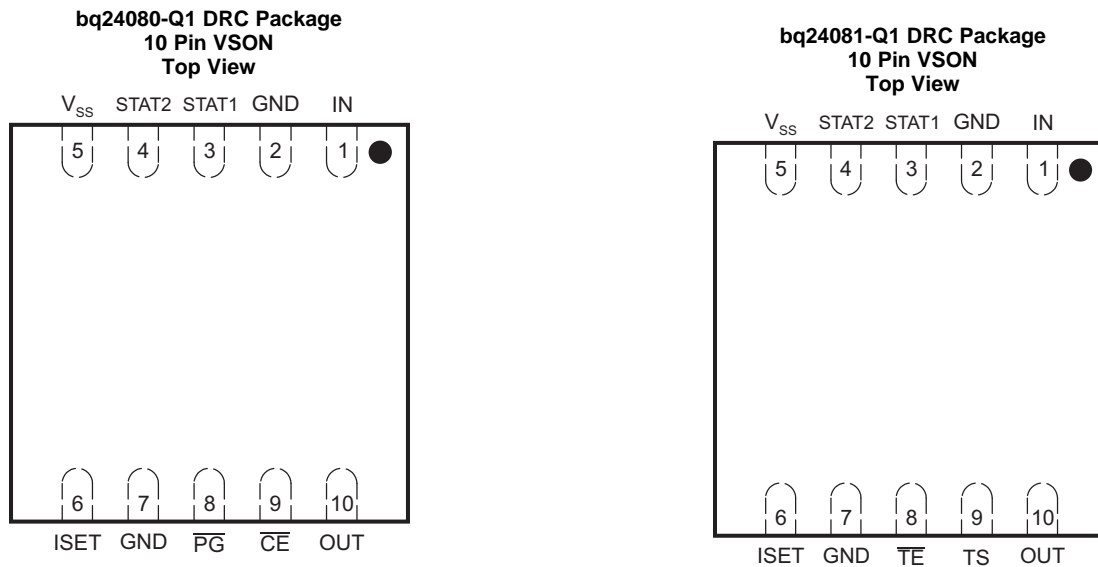
## 4 修订历史记录

<b>Changes from Revision A (August 2016) to Revision B</b>	<b>Page</b>
• Changed the $R_{\theta JC(top)}$ value From: 5034 °C/W To: 50.4 °C/W in the <i>Thermal Information</i> table .....	4

<b>Changes from Original (May 2016) to Revision A</b>	<b>Page</b>
• <a href="#">Recommended Operating Conditions</a> , Changed The $T_J$ MIN value From: 0 To: -40°C.....	4
• <a href="#">Electrical Characteristics</a> , Changed the conditions statement From: $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ To: $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ .....	5

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	bq24080-Q1	bq24081-Q1		
CE	9	–	I	Charge enable input (active-low)
GND	2, 7	2, 7	–	Ground
IN	1	1	I	Adapter dc voltage. Connect minimum 0.1- $\mu$ F capacitor to V <sub>SS</sub> .
ISET	6	6	I	Charge current. External resistor to V <sub>SS</sub> sets precharge and fast-charge current, and also the termination current value. Can be used to monitor the charge current.
OUT	10	10	O	Charge current output. Connect minimum 0.1- $\mu$ F capacitor to V <sub>SS</sub> .
PG	8	–	O	Power-good status output (open-drain)
STAT1	3	3	O	Charge status outputs (open-drain)
STAT2	4	4	O	
TE	–	8	I	Timer-enable input (active-low)
TS	–	9	I/O	Temperature sense; connect to NTC in battery pack.
V <sub>SS</sub>	5	5	–	Ground
Thermal pad	–	–	–	There is an internal electrical connection between the exposed thermal pad and the V <sub>SS</sub> pin of the device. The exposed thermal pad must be connected to the same potential as the V <sub>SS</sub> pin on the printed-circuit board. <b>Do not use the thermal pad as the primary ground input for the device.</b> The V <sub>SS</sub> pin must be connected to ground at all times.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		bq24080-Q1, bq24081-Q1		UNIT
		MIN	MAX	
Input voltage <sup>(2)</sup>	IN, $\overline{CE}$ , ISET, OUT, $\overline{PG}$ , STAT1, STAT2, $\overline{TE}$ , TS	-0.3	7	V
Output sink/source current	STAT1, STAT2, $\overline{PG}$		15	mA
Output current	OUT		1.5	A
Operating free-air temperature range, T <sub>A</sub>		-40	125	°C
Junction temperature range, T <sub>J</sub>				°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to V<sub>SS</sub>.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011	±500
			V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	6.5	V
T <sub>J</sub>	Operating junction temperature range	-40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		bq24080-Q1, bq24081-Q1	UNIT
		DRC (10 PINS)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	44.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	50.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	19.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.7	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	19.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	4.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$  and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT CURRENT</b>						
$I_{CC(VCC)}$	$V_{CC}$ current	$V_{CC} > V_{CC(\text{min})}$		1.2	2	mA
$I_{CC(\text{SLP})}$	Sleep current	Sum of currents into OUT pin, $V_{CC} < V_{(\text{SLP})}$		2	5	$\mu\text{A}$
$I_{CC(\text{STBY})}$	Standby current	$\overline{\text{CE}} = \text{High}$ , $0^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$			150	
$I_{\text{IB(OUT)}}$	Input current on OUT pin	Charge DONE, $V_{CC} > V_{CC(\text{MIN})}$		1	5	
<b>VOLTAGE REGULATION</b> $V_{O(\text{REG})} + V_{(\text{DO-MAX})} \leq V_{CC}$ , $I_{(\text{TERM})} < I_{O(\text{OUT})} \leq 1 \text{ A}$						
$V_{O(\text{REG})}$	Output voltage			4.2		V
	Voltage regulation accuracy	$T_A = 25^{\circ}\text{C}$	-0.35%		0.35%	
			-1%		1%	
$V_{(\text{DO})}$	Dropout voltage ( $V_{(\text{IN})} - V_{(\text{OUT})}$ )	$V_{O(\text{OUT})} = V_{O(\text{REG})}$ , $I_{O(\text{OUT})} = 1 \text{ A}$ $V_{O(\text{REG})} + V_{(\text{DO})} \leq V_{CC}$		350	500	mV
<b>CURRENT REGULATION</b>						
$I_{O(\text{OUT})}$	Output current range <sup>(1)</sup>	$V_{\text{I(OUT)}} > V_{(\text{LOWV})}$ , $V_{\text{I(IN)}} - V_{\text{I(OUT)}} > V_{(\text{DO})}$ , $V_{CC} \geq 4.5 \text{ V}$	20		1000	mA
$V_{(\text{SET})}$	Output current set voltage	Voltage on ISET pin, $V_{CC} \geq 4.5 \text{ V}$ , $V_{\text{I}} \geq 4.5 \text{ V}$ , $V_{\text{I(OUT)}} > V_{(\text{LOWV})}$ , $V_{\text{I}} - V_{\text{I(OUT)}} > V_{(\text{DO})}$	2.463	2.5	2.538	V
$K_{(\text{SET})}$	Output current set factor	$50 \text{ mA} \leq I_{O(\text{OUT})} \leq 1 \text{ A}$	307	322	337	
		$10 \text{ mA} \leq I_{O(\text{OUT})} < 50 \text{ mA}$	296	320	346	
		$1 \text{ mA} \leq I_{O(\text{OUT})} < 10 \text{ mA}$	246	320	416	
<b>PRECHARGE AND SHORT-CIRCUIT CURRENT REGULATION</b>						
$V_{(\text{LOWV})}$	Precharge to fast-charge transition threshold	Voltage on OUT pin	2.8	3	3.2	V
$I_{O(\text{PRECHG})}$	Precharge range <sup>(2)</sup>	$0 \text{ V} < V_{\text{I(OUT)}} < V_{(\text{LOWV})}$ , $t < t_{(\text{PRECHG})}$	2		100	mA
$V_{(\text{PRECHG})}$	Precharge set voltage	Voltage on ISET pin, $V_{O(\text{REG})} = 4.2 \text{ V}$ , $0 \text{ V} < V_{\text{I(OUT)}} > V_{(\text{LOWV})}$ , $t < t_{(\text{PRECHG})}$	240	255	270	mV
<b>TERMINATION DETECTION</b>						
$I_{(\text{TERM})}$	Charge termination detection range <sup>(3)</sup>	$V_{\text{I(OUT)}} > V_{(\text{RCH})}$ , $t < t_{(\text{TRMDET})}$	2		100	mA
$V_{(\text{TERM})}$	Charge termination detection set voltage	Voltage on ISET pin, $V_{O(\text{REG})} = 4.2 \text{ V}$ , $V_{\text{I(OUT)}} > V_{(\text{RCH})}$ , $t < t_{(\text{TRMDET})}$	235	250	265	mV
<b>BATTERY RECHARGE THRESHOLD</b>						
$V_{(\text{RCH})}$	Recharge threshold		$V_{O(\text{REG})}$ -0.115	$V_{O(\text{REG})}$ -0.10	$V_{O(\text{REG})}$ -0.085	V
<b>STAT1, STAT2, and PG OUTPUTS</b>						
$V_{\text{OL}}$	Low-level output saturation voltage	$I_{\text{O}} = 5 \text{ mA}$			0.25	V
<b><math>\overline{\text{CE}}</math> and <math>\overline{\text{TE}}</math> INPUTS</b>						
$V_{\text{IL}}$	Low-level input voltage		0		0.4	V
$V_{\text{IH}}$	High-level input voltage		1.4			
$I_{\text{IL}}$	Low-level input current		-1			$\mu\text{A}$
$I_{\text{IH}}$	High-level input current				1	
<b>TIMERS</b>						
$I_{(\text{FAULT})}$	Timer fault recovery current			200		$\mu\text{A}$

(1) See Equation 2.

(2) See Equation 1.

(3) See Equation 4.

## Electrical Characteristics (continued)

 over  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$  and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SLEEP COMPARATOR</b>						
$V_{(SLP)}$	Sleep-mode entry threshold voltage	$2.3\text{ V} \leq V_{I(OUT)} \leq V_{O(REG)}$	$V_{CC} \leq V_{I(OUT)} + 80\text{ mV}$			V
$V_{(SLPEXIT)}$	Sleep-mode exit threshold voltage		$V_{CC} \geq V_{I(OUT)} + 190$			
<b>THERMAL SHUTDOWN THRESHOLDS</b>						
$T_{(SHTDWN)}$	Thermal trip threshold	$T_J$ increasing	165			$^{\circ}\text{C}$
	Thermal hysteresis		15			
<b>UNDERVOLTAGE LOCKOUT</b>						
UVLO	Undervoltage lockout	Decreasing $V_{CC}$	2.4	2.5	2.6	V
	Hysteresis		27			mV
<b>TEMPERATURE SENSE COMPARATOR (bq24081-Q1)</b>						
$V_{(TS1)}$	High-voltage threshold		2.475	2.5	2.525	V
$V_{(TS2)}$	Low-voltage threshold		0.485	0.5	0.515	
$I_{(TS)}$	TS pin current source		96	102	108	$\mu\text{A}$

## 6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
<b>PRECHARGE AND SHORT-CIRCUIT CURRENT REGULATION</b>						
	Deglitch time for fast-charge to precharge transition	$V_{CC(MIN)} \geq 4.5\text{ V}$ , $t_{FALL} = 100\text{ ns}$ , 10-mV overdrive, $V_{I(OUT)}$ decreasing below threshold	250	375	500	ms
<b>TERMINATION DETECTION</b>						
$t_{TRMDET}$	Deglitch time for termination detection	$V_{CC(MIN)} \geq 4.5\text{ V}$ , $t_{FALL} = 100\text{ ns}$ charging current decreasing below 10-mV overdrive	250	375	500	ms
<b>BATTERY RECHARGE THRESHOLD</b>						
$t_{(DEGL)}$	Deglitch time for recharge detect	$V_{CC(MIN)} \geq 4.5\text{ V}$ , $t_{FALL} = 100\text{ ns}$ decreasing below or increasing above threshold, 10-mV overdrive	250	375	500	ms
<b>TIMERS</b>						
$t_{(PRECHG)}$	Precharge time		1,584	1,800	2,016	s
$t_{(CHG)}$	Charge time		22,176	25,200	28,224	s
<b>SLEEP COMPARATOR</b>						
	Sleep-mode entry deglitch time	$V_{(IN)}$ decreasing below threshold, $t_{FALL} = 100\text{ ns}$ , 10-mV overdrive	250	375	500	ms
<b>TEMPERATURE SENSE COMPARATOR (bq24081-Q1)</b>						
$t_{(DEGL)}$	Deglitch time for temperature fault		250	375	500	ms

## 6.7 Typical Characteristics

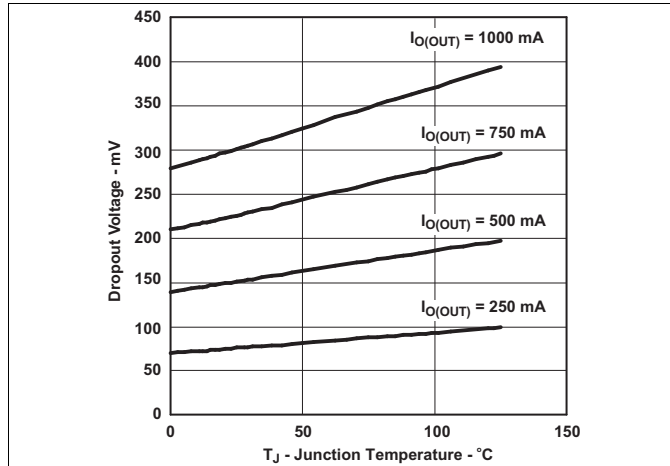


Figure 1. Dropout Voltage vs Junction Temperature

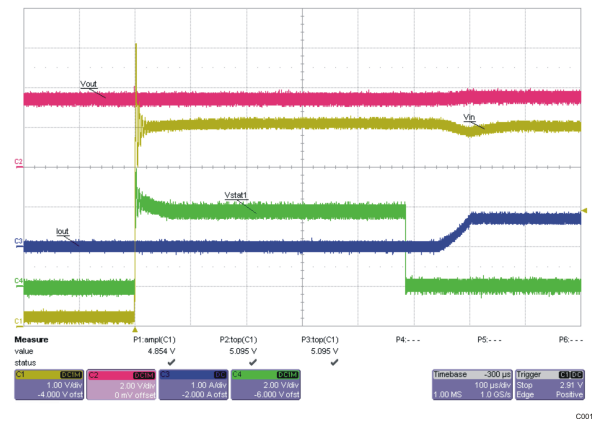


Figure 2. V<sub>IN</sub> Hot-Plug Power-Up Sequence

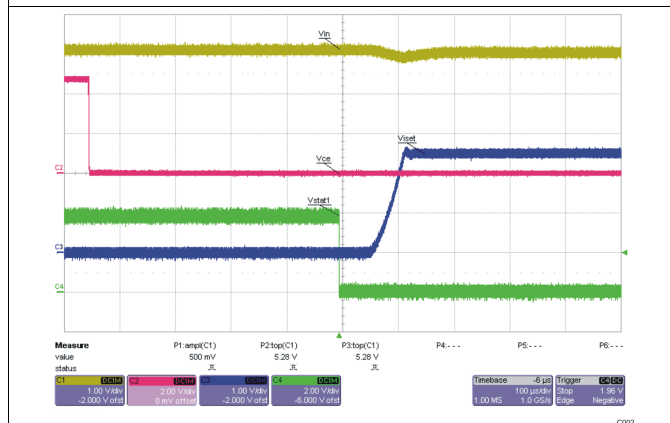


Figure 3. Charge Enable Power-Up Sequence (CE = High-to-Low)

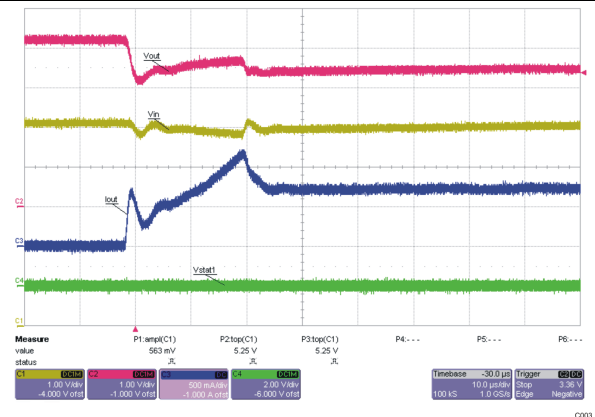
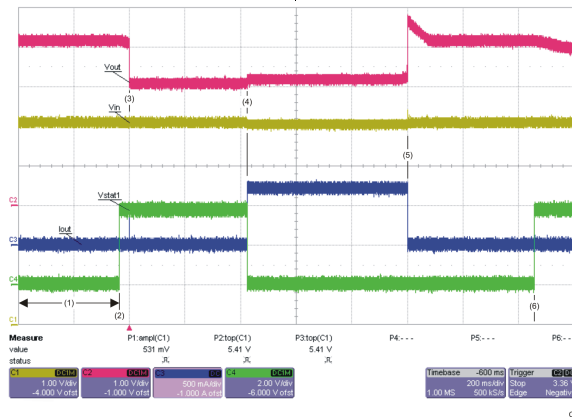


Figure 4. Battery Hot-Plug During Charging Phase



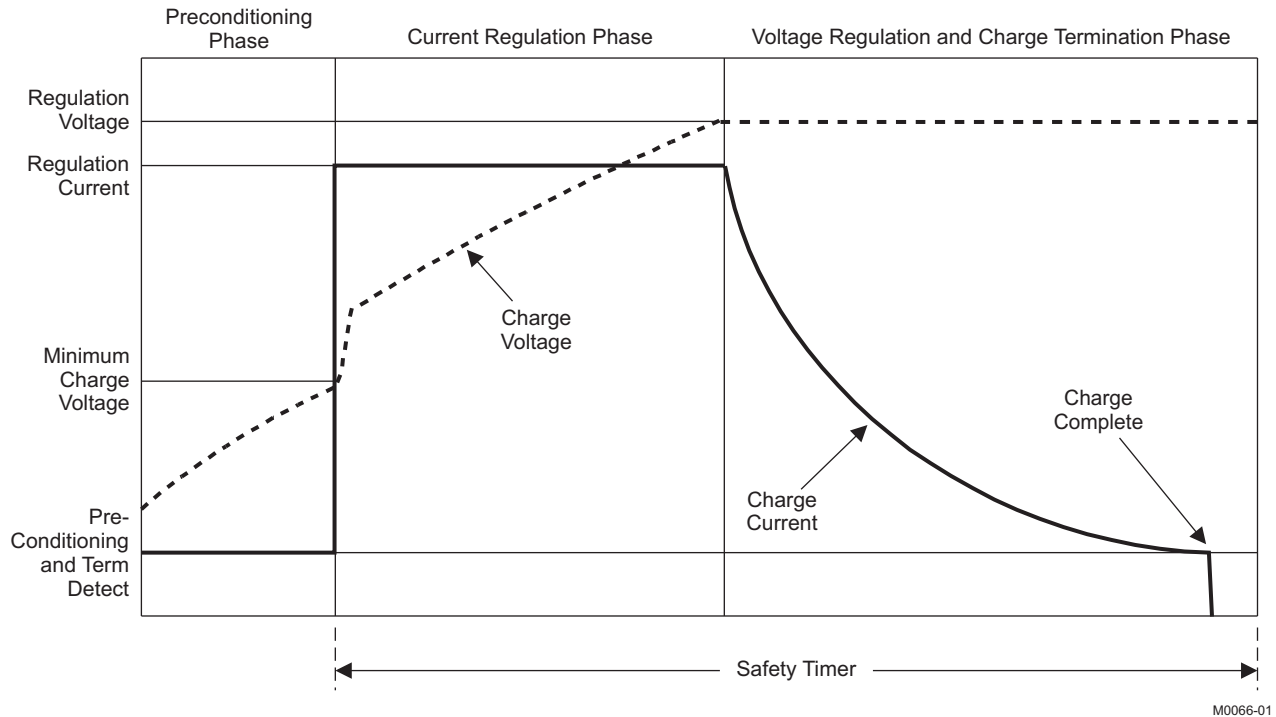
No battery – In termination deglitch prior to STAT1 going high. V<sub>OUT</sub> (V<sub>BAT</sub>) cycling between *charge* and *done* prior to screen capture  
 Stat1 goes high – In *done* state  
 2-V battery is inserted during the *charge done* state.  
 Charging is initiated – STAT1 goes low and charge current is applied.  
 Battery is removed – V<sub>OUT</sub> goes into regulation, I<sub>OUT</sub> goes to zero, and termination deglitch timer starts running (same as state 1).  
 Deglitch timer expires – *charge done* is declared.

Figure 5. Battery Hot-Plug and Removal Power Sequence

## 7 Detailed Description

### 7.1 Overview

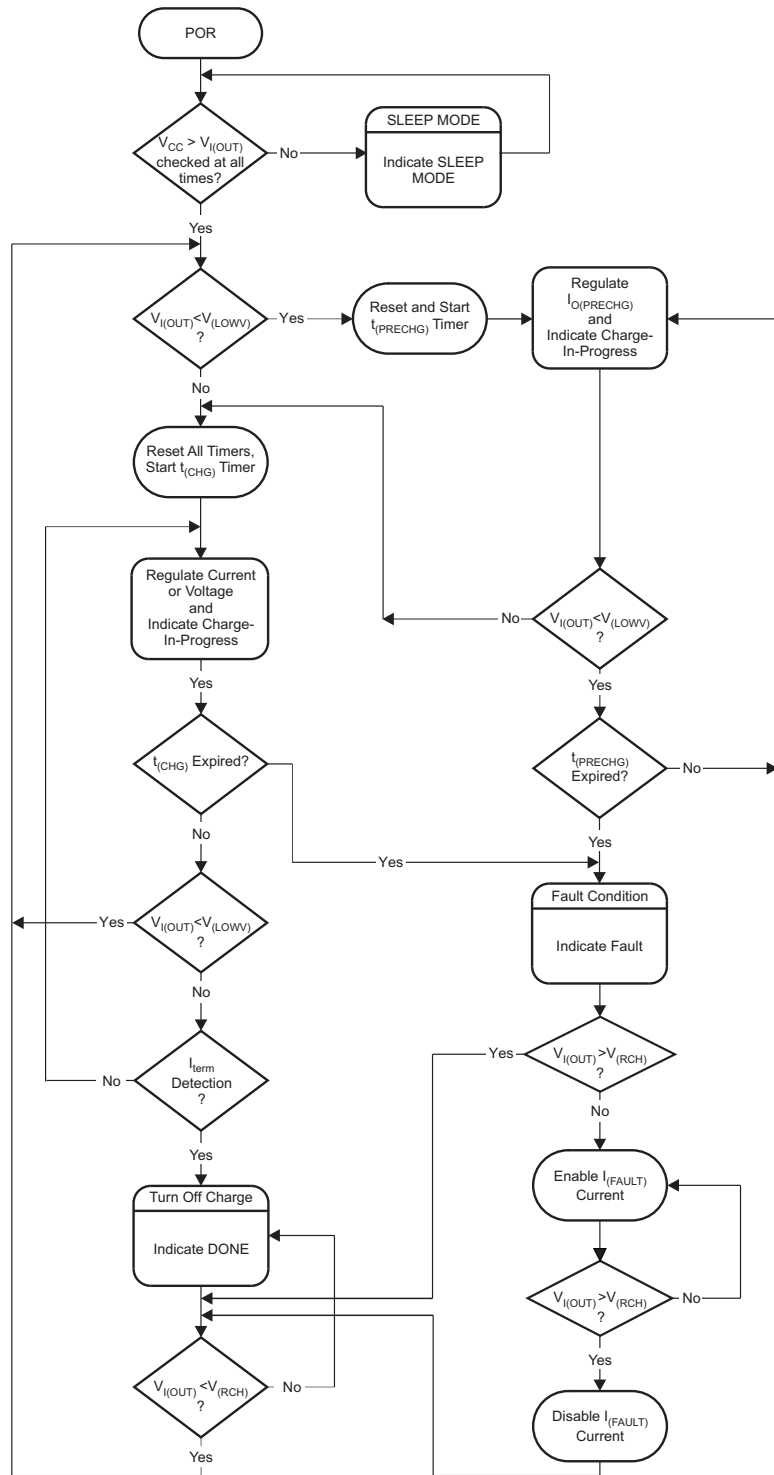
The device supports a precision Li-Ion, Li-Pol charging system suitable for single cells. [Figure 6](#) shows a typical charge profile, and [Figure 7](#) shows an operational flow chart.



**Figure 6. Typical Charging Profile**



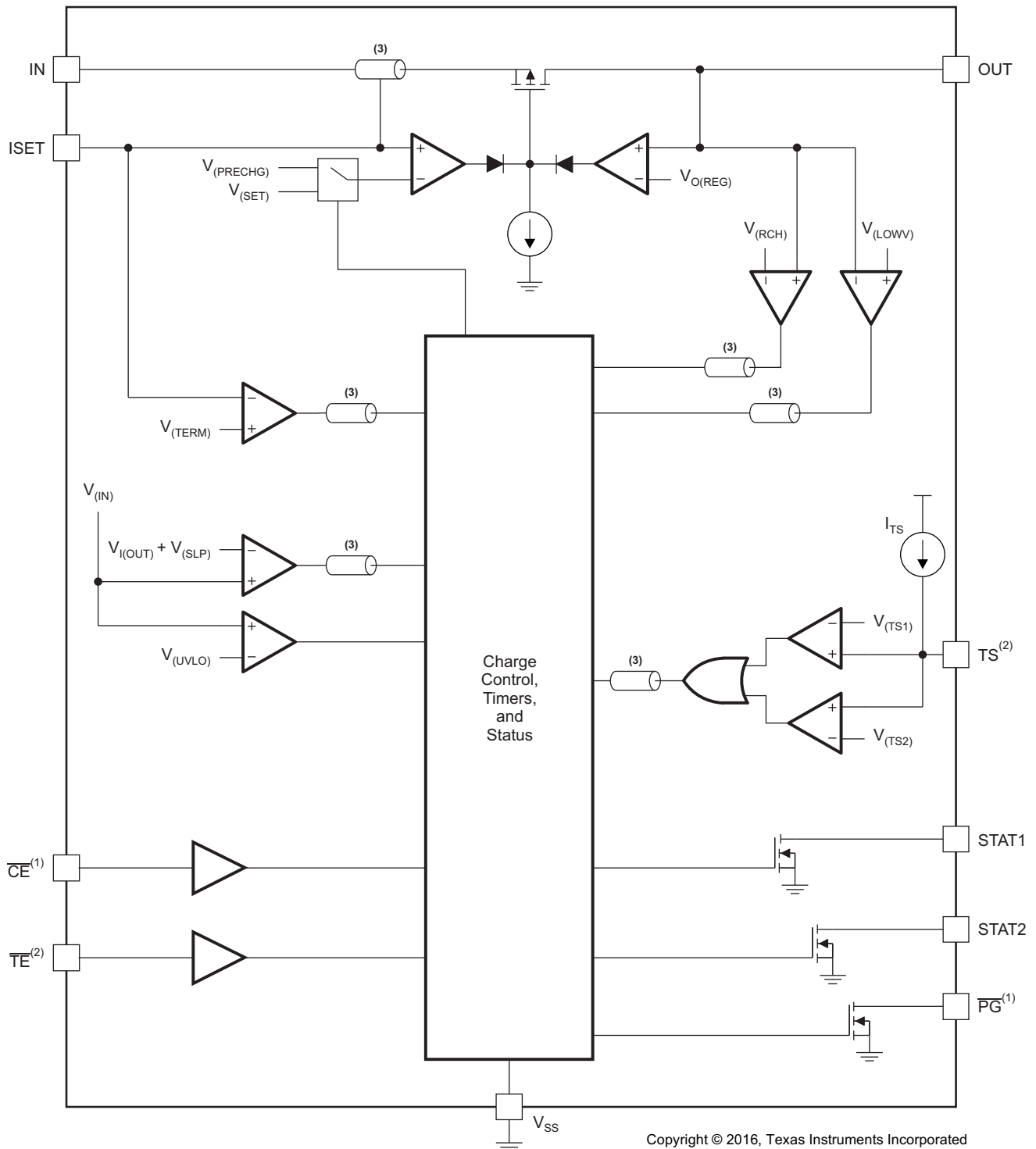
Overview (continued)



F0018-01

Figure 7. Operational Flow Chart

## 7.2 Functional Block Diagram



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- (1) bq24080-Q1 only
- (2) bq24081-Q1 only
- (3) Signal deglitched

## 7.3 Feature Description

### 7.3.1 Battery Preconditioning

During a charge cycle, if the battery voltage is below the  $V_{(LOWV)}$  threshold, the device applies a precharge current,  $I_{O(PRECHG)}$ , to the battery. This feature revives deeply discharged cells. Resistor  $R_{SET}$ , connected between the ISET and  $V_{SS}$ , determines the precharge rate. The  $V_{(PRECHG)}$  and  $K_{(SET)}$  parameters are specified in the [Electrical Characteristics](#) table.

$$I_{O(PRECHG)} = \frac{K_{(SET)} \times V_{(PRECHG)}}{R_{SET}} \quad (1)$$

The device activates a safety timer,  $t_{(PRECHG)}$ , during the conditioning phase. If the  $V_{(LOWV)}$  threshold is not reached within the timer period, the device turns off the charger and enunciates FAULT on the STATx pins. See the [Timer Fault and Recovery](#) section for additional details.

### 7.3.2 Battery Fast-Charge Constant Current

The device offers on-chip current regulation with programmable set point. Resistor  $R_{SET}$ , connected between the ISET and  $V_{SS}$ , determines the charge rate. The  $V_{(SET)}$  and  $K_{(SET)}$  parameters are specified in the specifications table.

$$I_{O(OUT)} = \frac{K_{(SET)} \times V_{(SET)}}{R_{SET}} \quad (2)$$

### 7.3.3 Charge-Current Monitor

When the charge function is enabled internal circuits generate a current proportional to the charge current at the ISET pin. This current, when applied to the external charge current programming resistor  $R_{ISET}$  generates an analog voltage that can be monitored by an external host to calculate the current sourced from the OUT pin.

$$V_{(ISET)} = I_{(OUT)} \times \frac{R_{(ISET)}}{K_{(ISET)}} \quad (3)$$

### 7.3.4 Battery Fast-Charge Voltage Regulation

The voltage regulation feedback is through the OUT pin. This input is tied directly to the positive side of the battery pack. The device monitors the battery-pack voltage between the OUT and  $V_{SS}$  pins. When the battery voltage rises to the  $V_{O(REG)}$  threshold, the voltage regulation phase begins and the charging current begins to taper down.

As a safety backup, the device also monitors the charge time in the charge mode. If charge is not terminated within this time period,  $t_{(CHG)}$ , the charger is turned off and FAULT is set on the STATx pins. See the [Timer Fault and Recovery](#) section for additional details.

### 7.3.5 Charge Termination Detection and Recharge

The device monitors the charging current during the voltage regulation phase. Once the termination threshold,  $I_{(TERM)}$ , is detected, charge is terminated. The  $V_{(TERM)}$  and  $K_{(SET)}$  parameters are specified in the [Electrical Characteristics](#) table.

$$I_{O(TERM)} = \frac{K_{(SET)} \times V_{(TERM)}}{R_{SET}} \quad (4)$$

After charge termination, the device restarts the charge once the voltage on the OUT pin falls below the  $V_{(RCH)}$  threshold. This feature keeps the battery at full capacity at all times.

The device monitors the charging current during the voltage regulation phase. Once the termination threshold,  $I_{(TERM)}$ , is detected, the charge is terminated immediately.

Resistor  $R_{SET}$ , connected between the ISET and  $V_{SS}$ , determines the current level at the termination threshold.

## Feature Description (continued)

### 7.3.6 Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in [Table 1](#). These status pins can be used to drive LEDs or communicate to the host processor. Note that *OFF* indicates the open-drain transistor is turned off.

**Table 1. Status Pin Summary**

CHANGE STATE	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Charge done	OFF	ON
Charge suspend (temperature)	OFF	OFF
Timer fault		
Sleep mode		

### 7.3.7 $\overline{\text{PG}}$ Output (bq24080-Q1)

The open-drain power-good ( $\overline{\text{PG}}$ ) output pulls low when a valid input voltage is present. This output is turned off (high-impedance) in sleep mode. The  $\overline{\text{PG}}$  pin can be used to drive an LED or communicate to the host processor.

### 7.3.8 Charge-Enabled ( $\overline{\text{CE}}$ ) Input (bq24080-Q1)

The  $\overline{\text{CE}}$  digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge and a high-level signal disables the charge and places the device in a low-power mode. A high-to-low transition on this pin also resets all timers and timer fault conditions.

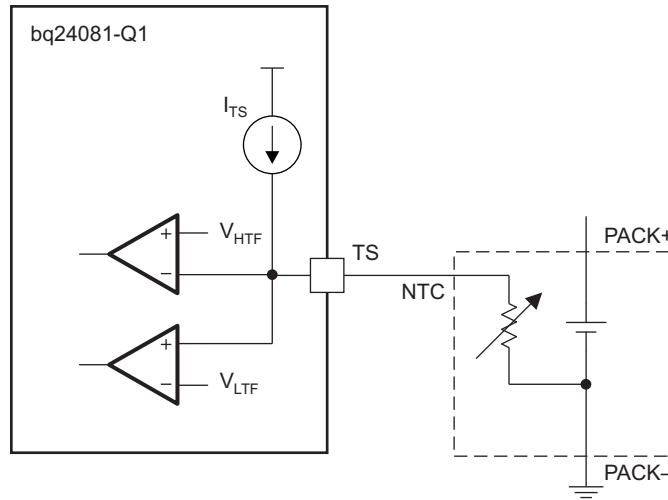
### 7.3.9 Timer Enabled ( $\overline{\text{TE}}$ ) Input (bq24081-Q1)

The  $\overline{\text{TE}}$  digital input is used to disable or enable the fast-charge timer. A low-level signal on this pin enables the fast-charge timer, and a high-level signal disables this feature.

### 7.3.10 Temperature Qualification (bq24081-Q1)

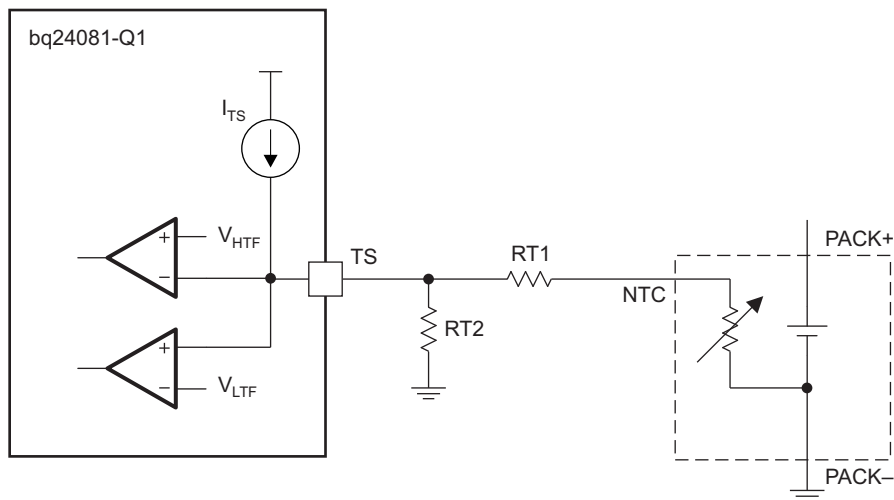
The bq24081-Q1 continuously monitors battery temperature by measuring the voltage between the TS and  $V_{\text{SS}}$  pins. An internal current source provides the bias for common 10-k $\Omega$  negative-temperature-coefficient thermistors (NTC) (see the functional block diagram). The device compares the voltage on the TS pin with the internal  $V_{(\text{TS}1)}$  and  $V_{(\text{TS}2)}$  thresholds to determine if charging is allowed. If a temperature outside the  $V_{(\text{TS}1)}$  and  $V_{(\text{TS}2)}$  thresholds is detected, the device immediately suspends the charge by turning off the power FET and holding the timer value (i.e., timers are not reset). Charge is resumed when the temperature returns within the normal range.

The allowed temperature range with a 103AT-type thermistor is 0°C to 45°C. However, the user may modify these thresholds by adding external resistors (see [Figure 8](#) and [Figure 9](#)).



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**Figure 8. Default Temperature Thresholds**



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**Figure 9. Temperature Thresholds Modified by External Resistors**

### 7.3.11 Timer Fault and Recovery

As shown in [Figure 7](#), the device provides a recovery method to deal with timer fault conditions. The following summarizes this method:

#### 7.3.11.1 Condition Number 1

OUT pin voltage is above the recharge threshold ( $V_{(RCH)}$ ), and a timeout fault occurs.

Recovery method: the device waits for the OUT pin voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge, or battery removal. Once the OUT pin voltage falls below the recharge threshold, the device clears the fault and starts a new charge cycle. A POR,  $\overline{TE}$ , or  $\overline{CE}$  toggle also clears the fault.

#### 7.3.11.2 Condition Number 2

OUT pin voltage is below the recharge threshold ( $V_{(RCH)}$ ), and a timeout fault occurs

Recovery method: Under this scenario, the device applies the  $I_{(FAULT)}$  current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the OUT pin voltage goes above the recharge threshold, then the device disables the  $I_{(FAULT)}$  current and executes the recovery method described for condition number 1. Once the OUT pin voltage falls below the recharge threshold, the bq24080-Q1 clears the fault and starts a new charge cycle. A POR,  $\overline{TE}$ , or  $\overline{CE}$  toggle also clears the fault.

## 7.4 Device Functional Modes

### 7.4.1 Sleep Mode

The device enters the low-power sleep mode if the input power (IN) is removed from the circuit. This feature prevents draining the battery during the absence of input supply.

## 8 Application and Implementation

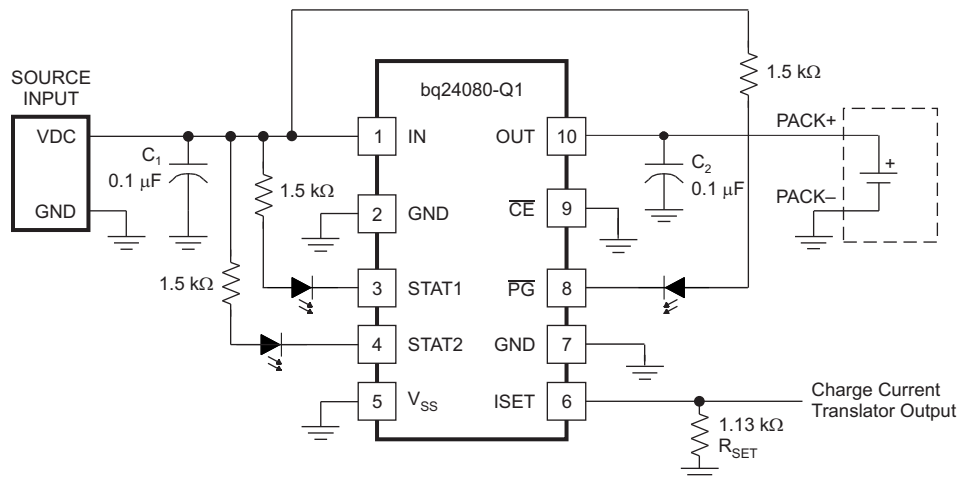
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The bq2408X-Q1 device is Lithium chemistry (Lithium Ion and Lithium Polymer) charger that is intended for automotive applications. The allows the designer to pick an automotive qualified charger for applications where the Li chemistry is needed. Such applications may involve E-Call (back up safety call) or infotainment systems within the automotive space. The device comes completely ready with an integrated charge current monitor and safety timers. The LDO based charger design allows for a cost optimized safe charging algorithm.

### 8.2 Typical Application



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**Figure 10. Typical Application Circuit**

#### 8.2.1 Design Requirements

For this design example, use the parameters shown in [Table 2](#).

**Table 2. Design Parameters**

PARAMETER	VALUE
Supply voltage	5 V
Fast-charge current	≈ 750 mA
Battery-Temperature sense (bq24081-Q1)	-2°C to 44.5°C (default setting)

## 8.2.2 Detailed Design Procedure

### 8.2.2.1 Calculations

Program the charge current for 750 mA:

$$R_{\text{ISET}} = [V_{(\text{SET})} \times K_{(\text{SET})} / I_{(\text{OUT})}] \quad (5)$$

From [Electrical Characteristics](#) table,  $V_{(\text{SET})} = 2.5 \text{ V}$ .

From [Electrical Characteristics](#) table,  $K_{(\text{SET})} = 322$ .

$$R_{\text{ISET}} = [2.5 \text{ V} \times 322 / 0.75 \text{ A}] = 1.073 \text{ k}\Omega \quad (6)$$

Selecting the closest standard value, use a 1.07-k $\Omega$  resistor connected between ISET (pin 6) and ground.

### 8.2.2.2 Battery Temperature Sense (bq24081-Q1):

Use a Semitec 103AT-4 NTC thermistor connected between TS (pin 9) and ground.

$$R_{\text{THERM-cold}} = [V_{(\text{TS1})} / I_{(\text{TS})}] = 2.5 \text{ V} / 100 \mu\text{A} = 25 \text{ k}\Omega \quad (7)$$

$$R_{\text{THERM-hot}} = [V_{(\text{TS2})} / I_{(\text{TS})}] = 0.5 \text{ V} / 100 \mu\text{A} = 5 \text{ k}\Omega \quad (8)$$

Look up the corresponding temperature value in the manufacturer's resistance-temperature table for the thermistor selected. For a 103AT-4 Semitec thermistor:

$$5 \text{ k}\Omega = 44.5^\circ\text{C}$$

$$25 \text{ k}\Omega = 2^\circ\text{C}$$

### 8.2.2.3 STAT Pins (All Devices) and PG Pin (bq24080-Q1):

Status pins Monitored by Processor:

Select a pullup resistor that can source more than the input bias (leakage) current of both the processor and status pins and still provide a logic high.

$$R_{\text{PULLUP}} \leq [V_{(\text{CC-pullup})} - V_{(\text{logic hi-min})} / (I_{(\mu\text{P-monitor})} + I_{(\text{STAT-OpenDrain})})] = (3.3 \text{ V} - 1.9 \text{ V}) / (1 \mu\text{A} + 1 \mu\text{A}) \leq 700 \text{ k}\Omega; \quad (9)$$

Connect a 100-k $\Omega$  pullup between each status pin and the  $V_{\text{CC}}$  of the processor. Connect each status pin to a  $\mu\text{P}$  monitor pin.

Status viewed by LED:

Select an LED with a current rating less than 10 mA and select a resistor to place in series with the LED to limit the current to the desired current value (brightness).

$$R_{\text{LED}} = [(V_{(\text{IN})} - V_{(\text{LED-on})}) / I_{(\text{LED})}] = (5 \text{ V} - 2 \text{ V}) / 1.5 \text{ mA} = 2 \text{ k}\Omega. \quad (10)$$

Place an LED and resistor in series between the input and each status pin.

### 8.2.2.4 Selecting Input and Output Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor on the input power pin. A 0.1- $\mu\text{F}$  ceramic capacitor, placed in close proximity to the IN pin and GND pad works well. In some applications, it may be necessary to protect against a hot plug input voltage overshoot. This is done in three ways:

1. The best way is to add an input zener, 6.2 V, between the IN pin and  $V_{\text{SS}}$ .
2. A low-power zener is adequate for the single event transient. Increasing the input capacitance lowers the characteristic impedance which makes the input resistance more effective at damping the overshoot, but risks damaging the input contacts by the high inrush current.
3. Placing a resistor in series with the input dampens the overshoot, but causes excess power dissipation.

The device only requires a small capacitor for loop stability. A 0.1- $\mu\text{F}$  ceramic capacitor placed between the OUT and GND pad is typically sufficient.



### 8.2.3 Application Curves

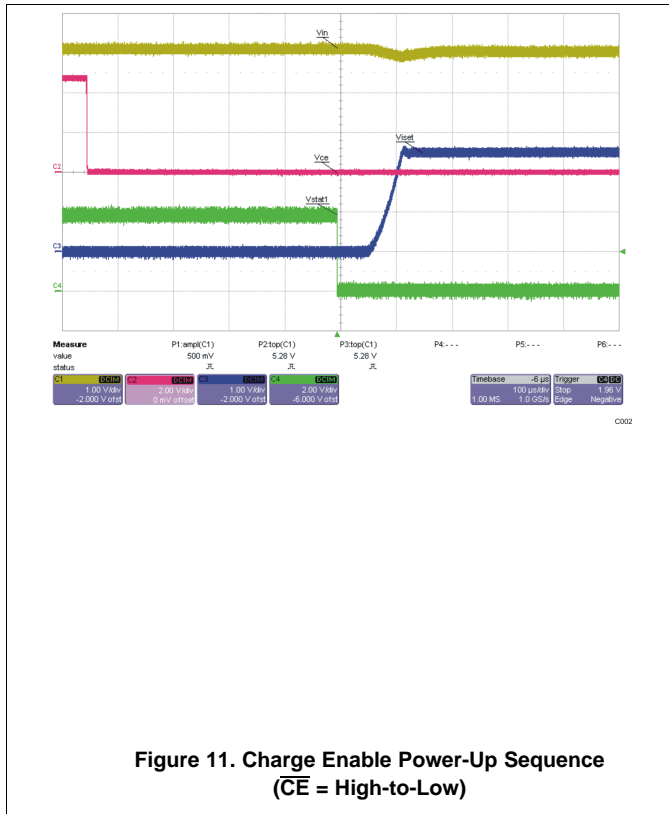


Figure 11. Charge Enable Power-Up Sequence (CE = High-to-Low)

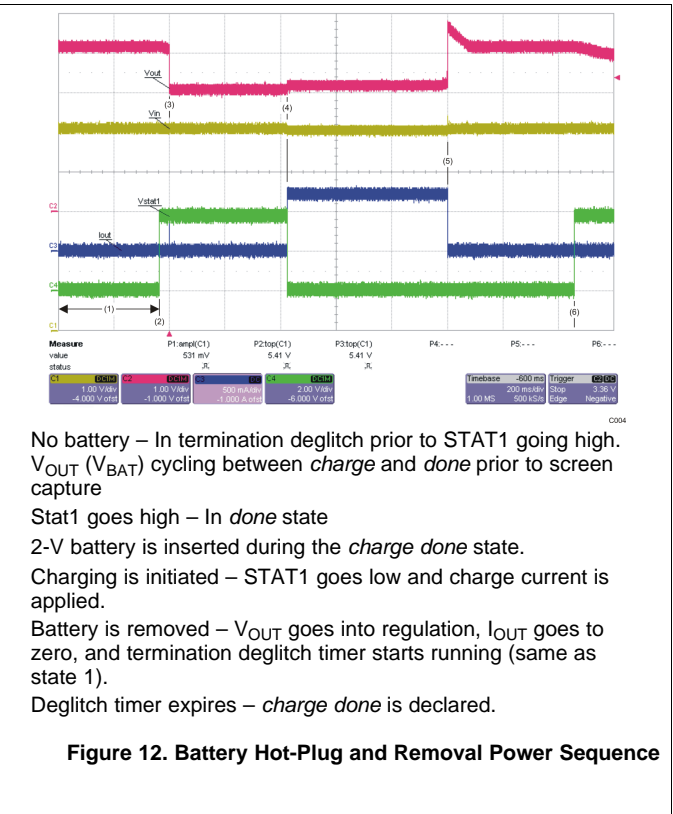


Figure 12. Battery Hot-Plug and Removal Power Sequence

No battery – In termination deglitch prior to STAT1 going high.  $V_{OUT}$  ( $V_{BAT}$ ) cycling between *charge* and *done* prior to screen capture  
 Stat1 goes high – In *done* state  
 2-V battery is inserted during the *charge done* state.  
 Charging is initiated – STAT1 goes low and charge current is applied.  
 Battery is removed –  $V_{OUT}$  goes into regulation,  $I_{OUT}$  goes to zero, and termination deglitch timer starts running (same as state 1).  
 Deglitch timer expires – *charge done* is declared.

## 9 Power Supply Recommendations

The devices are intended to operate within the ranges shown in Recommended Operating Conditions. Because the input of the device on pin IN is subject to a power source that is external, care must be taken to not exercise the pin above the Absolute Maximum Rating of the Pin shown in the [Absolute Maximum Ratings](#) table.

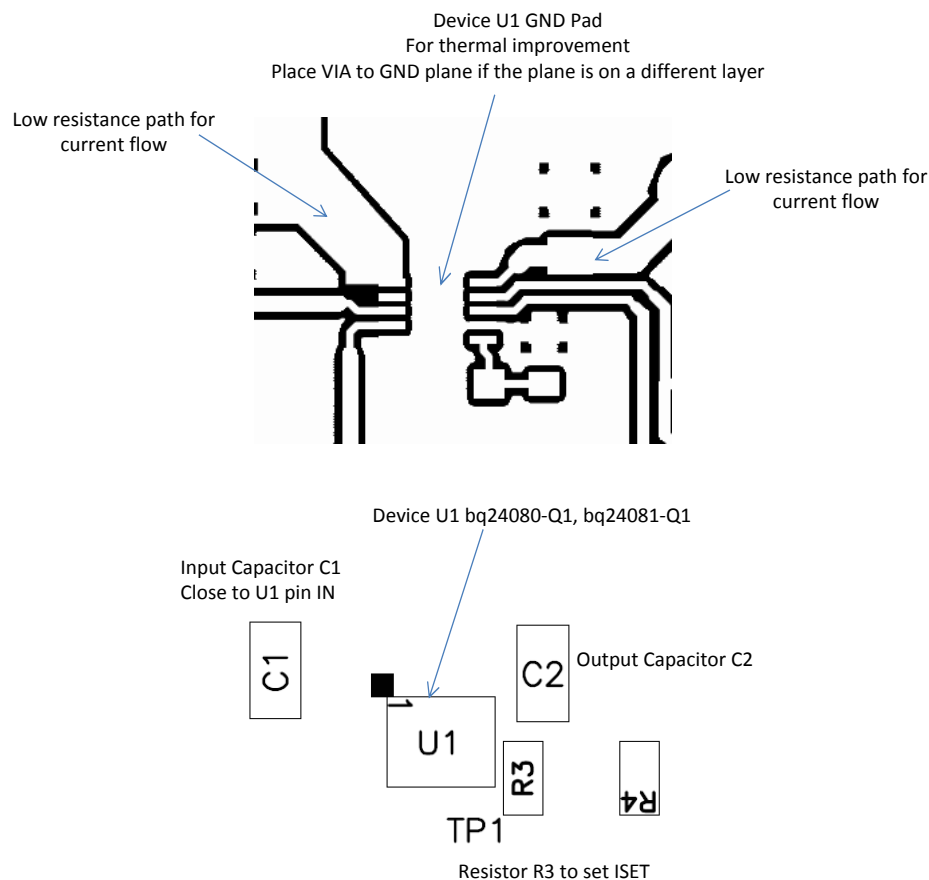
## 10 Layout

### 10.1 Layout Guidelines

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from  $V_{CC}$  to  $V_{(IN)}$  and the output filter capacitors from OUT to  $V_{SS}$  should be placed as close as possible to the device, with short trace runs to both signal and  $V_{SS}$  pins. The  $V_{SS}$  pin should have short trace runs to the GND pin.
- All low-current  $V_{SS}$  connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small-signal ground path and the power ground path.
- The high-current charge paths into IN and from the OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The device is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application report entitled, *QFN/SON PCB Attachment* (TI Literature Number [SLUA271](#)).

### 10.2 Layout Example



**Figure 13. Board Layout**

### 10.3 Thermal Considerations

The bq24080-Q1 and bq24081-Q1 are packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed-circuit board (PCB). Full PCB design guidelines for this package are provided in the application report entitled, *QFN/SON PCB Attachment* (TI Literature Number [SLUA271](#)).

The most common measure of package thermal performance is thermal impedance ( $R_{\theta JA}$ ) measured (or modeled) from the device junction to the air surrounding the package surface (ambient). The mathematical expression for  $R_{\theta JA}$  is:

$$R_{\theta JA} = \frac{T_J - T_A}{P} \quad (11)$$

Where:

- $T_J$  = device junction temperature
- $T_A$  = ambient temperature
- $P$  = device power dissipation

Factors that can greatly influence the measurement and calculation of  $R_{\theta JA}$  include:

- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested
- Use multiple 10–13 mil vias in the PowerPAD™ to copper ground plane.
- Avoid cutting the ground plane with a signal trace near the power IC.
- The PCB must be sized to have adequate surface area for heat dissipation.
- FR4 (figerglass) thickness should be minimized.

The device power dissipation,  $P$ , is a function of the charge rate and the voltage drop across the internal Power FET. It can be calculated from the following equation:

$$P = (V_{(IN)} - V_{(OUT)}) \times I_{O(OUT)} \quad (12)$$

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See [Figure 6](#).

## 11 器件和文档支持

### 11.1 器件支持

### 11.2 文档支持

《QFN/SON PCB 连接》（文献编号：[SLUA271](#)）。

### 11.3 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 3. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
bq24080-Q1	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
bq24081-Q1	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>

### 11.4 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

### 11.5 社区资源

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### 11.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24081QDRCRQ1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ZACQ	Samples
BQ24081QDRCTQ1	PREVIEW	VSON	DRC	10	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF BQ24081-Q1 :**

- Catalog : [BQ24081](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24081QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24081QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0



## GENERIC PACKAGE VIEW

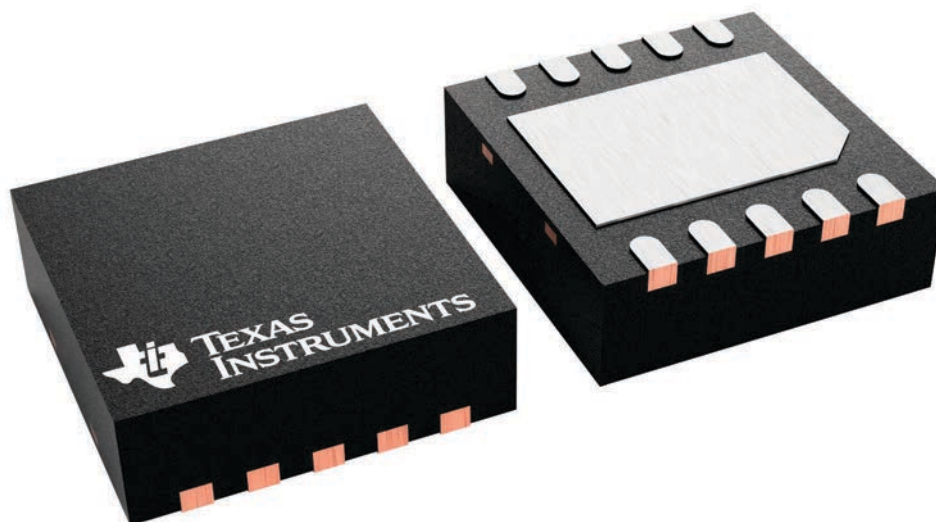
**DRC 10**

**VSON - 1 mm max height**

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226193/A



# EXAMPLE BOARD LAYOUT

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

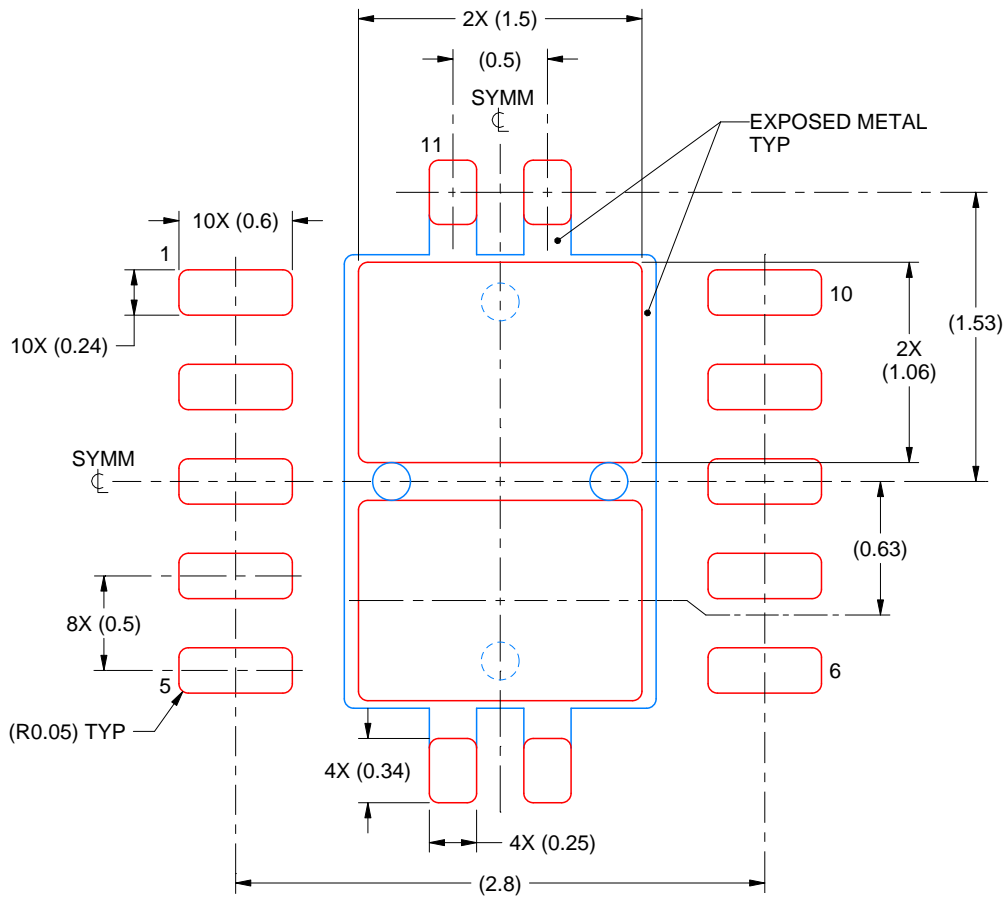
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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[ISL9538HRTZ](#) [ISL95522AIRZ](#) [S-82D1AAA-A8T2U7](#) [S-8224ABA-I8T1U](#) [MP2615CGQ-P](#) [ISL6251HRZ](#) [ISL6253HRZ](#) [ISL6292-2CR3](#)  
[ISL6292BCRZ-T](#) [ISL6299AIRZ](#) [ISL9211AIRU58XZ-T](#) [ISL9214IRZ](#) [ISL9220IRTZ-T](#) [FAN54161UCX](#) [SY6982CQDC](#)  
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[MP26124GR-Z](#) [MP2664GG-0000-Z](#) [MP26029GTF-0000-Z](#) [MP2695GQ-0000-Z](#) [XB5608AJ](#)