TEXAS INSTRUMENTS

bq294602, bq294604, bq294682, bq294624

ZHCS624D – DECEMBER 2011 – REVISED APRIL 2017

用于锂离子电池的 bq2946xx 单节电池保护器

1 特性

- 用于二级保护的单节电池过压监视器
- 固定可编程延迟计时器
- 固定过压保护 (OVP) 阈值
  - 3.85V 至 4.6V 的可用范围
- 固定 OVP 延迟选项：4s 或 6.5s
- 高精度 OVP：
  ±10mV
- 低功耗 I_{CC} ≈ 1μA
  ($V_{CELL(ALL)}$ < $V_{PROTECT}$)
- 每节电池输入的泄漏电流低于 100nA
- 小封装尺寸
  - 6 引脚 SON

2 应用

- 用于下列产品的锂离子电池组中的二级保护：
  - 平板电脑
  - 手写板电脑
  - 便携式设备和仪器

3 说明

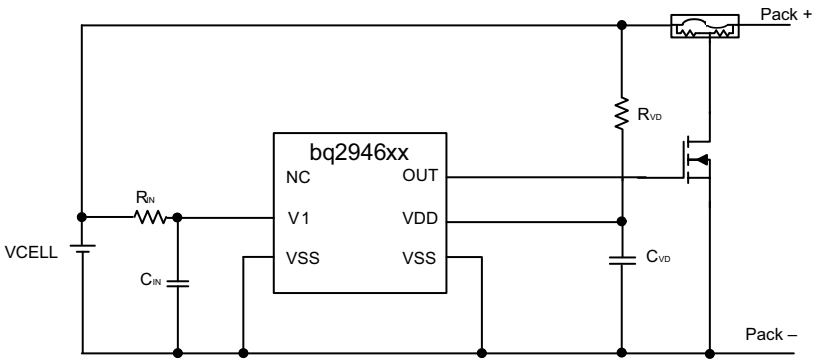
bq2946xx 系列产品是用于锂离子电池组系统的二级过压监视器和保护器。该系列产品监视电池的过压状况，一旦超过 OVP 阈值就触发内部计数器；在经过设置的固定延迟之后，输出转换为高电平。如果电池电压下降至低于设定阈值减去迟滞所得的值，输出将会复位（变为低电平）。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
bq294602	SON (6)	2.00mm × 2.00mm
bq294604		
bq294682		
bq294624		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (July 2015) to Revision D — **Page**

- 已添加 在*器件信息* 中添加了 bq294624 ... 1
- Added the bq294624 device into production ... 3
- 已添加 添加了*接收文档更新通知* 部分 ... 13

Changes from Revision B (March 2012) to Revision C — **Page**

- 已添加 添加了 *ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 已添加 在“说明”中添加了 “过压” ... 1
- 已更改 更改了项目以合并特性项 ... 1
- 已添加 在 “特性”中添加了“固定 OVP 延迟选项” ... 1
- 已更改 更改了 说明的措辞 ... 1
- Added the bq294682 device into production ... 3

Changes from Revision A (February 2012) to Revision B — **Page**

- Added a second I_{CC} Test Condition ... 5

Changes from Original (December 2011) to Revision A — **Page**

- Added the bq294604 device into production ... 3

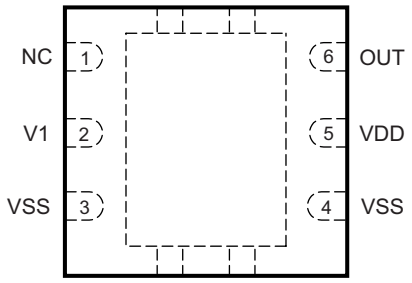
5 Device Options

T_A	PART NUMBER	OVP (V)	DELAY TIME (s)
–40°C to +110°C	bq294602	4.35	4
	bq294604	4.35	6.5
	bq294622(1)	4.45	4
	bq294624	4.45	6.5
	bq294682	4.225	4
	bq294684(1)	4.225	6.5

(1) Product Preview only.

6 Pin Configuration and Functions

DRV Package
6-Pin SON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
NC	1	—	No connection
OUT	6	OA	Output drive for external N-channel FET.
PWRPAD	Thermal Pad	—	VSS pin to be connected to the PWRPAD on the printed-circuit-board (PCB) for proper operation.
V1	2	IA	Sense input for positive voltage of the cell.
VSS	3	P	Electrically connected to IC ground and negative terminal of the cell.
VSS	4	P	Electrically connected to IC ground and negative terminal of the cell.
VDD	5	P	Power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	VDD–VSS	–0.3	30	V
Input voltage	V1–VSS	–0.3	8	V
Output voltage	OUT–VSS	–0.3	30	V
Continuous total power dissipation, P_{TOT}		See *Thermal Information*		
Functional temperature		–65	110	°C
Lead temperature (soldering, 10 s), T_{SOLDER}			300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{DD}(1)		3	8	V
Input voltage	V1–VSS	0	5	V
Operating ambient temperature, T_A		–40	110	°C

(1) See *Typical Application*.

7.4 Thermal Information

THERMAL METRIC(1)		bq2946xx DRV (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	186.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	90.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	110.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	96.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VDD = 4 V, MIN/MAX values stated where T_A = –40°C to +110°C and V_{DD} = 4 V (unless otherwise noted)

TEST NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE PROTECTION THRESHOLD VCx							
1.0	V_{OV}	$V_{(PROTECT)}$ – Overvoltage Detection	bq294602, fixed delay 4 s, V1 > V_{OV}		4.35		V
1.1			bq294604, fixed delay 6.5 s, V1 > V_{OV}		4.35		
1.2			bq294622, fixed delay 4 s, V1 > V_{OV} (1)		4.45		
1.3			bq294624, fixed delay 6.5 s, V1 > V_{OV}		4.45		
1.4			bq294682, fixed delay 4 s, V1 > V_{OV}		4.225		
1.5			bq294684, fixed delay 6.5 s, V1 > V_{OV} (1)		4.225		
1.6	V_{HYS}	Overvoltage Detection Hysteresis		250	300	400	V
1.7	V_{OA}	OV Detection Accuracy	T_A = 25°C	–10		10	mV
1.8	$V_{OA\ –DRIFT}$	OV Detection Accuracy due to Temperature	T_A = –40°C T_A = 0°C T_A = 60°C T_A = 110°C	–40 –20 –24 –54		44 20 24 54	mV
SUPPLY AND LEAKAGE CURRENT							
1.9	I_{CC}	Supply Current	(V1–VSS) = 4.0 V (see Figure 7 for reference)		1	2	µA
			(V1–VSS) = 2.8 V with T_A = –40°C to +60°C			1.25	
1.10	I_{IN}	Input Current at V1 Pins	Measured at V1 = 4.0 V (V1–VSS) = 4.0 V T_A = 0°C to 60°C (see Figure 7 for reference)	–0.1		0.1	µA
OUTPUT DRIVE OUT							
1.11	V_{OUT}	Output Drive Voltage	(V1–VSS) > V_{OV} V_{DD} = V1, I_{OH} = 100 µA, T_A = –40°C to +110°C	3	V_{DD} – 0.3		V
1.12							
1.13			(V1–VSS) < V_{OV}, I_{OL} = 100 µA, T_A = 25°C T_A = –40°C to +110°C		250	400	mV
1.14	$I_{OUT(Short)}$	OUT Short Circuit Current	OUT = 0 V, (V1–VSS) > V_{OV}		1.5	3	mA
1.15	t_R	Output Rise Time	CL = 1 nF, $V_{OH(OUT)}$ = 0 V to 5 V (2)		5		µs
1.16	Z_O	Output Impedance			2	5	kΩ
FIXED DELAY TIMER							
1.17	t_{DELAY}	Fault Detection Delay Time	Fixed Delay, bq2946x2	3.2	4	4.8	s
			Fixed Delay, bq2946x4	5.2	6.5	7.8	
1.18	t_{DELAY_CTM}	Fault Detection Delay Time in Test Mode	Fixed Delay (Internal settings)		15		ms

(1) Product Preview only.
(2) Specified by design. Not 100% tested in production.

7.6 Typical Characteristics

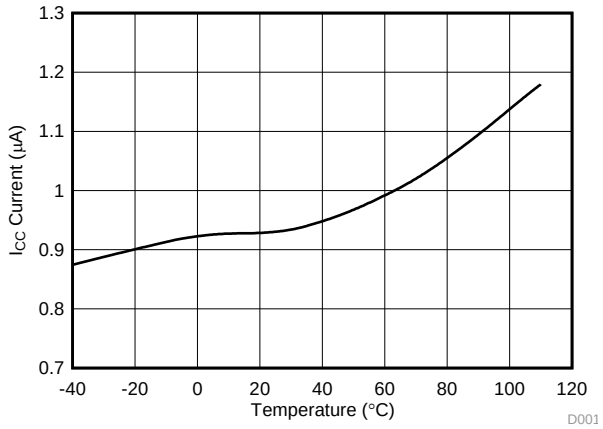


Figure 1. I_{CC} Current Consumption vs Temperature

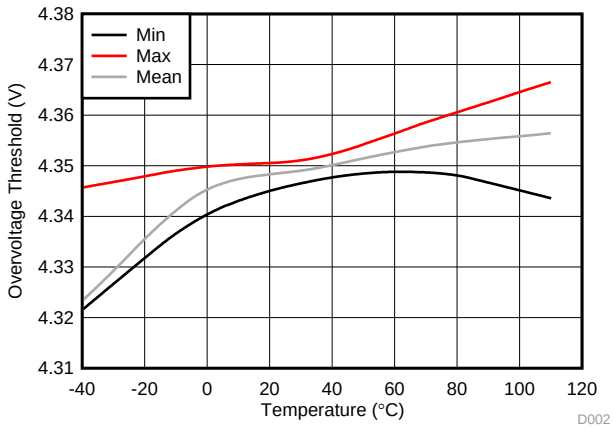


Figure 2. bq294602 Overvoltage Threshold (OVT) vs Temperature

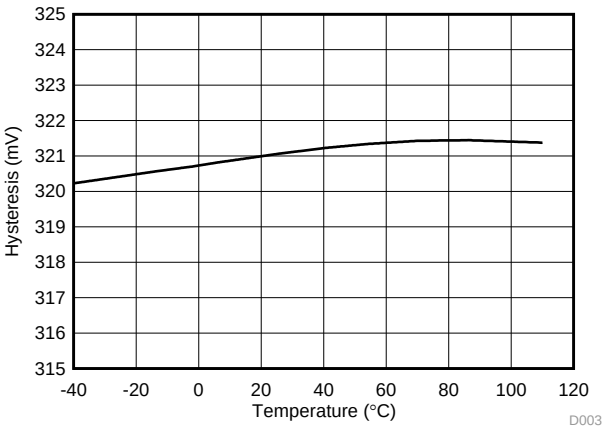


Figure 3. Hysteresis V_{HYS} vs Temperature

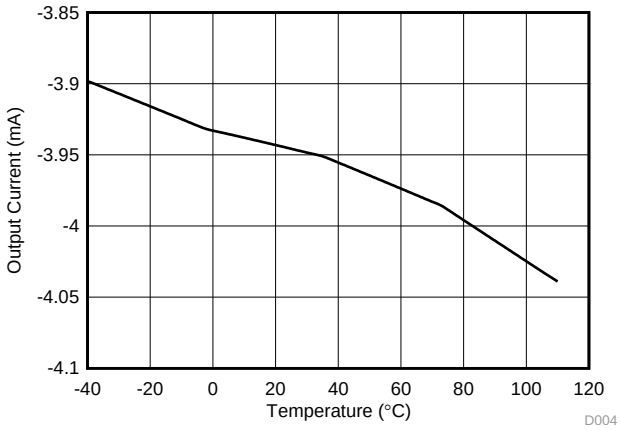


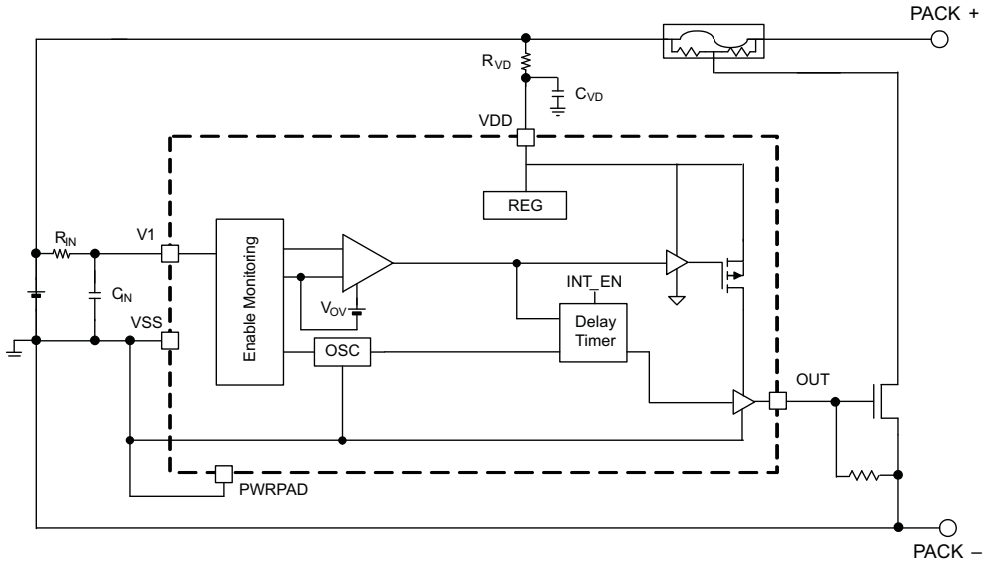
Figure 4. Output Current I_{OUT} vs Temperature

8 Detailed Description

8.1 Overview

The bq2946xx is a second-level overvoltage (OV) protector for a single cell. The cell voltage is compared to a protection voltage threshold, V_{OV}. The protection threshold is preprogrammed at the factory with a range from 3.85 V to 4.65 V. When the OVP is triggered, the OUT pin goes high to activate an external N-channel FET, which conducts a low-impedance path to blow a fuse.

8.2 Functional Block Diagram



8.3 Feature Description

The method of overvoltage detection is comparing the cell voltage to an OVP threshold voltage V_{OV}. Once the cell voltage exceeds the programmed fixed value V_{OV}, the delay timer circuit is activated. This delay (t_{DELAY}) is fixed for 4 seconds for the bq294602 device. When these conditions are satisfied, the OUT terminal is transitioned to a high level. This output (OUT) is released to a low condition if the cell input (V1) is below the OVP threshold minus the V_{HYS}.

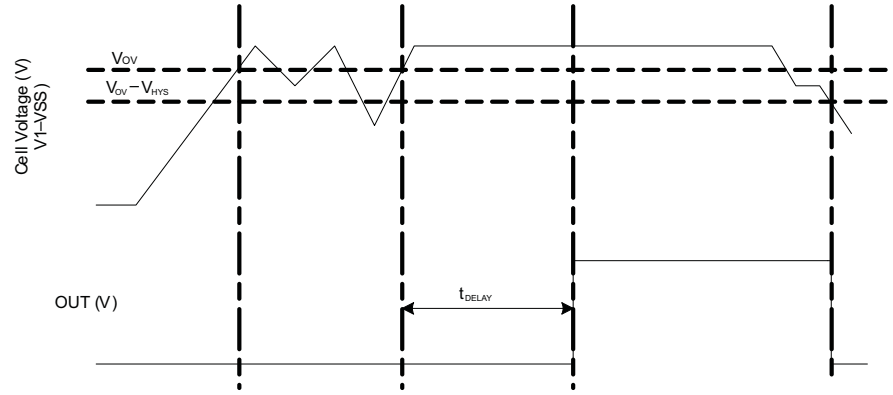


Figure 5. Timing for Overvoltage Sensing

8.3.1 Sense Positive Input for V1

This is an input to sense single battery cell voltage. A series resistor and a capacitor across the cell is required for noise filtering and stable voltage monitoring.

Feature Description (continued)

8.3.2 Output Drive, OUT

The gate of an external N-channel MOSFET is connected to this terminal. This output transitions to a high level when an overvoltage condition is detected and after the programmed delay timer. The OUT will reset to a low level if the cell voltage falls below the V_{OV} threshold before the fixed delay timer expires.

8.3.3 Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

8.3.4 Thermal Pad, PWRPAD

For correct operation, the power pad (PWRPAD) is connected to the V_{SS} terminal on the PCB.

8.4 Device Functional Modes

8.4.1 NORMAL Mode

When the cell voltage is below the overvoltage threshold, V_{OV}, the device operates in NORMAL mode. The OUT pin is inactive and is low.

8.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if the cell voltage exceeds the overvoltage threshold, V_{OV}, for configured OV delay time. The OUT pin is activated, internally pulled high, after a delay time, tDELAY. An external FET then turns on, shorting the fuse to ground, which allows the battery and/or charger power to blow the fuse. When the cell voltages fall below (VOV – VHYS), the device returns to NORMAL mode.

8.4.3 Customer Test Mode

Customer Test Mode (CTM) helps reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least 10 V higher than V1 (see Figure 6). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit CTM, remove the VDD to V1 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into CTM. Also avoid exceeding Absolute Maximum Voltage for the cell voltage (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 6 shows the timing for the CTM.

Device Functional Modes (continued)

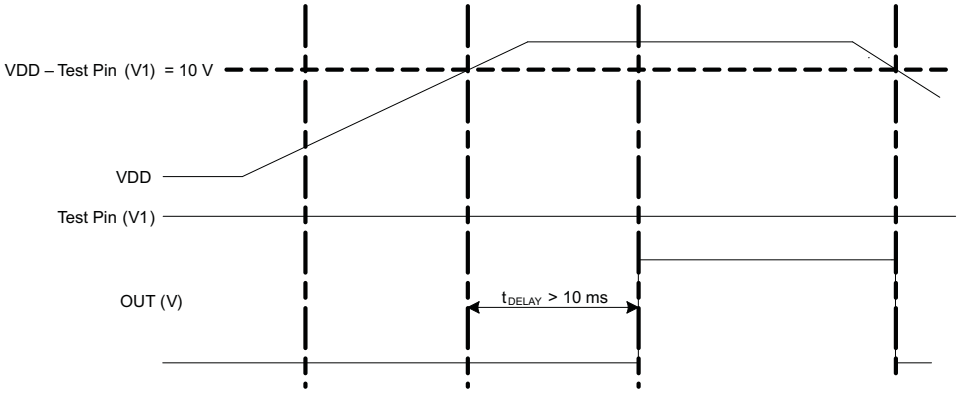


Figure 6. Timing for Customer Test Mode

Figure 7 shows the measurement for current consumption for the product for both VDD and Vx.

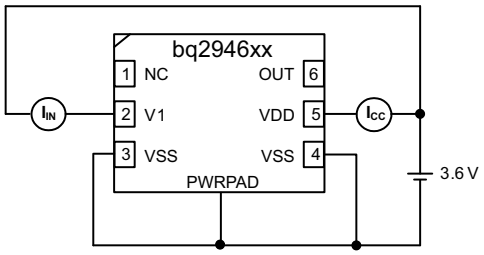


Figure 7. Configuration for IC Current Consumption Test

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq2946xx devices are a family of second-level protectors used for overvoltage protection of the single-cell battery pack in the application. The OUT pin drives a NMOS FET that connects the fuse to ground in the event of a fault condition. This provides a shorted path to use the battery and/or charger power to blow the fuse and cut the power path.

9.1.1 Application Configuration

Changes to the ranges stated in Table 1 may impact the accuracy of the cell measurements. Figure 8 shows each external component.

NOTE

Connect VSS (pins 3 and 4) externally to the CELL– terminal.

9.2 Typical Application

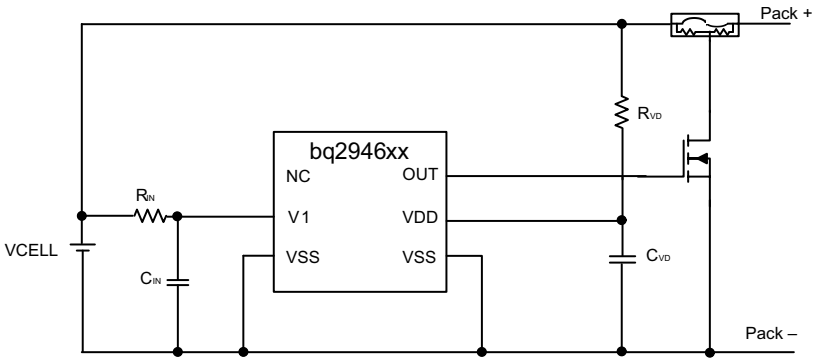


Figure 8. Application Configuration Schematic

NOTE

Connect VSS (pins 3 and 4) externally to the CELL– terminal.

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	RIN	900	1000	1100	Ω
Voltage monitor filter capacitance	CIN	0.01	0.1		µF
Supply voltage filter resistance	RVD	100		1K	Ω
Supply voltage filter capacitance	CVD		0.1		µF

9.2.2 Detailed Design Procedure

1. Determine the overvoltage protection and delay. Select a device with the corresponding thresholds.
2. Follow the application schematic (see Figure 8) to connect the device.
3. Ensure both Vss pins are connected to the CELL– terminal on the PCB layout.

9.2.3 Application Curves

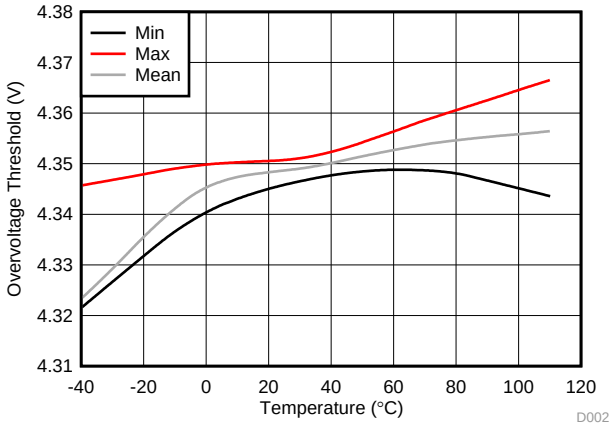


Figure 9. OVT vs Temperature

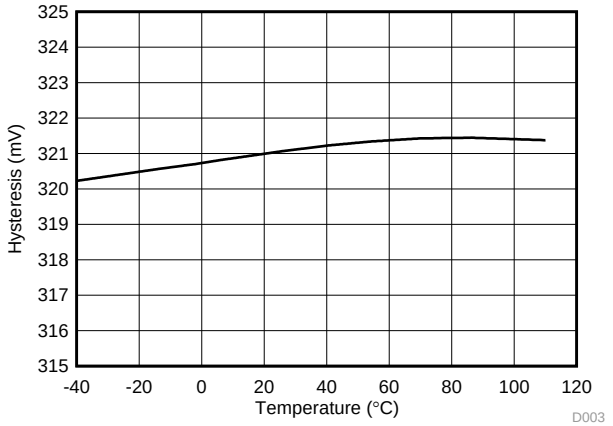


Figure 10. V_{HYS} vs Temperature

9.3 System Example

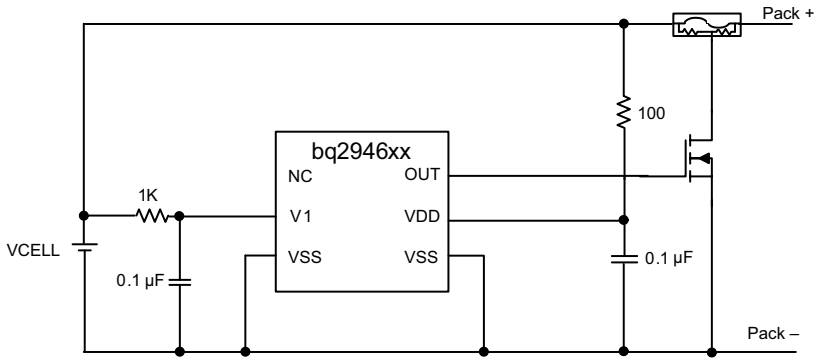


Figure 11. 1-Cell Configuration With Fixed Delay

10 Power Supply Recommendations

The maximum power of this device is 8 V on VDD.

11 Layout

11.1 Layout Guidelines

1. Ensure the RC filters for the V1 and VDD pins are placed as close as possible to the target terminal, reducing the tracing loop area.
2. The VSS pin should be routed to the CELL– terminal.
3. Ensure the trace connecting the fuse to the gate, source of the NFET to the Pack is sufficient to withstand the current during a fuse blown event.

11.2 Layout Example

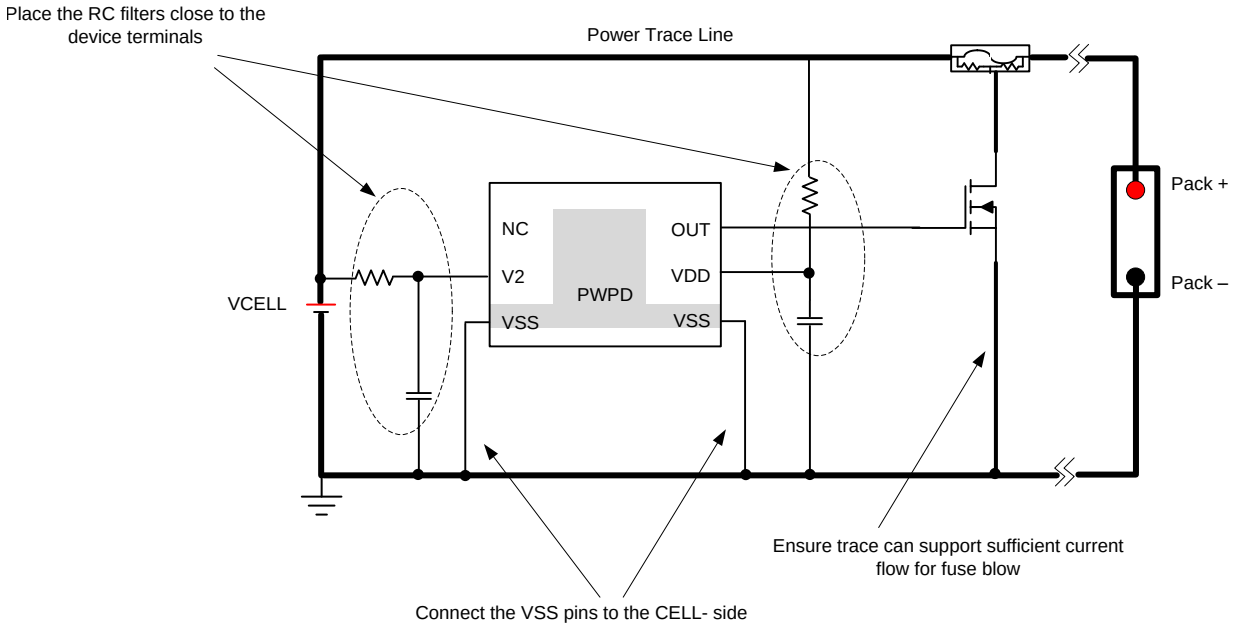


Figure 12. Layout Schematic

12 器件和文档支持

12.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及立即订购快速访问。

表 2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
bq294602	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq294604	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq294682	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*通知我*进行注册，即可收到所有产品信息更改每周摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ294602DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	4602	Samples
BQ294602DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	4602	Samples
BQ294604DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	4604	Samples
BQ294604DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	4604	Samples
BQ294624DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	4624	Samples
BQ294624DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	4624	Samples
BQ294682DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	4682	Samples
BQ294682DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	4682	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

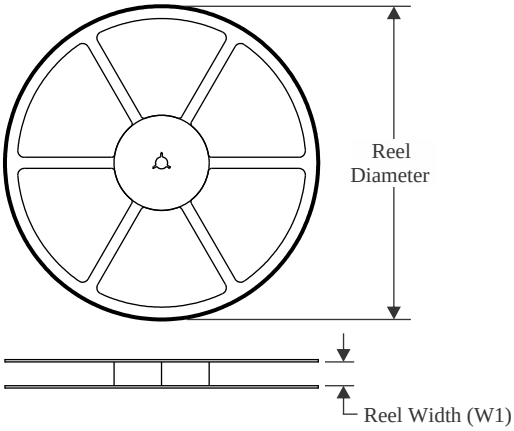
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

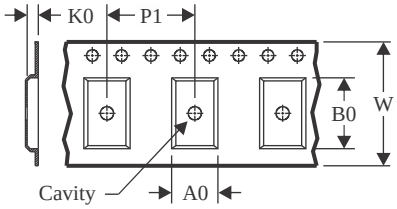
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

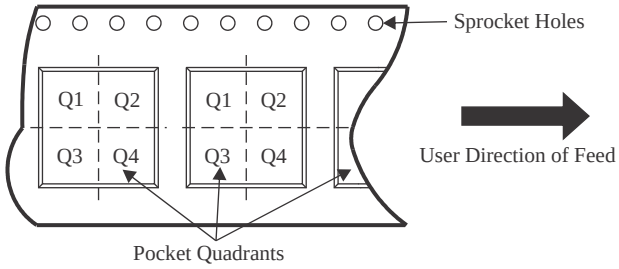


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

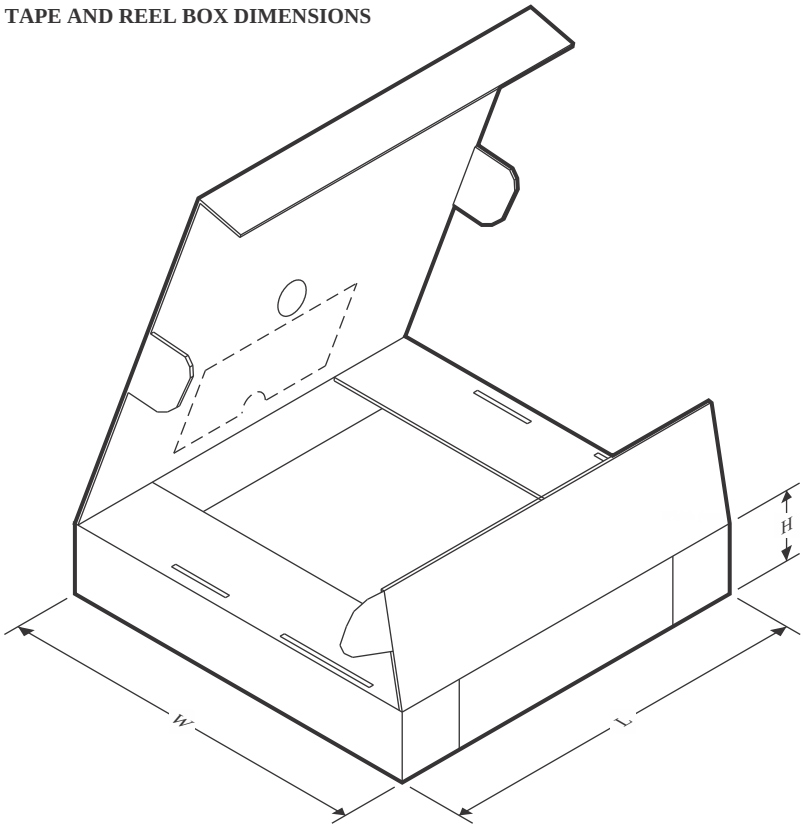
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294602DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294602DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294602DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294604DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294604DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294604DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294604DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294624DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294624DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294682DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294682DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294682DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294682DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

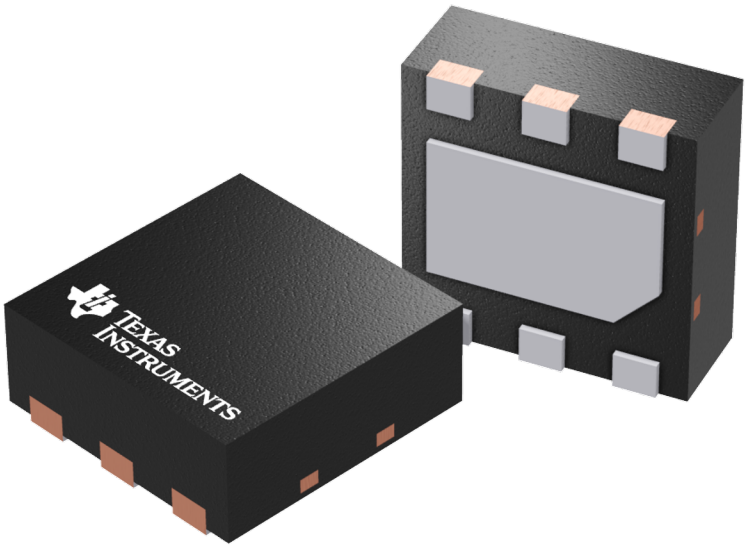


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294602DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294602DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
BQ294602DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294604DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294604DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294604DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294604DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294624DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294624DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294682DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294682DRVR	WSON	DRV	6	3000	182.0	182.0	20.0
BQ294682DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294682DRVT	WSON	DRV	6	250	182.0	182.0	20.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



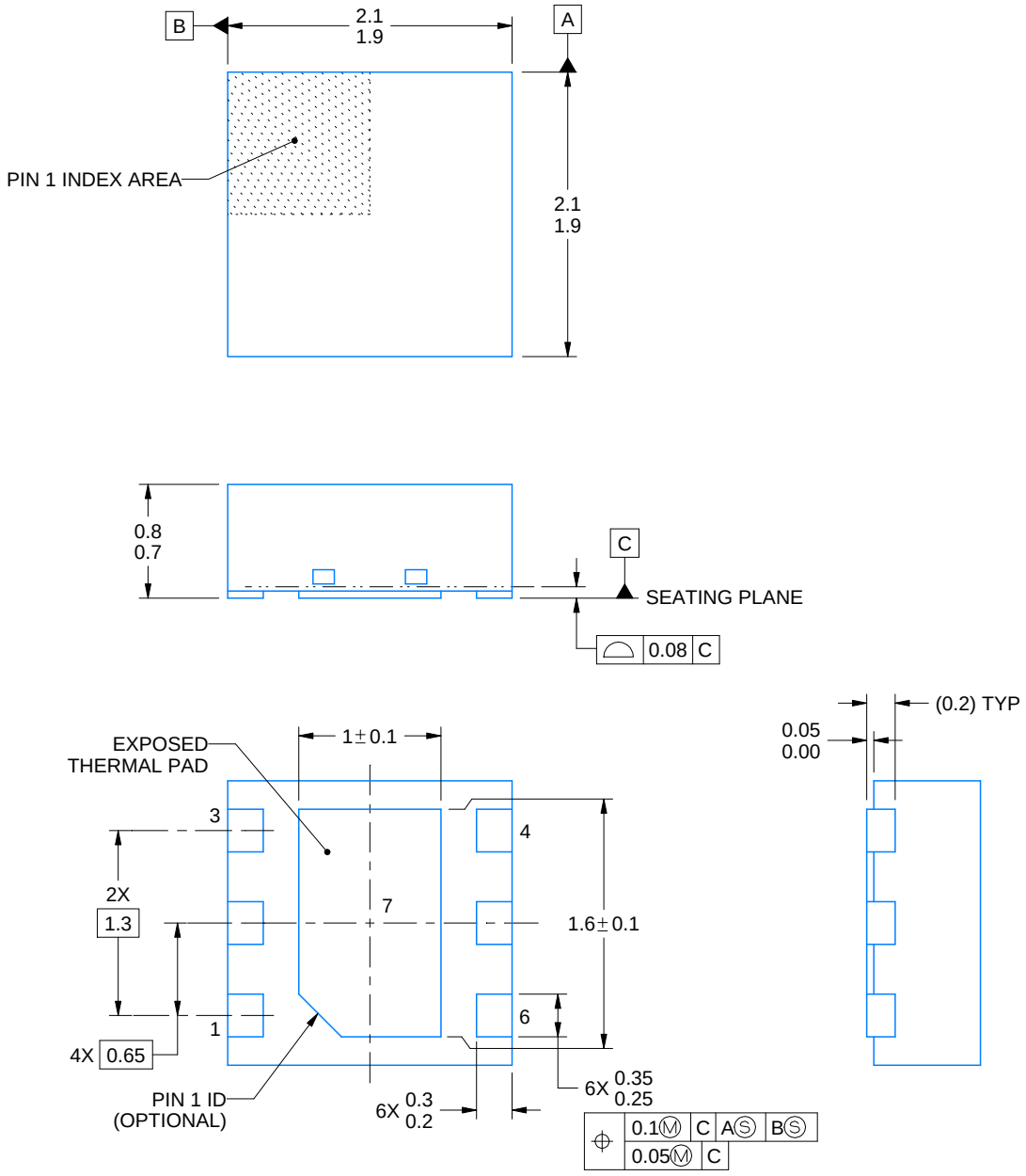
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

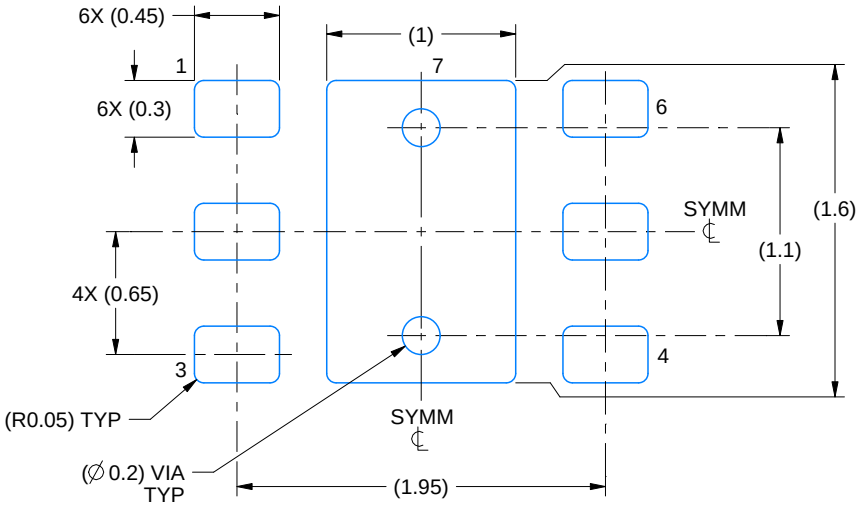
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

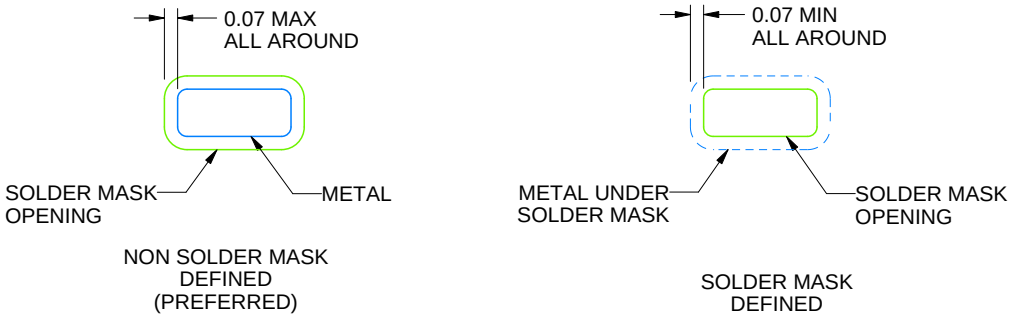


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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NOTES: (continued)

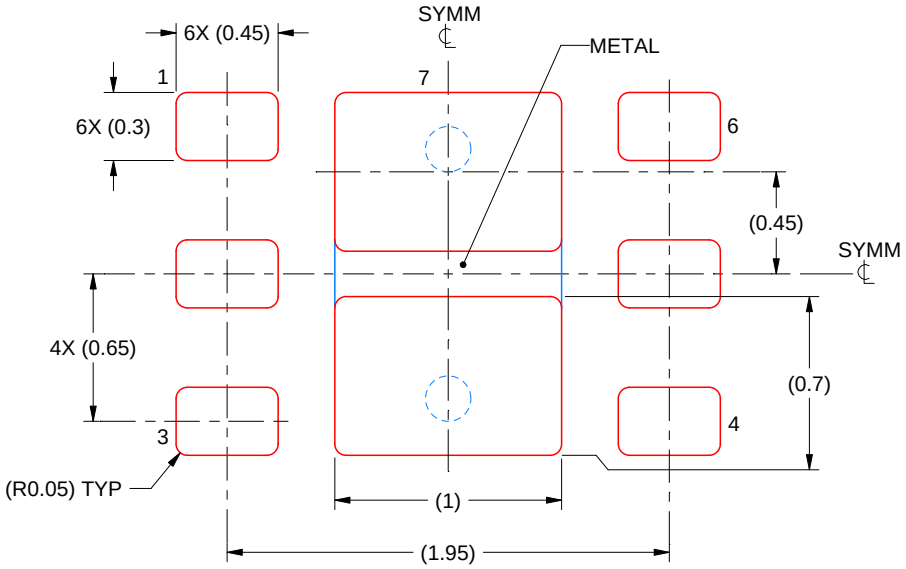
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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