CDCLVD1212 2:12 Low Additive Jitter LVDS Buffer

1 Features

- 2:12 Differential Buffer
- Low Additive Jitter: < 300-fs RMS in 10-kHz to 20-MHz
- Low Output Skew of 35 ps (Maximum)
- Universal Inputs Accept LVDS, LVPECL, and LVCMOS
- Selectable Clock Inputs Through Control Pin
- 12 LVDS Outputs, ANSI EIA/TIA-644A Standard Compatible
- Clock Frequency: Up to 800 MHz
- Device Power Supply: 2.375 V to 2.625 V
- LVDS Reference Voltage, V_{AC_REF}, Available for Capacitive Coupled Inputs
- Industrial Temperature Range: –40°C to 85°C
- Packaged in 6-mm × 6-mm, 40-Pin VQFN (RHA)
- ESD Protection Exceeds 3-kV HBM, 1-kV CDM

2 Applications

- Telecommunications and Networking
- Medical Imaging
- Test and Measurement Equipment
- Wireless Communications
- General-Purpose Clocking

3 Description

The CDCLVD1212 clock buffer distributes one of two selectable clock inputs (IN0 and IN1) to 12 pairs of differential LVDS clock outputs (OUT0 through OUT11) with minimum skew for clock distribution. The CDCLVD1212 can accept two clock sources into an input multiplexer. The inputs can either be LVDS, LVPECL, or LVCMOS.

The CDCLVD1212 is specifically designed for driving 50-Ω transmission lines. In case of driving the inputs in single-ended mode, the appropriate bias voltage, V_{AC_REF}, must be applied to the unused negative input pin.

The IN_SEL pin selects the input which is routed to the outputs. If this pin is left open, it disables the outputs (static). The part supports a fail-safe function. The device incorporates an input hysteresis which prevents random oscillation of the outputs in the absence of an input signal.

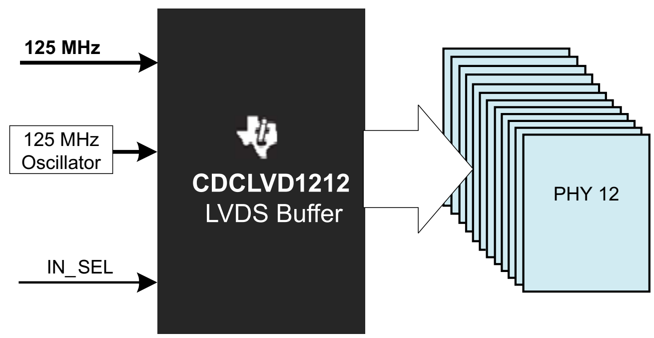
The device operates in 2.5-V supply environment and is characterized from –40°C to 85°C (ambient temperature). The CDCLVD1212 is packaged in small, 40-pin, 6-mm × 6-mm VQFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCLVD1212	VQFN (40)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Example



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2016) to Revision D	Page
• Changed output skew maximum value from: 50 ps to: 35 ps	1

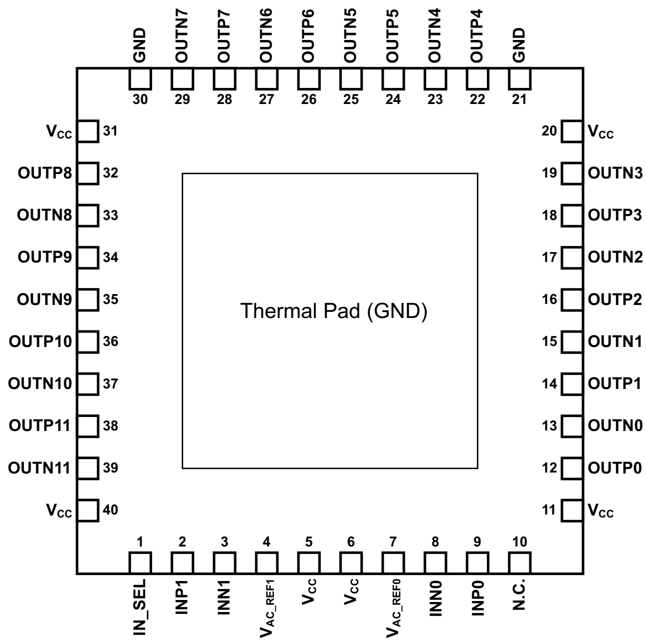
Changes from Revision B (January 2011) to Revision C	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

Changes from Revision A (November 2010) to Revision B	Page
• Changed the device status From: Product Preview To: Production	1

Changes from Original (September 2010) to Revision A	Page
• Deleted the Recommended PCB Layout illustration	16

5 Pin Configuration and Functions

RHA Package
40-Pin VQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN_SEL	Input with an internal 200-kΩ pullup and pulldown	Input selection – selects input port (see Table 1)
2, 3	INP1, INN1	Input	Differential redundant input pair or single-ended input
4	V_{AC_REF1}	Output	Bias voltage output for capacitive coupled inputs. If used, TI recommends using a 0.1-µF to GND on this pin.
5, 6, 11, 20, 31, 40	V_{CC}	Power	2.5-V supplies for the device
7	V_{AC_REF0}	Output	Bias voltage output for capacitive coupled inputs. If used, TI recommends using a 0.1-µF to GND on this pin
9, 8	INP0, INN0	Input	Differential input pair or single-ended input
10	N.C.	—	No connect
12, 13	OUTP0, OUTN0	Output	Differential LVDS output pair no. 0
14, 15	OUTP1, OUTN1	Output	Differential LVDS output pair no. 1
16, 17	OUTP2, OUTN2	Output	Differential LVDS output pair no. 2
18, 19	OUTP3, OUTN3	Output	Differential LVDS output pair no. 3
21, 30	GND	Ground	Device ground
22, 23	OUTP4, OUTN4	Output	Differential LVDS output pair no. 4
24, 25	OUTP5, OUTN5	Output	Differential LVDS output pair no. 5
26, 27	OUTP6, OUTN6	Output	Differential LVDS output pair no. 6
28, 29	OUTP7, OUTN7	Output	Differential LVDS output pair no. 7
32, 33	OUTP8,OUTN8	Output	Differential LVDS output pair no. 8
34, 35	OUTP9,OUTN9	Output	Differential LVDS output pair no. 9
36, 37	OUTP10,OUTN10	Output	Differential LVDS output pair no. 10

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
38, 39	OUTP11,OUTN11	Output	Differential LVDS output pair no. 11
—	Thermal Pad	Ground	Device ground. Thermal pad must be soldered to ground. See thermal management recommendations

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

	MIN	MAX	UNIT
Supply voltage, V_{CC}	–0.3	2.8	V
Input voltage, V_I	–0.2	V_{CC} + 0.2	V
Output voltage, V_O	–0.2	V_{CC} + 0.2	V
Driver short-circuit current, I_{OSD}	See [(2)]		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The output can handle the permanent short.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [(1)]	>3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [(2)]	>1000	

(1) Human-body model, 1.5-kΩ, 100-pF
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Device supply voltage	2.375	2.5	2.625	V
T_A	Ambient temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC [(1)]		CDCLVD1212 RHA (VQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{CC} = 2.375 V to 2.625 V and T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN_SEL CONTROL INPUT CHARACTERISTICS						
V_{dI3}	3-state input	Open		0.5 × V_{CC}		V
V_{dIH}	Input high voltage		0.7 × V_{CC}			V
V_{dIL}	Input low voltage				0.2 × V_{CC}	V
I_{dIH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			30	μA
I_{dIL}	Input low current	V_{CC} = 2.625 V, V_{IL} = 0 V			–30	μA
$R_{pull(IN\_SEL)}$	Input pullup or pulldown resistor			200		kΩ
2.5V LVCMOS (SEE Figure 5) INPUT CHARACTERISTICS						
f_{IN}	Input frequency				200	MHz
V_{th}	Input threshold voltage	External threshold voltage applied to complementary input	1.1		1.5	V
V_{IH}	Input high voltage		V_{th} + 0.1		V_{CC}	V
V_{IL}	Input low voltage		0		V_{th} – 0.1	V
I_{IH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			10	μA
I_{IL}	Input low current	V_{CC} = 2.625 V, V_{IL} = 0 V			–10	μA
ΔV/ΔT	Input edge rate	20%–80%	1.5			V/ns
C_{IN}	Input capacitance			2.5		pF
DIFFERENTIAL INPUT CHARACTERISTICS						
f_{IN}	Input frequency	Clock input			800	MHz
$V_{IN,\ DIFF}$	Differential input voltage peak-to-peak	V_{ICM} = 1.25 V	0.3		1.6	V_{PP}
V_{ICM}	Input common-mode voltage range	$V_{IN,\ DIFF,\ PP}$ > 0.4 V	1		V_{CC} – 0.3	V
I_{IH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			10	μA
I_{IL}	Input low current	V_{CC} = 2.625, V_{IL} = 0 V			–10	μA
ΔV/ΔT	Input edge rate	20%–80%	0.75			V/ns
C_{IN}	Input capacitance			2.5		pF
LVDS OUTPUT CHARACTERISTICS						
$\lvert V_{OD}\rvert$	Differential output voltage magnitude	$V_{IN,\ DIFF,\ PP}$ = 0.3 V, R_L = 100 Ω	250		450	mV
ΔV_{OD}	Change in differential output voltage magnitude		–15		15	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage		1.1		1.375	V
$\Delta V_{OC(SS)}$	Steady-state common-mode output voltage	$V_{IN,\ DIFF,\ PP}$ = 0.6 V, R_L = 100 Ω	–15		15	mV
V_{ring}	Output overshoot and undershoot	Percentage of output amplitude V_{OD}			10%	
V_{OS}	Output AC common mode	$V_{IN,\ DIFF,\ PP}$ = 0.6 V, R_L = 100 Ω		40	70	mV_{PP}
I_{OS}	Short-circuit output current	V_{OD} = 0 V			±24	mA
t_{PD}	Propagation delay	$V_{IN,\ DIFF,\ PP}$ = 0.3 V		1.5	2.5	ns
$t_{SK,\ PP}$	Part-to-part skew				600	ps
$t_{SK,\ O}$	Output skew				35	ps
$t_{SK,P}$	Pulse skew (with 50% duty cycle input)	Crossing-point-to-crossing-point distortion	–50		50	ps
t_{RJIT}	Random additive jitter (with 50% duty cycle input)	Edge speed 0.75 V/ns, 10 kHz – 20 MHz			0.3	ps, RMS
t_R/t_F	Output rise/fall time	20% to 80%, 100 Ω, 5 pF	50		300	ps
I_{CCSTAT}	Static supply current	Outputs unterminated, f = 0 Hz		17	28	mA
I_{CC100}	Supply current	All outputs, R_L = 100 Ω, f = 100 MHz		85	110	mA
I_{CC800}	Supply current	All outputs, R_L = 100 Ω, f = 800 MHz		117	146	mA

Electrical Characteristics (continued)

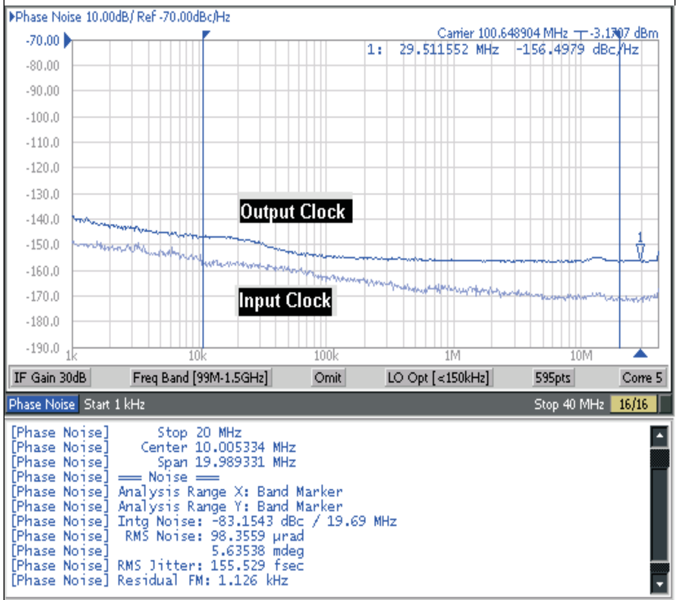
V_{CC} = 2.375 V to 2.625 V and T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AC_REF} CHARACTERISTICS						
V_{AC_REF}	Reference output voltage	V_{CC} = 2.5 V, I_{load} = 100 µA	1.1	1.25	1.35	V

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
ADDITIVE PHASE NOISE FOR 100-MHZ CLOCK					
phn_{100}	Phase noise at 100-Hz offset		–132.9		dBc/Hz
phn_{1k}	Phase noise at 1-kHz offset		–138.8		dBc/Hz
phn_{10k}	Phase noise at 10-kHz offset		–147.4		dBc/Hz
phn_{100k}	Phase noise at 100-kHz offset		–153.6		dBc/Hz
phn_{1M}	Phase noise at 1-MHz offset		–155.2		dBc/Hz
phn_{10M}	Phase noise at 10-MHz offset		–156.2		dBc/Hz
phn_{20M}	Phase noise at 20-MHz offset		–156.6		dBc/Hz
t_{RJIT}	Random additive jitter from 10 kHz to 20 MHz		171		fs, RMS
ADDITIVE PHASE NOISE FOR 737.27-MHZ CLOCK					
phn_{100}	Phase noise at 100-Hz offset		–80.2		dBc/Hz
phn_{1k}	Phase noise at 1-kHz offset		–114.3		dBc/Hz
phn_{10k}	Phase noise at 10-kHz offset		–138		dBc/Hz
phn_{100k}	Phase noise at 100-kHz offset		–143.9		dBc/Hz
phn_{1M}	Phase noise at 1-MHz offset		–145.2		dBc/Hz
phn_{10M}	Phase noise at 10-MHz offset		–146.5		dBc/Hz
phn_{20M}	Phase noise at 20-MHz offset		–146.6		dBc/Hz
t_{RJIT}	Random additive jitter from 10 kHz to 20 MHz		65		fs, RMS

6.7 Typical Characteristics



Input clock RMS jitter is 32 fs from 10 kHz to 20 MHz and additive RMS jitter is 152 fs, T_A = 25°C, and V_{CC} = 2.5 V

Figure 1. 100-MHz Input and Output Phase Noise Plot

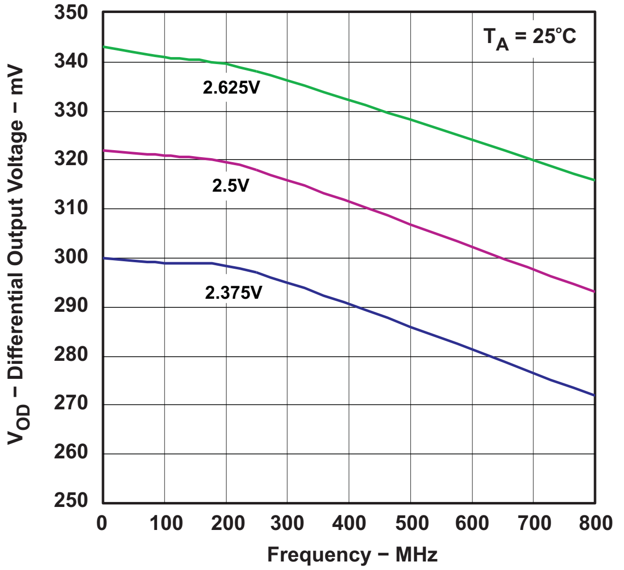


Figure 2. Differential Output Voltage vs Frequency

7 Parameter Measurement Information

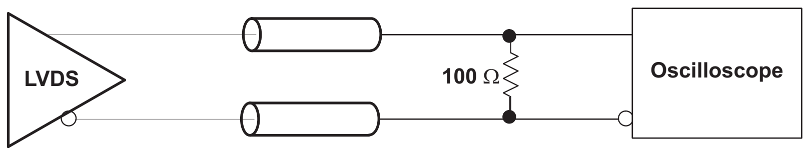


Figure 3. LVDS Output DC Configuration During Device Test

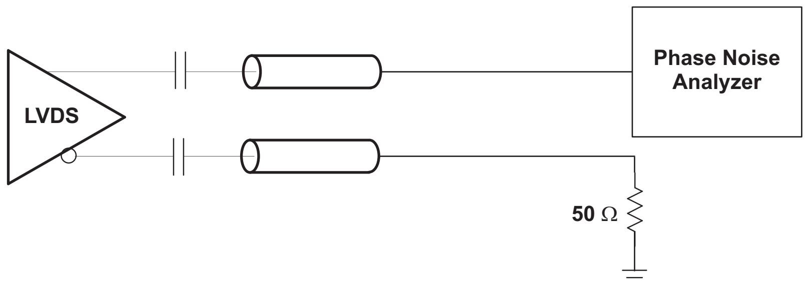


Figure 4. LVDS Output AC Configuration During Device Test

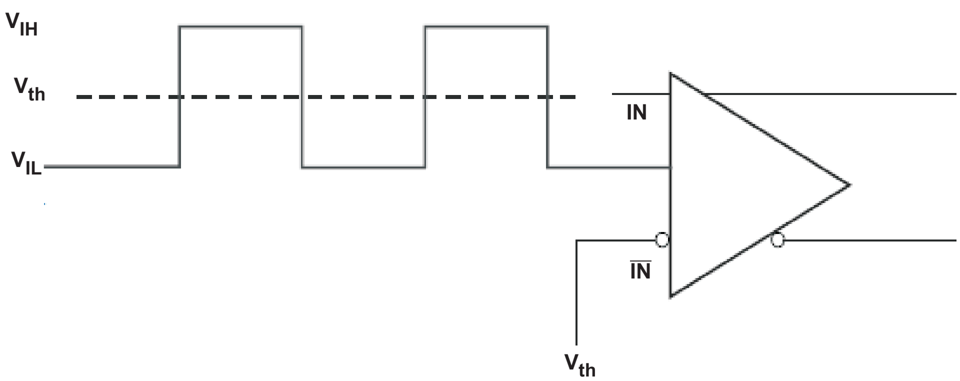


Figure 5. DC-Coupled LVCMOS Input During Device Test

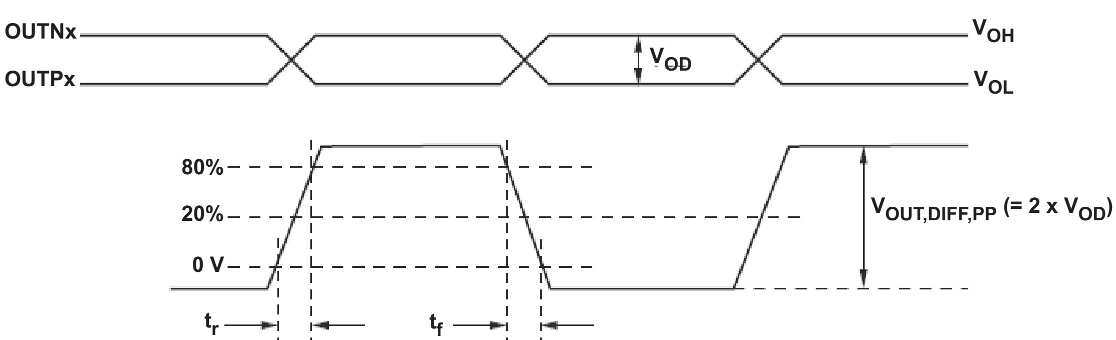
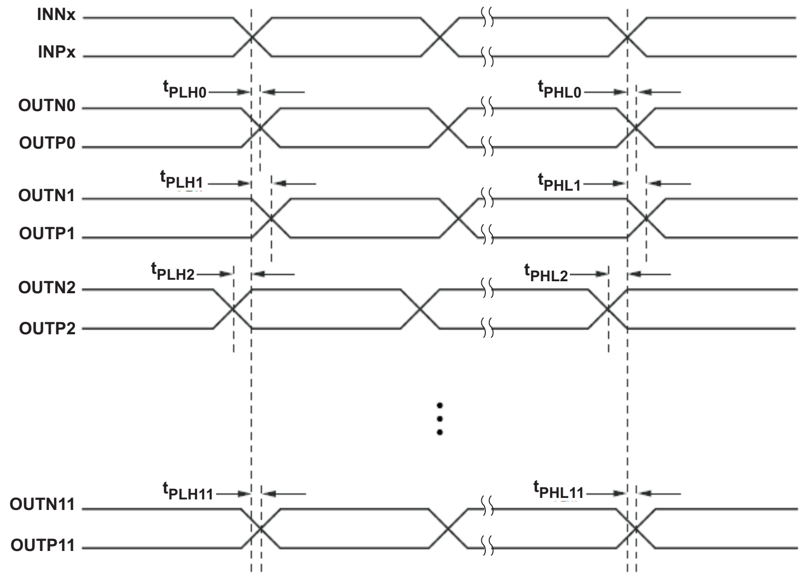


Figure 6. Output Voltage and Rise/Fall Time



A. Output skew is calculated as the greater of the following: As of the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1, 2, ..11)

B. Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} across multiple devices (n = 0, 1, 2, ..11)

Figure 7. Output Skew and Part-to-Part Skew

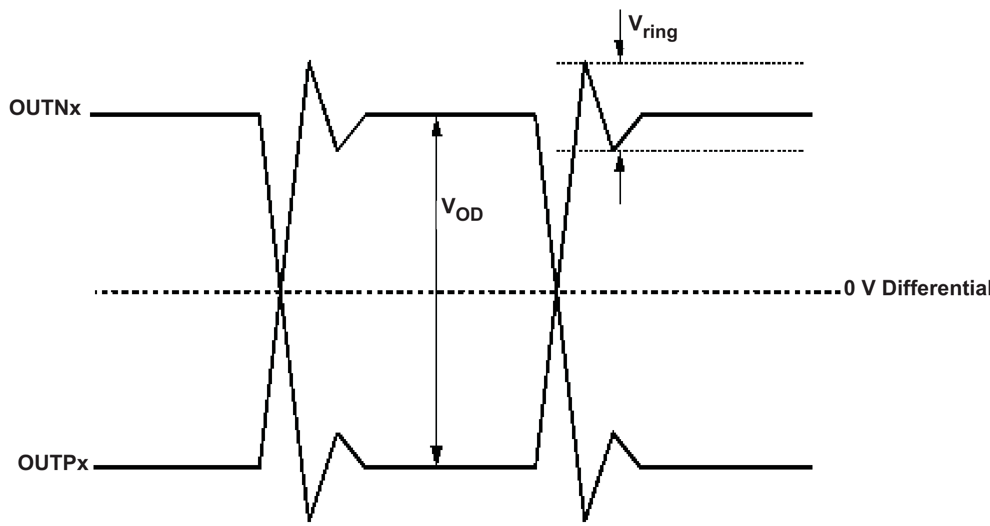


Figure 8. Output Overshoot and Undershoot

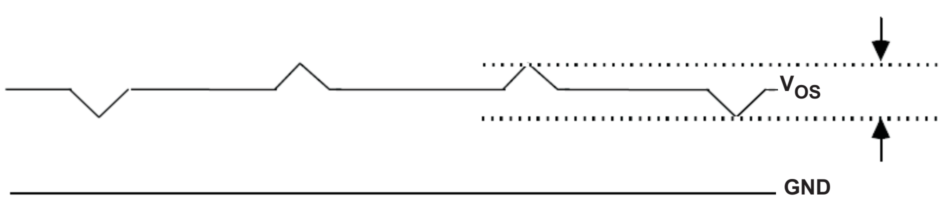


Figure 9. Output AC Common Mode

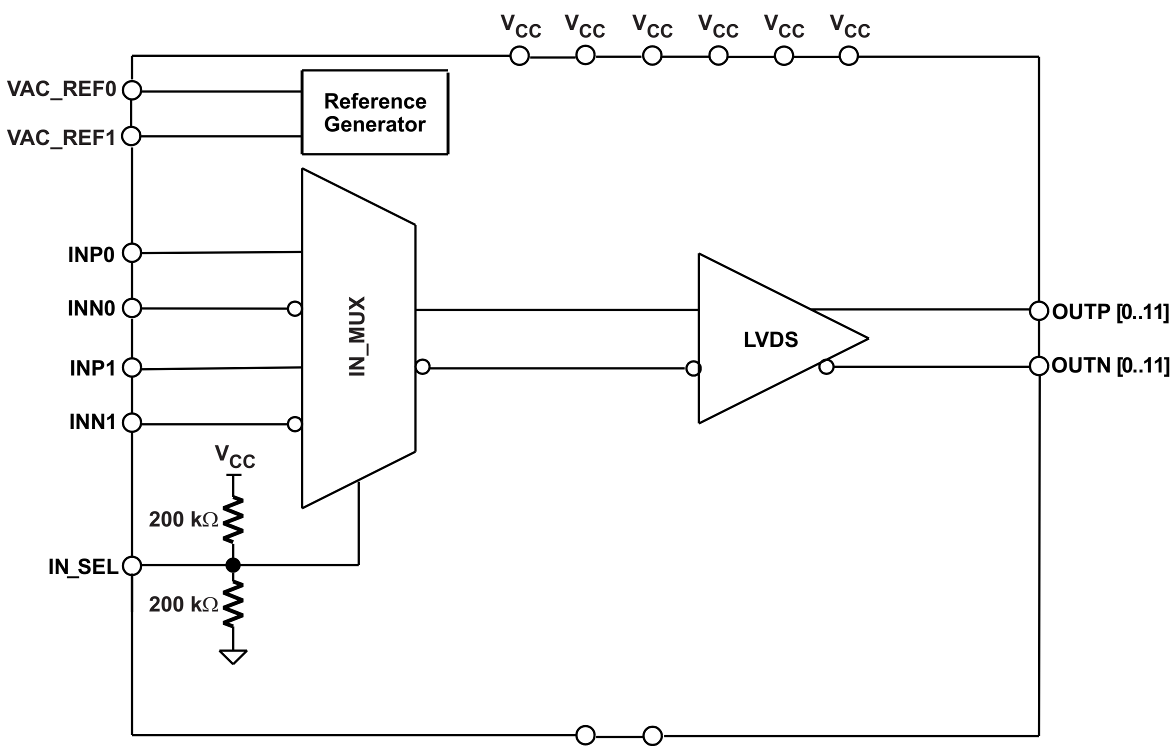
8 Detailed Description

8.1 Overview

The CDCLVD1212 LVDS drivers use CMOS transistors to control the output current. Therefore, proper biasing and termination are required to ensure correct operation of the device and to maximize signal integrity.

The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either DC-coupled termination or AC-coupled termination can be used for LVDS outputs. TI recommends placing a termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common-mode voltage of the CDCLVD1212, AC-coupling must be used. If the LVDS receiver has internal 100-Ω termination, external termination must be omitted.

8.2 Functional Block Diagram



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8.3 Feature Description

The CDCLVD1212 is a low additive jitter LVDS fan-out buffer that can generate twelve copies of two selectable LVPECL, LVDS, or LVCMOS inputs. The CDCLVD1212 can accept reference clock frequencies up to 800 MHz while providing low output skew.

8.4 Device Functional Modes

The two inputs of the CDCLVD1212 are internally muxed together and can be selected through the control pin (see Table 1). Unused inputs and outputs can be left floating to reduce overall component cost. Both AC- and DC-coupling schemes can be used with the CDCLVD1212 to provide greater system flexibility.

Table 1. Input Selection Table

IN_SEL	ACTIVE CLOCK INPUT
0	INP0, INN0
1	INP1, INN1
Open	None (1)

(1) The input buffers are disabled and the outputs are static.

8.4.1 LVDS Output Termination

Unused outputs can be left open without connecting any trace to the output pins.

The CDCLVD1212 can be connected to LVDS receiver inputs with DC- and AC-coupling as shown in Figure 10 and Figure 11 (respectively).

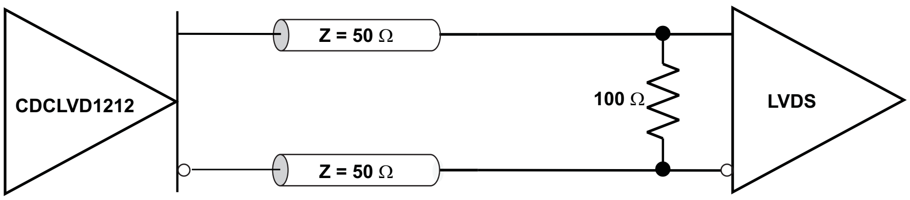


Figure 10. Output DC Termination

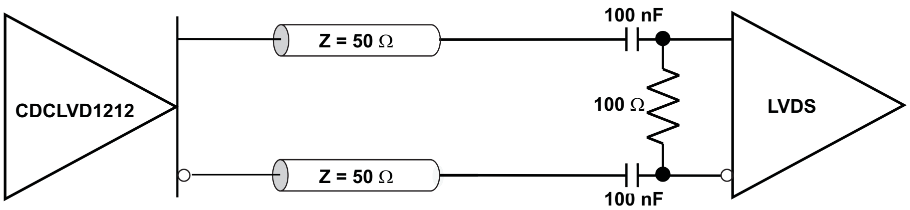


Figure 11. Output AC Termination (With the Receiver Internally Biased)

8.4.2 Input Termination

The CDCLVD1212 inputs can be interfaced with LVDS, LVPECL, or LVCMOS drivers.

LVDS drivers can be connected to CDCLVD1212 inputs with DC- or AC-coupling as shown in Figure 12 and Figure 13 (respectively).

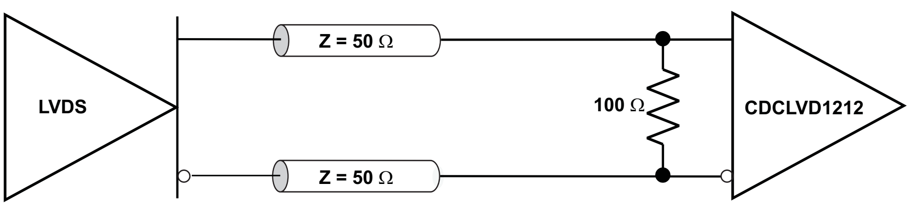


Figure 12. LVDS Clock Driver Connected to CDCLVD1212 Input (DC-Coupled)

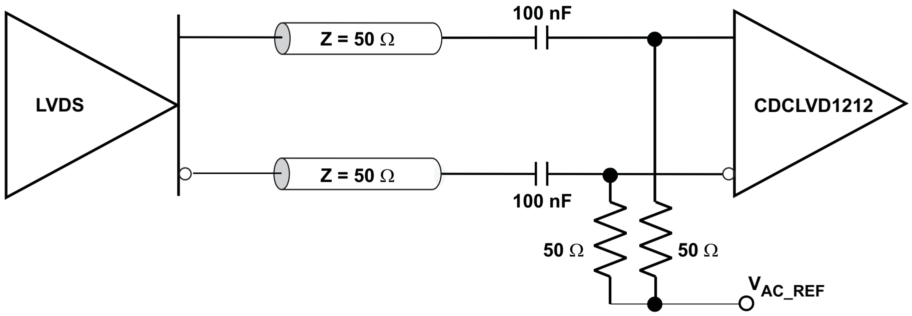


Figure 13. LVDS Clock Driver Connected to CDCLVD1212 Input (AC-Coupled)

Figure 14 shows how to connect LVPECL inputs to the CDCLVD1212. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6 V_{PP}.

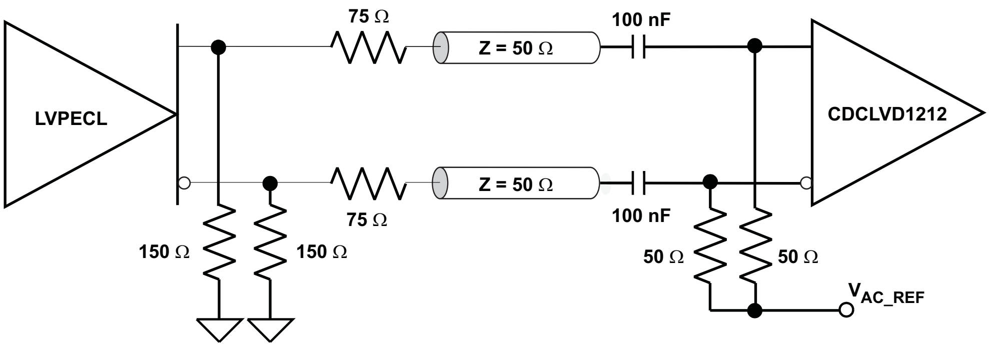


Figure 14. LVPECL Clock Driver Connected to CDCLVD1212 Input

Figure 15 illustrates how to couple a 2.5-V LVCMOS clock input to the CDCLVD1212 directly. The series resistance, R_S, must be placed close to the LVCMOS driver if required. 3.3-V LVCMOS clock input swing must be limited to $V_{IH} \le V_{CC}$.

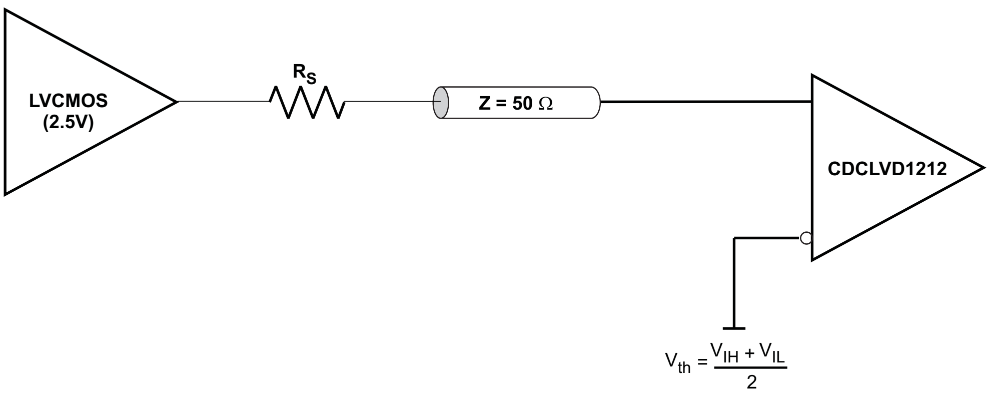


Figure 15. 2.5-V LVCMOS Clock Driver Connected to CDCLVD1212 Input

For unused input, TI recommends grounding both input pins (INP, INN) using 1-kΩ resistors.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CDCLVD1212 is a low additive jitter universal to LVDS fan-out buffer with 2 selectable inputs. The small package, low output skew, and low additive jitter make for a flexible device in demanding applications.

9.2 Typical Application

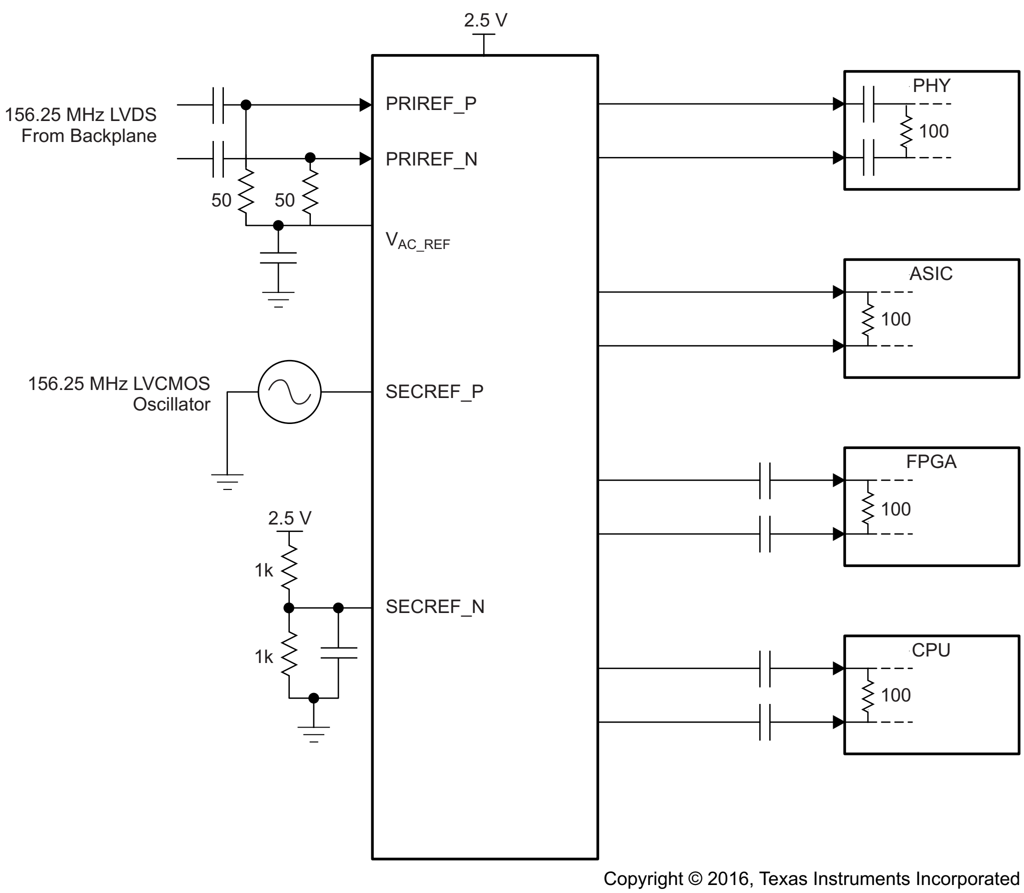


Figure 16. Fan-Out Buffer for Line Card Application

Typical Application (continued)

9.2.1 Design Requirements

The CDCLVD1212 shown in Figure 16 is configured to select two inputs: a 156.25-MHz LVDS clock from the backplane, or a secondary 156.25-MHz LVCMOS 2.5-V oscillator. The LVDS clock is AC-coupled and biased using the integrated reference voltage generator. A resistor divider is used to set the threshold voltage correctly for the LVCMOS clock. 0.1-µF capacitors are used to reduce noise on both V_{AC_REF} and SECREF_N. Either input signal can be then fanned out to desired devices, as shown. The configuration example is driving 4 LVDS receivers in a line card application with the following properties:

- The PHY device is capable of DC-coupling with an LVDS driver such as the CDCLVD1212. This PHY device features internal termination so no additional components are required for proper operation.
- The ASIC LVDS receiver features internal termination and operates at the same common-mode voltage as the CDCLVD1212. Again, no additional components are required.
- The FPGA requires external AC-coupling, but has internal termination. 0.1-µF capacitors are placed to provide AC-coupling. Similarly, the CPU is internally terminated, and requires only external AC-coupling capacitors.
- The unused outputs of the CDCLVD1212 are left floating.

9.2.2 Detailed Design Procedure

See *Input Termination* for proper input terminations, dependent on single-ended or differential inputs.

See *LVDS Output Termination* for output termination schemes depending on the receiver application.

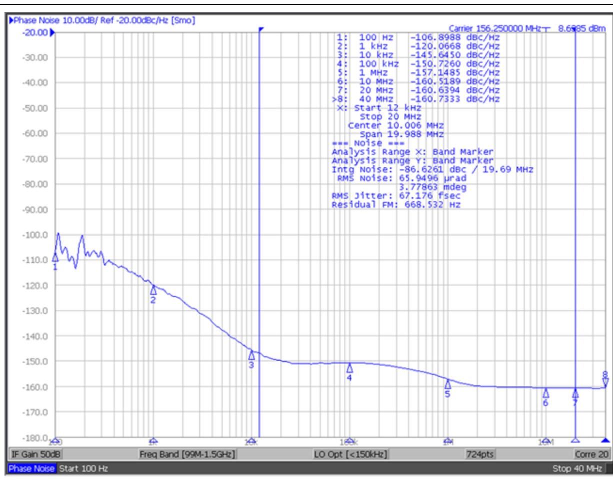
Unused outputs can be left floating.

In this example, the PHY, ASIC, and FPGA or CPU require different schemes. Power supply filtering and bypassing is critical for low-noise applications.

See *Power Supply Recommendations* for recommended filtering techniques. A reference layout is provided in *Low-Additive Jitter, Twelve LVDS Outputs Clock Buffer Evaluation Board* (SCAU045).

9.2.3 Application Curves

The CDCLVD12xx's low additive noise is shown in this line card application. The low noise 156.25-MHz source with 67-fs RMS jitter drives the CDCLVD12xx, resulting in 80-fs RMS when integrated from 12 kHz to 20 MHz. The resultant additive jitter is a low 44-fs RMS for this configuration.



Reference signal is low-noise Rohde & Schwarz SMA100A

Figure 17. CDCLVD12xx Reference Phase Noise, 67-fs RMS (12 kHz to 20 MHz)

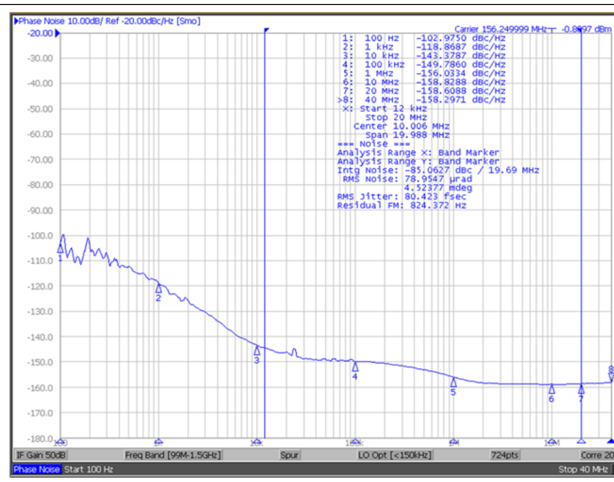


Figure 18. CDCLVD12xx Output Phase Noise, 80-fs RMS (12 kHz to 20 MHz)

10 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1 µF) bypass capacitors as there are supply pins in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low DC-resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

Figure 19 shows this recommended power-supply decoupling method.

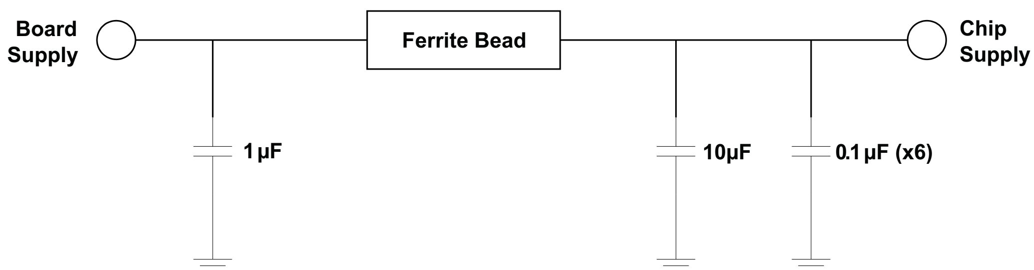


Figure 19. Power Supply Decoupling

11 Layout

11.1 Layout Guidelines

For reliability and performance reasons, the die temperature must be limited to a maximum of 125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed-circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. Figure 20 shows a recommended land and via pattern.

11.2 Layout Example

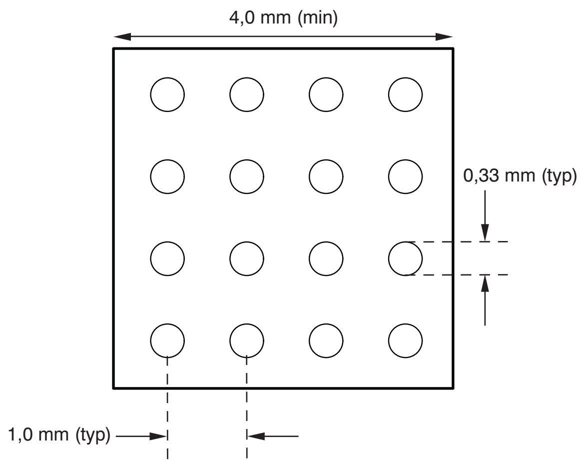


Figure 20. Recommended PCB Layout

11.3 Thermal Considerations

The CDCLVD1212 supports high temperatures on the printed-circuit board (PCB) measured at the thermal pad. The system designer must ensure that the maximum junction temperature is not exceeded. Ψ_{JB} can allow the system designer to measure the board temperature with a fine gauge thermocouple and back calculate the junction temperature using Equation 1. Note that Ψ_{JB} is close to $R_{\theta JB}$ as 75% to 95% of a device's heat is dissipated by the PCB.

$$T_J = T_{PCB} + (\Psi_{JB} \times Power) \quad (1)$$

Example:

Calculation of the junction-lead temperature with a 4-layer JEDEC test board using four thermal vias:

T_{PCB} = 105°C

Ψ_{JB} = 9.3°C/W

$Power_{inclTerm} = I_{max} \times V_{max}$ = 146 mA × 2.625 V = 383 mW (maximum power consumption including termination resistors)

$Power_{exclTerm}$ = 359 mW (maximum power consumption excluding termination resistors, see *Power Consumption of LVPECL and LVDS* (SLYT127) for further details)

$\Delta T_J = \Psi_{JB} \times Power_{exclTerm}$ = 9.3°C/W × 359 mW = 3.34°C

$T_J = \Delta T_J + T_{Chassis}$ = 3.34°C + 105°C = 108.34°C (maximum junction temperature of 125°C is not violated)

Further information can be found at *Semiconductor and IC Package Thermal Metrics* (SPRA953) and *Using Thermal Calculation Tools for Analog Components* (SLUA566).

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Low-Additive Jitter, Twelve LVDS Outputs Clock Buffer Evaluation Board* (SCAU045)
- *Power Consumption of LVPECL and LVDS* (SLYT127)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Using Thermal Calculation Tools for Analog Components* (SLUA566)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCLVD1212RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCLVD 1212	Samples
CDCLVD1212RHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCLVD 1212	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

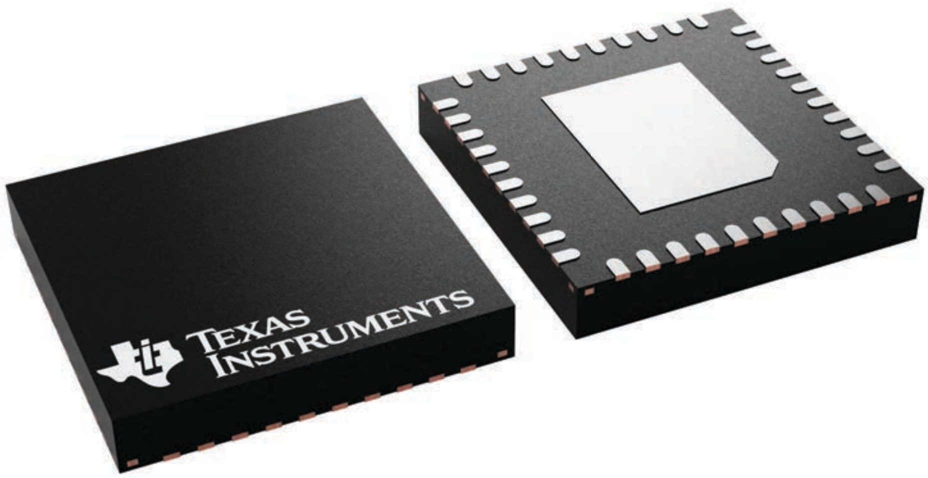
RHA 40

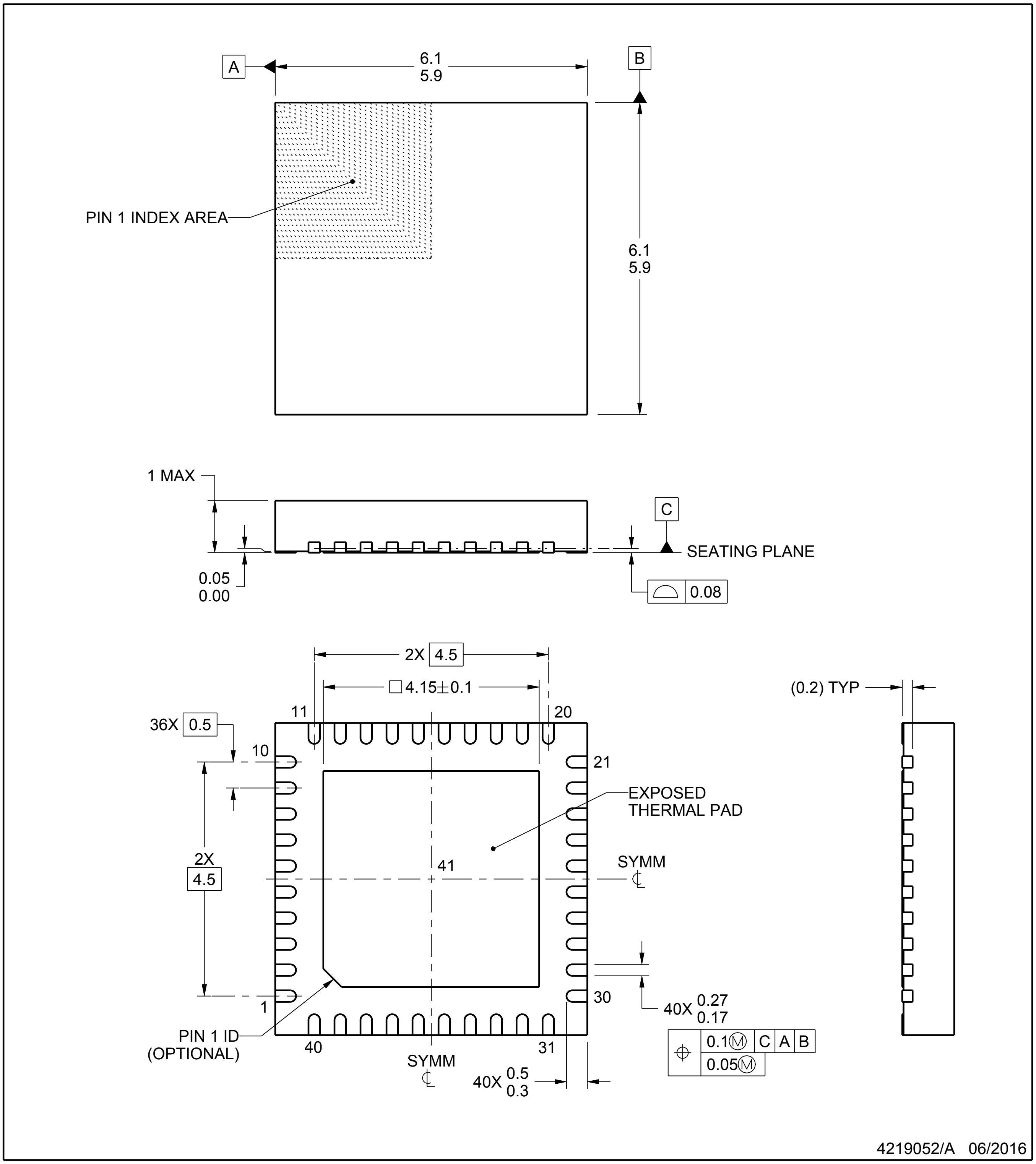
VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

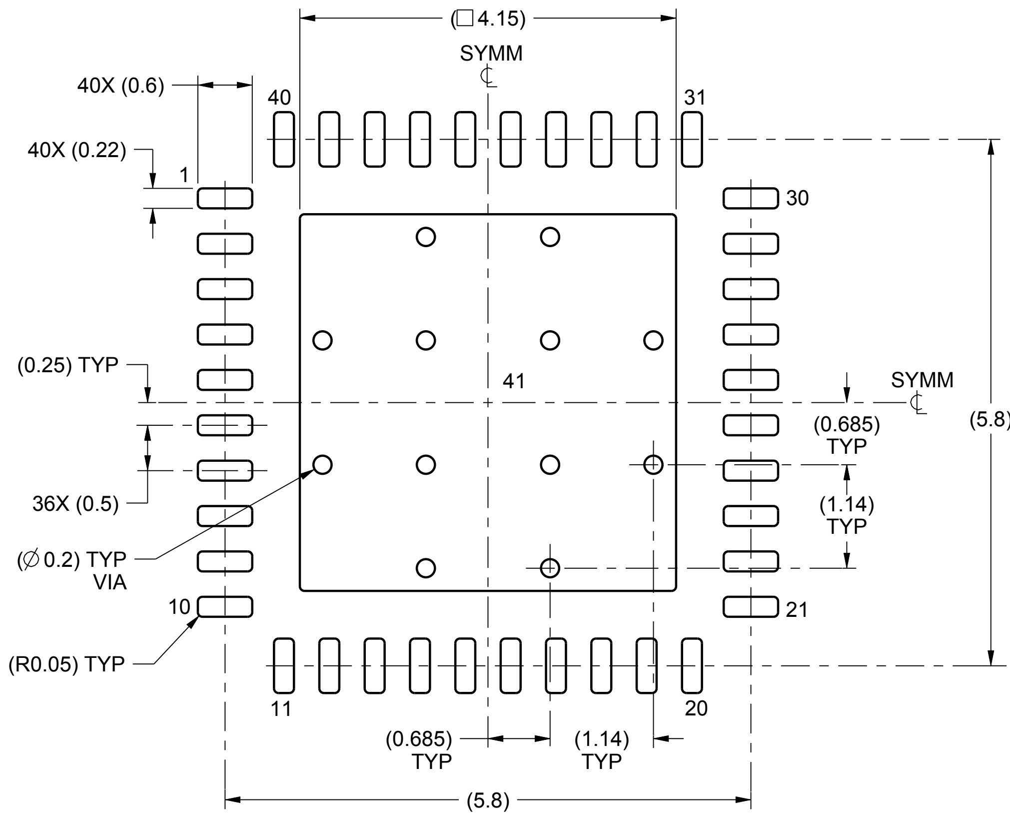
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



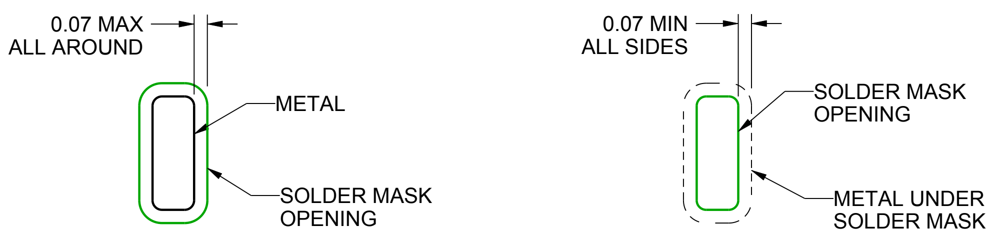


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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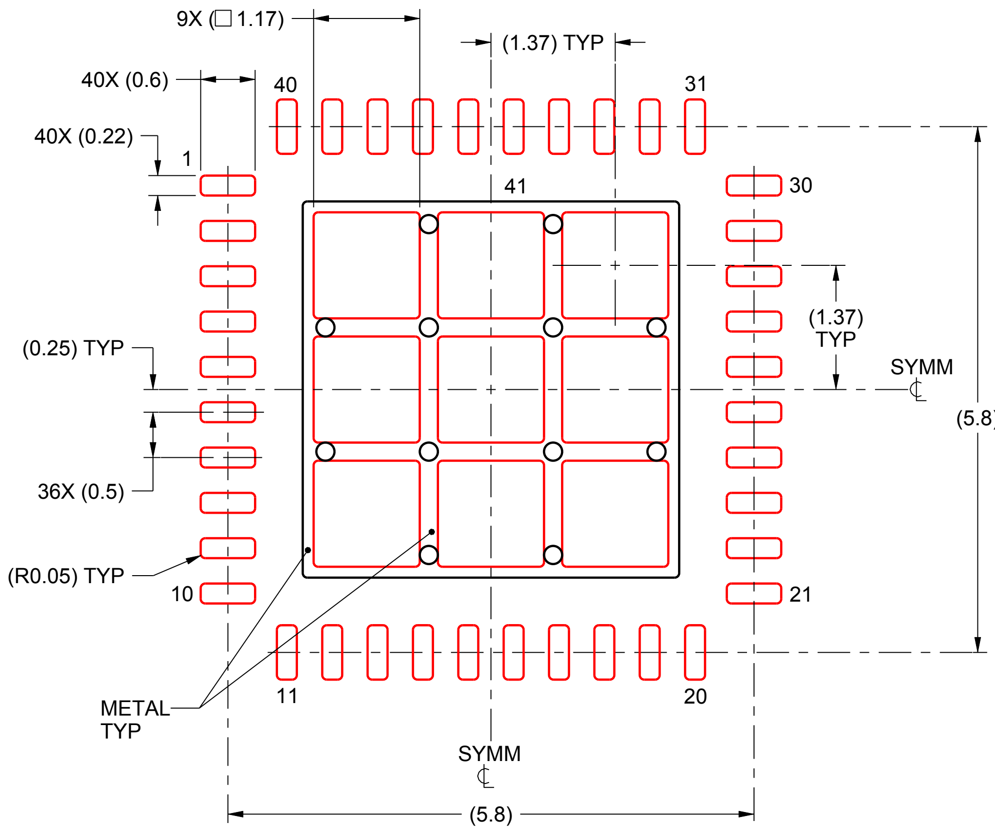
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4219052/A 06/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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