

CSD18510KCS 40V N 通道 NexFET™ 功率 MOSFET

1 特性

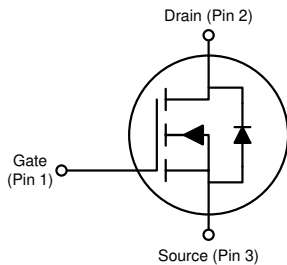
- 低 Q_g 和 Q_{gd}
- 低 $R_{DS(on)}$
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 RoHS
- 无卤素
- TO-220 塑料封装

2 应用

- 次级侧同步整流器
- 电机控制

3 说明

这款 40V、1.4mΩ、TO-220 NexFET™ 功率 MOSFET 旨在用于更大限度地降低功率转换应用中的损耗。



产品概要

| $T_A = 25^\circ\text{C}$ | | 典型值 | | 单位 |
|--------------------------|--------------|------------------------|-----|----|
| V_{DS} | 漏源电压 | 40 | | V |
| Q_g | 栅极电荷总量 (10V) | 118 | | nC |
| Q_{gd} | 栅极电荷 (栅极到漏极) | 21 | | nC |
| $R_{DS(on)}$ | 漏源导通电阻 | $V_{GS} = 4.5\text{V}$ | 2.0 | mΩ |
| | | $V_{GS} = 10\text{V}$ | 1.4 | |
| $V_{GS(th)}$ | 阈值电压 | 1.7 | | V |

器件信息(1)

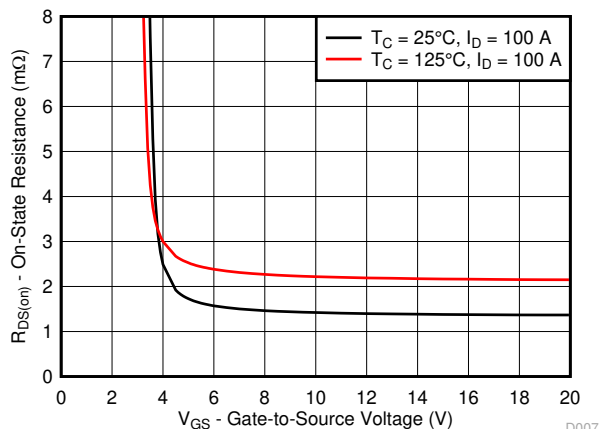
| 器件 | 介质 | 数量 | 封装 | 配送 |
|-------------|----|----|-------------|----|
| CSD18510KCS | 管 | 50 | TO-220 塑料封装 | 管 |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

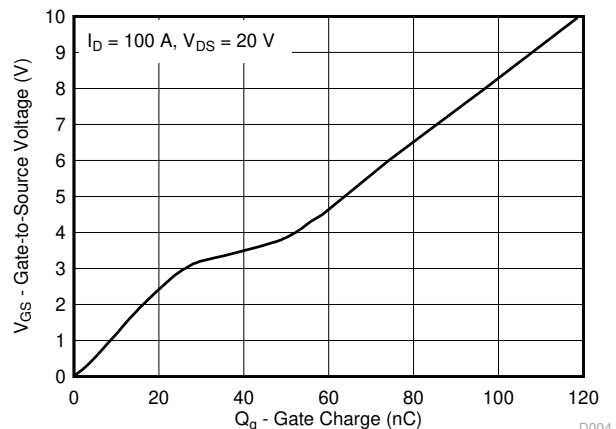
绝对最大额定值

| $T_A = 25^\circ\text{C}$ | | 值 | 单位 |
|--------------------------|---|-----------|----|
| V_{DS} | 漏源电压 | 40 | V |
| V_{GS} | 栅源电压 | ±20 | V |
| I_D | 持续漏极电流 (受封装限制) | 200 | A |
| | 持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得 | 288 | |
| | 持续漏极电流 (受芯片限制), $T_C = 100^\circ\text{C}$ 时测得 | 204 | |
| I_{DM} | 脉冲漏极电流(1) | 400 | A |
| P_D | 功率耗散 | 250 | W |
| T_J 、 T_{stg} | 工作结温、贮存温度 | -55 至 175 | °C |
| E_{AS} | 雪崩能量, 单脉冲 $I_D = 81\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$ | 328 | mJ |

(1) 最大 $R_{\theta JC} = 0.6^\circ\text{C/W}$, 脉冲持续时间 $\leq 100 \mu\text{s}$, 占空比 $\leq 1\%$ 。



$R_{DS(on)}$ 与 V_{GS} 之间的关系



栅极电荷



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision A (July 2017) to Revision B (November 2022) | Page |
|--|-------------|
| • Updated 图 5-3 | 4 |

| Changes from Revision * (March 2017) to Revision A (July 2017) | Page |
|---|-------------|
| • 更正了节 1 部分中的封装类型错误..... | 1 |

5 Specifications

5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|----------------------------------|--|---|------|-------|---------------|
| STATIC CHARACTERISTICS | | | | | | |
| BV_{DSS} | Drain-to-source voltage | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 40 | | | V |
| I_{DSS} | Drain-to-source leakage current | $V_{GS} = 0\text{ V}, V_{DS} = 32\text{ V}$ | | | 1 | μA |
| I_{GSS} | Gate-to-source leakage current | $V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$ | | | 100 | nA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ | 1.4 | 1.7 | 2.3 | V |
| $R_{DS(on)}$ | Drain-to-source on-resistance | $V_{GS} = 4.5\text{ V}, I_D = 100\text{ A}$ | | 2.0 | 2.6 | m Ω |
| | | $V_{GS} = 10\text{ V}, I_D = 100\text{ A}$ | | 1.4 | 1.7 | |
| g_{fs} | Transconductance | $V_{DS} = 4\text{ V}, I_D = 100\text{ A}$ | | 330 | | S |
| DYNAMIC CHARACTERISTICS | | | | | | |
| C_{iss} | Input capacitance | $V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}, f = 1\text{ MHz}$ | | 8770 | 11400 | pF |
| C_{oss} | Output capacitance | | | 832 | 1080 | pF |
| C_{riss} | Reverse transfer capacitance | | | 424 | 551 | pF |
| R_G | Series gate resistance | | | 0.9 | 1.8 | Ω |
| Q_g | Gate charge total (4.5 V) | $V_{DS} = 20\text{ V}, I_D = 100\text{ A}$ | | 58 | 75 | nC |
| Q_g | Gate charge total (10 V) | | | 118 | 153 | nC |
| Q_{gd} | Gate charge gate-to-drain | | | 21 | | nC |
| Q_{gs} | Gate charge gate-to-source | | | 28 | | nC |
| $Q_{g(th)}$ | Gate charge at V_{th} | | | 15 | | nC |
| Q_{oss} | Output charge | | $V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$ | | 35 | |
| $t_{d(on)}$ | Turnon delay time | $V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 100\text{ A}, R_G = 0\ \Omega$ | | 10 | | ns |
| t_r | Rise time | | | 8 | | ns |
| $t_{d(off)}$ | Turnoff delay time | | | 29 | | ns |
| t_f | Fall time | | | 8 | | ns |
| DIODE CHARACTERISTICS | | | | | | |
| V_{SD} | Diode forward voltage | $I_{SD} = 100\text{ A}, V_{GS} = 0\text{ V}$ | | 0.85 | 1.0 | V |
| Q_{rr} | Reverse recovery charge | $V_{DS} = 20\text{ V}, I_F = 100\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$ | | 70 | | nC |
| t_{rr} | Reverse recovery time | | | 41 | | ns |

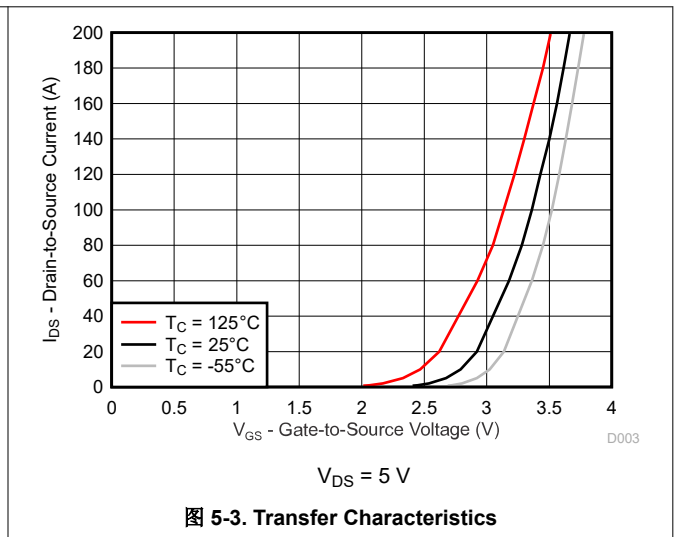
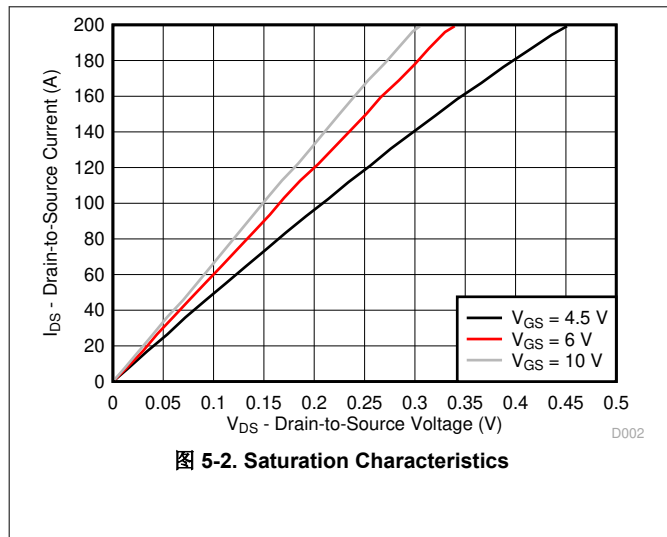
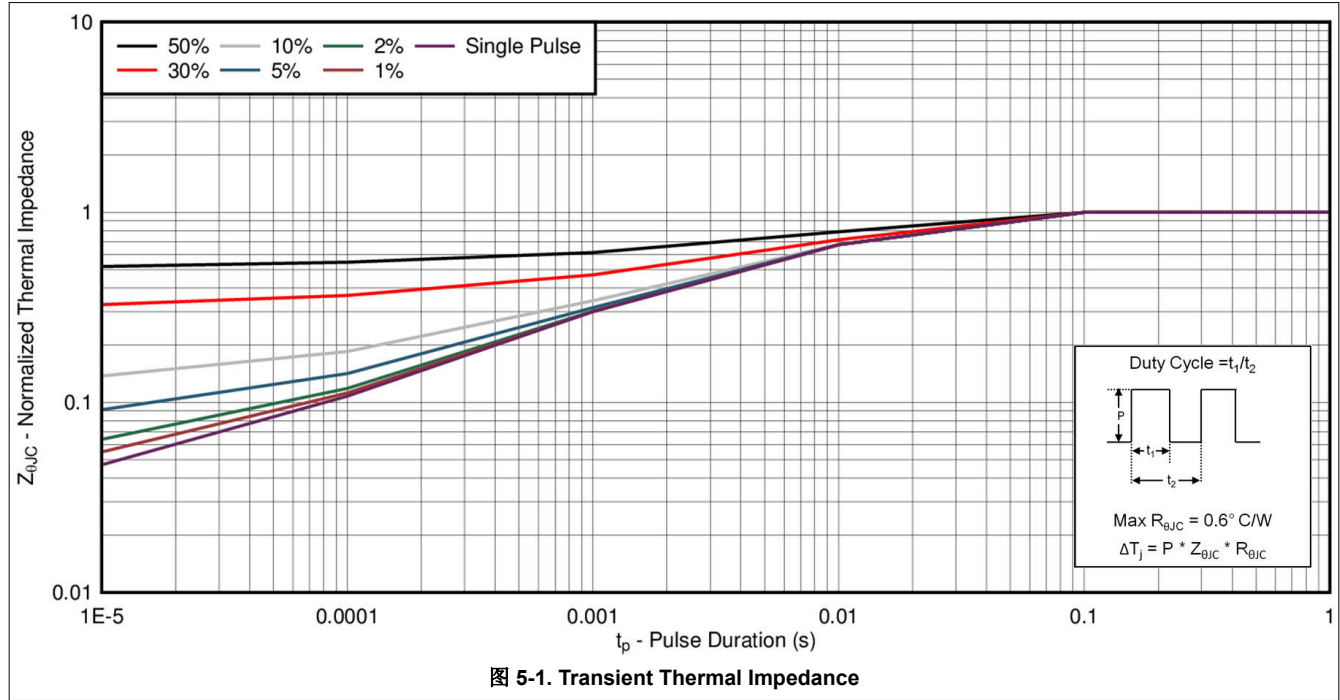
5.2 Thermal Information

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|-----------------|--|-----|-----|-----|---------------------------|
| $R_{\theta JC}$ | Junction-to-case thermal resistance | | | 0.6 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | | | 62 | $^\circ\text{C}/\text{W}$ |

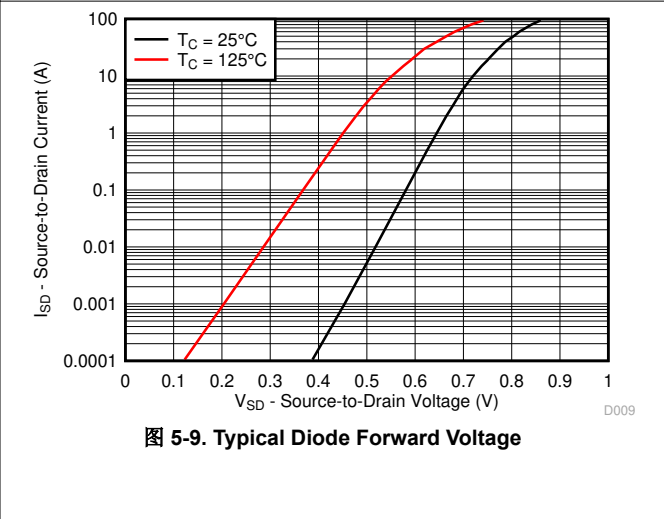
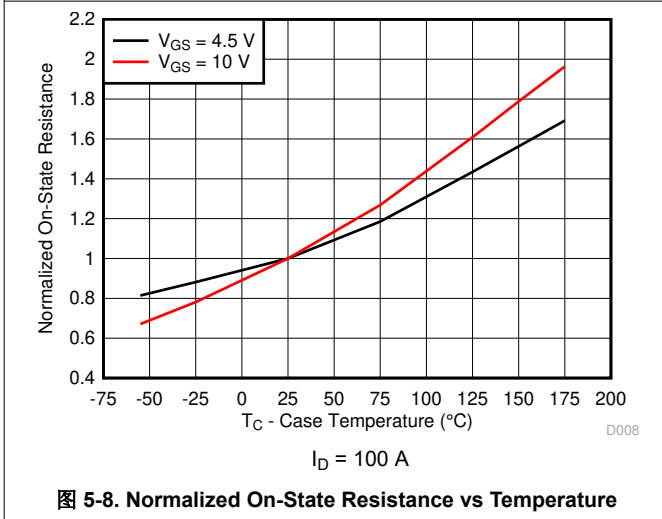
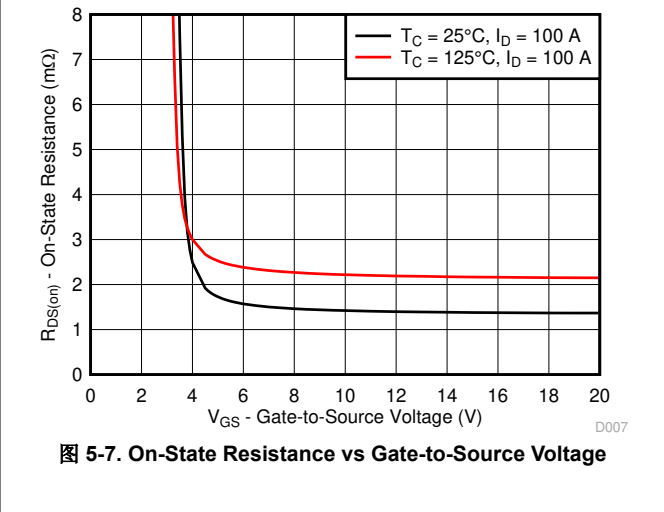
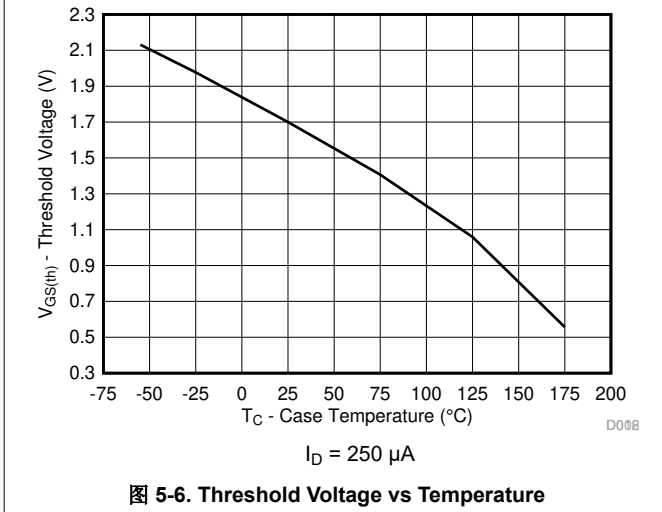
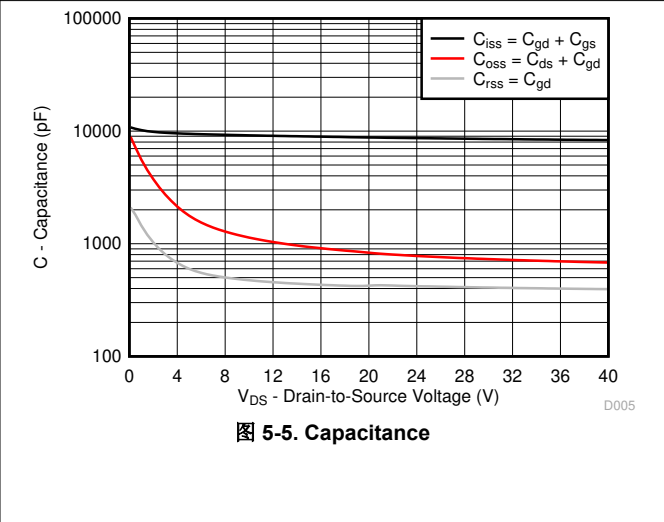
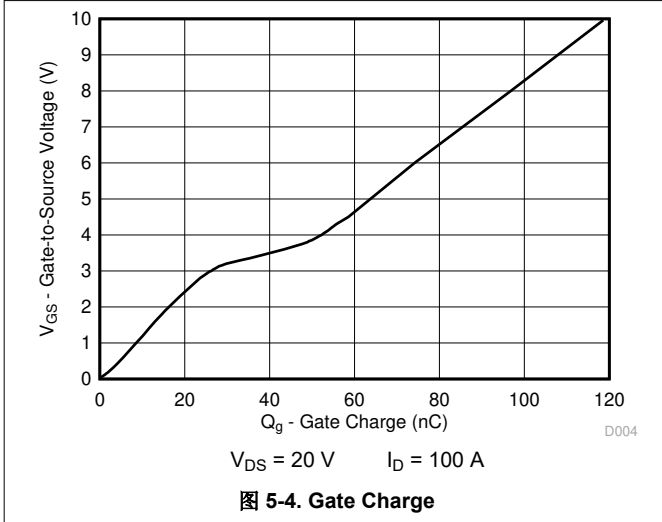
5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)



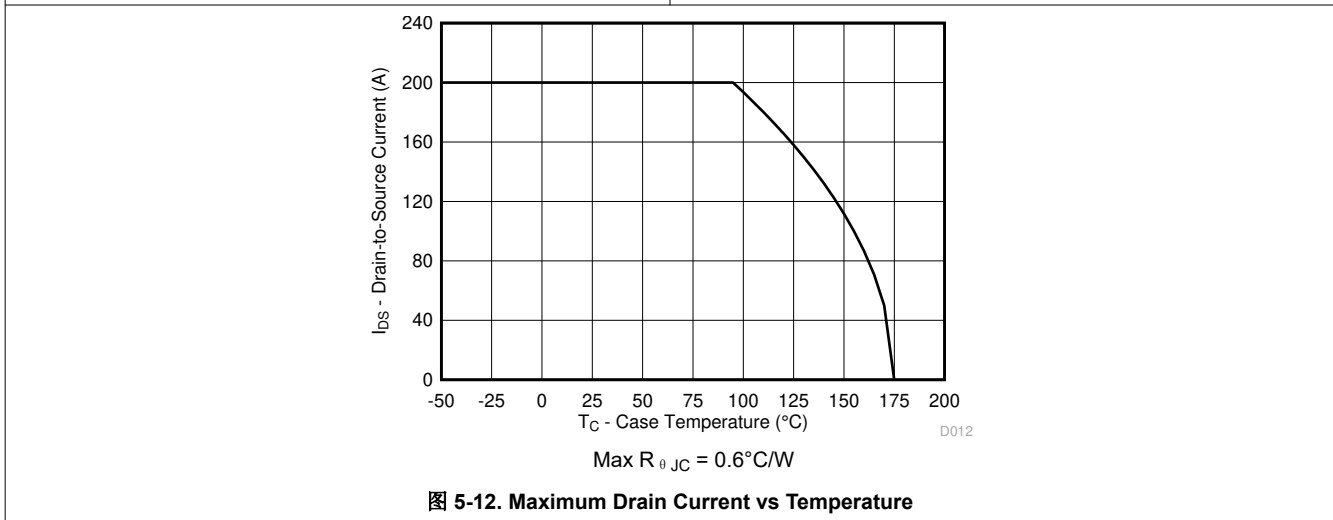
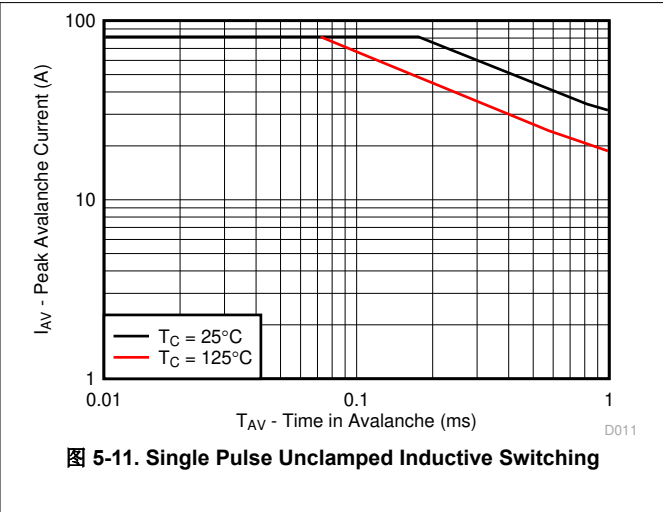
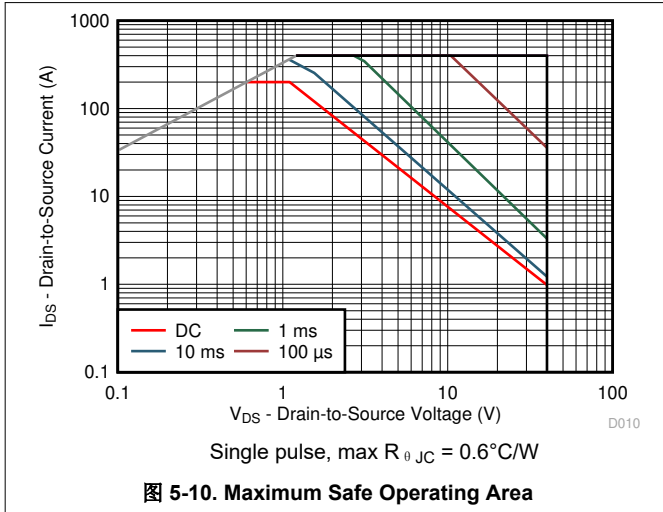
5.3 Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)



5.3 Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)



6 Device and Documentation Support

6.1 接收文档更新通知

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[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

6.3 Trademarks

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6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

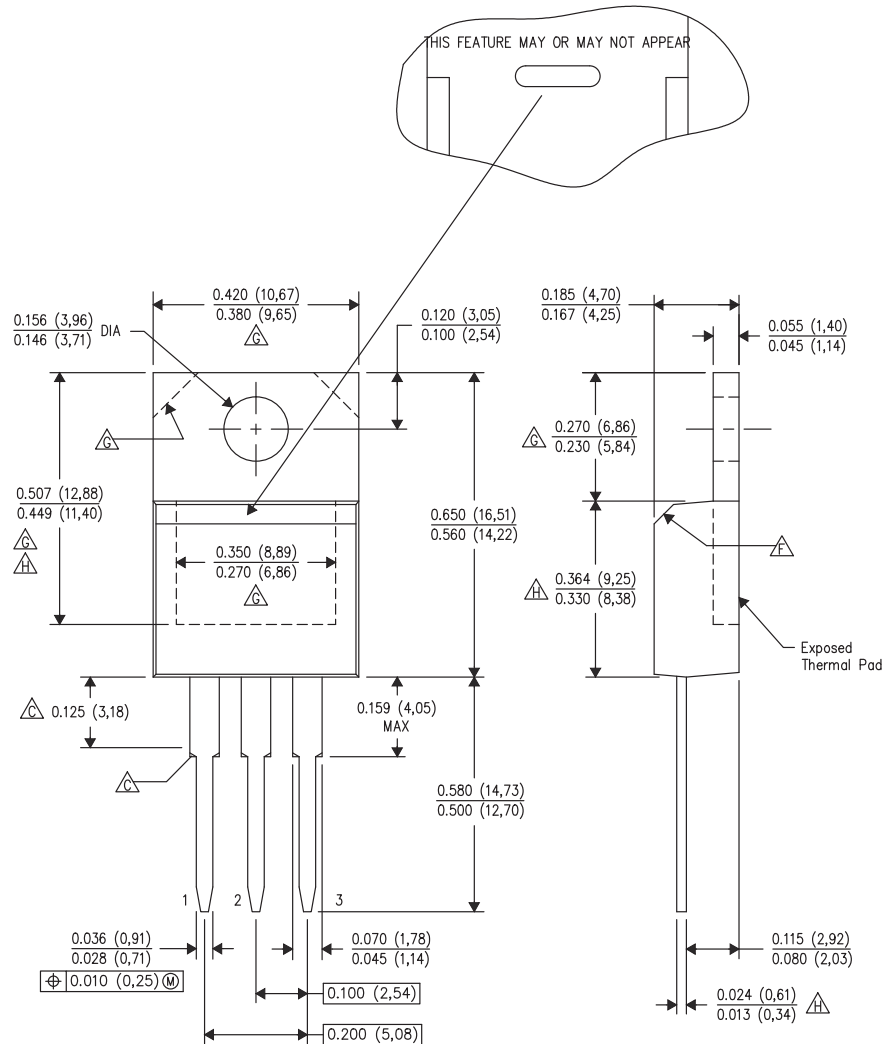
6.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KCS Package Dimensions



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Lead dimensions are not controlled within this area. Chamfer may or may not appear.
 - D. All lead dimensions apply before solder dip.
 - E. The center lead is in electrical contact with the mounting tab.
 - F. The chamfer is optional.
 - G. Thermal pad contour optional within these dimensions.
 - H. Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

表 7-1. Pin Configuration

| POSITION | DESIGNATION |
|-------------|-------------|
| Pin 1 | Gate |
| Pin 2 / Tab | Drain |
| Pin 3 | Source |

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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| CSD18510KCS | ACTIVE | TO-220 | KCS | 3 | 50 | RoHS-Exempt & Green | SN | N / A for Pkg Type | -55 to 175 | CSD18510KCS | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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[SQD23N06-31L-GE3](#) [TK16J60W,S1VQ\(O](#) [2SK2614\(TE16L1,Q\)](#) [DMN1017UCP3-7](#) [EFC2J004NUZTDG](#) [DMN1053UCP4-7](#) [SQJ469EP-](#)
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[TSM60NB380CP](#) [ROG](#) [RQ7L055BGTCR](#) [DMNH15H110SK3-13](#) [SLF10N65ABV2](#)