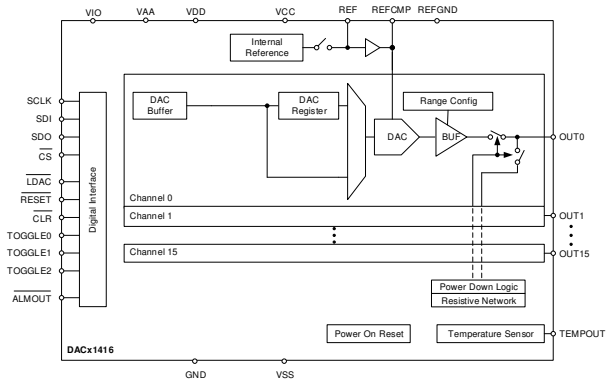
具有内部基准电压的 DACx1416 16 通道 16 位、14 位和 12 位高电压输出 DAC

1 特性

- 高性能
  - 在 16 位分辨率下具有单调性
  - INL：16 位分辨率下为 ±1LSB（最大值）
  - TUE：FSR 最大值的 ±0.1%
- 集成 2.5V 精密内部基准
  - 初始精度：±2.5 mV（最大值）
  - 低漂移：5ppm/°C（典型值）
- 灵活的输出配置
  - 输出范围：±2.5V、±5V、±10V、±20V
    0 至 5V、0 至 10V、0 至 20V、0 至 40V
  - 差分输出模式
- 高驱动能力：±25mA，相对于电源轨的摆幅为 1.5V
- 三个专用 A-B 切换引脚可用于生成抖动信号
- 模拟温度输出
  - -4 mV/°C 的传感器增益
- 50MHz SPI 兼容型串行接口
  - 4 线制模式，工作电压为 1.7V 至 5.5V
  - 菊花链运行方式
  - CRC 误差校验
- 温度范围：–40°C 至 +125°C
- 小封装
  - 6mm × 6mm，40 引脚 VQFN

2 应用

- 数据中心内部互联（长距离、水下）
- 数据中心间互联（地铁）
- 光学模块
- 半导体测试
- 实验室和现场仪表
- 数据采集 (DAQ)



功能方框图

3 说明

DAC81416、DAC71416 和 DAC61416 (DACx1416) 是具有引脚兼容性和 16 位、14 位、12 位分辨率的 16 通道缓冲高电压输出数模转换器 (DAC) 系列产品。DACx1416 包括一个低漂移 2.5V 内部电压基准，因此在大多数应用中无需使用外部精密基准。这些器件具有单调性，并能提供 ±1LSB INL 的高线性度。

用户可自行选择输出配置，包括满量程双极输出电压 ±20V、±10V、±5V 或 ±2.5V，以及满量程单极输出电压 40V、20V、10V 和 5V。而且，每个 DAC 通道的满量程输出范围都是独立可编程的。集成的 DAC 输出缓冲器可实现高达 25 mA 的灌电流或拉电流，从而减少了对额外的运算放大器的需求。每个通道对都可进行相应配置，从而提供经过失调校准的差分输出。通过三个专用 A-B 切换引脚，可以生成最多具有三种频率的抖动信号。

DACx1416 包含的上电复位电路可在上电时将 DAC 输出端连接至接地端。输出端会保持该状态，直至器件寄存器得到适当的运行配置。

与 DACx1416 之间的通信通过一个支持 1.7V 至 5.5V 工作电压的 4 线制串行接口进行。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
DAC81416	VQFN (40)	6.00mm × 6.00mm
DAC71416		
DAC61416		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (November 2018) to Revision B (June 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 为清晰起见，更改了格式和小的编辑问题	1

Changes from Revision * (July 2018) to Revision A (November 2018)	Page
• 将 DAC81416 从“预告信息”更改为“量产数据”	1
• 将 DAC71416 和 DAC61416 从“产品预发布”更改为“量产数据”	1

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5 Device Comparison Table

DEVICE	RESOLUTION
DAC81416	16-bit
DAC71416	14-bit
DAC61416	12-bit

6 Pin Configuration and Functions

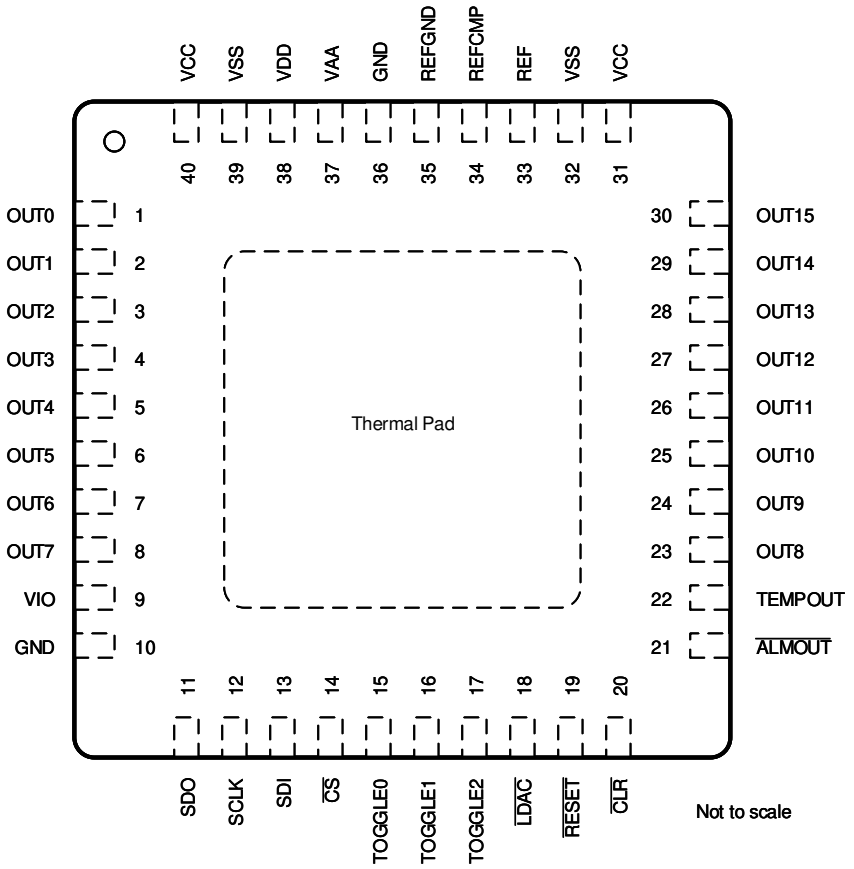

图 6-1. RHA Package, 40-Pin VQFN, Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT0	Output	Channel 0 analog DAC output voltage.
2	OUT1	Output	Channel 1 analog DAC output voltage.
3	OUT2	Output	Channel 2 analog DAC output voltage.
4	OUT3	Output	Channel 3 analog DAC output voltage.
5	OUT4	Output	Channel 4 analog DAC output voltage.
6	OUT5	Output	Channel 5 analog DAC output voltage.
7	OUT6	Output	Channel 6 analog DAC output voltage.
8	OUT7	Output	Channel 7 analog DAC output voltage.
9	VIO	Power	IO supply voltage. (1.7 V to 5.5 V). This pin sets the I/O operating voltage for the device.
10, 36	GND	Ground	Ground reference point for all circuitry on the device.
11	SDO	Output	Serial interface data output. The SDO pin must be enabled before operation by setting the SDO-EN bit. Data are clocked out of the input shift register on either rising or falling edges of the SCLK pin as specified by the FSDO bit (rising edge by default).

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表 6-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
12	SCLK	Input	Serial interface clock.
13	SDI	Input	Serial interface data input. Data are clocked into the input shift register on each falling edge of the SCLK pin.
14	$\overline{CS}$	Input	Active low serial data enable. This input is the frame synchronization signal for the serial data. When the signal goes low, it enables the serial interface input shift register.
15	TOGGLE0	Input	Toggle pin 0. Control signal for those DAC outputs configured for toggle operation to switch between the two DAC data registers associated with each DAC. A logic low updates the DAC output to the value set by Register A. A logic high updates the DAC output to the value set by Register B. Connect the TOGGLE0 pin to ground if unused.
16	TOGGLE1	Input	Toggle pin 1. Control signal for those DAC outputs configured for toggle operation to switch between the two DAC data registers associated with each DAC. A logic low updates the DAC output to the value set by Register A. A logic high updates the DAC output to the value set by Register B. Connect the TOGGLE1 pin to ground if unused.
17	TOGGLE2	Input	Toggle pin 2. Control signal for those DAC outputs configured for toggle operation to switch between the two DAC data registers associated with each DAC. A logic low updates the DAC output to the value set by Register A. A logic high updates the DAC output to the value set by Register B. Connect the TOGGLE2 pin to ground if unused.
18	$\overline{LDAC}$	Input	Active low synchronization signal. When the $\overline{LDAC}$ pin is low, the DAC outputs of those channels configured in synchronous mode are updated simultaneously. Connect to VIO if unused.
19	$\overline{RESET}$	Input	Active low reset input. Logic low on this pin causes the device to issue a power-on-reset event.
20	$\overline{CLR}$	Input	Active low clear input. Logic low on this pin clears all DAC outputs to their clear code. Connect to VIO if unused.
21	$\overline{ALMOUT}$	Output	$\overline{ALMOUT}$ is an open drain alarm output. An external 10-kΩ pull-up resistor to a voltage no higher than V_{IO} is required.
22	TEMPOUT	Output	Analog temperature monitor output.
23	OUT8	Output	Channel 8 analog DAC output voltage.
24	OUT9	Output	Channel 9 analog DAC output voltage.
25	OUT10	Output	Channel 10 analog DAC output voltage.
26	OUT11	Output	Channel 11 analog DAC output voltage.
27	OUT12	Output	Channel 12 analog DAC output voltage.
28	OUT13	Output	Channel 13 analog DAC output voltage.
29	OUT14	Output	Channel 14 analog DAC output voltage.
30	OUT15	Output	Channel 15 analog DAC output voltage.
31, 40	VCC	Power	Output positive analog power supply (9 V to 41.5 V).
32, 39	VSS	Power	Output negative analog power supply (– 21.5 V to 0 V).
33	REF	Input/Output	Reference input to the device when operating with external reference. When using internal reference, this is the reference output voltage pin. Connect a 150-nF capacitor to ground.
34	REFCMP	Input/Output	Reference compensation capacitor connection. Connect a 330-pF capacitor between REFCMP and REFGND.
35	REFGND	Ground	Ground reference point for the internal reference.
37	VAA	Power	Analog supply voltage (4.5 V to 5.5 V). This pin must be at the same potential as the VDD pin.
38	VDD	Power	Digital supply voltage (4.5 V to 5.5 V). This pin must be at the same potential as the VAA pin.
Thermal Pad	Thermal Pad	—	The thermal pad is located on the package underside. Connect the thermal pad to any internal PCB ground plane through multiple vias for good thermal performance.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{DD} to GND	–0.3	6	V
	V_{IO} to GND	–0.3	6	V
	V_{CC} to GND	–0.3	44	V
	V_{SS} to GND	–22	0.3	V
	REFGND to GND	–0.3	0.9	V
	V_{DD} to V_{AA}	–0.3	0.3	V
	V_{CC} to V_{SS}	–0.3	44	V
Pin voltage	DAC outputs to GND	V_{SS} – 0.3	V_{CC} + 0.3	V
	TEMPOUT to GND	–0.3	V_{DD} + 0.3	V
	REF and REFCMP to GND	–0.3	V_{DD} + 0.3	V
	Digital inputs to GND	–0.3	V_{IO} + 0.3	V
	SDO to GND	–0.3	V_{IO} + 0.3	V
	$\overline{\text{ALARMOUT}}$ to GND	–0.3	6	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{AA} (1)	Analog supply voltage	4.5		5.5	V
V_{DD} (1)	Digital supply voltage	4.5		5.5	V
V_{IO}	IO supply voltage	1.7		5.5	V
V_{CC}	Output buffer positive supply voltage	9		41.5	V
V_{SS} (2)	Output buffer negative supply voltage	–21.5		0	V
V_{CC} – V_{SS}	Output buffer supply voltage range	9		43	V
	Digital input voltage	0		V_{IO}	V
V_{REFIN}	Reference input voltage to V_{REFGND}	2.49	2.5	2.51	V
V_{REFGND} (3)	REFGND pin voltage	0	0	0.6	V
T_A	Operating ambient temperature	–40		125	°C

(1) V_{AA} and V_{DD} must be at the same potential.
(2) V_{SS} is only connected to GND when all DAC outputs are unipolar.

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(3) If V_{REFGND} is not connected to GND, a buffered source must be used to drive it.

7.4 Thermal Information

THERMAL METRIC(1)		DACx1416 RHA (VQFN) 40 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	26.8	℃/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	14.1	℃/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	3.4	℃/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	℃/W
Ψ_{JB}	Junction-to-board characterization parameter	3.4	℃/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	℃/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

all minimum/maximum specifications at T_A = –40℃ to +125℃ and all typical specifications at T_A = 25℃, V_{CC} = 9 V to 41.5 V, V_{SS} = –21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
	Resolution	DAC81416	16			Bits
		DAC71416	14			
		DAC61416	12			
INL	Integral nonlinearity	DAC81416, all ranges, except 0 V to 40 V and ±2.5 V	–1	±0.5	1	LSB
		DAC81416, 0 V to 40 V and ±2.5-V ranges	–2	±1	2	
		DAC71416, all ranges	–1	±0.5	1	
		DAC61416, all ranges	–1	±0.5	1	
DNL	Differential nonlinearity	DAC81416, specified 16-bit monotonic	–1	±0.5	1	LSB
		DAC71416, specified 14-bit monotonic	–1	±0.5	1	
		DAC61416, specified 12-bit monotonic	–1	±0.5	1	
TUE	Total unadjusted error	All ranges, except ±2.5 V	–0.1	±0.01	0.1	%FSR
		±2.5-V range	–0.2	±0.02	0.2	
	Unipolar offset error	All unipolar ranges	–0.03	±0.015	0.03	%FSR
	Unipolar zero-code error	All unipolar ranges	0	0.04	0.1	%FSR
	Bipolar zero error	All bipolar ranges	–0.2	±0.02	0.2	%FSR
	Full-scale error	All ranges	–0.2	±0.075	0.2	%FSR
	Gain error	All ranges, except ±2.5 V	–0.1	±0.02	0.1	%FSR
		±2.5-V range	–0.2	±0.02	0.2	
	Unipolar offset error drift	All unipolar ranges		±2		ppm of FSR/°C
	Bipolar zero error drift	All bipolar ranges		±2		ppm of FSR/°C
	Gain error drift	All ranges		±2		ppm of FSR/°C

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7.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40℃ to +125℃ and all typical specifications at T_A = 25℃, V_{CC} = 9 V to 41.5 V, V_{SS} = –21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output voltage drift over time	T_A = 40°C, full-scale code, 1900 hours		5		ppm of FSR

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7.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40℃ to +125℃ and all typical specifications at T_A = 25℃, V_{CC} = 9 V to 41.5 V, V_{SS} = –21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIFFERENTIAL MODE PERFORMANCE(1)						
TUE	Total unadjusted error	All ranges	–0.1	±0.01	0.1	%FSR
		±2.5-V range	–0.2	±0.02	0.2	
	Common-mode error	All bipolar ranges, midscale code	–0.1	±0.01	0.1	%FSR
OUTPUT CHARACTERISTICS						
	Output voltage headroom	To V_{SS} and V_{CC} (–10 mA ≤ I_{OUT} ≤ 10 mA)	1			V
		To V_{SS} and V_{CC} (–15 mA ≤ I_{OUT} ≤ 15 mA)	1.5			
	Short-circuit current(2)	Full-scale output shorted to V_{SS}		40		mA
		Zero-scale output shorted to V_{CC}		40		
	Load regulation	Midscale code, –15 mA ≤ I_{OUT} ≤ 15 mA		70		µV/mA
	Maximum capacitive load(3)	R_{LOAD} = open	0		1	nF
	DC output impedance	Midscale code		0.05		Ω
		Full-scale code		40		
DYNAMIC PERFORMANCE						
	Output voltage settling time	¼ to ¾ scale and ¾ to ¼ scale settling time to ±1 LSB, ±10-V range, R_L = 5 kΩ, C_L = 200 pF		12		µs
	Slew rate	0-V to 5-V range		1		V/µs
		All other output ranges		4		
	Power-on glitch magnitude	Power-down to active DAC output, ±20 V range, midscale code, R_L = 5 kΩ, C_L = 200 pF		0.3		V
	Output noise	0.1 Hz to 10 Hz, midscale code, 0-V to 5-V range		15		µVpp
	Output noise density	1 kHz, midscale code, 0-V to 5-V range		78		nV/Hz
PSRR-AC	Power supply ac rejection ratio	Midscale code, frequency = 60 Hz, amplitude = 200 mVpp superimposed on V_{DD}, V_{CC} or V_{SS}		1		LSB/V
PSRR-DC	Power supply dc rejection ratio	Midscale code, V_{DD} = 5 V ± 5%, V_{CC} = 20 V, V_{SS} = –20 V		1		LSB/V
		Midscale code, V_{DD} = 5 V, V_{CC} = 20 V ± 5%, V_{SS} = –20 V		1		
		Midscale code, V_{DD} = 5 V, V_{CC} = 20 V, V_{SS} = –20 V ± 5%		1		
	Code change glitch impulse	1-LSB change around major carrier, 0-V to 5-V range		4		nV-s
	Channel-to-channel ac crosstalk	0-V to 5-V range, measured channel at midscale, full-scale swing on all other channels		4		nV-s
	Channel-to-channel dc crosstalk	0-V to 5-V range, measured channel at midscale, all other channels at full-scale		0.25		LSB
	Digital feedthrough	0-V to 5-V range, midscale code, f_{SCLK} = 1 MHz		1		nV-s

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7.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40℃ to +125℃ and all typical specifications at T_A = 25℃, V_{CC} = 9 V to 41.5 V, V_{SS} = –21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL REFERENCE INPUT						
V_{REFIN}	Reference input voltage range	To V_{REFGND}	2.49	2.5	2.51	V
	Reference input current			50		µA
	Reference input impedance			50		kΩ
	Reference input capacitance			20		pF
INTERNAL REFERENCE						
V_{REFOUT}	Reference output voltage range	T_A = 25°C	2.4975		2.5025	V
	Reference output drift			5	15	ppm/°C
	Reference output impedance			0.1		Ω
	Reference output noise	0.1 Hz to 10 Hz		12		µVpp
	Reference output noise density	10 kHz, REF_{LOAD} = 10 nF		150		nV/Hz
	Reference load current			5		mA
	Reference load regulation	Source		80		µV/mA
	Reference line regulation			20		µV/V
	Reference output drift over time	T_A = 25°C, 1900 hours		250		µV
	Reference thermal hysteresis	First cycle		±700		µV
		Additional cycle		±50		
DIGITAL INPUTS AND OUTPUTS						
V_{IH}	High-level input voltage		0.7 × V_{IO}			V
V_{IL}	Low-level input voltage				0.3 × V_{IO}	V
	Input current			±2		µA
	Input pin capacitance			2		pF
V_{OH}	High-level output voltage	I_{OH} = 0.2 mA	V_{IO} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 0.2 mA			0.4	V
	Output pin capacitance			5		pF
ALARM OUTPUT						
	Output pin capacitance			5		pF
V_{OL}	Low-level output voltage	I_{LOAD} = –0.2 mA			0.4	V
TEMPERATURE OUTPUT						
$V_{TEMPOUT,0C}$	Output voltage offset at 0℃			1.34		V
	Sensor gain			–4		mV/°C

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7.5 Electrical Characteristics (continued)

all minimum/maximum specifications at T_A = –40℃ to +125℃ and all typical specifications at T_A = 25℃, V_{CC} = 9 V to 41.5 V, V_{SS} = –21.5 V to 0 V, V_{DD} = V_{AA} = 4.5 V to 5.5 V, V_{REFIN} = 2.5 V, V_{IO} = 1.7 V to 5.5 V, DAC outputs unloaded, digital inputs at V_{IO} or GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER REQUIREMENTS						
I_{DD}	V_{DD} supply current	Active mode, internal reference enabled, full-scale code, ±20 V output range, SPI static		0.05	0.5	mA
		Active mode, internal reference disabled, full-scale code, ±20 V output range, SPI static		0.05	0.5	mA
		Power-down mode		0.05	0.5	mA
I_{AA}	V_{AA} supply current	Active mode, internal reference enabled, full-scale code, ±20 V output range, SPI static		20	30	mA
		Active mode, internal reference disabled, full-scale code, ±20 V output range, SPI static		18	28	mA
		Power-down mode		2	85	µA
I_{CC}	V_{CC} supply current	Active mode, internal reference enabled, full-scale code, ±20 V output range, SPI static		10	25	mA
		Active mode, internal reference disabled, full-scale code, ±20 V output range, SPI static		10	25	mA
		Power-down mode		10	30	µA
I_{SS}	V_{SS} supply current	Active mode, internal reference enabled, full-scale code, ±20 V output range, SPI static	–15	–10		mA
		Active mode, internal reference disabled, full-scale code, ±20 V output range, SPI static	–15	–10		mA
		Power-down mode	–30	–10		µA
I_{IO}	V_{IO} supply current	SCLK and SDI toggling at 50 MHz		350	500	µA

(1) End point fit between codes. 16-bit: Code 256 to 65280, 14-bit: Code 128 to 16256, 12-bit: Code 32 to 4064.
(2) Temporary overload condition protection. Junction temperature can be exceeded during current limit. Operation above the specified maximum junction temperature may impair device reliability.
(3) Specified by design and characterization, not production tested.

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7.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SERIAL INTERFACE - WRITE OPERATION						
$f_{(SCLK)}$	Serial clock frequency	V_{IO} = 1.7 V to 2.7 V			25	MHz
		V_{IO} = 2.7 V to 5.5 V			50	
$t_{SCLKHIGH}$	SCLK high time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	10			
$t_{SCLKLOW}$	SCLK low time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	10			
t_{SDIS}	SDI setup time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{SDIH}	SDI hold time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup time	V_{IO} = 1.7 V to 2.7 V	30			ns
		V_{IO} = 2.7 V to 5.5 V	15			
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSHIGH}	$\overline{CS}$ hight time	V_{IO} = 1.7 V to 2.7 V	50			ns
		V_{IO} = 2.7 V to 5.5 V	25			
$t_{DACWAIT}$	Sequential DAC update wait time	V_{IO} = 1.7 V to 2.7 V	2.4			µs
		V_{IO} = 2.7 V to 5.5 V	2.4			
$t_{BCASTWAIT}$	Broadcast DAC update wait time	V_{IO} = 1.7 V to 2.7 V	4			µs
		V_{IO} = 2.7 V to 5.5 V	4			
SERIAL INTERFACE - READ AND DAISY CHAIN OPERATION, FSDO = 0						
$f_{(SCLK)}$	Serial clock frequency	V_{IO} = 1.7 V to 2.7 V			15	MHz
		V_{IO} = 2.7 V to 5.5 V			20	
$t_{SCLKHIGH}$	SCLK high time	V_{IO} = 1.7 V to 2.7 V	33			ns
		V_{IO} = 2.7 V to 5.5 V	25			
$t_{SCLKLOW}$	SCLK low time	V_{IO} = 1.7 V to 2.7 V	33			ns
		V_{IO} = 2.7 V to 5.5 V	25			
t_{SDIS}	SDI setup time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{SDIH}	SDI hold time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup time	V_{IO} = 1.7 V to 2.7 V	30			ns
		V_{IO} = 2.7 V to 5.5 V	20			
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	V_{IO} = 1.7 V to 2.7 V	8			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSHIGH}	$\overline{CS}$ high time	V_{IO} = 1.7 V to 2.7 V	50			ns
		V_{IO} = 2.7 V to 5.5 V	25			
t_{SDOZD}	SDO tri-state to driven	V_{IO} = 1.7 V to 2.7 V	0		20	ns
		V_{IO} = 2.7 V to 5.5 V	0		20	
t_{SDODLY}	SDO output delay	V_{IO} = 1.7 V to 2.7 V	0		35	ns
		V_{IO} = 2.7 V to 5.5 V	0		20	

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7.6 Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SERIAL INTERFACE - READ AND DAISY CHAIN OPERATION, FSDO = 1						
$f_{(SCLK)}$	Serial clock frequency	V_{IO} = 1.7 V to 2.7 V			25	MHz
		V_{IO} = 2.7 V to 5.5 V			35	
$t_{SCLKHIGH}$	SCLK high time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	14			
$t_{SCLKLOW}$	SCLK low time	V_{IO} = 1.7 V to 2.7 V	20			ns
		V_{IO} = 2.7 V to 5.5 V	14			
t_{SDIS}	SDI setup time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{SDIH}	SDI hold time	V_{IO} = 1.7 V to 2.7 V	10			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup time	V_{IO} = 1.7 V to 2.7 V	30			ns
		V_{IO} = 2.7 V to 5.5 V	20			
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	V_{IO} = 1.7 V to 2.7 V	8			ns
		V_{IO} = 2.7 V to 5.5 V	5			
t_{CSHIGH}	$\overline{CS}$ high time	V_{IO} = 1.7 V to 2.7 V	50			ns
		V_{IO} = 2.7 V to 5.5 V	25			
t_{SDOZD}	SDO tri-state to driven	V_{IO} = 1.7 V to 2.7 V	0		20	ns
		V_{IO} = 2.7 V to 5.5 V	0		20	
t_{SDODLY}	SDO output delay	V_{IO} = 1.7 V to 2.7 V	0		35	ns
		V_{IO} = 2.7 V to 5.5 V	0		20	
DIGITAL LOGIC						
t_{LOGDLY}	$\overline{CS}$ rising edge to $\overline{LDAC}$ or $\overline{CLR}$ falling edge delay time	VIO = 1.7 V to 2.7 V	40			ns
t_{LOGDLY}	$\overline{CS}$ rising edge to $\overline{LDAC}$ or $\overline{CLR}$ falling edge delay time	VIO = 2.7 V to 5.5 V	20			
t_{LDAC}	$\overline{LDAC}$ low time	VIO = 1.7 V to 2.7 V	20			ns
		VIO = 2.7 V to 5.5 V	10			
t_{CLR}	$\overline{CLR}$ low time	VIO = 1.7 V to 2.7 V	20			ns
		VIO = 2.7 V to 5.5 V	10			
t_{RESET}	POR reset delay	VIO = 1.7 V to 2.7 V			1	ms
		VIO = 2.7 V to 5.5 V			1	
f_{TOGGLE}	TOGGLE frequency	VIO = 1.7 V to 2.7 V			100	kHz
		VIO = 2.7 V to 5.5 V			100	

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7.7 Timing Diagrams

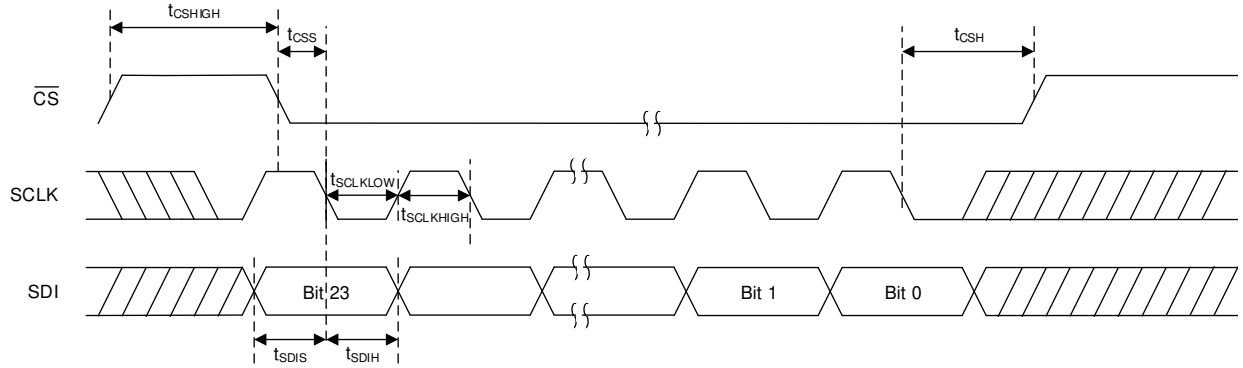

图 7-1. Serial Interface Write Timing Diagram

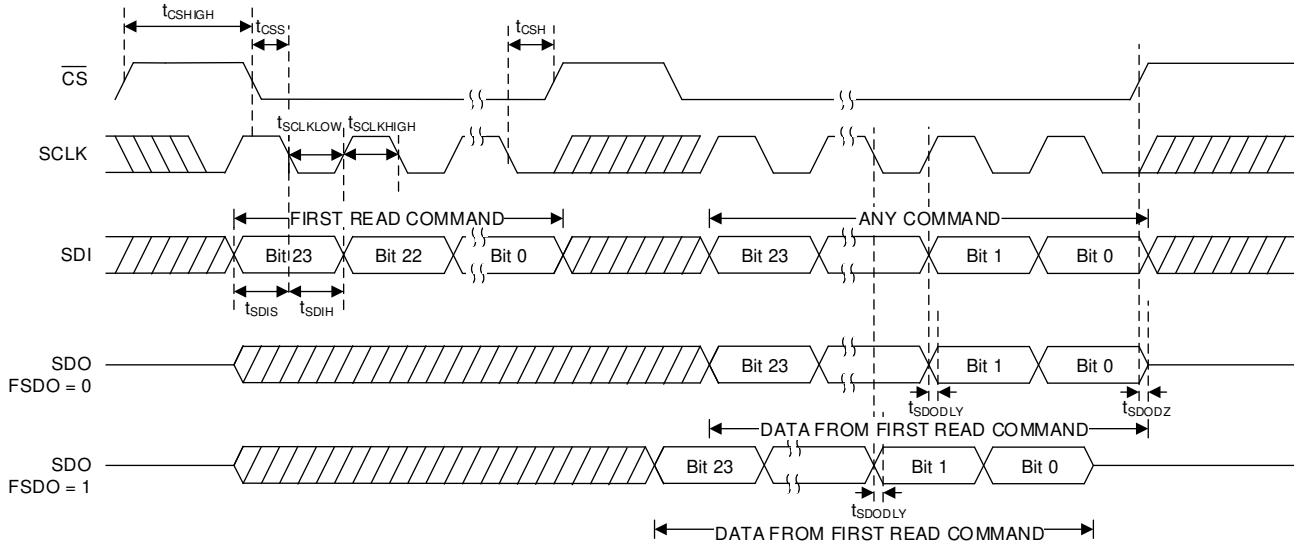

图 7-2. Serial Interface Read Timing Diagram

7.8 Typical Characteristics

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $V_{SS} \leq V_{MIN}$ – 1.5 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

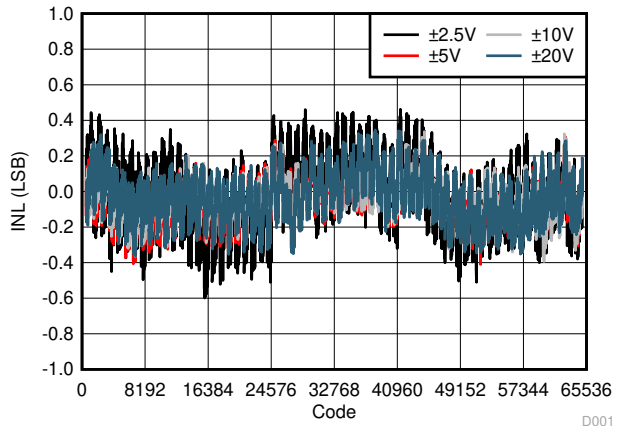

图 7-3. Integral Linearity Error vs Digital Input Code (Bipolar Outputs)

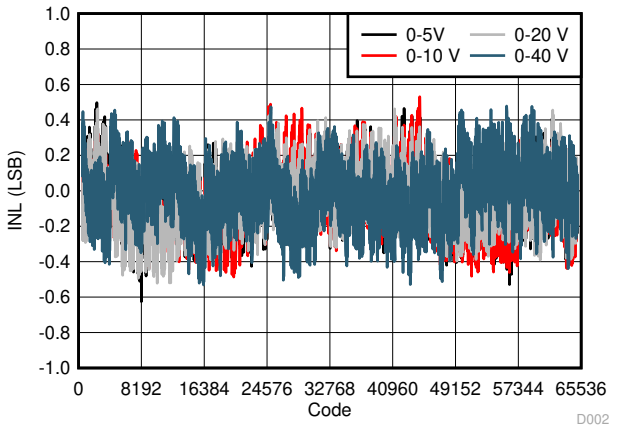

图 7-4. Integral Linearity Error vs Digital Input Code (Unipolar Outputs)

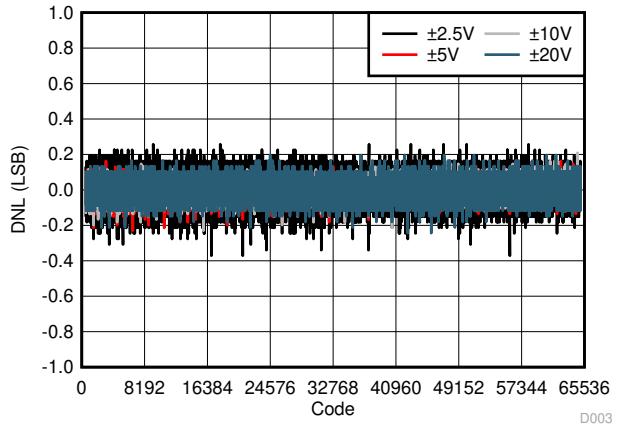

图 7-5. Differential Linearity Error vs Digital Input Code (Bipolar Outputs)

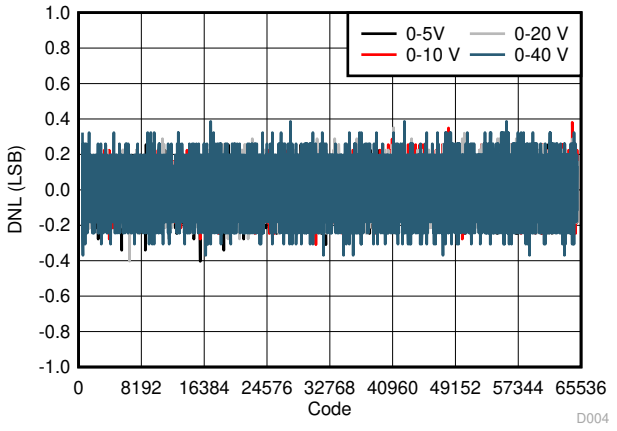

图 7-6. Differential Linearity Error vs Digital Input Code (Unipolar Outputs)

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7.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and $V_{CC} \geqslant V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $V_{SS} \leqslant V_{MIN}$ – 1.5 V and $V_{CC} \geqslant V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

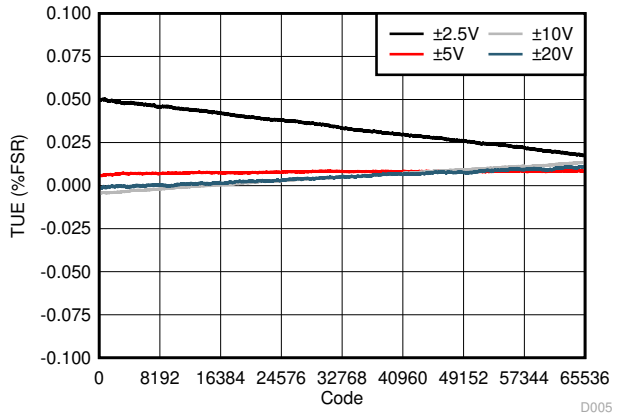


图 7-7. Total Unadjusted Error vs Digital Input Code (Bipolar Outputs)

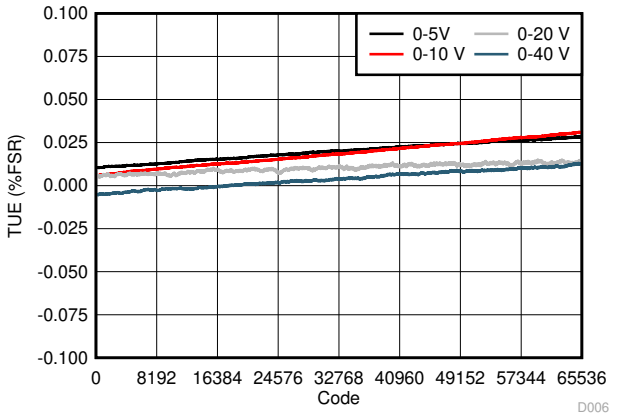


图 7-8. Total Unadjusted Error vs Digital Input Code (Unipolar Outputs)

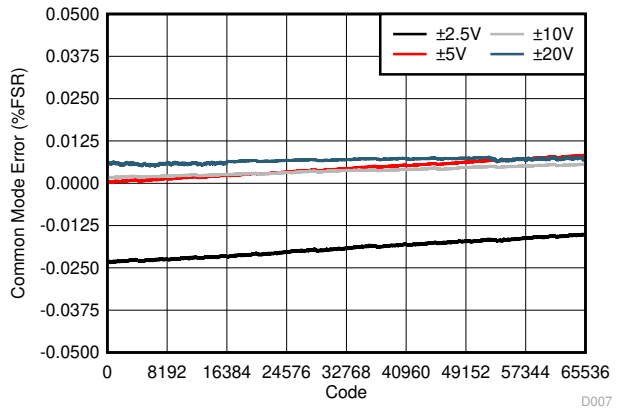


图 7-9. Common Mode Error vs Digital Input Code (Differential Bipolar Outputs)

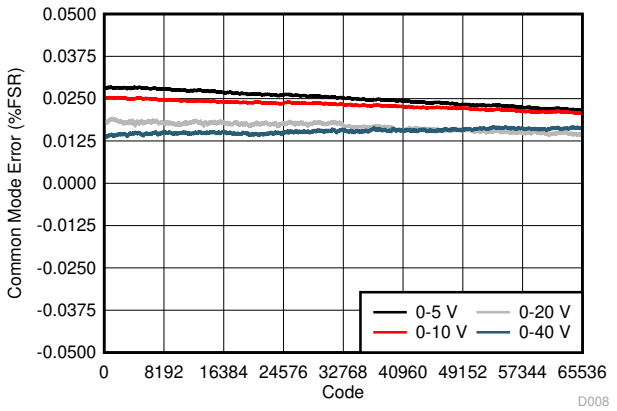
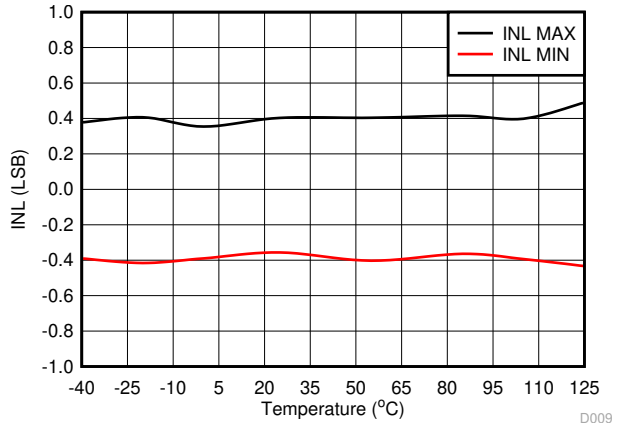
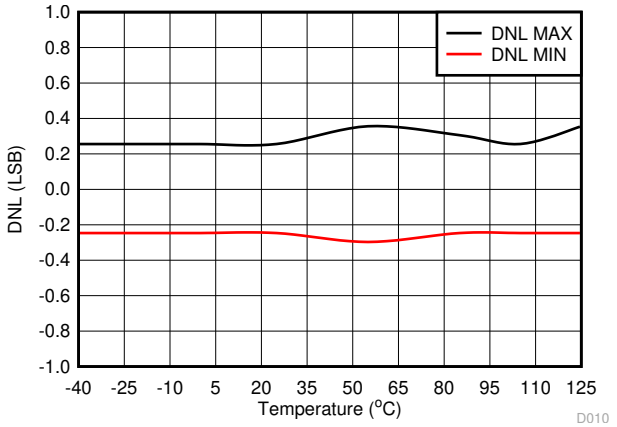


图 7-10. Common Mode Error vs Digital Input Code (Differential Unipolar Outputs)



±20-V output range

图 7-11. Integral Linearity Error vs Temperature



±20-V output range

图 7-12. Differential Linearity Error vs Temperature

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7.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and $V_{CC} \geqslant V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $V_{SS} \leqslant V_{MIN}$ – 1.5 V and $V_{CC} \geqslant V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

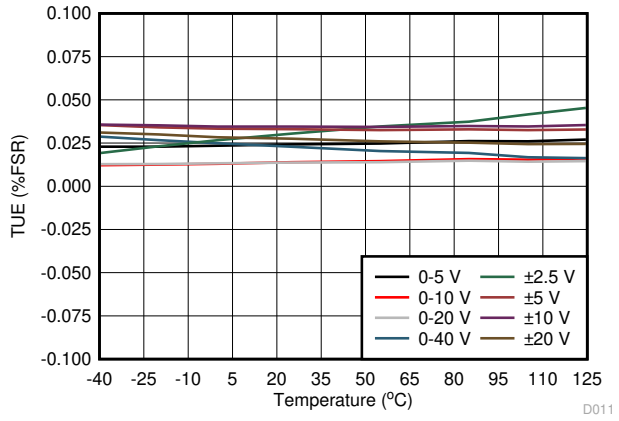

图 7-13. Total Unadjusted Error vs Temperature

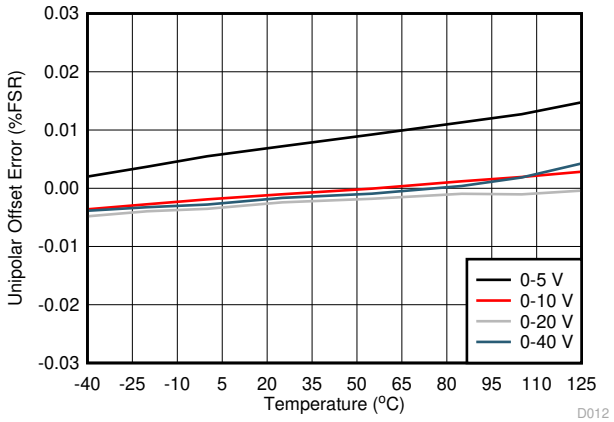

图 7-14. Unipolar Offset Error vs Temperature

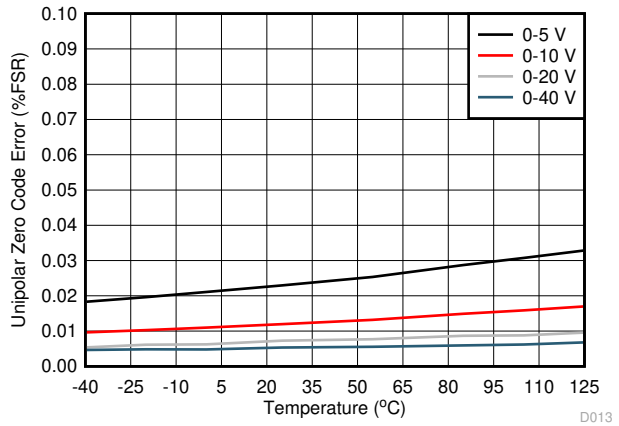

图 7-15. Unipolar Zero Code Error vs Temperature

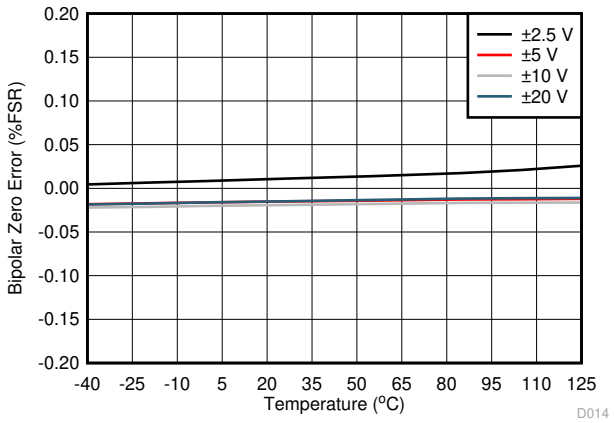

图 7-16. Bipolar Zero Error vs Temperature

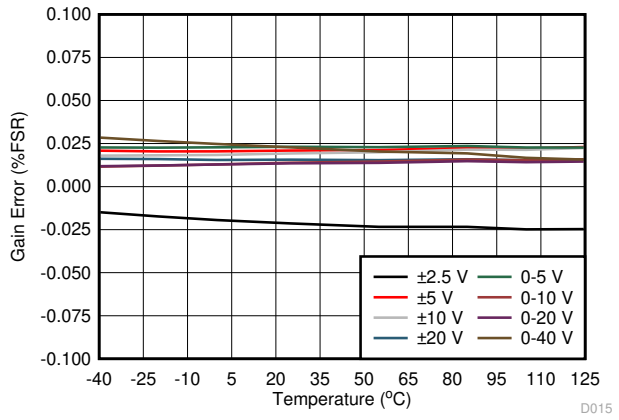

图 7-17. Gain Error vs Temperature

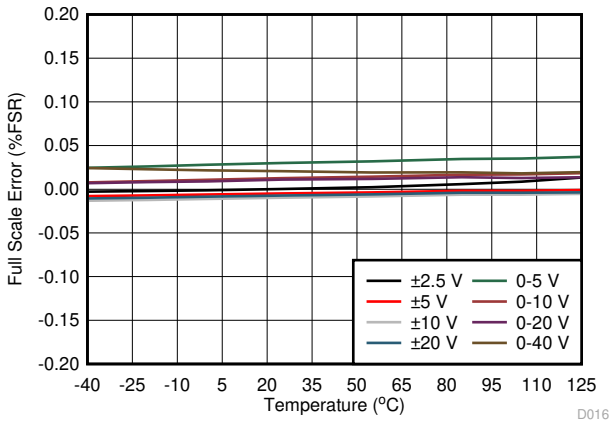

图 7-18. Full-Scale Error vs Temperature

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7.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and $V_{CC} \geqslant V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $V_{SS} \leqslant V_{MIN}$ – 1.5 V and $V_{CC} \geqslant V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

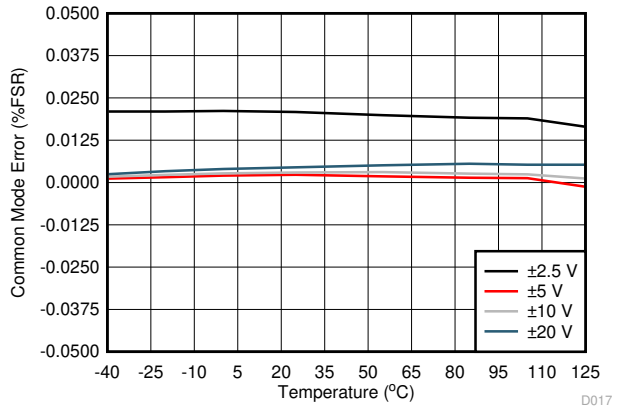


图 7-19. Common Mode Error vs Temperature (Differential Bipolar Outputs)

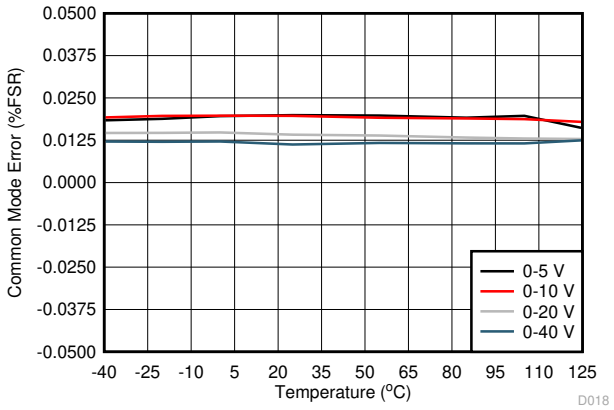
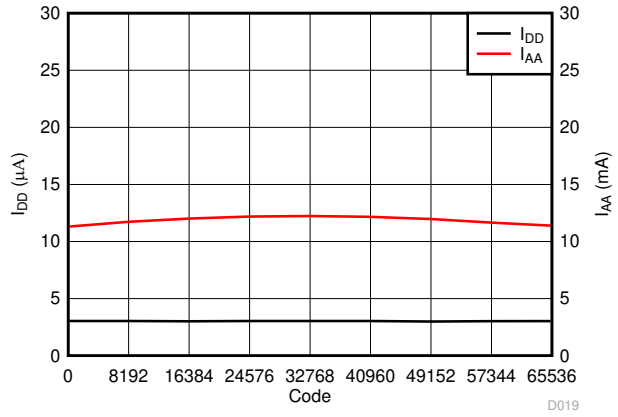
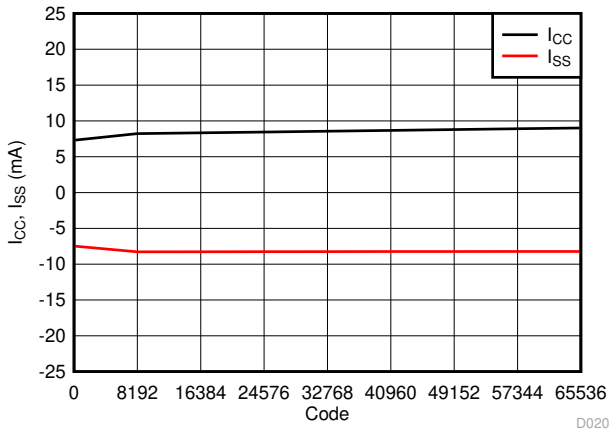


图 7-20. Common Mode Error vs Temperature (Differential Unipolar Outputs)



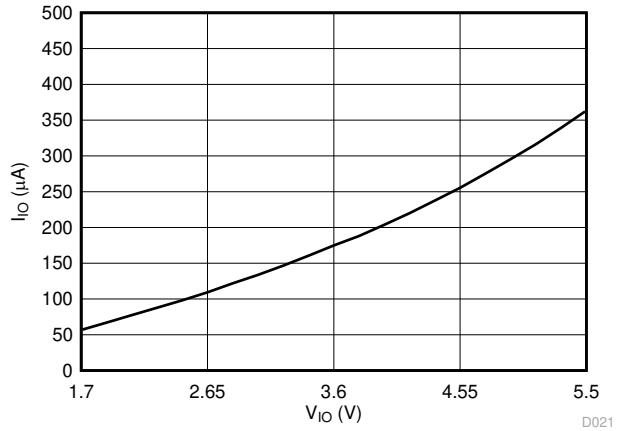
±20-V output range

图 7-21. Supply Current (I_{DD}, I_{AA}) vs Digital Input Code



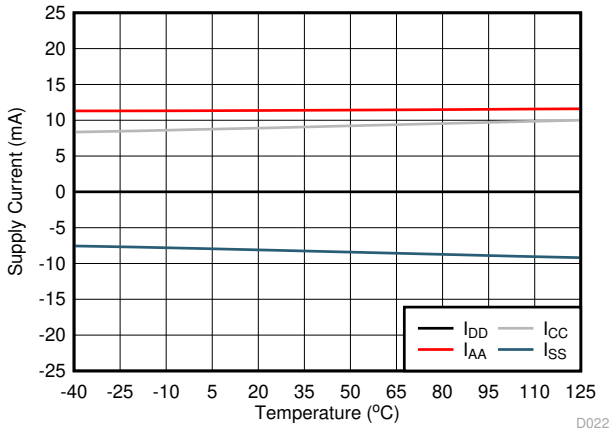
±20-V output range

图 7-22. Supply Current (I_{CC}, I_{SS}) vs Digital Input Code



±20-V output range

图 7-23. Supply Current (I_{IO}) vs Supply Voltage



±20-V output range

图 7-24. Supply Current vs Temperature

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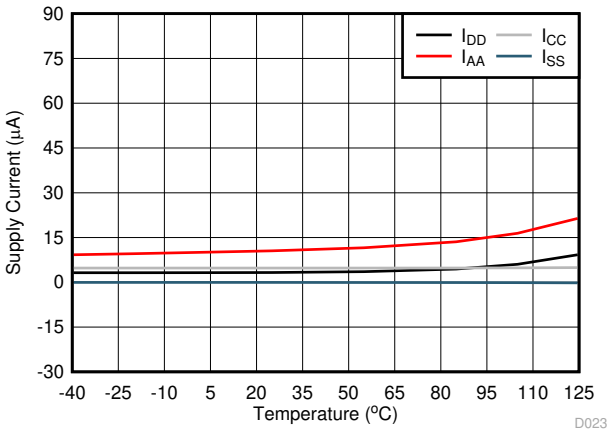
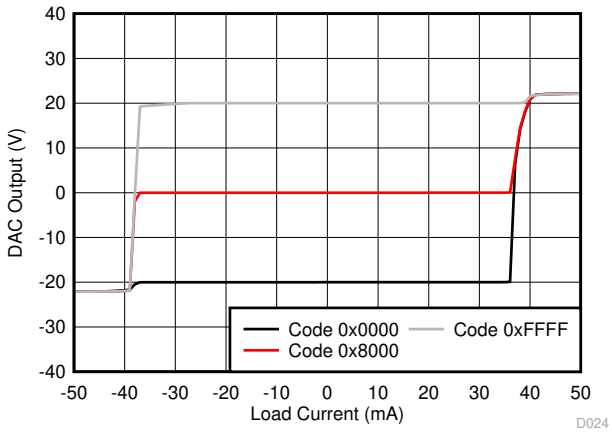
7.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and $V_{CC} \geqslant V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $V_{SS} \leqslant V_{MIN}$ – 1.5 V and $V_{CC} \geqslant V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)



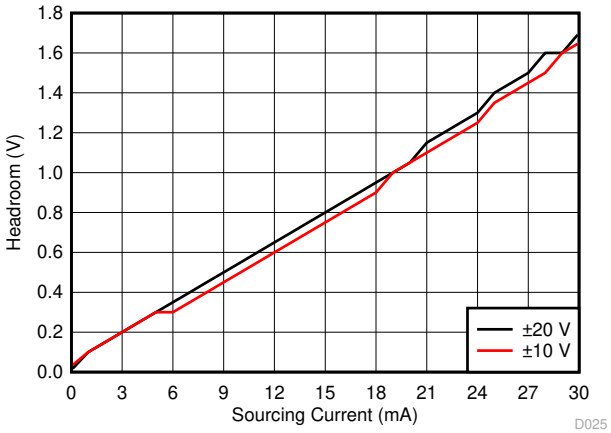
±20-V output range

图 7-25. Power-Down Current vs Temperature



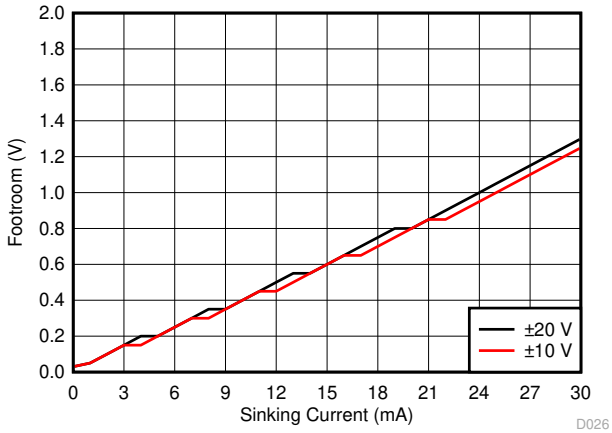
±20-V output range

图 7-26. Source and Sink Capability



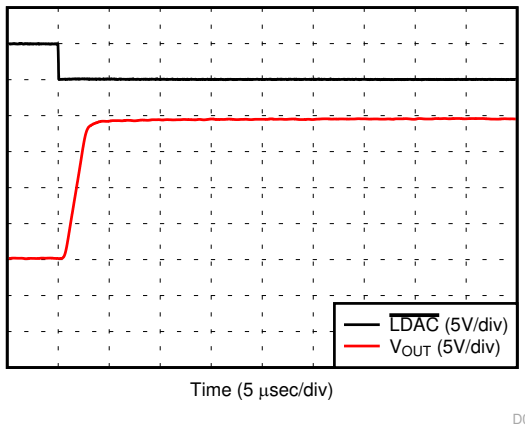
Full-scale code

图 7-27. V_{CC} Headroom vs Sourcing Current



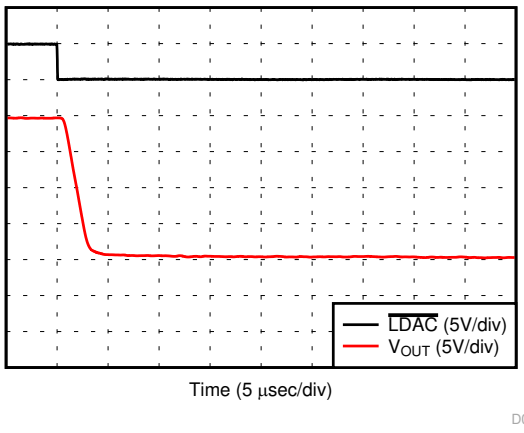
Zero code

图 7-28. V_{SS} Footroom vs Sinking Current



±20-V output range

图 7-29. Full-Scale Settling Time, Rising Edge



±20-V output range

图 7-30. Full-Scale Settling Time, Falling Edge

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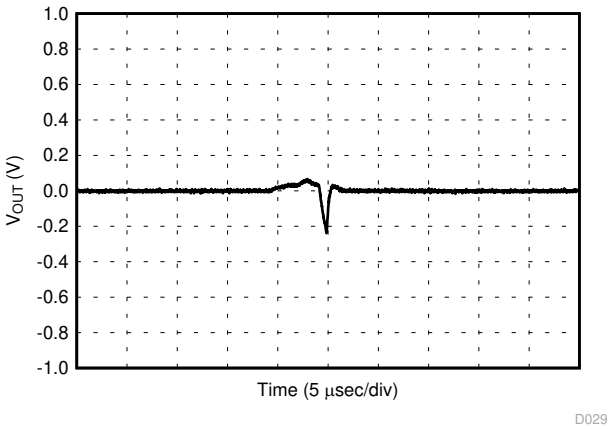
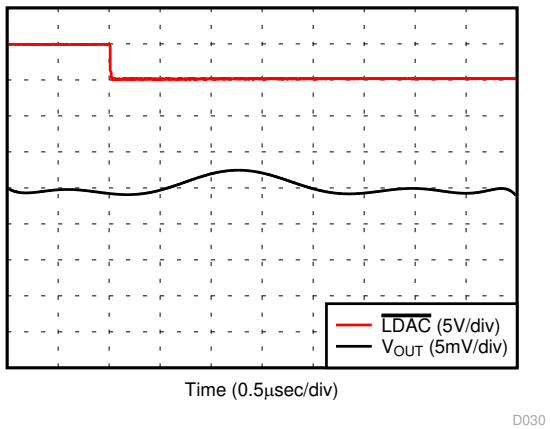
7.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $V_{SS} \leq V_{MIN}$ – 1.5 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)



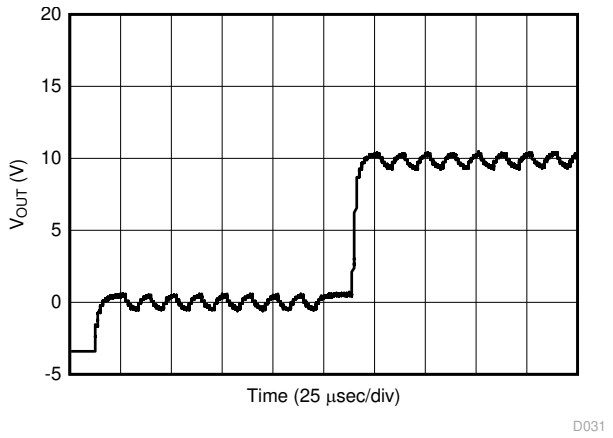
Power-down to active DAC mode
±20-V output range

图 7-31. DAC Output Enable Glitch



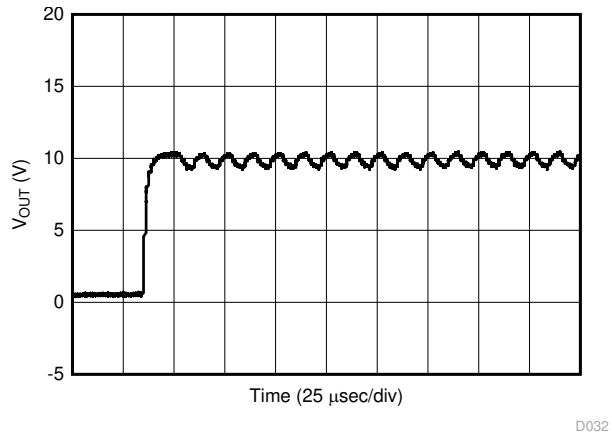
0-V to 5-V output range

图 7-32. Glitch Impulse, 1 LSB Step



±20-V output range
Toggle signal: 1 V_{PP}
DC change: midscale to 3/4 full-scale

图 7-33. Toggle Output Change Response



±20-V output range
Toggle signal: 1 V_{PP}
DC value: 3/4 full-scale

图 7-34. Toggle Enable Response

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7.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $V_{SS} \leq V_{MIN}$ – 1.5 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

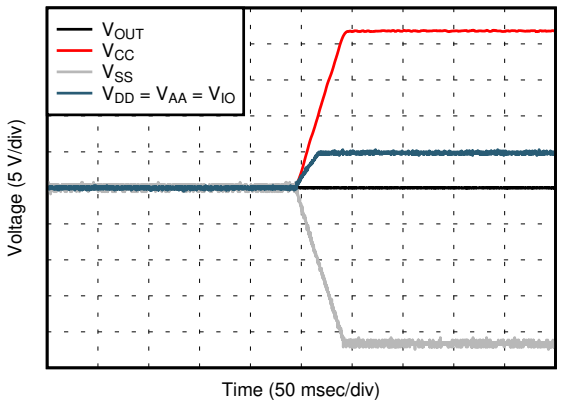


图 7-35. Power-Up Response

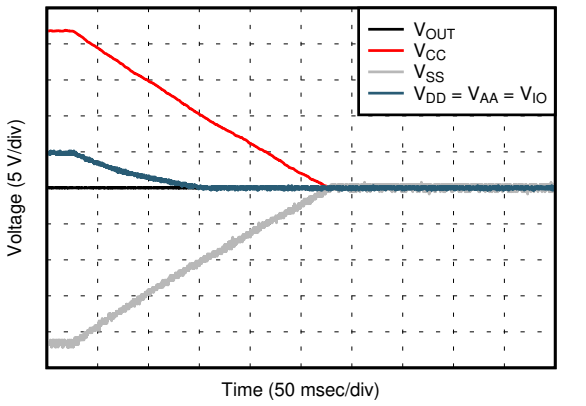
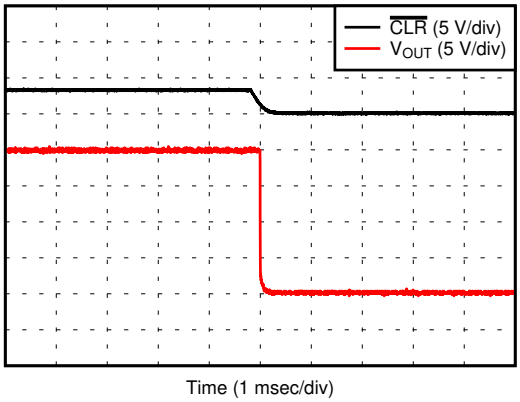
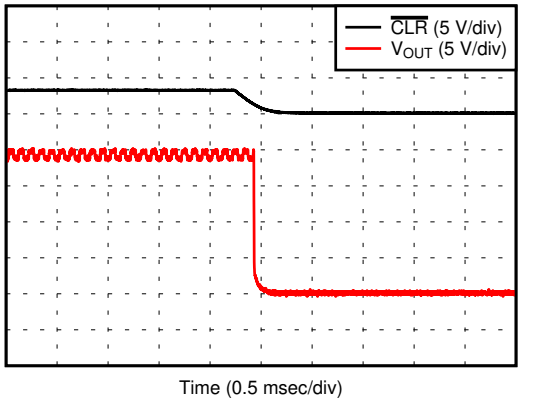


图 7-36. Power-Down Response



±20-V output range
Full-scale code to 0 V

图 7-37. Clear Command Response



±20-V output range
Toggle signal: 1 V_{PP}
DC value at 20 V

图 7-38. Clear Command Response in Toggle Mode

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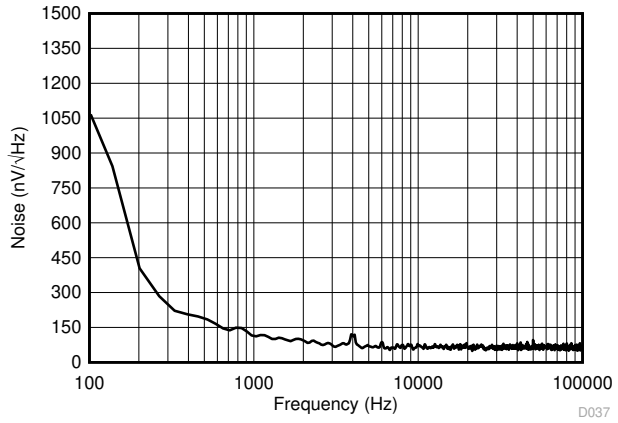
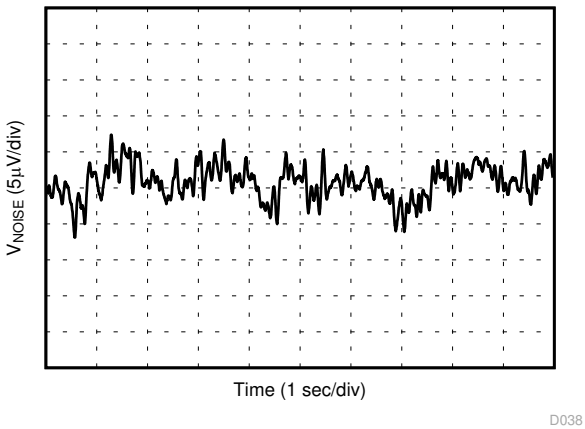
7.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and $V_{CC} \geqslant V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $V_{SS} \leqslant V_{MIN}$ – 1.5 V and $V_{CC} \geqslant V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)



0 to 5-V output range
Midscale code

图 7-39. DAC Output Noise Density vs Frequency



0 to 5-V output range
Midscale code

图 7-40. DAC Output Noise

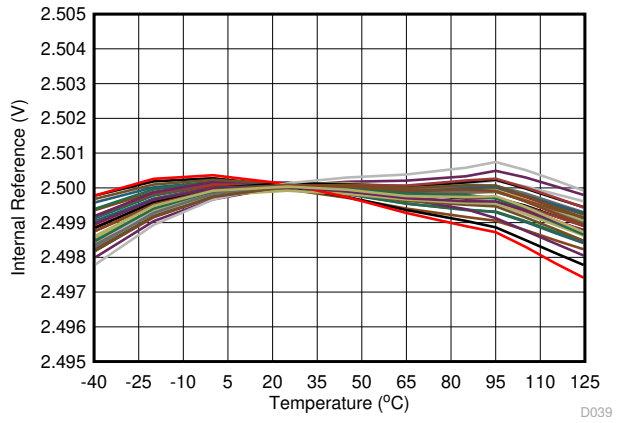


图 7-41. Internal Reference Voltage vs Temperature

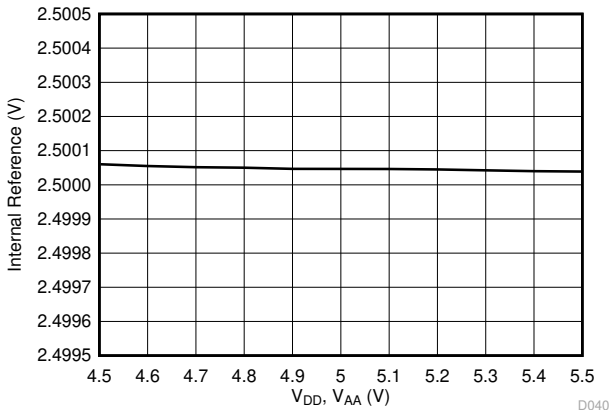


图 7-42. Internal Reference Voltage vs Supply Voltage

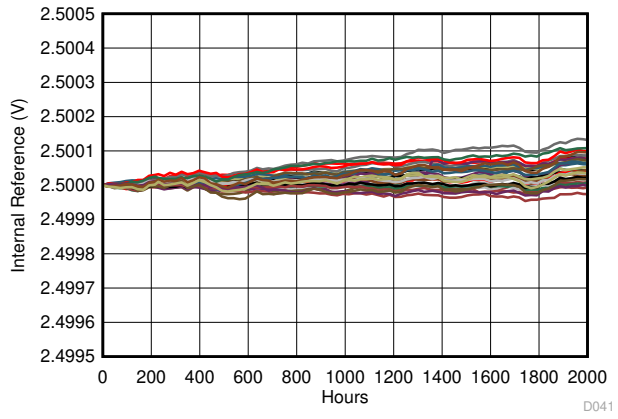


图 7-43. Internal Reference Voltage vs Time

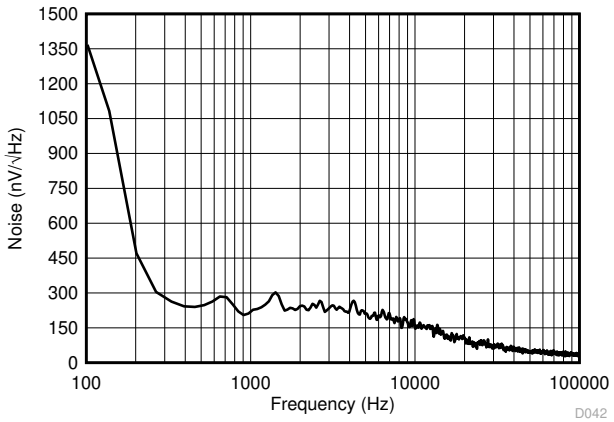


图 7-44. Internal Reference Noise Density vs Frequency

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7.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = V_{AA} = 5 V, V_{REFIN} = 2.5 V, unipolar ranges: V_{SS} = 0 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range, bipolar ranges: $V_{SS} \leq V_{MIN}$ – 1.5 V and $V_{CC} \geq V_{MAX}$ + 1.5 V for the DAC range, and DAC outputs unloaded (unless otherwise noted)

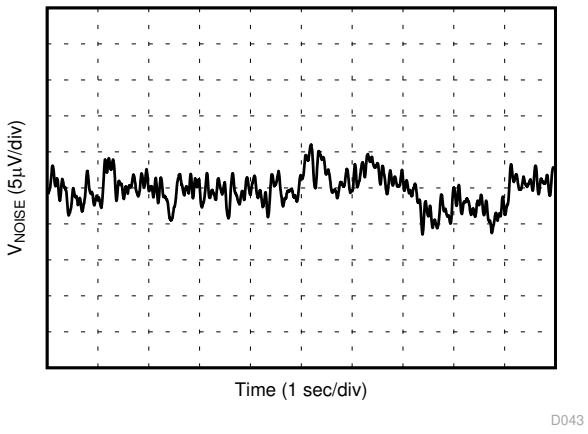

图 7-45. Internal Reference Noise

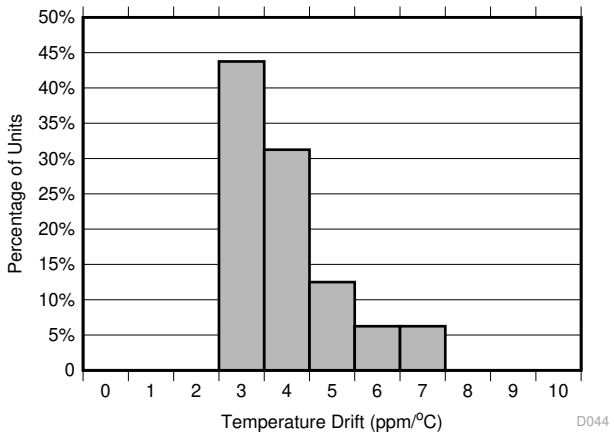

图 7-46. Internal Reference Temperature Drift Histogram

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8 Detailed Description

8.1 Overview

The DACx1416 are a pin-compatible family of 16-channel, buffered, high-voltage output digital-to-analog converters (DACs) with 16-bit, 14-bit, and 12-bit resolution. The DACx1416 include a 2.5-V internal reference. A user-selectable output configuration enables full-scale bipolar output voltages of ±20 V, ±10 V, ±5 V or ±2.5 V, and full-scale unipolar output voltages of 40 V, 20 V, 10 V or 5 V. The full-scale output range for each DAC channel is independently programmable. In addition, each pair of DAC channels can be configured to provide a differential output. Three dedicated A-B toggle pins enable dither signal generation with up to three possible frequencies.

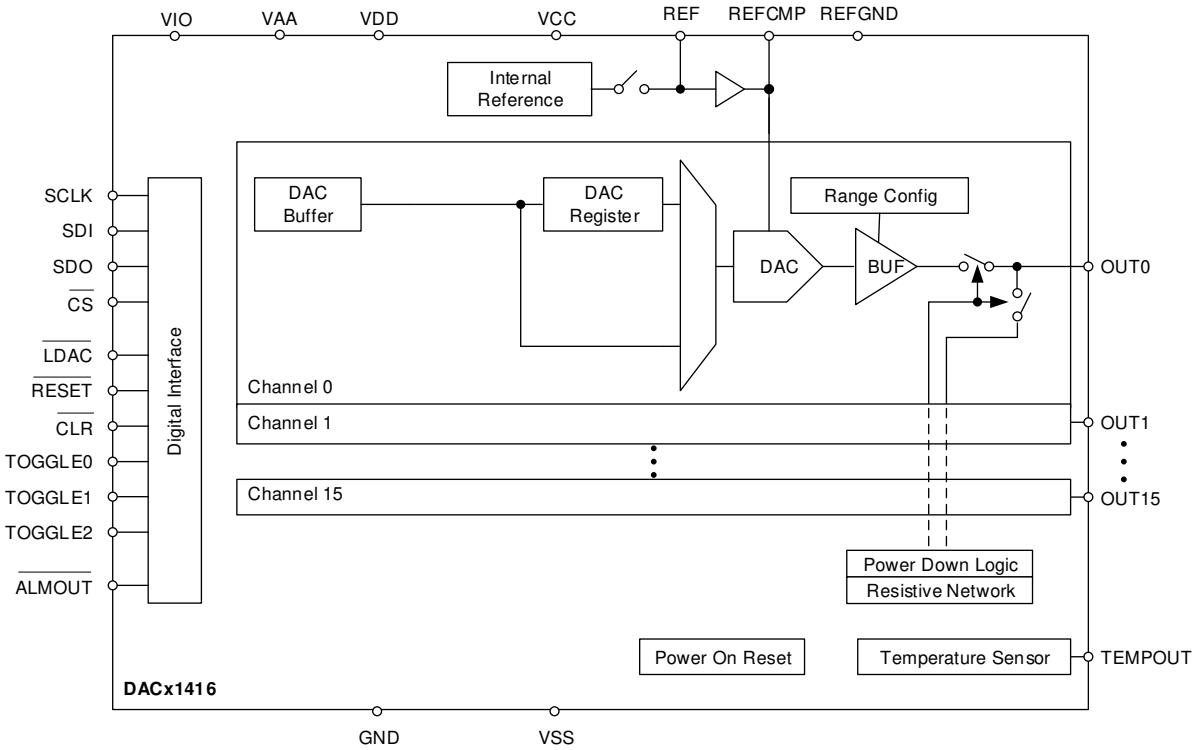
The DACx1416 operate from five supply voltages: V_{DD}, V_{AA}, V_{CC}, V_{SS} and V_{IO}.

- V_{DD} and V_{AA} are the digital and analog supplies for the DACs, internal reference and other low voltage components and must be set at the same potential.
- V_{CC} and V_{SS} are the positive and analog supplies for the DAC output amplifiers.
- V_{IO} sets the logic levels for the digital inputs and outputs.

Communication with the DACx1416 is performed through a 4-wire serial interface that supports stand-alone and daisy-chain operation. The optional frame-error checking provides added robustness to the DACx1416 serial interface.

The DACx1416 incorporate a power-on-reset circuit that connects the DAC outputs to ground at power up. The outputs remain in this state until the device registers are properly configured for operation.

8.2 Functional Block Diagram



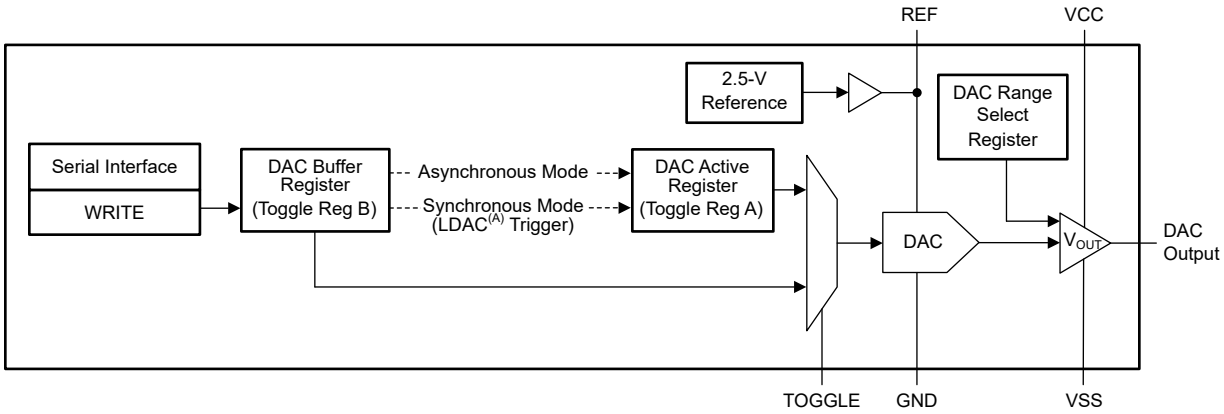
8.3 Feature Description

8.3.1 Digital-to-Analog Converter (DAC) Architecture

Each output channel in the DACx1416 consists of an R-2R ladder architecture followed by an output buffer amplifier capable of rail-to-rail operation. The output amplifiers can drive 25 mA with 1.5-V headroom from either V_{CC} or V_{SS} while maintaining the specified TUE specification for the device. The full-scale output voltage for each channel can be individually configured to the following ranges:

- – 20 V to +20 V
- – 10 V to +10 V
- – 5 V to +5 V
- – 2.5 V to +2.5 V
- 0 V to 40 V
- 0 V to 20 V
- 0 V to 10 V
- 0 V to 5 V

图 8-1 shows a block diagram of the DAC architecture.



A. The DAC trigger is generated by either by writing 1 to the LDAC bit or by the $\overline{LDAC}$ pin in synchronous mode. In asynchronous mode, the DAC latch is transparent.

图 8-1. DACx1416 DAC Block Diagram

8.3.1.1 DAC Transfer Function

The input data are written to the individual DAC Data registers in straight binary format for all output ranges. The DAC transfer function is given by 方程式 1.

$$V_{OUT} = \left(\frac{CODE}{2^n} \times FSR \right) + V_{MIN} \quad (1)$$

where:

- CODE is the decimal equivalent of the binary code that is loaded to the DAC register. CODE range is from 0 to 2^n – 1.
- n is the DAC resolution in bits. Either 12 (DAC61416), 14 (DAC71416) or 16 (DAC81416).
- FSR is the DAC full-scale range. Equal to V_{MAX} – V_{MIN} for the selected DAC output range.
- V_{MIN} is the lowest voltage for the selected DAC output range.

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8.3.1.2 DAC Register Structure

Data written to the DAC data registers is initially stored in the DAC buffer registers. Transfer of data from the DAC buffer registers to the active DAC registers can be configured to happen immediately (asynchronous mode) or initiated by a DAC trigger signal (synchronous mode). Once the DAC active registers are updated, the DAC outputs change to the new values.

After a power-on or reset event, all DAC registers are set to zero code, the DAC output amplifiers are powered down, and the DAC outputs are clamped to ground.

8.3.1.2.1 DAC Register Synchronous and Asynchronous Updates

The update mode for each DAC channel is determined by the status of its corresponding SYNC-EN bit. In asynchronous mode, a write to the DAC data register results in an immediate update of the DAC active register and DAC output on a $\overline{CS}$ rising edge. In synchronous mode, writing to the DAC data register does not automatically update the DAC output. Instead the update occurs only after a trigger event. A DAC trigger signal is generated either through the LDAC bit or by the $\overline{LDAC}$ pin. The synchronous update mode enables simultaneous update of multiple DAC outputs. In both update modes a minimum wait time of 1 µs is required between DAC output updates.

8.3.1.2.2 Broadcast DAC Register

The DAC broadcast register enables a simultaneous update of multiple DAC outputs with the same value with a single register write. Broadcast operation is only possible when all DAC channels are in single-ended mode operation. If one or more outputs are configured in differential mode the broadcast command is ignored.

Each DAC channel can be configured to update or remain unaffected by a broadcast command by setting the corresponding DAC-BRDCAST-EN bit. A register write to the BRDCAST-DATA register forces those DAC channels that have been configured for broadcast operation to update their DAC buffer registers to this value. The DAC outputs update to the broadcast value according to their synchronous mode configuration.

8.3.1.2.3 Clear DAC Operation

The DAC outputs are set in clear mode through the $\overline{CLR}$ pin. In clear mode each DAC data channel is set to the clear code associated with its configuration as shown in 表 8-1. A $\overline{CLR}$ pin logic low forces all DAC channels to clear the contents of their buffer and active registers to the clear code, and sets the analog outputs accordingly regardless of their synchronization setting.

表 8-1. Clear DAC Value

UNIPOLAR / BIPOLAR RANGE	DIFFERENTIAL MODE	CLEAR CODE
Unipolar	No	Zero code
Unipolar	Yes	Midscale code
Bipolar	No	Midscale code
Bipolar	Yes	Midscale code

When a DAC is operating in toggle mode, a clear command sets both toggle registers to the clear value.

8.3.2 Internal Reference

The DAx1416 includes a precision 2.5-V bandgap reference with a typical temperature drift of 5 ppm/°C. The internal reference is externally available at the REF pin. An external buffer amplifier with a high impedance input is required to drive any external load.

A minimum 150-nF capacitor is recommended between the reference output and GND for noise filtering. A compensation capacitor (330 pF, typical) should be connected between the REFCMP pin and REFGND.

Operation from an external reference is also supported by powering down the internal reference. The external reference is applied to the REF pin.

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8.3.3 Device Reset Options

8.3.3.1 Power-on-Reset (POR)

The DACx1416 includes a power-on reset function. After the supplies have been established, a POR event is issued. The POR causes all registers to initialize to their default values and communication with the device is valid only after a 1-ms power-on-reset delay. After a POR event, the device is set in power-down mode where all DAC channels and internal reference are powered down and the DAC output pins are connected to ground through a 10-kΩ internal resistor.

8.3.3.2 Hardware Reset

A device hardware reset event is initiated by a minimum 500 ns logic low on the $\overline{\text{RESET}}$ pin. A hardware reset initiates a POR event.

8.3.3.3 Software Reset

A device software reset event is initiated by writing the reserved code 0x1010 to SOFT-RESET in the TRIGGER register. The software reset command is triggered on the $\overline{\text{CS}}$ rising edge of the instruction. A software reset initiates a POR event.

8.3.4 Thermal Protection

Because of the device DAC channel density and high drive capability, make sure that the effects of power dissipation on the device temperature are understood and that the device temperature does not exceed the maximum junction temperature.

8.3.4.1 Analog Temperature Sensor: TEMPOUT Pin

The DACx1416 includes an analog temperature monitor with an unbuffered output voltage that is inversely proportional to the device junction temperature. The TEMPOUT pin output voltage has a temperature slope of –4 mV/°C and a 1.34-V offset as described by 方程式 2.

$$V_{TEMPOUT} = \left(\frac{-4\ mV}{°C} \times T \right) + 1.34\ V \tag{2}$$

where:

- T is the device junction temperature in °C.
- $V_{TEMPOUT}$ is the temperature monitor output voltage.

8.3.4.2 Thermal Shutdown

The DACx1416 incorporates a thermal shutdown that is triggered when the die temperature exceeds 140°C. A thermal shutdown sets the TEMP-ALM bit and causes all DAC outputs to power-down, however the internal reference remains powered on. The $\overline{\text{ALMOUT}}$ pin can be configured to monitor a thermal shutdown condition by setting the TEMPALM-EN bit. Once a thermal shutdown is triggered, the device stays in shutdown even after the device temperature lowers.

The die temperature must fall below 140°C before the device can be returned to normal operation. To resume normal operation, the thermal alarm must be cleared through the ALM-RESET bit while the DAC channels are in power-down mode.

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8.4 Device Functional Modes

8.4.1 Toggle Mode

Each DAC in the device can be independently configured to operate in toggle mode. A DAC channel in toggle mode incorporates two DAC registers (Register A and Register B) and can be set to switch repetitively between these two values. The DACx1416 toggle mode operation can be configured to introduce a dither signal to the DAC output, to generate a periodic signal or to implement ON/OFF signaling, among some examples.

To update the toggle registers the following sequence should be followed:

1. Set DAC channel in synchronous mode and disable toggle mode for that channel
2. Write the desired Register A value to the DAC data register
3. Issue a DAC trigger signal to load Register A
4. Write the desired Register B value to the DAC data register
5. Enable toggle mode to load Register B

Once both registers are loaded with data, any of the three TOGGLE[2:0] pins can be used to switch those DACs configured for toggle operation back and forth between the contents of their two DAC specific registers by using an external clock or logic signal. A TOGGLE pin logic low updates the DAC output to the value set by Register A. A logic high updates the DAC output to the value set by Register B. The three TOGGLE[2:0] pins give the DACx1416 the option to operate with up to three toggle rates.

Additionally, the device can be configured for software controlled toggle operation by setting the SOFTTOGGLE-EN bit. In this mode, any of the three AB-TOG[2:0] bits can be used as a toggle control signal. Setting the AB-TOG bit to 1 enables Register B and clearing it to 0 enables Register A.

8.4.2 Differential Mode

Each DAC pair in the device, can be independently configured to operate as a differential output pair. The differential output of a *DACx-y* pair is updated by writing to the *DACx* channel. For proper operation, the two DAC pairs must be configured to the same output range prior to enabling differential mode. 图 8-2 and 图 8-3 show the ideal differential output voltages (V_{DIFF}) and common mode voltages (V_{CM}) for a DAC differential pair configured for ±20-V and 0 to 40-V operation, respectively.

After being configured as a differential output, the *DACx-y* pair can be set for toggle operation by updating the *DACx* toggle registers as described in 节 8.4.1.

Imbalances between the two differential signals result in common-mode and amplitude errors. The device incorporates an offset register that enables the user to introduce a voltage offset to the *DACy* channel of the *DACx-y* differential pair to compensate for a DC offset error between the two channels. The offset compensation gives approximately a ±0.2%FSR adjustment window. The differential DAC data register must be rewritten after an update to the offset register.

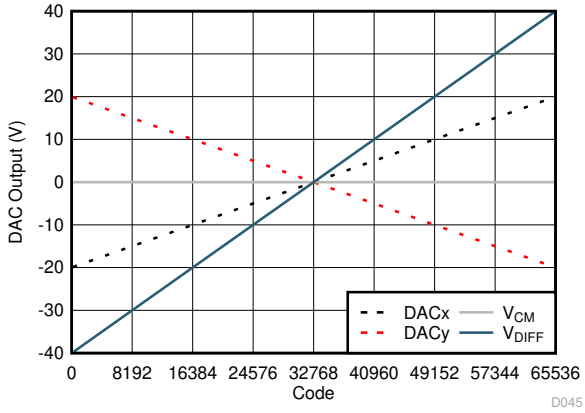

图 8-2. Differential Bipolar Output (16-Bit): ±20-V Output Range

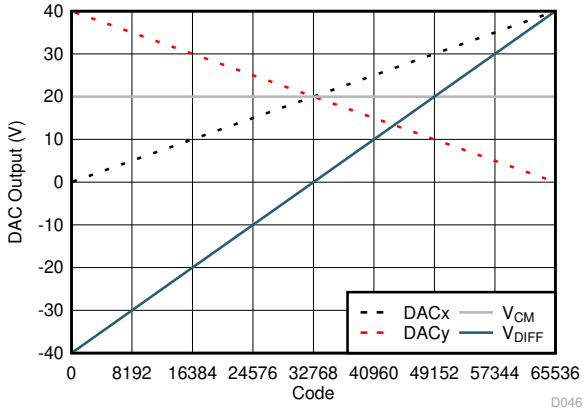

图 8-3. Differential Unipolar Output (16-Bit): 0-V to 40-V Output Range

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8.4.3 Power-Down Mode

The DACx1416 DAC output amplifiers and internal reference power-down status can be individually configured and monitored though the PWDWN registers. Setting a DAC channel in power-down mode disables the output amplifier and clamps the output pin to ground through an internal 10-kΩ resistor.

The DAC data registers are not cleared when the DAC goes into power-down which makes it possible to return to the same output voltage upon return to normal operation. The DAC data registers can also be updated while in power-down mode.

After a power-on or reset event all the DAC channels and the internal reference are in power-down mode. The entire device can be configured into power-down or active modes through the DEV-PWDWN bit.

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8.5 Programming

The DACx1416 family of devices is controlled through a flexible four-wire serial interface that is compatible with SPI type interfaces used on many microcontrollers and DSP controllers. The interface provides access to the DACx1416 registers and can be configured to daisy-chain multiple devices for write operations. The DACx1416 incorporates an optional error checking mode to validate SPI data communication integrity in noisy environments.

8.5.1 Stand-Alone Operation

A serial interface access cycle is initiated by asserting the $\overline{CS}$ pin low. The serial clock SCLK can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. A regular serial interface access cycle is 24 bits long with error checking disabled and 32 bits long with error checking enabled, thus the $\overline{CS}$ pin must stay low for at least 24 or 32 SCLK falling edges. The access cycle ends when the $\overline{CS}$ pin is de-asserted high. If the access cycle contains less than then minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges, only the first 24 or 32 bits are used by the device. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked and the SDO is in a Hi-Z state.

In an error checking disabled access cycle (24-bits long) the first byte input to SDI is the instruction cycle which identifies the request as a read or write command and the 6-bit address to be accessed. The last 16 bits in the cycle form the data cycle.

表 8-2. Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Identifies the communication as a read or write command to the address register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
22	x	Don't care bit.
21-16	A[5:0]	Register address. Specifies the register to be accessed during the read or write operation.
15-0	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[5:0]. If a read command, the data cycle bits are don't care values.

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. Data are clocked out on SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit.

表 8-3. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Echo RW from previous access cycle.
22	x	Echo bit 22 from previous access cycle.
21-16	A[5:0]	Echo address from previous access cycle.
15-0	DO[15:0]	Readback data requested on previous access cycle.

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8.5.1.1 Streaming Mode Operation

Since updating the sixteen channels data registers requires a large amount of data to be passed to the device, the device supports streaming mode. In streaming mode the DAC data registers can be written to the device without providing an instruction command for each data register. Streaming mode is enabled by setting the STR-EN bit. Once enabled the streaming operation is implemented by holding the $\overline{CS}$ active and continuing to shift new data into the device.

The instruction cycle includes the starting address. The device starts writing to this address and automatically increments the address as long as $\overline{CS}$ is asserted. If the last DAC data register address has been reached and $\overline{CS}$ is still asserted, the data for this address is overwritten with the new data.

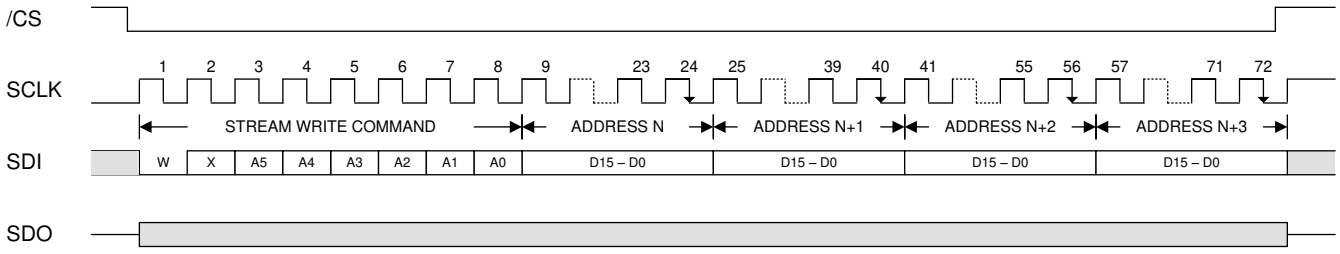

图 8-4. Serial Interface Streaming Cycle

8.5.2 Daisy-Chain Operation

For systems that contain more than one DACx1416 devices, the SDO pin can be used to daisy-chain them together. The SDO pin must be enabled by setting the SDO-EN bit before initiating the daisy-chain operation. Daisy-chain operation is useful in reducing the number of serial interface lines.

The first falling edge on the $\overline{CS}$ pin starts the operation cycle. If more than 24 SCLK pulses are applied while the $\overline{CS}$ pin is kept low, the data ripples out of the shift register and is clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. As a result the total number of clock cycles must be equal to 24 × N, where N is the total number of DACx1416 devices in the daisy chain. When the serial transfer to all devices is complete the $\overline{CS}$ signal is taken high. This action transfers the data from the SPI shift registers to the internal registers of each device in the daisy chain and prevents any further data from being clocked into the input shift register. Daisy-chain operation is not supported while in streaming mode.

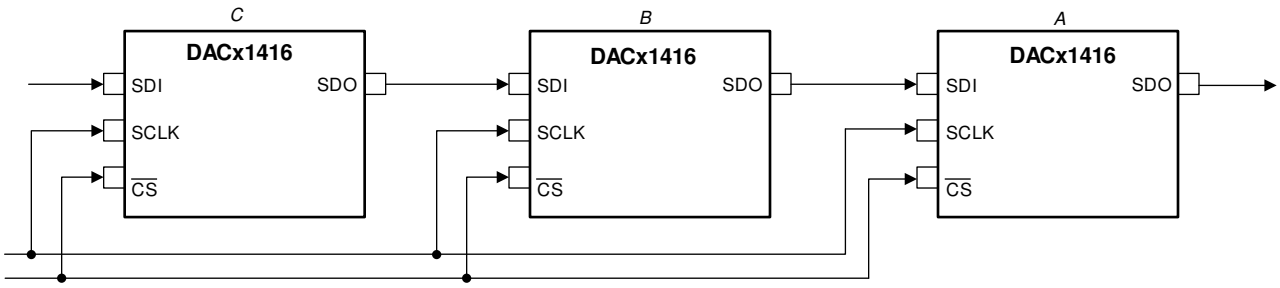

图 8-5. Daisy-Chain Layout

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8.5.3 Frame Error Checking

If the DACx1416 is used in a noisy environment, error checking can be used to check the integrity of SPI data communication between the device and the host processor. This feature is enabled by setting the CRC-EN bit.

The error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, 100000111). When error checking is enabled, the serial interface access cycle width is 32 bits. The normal 24-bit SPI data is appended with an 8-bit CRC polynomial by the host processor before feeding it to the device. In all serial interface readback operations the CRC polynomial is output on the SDO pin as part of the 32-bit cycle.

表 8-4. Error Checking Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
31	RW	Identifies the communication as a read or write command to the address register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
30	CRC-ERROR	Reserved bit. Set to zero.
29-24	A[5:0]	Register address. Specifies the register to be accessed during the read or write operation.
23-8	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[5:0]. If a read command, the data cycle bits are don't care values.
7-0	CRC	8-bit CRC polynomial.

The DACx1416 decodes the 32-bit access cycle to compute the CRC remainder on $\overline{CS}$ rising edges. If no error exists, the CRC remainder is zero and data are accepted by the device.

A write operation failing the CRC check causes the data to be ignored by the device. After the write command, a second access cycle can be issued to determine the error checking results (CRC-ERROR bit) on the SDO pin.

If there is a CRC error, the CRC-ALM bit of the status register is set to 1. The $\overline{ALMOUT}$ pin can be configured to monitor a CRC error by setting the CRCALM-EN bit.

表 8-5. Write Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31	RW	Echo RW from previous access cycle (RW = 0).
30	CRC-ERROR	Returns a 1 when a CRC error is detected, 0 otherwise.
29-24	A[5:0]	Echo address from previous access cycle.
23-8	DO[15:0]	Echo data from previous access cycle.
7-0	CRC	Calculated CRC value of bits 31:8.

A read operation must be followed by a second access cycle to get the requested data on the SDO pin. The error check result (CRC-ERROR bit) from the read command is output on the SDO pin.

As in the case of a write operation failing the CRC check, the CRC-ALM bit of the status register is set to 1 and the $\overline{ALMOUT}$ pin, if configured for CRC alerts, is set low.

表 8-6. Read Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31	RW	Echo RW from previous access cycle (RW = 1).
30	CRC-ERROR	Returns a 1 when a CRC error is detected, 0 otherwise.
29-24	A[5:0]	Echo address from previous access cycle.
23-8	DO[15:0]	Readback data requested on previous access cycle.
7-0	CRC	Calculated CRC value of bits 31:8.

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8.6 Register Maps

表 8-7 lists the memory-mapped registers for the device. All register offset addresses not listed in 表 8-7 should be considered as reserved locations and the register contents should not be modified.

表 8-7. DACx1416 Registers

Offset	Acronym	Register Name	Section
00h	NOP	NOP Register	Go
01h	DEVICEID	Device ID Register	Go
02h	STATUS	Status Register	Go
03h	SPICONFIG	SPI Configuration Register	Go
04h	GENCONFIG	General Configuration Register	Go
05h	BRDCONFIG	Broadcast Configuration Register	Go
06h	SYNCCONFIG	Sync Configuration Register	Go
07h	TOGGCONFIG0	DAC[15:8] Toggle Configuration Register	Go
08h	TOGGCONFIG1	DAC[7:0] Toggle Configuration Register	Go
09h	DACPWDWN	DAC Power-Down Register	Go
0Ah	DACRANGE0	DAC[15:12] Range Register	Go
0Bh	DACRANGE1	DAC[11:8] Range Register	Go
0Ch	DACRANGE2	DAC[7:4] Range Register	Go
0Dh	DACRANGE3	DAC[3:0] Range Register	Go
0Eh	TRIGGER	Trigger Register	Go
0Fh	BRDCAST	Broadcast Data Register	Go
10h	DAC0	DAC0 Data Register	Go
11h	DAC1	DAC1 Data Register	Go
12h	DAC2	DAC2 Data Register	Go
13h	DAC3	DAC3 Data Register	Go
14h	DAC4	DAC4 Data Register	Go
15h	DAC5	DAC5 Data Register	Go
16h	DAC6	DAC6 Data Register	Go
17h	DAC7	DAC7 Data Register	Go
18h	DAC8	DAC8 Data Register	Go
19h	DAC9	DAC9 Data Register	Go
1Ah	DAC10	DAC10 Data Register	Go
1Bh	DAC11	DAC11 Data Register	Go
1Ch	DAC12	DAC12 Data Register	Go
1Dh	DAC13	DAC13 Data Register	Go
1Eh	DAC14	DAC14 Data Register	Go
1Fh	DAC15	DAC15 Data Register	Go
20h	OFFSET0	DAC[14-15;12-13] Differential Offset Register	Go
21h	OFFSET1	DAC[10-11;8-9] Differential Offset Register	Go
22h	OFFSET2	DAC[6-7;4-5] Differential Offset Register	Go
23h	OFFSET3	DAC[2-3;0-1] Differential Offset Register	Go

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Complex bit access types are encoded to fit into small table cells. 表 8-8 shows the codes that are used for access types in this section.

表 8-8. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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8.6.1 NOP Register (Offset = 00h) [reset = 0000h]

NOP is shown in 图 8-6 and described in 表 8-9.

Return to Summary Table.

图 8-6. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
W-0h															

表 8-9. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	W	0h	No operation. Write 0000h for proper no-operation command.

8.6.2 DEVICEID Register (Offset = 01h) [reset = ----h]

DEVICEID is shown in 图 8-7 and described in 表 8-10.

Return to Summary Table.

图 8-7. DEVICEID Register

15	14	13	12	11	10	9	8
DEVICEID							
R----h							
7	6	5	4	3	2	1	0
DEVICEID						VERSIONID	
R----h						R-0h	

表 8-10. DEVICEID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	DEVICEID	R	---h	Device ID DAC81416: 29Ch DAC71416: 28Ch DAC61416: 24Ch
1-0	VERSIONID	R	0h	Version ID. Subject to change.

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8.6.3 STATUS Register (Offset = 02h) [reset = 0000h]

STATUS is shown in 图 8-8 and described in 表 8-11.

Return to Summary Table.

图 8-8. STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CRC-ALM	DAC-BUSY	TEMP-ALM
R-0h					R-0h	R-0h	R-0h

表 8-11. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	This bit is reserved.
2	CRC-ALM	R	0h	CRC-ALM = 1 indicates a CRC error.
1	DAC-BUSY	R	0h	DAC-BUSY = 1 indicates DAC registers are not ready for updates.
0	TEMP-ALM	R	0h	TEMP-ALM = 1 indicates die temperature is over +140°C. A thermal alarm event forces the DAC outputs to go into power-down mode.

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8.6.4 SPICONFIG Register (Offset = 03h) [reset = 0AA4h]

SPICONFIG is shown in 图 8-9 and described in 表 8-12.

Return to Summary Table.

图 8-9. SPICONFIG Register

15	14	13	12	11	10	9	8
RESERVED				TEMPALM-EN	DACBUSY-EN	CRCALM-EN	RESERVED
R-0h				R/W-1h	R/W-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
RESERVED	SOFTTOGGLE-EN	DEV-PWDWN	CRC-EN	STR-EN	SDO-EN	FSDO	RESERVED
R-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R-0h

表 8-12. SPICONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	This bit is reserved.
11	TEMPALM-EN	R/W	1h	When set to 1 a thermal alarm triggers the $\overline{\text{ALMOUT}}$ pin.
10	DACBUSY-EN	R/W	0h	When set to 1 the $\overline{\text{ALMOUT}}$ pin is set between DAC output updates. Contrary to other alarm events, this alarm resets automatically.
9	CRCALM-EN	R/W	1h	When set to 1 a CRC error triggers the $\overline{\text{ALMOUT}}$ pin.
8	RESERVED	R	0h	This bit is reserved.
7	RESERVED	R	1h	This bit is reserved.
6	SOFTTOGGLE-EN	R/W	0h	When set to 1 enables soft toggle operation.
5	DEV-PWDWN	R/W	1h	DEV-PWDWN = 1 sets the device in power-down mode DEV-PWDWN = 0 sets the device in active mode
4	CRC-EN	R/W	0h	When set to 1 frame error checking is enabled.
3	STR-EN	R/W	0h	When set to 1 streaming mode operation is enabled.
2	SDO-EN	R/W	1h	When set to 1 the SDO pin is operational.
1	FSDO	R/W	0h	Fast SDO bit (half-cycle speedup). When 0, SDO updates during SCLK rising edges. When 1, SDO updates during SCLK falling edges.
0	RESERVED	R	0h	This bit is reserved.

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8.6.5 GENCONFIG Register (Offset = 04h) [reset = 7F00h]

GENCONFIG is shown in 图 8-10 and described in 表 8-13.

Return to Summary Table.

图 8-10. GENCONFIG Register

15	14	13	12	11	10	9	8
RESERVED	REF-PWDWN	RESERVED					
R-0h	R/W-1h	R-1h					
7	6	5	4	3	2	1	0
DAC-14-15-DIFF-EN	DAC-12-13-DIFF-EN	DAC-10-11-DIFF-EN	DAC-8-9-DIFF-EN	DAC-6-7-DIFF-EN	DAC-4-5-DIFF-EN	DAC-2-3-DIFF-EN	DAC-0-1-DIFF-EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-13. GENCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	This bit is reserved.
14	REF-PWDWN	R/W	1h	REF-PWDWN = 1 powers down the internal reference REF-PWDWN = 0 activates the internal reference
13-8	RESERVED	R	1h	This bit is reserved.
7	DAC-14-15-DIFF-EN	R/W	0h	When set to 1 the corresponding DAC pair is set to operate in differential mode. The DAC data registers must be rewritten after enabling or disabling differential operation.
6	DAC-12-13-DIFF-EN	R/W	0h	
5	DAC-10-11-DIFF-EN	R/W	0h	
4	DAC-8-9-DIFF-EN	R/W	0h	
3	DAC-6-7-DIFF-EN	R/W	0h	
2	DAC-4-5-DIFF-EN	R/W	0h	
1	DAC-2-3-DIFF-EN	R/W	0h	
0	DAC-0-1-DIFF-EN	R/W	0h	

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8.6.6 BRDCONFIG Register (Offset = 05h) [reset = FFFFh]

BRDCONFIG is shown in 图 8-11 and described in 表 8-14.

Return to Summary Table.

图 8-11. BRDCONFIG Register

15	14	13	12	11	10	9	8
DAC15-BRDCAST-EN	DAC14-BRDCAST-EN	DAC13-BRDCAST-EN	DAC12-BRDCAST-EN	DAC11-BRDCAST-EN	DAC10-BRDCAST-EN	DAC9-BRDCAST-EN	DAC8-BRDCAST-EN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
DAC7-BRDCAST-EN	DAC6-BRDCAST-EN	DAC5-BRDCAST-EN	DAC4-BRDCAST-EN	DAC3-BRDCAST-EN	DAC2-BRDCAST-EN	DAC1-BRDCAST-EN	DAC0-BRDCAST-EN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

表 8-14. BRDCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DAC15-BRDCAST-EN	R/W	1h	When set to 1 the corresponding DAC is set to update its output to the value set in the BRDCAST register. All DAC channels must be configured in single-ended mode for broadcast operation. If one or more outputs are configured in differential mode the broadcast mode is ignored. When cleared to 0 the corresponding DAC output remains unaffected by a BRDCAST command.
14	DAC14-BRDCAST-EN	R/W	1h	
13	DAC13-BRDCAST-EN	R/W	1h	
12	DAC12-BRDCAST-EN	R/W	1h	
11	DAC11-BRDCAST-EN	R/W	1h	
10	DAC10-BRDCAST-EN	R/W	1h	
9	DAC9-BRDCAST-EN	R/W	1h	
8	DAC8-BRDCAST-EN	R/W	1h	
7	DAC7-BRDCAST-EN	R/W	1h	
6	DAC6-BRDCAST-EN	R/W	1h	
5	DAC5-BRDCAST-EN	R/W	1h	
4	DAC4-BRDCAST-EN	R/W	1h	
3	DAC3-BRDCAST-EN	R/W	1h	
2	DAC2-BRDCAST-EN	R/W	1h	
1	DAC1-BRDCAST-EN	R/W	1h	
0	DAC0-BRDCAST-EN	R/W	1h	

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8.6.7 SYNCCONFIG Register (Offset = 06h) [reset = 0000h]

SYNCCONFIG is shown in 图 8-12 and described in 表 8-15.

Return to Summary Table.

图 8-12. SYNCCONFIG Register

15	14	13	12	11	10	9	8
DAC15-SYNC-EN	DAC14-SYNC-EN	DAC13-SYNC-EN	DAC12-SYNC-EN	DAC11-SYNC-EN	DAC10-SYNC-EN	DAC9-SYNC-EN	DAC8-SYNC-EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DAC7-SYNC-EN	DAC6-SYNC-EN	DAC5-SYNC-EN	DAC4-SYNC-EN	DAC3-SYNC-EN	DAC2-SYNC-EN	DAC1-SYNC-EN	DAC0-SYNC-EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-15. SYNCCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DAC15-SYNC-EN	R/W	0h	When set to 1 the corresponding DAC output is set to update in response to an LDAC trigger (synchronous mode). When cleared to 0 the corresponding DAC output is set to update immediately (asynchronous mode).
14	DAC14-SYNC-EN	R/W	0h	
13	DAC13-SYNC-EN	R/W	0h	
12	DAC12-SYNC-EN	R/W	0h	
11	DAC11-SYNC-EN	R/W	0h	
10	DAC10-SYNC-EN	R/W	0h	
9	DAC9-SYNC-EN	R/W	0h	
8	DAC8-SYNC-EN	R/W	0h	
7	DAC7-SYNC-EN	R/W	0h	
6	DAC6-SYNC-EN	R/W	0h	
5	DAC5-SYNC-EN	R/W	0h	
4	DAC4-SYNC-EN	R/W	0h	
3	DAC3-SYNC-EN	R/W	0h	
2	DAC2-SYNC-EN	R/W	0h	
1	DAC1-SYNC-EN	R/W	0h	
0	DAC0-SYNC-EN	R/W	0h	

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8.6.8 TOGGCONFIG0 Register (Offset = 07h) [reset = 0000h]

TOGGCONFIG0 is shown in 图 8-13 and described in 表 8-16.

Return to Summary Table.

图 8-13. TOGGCONFIG0 Register

15	14	13	12	11	10	9	8
DAC15-AB-TOGG-EN		DAC14-AB-TOGG-EN		DAC13-AB-TOGG-EN		DAC12-AB-TOGG-EN	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
DAC11-AB-TOGG-EN		DAC10-AB-TOGG-EN		DAC9-AB-TOGG-EN		DAC8-AB-TOGG-EN	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

表 8-16. TOGGCONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DAC15-AB-TOGG-EN	R/W	0h	Enables toggle mode operation and configures the toggle pin or soft toggle bit: 00 = Toggle mode disabled 01 = Toggle mode enabled: TOGGLE0 10 = Toggle mode enabled: TOGGLE1 11 = Toggle mode enabled: TOGGLE2
13-12	DAC14-AB-TOGG-EN	R/W	0h	
11-10	DAC13-AB-TOGG-EN	R/W	0h	
9-8	DAC12-AB-TOGG-EN	R/W	0h	
7-6	DAC11-AB-TOGG-EN	R/W	0h	
5-4	DAC10-AB-TOGG-EN	R/W	0h	
3-2	DAC9-AB-TOGG-EN	R/W	0h	
1-0	DAC8-AB-TOGG-EN	R/W	0h	

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8.6.9 TOGGCONFIG1 Register (Offset = 08h) [reset = 0000h]

TOGGCONFIG1 is shown in 图 8-14 and described in 表 8-17.

Return to Summary Table.

图 8-14. TOGGCONFIG1 Register

15	14	13	12	11	10	9	8
DAC7-AB-TOGG-EN		DAC6-AB-TOGG-EN		DAC5-AB-TOGG-EN		DAC4-AB-TOGG-EN	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
DAC3-AB-TOGG-EN		DAC2-AB-TOGG-EN		DAC1-AB-TOGG-EN		DAC0-AB-TOGG-EN	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

表 8-17. TOGGCONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DAC7-AB-TOGG-EN	R/W	0h	Enables toggle mode operation and configures the toggle pin or soft toggle bit: 00 = Toggle mode disabled 01 = Toggle mode enabled: TOGGLE0 10 = Toggle mode enabled: TOGGLE1 11 = Toggle mode enabled: TOGGLE2
13-12	DAC6-AB-TOGG-EN	R/W	0h	
11-10	DAC5-AB-TOGG-EN	R/W	0h	
9-8	DAC4-AB-TOGG-EN	R/W	0h	
7-6	DAC3-AB-TOGG-EN	R/W	0h	
5-4	DAC2-AB-TOGG-EN	R/W	0h	
3-2	DAC1-AB-TOGG-EN	R/W	0h	
1-0	DAC0-AB-TOGG-EN	R/W	0h	

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8.6.10 DACPWDWN Register (Offset = 09h) [reset = FFFFh]

DACPWDWN is shown in 图 8-15 and described in 表 8-18.

Return to Summary Table.

图 8-15. DACPWDWN Register

15	14	13	12	11	10	9	8
DAC15-PWDWN	DAC14-PWDWN	DAC13-PWDWN	DAC12-PWDWN	DAC11-PWDWN	DAC10-PWDWN	DAC9-PWDWN	DAC8-PWDWN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
DAC7-PWDWN	DAC6-PWDWN	DAC5-PWDWN	DAC4-PWDWN	DAC3-PWDWN	DAC2-PWDWN	DAC1-PWDWN	DAC0-PWDWN
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

表 8-18. DACPWDWN Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DAC15-PWDWN	R/W	1h	When set to 1 the corresponding DAC is in power-down mode and its output is connected to GND through a 10-kΩ internal resistor.
14	DAC14-PWDWN	R/W	1h	
13	DAC13-PWDWN	R/W	1h	
12	DAC12-PWDWN	R/W	1h	
11	DAC11-PWDWN	R/W	1h	
10	DAC10-PWDWN	R/W	1h	
9	DAC9-PWDWN	R/W	1h	
8	DAC8-PWDWN	R/W	1h	
7	DAC7-PWDWN	R/W	1h	
6	DAC6-PWDWN	R/W	1h	
5	DAC5-PWDWN	R/W	1h	
4	DAC4-PWDWN	R/W	1h	
3	DAC3-PWDWN	R/W	1h	
2	DAC2-PWDWN	R/W	1h	
1	DAC1-PWDWN	R/W	1h	
0	DAC0-PWDWN	R/W	1h	

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8.6.11 DACRANGEn Register (Offset = 0Ah - 0Dh) [reset = 0000h]

DACRANGEn is shown in 图 8-16 and described in 表 8-19.

Return to Summary Table.

图 8-16. DACRANGEn Register

15	14	13	12	11	10	9	8
DACa-RANGE[3:0]				DACb-RANGE[3:0]			
W-0h				W-0h			
7	6	5	4	3	2	1	0
DACc-RANGE[3:0]				DACd-RANGE[3:0]			
W-0h				W-0h			

表 8-19. DACRANGEn Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DACa-RANGE[3:0]	W	0h	Sets the output range for the corresponding DAC. 0000 = 0 to 5 V 0001 = 0 to 10 V 0010 = 0 to 20 V 0100 = 0 to 40 V 1001 = -5 V to +5 V 1010 = -10 V to +10 V 1100 = -20 V to +20 V 1110 = -2.5 V to +2.5 V All others: invalid The two outputs of a differential DAC pair must be configured to the same output range prior to setting them up as a differential pair. a: 15, 11, 7 or 3; b: 14, 10, 6 or 2; c: 13, 9, 5 or 1; d: 12, 8, 4 or 0
11-8	DACb-RANGE[3:0]	W	0h	
7-4	DACc-RANGE[3:0]	W	0h	
3-0	DACd-RANGE[3:0]	W	0h	

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8.6.12 TRIGGER Register (Offset = 0Eh) [reset = 0000h]

TRIGGER is shown in 图 8-17 and described in 表 8-20.

Return to Summary Table.

图 8-17. TRIGGER Register

15	14	13	12	11	10	9	8
RESERVED							ALM-RESET
W-0h							W-0h
7	6	5	4	3	2	1	0
AB-TOG2	AB-TOG1	AB-TOG0	LDAC	SOFT-RESET[3:0]			
W-0h	W-0h	W-0h	W-0h	W-0h			

表 8-20. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	W	0h	This bit is reserved
8	ALM-RESET	W	0h	Set this bit to 1 to clear an alarm event. Not applicable for a DAC-BUSY alarm event.
7	AB-TOG2	W	0h	If soft toggle is enabled set, this bit controls the toggle between values for those DACs that have been set in toggle mode 2 in the TOGGCONFIG register. Set to 1 to update to Register B and clear to 0 for Register A.
6	AB-TOG1	W	0h	If soft toggle is enabled set, this bit controls the toggle between values for those DACs that have been set in toggle mode 1 in the TOGGCONFIG register. Set to 1 to updated to Register B and clear to 0 for Register A.
5	AB-TOG0	W	0h	If soft toggle is enabled set, this bit controls the toggle between values for those DACs that have been set in toggle mode 0 in the TOGGCONFIG register. Set to 1 to update to Register B and clear to 0 for Register A.
4	LDAC	W	0h	Set this bit to 1 to synchronously load those DACs who have been set in synchronous mode in the SYNCCONFIG register.
3-0	SOFT-RESET[3:0]	W	0h	When set to the reserved code 1010 resets the device to its default state.

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8.6.13 BRDCAST Register (Offset = 0Fh) [reset = 0000h]

BRDCAST is shown in 图 8-18 and described in 表 8-21.

Return to Summary Table.

图 8-18. BRDCAST Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRDCAST-DATA[15:0]															
R/W-0h															

表 8-21. BRDCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	BRDCAST-DATA[15:0]	R/W	0h	Writing to the BRDCAST register forces those DAC channels that have been set to broadcast in the BRDCONFIG register to update its data register data to the BRDCAST-DATA one. Data is MSB aligned in straight binary format and follows the format below: DAC81416: { DATA[15:0] } DAC71416: { DATA[13:0], x, x } DAC61416: { DATA[11:0], x, x, x, x} x – Don 't care bits

8.6.14 DACn Register (Offset = 10h - 1Fh) [reset = 0000h]

DACn is shown in 图 8-19 and described in 表 8-22.

Return to Summary Table.

图 8-19. DACn Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DACn-DATA[15:0]															
R/W-0h															

表 8-22. DACn Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DACn-DATA[15:0]	R/W	0h	Stores the 16-, 14- or 12-bit data to be loaded to DACn in MSB aligned straight binary format. In differential DAC mode data is loaded into the lowest-valued DAC in the DAC pair (in pair DAC*xy*, data is loaded into DAC*x* and writes to DAC*y* are ignored). Data follows the format below: DAC81416: { DATA[15:0] } DAC71416: { DATA[13:0], x, x } DAC61416: { DATA[11:0], x, x, x, x} x – Don 't care bits

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8.6.15 OFFSETn Register (Offset = 20h - 23h) [reset = 0000h]

OFFSETn is shown in 图 8-20 and described in 表 8-23.

Return to Summary Table.

图 8-20. OFFSETn Register

15	14	13	12	11	10	9	8
OFFSETab[7:0]							
R/W-0h							
7	6	5	4	3	2	1	0
OFFSETcd[7:0]							
R/W-0h							

表 8-23. OFFSETn Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	OFFSETab[7:0]	R/W	0h	Provides offset adjustment to DAC*y* in the differential DAC*x-y* pair in two 's complement format. Data follows the format below: • DAC81416: – Format: { OFFSET[7:0] } – Range: -128 LSB to +127 LSB • DAC71416: – Format: { OFFSET[5:0], x, x } – Range: -32 LSB to +31 LSB • DAC61416: – Format: { OFFSET[3:0], x, x, x} – Range: -8 LSB to +7 LSB x – Don 't care bits The differential DAC data register must be rewritten after updating the offset register. ab: 14-15, 10-11, 6-7 or 2-3; cd: 12-13, 8-9, 4-5 or 0-1
7-0	OFFSETcd[7:0]	R/W	0h	

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9 Application and Implementation

Note

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9.1 Application Information

One of the primary applications of the DACx1416 family is Mach Zehnder Modulator (MZM) biasing, employed in Optical Line Cards and Optical Modules. With high-voltage, high-current and differential output features, the DACx1416 family can be used for biasing both $LiNbO_3$ and InP type modulators. With the help of the toggle mode and multiple corresponding input pins, the required dither waveform for such applications can be generated without involving SPI programming. The small package size and integrated reference minimize the total footprint of such applications.

9.2 Typical Application

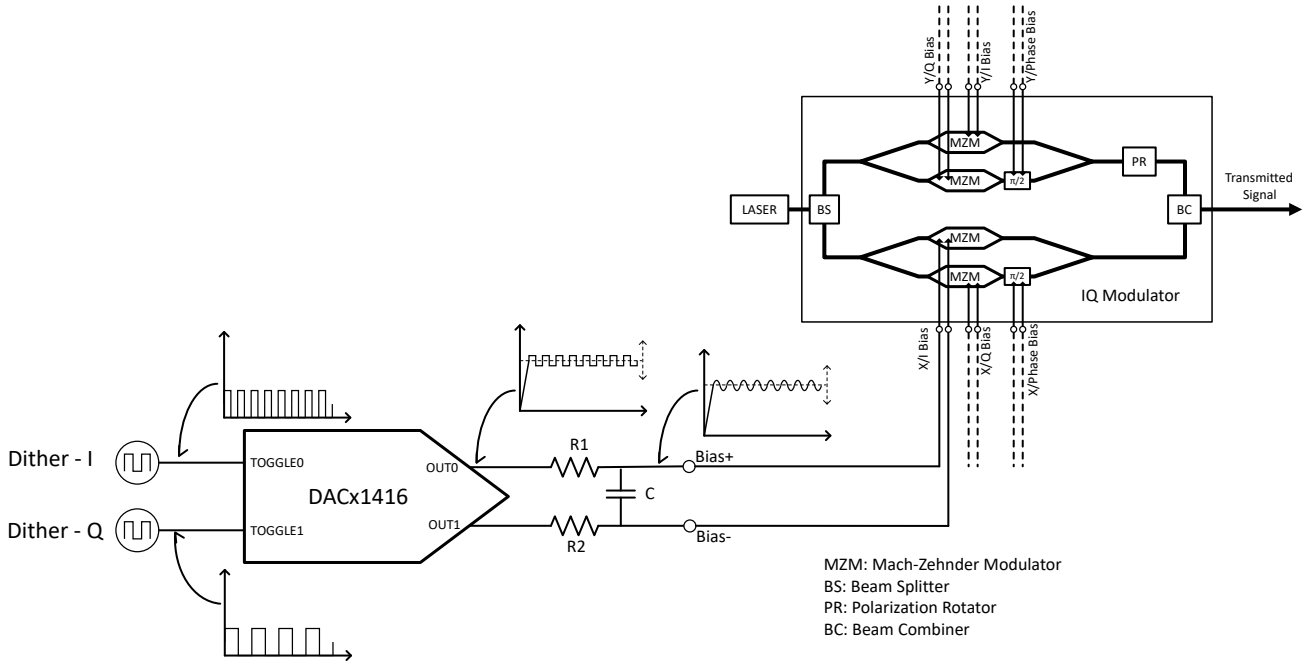

图 9-1. Biasing a Mach Zehnder Modulator

9.2.1 Design Requirements

Designing biasing circuits that are made to match both types of MZM technologies ($LiNbO_3$ and InP) requires high voltage and current ranges as shown in 表 9-1. The Optical Internetworking Forum (OIF) recommends four differential IQ bias and two differential phase bias inputs, as shown in 图 9-1. This differential signaling scheme helps in minimizing the crosstalk and noise between channels, which may otherwise result in a complicated bias control algorithm. While an ideal dither tone should be a sine wave, generating a sine wave can be cumbersome in a largely digital circuit domain. A square wave is relatively easier to generate through digital circuits, and can also be used, provided that the bandwidth of this dither signal is lower than the low cutoff frequency of the receiver (that is, 100 kHz or 1 MHz as per OIF). Passive RC filters with cutoff frequency lower than 100 kHz can be used at the DAC output for $LiNbO_3$ modulators, which have very small bias current requirement. For InP modulators that are mainly used with optical modules, typically requiring a receiver low cutoff frequency of MHz, choose RC values so that the power dissipation across the resistors is small.

For smooth detection of the dither signal at the MZM output, use two orthogonal dither frequency sources for the *I* and *Q* arms. The amplitude of the dither waveform is typically 0.5% to 2.5% of the dc bias voltage, which is mainly governed by the design implementation.

表 9-1. Requirements of MZM Biasing Circuit

PARAMETER	VALUE
DC range	Up to ±18 V
Dither amplitude	40 mV to 500 mV
Dither frequency	100 Hz to 100 kHz
Dither shape	Sine or square
Bias current	Up to 25 mA (for InP MZM)
Number of dither frequencies	2
Output type	Differential (6 pairs)

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9.2.2 Detailed Design Procedure

图 9-1 provides the simplified circuit diagram for biasing a MZM for a *Dither-type Bias Control* circuit. As shown, this cicuit requires four differential input pairs for IQ biasing, and two differential input pairs for phase biasing. To bias a $LiNbO_3$ MZM, the voltage can be as high as ±18 V, whereas the current requirement is of the order of few micro amperes. The low cutoff frequency of the receiver is typically 100 kHz, and hence, the bandwidth of the dither signals should be well below this frequency. Be aware that only the IQ bias inputs require the dither signal, and not the phase bias. The DACx1416 featuresa toggle mode wherein the outputs can be configured to provide a square wave imposed on a dc bias. This mode requires setting the HIGH and LOW codes for the square wave and the transition happens in sync with the selected toggle input pin. The pseudocode to achieve the dither output using the toggle function is provided below.

```
//SYNTAX: WRITE <REGISTER NAME>,<DATA>
//Power-on Device, Disable Soft-toggle
WRITE SPICONFIG,0x0A84
//Select Range for all 12 channels as ±10V
WRITE DACRANGE2, 0xAAAA
WRITE DACRANGE3, 0xAAAA
WRITE DACRANGE4, 0xAAAA
//Power-on DAC Channels 0 - 11
WRITE DACPWDWN,0xF000
//Write HIGH code to Register A of all IQ Bias Differential Pairs
WRITE DAC0,0xXXXX
WRITE DAC2,0xXXXX
WRITE DAC4,0xXXXX
WRITE DAC6,0xXXXX
//Write Data to Phase Bias Channels
WRITE DAC8,0xXXXX
WRITE DAC10,0xXXXX
//Enable Sync for All Differential Pairs
WRITE SYNCCONFIG,0x0FFF
//Enable Software LDAC
WRITE TRIGGER,0x0002
//Write LOW code to Register B of all IQ Bias Differential Pairs
WRITE DAC_DATA0,0xXXXX
WRITE DAC_DATA0,0xXXXX
WRITE DAC_DATA0,0xXXXX
WRITE DAC_DATA0,0xXXXX
//Turn Toggle Mode ON for All IQ Differential Pairs
//DAC11-10:Y/Phase Bias , DAC9-8:Y/I Bias - TOGG0, DAC7-6:Y/Q Bias - TOGG 1
//DAC5-4:Y/Phase Bias , DAC3-2:Y/I Bias - TOGG0, DAC1-0:Y/Q Bias - TOGG 1
WRITE TOGGCONFIG0,0x0005
WRITE TOGGCONFIG1,0xA05A
//Method to Modify the DC Value of Any IQ Differential Pair
//Turn Off Toggle Mode for that Channel (e.g. DAC0-1)
WRITE TOGGCONFIG1,0xA050
//Turn Off Sync for the Channel
WRITE SYNCCONFIG,0x0FFC
//Write HIGH code to Register A of the Channel Pair
WRITE DAC0,0xXXXX
//Turn On Sync for the Channel Pair
WRITE SYNCCONFIG,0x0FFF
//Turn On Toggle for the Channel Pair
WRITE TOGGCONFIG1,0xA05A
```

The dither frequencies can be set at 1 kHz and 2 kHz so that a single-pole RC low-pass filter can provide sufficient attenuation at 100 kHz. For example, when R1 = R2 = 10 kΩ and C = 0.01 µF, an attenuation of approximately 40 dB is obtained at 100 kHz.

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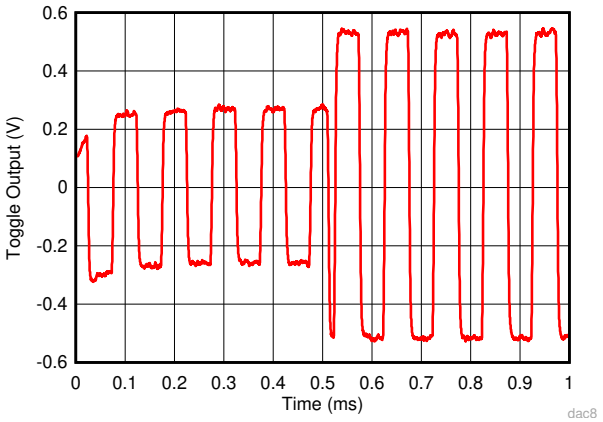
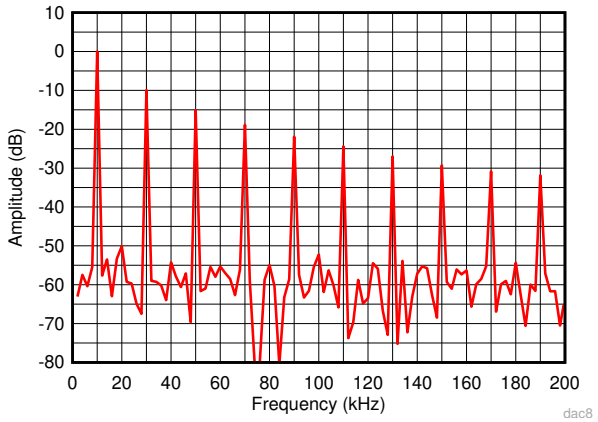
9.2.3 Application Curves



Toggle frequency = 10 kHz

图 9-2. Toggle AC Amplitude Transition



Toggle frequency = 10 kHz, no filter at output

图 9-3. Frequency Spectrum of Toggle Output

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10 Power Supply Recommendations

The DACx1416 require five power supply inputs: VIO, VDD, VAA, VCC and VSS. VDD and VAA should be at same level. Assuming VIO and VDD/VAA to be different, there are four separate power-supply sources required.

Place a 0.1-µF ceramic capacitor close to each power-supply pin. Be aware that VCC and VSS have two pins each. In addition, a 4.7-µF or 10-µF bulk capacitor is recommended for each power supply; tantalum or aluminum types can be chosen for the bulk capacitors.

There is no sequencing requirement for the power supplies. As the DAC output range is configurable, make sure that the power-supplies have enough headroom to achieve linearity at codes close to the power supply rails. When sourcing or sinking current from or to the DAC output, the heat dissipation must be considered. For example, a typical application of MZM bias with 25-mA load current from or to 12 channels with 2.5-V power-supply headroom can create a power dissipation across the DAC of (12 × 2.5 × 25 mA) = 0.75 W. The thermal design to dissipate the power in this example may involve inclusion of heat sinks in order to avoid thermal shutdown of the device.

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11 Layout

11.1 Layout Guidelines

The pin configuration of the DACx1416 has been designed in such a way that the analog, digital, and power pins are spatially separated from each other, which makes the PCB layout simple. An example layout is shown in 图 11-1. As evident, every power supply pin has a 0.1-µF capacitor close to the pin. Make sure to lay out the analog and digital signals away from each other, or on different PCB layers. Make sure to provide an unbroken reference plane (either ground or VIO) for the digital signals. The higher frequency signals, such as SCLK and SDI, must have appropriate impedance termination in order to address signal integrity.

11.2 Layout Example

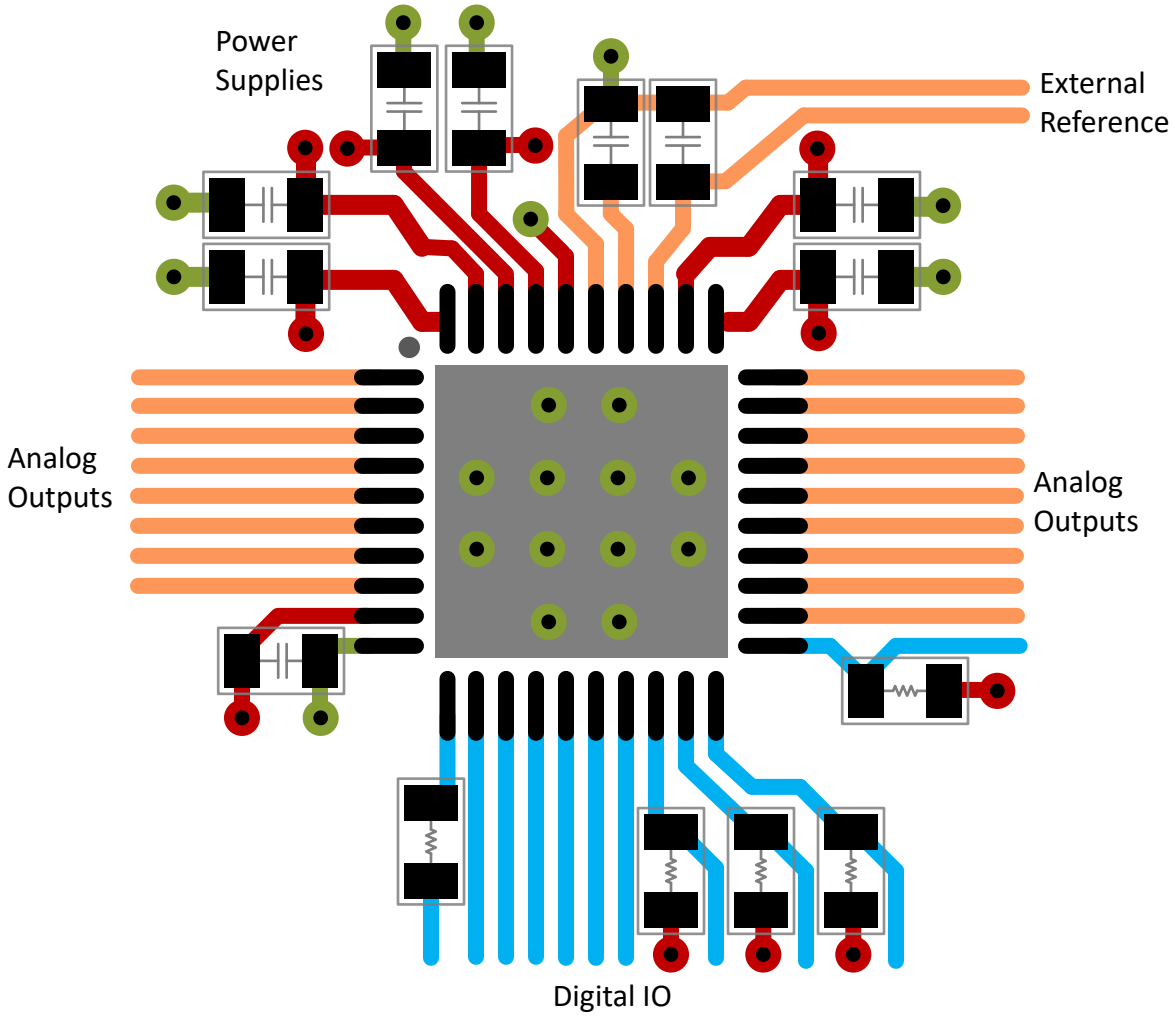

图 11-1. Example Layout

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For development support, see the following: DAC81416 Evaluation Module

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, DAC81416EVM User's Guide
- Texas Instruments, *DACx1416 Delivers Optimized Solution to Mach Zehnder Modulator Biasing* application note
- Texas Instruments, *Programmable Voltage Output With Sense Connections Circuit* application note

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12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC61416RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC61416	Samples
DAC61416RHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC61416	Samples
DAC71416RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC71416	Samples
DAC71416RHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC71416	Samples
DAC81416RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC81416	Samples
DAC81416RHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	DAC81416	Samples

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(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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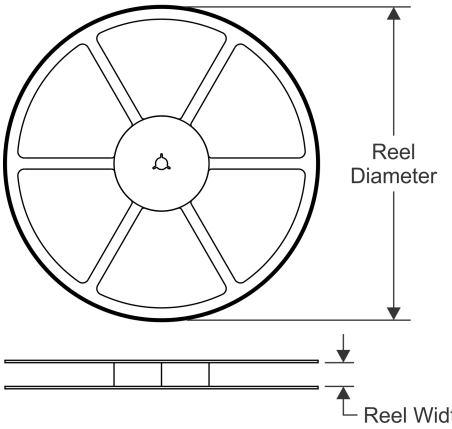
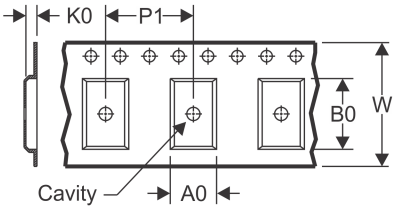
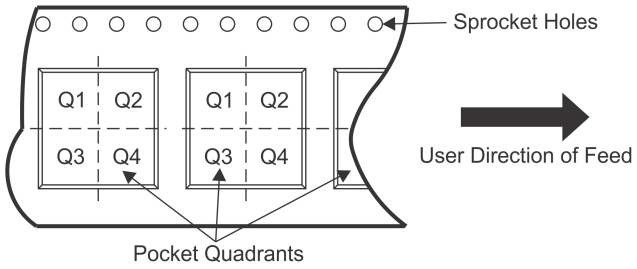


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

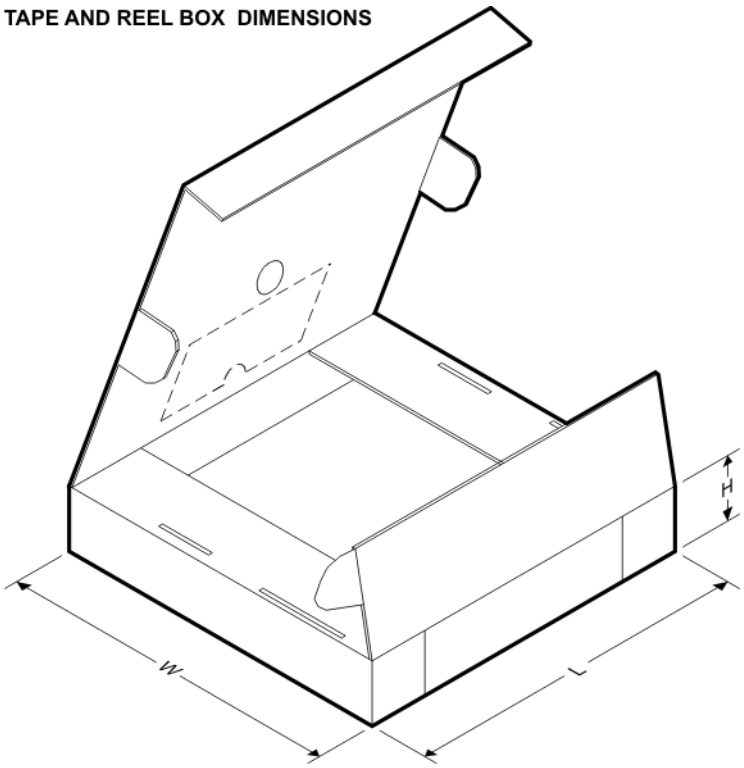
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC61416RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1
DAC61416RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1
DAC71416RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1
DAC71416RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1
DAC81416RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1
DAC81416RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC61416RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC61416RHAT	VQFN	RHA	40	250	213.0	191.0	35.0
DAC71416RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC71416RHAT	VQFN	RHA	40	250	213.0	191.0	35.0
DAC81416RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC81416RHAT	VQFN	RHA	40	250	213.0	191.0	35.0

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