

# 具有精密内部基准的 DACx0502 双通道 16 位、14 位和 12 位 1LSB INL 电压输出 DAC

## 1 特性

- 16 位性能：1LSB INL 和 DNL（最大值）
- 低毛刺脉冲能量：4nV-s
- 宽电源电压范围：2.7V 至 5.5V
- 缓冲输出范围：5V、2.5V 或 1.25V
- 低功耗：1mA/通道 (5.5V)
- 集成 5ppm/°C（最大值）、2.5V 精密基准
- 引脚可选串行接口
  - 3 线制，兼容 SPI，高达 50MHz
  - 两线制，兼容 I<sup>2</sup>C
- 上电复位：零电平或中间电平
- VDD = 5.5V 时的 V<sub>IH</sub> 为 1.62V
- 温度范围：-40°C 至 +125°C
- 封装：微型 10 引脚 WSON

## 2 应用

- 示波器 (DSO)
- 电池测试
- 半导体测试
- 数据采集 (DAQ)
- LCD 测试
- 小型蜂窝基站
- 模拟输出模块
- 过程分析 (pH、气体、浓度、力和湿度)
- 直流电源、交流电源、电子负载

## 3 说明

16 位 DAC80502、14 位 DAC70502 和 12 位 DAC60502 (DACx0502) 数模转换器 (DAC) 均为具有电压输出的高精度、低功耗器件。

DACx0502 线性度小于 1LSB。凭借高精度和微型封装特性，DACx0502 非常适合以下应用：增益和失调电压校准、电流或电压设置点设定和电源控制。这些器件包括一个 2.5V、5ppm/°C 内部基准，可提供 1.25V、2.5V 或 5V 的满量程输出电压范围。DACx0502 采用了上电复位电路，可确保 DAC 输出根据 RSTSEL 引脚的状态以零电平或中间电平上电，并在向器件写入有效代码之前一直保持该电平。

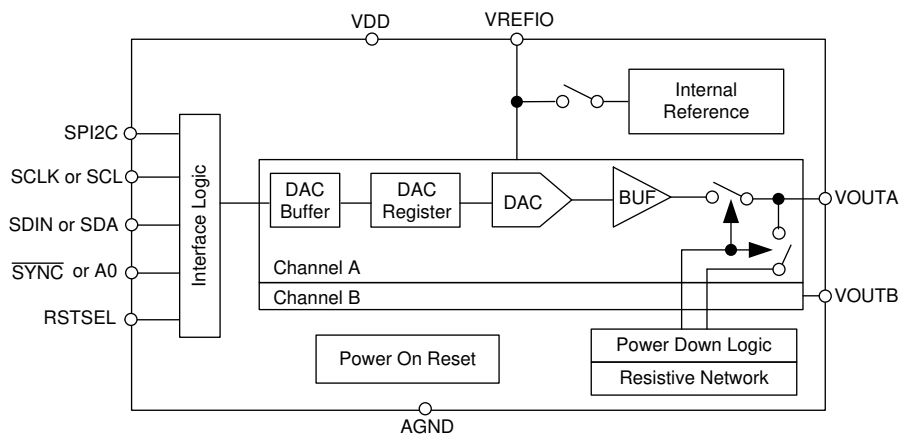
DACx0502 的数字接口可通过 SPI2C 引脚配置为 SPI 或 I<sup>2</sup>C 模式。在 SPI 模式下，DACx0502 使用一个在高达 50MHz 的时钟频率下运行的通用 3 线制串行接口。在 I<sup>2</sup>C 模式下，DACx0502 支持标准 (100kbps)、快速 (400kbps) 和快速+ (1.0Mbps) 工作模式。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
DAC80502	WSON (10)	2.50mm x 2.50mm
DAC70502		
DAC60502		

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

功能方框图



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## 4 修订历史记录

### Changes from Original (November 2019) to Revision A

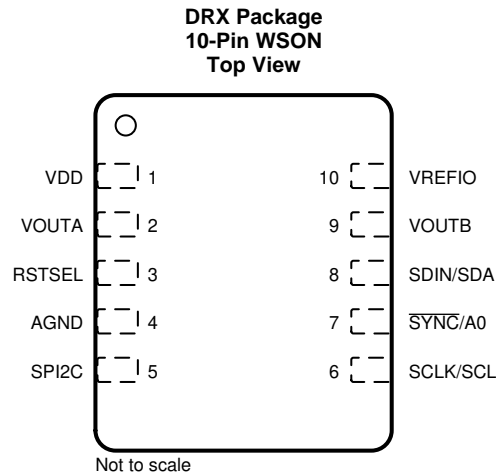
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- 已更改 将器件从“预告信息（预发布）”更改为“生产数据（正在供货）”..... **1**

## 5 Device Comparison Table

DEVICE	RESOLUTION	REFERENCE
DAC80502	16-bit	Internal (default) or external
DAC70502	14-bit	Internal (default) or external
DAC60502	12-bit	Internal (default) or external

## 6 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	4	Ground	Ground reference point for all circuitry on the device
RSTSEL	3	Input	Reset select pin. DACs power up to zero scale if RSTSEL = AGND. DACs power up to midscale if RSTSEL = VDD
SCLK/SCL	6	Input	Serial interface clock. SPI or I <sup>2</sup> C mode.
SDIN/SDA	8	Input/Output	SPI mode: Serial interface data input. Data are clocked into the input shift register on each falling edge of the SCLK pin. I <sup>2</sup> C mode: Data are clocked into or out of the input register. This pin is a bidirectional, SDA drain data line that must be connected to the supply voltage with an external pull-up resistor.
SPI2C	5	Input	Interface select pin. The SPI2C pin must be kept static after device powers up. If SPI2C = 0, the digital interface is in SPI mode If SPI2C = 1, the digital interface is in I <sup>2</sup> C mode
$\overline{\text{SYNC/A0}}$	7	Input	SPI mode: Active low serial data enable. This input is the frame-synchronization signal for the serial data. When the signal goes low, the serial interface input shift register is enabled. I <sup>2</sup> C mode: Four-state address input.
VDD	1	Power	Analog supply voltage (2.7 V to 5.5 V)
VOUTA	2	Output	Analog output voltage from DAC A
VOUTB	9	Output	Analog output voltage from DAC B
VREFIO	10	Input/Output	When using the internal reference, this pin is the reference output voltage pin (default). When operating with an external reference, this pin is the reference input to the device.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage	VDD to AGND	-0.3	6	V
	VREFIO to AGND	-0.3	VDD + 0.3	
	Digital input(s) to AGND	-0.3	VDD + 0.3	
Output voltage	VOU <sub>Tx</sub> to AGND	-0.3	VDD + 0.3	V
Input current	Current into any pin	-10	10	mA
Temperature	Junction temperature (T <sub>J</sub> )	-40	150	°C
	Storage temperature (T <sub>stg</sub> )	-65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
<b>POWER SUPPLY</b>					
VDD to AGND	Positive supply voltage to ground	2.7		5.5	V
<b>DIGITAL INPUTS</b>					
V <sub>IH</sub>	Input high voltage	1.62			V
V <sub>IL</sub>	Input low voltage			0.45	V
<b>REFERENCE INPUT</b>					
VREFIO to AGND	2.7 V ≤ VDD < 3.3 V, reference divider disabled (REF-DIV bit = 0)	1.2		0.5 × (VDD - 0.2)	V
VREFIO to AGND	2.7 V ≤ VDD < 3.3 V, reference divider enabled (REF-DIV bit = 1)	2.4		(VDD - 0.2)	V
VREFIO to AGND	3.3 V ≤ VDD ≤ 5.5 V, reference divider disabled (REF-DIV bit = 0)	1.2		0.5 × VDD	V
VREFIO to AGND	3.3 V ≤ VDD ≤ 5.5 V, reference divider enabled (REF-DIV bit = 1)	2.4		VDD	V
<b>TEMPERATURE</b>					
T <sub>A</sub>	Operating temperature	-40		125	°C

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DACx0502	
		DRX (WSON)	
		10 PINS	
			UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	99.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	49.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	35.9	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.7	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	35.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 7.5 Electrical Characteristics

all minimum and maximum values at T<sub>A</sub> = –40°C to +125°C and all typical values at T<sub>A</sub> = 25°C, 2.7 V ≤ VDD ≤ 5.5 V, external or internal VREFIO = 1.25 V to 5.5 V, R<sub>LOAD</sub> = 2 kΩ to AGND, C<sub>LOAD</sub> = 200 pF to AGND, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC PERFORMANCE</b>						
	Resolution	DAC80502	16			Bits
		DAC70502	14			
		DAC60502	12			
INL	Integral nonlinearity <sup>(1)</sup>		–1		1	LSB
DNL	Differential nonlinearity <sup>(1)</sup>		–1		1	LSB
TUE	Total unadjusted error <sup>(1)</sup>		–0.1	0.04	0.1	%FSR
	Zero code error <sup>(1)</sup>	DAC loaded with zero scale code	–1.5	0.5	1.5	mV
	Zero code error temperature coefficient <sup>(1)</sup>			±2		μV/°C
	Offset error <sup>(1)</sup>		–1.5	0.5	1.5	mV
	Offset error temperature coefficient <sup>(1)</sup>			±2		μV/°C
	Gain error <sup>(1)</sup>		–0.1	0.04	0.1	%FSR
	Gain error temperature coefficient <sup>(1)</sup>			±1		ppm FSR/°C
	Full-scale error <sup>(1)</sup>		–0.1	0.04	0.1	%FSR
	Full-scale error temperature coefficient <sup>(1)</sup>			±2		ppm FSR/°C

(1) End point fit between code 256 to code 64,511 for 16-bit, code 64 to code 16,127 for 14-bit, code 16 to code 4031 for 12-bit, DAC output unloaded, performance under resistive and capacitive load conditions are specified by design and characterization, DAC output range ≥ 2.5 V.

## Electrical Characteristics (continued)

all minimum and maximum values at  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  and all typical values at  $T_A = 25^\circ\text{C}$ ,  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , external or internal  $V_{REFIO} = 1.25\text{ V}$  to  $5.5\text{ V}$ ,  $R_{LOAD} = 2\text{ k}\Omega$  to AGND,  $C_{LOAD} = 200\text{ pF}$  to AGND, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT CHARACTERISTICS</b>						
$V_O$	Output voltage	BUFF-GAIN bit set to 1, REF-DIV bit set to 0	0		$2 \times V_{REFIO}$	V
		BUFF-GAIN bit set to 1, REF-DIV bit set to 1	0		$V_{REFIO}$	
		BUFF-GAIN bit set to 0, REF-DIV bit set to 1	0		$0.5 \times V_{REFIO}$	
$R_{LOAD}$	Resistive load <sup>(2)</sup>	VDD = 2.7 V	0.25			k $\Omega$
		VDD = 5.5 V	0.5			
$C_{LOAD}$	Capacitive load <sup>(2)</sup>	$R_{LOAD} = \text{infinite}$			2	nF
		$R_{LOAD} = 2\text{ k}\Omega$			10	
	Load regulation	DAC at midscale, $-10\text{ mA} \leq I_{OUT} \leq 10\text{ mA}$		80		$\mu\text{V}/\text{mA}$
	Short circuit current	Full scale output shorted to AGND (per channel)		30		mA
		Zero output shorted to VDD (per channel)		30		
	Output voltage headroom	to VDD, DAC at full code, $I_{OUT} = 10\text{ mA}$ (sourcing)	0.3	0.1		V
	Output voltage footroom	to AGND, DAC at zero code, $I_{OUT} = 10\text{ mA}$ (sinking)	0.3			V
$Z_O$	DC small signal output impedance	DAC at midscale		0.1		$\Omega$
		DAC at code 256		10		
		DAC at code 65279		10		
	Power supply rejection ratio (DC)	DAC at midscale; VDD = $5\text{ V} \pm 10\%$		0.15		mV/V
	Output voltage drift vs time	$T_A = 35^\circ\text{C}$ , $V_{OUT} = \text{midscale}$ , 1900 hr		20		ppm of FSR
<b>VOLTAGE REFERENCE INPUT</b>						
$Z_{VREFIO}$	Reference input impedance (VREFIO)			100		k $\Omega$
$C_{VREFIO}$	Reference input capacitance (VREFIO)			5		pF
<b>VOLTAGE REFERENCE OUTPUT</b>						
	Output (initial accuracy)	$T_A = 25^\circ\text{C}$	2.4975		2.5025	V
	Output drift	DAC80502			5	ppm/ $^\circ\text{C}$
		DAC70502, DAC60502			10	
	Output impedance			0.1		$\Omega$
	Output noise	0.1 Hz to 10 Hz		14		$\mu\text{V}_{PP}$
	Output noise density	Measured at 10 kHz, reference load = 10 nF		140		nV/ $\sqrt{\text{Hz}}$
	Load current			$\pm 5$		mA
	Load regulation	Sourcing and sinking		90		$\mu\text{V}/\text{mA}$
	Line regulation			20		$\mu\text{V}/\text{V}$
	Output voltage drift vs time	$T_A = 35^\circ\text{C}$ , 1900 hr		20		$\mu\text{V}$
	Thermal hysteresis	1st cycle		480		ppm
		Additional cycle			25	

(2) Not production tested.

## Electrical Characteristics (continued)

all minimum and maximum values at  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  and all typical values at  $T_A = 25^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$ , external or internal  $\text{VREFIO} = 1.25\text{ V}$  to  $5.5\text{ V}$ ,  $\text{R}_{\text{LOAD}} = 2\text{ k}\Omega$  to AGND,  $\text{C}_{\text{LOAD}} = 200\text{ pF}$  to AGND, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DYNAMIC PERFORMANCE</b>						
$t_s$	Output voltage settling time <sup>(3)</sup>	¼ to ¾ scale and ¾ to ¼ scale settling to $\pm 2$ LSB, VDD = 5.5 V, VREFIO = 2.5 V		5		$\mu\text{s}$
		10-mV settling to $\pm 2$ LSB, VDD = 5.5 V, VREFIO = 2.5 V		3		
	Slew rate <sup>(3)</sup>	VDD = 5.5 V, VREFIO = 2.5 V		2		V/ $\mu\text{s}$
	Power on glitch magnitude	$\text{C}_{\text{LOAD}} = 50\text{ pF}$		200		mV
$V_n$	Output noise <sup>(3)</sup>	0.1 Hz to 10 Hz, DAC at midscale, VDD = 5.5 V, external VREFIO = 2.5 V		14		$\mu\text{V}_{\text{PP}}$
		100-kHz Bandwidth, DAC at midscale, VDD = 5.5 V, external VREFIO = 2.5 V		23		$\mu\text{V}_{\text{rms}}$
$V_n$	Output noise density	Measured at 1 kHz, DAC at midscale, VDD = 5.5 V, external VREFIO = 2.5 V, gain = 2X (BUFF-GAIN bit = 1)		78		nV/ $\sqrt{\text{Hz}}$
		Measured at 10 kHz, DAC at midscale, VDD = 5.5 V, external VREFIO = 2.5 V, gain = 2X (BUFF-GAIN bit = 1)		74		
		Measured at 1 kHz, DAC at full scale, VDD = 2.7 V, external VREFIO = 2.5 V, gain = 1X (BUFF-GAIN bit = 0)		55		
		Measured at 10 kHz, DAC at full scale, VDD = 2.7 V, external VREFIO = 2.5 V, gain = 1X (BUFF-GAIN bit = 0)		50		
SFDR	Spurious free dynamic range	1-kHz sinusoid at DAC output, DAC updated at 500 kHz, include up to 7th harmonics, no filter on DAC output		70		dB
THD	Total harmonic distortion	1-kHz sinusoid at DAC output, DAC updated at 500 kHz, include up to 7th harmonics, no filter on DAC output		70		dB
	Power supply rejection ratio (ac)	200-mV, 50-Hz to 60-Hz sine wave on VDD, DAC at midscale.		85		dB
	Code change glitch impulse	Midcode $\pm 1$ LSB (including feedthrough)		4		nV-s
	Code change glitch magnitude	Midcode $\pm 1$ LSB (including feedthrough) gain = 1X (BUFF-GAIN bit = 0)		7.5		mV
	Channel to channel ac crosstalk	Full scale swing on adjacent channel, measured channel at midscale		4		nV-s
	Channel to channel dc crosstalk	Full scale swing on adjacent channel, measured channel at midscale		1		LSB
	Digital feedthrough	At SCLK = 1 MHz, DAC output at midscale		4		nV-s
<b>DIGITAL INPUTS</b>						
	Hysteresis voltage			0.4		V
	Input current		-5		5	$\mu\text{A}$
	Pin capacitance	Per pin		10		pF

(3) Output buffer in gain = 2X setting (BUFF-GAIN bit = 1).

## Electrical Characteristics (continued)

all minimum and maximum values at  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  and all typical values at  $T_A = 25^\circ\text{C}$ ,  $2.7\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$ , external or internal  $\text{VREFIO} = 1.25\text{ V}$  to  $5.5\text{ V}$ ,  $R_{\text{LOAD}} = 2\text{ k}\Omega$  to AGND,  $C_{\text{LOAD}} = 200\text{ pF}$  to AGND, and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER</b>						
$I_{\text{VDD}}$	Current flowing into VDD	Normal mode, internal reference enabled, all DACs at full scale, SPI static		1.9	2.6	mA
		Normal mode, external reference = 2.5 V, all DACs at full scale, SPI static		1.5	1.9	
		All DACs and Internal reference power-down		15		
$I_{\text{VREFIO}}$	Current flowing into VREFIO	0-V to 5-V range, midscale code		25		$\mu\text{A}$



## 7.6 Timing Requirements : SPI Mode

all input signals are specified with  $t_R = t_F = 1 \text{ ns/V}$  and timed from a voltage level of  $(V_{IL} + V_{IH}) / 2$ .  $2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ ,  $V_{IH} = 1.62 \text{ V}$ ,  $V_{IL} = 0.15 \text{ V}$ ,  $V_{REFIO} = 1.25 \text{ V}$  to  $5.5 \text{ V}$ , and  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$f_{\text{SCLK}}$	SCLK frequency			50	MHz
$t_{\text{SCLKHIGH}}$	SCLK high time	9			ns
$t_{\text{SCLKLOW}}$	SCLK low time	9			ns
$t_{\text{SDIS}}$	SDIN setup	5			ns
$t_{\text{SDIH}}$	SDIN hold	10			ns
$t_{\text{SYNCS}}$	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup	13			ns
$t_{\text{SYNCH}}$	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	10			ns
$t_{\text{SYNCHIGH}}$	$\overline{\text{SYNC}}$ high time	160			ns
$t_{\text{SYNCSIGNORE}}$	SCLK falling edge to $\overline{\text{SYNC}}$ ignore	15			ns
$t_{\text{DACWAIT}}$	Sequential DAC update wait time	1			$\mu\text{s}$

## 7.7 Timing Requirements : I<sup>2</sup>C Standard Mode

all input signals are specified with  $t_R = t_F = 1 \text{ ns/V}$  and timed from a voltage level of  $(V_{IL} + V_{IH}) / 2$ .  $2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ ,  $V_{IH} = 1.62 \text{ V}$ ,  $V_{IL} = 0.45 \text{ V}$ ,  $V_{REFIO} = 1.25 \text{ V}$  to  $5.5 \text{ V}$ , and  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$f_{\text{SCLK}}$	SCL frequency			0.1	MHz
$t_{\text{BUF}}$	Bus free time between stop and start conditions	4.7			$\mu\text{s}$
$t_{\text{HDSTA}}$	Hold time after repeated start	4			$\mu\text{s}$
$t_{\text{SUSTA}}$	Repeated start setup time	4.7			$\mu\text{s}$
$t_{\text{SUSTO}}$	Stop condition setup time	4			$\mu\text{s}$
$t_{\text{HDDAT}}$	Data hold time	0			ns
$t_{\text{SUDAT}}$	Data setup time	250			ns
$t_{\text{LOW}}$	SCL clock low period	4700			ns
$t_{\text{HIGH}}$	SCL clock high period	4000			ns
$t_{\text{R}}$	Clock and data fall time			300	ns
$t_{\text{F}}$	Clock and data rise time			1000	ns
$t_{\text{UPDATE}}$	Sequential DAC update wait time	1			$\mu\text{s}$

## 7.8 Timing Requirements : I<sup>2</sup>C Fast Mode

all input signals are specified with  $t_R = t_F = 1 \text{ ns/V}$  and timed from a voltage level of  $(V_{IL} + V_{IH}) / 2$ .  $2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ ,  $V_{IH} = 1.62 \text{ V}$ ,  $V_{IL} = 0.45 \text{ V}$ ,  $V_{REFIO} = 1.25 \text{ V}$  to  $5.5 \text{ V}$ , and  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$f_{\text{SCLK}}$	SCL frequency			0.4	MHz
$t_{\text{BUF}}$	Bus free time between stop and start conditions	1.3			$\mu\text{s}$
$t_{\text{HDSTA}}$	Hold time after repeated start	0.6			$\mu\text{s}$
$t_{\text{SUSTA}}$	Repeated start setup time	0.6			$\mu\text{s}$
$t_{\text{SUSTO}}$	Stop condition setup time	0.6			$\mu\text{s}$
$t_{\text{HDDAT}}$	Data hold time	0			ns
$t_{\text{SUDAT}}$	Data setup time	100			ns
$t_{\text{LOW}}$	SCL clock low period	1300			ns
$t_{\text{HIGH}}$	SCL clock high period	600			ns
$t_{\text{R}}$	Clock and data fall time			300	ns
$t_{\text{F}}$	Clock and data rise time			300	ns
$t_{\text{UPDATE}}$	Sequential DAC update wait time	1			$\mu\text{s}$

### 7.9 Timing Requirements : I<sup>2</sup>C Fast-Mode Plus

all input signals are specified with  $t_R = t_F = 1 \text{ ns/V}$  and timed from a voltage level of  $(V_{IL} + V_{IH}) / 2$ .  $2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ ,  $V_{IH} = 1.62 \text{ V}$ ,  $V_{IL} = 0.45 \text{ V}$ ,  $V_{REFIO} = 1.25 \text{ V}$  to  $5.5 \text{ V}$ , and  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$f_{SCLK}$	SCL frequency			1	MHz
$t_{BUF}$	Bus free time between stop and start conditions	0.5			$\mu\text{s}$
$t_{HDSTA}$	Hold time after repeated start	0.26			$\mu\text{s}$
$t_{SUSTA}$	Repeated start setup time	0.26			$\mu\text{s}$
$t_{SUSTO}$	Stop condition setup time	0.26			$\mu\text{s}$
$t_{HDDAT}$	Data hold time	0			ns
$t_{SUDAT}$	Data setup time	50			ns
$t_{LOW}$	SCL clock low period	500			ns
$t_{HIGH}$	SCL clock high period	260			ns
$t_R$	Clock and data fall time			120	ns
$t_F$	Clock and data rise time			120	ns
$t_{UPDATE}$	Sequential DAC update wait time	1			$\mu\text{s}$

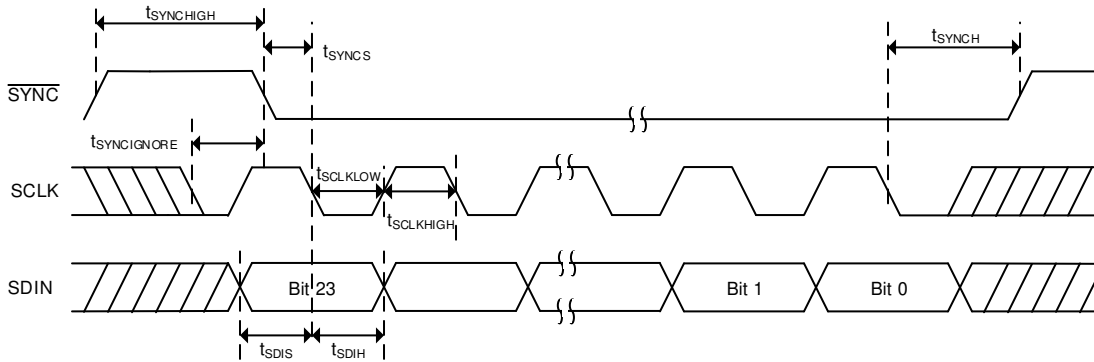


图 1. SPI Mode Timing

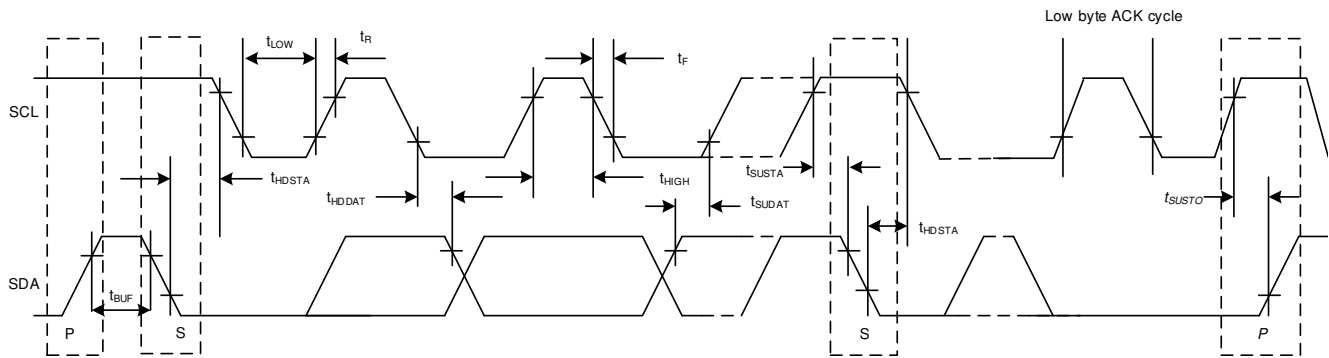


图 2. I<sup>2</sup>C Mode Timing

### 7.10 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , internal reference = 2.5 V, REF-DIV = 0 and BUFF-GAIN = 1, channel A shown, and DAC outputs unloaded (unless otherwise noted)

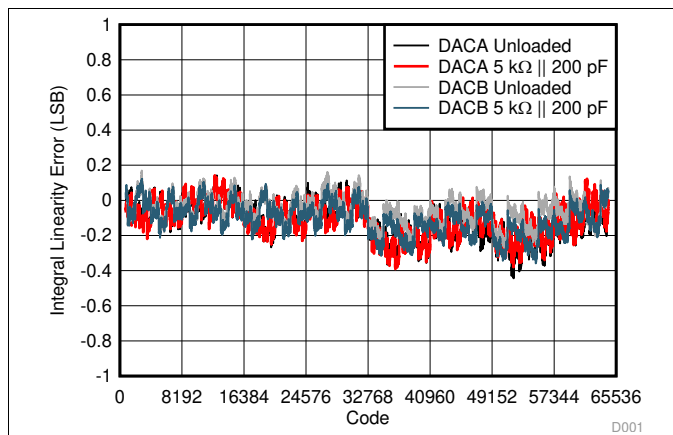


图 3. Integral Linearity Error vs Digital Input Code

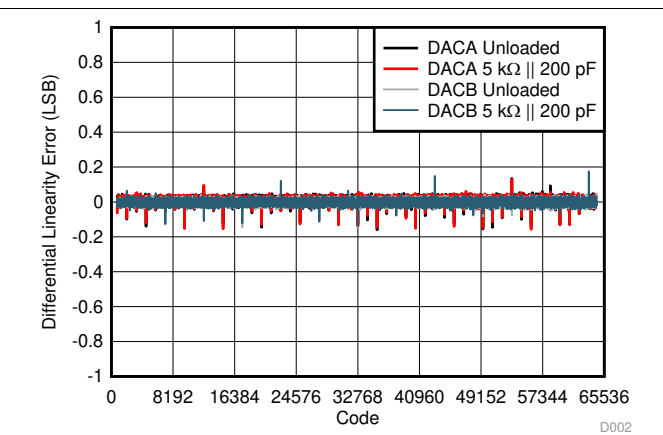


图 4. Differential Linearity Error vs Digital Input Code

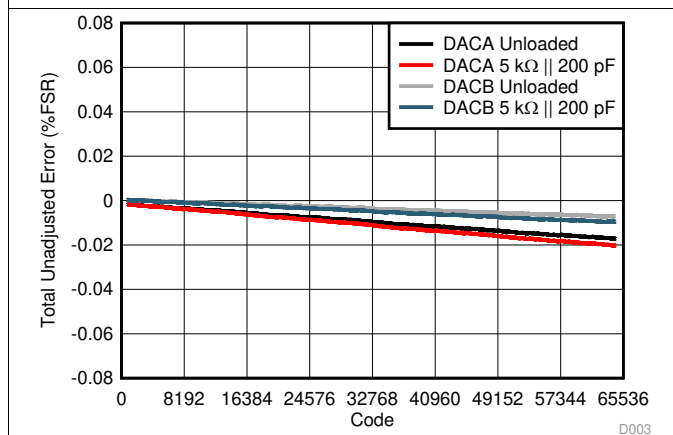


图 5. Total Unadjusted Error vs Digital Input Code

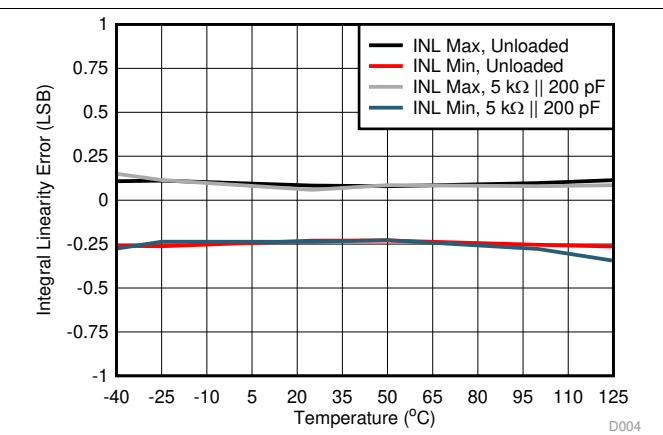


图 6. Integral Linearity Error vs Temperature

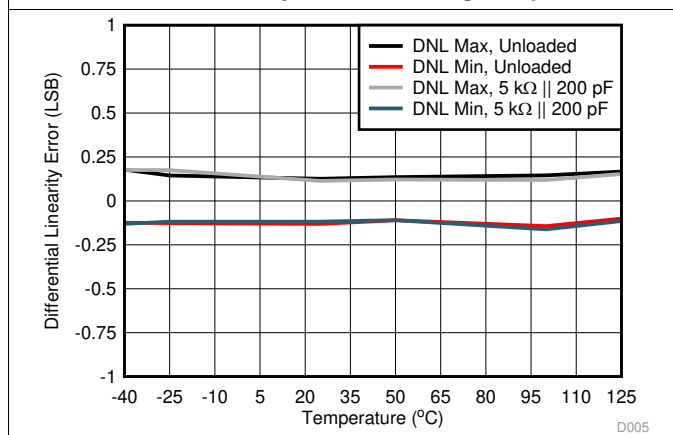


图 7. Differential Linearity Error vs Temperature

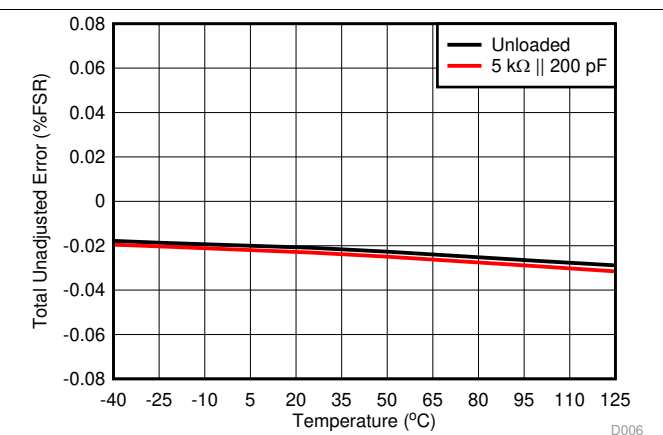


图 8. Total Unadjusted Error vs Temperature

### Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , internal reference = 2.5 V, REF-DIV = 0 and BUFF-GAIN = 1, channel A shown, and DAC outputs unloaded (unless otherwise noted)

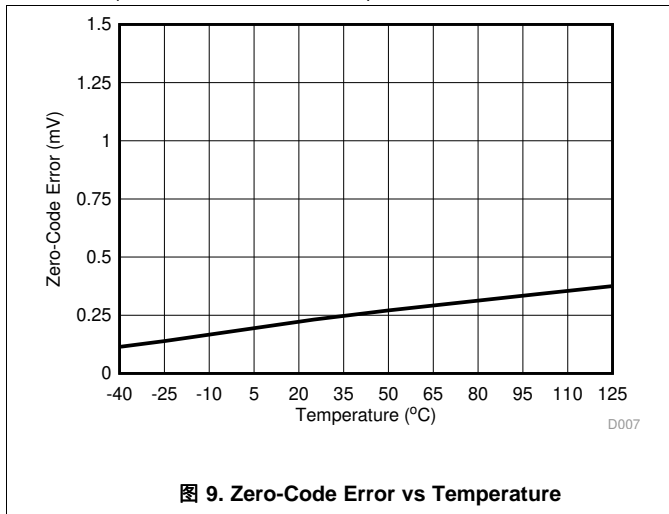


图 9. Zero-Code Error vs Temperature

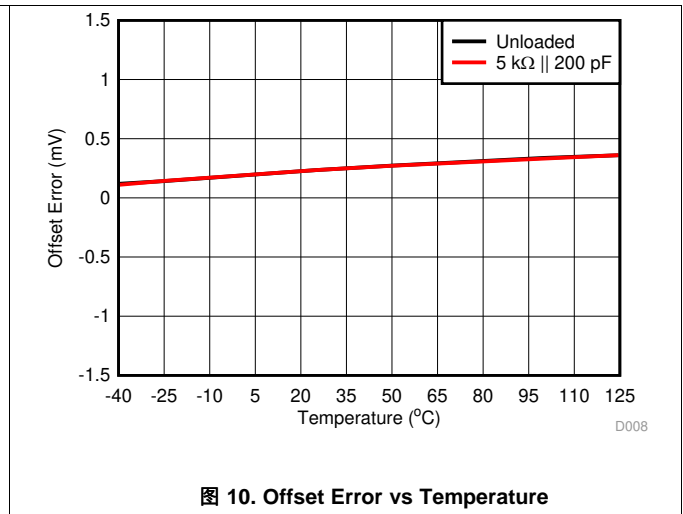


图 10. Offset Error vs Temperature

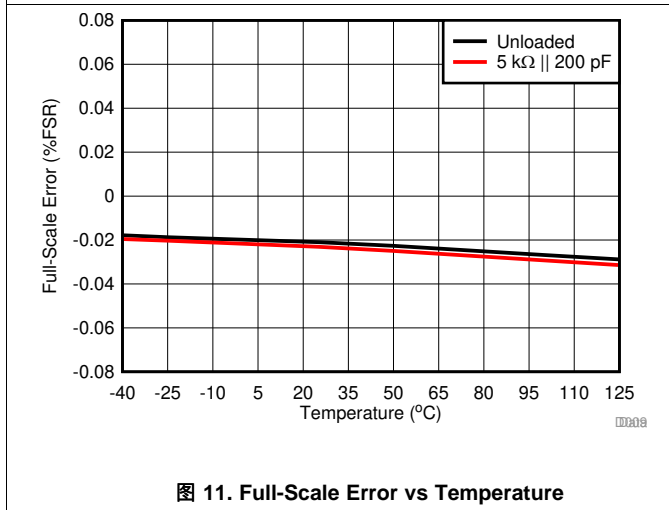


图 11. Full-Scale Error vs Temperature

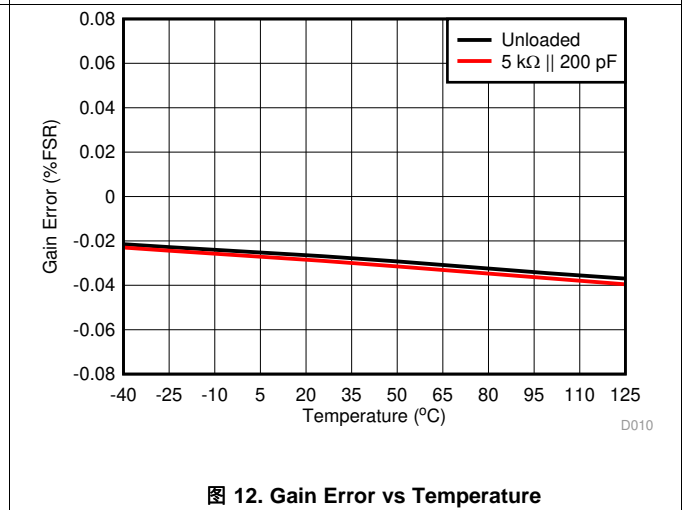


图 12. Gain Error vs Temperature

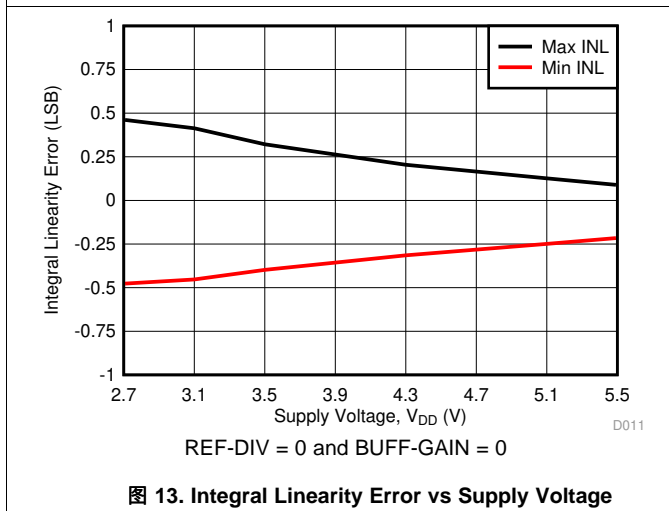


图 13. Integral Linearity Error vs Supply Voltage

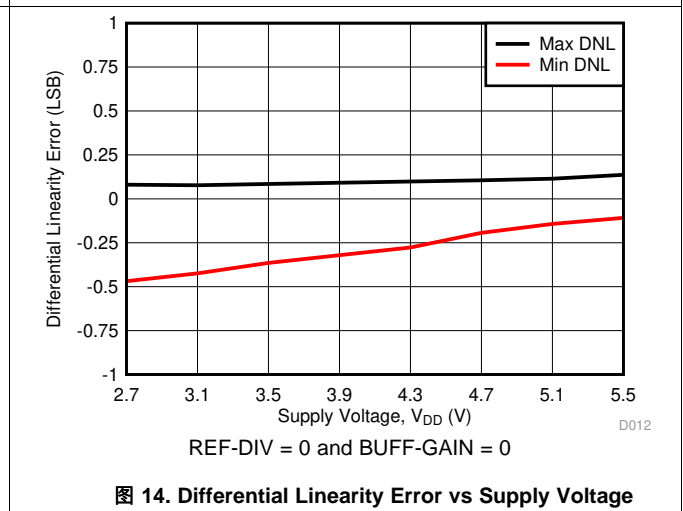
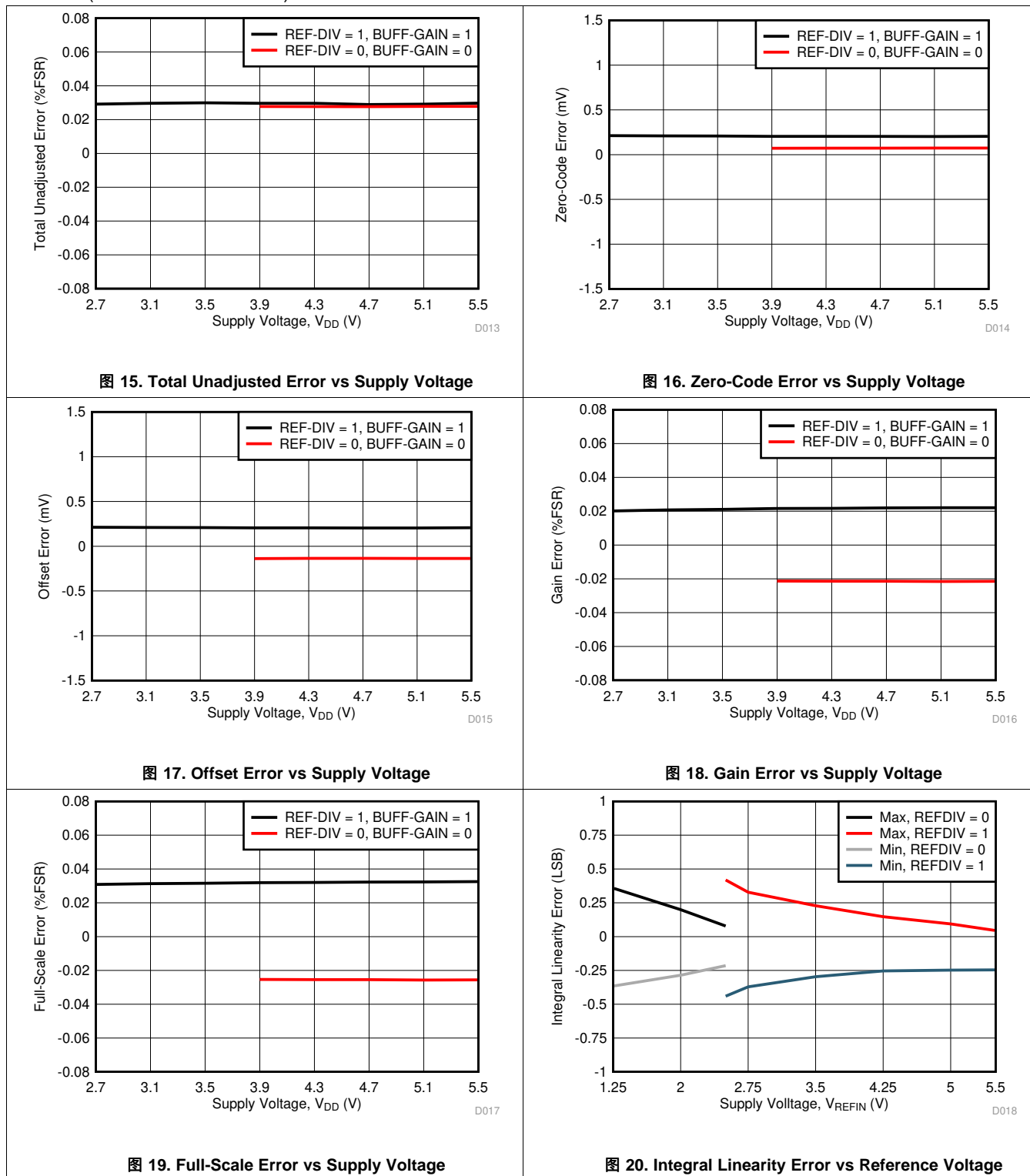


图 14. Differential Linearity Error vs Supply Voltage

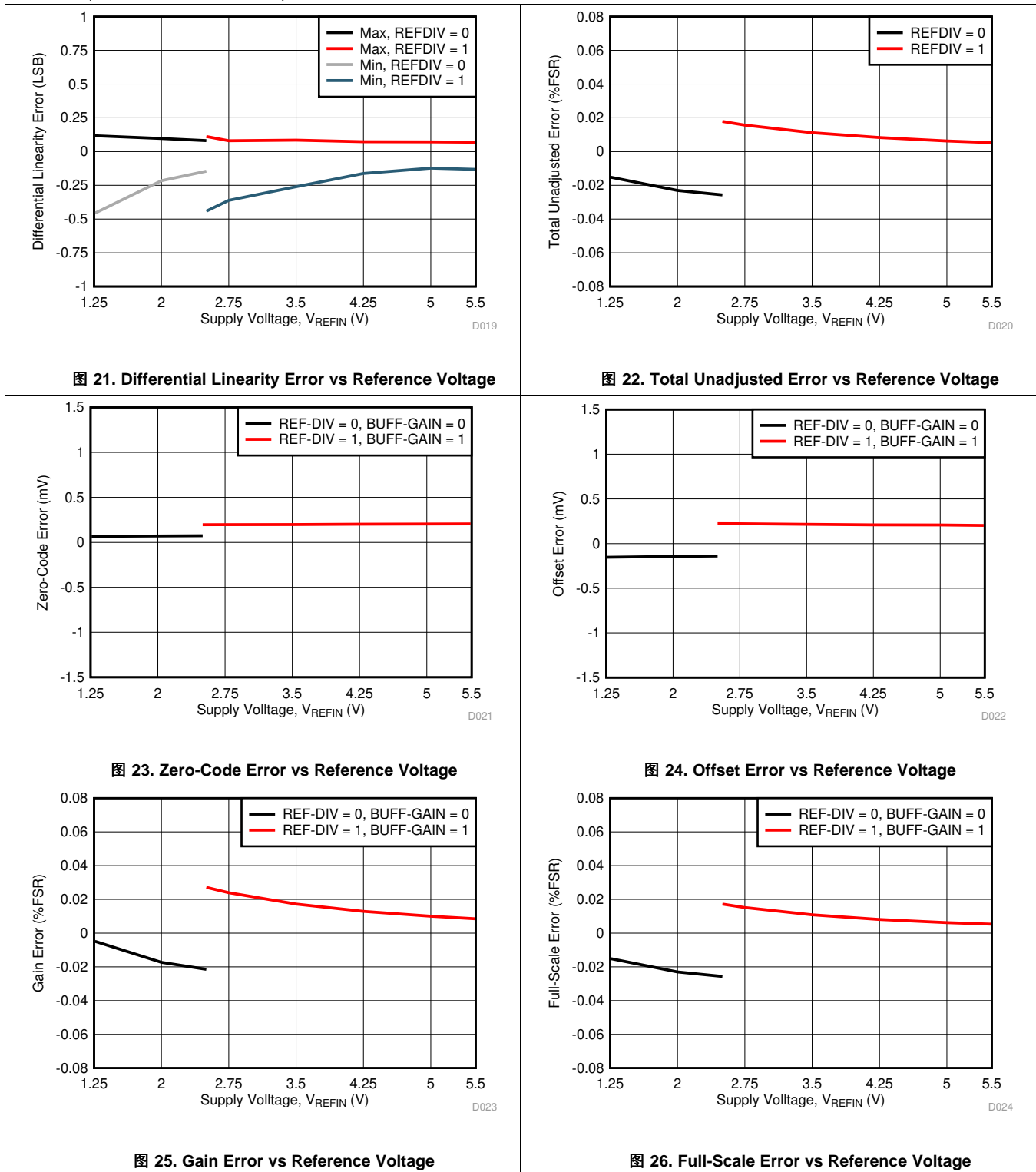
Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , internal reference = 2.5 V, REF-DIV = 0 and BUFF-GAIN = 1, channel A shown, and DAC outputs unloaded (unless otherwise noted)



## Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , internal reference = 2.5 V, REF-DIV = 0 and BUFF-GAIN = 1, channel A shown, and DAC outputs unloaded (unless otherwise noted)



Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , internal reference = 2.5 V, REF-DIV = 0 and BUFF-GAIN = 1, channel A shown, and DAC outputs unloaded (unless otherwise noted)

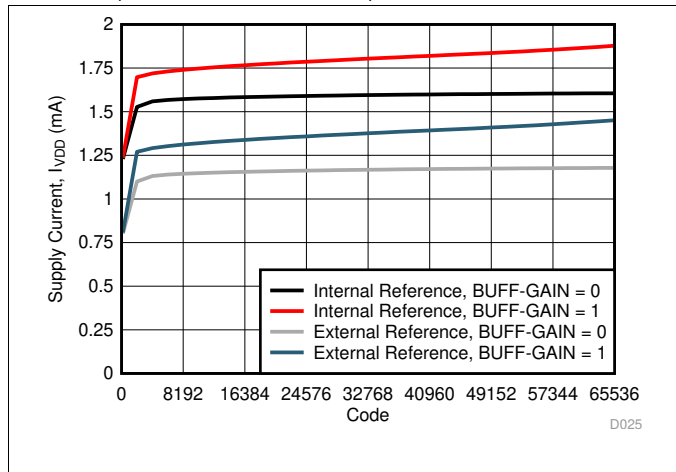


图 27. Supply Current vs Digital Input Code

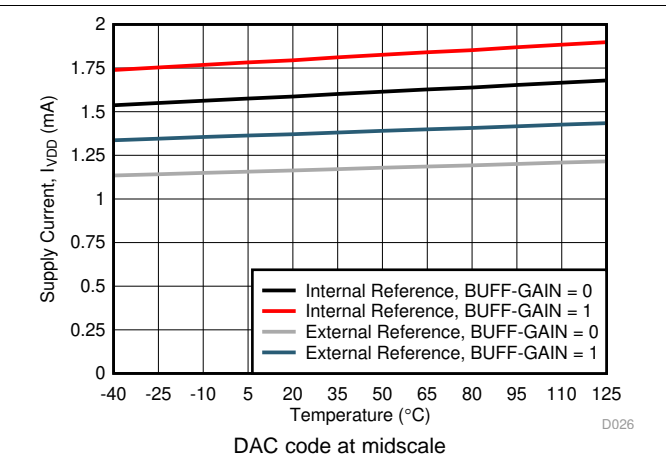


图 28. Supply Current vs Temperature

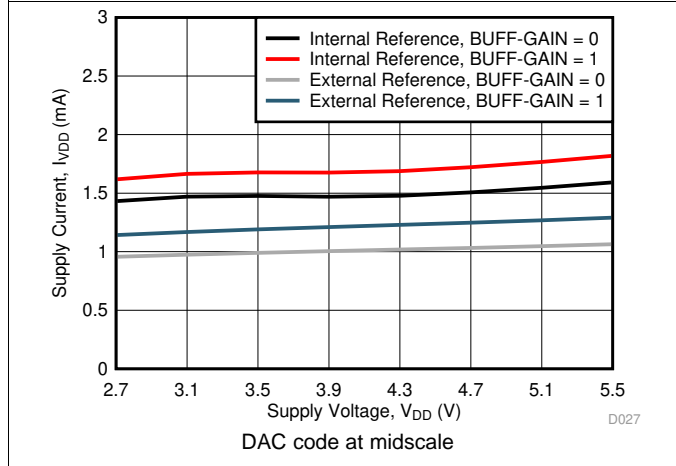


图 29. Supply Current vs Supply Voltage

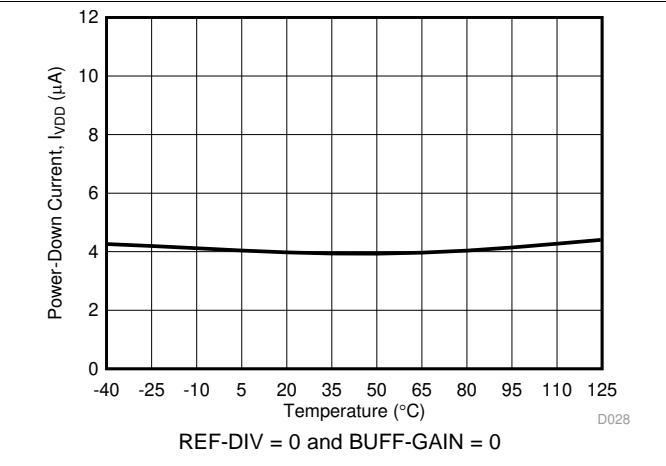


图 30. Power-Down Current vs Temperature

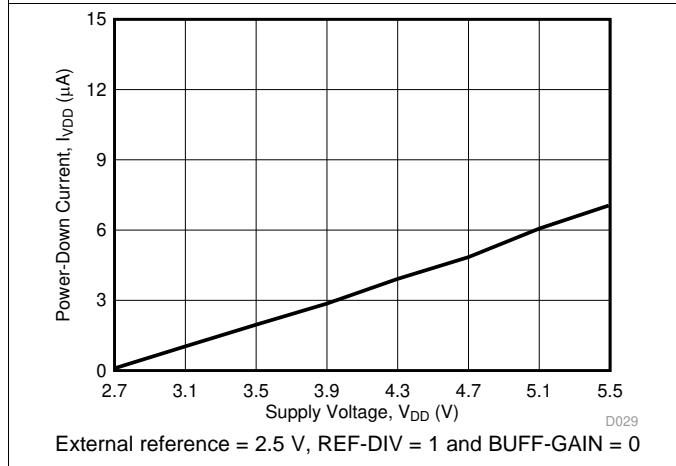


图 31. Power Down Current vs Supply Voltage

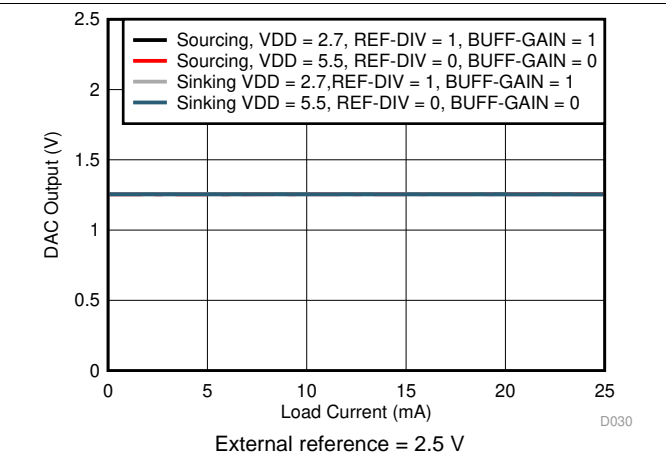


图 32. Headroom and Footroom vs Load Current

Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , internal reference = 2.5 V, REF-DIV = 0 and BUFF-GAIN = 1, channel A shown, and DAC outputs unloaded (unless otherwise noted)

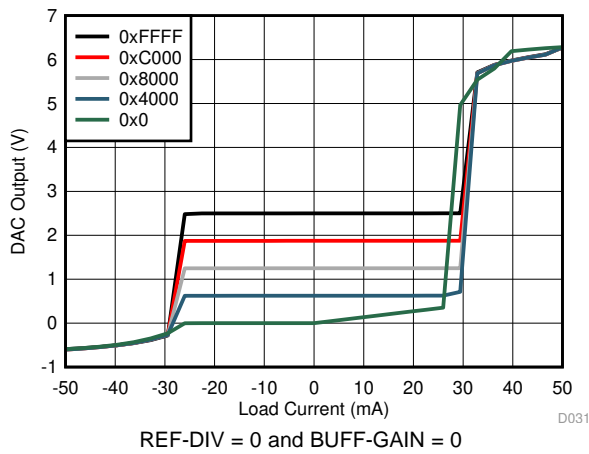


图 33. Source and Sink Capability

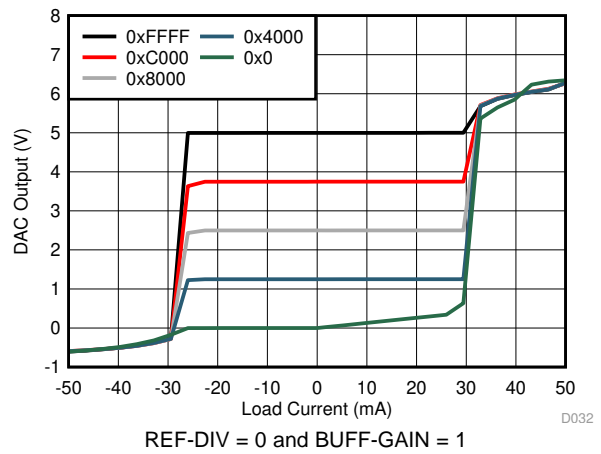


图 34. Source and Sink Capability

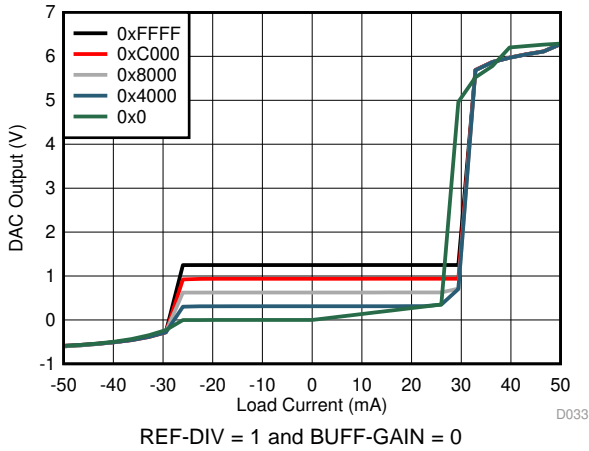
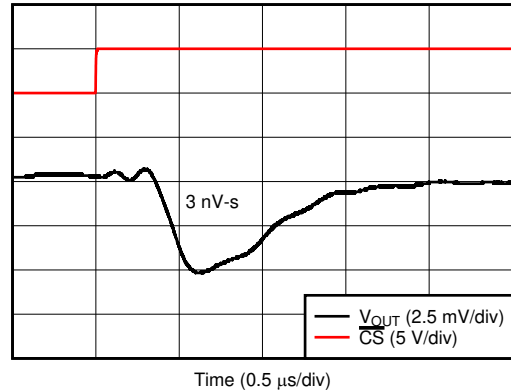
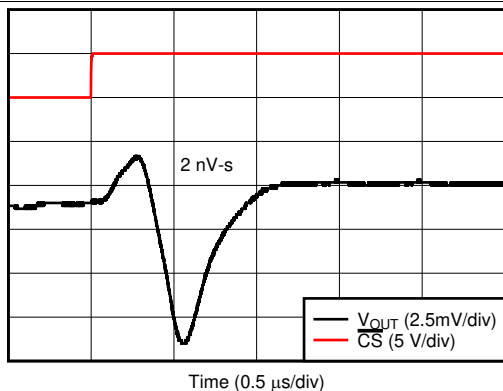


图 35. Source and Sink Capability



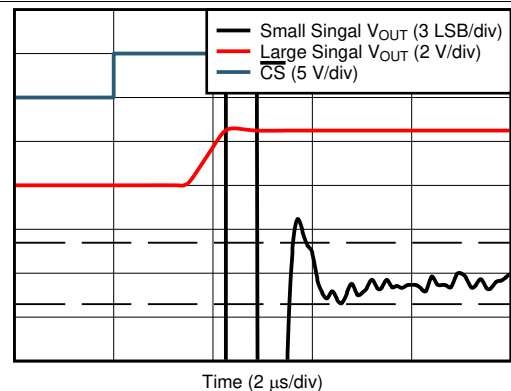
DAC code transition from midscale – 1 to midscale LSB, REF-DIV = 0 and BUFF-GAIN = 0

图 36. Glitch Impulse, Rising Edge, 1-LSB Step



DAC code transition from midscale to midscale – 1 LSB, REF-DIV = 0 and BUFF-GAIN = 0

图 37. Glitch Impulse, Falling Edge, 1-LSB Step



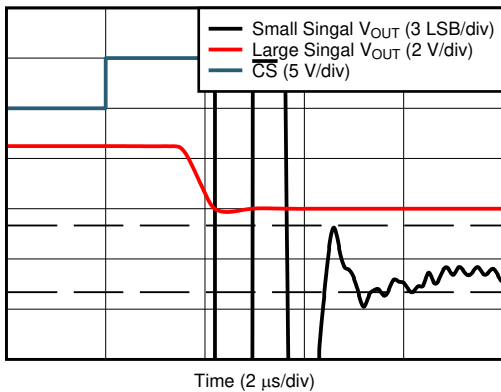
REF-DIV = 0 and BUFF-GAIN = 0

图 38. Full-Scale Settling Time, Rising Edge



Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , internal reference = 2.5 V, REF-DIV = 0 and BUFF-GAIN = 1, channel A shown, and DAC outputs unloaded (unless otherwise noted)

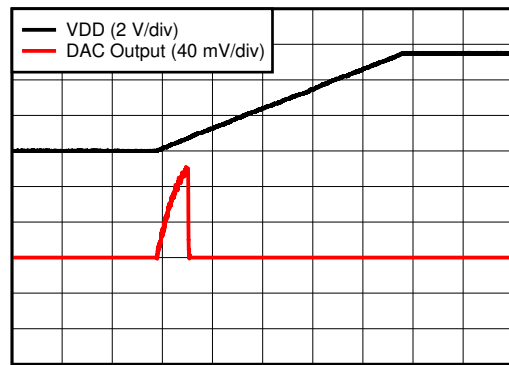


Time (2  $\mu\text{s}/\text{div}$ )

D037

REF-DIV = 0 and BUFF-GAIN = 0

图 39. Full-Scale Settling Time, Falling Edge

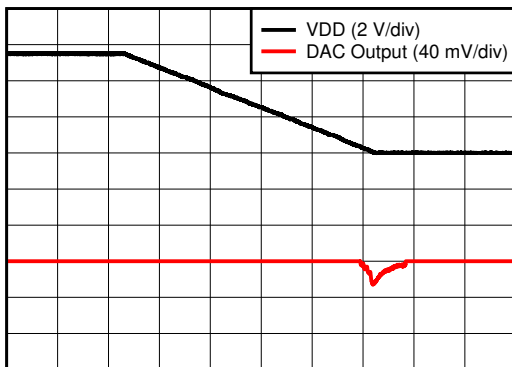


Time (1 ms/div)

D038

REF-DIV = 0 and BUFF-GAIN = 0

图 40. Power-On Glitch

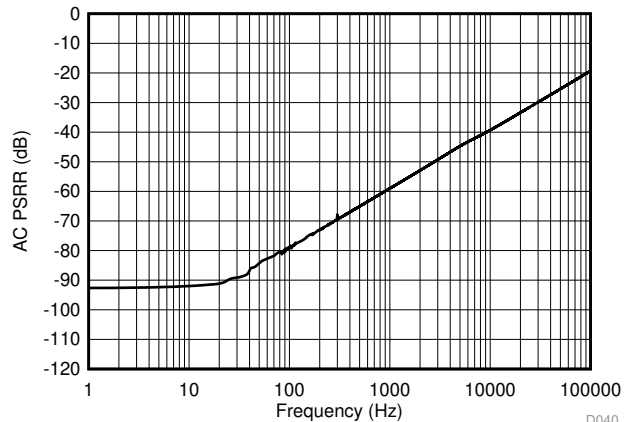


Time (1 ms/div)

D039

REF-DIV = 0 and BUFF-GAIN = 0

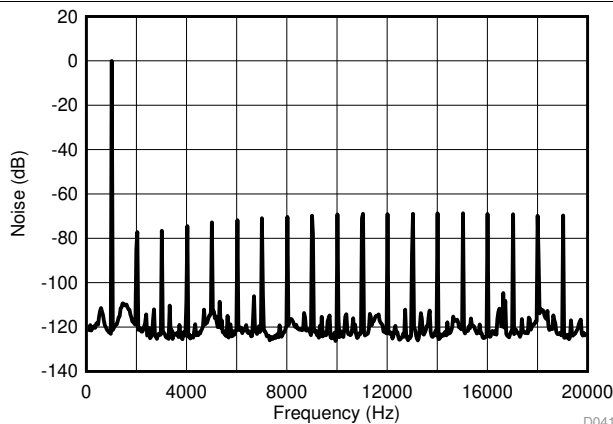
图 41. Power-Off Glitch



D040

DAC code at midscale,  $V_{DD} = 5.0\text{ V} + 0.2\text{ V}_{PP}$ ,  
REF-DIV = 0 and BUFF-GAIN = 0

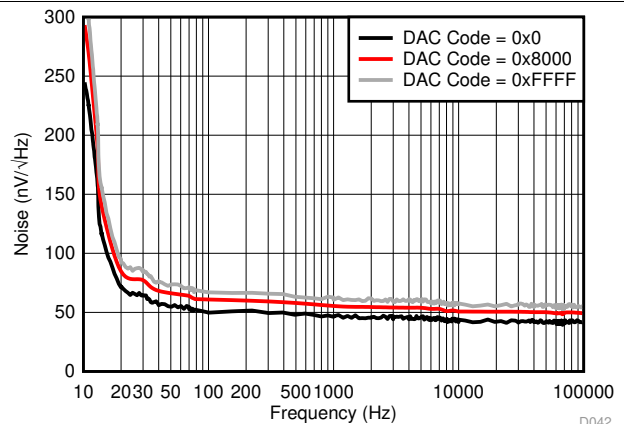
图 42. DAC Output AC PSRR vs Frequency



D041

$f_o = 1\text{ kHz}$ ,  $f_s = 400\text{ kHz}$ , includes 7 harmonics,  
measurement bandwidth = 20 kHz, external reference = 2.5 V,  
REF-DIV = 0 and BUFF-GAIN = 0

图 43. DAC Output THD+N vs Frequency



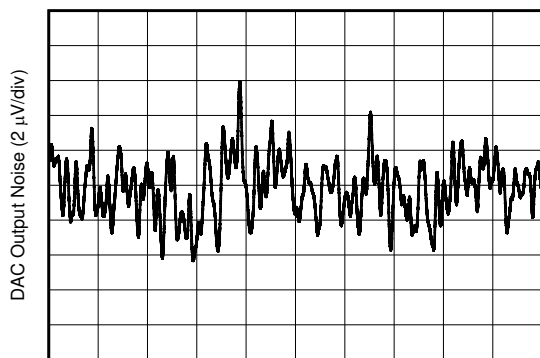
D042

Gain = 1X (REF-DIV = 1 and BUFF-GAIN = 1),  
external reference = 2.5 V,  
REF-DIV = 0 and BUFF-GAIN = 0

图 44. DAC Output Noise Spectral Density

Typical Characteristics (接下页)

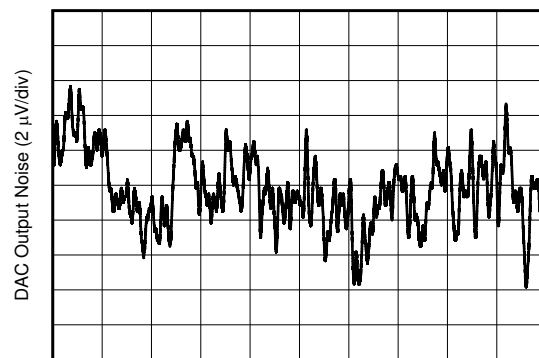
at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , internal reference = 2.5 V, REF-DIV = 0 and BUFF-GAIN = 1, channel A shown, and DAC outputs unloaded (unless otherwise noted)



D043

DAC code at midscale, external reference = 2.5 V, REF-DIV = 0 and BUFF-GAIN = 0

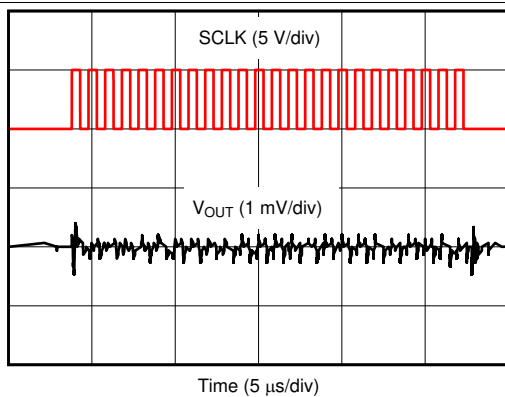
图 45. DAC Output Noise: 0.1 Hz to 10 Hz



D044

DAC code at midscale, internal reference = 2.5 V, REF-DIV = 0 and BUFF-GAIN = 0

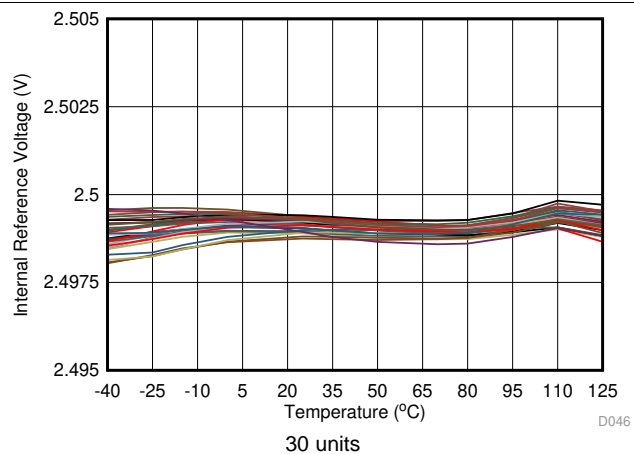
图 46. DAC Output Noise: 0.1 Hz to 10 Hz



D045

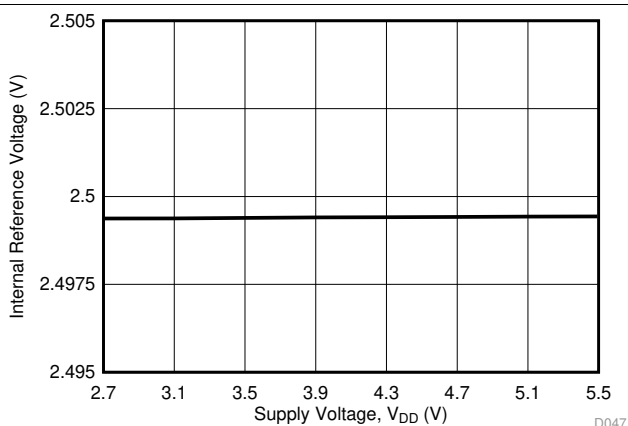
SCLK = 1 MHz, DAC code at midscale, external reference = 2.5 V, REF-DIV = 0 and BUFF-GAIN = 0

图 47. Clock Feedthrough



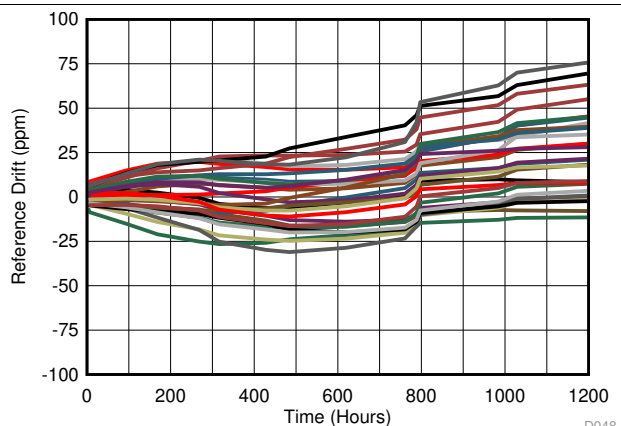
D046

图 48. Internal Reference Voltage vs Temperature



D047

图 49. Internal Reference Voltage vs Supply Voltage



D048

图 50. Internal Reference Voltage vs Time

Typical Characteristics (接下页)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , internal reference =  $2.5\text{ V}$ , REF-DIV = 0 and BUFF-GAIN = 1, channel A shown, and DAC outputs unloaded (unless otherwise noted)

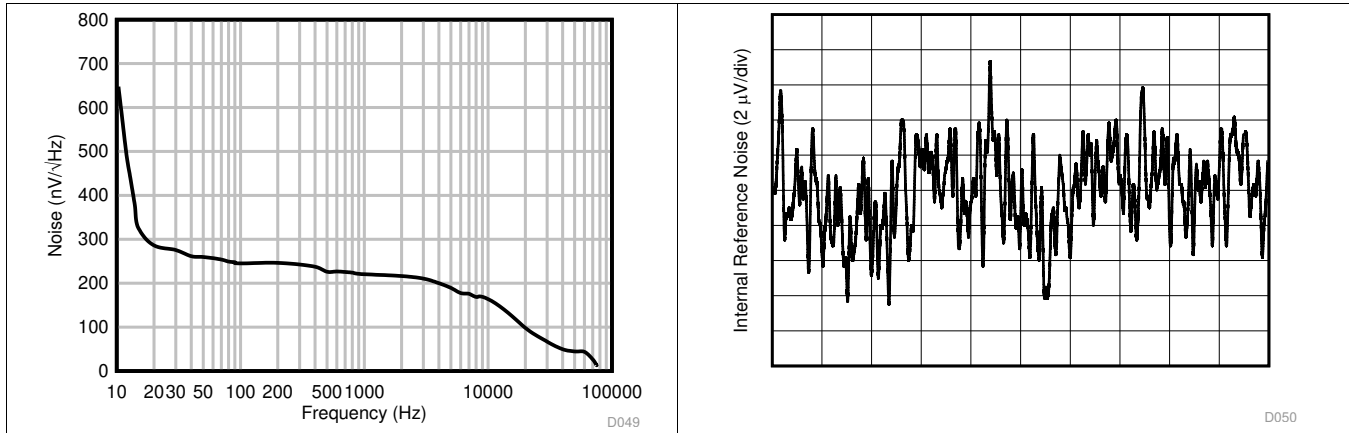


图 51. Internal Reference Noise Density vs Frequency

图 52. Internal Reference Noise: 0.1 Hz to 10 Hz

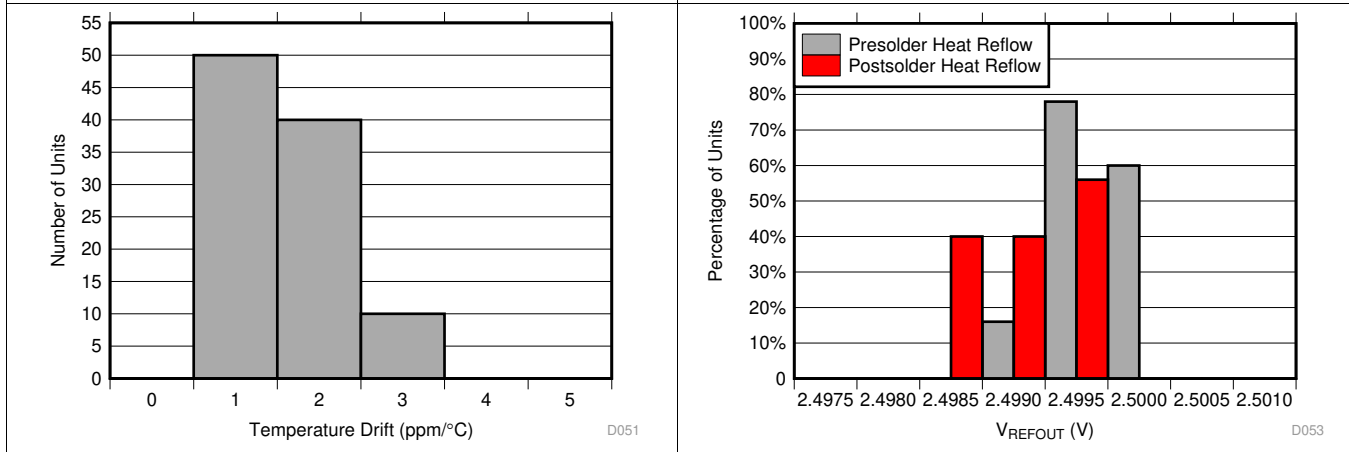


图 53. Internal Reference Temperature Drift Histogram

图 54. Internal Reference Initial Accuracy (Pre- and Post-Solder) Histogram

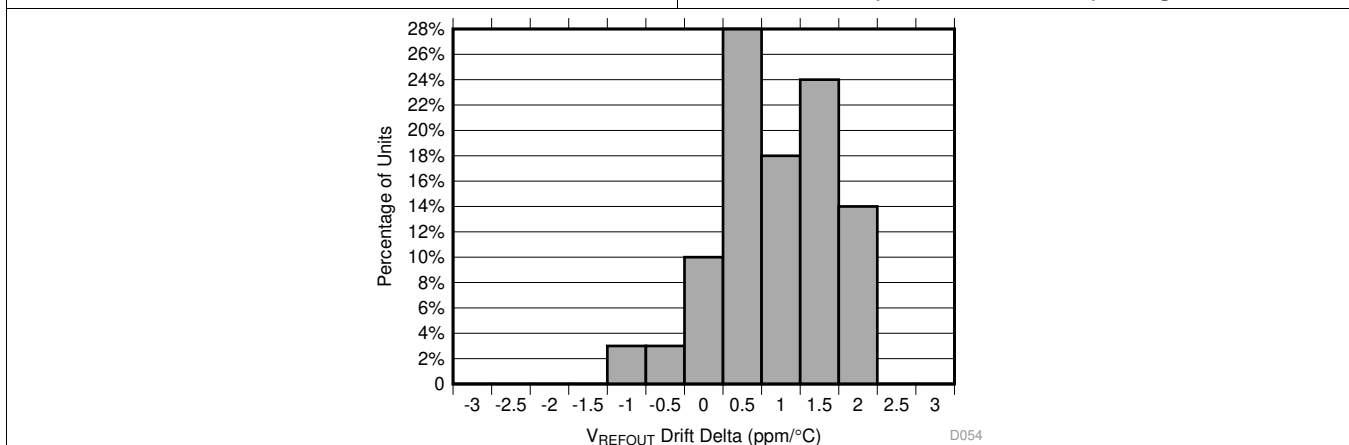


图 55. Internal Reference Temperature Drift (Pre-Solder and Post-Solder) Histogram

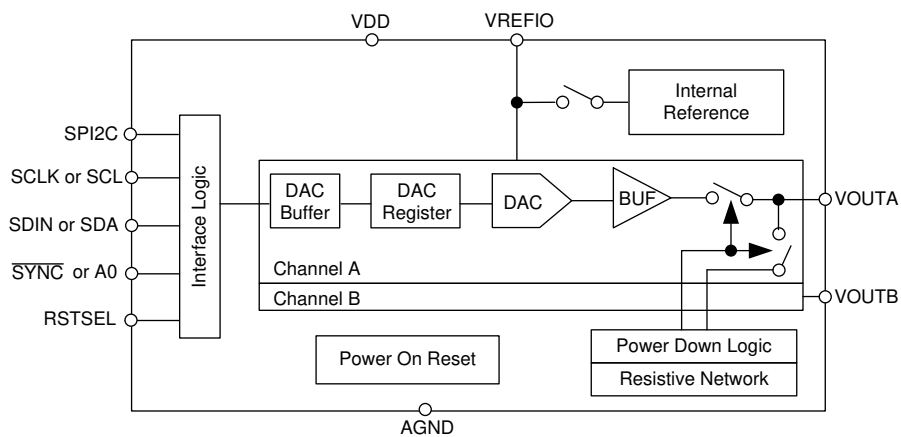
## 8 Detailed Description

### 8.1 Overview

The DAC80502, DAC70502, DAC60502 (DACx0502) family of devices are dual-channel, buffered voltage output, 16-bit, 14-bit, or 12-bit digital-to-analog converters (DACs), respectively. These devices include a 2.5-V, 5-ppm/°C internal reference, giving full-scale output voltage ranges of 1.25 V, 2.5 V, or 5 V. The DACx0502 devices incorporate a power-on-reset circuit that makes sure that the DAC output powers up at zero scale or midscale, depending on status of the RSTSEL pin, and remains at that scale until a valid code is written to the device.

The digital interface of the DACx0502 can be configured to SPI or I<sup>2</sup>C mode using the SPI2C pin. In SPI mode, the DACx0502 family uses a 3-wire serial interface that operates at clock rates up to 50 MHz. In I<sup>2</sup>C mode, the DACx0502 devices operate in standard (100 kbps), fast (400 kbps), and fast+ (1.0 Mbps) modes.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Digital-to-Analog Converter (DAC) Architecture

Each output channel in the DACx0502 family of devices consists of a rail-to-rail ladder architecture with an output buffer amplifier. The devices include an internal 2.5-V reference. [Figure 56](#) shows a block diagram of the DAC architecture.

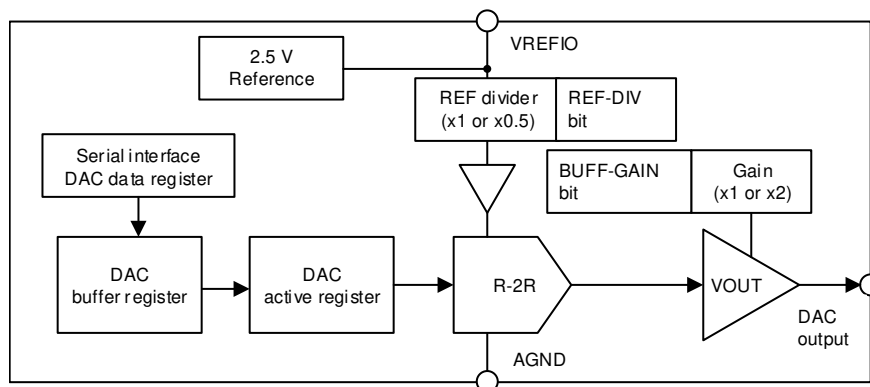


图 56. DACx0502 DAC Block Diagram

## Feature Description (接下页)

### 8.3.1.1 DAC Transfer Function

The input data writes to the individual DAC data registers in straight binary format. After a power-on or a reset event, all DAC registers are set to zero code (RSTSEL = 0) or midscale code (RSTSEL = 1). The DAC transfer function is shown by [公式 1](#).

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times \frac{VREFIO}{DIV} \times GAIN$$

where:

- N = resolution in bits = either 12 (DAC60502), 14 (DAC70502) or 16 (DAC80502).
- DAC\_DATA = decimal equivalent of the binary code that is loaded to the DAC register (address 8h), DAC\_DATA ranges from 0 to  $2^N - 1$ .
- VREFIO = DAC reference voltage. Either VREFIO from the internal 2.5-V reference or VREFIO from an external reference.
- DIV = 1 (default) or 2 as set by the REF-DIV bit in the GAIN register (address 4h).
- GAIN = 1 or 2 (default) as set by the BUFF-GAIN bit for that DAC channel in the GAIN register (address 4h). (1)

### 8.3.1.2 DAC Register Structure

Data written to the DAC data registers are initially stored in the DAC buffer registers. The update mode of the DAC output is determined by the status of the DAC\_SYNC\_EN bit (address 2h).

In asynchronous mode (default, DAC\_SYNC\_EN = 0), a write to the DAC buffer register results in an immediate update of the DAC active register. In SPI mode, the DAC output (VOUTx pin) updates on the rising edge of SYNC. In I<sup>2</sup>C mode, the DAC output (VOUT pin) updates on the falling edge of SCL on the last acknowledge bit.

In synchronous mode (DAC\_SYNC\_EN = 1), writing to the DAC buffer register does not automatically update the DAC active register. Instead, the update occurs only after a software LDAC trigger event. A software LDAC trigger generates through the LDAC bit in the TRIGGER register (address 5h). When the host reads from a DAC buffer register, the value held in the DAC buffer register is returned (not the value held in the DAC active register).

### 8.3.1.3 Output Amplifier

The output buffer amplifier generates rail-to-rail voltages on the output, giving a maximum output range of 0 V to VDD. [公式 1](#) shows that the full-scale output range of the DAC output is determined by the voltage on the VREFIO pin, the reference divider setting (DIV) as set by the REF-DIV bit (address 4h), and the gain configuration for that channel set by the corresponding BUFF-GAIN bit (address 4h).

## 8.3.2 Internal Reference

The DAx0502 family of devices includes a 2.5-V precision band-gap reference enabled by default. Operation from an external reference is supported by disabling the internal reference in the REF\_PWDWN bit (address 3h). The internal reference is externally available at the VREFIO pin and sources up to 5 mA. For noise filtering, use a minimum 150-nF capacitor between the reference output and AGND.

The reference voltage to the device, either from the internal reference or an external one, can be divided by a factor of two by setting the REF-DIV bit (address 4h) to 1. The REF-DIV bit provides additional flexibility in setting the full-scale output range of the DAC output. Make sure to configure REF-DIV so that there is sufficient headroom from VDD to the DAC operating reference voltage, VREFIO (see [公式 1](#)). See the [Recommended Operating Conditions](#) for more information.

Improper configuration of the reference divider triggers a reference alarm condition. In this case, the reference buffer is shut down, and all the DAC outputs go to 0 V. The DAC data registers are unaffected by the alarm condition, and thus enable the DAC output to return to normal operation after the reference divider is configured correctly.

### 8.3.2.1 Solder Heat Reflow

A known behavior of IC reference voltage circuits is the shift induced by the soldering process. [图 54](#) and [图 55](#) show the effect of solder heat reflow for the DACx0502 internal reference.

## Feature Description (接下页)

### 8.3.3 Power-On Reset (POR)

The DACx0502 family of devices includes a power-on reset function that controls the output voltage at power up. After the VDD supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a 250- $\mu$ s, power-on-reset delay. The default value for all DACs is zero code if RSTSEL = 0, and midscale code if RSTSEL = 1. Each DAC channel remains at the power-up voltage until a valid command is written to a channel.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific VDD levels, as indicated in 图 57, in order to make sure that the internal capacitors discharge and reset the device on power up. In order to make sure that a POR occurs, VDD must be less than 0.7 V for at least 1 ms. When VDD drops to less than 2.2 V but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When VDD remains greater than 2.2 V, a POR does not occur.

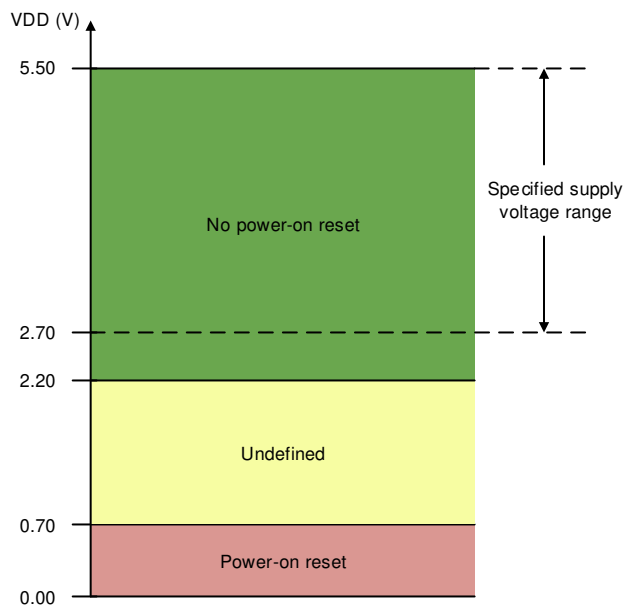


图 57. Threshold Levels for the VDD POR Circuit

### 8.3.4 Software Reset

A device software reset event is initiated by writing the reserved code 0x1010 to the SOFT-RESET bit in the TRIGGER register (address 5h). A software reset initiates a POR event.

## 8.4 Device Functional Modes

The DACx0502 have two modes of operation: normal and power-down.

### 8.4.1 Power-Down Mode

The DACx0502 output amplifiers and internal reference can be independently powered down through the CONFIG register (3h). At power up, the DAC output and the internal reference are active by default. In power-down mode, the DACs output (VOUTx pin) is internally connected to AGND through a 1-k $\Omega$  resistor.

## 8.5 Programming

### 8.5.1 Serial Interface

The DACx0502 family of devices is controlled through either a 3-wire SPI or a 2-wire I<sup>2</sup>C interface.

The type of interface is determined at device power up based on the logic level of the SPI2C pin. A logic 0 on the SPI2C pin puts the DACx0502 in SPI mode; whereas, logic 1 on SPI2C puts the DACx0502 in I<sup>2</sup>C mode. The SPI2C pin must be kept static after the device powers up.

#### 8.5.1.1 SPI Mode

The DACx0502 digital interface is programmed to work in SPI mode when the logic level of the SPI2C pin is 0 at power up. 表 1 shows the frame format for SPI mode. In SPI mode, the DACx0502 have a 3-wire serial interface:  $\overline{\text{SYNC}}$ , SCLK, and SDIN. The serial interface is compatible with SPI, QSPI, and Microwire interface standards, and most digital signal processors (DSPs). The serial interface operates at up to 50 MHz. The input shift register is 24-bits wide.

表 1. SPI Mode Frame Format

BIT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DESC	R/ $\overline{\text{W}}$	Register Address - Command Byte								16-Bit MSB-Aligned DAC Data: DAC80502 {15:0}, DAC70502 {13:0, x, x}, DAC60502 {11:0, x, x, x, x}														

Serial clock SCLK is a continuous or a gated clock. The first falling edge of  $\overline{\text{SYNC}}$  starts the operation cycle. When  $\overline{\text{SYNC}}$  is high, the SCLK and SDIN signals are blocked. The device internal registers are updated from the shift register on the rising edge of  $\overline{\text{SYNC}}$ .

##### 8.5.1.1.1 $\overline{\text{SYNC}}$ Interrupt

For SPI-mode operation, the  $\overline{\text{SYNC}}$  line stays low for at least 24 falling edges of SCLK, and the addressed DAC register updates on the  $\overline{\text{SYNC}}$  rising edge. However, if the  $\overline{\text{SYNC}}$  line is brought high before the 24th SCLK falling edge, this event acts as an interrupt to the write sequence. The shift register resets and the write sequence is discarded. The data buffer contents and the DAC register contents do not update, and the the operating mode does not change, as shown in 图 58.

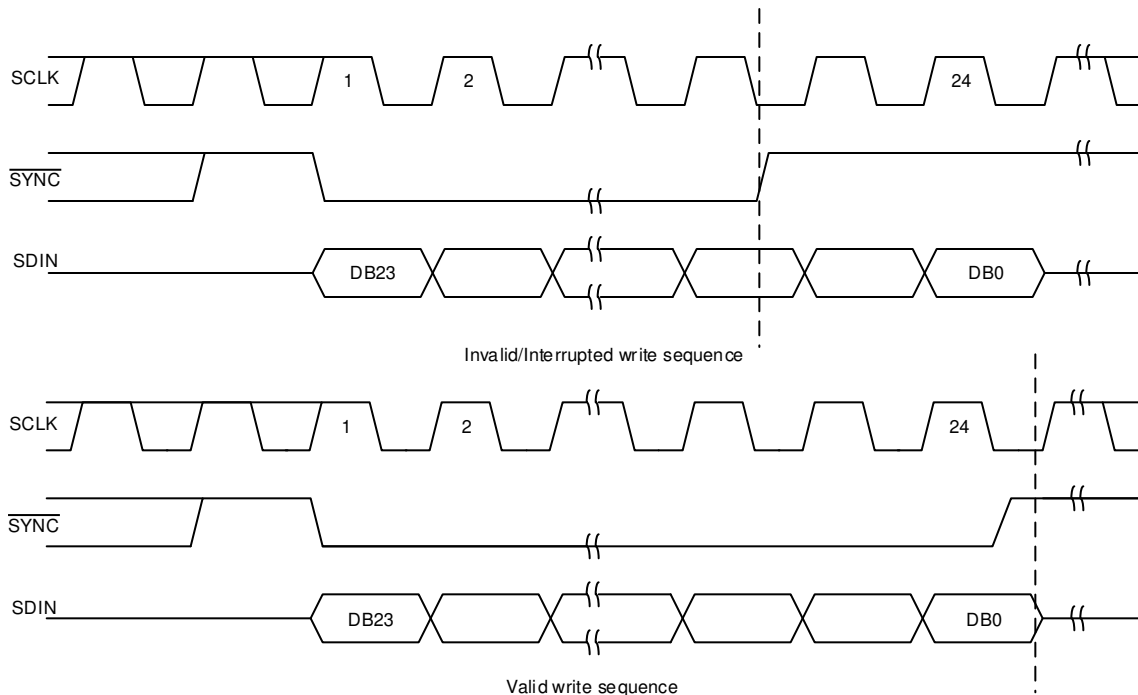


图 58.  $\overline{\text{SYNC}}$  Interrupt

### 8.5.1.2 I<sup>2</sup>C Mode

The DACx0502 digital interface is programmed to work in I<sup>2</sup>C mode when the logic level of the SPI2C pin is 1 at power up. In I<sup>2</sup>C mode, the DACx0502 have a 2-wire serial interface: SCL, SDA, and one address pin, A0. The I<sup>2</sup>C bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both the SDA and SCL lines are pulled high. All the I<sup>2</sup>C-compatible devices connect to the I<sup>2</sup>C bus through open-drain I/O pins SDA and SCL.

The I<sup>2</sup>C specification states that the device that controls communication is called a *master*, and the devices that are controlled by the master are called *slaves*. The master device generates the SCL signal. The master device also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the master. The master device on an I<sup>2</sup>C bus is typically a microcontroller or DSP. The DACx0502 operate as a slave device on the I<sup>2</sup>C bus. A slave device acknowledges master commands, and upon master control, receives or transmits data.

Typically, the DACx0502 operate as a slave receiver. A master device writes to the DACx0502, a slave receiver. However, if a master device requires the DACx0502 internal register data, the DACx0502 operate as a slave transmitter. In this case, the master device reads from the DACx0502. According to I<sup>2</sup>C terminology, read and write refer to the master device.

The DACx0502 are slave devices that support the following data transfer modes:

1. Standard mode (100 kbps)
2. Fast mode (400 kbps)
3. Fast-mode plus (1.0 Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, these modes are referred to as F/S-mode in this document. The fast-mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current would be 3 mA, similar to the case of standard and fast modes. The DACx0502 support 7-bit addressing. The 10-bit addressing mode is not supported. These devices support the general call reset function. Sending the following sequence initiates a software reset within the device: start/repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the falling edge of the ACK bit, following the second byte.

Other than specific timing signals, the I<sup>2</sup>C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. Acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. A not-acknowledge is when the SDA line is left high during the high period of the ninth clock cycle as shown in [图 59](#).

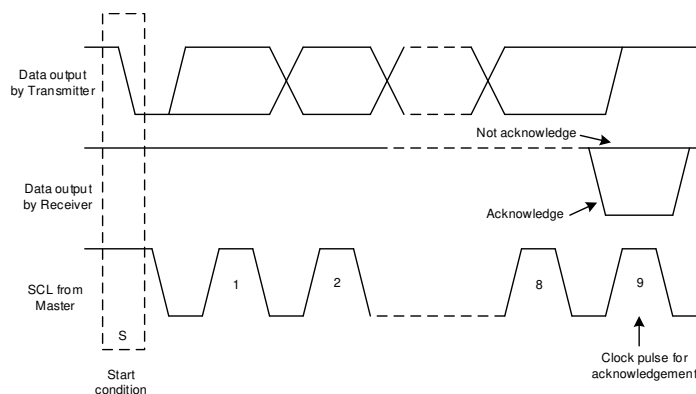
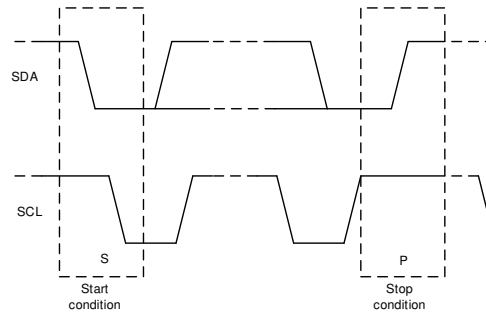


图 59. Acknowledge and Not Acknowledge on the I<sup>2</sup>C Bus

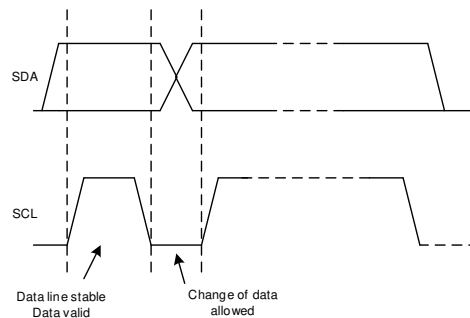


### 8.5.1.2.1 F/S Mode Protocol

1. The master initiates data transfer by generating a start condition. The start condition is when a high to-low transition occurs on the SDA line while SCL is high, as shown in [图 60](#). All I<sup>2</sup>C-compatible devices recognize a start condition.



**图 60. Start and Stop Conditions**



**图 61. Bit Transfer on the I<sup>2</sup>C Bus**

2. The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/W) on the SDA line. During all transmissions, the master makes sure that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in [图 61](#). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle, as shown in [图 59](#). Upon detecting this acknowledge, the master knows the communication link with a slave has been established.
3. The master generates further SCL cycles to transmit (R/W bit 0) or receive (R/W bit 1) data to the slave. In either case, the receiver must acknowledge the data sent by the transmitter so that the acknowledge signal can be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consists of eight data bits and one acknowledge-bit, and can continue for as long as necessary.
4. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high (see [图 60](#)). This action releases the bus and stops the communication link with the addressed slave. All I<sup>2</sup>C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all slave devices then wait for a start condition followed by a matching address.

8.5.1.2.2 DACx0502 I<sup>2</sup>C Update Sequence

For a single update, the DACx0502 requires a start condition, a valid I<sup>2</sup>C address byte, a command byte, and two data bytes (the most significant data byte, MSDB, and least significant data byte, LSDB), as listed in 表 2.

表 2. Update Sequence

MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte				Command byte				MSDB				LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

After each byte is received, the DACx0502 acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse, as shown in 图 62. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I<sup>2</sup>C™ address byte selects the DACx0502 devices.

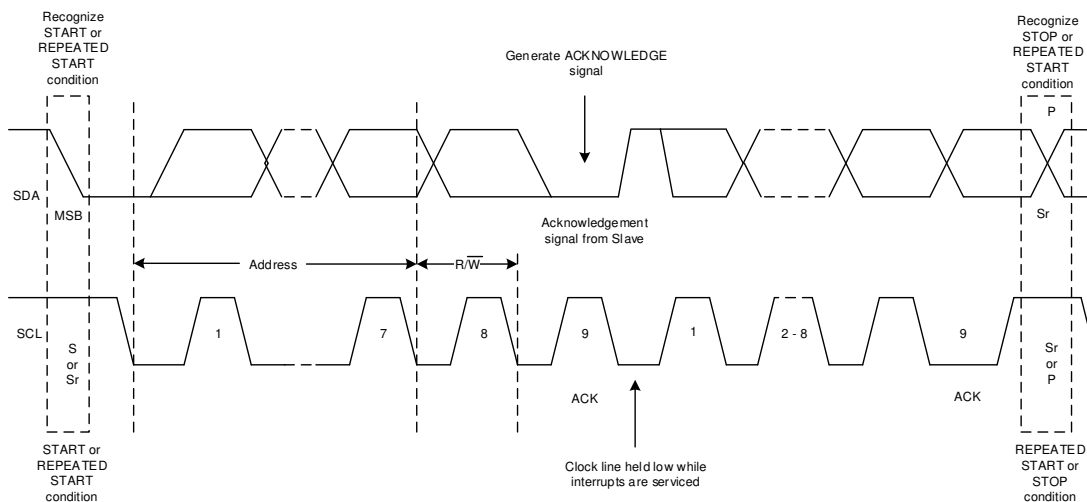


图 62. I<sup>2</sup>C Bus Protocol

The command byte sets the operating mode of the selected DACx0502 device. When the operating mode is selected by this byte, the DACx0502 series must receive two data bytes, the most significant data byte (MSDB) and least significant data byte (LSDB), for a data update to occur. The DACx0502 devices perform an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum DAC update rate is limited to 22.22 kSPS. Using the fast-mode plus (clock = 1 MHz), the maximum DAC update rate is limited to 55.55 kSPS. When a stop condition is received, the DACx0502 family releases the I<sup>2</sup>C bus and awaits a new start condition.

**8.5.1.2.2.1 DACx0502 Address Byte**

The address byte, as shown in 表 3, is the first byte received following the start condition from the master device. The first four bits (MSBs) of the address are factory preset to 1001. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin and consequently responds to that particular address according to 表 4.

**表 3. DACx0502 Address Byte**

B31	B30	B29	B28	B27	B26	B25	B24	COMMENT
AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/ $\bar{W}$	
1	0	0	1	See 表 4 (slave address column)			0 or 1	General address

**表 4. Address Format**

SLAVE ADDRESS	A0 PIN
1001 000	AGND
1001 001	VDD
1001 010	SDA
1001 011	SCL

**8.5.1.2.2.2 DACx0502 Command Byte**

The DACx0502 command byte (shown in 表 5) controls which command is executed and which register is being accessed when writing to or reading from the DACx0502 series.

**表 5. DACx0502 Command Byte**

B23	B22	B21	B20	B19	B18	B17	B16	REGISTER
0	0	0	0	0	0	0	0	NOOP
0	0	0	0	0	0	0	1	DEVID
0	0	0	0	0	0	1	0	SYNC
0	0	0	0	0	0	1	1	CONFIG
0	0	0	0	0	1	0	0	GAIN
0	0	0	0	0	1	0	1	TRIGGER
0	0	0	0	0	1	1	0	BRDCAST
0	0	0	0	0	1	1	1	STATUS
0	0	0	0	1	0	0	0	DAC-A DATA
0	0	0	0	1	0	0	1	DAC-B DATA

**8.5.1.2.2.3 DACx0502 Data Byte (MSDB and LSDB)**

The MSDB and LSDB contain the data that are passed to the register(s) specified by the command byte, as shown in 表 6. The DACx0502 updates at the falling edge of the acknowledge signal that follows the LSDB[0] bit.

**表 6. DACx0502 Data Byte**

REGISTER NAME	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
	MSDB								LSDB							
NOOP	NOOP - No operation															
DEVID	0	RESOLUTION			0	0	1	0	0	0	0	1	0	1	0	1
SYNC	RESERVED						DAC-B-BRDCST-EN	DAC-A-BRDCST-EN	RESERVED						DAC-B-SYNC-EN	DAC-A-SYNC-EN
CONFIG	RESERVED						REF-PWDWN	RESERVED						DAC-B-PWDWN	DAC-A-PWDWN	
GAIN	RESERVED						REF-DIV	RESERVED						BUF-B-GAIN	BUF-A-GAIN	
TRIGGER											LDAC	SOFT-RESET [3:0]				
BRDCAST	BROADCAST-DAC-DATA [15:0] / BROADCAST-DAC-DATA [13:0] / BROADCAST-DAC-DATA [11:0] -- left Aligned															
STATUS	RESERVED														REF-ALARM	
DAC-A	DAC-A-DATA [15:0] for 16-bit / DAC-A-DATA [13:0] for 14-bit / DAC-A-DATA [11:0] for 12-bit -- left Aligned															
DAC-B	DAC-B-DATA [15:0] for 16-bit / DAC-B-DATA [13:0] for 14-bit / DAC-B-DATA [11:0] for 12-bit -- left Aligned															

**8.5.1.2.3 DACx0502 I<sup>2</sup>C Read Sequence**

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a slave address and the  $\overline{R/\overline{W}}$  bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the slave address and the  $\overline{R/\overline{W}}$  bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The master must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register

An alternative reading method allows for reading back the value of the last register written. The sequence is a start or repeated start with the slave address and the  $\overline{R/\overline{W}}$  bit set to 1, and the two bytes of the last register are read out. All the registers in DACx0502 family can be read out with the exception of SOFT-RESET register. 表 6 shows the read command set.

**表 7. Read Sequence**

S	MSB	...	$\overline{R/\overline{W}}$ (0)	ACK	MSB	...	LSB	ACK	Sr	MSB	...	$\overline{R/\overline{W}}$ (1)	ACK	MSB	...	LSB	ACK	MSB	...	LSB	NACK
	ADDRESS BYTE				COMMAND BYTE				Sr	ADDRESS BYTE				MSDB				LSDB			
	From Master			Slave	From Master			Slave	From Master			Slave	From Slave			Master	From Slave			Master	

## 8.6 Register Maps

### 8.6.1 Registers

**Table 8. DACx0502 Register Map**

Offset	Register Name	Section
0h	No Operation	NOOP Register
1h	Device Identification	DEVID Register
2h	Synchronization	SYNC Register
3h	Configuration	CONFIG Register
4h	Gain	GAIN Register
5h	Trigger	TRIGGER Register
6h	Broadcast	BRDCAST Register
7h	Device Status	STATUS Register
8h	DAC-A	DAC-A Register
9h	DAC-B	DAC-B Register

#### 8.6.1.1 NOOP Register (offset = 0h) [reset = 0000h]

**Figure 63. NOOP Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOOP															
W-0h															

**Table 9. NOOP Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	No operation	W	0h	No Operation command

#### 8.6.1.2 DEVID Register (offset = 1h) [reset = 0214h for DAC80502, 1214h for DAC70502, 2214h for DAC60502]

**Figure 64. DEVID Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RESOLUTION			0	0	1	0	0	0	0	1	0	1	0	1
R-0h	R/W-0000h (DAC80502) or 0001h (DAC70502) or 0020h (DAC60502)			R-0h	R-0h	R-1h	R-0h	R-0h	R-0h	R-0h	R-1h	R-0h	R-1h	R-0h	R-1h

**Table 10. DEVID Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	RESERVED
14-12	RESOLUTION	R	0000h (DAC80502) 0001h (DAC70502) 0020h (DAC60502)	DAC Resolution: 0000h (DAC80502 16-bit) 0001h (DAC70502 14-bit) 0020h (DAC60502 12-bit)
11-0	RESERVED	R	0215h	RESERVED

**8.6.1.3 SYNC Register (offset = 2h) [reset = 0300h]**

**Figure 65. SYNC Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						DAC-B-BRDCAST-EN	DAC-A-BRDCAST-EN	RESERVED						DAC-B-SYNC-EN	DAC-A-SYNC-EN
R/W-0h						R/W-1h	R/W-1h	R/W-0h						R/W-0h	R/W-0h

**Table 11. SYNC Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-10	RESERVED	RW	0h	RESERVED
9	DAC-B-BRDCAST-EN	RW	1h	When set to 1 the corresponding DAC is set to update its output after a serial interface write to the BRDCAST register. When cleared to 0 the corresponding DAC output remains unaffected after a serial interface write to the BRDCAST register.
8	DAC-A-BRDCAST-EN	RW	1h	When set to 1 the corresponding DAC is set to update its output after a serial interface write to the BRDCAST register. When cleared to 0 the corresponding DAC output remains unaffected after a serial interface write to the BRDCAST register.
7-2	RESERVED	RW	0h	RESERVED
1	DAC-B-SYNC-EN	RW	0h	When set to 1, the DAC output is set to update in response to an LDAC trigger (synchronous mode). When cleared to 0, the DAC output is set to update immediately (asynchronous mode), default.
0	DAC-A-SYNC-EN	RW	0h	When set to 1, the DAC output is set to update in response to an LDAC trigger (synchronous mode). When cleared to 0, the DAC output is set to update immediately (asynchronous mode), default.

**8.6.1.4 CONFIG Register (offset = 3h) [reset = 0000h]**

**Figure 66. CONFIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						REF-PWDWN	RESERVED						DAC-B-PWDWN	DAC-A-PWDWN	
R/W-0h						R/W-0h	R/W-0h						R/W-0h	R/W-0h	

**Table 12. CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-9	RESERVED	RW	0h	RESERVED
8	REF-PWDWN	RW	0h	When set to 1 disables the device internal reference
7-2	RESERVED	RW	0h	RESERVED
1	DAC-B-PWDWN	RW	0h	When set to 1, the corresponding DAC in power-down mode and output is connected to GND through a 1-kΩ internal resistor.
0	DAC-A-PWDWN	RW	0h	When set to 1, the corresponding DAC in power-down mode and output is connected to GND through a 1-kΩ internal resistor.

**8.6.1.5 GAIN Register (offset = 4h) [reset = 0003h]**
**Figure 67. GAIN Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							REF-DIV	RESERVED					BUFF-B-GAIN	BUFF-A-GAIN	
R/W-0h							R/W-0h	R/W-0h					R/W-1h	R/W-1h	

**Table 13. GAIN Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-9	RESERVED	RW	0h	RESERVED
8	REF-DIV	RW	0h	The reference voltage to the device (either from the internal or external reference) can be divided by a factor of two by setting the REF-DIV bit to 1. Make sure to configure REF-DIV so that there is sufficient headroom from VDD to the DAC operating reference voltage. Improper configuration of the reference divider triggers a reference alarm condition. In the case of an alarm condition, the reference buffer is shut down, and all the DAC outputs go to 0 V. The DAC data registers are unaffected by the alarm condition, and thus enable the DAC output to return to normal operation after the reference divider is configured correctly.  When set to 1 the reference voltage is internally divided by a factor of 2.  When cleared to 0 the reference voltage is unaffected.
7-2	RESERVED	RW	0h	RESERVED
1	BUFF-B-GAIN	RW	1h	When set to 1 the buffer amplifier for corresponding DAC has a gain of 2.  When cleared to 0 the buffer amplifier for corresponding DAC has a gain of 1.
0	BUFF-A-GAIN	RW	1h	When set to 1 the buffer amplifier for corresponding DAC has a gain of 2.  When cleared to 0 the buffer amplifier for corresponding DAC has a gain of 1.

**8.6.1.6 TRIGGER Register (offset = 5h) [reset = 0000h]**
**Figure 68. TRIGGER Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											LDAC	SOFT-RESET [3:0]			
R/W-0h											W-0h	W-0h			

**Table 14. TRIGGER Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-5	RESERVED	RW	0h	RESERVED
4	LDAC	W	0h	Set this bit to 1 to synchronously load those DACs who have been set in synchronous mode in the SYNC register. This is a self resetting bit.
3-0	SOFT-RESET [3:0]	W	0h	When set to the reserved code 1010 resets the device to its default state. This is a self resetting bit.

**8.6.1.7 BRDCAST Register (offset = 6h) [reset = 0000h for RSTSEL = 0, or reset = 8000h for RSTSEL = 1]**
**Figure 69. BRDCAST Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-DATA [15:0]															
W-0000h when RSTSEL = 0 or reset = 8000h when RSTSEL = 1															

**Table 15. BRDCAST Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	BRDCAST-DATA [15:0]	W	0000h when RSTSEL = 0 or 8000h when RSTSEL = 1	Writing to the BRDCAST register forces those DAC channels who have been set to broadcast in the SYNC register to update its active register data to the BRDCAST-DATA one. Data is MSB aligned in straight binary format and follows the format below: DAC80502: { DATA[15:0] } DAC70502: { DATA[13:0], x, x } DAC60502: { DATA[11:0], x, x, x, x } x – Don't care bits

**8.6.1.8 STATUS Register (offset = 7h) [reset = 0000h]**
**Figure 70. STATUS Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														REF-ALARM	
R/W-0h														R-0h	

**Table 16. STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-1	RESERVED	RW	0h	RESERVED
0	REF-ALARM	R	0	REF-ALARM bit. Reads 1 when the difference between the reference and supply pins is below a minimum analog threshold. Reads 0 otherwise. When 1, the reference buffer is shut down, and the DAC outputs are all 0 V. The DAC codes are unaffected, and the DAC output returns to normal when the difference is above the analog threshold.



**8.6.1.9 DAC-n Register (offset = 8h–9h) [reset = 0000h for RSTSEL = 0, or reset = 8000h for RSTSEL = 1]**
**Figure 71. DAC-n Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-n-DATA [15:0]															
R/W-0000h when RSTSEL = 0 or reset = 8000h when RSTSEL = 1															

**Table 17. DAC-A Data Register Field Descriptions (8h)**

Bit	Field	Type	Reset	Description
15-0	DAC-A-DATA [15:0]	RW	0000h when RSTSEL = 0 or 8000h when RSTSEL = 1	Data is MSB aligned in straight binary format and follows the format below: DAC80502: { DATA[15:0] } DAC70502: { DATA[13:0], x, x } DAC60502: { DATA[11:0], x, x, x, x } x – Don't care bits

**Table 18. DAC-B Data Register Field Descriptions (9h)**

Bit	Field	Type	Reset	Description
15-0	DAC-B-DATA [15:0]	RW	0000h when RSTSEL = 0 or 8000h when RSTSEL = 1	Data is MSB aligned in straight binary format and follows the format below: DAC80502: { DATA[15:0] } DAC70502: { DATA[13:0], x, x } DAC60502: { DATA[11:0], x, x, x, x } x – Don't care bits

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Generating accurate, stable programmable dc voltages is a key requirement in most precision end equipment. The DACx0502 family of precision DACs are an excellent choice for such applications. The DACx0502 tiny package, high resolution, and simple interface makes these devices a great choice for applications such as offset and gain control, VCO tuning, programmable reference, and more. With the aforementioned features, this family of DACs caters to a wide range of end equipment, such as battery testers, communications equipment, factory automation and control, test and measurement, and more.

### 9.2 Typical Application

Battery test equipment requires a two-channel DAC for every channel of battery test output. A battery tester operates in constant-current (CC) and constant-voltage (CV) modes. The two DAC channels are used to set the voltage and current for battery charge and discharge control. The low INL of the DACx0502 makes system calibration simple. The integrated reference and the small package make the design very compact.

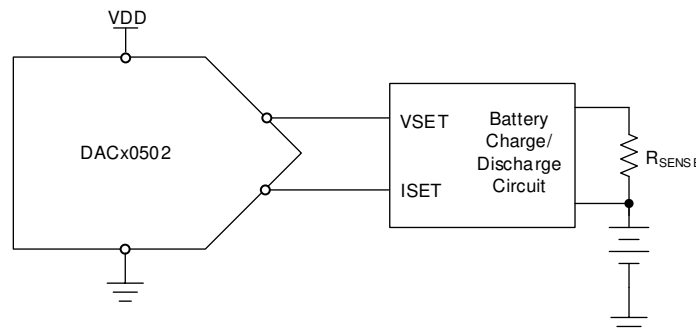


图 72. Battery Test Equipment

#### 9.2.1 Design Requirements

- DAC output range: 0 V to 2.5 V
- DAC output accuracy after calibration: 0.05%FSR
- Operating temperature: 0°C to 100°C

#### 9.2.2 Detailed Design Procedure

图 72 shows a simplified circuit diagram of a battery test system. Use the internal reference (2.5 V) and gain of 1 for an output range of 2.5 V. The reference divider is 1. Select the 16-bit DAC80502 for the best accuracy. The typical value of the TUE is 0.02%FSR, as specified in the [Typical Characteristics](#) table. The absolute error at the DAC output includes the error from the reference, the error from the DAC, and the temperatures drifts of offset error, gain error, and reference. Ignore the load regulation, line regulation, and long-term drift of the reference as compared to the initial accuracy and temperature drift. Write the total TUE at the DAC output, as given in [公式 2](#).

### Typical Application (接下页)

$$TUE_{TOTAL} = \sqrt{(TUE)^2 + (TC_{OE})^2 + (TC_{GE})^2 + (E_{REF} \times GAIN)^2 + (TC_{REF} \times GAIN)^2}$$

where

- $TC_{OE}$  is the temperature drift of the offset error.
- $TC_{GE}$  is the temperature drift of the gain error.
- $E_{REF}$  is the initial accuracy of the reference.
- $TC_{REF}$  is the temperature drift of the reference.
- GAIN is the gain setting of the DAC in combination with the reference divider.

(2)

Convert the INL value in LSB to %FSR using 公式 3.

$$\%FSR = \frac{LSB}{2^N} \times 100$$

(3)

Convert the temperature drift values in ppm/°C to %FSR using 公式 4.

$$\%FSR = \frac{(PPM / ^\circ C) \times \Delta T}{10^4}$$

where

- $\Delta T$  is the temperature range.

(4)

Calculate the total error after the offset and gain of DAC are calibrated using 公式 5

$$TUE_{TOTAL} = \sqrt{(INL)^2 + (TC_{OE})^2 + (TC_{GE})^2 + (TC_{REF} \times GAIN)^2}$$

(5)

The total error at the DAC output calculated using the previous equations is 0.112%FSR before calibration, and 0.05%FSR after calibration. For better accuracy, perform a temperature calibration. 图 73 and 图 74 show the drift in the internal reference voltage and TUE, respectively over 0°C to 100°C.

### 9.2.3 Application Curves

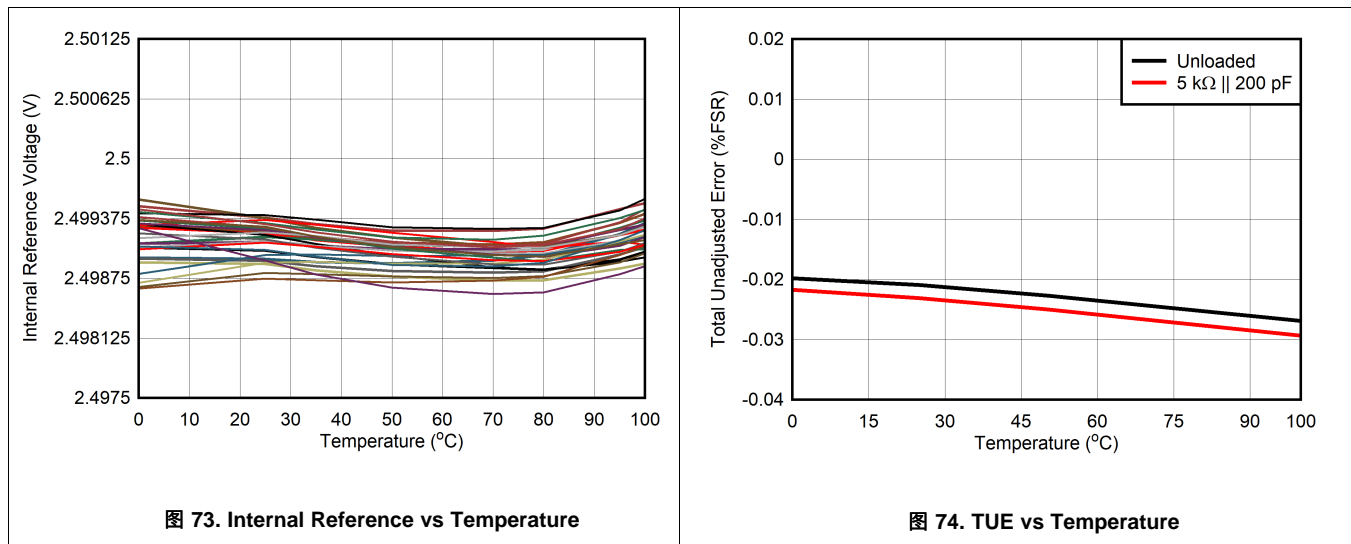


图 73. Internal Reference vs Temperature

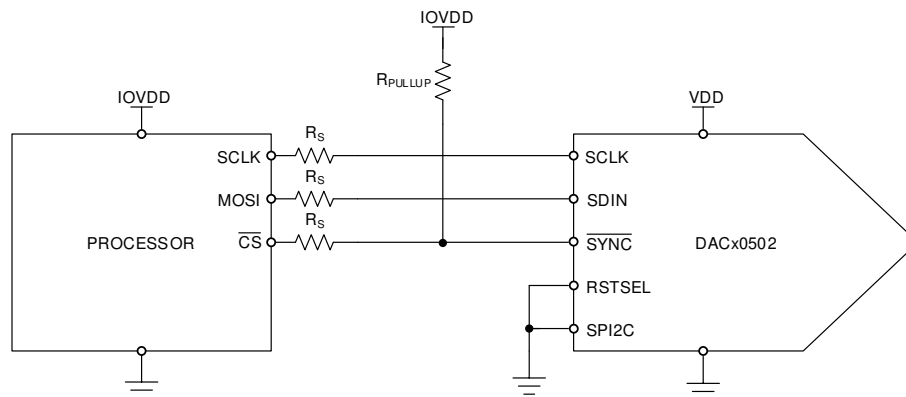
图 74. TUE vs Temperature

## 9.3 System Examples

The DACx0502 come with a pin-selectable SPI or I<sup>2</sup>C interface. This configuration makes the system design generic. Pull the SPI2C pin low for SPI or high for I<sup>2</sup>C. The RSTSEL pin provides a known output at the DAC channels at power up, which helps the system achieve a predictable behavior during start up. When using a processor with multiple power-supply domains, make sure the input/output power (IOVDD) never exceeds the VDD voltage of the DAC. Switching on the IOVDD before VDD can violate the absolute maximum ratings. When there is no power-supply sequencing implemented on the system between the processor and the DAC, use a series resistor on the digital lines so that the current flow on the digital lines is limited to  $\pm 10$  mA on any pin.

### 9.3.1 SPI Connection to a Processor

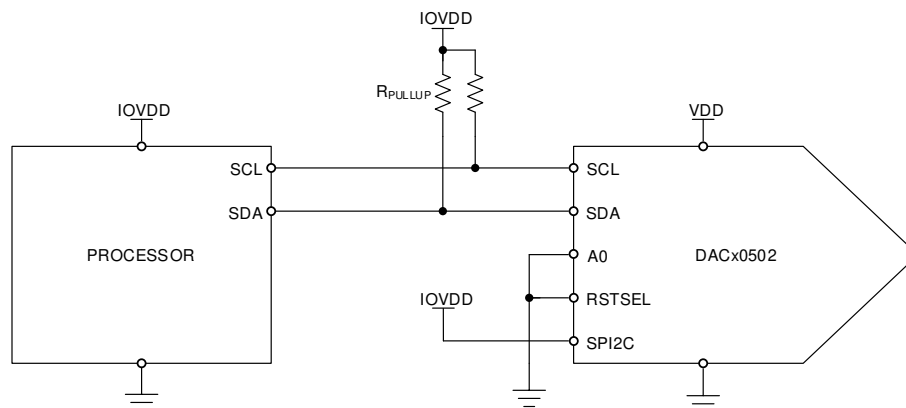
The DACx0502 provides a 3-wire serial peripheral interface (SPI). The connections can be made to a processor, as shown in [图 75](#). Connect the SPI2C pin to ground either directly or through a pulldown resistor. Pull the RSTSEL pin low or high based on the desired output state at power-up. Use a pullup resistor on the SYNC signal so that the signal is high by default. Use termination resistors at the digital source so that the transmission line reflections are minimized. The source termination resistors also help in slowing down the rise and fall times of the digital signals, and in turn, help in minimizing the digital feedthrough of the DAC.



**图 75. SPI Connection to a Processor**

### 9.3.2 I<sup>2</sup>C Interface Connection to a Processor

The I<sup>2</sup>C interface on DACx0502 provides a slave address selection pin A0 in addition to the standard SCL and SDA signals. The A0 can be configured to provide four slave addresses, as specified in [表 3](#). Pull up the SCL and SDA pins, as shown in [图 76](#). The pullup resistor must be selected considering the parasitic capacitance of the I<sup>2</sup>C bus on the printed circuit board (PCB). A small resistance provides better speed, but at the cost of increased power consumption.



**图 76. I<sup>2</sup>C Interface Connection to a Processor**

## 9.4 What To Do and What Not To Do

### 9.4.1 What To Do

- When using an external reference, disable the internal reference. This step must be the first step after power on, especially when the external reference is greater than the 2.5-V internal reference.
- Maintain the required headroom between the reference voltage and VDD.
- Use the reference divider when the headroom exceeds the limit.

### 9.4.2 What Not To Do

- Do not use an external reference when the internal reference is on. There is no current limit on the internal reference.

## 9.5 Initialization Setup

The DACx0502 requires a simple software initialization process based on the interface, power supply, and reference selection. The initialization steps are as follows:

1. When using an external reference, disable the internal reference.
2. Divide the reference by two when the reference voltage exceeds the headroom required from VDD. For example, when using 3.3-V VDD and the internal reference of 2.5 V, the DAC outputs are disabled unless the reference is divided by two.
3. Set the output gain.
4. Write to the DAC register.

The following text shows the pseudocode to get started with the DACx0502:

```
//SPI Settings
//Mode: Mode-1 (CPOL: 0, CPHA: 1)
//CS Type: Active Low, Per Packet
//Frame length: 24

//SYNTAX: <WRITE REGISTER (HEX ADDRESS)>, <HEX DATA>
//Disable internal reference (only in case of external reference)
WRITE CONFIG (0x03), 0x0100
//Select REFDIV=1 (reference divided by 2) and GAIN=1 (gain at both the DAC outputs is 2)
WRITE GAIN (0x04), 0x0103
//Write mid-code to DACA
WRITE DAC-A (0x08), 0x7FFF
//Write Full-code to DACB
WRITE DAC-B (0x09), 0xFFFF
```

## 10 Power Supply Recommendations

The DACx0502 operate within the specified VDD supply range of 2.7 V to 5.5 V. The DACx0502 do not require specific supply sequencing. The VDD supply must be well regulated and low noise. Switching power supplies and DC/DC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components create similar high-frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. To further minimize noise from the power supply, include a 1- $\mu\text{F}$  to 10- $\mu\text{F}$  capacitor and 0.1- $\mu\text{F}$  bypass capacitor. The current consumption on the VDD pin, the short-circuit current limit, and the load current for the device is listed in the [Electrical Characteristics](#) section. The power supply must meet the aforementioned current requirements.

## 11 Layout

### 11.1 Layout Guidelines

A precision analog component requires careful layout. The following list provides some insight into good layout practices.

- Bypass the VDD to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1- $\mu\text{F}$  to 0.22- $\mu\text{F}$  ceramic capacitor, with a X7R or NP0 dielectric.
- Place power supplies and REF bypass capacitors close to the pins to minimize inductance and optimize performance.
- Use a high-quality, ceramic-type NP0 or X7R for optimal performance across temperature, and a very low dissipation factor.
- The digital and analog sections must have proper placement with respect to the digital pins and analog pins of the DACx0502 devices. The separation of analog and digital blocks minimizes coupling into neighboring blocks, as well as interaction between analog and digital return currents.

### 11.2 Layout Example

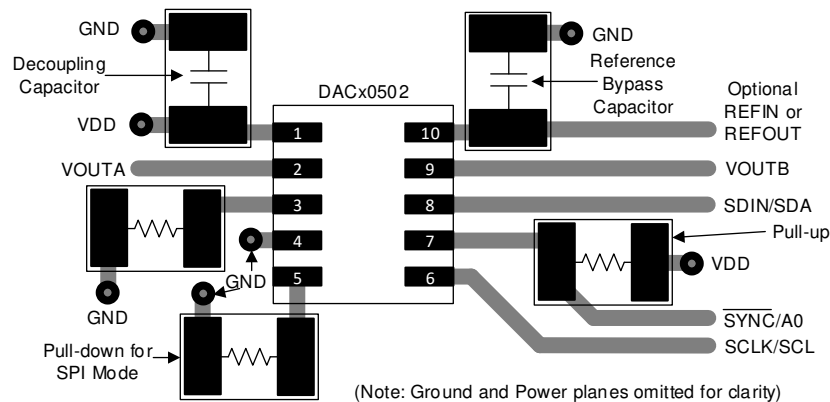


图 77. Layout Example

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

请参阅如下相关文档: [DAC80502EVM 用户指南](#)

### 12.2 相关链接

**表 19** 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

**表 19. 相关链接**

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
DAC80502	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
DAC70502	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
DAC60502	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>

### 12.3 接收文档更新通知

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.7 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC60502DRXR	ACTIVE	WSON	DRX	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D652	<a href="#">Samples</a>
DAC60502DRXT	ACTIVE	WSON	DRX	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D652	<a href="#">Samples</a>
DAC70502DRXR	ACTIVE	WSON	DRX	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D752	<a href="#">Samples</a>
DAC70502DRXT	ACTIVE	WSON	DRX	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D752	<a href="#">Samples</a>
DAC80502DRXR	ACTIVE	WSON	DRX	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D852	<a href="#">Samples</a>
DAC80502DRXT	ACTIVE	WSON	DRX	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D852	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC60502DRXR	WSON	DRX	10	3000	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2
DAC60502DRXT	WSON	DRX	10	250	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2
DAC70502DRXR	WSON	DRX	10	3000	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2
DAC70502DRXT	WSON	DRX	10	250	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2
DAC80502DRXR	WSON	DRX	10	3000	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2
DAC80502DRXT	WSON	DRX	10	250	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC60502DRXR	WSON	DRX	10	3000	205.0	200.0	33.0
DAC60502DRXT	WSON	DRX	10	250	205.0	200.0	33.0
DAC70502DRXR	WSON	DRX	10	3000	205.0	200.0	33.0
DAC70502DRXT	WSON	DRX	10	250	205.0	200.0	33.0
DAC80502DRXR	WSON	DRX	10	3000	205.0	200.0	33.0
DAC80502DRXT	WSON	DRX	10	250	205.0	200.0	33.0

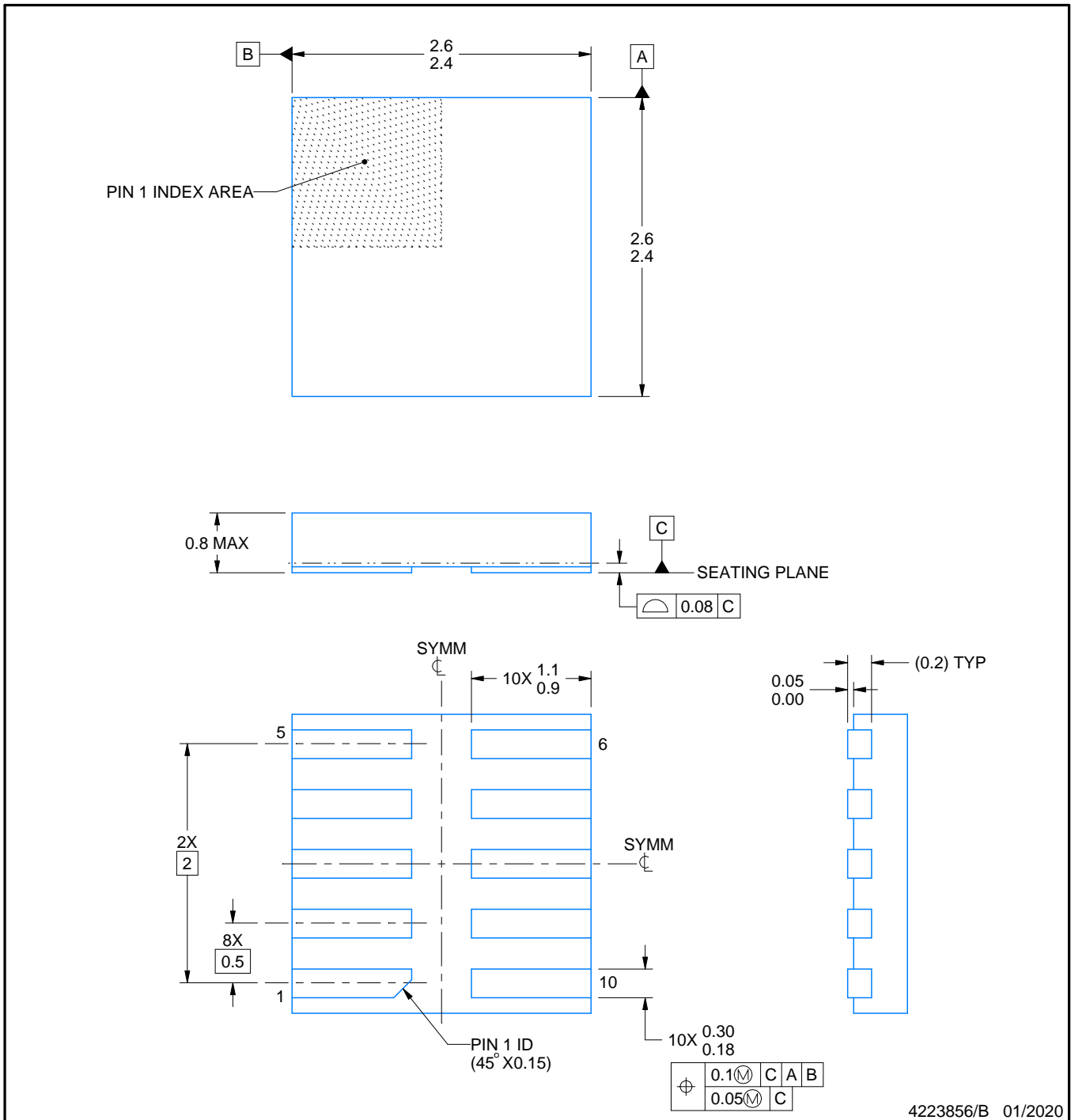
# DRX0010A



# PACKAGE OUTLINE

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



### NOTES:

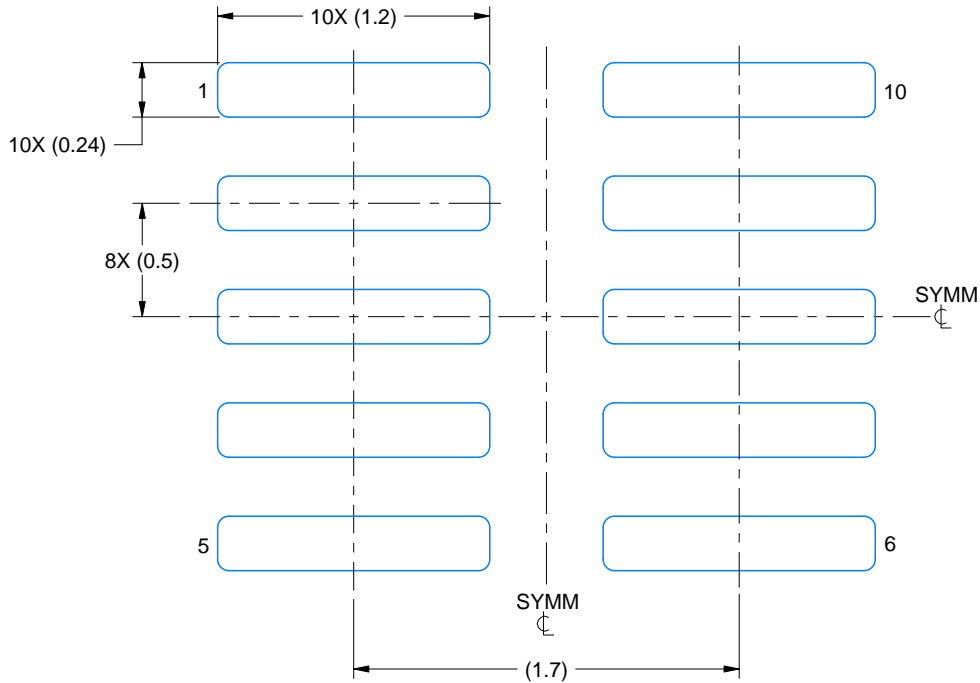
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

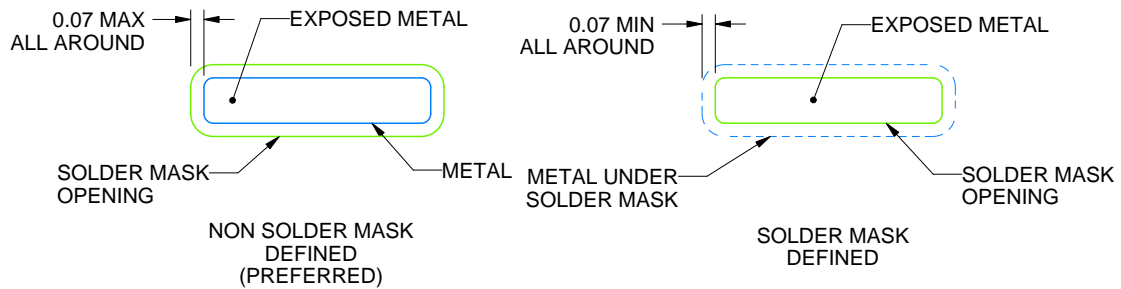
DRX0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:30X



**SOLDER MASK DETAILS**

4223856/B 01/2020

NOTES: (continued)

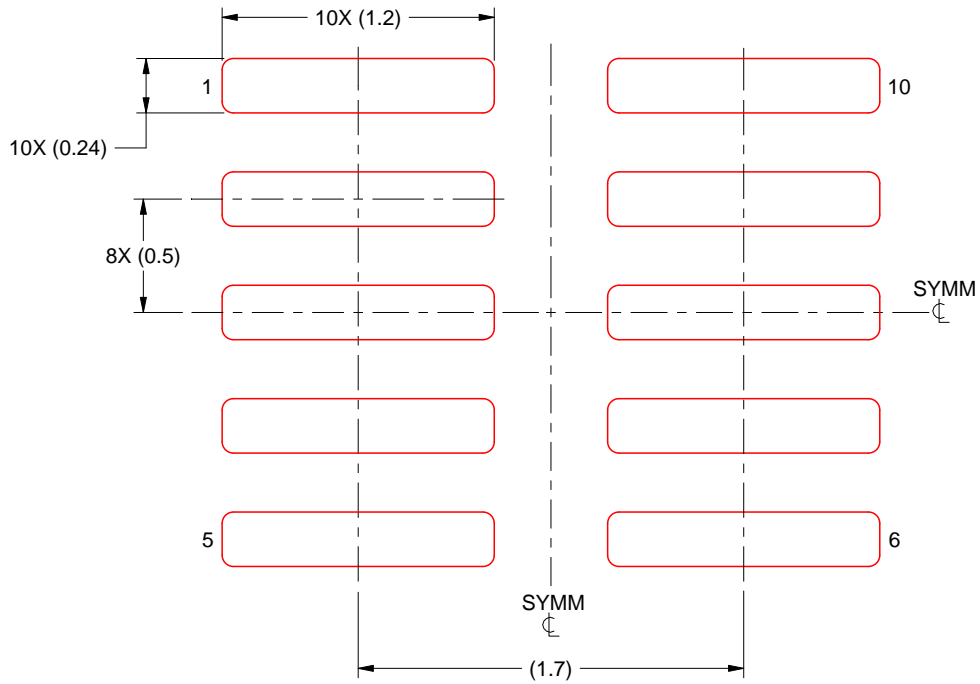
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DRX0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4223856/B 01/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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[ISL5927IN](#) [ISL5961IA](#) [TLV5614IDR](#) [AD5689RBRUZ-RL7](#) [AD7528JPZ-REEL](#) [AD5064BRUZ-1REEL7](#) [AD5664RBRMZ-5REEL7](#)  
[MS5620](#) [DAC60508ZRTER](#) [DAC8411IDCKR](#) [AD5676RARUZ-REEL7](#) [LTC2654BIGN-L16#PBF](#) [AD5781ARUZ-REEL7](#)  
[AD5667RBRMZ-2REEL7](#) [AD5686RBRUZ-RL7](#) [AD5696BRUZ-RL7](#) [MS5314](#) [DAC8560IDDGKR](#) [DAC81401PWR](#) [DAC8728SPAGR](#)  
[ADV7125BCPZ170-RL](#) [LTC2642CMS-12#TRPBF](#) [AD5413BCPZ-RL7](#) [AD5541ARZ-REEL7](#) [AD5732AREZ-REEL7](#) [AD5640CRMZ-](#)  
[2REEL7](#) [LTC2642CMS-16#TRPBF](#) [AD5781BRUZ-REEL7](#) [LTC1658IMS8#TRPBF](#) [AD5674RBCPZ-1-RL7](#) [AD5667RBRMZ-1REEL7](#)  
[AD5449YRUZ-REEL](#) [LTC2621IDD-1#TRPBF](#) [LTC2633AHTS8-LI12#TRMPBF](#) [CLM5615ID](#) [MS5541](#) [MS4344](#) [MS5542](#) [MS9708](#)