DLP2010 .2 WVGA DMD

1 特性

- 0.2 英寸 (5.29mm) 对角线微镜阵列
  - 在正交布局中显示 854 × 480 像素阵列
  - 5.4 微米微镜间距
  - ±17° 微镜倾斜度（相对于平坦表面）
  - 采用侧面照明，实现最优的效率和光学引擎尺寸
  - 偏振无关型铝微镜表面
- 4 位 SubLVDS 输入数据总线
- 专用 DLPC3430 或 DLPC3435 显示控制器以及 DLPA200x/DLPA3000 PMIC 和 LED 驱动器，确保可靠运行

2 应用

- 产品嵌入式显示屏，包括：
  - 平板电脑、移动电话
  - 人工智能 (AI) 助理、智能音箱
- 控制面板、安防系统和恒温器
- 可穿戴显示器

3 说明

DLP2010 数字微镜器件 (DMD) 是一款数控微光机电系统 (MOEMS) 空间照明调制器 (SLM)。当与适当的光学系统配合使用时，此 DMD 可显示图像、视频和图案。此器件是由 DLP2010 DMD、DLPC3430 或 DLPC3435 控制器以及 DLPA200x/DLPA3000 PMIC/LED 驱动器组成的芯片组的一个组件。此 DMD 紧凑的物理尺寸适合用于注重小外形尺寸和低功耗的便携式设备。紧凑的封装与 LED 的小尺寸相得益彰，是空间受限型光引擎的理想选择。

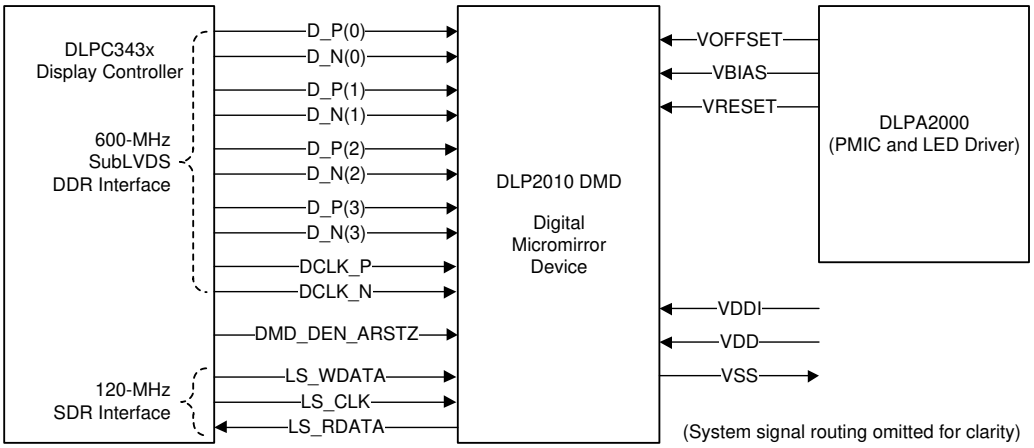
请访问 TI DLP®PicoTM 显示技术入门页，了解如何开始使用 DLP2010。

生态系统包含现成的资源，可帮助用户加快设计周期。这些资源包括可直接用于量产环境的光学模块、光学模块制造商和设计公司。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
DLP2010	FQJ (40)	15.9mm × 5.3mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



0.2 WVGA 芯片组

Table of Contents

4 Revision History

Changes from Revision A (January 2022) to Revision B (May 2022) **Page**

- Updated Absolute Maximum Ratings disclosure to the latest TI standard 6
- Updated *Micromirror Array Optical Characteristics* 18
- Added *Third-Party Products Disclaimer* 36

Changes from Revision * (February 2019) to Revision A (January 2022) **Page**

- 更新了整个文档中的表、图和交叉参考的编号格式 1
- Updated $|T_{DELTA}|$ MAX from 30°C to 15°C 7

5 Pin Configuration and Functions

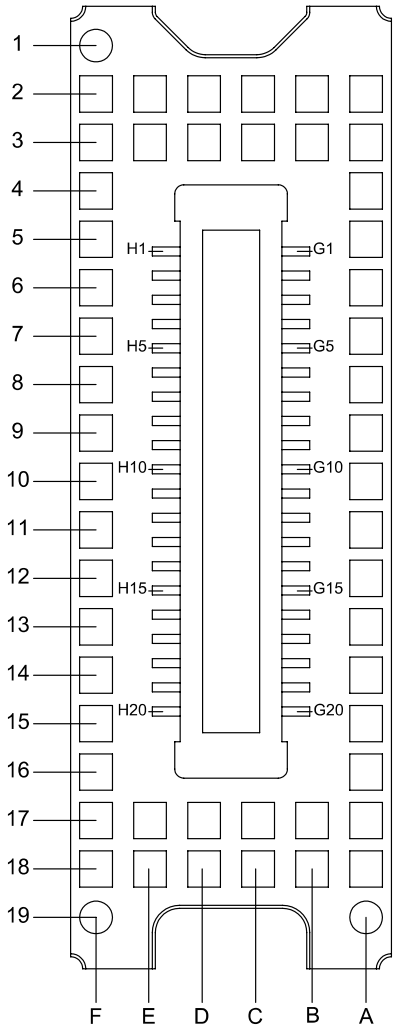


图 5-1. FQJ Package 40-Pin Connector Bottom View

表 5-1. Pin Functions – Connector Pins(1)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH(2) (mm)
NAME	NO.					
DATA INPUTS						
D_N(0)	G4	I	SubLVDS	Double	Data, Negative	7.03
D_P(0)	G3	I	SubLVDS	Double	Data, Positive	7.03
D_N(1)	G8	I	SubLVDS	Double	Data, Negative	7.03
D_P(1)	G7	I	SubLVDS	Double	Data, Positive	7.03
D_N(2)	H5	I	SubLVDS	Double	Data, Negative	7.02
D_P(2)	H6	I	SubLVDS	Double	Data, Positive	7.02
D_N(3)	H1	I	SubLVDS	Double	Data, Negative	7.00
D_P(3)	H2	I	SubLVDS	Double	Data, Positive	7.00
DCLK_N	H9	I	SubLVDS	Double	Clock, Negative	7.03
DCLK_P	H10	I	SubLVDS	Double	Clock, Positive	7.03
CONTROL INPUTS						

表 5-1. Pin Functions – Connector Pins[1] (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[2] (mm)
NAME	NO.					
DMD_DEN_ARSTZ	G12	I	LPSDR[1]		Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.	5.72
LS_CLK	G19	I	LPSDR	Single	Clock for low-speed interface	3.54
LS_WDATA	G18	I	LPSDR	Single	Write data for low-speed interface	3.54
LS_RDATA	G11	O	LPSDR	Single	Read data for low-speed interface	8.11
POWER						
VBIAS[3]	H17	Power			Supply voltage for positive bias level at micromirrors	
VOFFSET[3]	H13	Power			Supply voltage for HVCMOS core logic. Includes: supply voltage for stepped high level at micromirror address electrodes and supply voltage for offset level at micromirrors	
VRESET[3]	H18	Power			Supply voltage for negative reset level at micromirrors	
VDD[3]	G20	Power			Supply voltage for micromirror low voltage CMOS core logic includes supply voltage for LPSDR inputs and supply voltage for normal high level at micromirror address electrodes.	
VDD	H14	Power				
VDD	H15	Power				
VDD	H16	Power				
VDD	H19	Power				
VDD	H20	Power				
VDDI[3]	G1	Power			Supply voltage for SubLVDS receivers	
VDDI	G2	Power				
VDDI	G5	Power				
VDDI	G6	Power				
VSS[3]	G9	Ground			Ground. Common return for all power.	
VSS	G10	Ground				
VSS	G13	Ground				
VSS	G14	Ground				
VSS	G15	Ground				
VSS	G16	Ground				
VSS	G17	Ground				
VSS	H3	Ground				
VSS	H4	Ground				
VSS	H7	Ground				
VSS	H8	Ground				
VSS	H11	Ground				
VSS	H12	Ground				

(1) Low speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.
(2) Net trace lengths inside the package:
Relative dielectric constant for the FQJ ceramic package is 9.8.
Propagation speed = 11.8 / sqrt(9.8) = 3.769 inches/ns.
Propagation delay = 0.265 ns/inch = 265 ps/inch = 10.43 ps/mm.
(3) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.

表 5-2. Pin Functions – Test Pads

NUMBER	SYSTEM BOARD	NUMBER	SYSTEM BOARD
A2	Do not connect	D2	Do not connect
A3	Do not connect	D3	Do not connect
A4	Do not connect	D17	Do not connect
A5	Do not connect	D18	Do not connect
A6	Do not connect		
A7	Do not connect	E2	Do not connect
A8	Do not connect	E3	Do not connect
A9	Do not connect	E17	Do not connect
A10	Do not connect	E18	Do not connect
A11	Do not connect		
A12	Do not connect	F1	Do not connect
A13	Do not connect	F2	Do not connect
A14	Do not connect	F3	Do not connect
A15	Do not connect	F4	Do not connect
A16	Do not connect	F5	Do not connect
A17	Do not connect	F6	Do not connect
A18	Do not connect	F7	Do not connect
A19	Do not connect	F8	Do not connect
		F9	Do not connect
B2	Do not connect	F10	Do not connect
B3	Do not connect	F11	Do not connect
B17	Do not connect	F12	Do not connect
B18	Do not connect	F13	Do not connect
		F14	Do not connect
C2	Do not connect	F15	Do not connect
C3	Do not connect	F16	Do not connect
C17	Do not connect	F17	Do not connect
C18	Do not connect	F18	Do not connect
		F19	Do not connect

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

			MIN	MAX	UBIT
Supply voltage	VDD	for LVCMOS core logic(2) Supply voltage for LPSDR low speed interface	– 0.5	2.3	V
	VDDI	for SubLVDS receivers(2)	– 0.5	2.3	
	VOFFSET	for HVCMOS and micromirror electrode(2) (3)	– 0.5	10.6	
	VBIAS	for micromirror electrode(2)	– 0.5	19	
	VRESET	for micromirror electrode(2)	– 15	0.5	
	| VDDI – VDD |	delta (absolute value)(4)		0.3	
	| VBIAS – VOFFSET |	delta (absolute value)(5)		11	
	| VBIAS – VRESET |	delta (absolute value)(6)		34	
Input voltage	for other inputs LPSDR(2)		– 0.5	VDD + 0.5	V
	for other inputs SubLVDS(2) (7)		– 0.5	VDDI + 0.5	
Input pins	| VID |	SubLVDS input differential voltage (absolute value)(7)		810	mV
	IID	SubLVDS input differential current		8.1	mA
Clock frequency	f_{clock}	Clock frequency for low speed interface LS_CLK		130	MHz
	f_{clock}	Clock frequency for high speed interface DCLK		620	
Environmental	T_{ARRAY} and T_{WINDOW}	Temperature – operational(8)	– 20	90	°C
		Temperature – non-operational(8)	– 40	90	
	T_{DP}	Dew Point Temperature - operating and non-operating (non-condensing)		81	
	$\|T_{DELTA}\|$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1(9)		30	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the ground terminals (VSS). The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET.
(3) VOFFSET supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable absolute voltage difference between VDDI and VDD may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between VBIAS and VOFFSET may result in excessive current draw.
(6) Exceeding the recommended allowable absolute voltage difference between VBIAS and VRESET may result in excessive current draw.
(7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) The highest temperature of the active array (as calculated by the 节 7.6), or of any point along the Window Edge as defined in 图 7-1. The locations of thermal test points TP2 and TP3 in 图 7-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 图 7-1. The window test points TP2 and TP3 shown in 图 7-1 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

6.2 Storage Conditions

applicable for the DMD as a component or non-operational in a system

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	– 40	85	°C
T_{DP-AVG}	Average dew point temperature, (non-condensing)(1)		24	°C
T_{DP-ELR}	Elevated dew point temperature range, (non-condensing)(2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		6	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE(4)					
VDD	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.65	1.8	1.95	V
VDDI	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode(5)	9.5	10	10.5	V
VBIAS	Supply voltage for mirror electrode	17.5	18	18.5	V
VRESET	Supply voltage for micromirror electrode	– 14.5	– 14	– 13.5	V
|VDDI – VDD|	Supply voltage delta (absolute value)(6)			0.3	V
|VBIAS – VOFFSET|	Supply voltage delta (absolute value)(7)			10.5	V
|VBIAS – VRESET|	Supply voltage delta (absolute value)(8)			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low speed interface LS_CLK(9)	108		120	MHz
f_{clock}	Clock frequency for high speed interface DCLK(10)	300		600	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFACE(10)					
$\lvert V_{ID} \rvert$	SubLVDS input differential voltage (absolute value) 图 6-8, 图 6-9	150	250	350	mV
V_{CM}	Common mode voltage 图 6-8, 图 6-9	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage 图 6-8, 图 6-9	575		1225	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance 图 6-10	80	100	120	Ω
	100-Ω differential PCB trace	6.35		152.4	mm

6.4 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	NOM	MAX	UNIT
ENVIRONMENTAL					
T_{ARRAY}	Array Temperature – long-term operational(11) (12) (13) (14)	0		40 to 70(13)	°C
	Array Temperature - short-term operational, 25 hr max(12) (15)	–20		–10	
	Array Temperature - short-term operational, 500 hr max(12) (15)	–10		0	
	Array Temperature – short-term operational, 500 hr max(12) (15)	70		75	
$\lvert T_{DELTA} \rvert$	Absolute Temperature difference between any point on the window edge and the ceramic test point TP1 (16)			15	°C
T_{WINDOW}	Window temperature – operational(11) (17)			90	°C
T_{DP-AVG}	Average dew point temperature (non-condensing)(18)			24	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)(19)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			6	Months
ILL_{UV}	Illumination wavelengths < 420 nm(11)			0.68	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 420 nm and 700 nm			Thermally limited	
ILL_{IR}	Illumination wavelengths > 700 nm			10	mW/cm^2
ILL_{θ}	Illumination marginal ray angle(20)			55	deg

(1) 节 6.4 are applicable after the DMD is installed in the final product.
(2) The functional performance of the device specified in this datasheet is achieved when operating the device within the limits defined by the 节 6.4. No level of performance is implied when operating the device above or below the 节 6.4 limits.
(3) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET.
(4) All voltage values are with respect to the ground pins (VSS).
(5) VOFFSET supply transients must fall within specified maximum voltages.
(6) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.
(7) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(8) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit.
(9) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(10) Refer to the SubLVDS timing requirements in 节 6.7.
(11) Simultaneous exposure of the DMD to the maximum 节 6.4 for temperature and UV illumination will reduce device lifetime.
(12) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 图 7-1 and the Package Thermal Resistance using 节 7.6.
(13) Per 图 6-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to 节 7.7 for a definition of micromirror landed duty cycle.
(14) Long-term is defined as the usable life of the device
(15) Short-term is the total cumulative time over the useful life of the device.
(16) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in 图 7-1. The window test points TP2 and TP3 shown in 图 7-1 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(17) Window temperature is the highest temperature on the window edge shown in 图 7-1. The locations of thermal test points TP2 and TP3 in 图 7-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(18) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(19) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
(20) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including Pond of Micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.

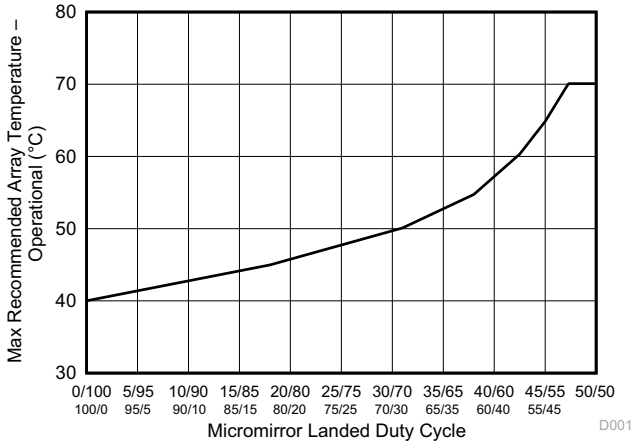


图 6-1. Maximum Recommended Array Temperature – Derating Curve

6.5 Thermal Information

THERMAL METRIC(1)	DLP2010 FQJ Package 40 PINS	UNIT
Thermal resistance Active area to test point 1 (TP1)(1)	7.9	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the 节 6.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: VDD(3) (4)	VDD = 1.95 V			34.7	mA
		VDD = 1.8 V		27.5		
I_{DDI}	Supply current: VDDI(3) (4)	VDDI = 1.95 V			9.4	mA
		VDD = 1.8 V		6.6		
I_{OFFSET}	Supply current: VOFFSET(5) (6)	VOFFSET = 10.5 V			1.7	mA
		VOFFSET = 10 V		0.9		
I_{BIAS}	Supply current: VBIAS(5) (6)	VBIAS = 18.5 V			0.4	mA
		VBIAS = 18 V		0.2		
I_{RESET}	Supply current: VRESET(6)	VRESET = – 14.5 V			2	mA
		VRESET = – 14 V		1.2		
POWER(7)						
P_{DD}	Supply power dissipation: VDD(3) (4)	VDD = 1.95 V			67.7	mW
		VDD = 1.8 V		49.5		
P_{DDI}	Supply power dissipation: VDDI(3) (4)	VDDI = 1.95 V			18.3	mW
		VDD = 1.8 V		11.9		
P_{OFFSET}	Supply power dissipation: VOFFSET(5) (6)	VOFFSET = 10.5 V			17.9	mW
		VOFFSET = 10 V		9		
P_{BIAS}	Supply power dissipation: VBIAS(5) (6)	VBIAS = 18.5 V			7.4	mW
		VBIAS = 18 V		3.6		

6.6 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
P_{RESET}	Supply power dissipation: VRESET(6)	VRESET = –14.5 V			29	mW
		VRESET = –14 V		16.8		
P_{TOTAL}	Supply power dissipation: Total			90.8	140.3	mW
LPSDR INPUT(8)						
$V_{IH(DC)}$	DC input high voltage(9)		0.7 × VDD		VDD + 0.3	V
$V_{IL(DC)}$	DC input low voltage(9)		–0.3		0.3 × VDD	V
$V_{IH(AC)}$	AC input high voltage(9)		0.8 × VDD		VDD + 0.3	V
$V_{IL(AC)}$	AC input low voltage(9)		–0.3		0.2 × VDD	V
ΔV_T	Hysteresis (V_{T+} – V_{T-})	图 6-11	0.1 × VDD		0.4 × VDD	V
I_{IL}	Low–level input current	VDD = 1.95 V; V_I = 0 V	–100			nA
I_{IH}	High–level input current	VDD = 1.95 V; V_I = 1.95 V			100	nA
LPSDR OUTPUT(10)						
V_{OH}	DC output high voltage	I_{OH} = –2 mA	0.8 × VDD			V
V_{OL}	DC output low voltage	I_{OL} = 2 mA			0.2 × VDD	V
CAPACITANCE						
C_{IN}	Input capacitance LPSDR	f = 1 MHz			10	pF
	Input capacitance SubLVDS	f = 1 MHz			20	
C_{OUT}	Output capacitance	f = 1 MHz			10	pF
C_{RESET}	Reset group capacitance	f = 1 MHz; (480 × 108) micromirrors	95		113	pF

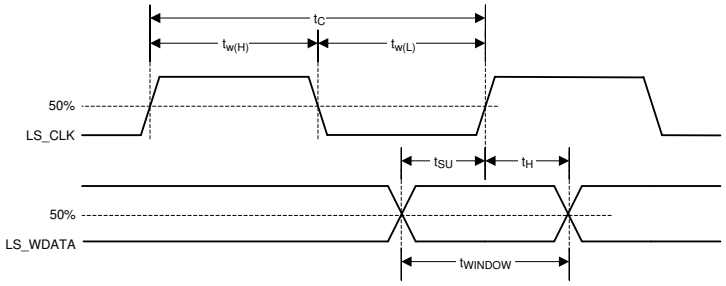
(1) Device electrical characteristics are over 节 6.4 unless otherwise noted.
(2) All voltage values are with respect to the ground pins (VSS).
(3) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.
(4) Supply power dissipation based on non–compressed commands and data.
(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(6) Supply power dissipation based on 3 global resets in 200 µs.
(7) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.
(8) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate* (LPDDR) JESD209B.
(10) LPSDR specification is for pin LS_RDATA.

6.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

			MIN	NOM	MAX	UNIT
LPSDR						
t_R	Rise slew rate(1)	(30% to 80%) × VDD, 图 6-3	1		3	V/ns
t_F	Fall slew rate(1)	(70% to 20%) × VDD, 图 6-3	1		3	V/ns
t_R	Rise slew rate(2)	(20% to 80%) × VDD, 图 6-3	0.25			V/ns
t_F	Fall slew rate(2)	(80% to 20%) × VDD, 图 6-3	0.25			V/ns
t_C	Cycle time LS_CLK,	图 6-2	7.7	8.3		ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points, 图 6-2	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points, 图 6-2	3.1			ns
t_{SU}	Setup time	LS_WDATA valid before LS_CLK ↑, 图 6-2	1.5			ns
t_H	Hold time	LS_WDATA valid after LS_CLK ↑, 图 6-2	1.5			ns
t_{WINDOW}	Window time(1) (3)	Setup time + Hold time, 图 6-2	3.0			ns
$t_{DERATING}$	Window time derating(1) (3)	For each 0.25 V/ns reduction in slew rate below 1 V/ns, 图 6-5		0.35		ns
SubLVDS						
t_R	Rise slew rate	20% to 80% reference points, 图 6-4	0.7	1		V/ns
t_F	Fall slew rate	80% to 20% reference points, 图 6-4	0.7	1		V/ns
t_C	Cycle time LS_CLK,	图 6-6	1.61	1.67		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points, 图 6-6	0.71			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points, 图 6-6	0.71			ns
t_{SU}	Setup time	D(0:3) valid before DCLK ↑ or DCLK ↓, 图 6-6				
t_H	Hold time	D(0:3) valid after DCLK ↑ or DCLK ↓, 图 6-6				
t_{WINDOW}	Window time	Setup time + Hold time, 图 6-6, 图 6-7	3.0			ns
$t_{LVDS-ENABLE+REFGEN}$	Power-up receiver(4)				2000	ns

(1) Specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in 图 6-3.
(2) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in 图 6-3.
(3) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 to 3.7 ns.
(4) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.



A. Low-speed interface is LPSDR and adheres to the 节 6.6 and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

图 6-2. LPSDR Switching Parameters

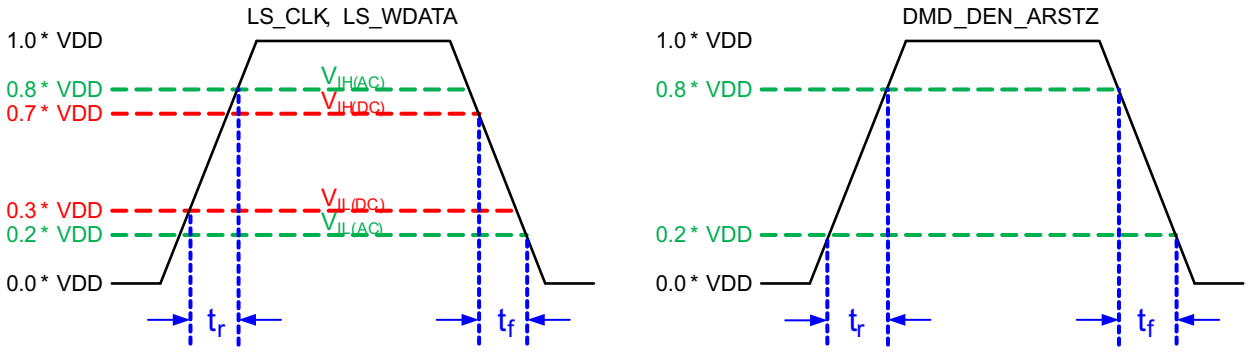


图 6-3. LPSDR Input Rise and Fall Slew Rate

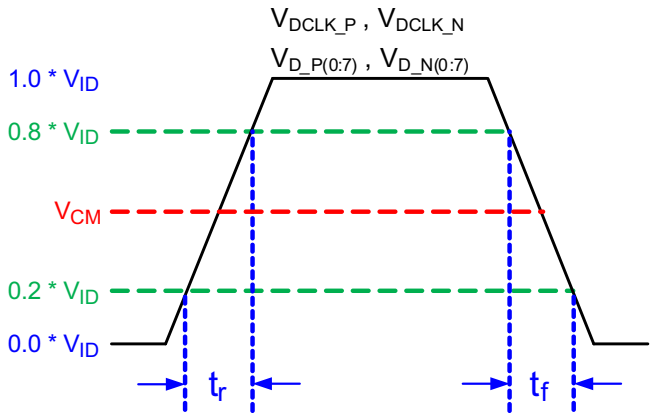


图 6-4. SubLVDS Input Rise and Fall Slew Rate

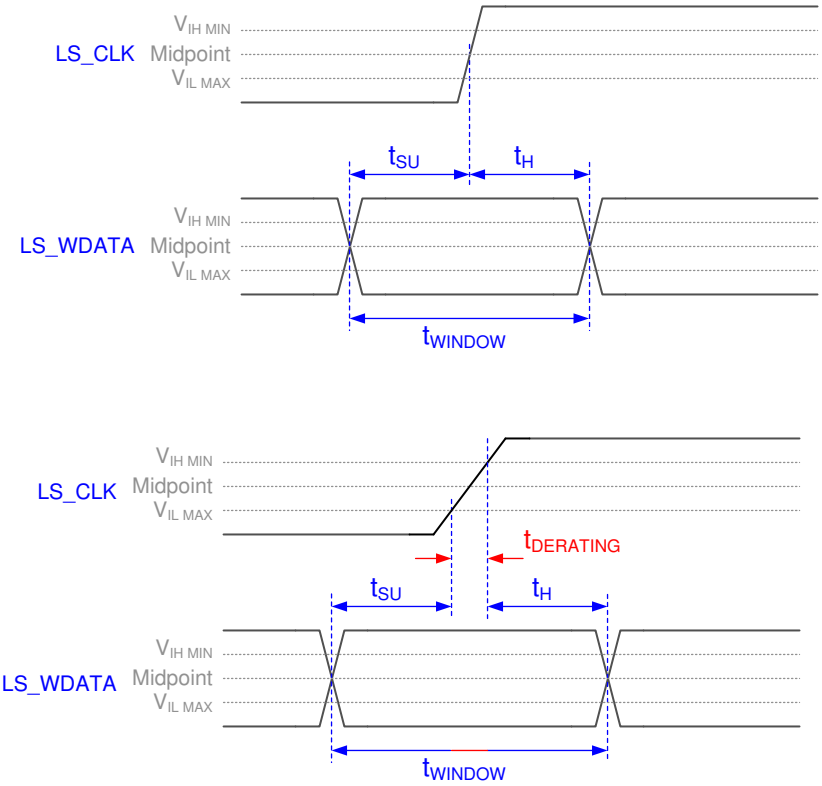


图 6-5. Window Time Derating Concept

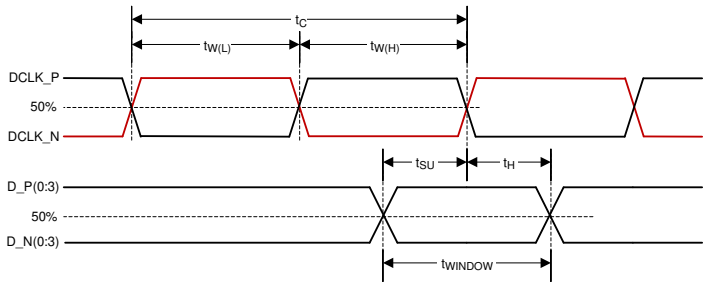
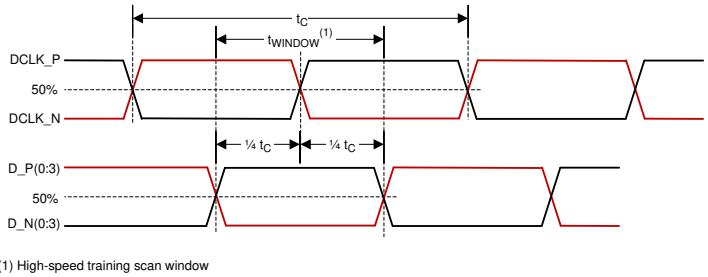


图 6-6. SubLVDS Switching Parameters



Note: Refer to 节 7.3.3 for details.

图 6-7. High-Speed Training Scan Window

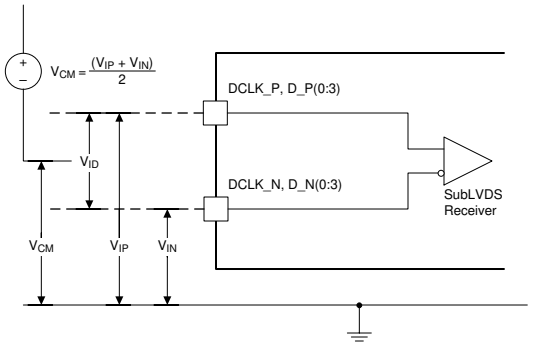
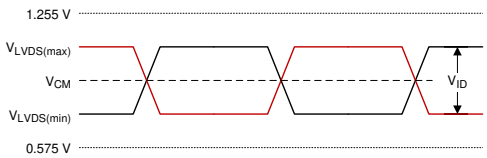


图 6-8. SubLVDS Voltage Parameters



A. $V_{SubLVDS(max)} = V_{CM(max)} + | ½ \times V_{ID(max)} |$

B. $V_{SubLVDS(min)} = V_{CM(min)} - | ½ \times V_{ID(max)} |$

图 6-9. SubLVDS Waveform Parameters

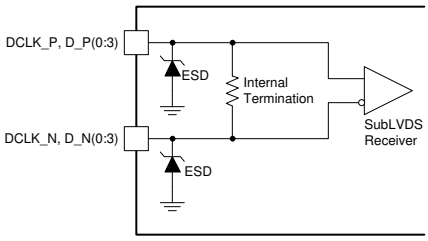


图 6-10. SubLVDS Equivalent Input Circuit

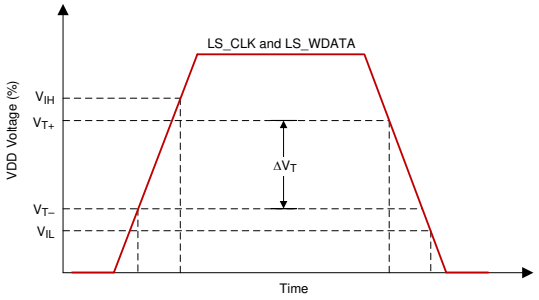


图 6-11. LPSDR Input Hysteresis

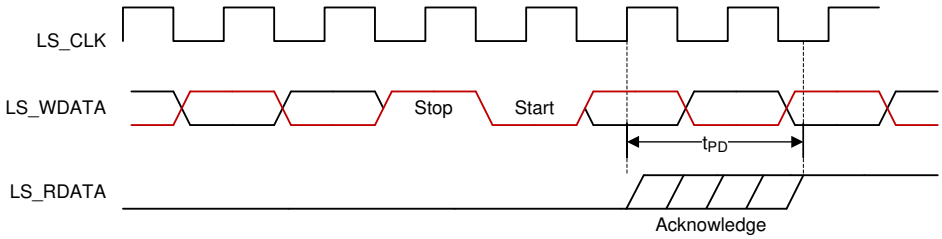
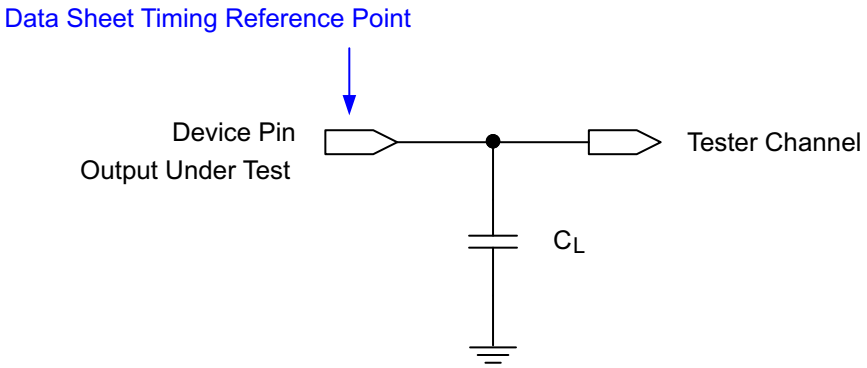


图 6-12. LPSDR Read Out



A. See 节 7.3.4 for more information.

图 6-13. Test Load Circuit for Output Propagation Measurement

6.8 Switching Characteristics(1)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, Clock to Q, rising edge of LS_CLK input to LS_RDATA output. 图 6-12	C_L = 45 pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns

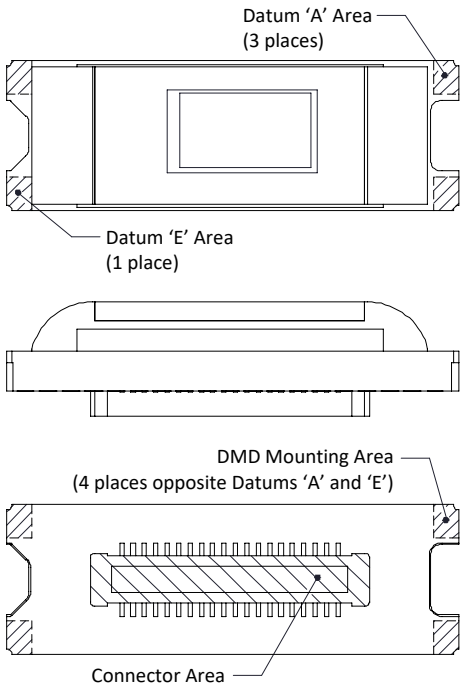
Over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output duty cycle distortion, LS_RDATA		40%		60%	

(1) Device electrical characteristics are over 节 6.4 unless otherwise noted.

6.9 System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:	Connector area (see 图 6-14)			45	N
	DMD mounting area uniformly distributed over 4 areas (see 图 6-14)			100	N



6.10 Physical Characteristics of the Micromirror Array

PARAMETER		VALUE	UNIT
Number of active columns	See 图 6-15	854	micromirrors
Number of active rows	See 图 6-15	480	micromirrors
Micromirror (pixel) pitch	See 图 6-16	5.4	µm
Micromirror active array width	Micromirror pitch × number of active columns; see 图 6-15	4.6116	mm
Micromirror active array height	Micromirror pitch × number of active rows; see 图 6-15	2.592	mm
Micromirror active border	Pond of micromirror (POM)(1)	20	micromirrors/side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

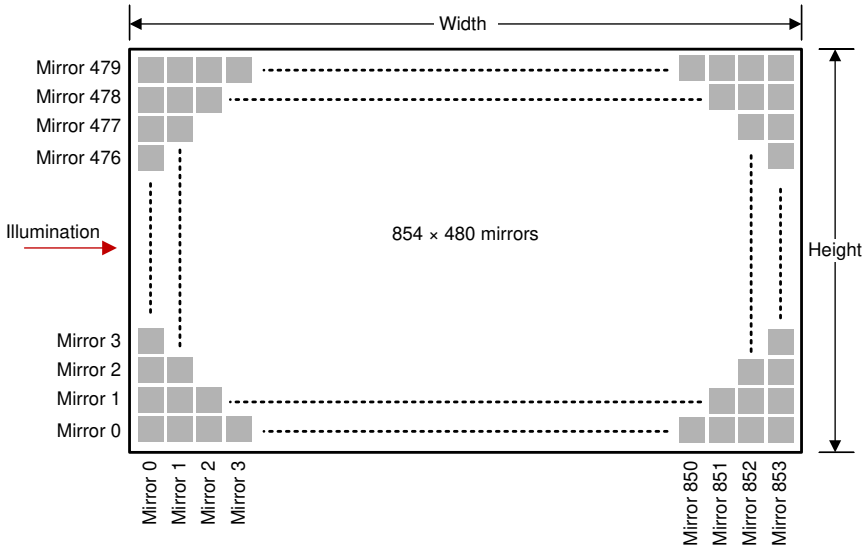


图 6-15. Micromirror Array Physical Characteristics

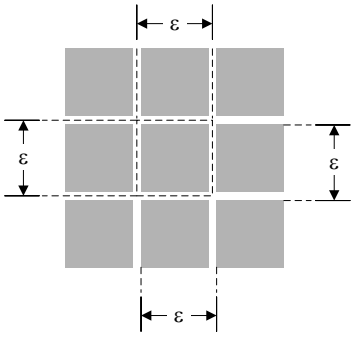


图 6-16. Mirror (Pixel) Pitch

6.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle		DMD landed state(1)		17		degrees
Micromirror tilt angle tolerance(2) (3) (4) (5)			–1.4		1.4	degrees
Micromirror tilt direction(6) (7)		Landed ON state		180		degrees
		Landed OFF state		270		
Micromirror crossover time(8)		Typical Performance		1	3	µs
Micromirror switching time(9)		Typical Performance	10			
Image performance(10)	Bright pixel(s) in active area (11)	Gray 10 Screen (12)			0	micromirrors
	Bright pixel(s) in the POM (13)	Gray 10 Screen (12)			1	
	Dark pixel(s) in the active area (14)	White Screen			4	
	Adjacent pixel(s) (15)	Any Screen			0	
	Unstable pixel(s) in active area (16)	Any Screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON state direction. A binary value of 0 results in a micromirror landing in the OFF state direction. See 图 6-17
(7) Micromirror tilt direction is measured as in a typical polar coordinate system: Measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
(8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(9) The minimum time between successive transitions of a micromirror.
(10) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
Test set degamma shall be linear
Test set brightness and contrast shall be set to nominal
The diagonal size of the projected image shall be a minimum of 20 inches
The projections screen shall be 1X gain
The projected image shall be inspected from a 38 inch minimum viewing distance
The image shall be in focus during all image quality tests
(11) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
(12) Gray 10 screen definition: All areas of the screen are colored with the following settings:
Red = 10/255
Green = 10/255
Blue = 10/255
(13) POM definition: Rectangular border of off-state mirrors surrounding the active area
(14) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
(15) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
(16) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image

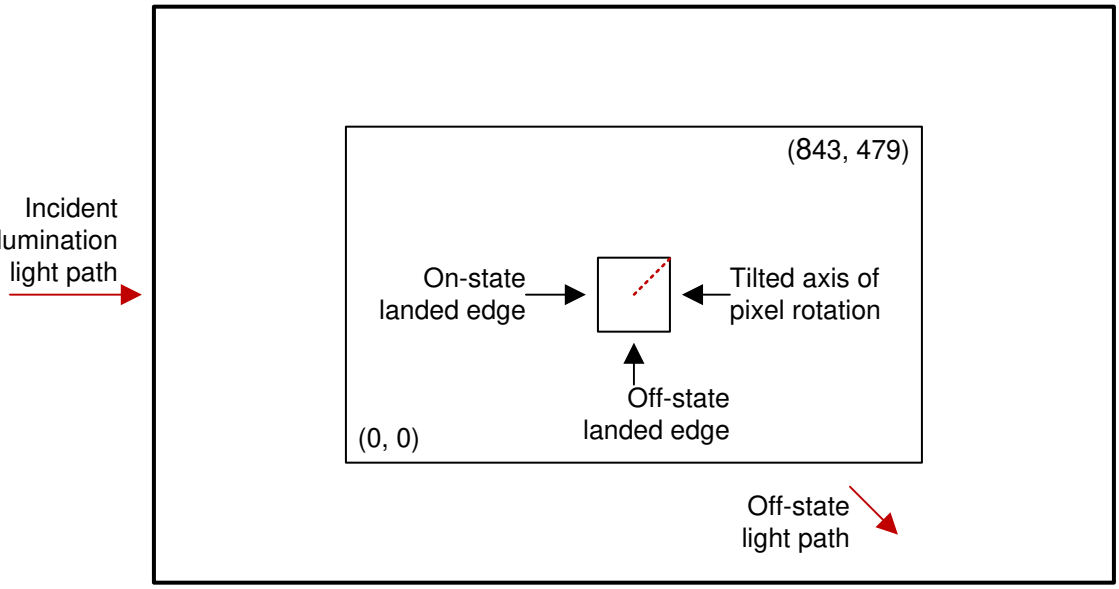


图 6-17. Landed Pixel Orientation and Tilt

6.12 Window Characteristics

PARAMETER(1)		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture(2)				See (2)	
Illumination overfill(3)				See (3)	
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
Window Transmittance, single-pass through both surfaces and glass	Average over the wavelength range 420 to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See 节 7.5 for more information.
(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(3) The active area of the DLP2010 device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.

6.13 Chipset Component Usage Specification

The DLP2010 is a component of one or more TI DLP® chipsets. Reliable function and operation of the DLP2010 requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

备注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

6.14 Software Requirements

CAUTION

The DLP2010 DMD has mandatory software requirements. Refer to *Software Requirements for TI DLP®Pico® TRP Digital Micromirror Devices* application report for additional information. Failure to use the specified software will result in failure at power up.

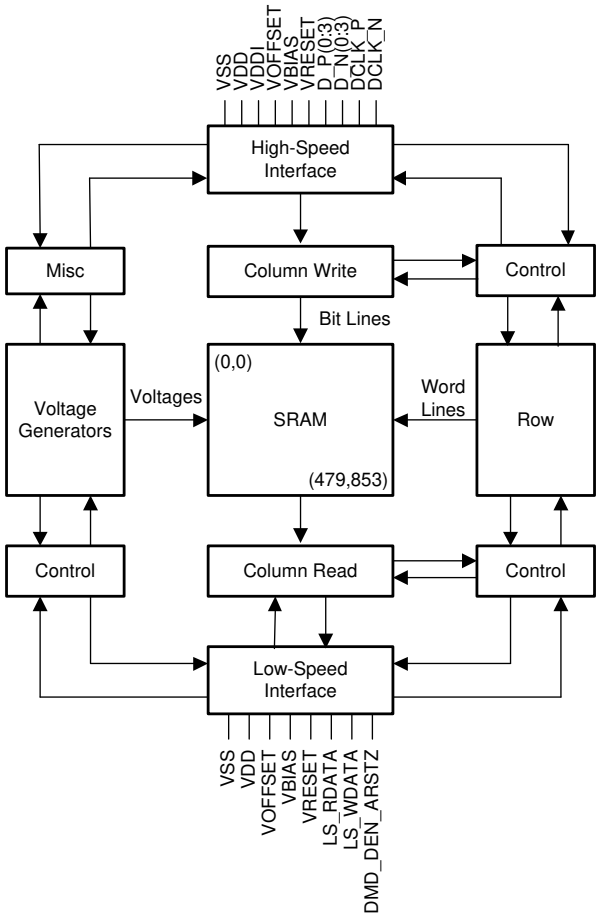
7 Detailed Description

7.1 Overview

The DLP2010 is a 0.2 inch diagonal spatial light modulator of aluminum micromirrors. Pixel array size is 854 columns by 480 rows in a square grid pixel arrangement. The electrical interface is sub low voltage differential signaling (SubLVDS) data.

This DMD is part of the chipset that is composed of the DMD, DLPC3430 or DLPC3435 display controller and the DLPA200x/DLPA3000 PMIC and LED driver. To ensure reliable operation, the DMD must always be used with the DLPC3430 or DLPC3435 display controller and the DLPA200x/DLPA3000 PMIC and LED driver.

7.2 Functional Block Diagram



Details omitted for clarity.

7.3 Feature Description

7.3.1 Power Interface

The power management component DLPA200x/DLPA3000, contains three 3 regulated DC supplies for the DMD reset circuitry: VBIAS, VRESET and VOFFSET, as well as the two regulated DC supplies for the DLPC3430 or DLPC3435 controller.

7.3.2 Low-Speed Interface

The low speed interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low‑speed clock, and LS_WDATA is the low speed data input.

7.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface uses differential SubLVDS receivers for inputs, with a dedicated clock.

7.3.4 Timing

The data sheet provides timing test results at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Test Load Circuit for Output Propagation Measurement shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is intended for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC3430 or DLPC3435 controller. See the DLPC3430 or DLPC3435 controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

备注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area is typically the same. Ensure this angle does not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat‑state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and/or active area may occur.

7.5.1.2 Pupil Match

The optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and/or active area. These artifacts may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.1.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Be sure to design an illumination optical system that limits light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular optical architecture, overfill light may require further reduction below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

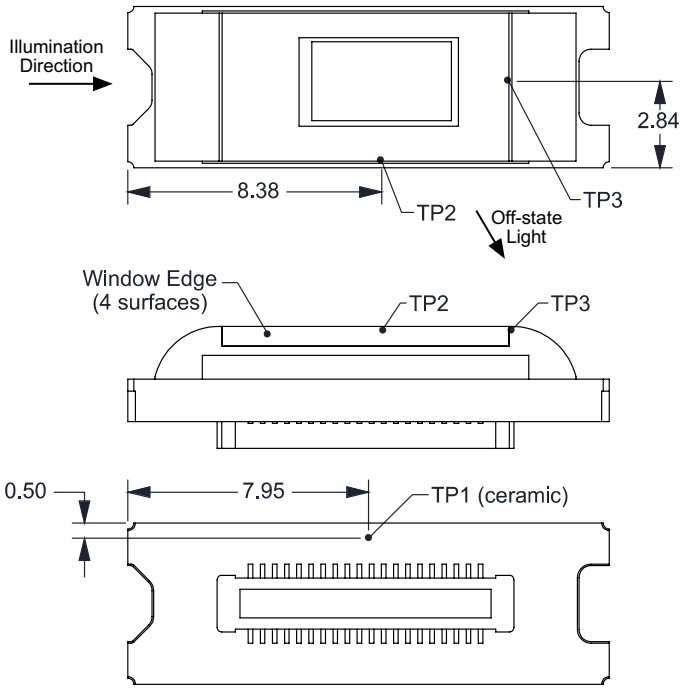


图 7-1. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the ceramic package thermal resistance, the electrical power dissipation, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

$$Q_{ILLUMINATION} = (C_{L2W} \times SL) \quad (3)$$

where

- T_{ARRAY} = Computed DMD array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in DMD Thermal Test Points

- $R_{ARRAY\_TO\_CERAMIC}$ = DMD package thermal resistance from array to outside ceramic (°C/W) specified in *Thermal Information*
- Q_{ARRAY} = Total DMD power; electrical plus absorbed (calculated) (W)
- $Q_{ELECTRICAL}$ = Nominal DMD electrical power dissipation (W)
- C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
- SL = Measured ANSI screen lumens (lm)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.07 W. Absorbed optical power from the illumination source varies and depends on the operating state of the micromirrors and the intensity of the light source. Equation 1 through Equation 1 are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant CL2W is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00266 W/lm.

The following is a sample calculation for typical projection application:

$T_{CERAMIC}$ = 55°C (measured)

SL = 150 lm (measured)

$Q_{ELECTRICAL}$ = 0.070 W

CL2W = 0.00266 W/lm

Q_{ARRAY} = 0.070 W + (0.00266 W/lm × 150 lm) = 0.469 W

T_{ARRAY} = 55°C + (0.469 W × 7.9°C/W) = 58.7°C

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On and Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 75/25 indicates that the referenced pixel is in the ON state 75% of the time (and in the OFF state 25% of the time), whereas 25/75 indicates that the pixel is in the OFF state 75% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

When assessing landed duty cycle, the time spent switching from the current state to the opposite state is considered negligible and is thus ignored.

Because a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) nominally add to 100.In practice, image processing algorithms in the DLP chipset can result a total of less that 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD’s micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD’s usable life.

It is the symmetry or asymmetry of the landed duty cycle that is relevant. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect the usable life of the DMD. This interaction can be used to reduce the impact that an asymmetrical landed duty cycle has on the useable life of the DMD. 图 6-1 describes this relationship. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature that the DMD should be operated at for a give long-term average landed duty cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel depends on the image content being displayed by that pixel.

In the simplest case for example, when the system displays pure-white on a given pixel for a given time period, that pixel operates very close to a 100/0 landed duty cycle during that time period. Likewise, when the system displays pure-black, the pixel operates very close to a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in 表 7-1.

表 7-1. Grayscale Value and Landed Duty Cycle

Grayscale Value	Nominal Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

To account for color rendition (and continuing to ignore image processing for this example) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where *color cycle time* describes the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the nominal landed duty cycle of a given pixel can be calculated as shown in 方程式 4:

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \quad (4)$$

where

- Red_Cycle_% represents the percentage of the frame time that red displays to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green displays to achieve the desired white point
- Blue_Cycle_% represents the percentage of the frame time that blue displays to achieve the desired white point

For example, assume that the ratio of red, green and blue color cycle times are as listed in 表 7-2 (in order to achieve the desired white point) then the resulting nominal landed duty cycle for various combinations of red, green, blue color intensities are as shown in 表 7-3.

表 7-2. Example Landed Duty Cycle for Full-Color Pixels

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage
50%	20%	30%

表 7-3. Color Intensity Combinations

Red Scale Value	Green Scale Value	Blue Scale Value	Nominal Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to consider when estimating the landed duty cycle is any applied image processing. In the DLPC34xx controller family, the two functions which influence the actual landed duty cycle are Gamma and IntelliBright™, and bitplane sequencing rules.

Gamma is a power function of the form $Output\_Level = A \times Input\_Level^{Gamma}$, where A is a scaling factor that is typically set to 1.

In the DLPC34xx controller family, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in 图 7-2.

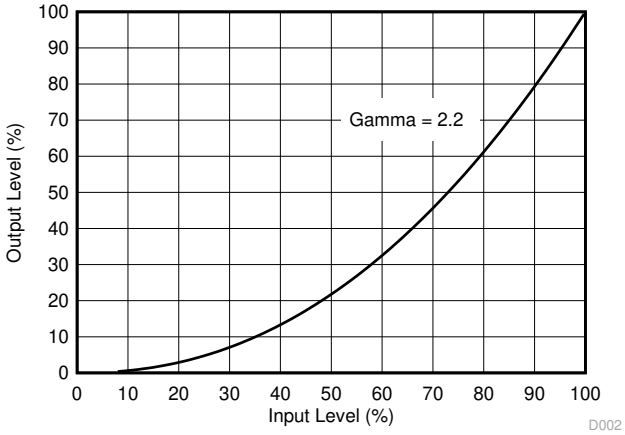


图 7-2. Example of Gamma = 2.2

As shown in 图 7-2, when the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value is 13% after gamma is applied. Because gamma has a direct impact on the displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

The IntelliBright algorithms content adaptive illumination control (CAIC) and local area brightness boost (LABB) also apply transform functions on the gray scale level of each pixel. But while amount of gamma applied to every pixel (of every frame) is constant (the exponent, gamma, is constant), CAIC and LABB are both adaptive functions that can apply a different amounts of either boost or compression to every pixel of every frame. Be sure to account for any image processing which occurs before the controller.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application depends primarily on the optical architecture of the system and the format of the data coming into the DLPC3430 or DLPC3435 controller. The new high-tilt pixel in the side-illuminated DMD increases brightness performance and enables a smaller system electronics footprint for thickness constrained applications. Applications include

- projection embedded in display devices
  - smartphones
  - tablets
  - cameras
  - camcorders
- wearable (near-eye) displays
- battery powered mobile accessory
- interactive display
- low-latency gaming display
- digital signage

DMD power-up and power-down sequencing is strictly controlled by the DLPA200x/DLPA3000. Refer to 节 9 for power-up and power-down specifications. DLP2010 DMD reliability is specified when used with DLPC3430 or DLPC3435 controller and DLPA200x/DLPA3000 PMIC/LED driver only.

8.2 Typical Application

This section describes a pico-projector using a DLP chipset that includes a DLP2010 DMD, DLPC3430 or DLPC3435 controller and DLPA200x/DLPA3000 PMIC/LED driver. The DLPC3430 or DLPC3435 controller does the digital image processing, the DLPA200x/DLPA3000 provides the needed analog functions for the projector, and DMD is the display device for producing the projected image.

The DLPC3430 controller in the pico-projector embedded module typically receives images/video from a host processor within the product. DLPC3430 controller then drives the DMD synchronized with the R, G, B LEDs in the optical engine to display the image/video as output of the optical engine.

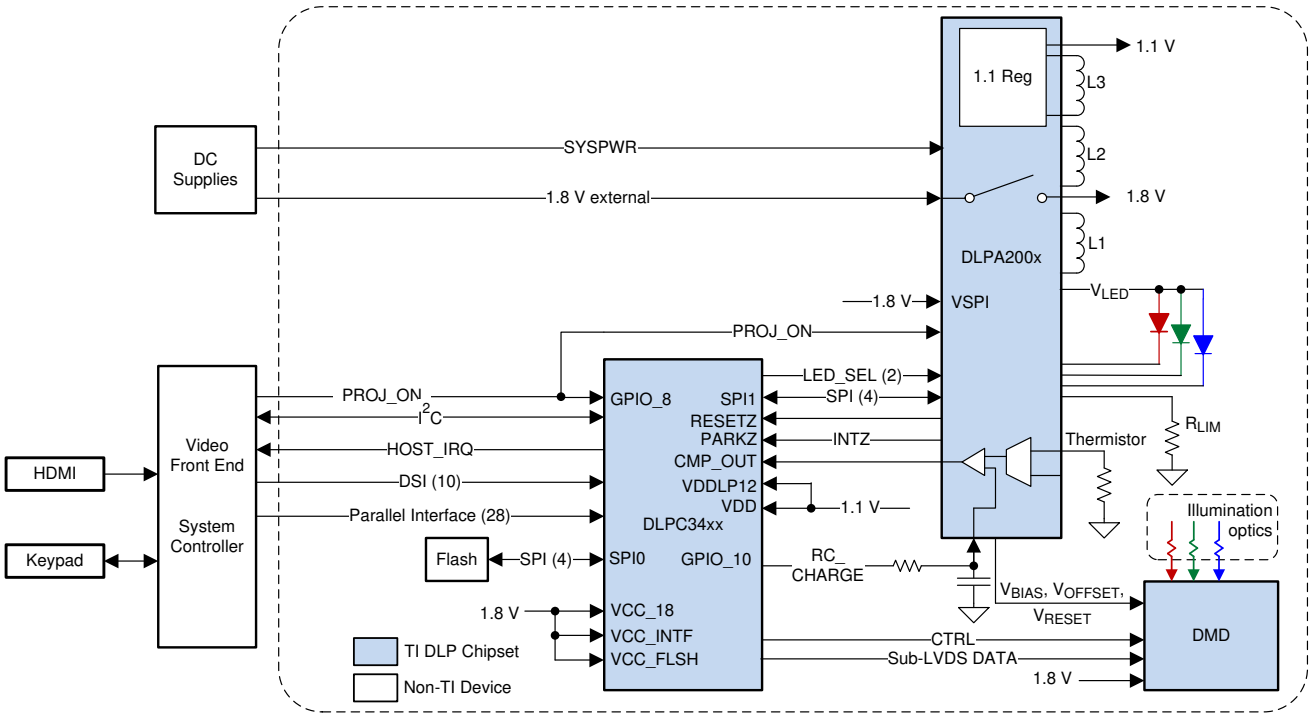


图 8-1. Typical Application

8.2.1 Design Requirements

In addition to the three DLP devices in the chipset, other IC components may be needed. At a minimum, this design requires a flash device to store the software and firmware to control the DLPC3430 or DLPC3435.

Red, green, and blue LEDs typically supply the illumination light that is applied to the DMD. These LEDs are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector.

A parallel interface connects the DLPC3430 or DLPC3435 to the host processing for receiving images. When the parallel interface is used, use an I^2C interface to the host processor for sending commands to the DLPC3430 or DLPC3435.

The battery (SYSPWR) and a regulated 1.8-V supply are the only power supplies needed external to the projector in case of DLPA200x. The DLPA3000 supplies the 1.8V without external regulator.

8.2.2 Detailed Design Procedure

For connecting together the DLPC3430 or DLPC3435, the DLPA200x/DLPA3000, and the DMD, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

A miniature stepper motor can optionally be added to the optical engine for creating a motorized focus. Direct control and driving of the motor can be done by the DLPA200x/DLPA3000, and software commands sent over I^2C to the DLPC3430 or DLPC3435 are available to move the motor to the desired position.

8.2.3 Application Curve

This device drives current time-sequentially though the LEDs. As the LED currents through the red, green, and blue LEDs increases, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents as shown in 图 8-2. For the LED currents shown, assumed that the same current amplitude is applied to the red, green, and blue.

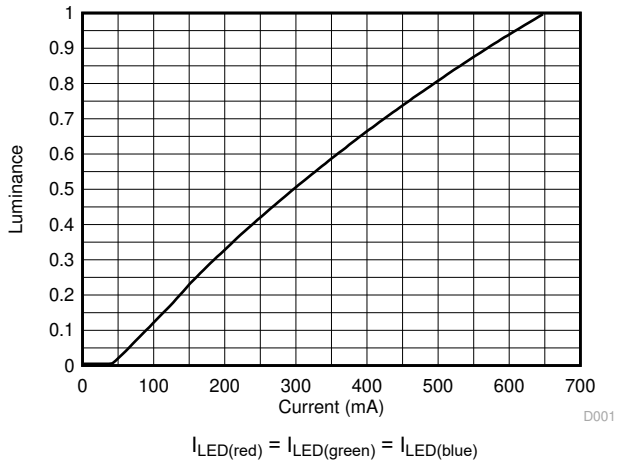


图 8-2. Luminance vs Current

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- VSS
- VBIAS
- VDD
- VDDI
- VOFFSET
- VRESET

The DLPAxxxx device strictly controls the DMD power-up and power-down sequences as described in 图 9-1.

CAUTION

To ensure reliable operation of the DMD, follow the power supply sequencing requirements described in this section. Failure to adhere to any of these requirements can result in a significant reduction in the DMD reliability and lifetime.

VBIAS, VDD, VDDI, VOFFSET, and VRESET power supplies must be coordinated during power-up and power-down operations . Common ground (VSS) to all lines must also be connected.

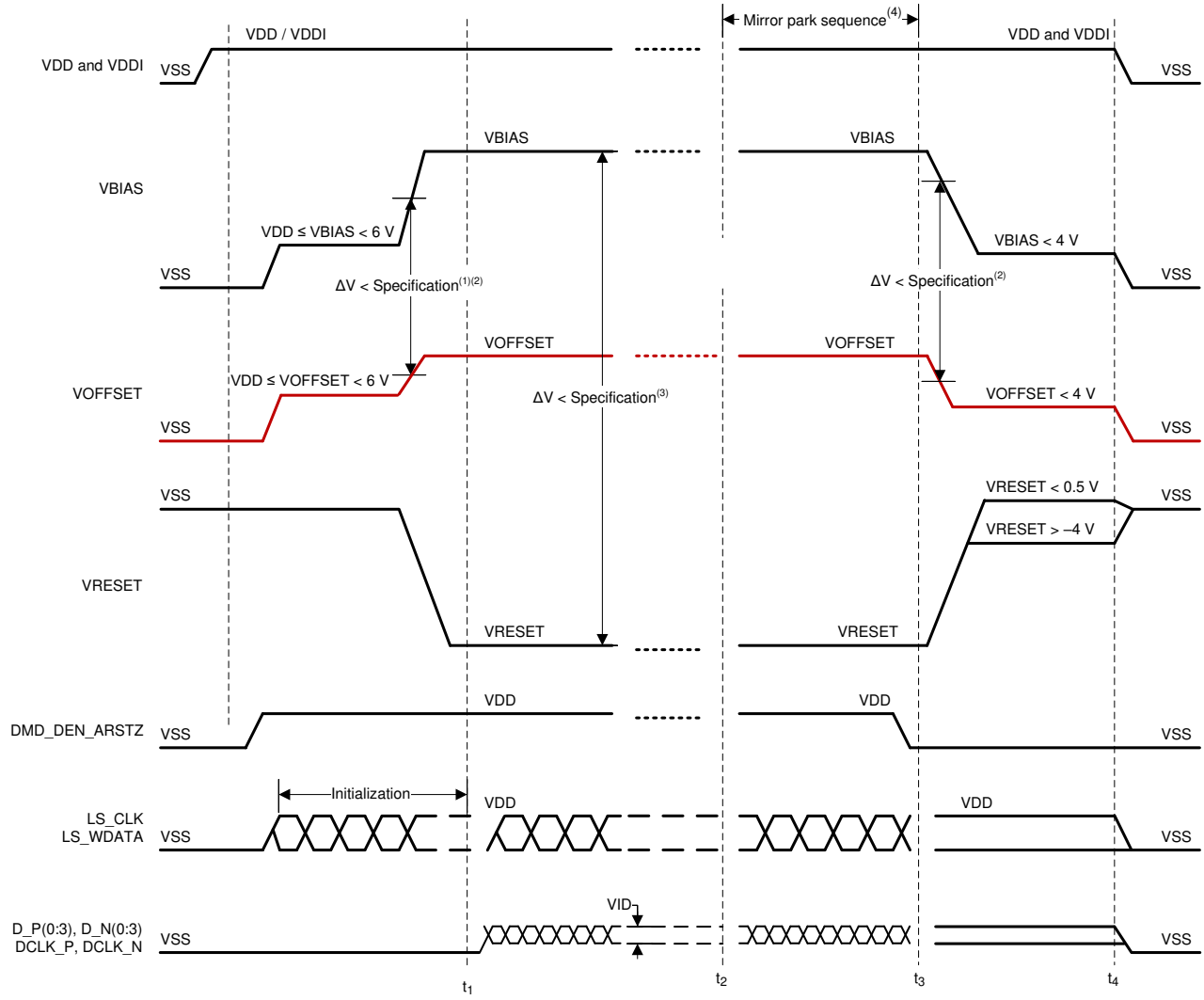
9.1 DMD Power Supply Power-Up Procedure

- During the power-up sequence, VDD and VDDI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During the power-up sequence, it is a strict requirement that the voltage difference between VBIAS and VOFFSET must be within the specified limit shown in 节 *6.4*. Refer to 表 9-1 for the power-up sequence, delay requirements.
- During the power-up sequence, there is no requirement for the relative timing of VRESET with respect to VBIAS and VOFFSET.
- Power supply slew rates during the power-up sequence are flexible, provided that the transient voltage levels follow the requirements specified in 节 *6.1*, in 节 *6.4*, and in 节 9.3.
- During the power-up sequence, LPSDR input pins must not be driven high until after VDD/VDDI have settled at operating voltages listed in 节 *6.4*.

9.2 DMD Power Supply Power-Down Procedure

- The power-down sequence is the reverse order of the previous power-up sequence. During the power-down sequence, VDD and VDDI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within 4 V of ground.
- During the power-down sequence, it is a strict requirement that the voltage difference between VBIAS and VOFFSET must be within the specified limit shown in 节 *6.4*.
- During the power-down sequence, there is no requirement for the relative timing of VRESET with respect to VBIAS and VOFFSET.
- Power supply slew rates during the power-down sequence, are flexible, provided that the transient voltage levels follow the requirements specified in 节 *6.1*, in 节 *6.4*, and in 节 9.3.
- During the power-down sequence, LPSDR input pins must be less than VDD/VDDI specified in 节 *6.4*.

9.3 Power Supply Sequencing Requirements



DLP controller and PMIC controls start of DMD operation

Mirror park sequence starts

Mirror park sequence ends. DLP controller and PMIC disables VBIAS, VOFFSET, and VRESET.

Power off.

Refer to 表 9-1 and 图 9-2 for critical power-up sequence delay requirements.

When system power is interrupted, the ASIC driver initiates hardware the power-down sequence, that disables VBIAS, VRESET and VOFFSET after the micromirror park sequence is complete. Software the power-down sequence, disables VBIAS, VRESET, and VOFFSET after the micromirror park sequence through software control.

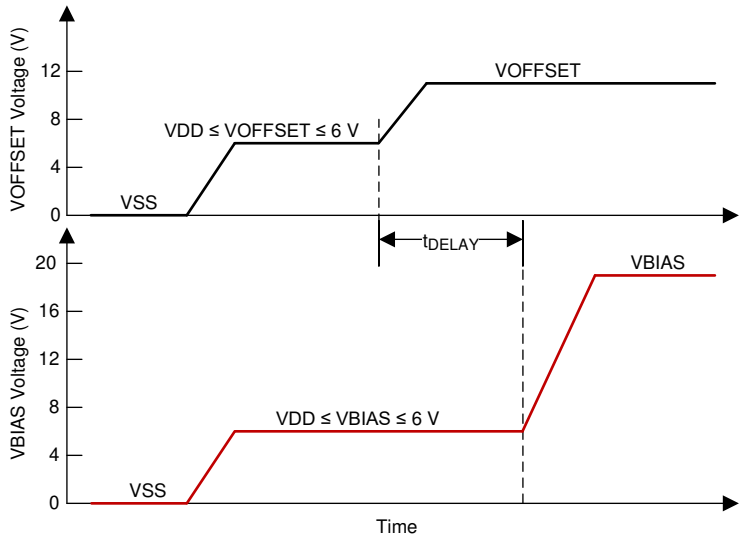
To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit shown in 节 6.4.

Drawing is not to scale and details are omitted for clarity.

图 9-1. Power Supply Sequencing Requirements

表 9-1. Power-Up Sequence Delay Requirement

PARAMETER		MIN	MAX	UNIT
t_{DELAY}	Delay requirement from VOFFSET power up to VBIAS power up	2		ms
VOFFSET	Supply voltage level during power – up sequence delay (see 图 9-2)		6	V
VBIAS	Supply voltage level during power – up sequence delay (see 图 9-2)		6	V



Refer to 表 9-1 for VOFFSET and VBIAS supply voltage levels during power-up sequence delay.

图 9-2. Power-Up Sequence Delay Requirement

10 Layout

10.1 Layout Guidelines

There are no specific layout guidelines because in most cases the DMD is connected using a board-to-board connector to a flex cable. The flex cable provides the interface of data and control signals between the DLPC3430 or DLPC3435 controller and the DLP2010 DMD. For detailed layout guidelines refer to the layout design files.

Layout guidelines for the flex cable interface with DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer 图 10-1.
- Place a decoupling capacitor (minimum 100-nF) close to VBIAS. See capacitor C4 in 图 10-2.
- Place a decoupling capacitor (minimum 100-nF) close to VRST. See capacitor C6 in 图 10-2.
- Place a decoupling capacitor (minimum 220-nF) close to VOFS. See capacitor C7 in 图 10-2.
- Place the optional decoupling capacitor (minimum between 200-nF and 220-nF) to meet the ripple requirements of the DMD. See capacitor C5 in 图 10-2.
- Place a decoupling capacitor (minimum 100-nF) close to VDDI. See capacitor C1 in 图 10-2.
- Place a decoupling capacitor (minimum 100-nF) close to both groups of VDD pins, for a total of 200 nF for VDD. See capacitors C2 and C3 in 图 10-2.

10.2 Layout Example

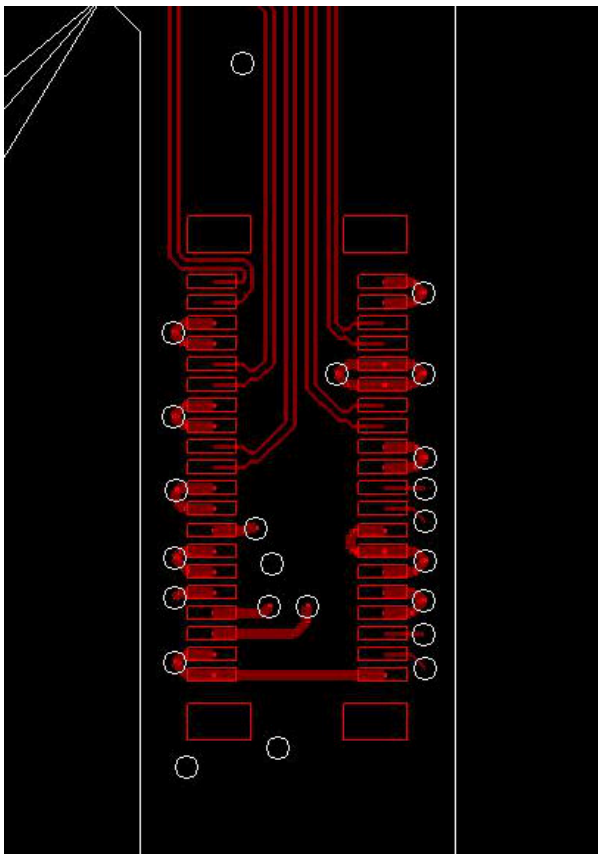


图 10-1. High-Speed (HS) Bus Connections

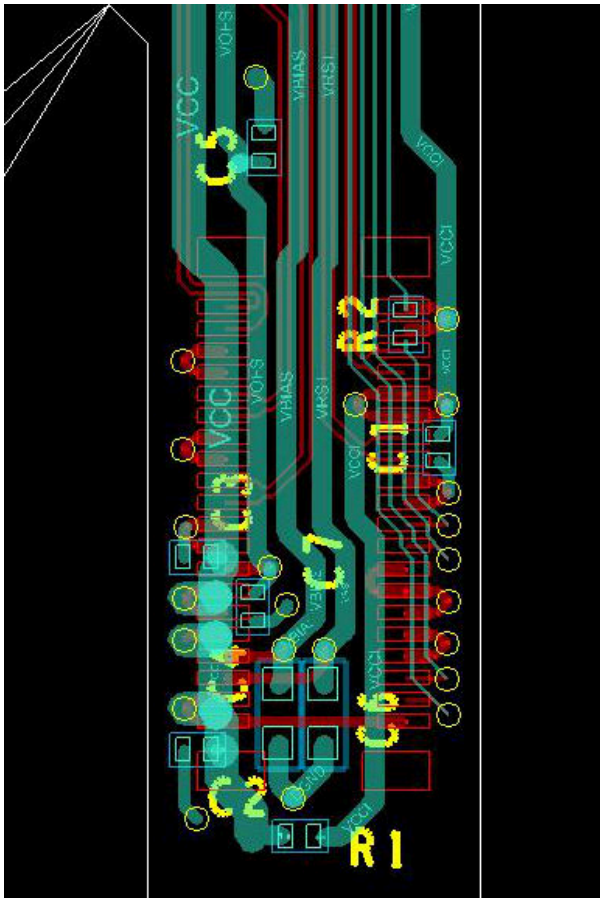


图 10-2. Power Supply Connections

11 Device and Documentation Support

11.1 Device Support

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.1.2 Device Nomenclature

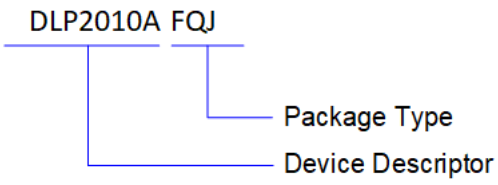


图 11-1. Part Number Description

11.1.3 Device Markings

Device Marking will include the human‐readable character string GHJJJJK VVVV on the electrical connector. GHJJJJK is the lot trace code. VVVV is a 4 character encoded device part number.

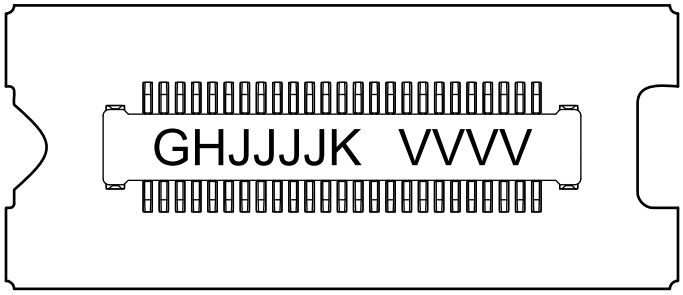


图 11-2. DMD Marking

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLPC3430	Click here	Click here	Click here	Click here	Click here
DLPC3435	Click here	Click here	Click here	Click here	Click here
DLPA2000	Click here	Click here	Click here	Click here	Click here
DLPA2005	Click here	Click here	Click here	Click here	Click here
DLPA3000	Click here	Click here	Click here	Click here	Click here

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.5 Trademarks

IntelliBright™ and TI E2E™ are trademarks of Texas Instruments.
DLP® and Pico® are registered trademarks of Texas Instruments.
所有商标均为其各自所有者的财产。

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP2010AFQJ	ACTIVE	CLGA	FQJ	40	120	RoHS & Green	Call TI	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

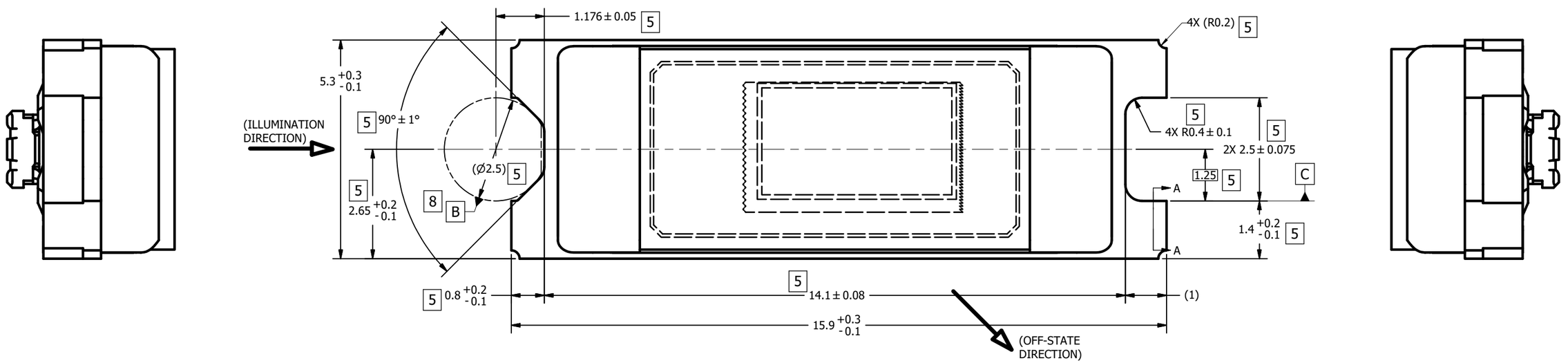
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

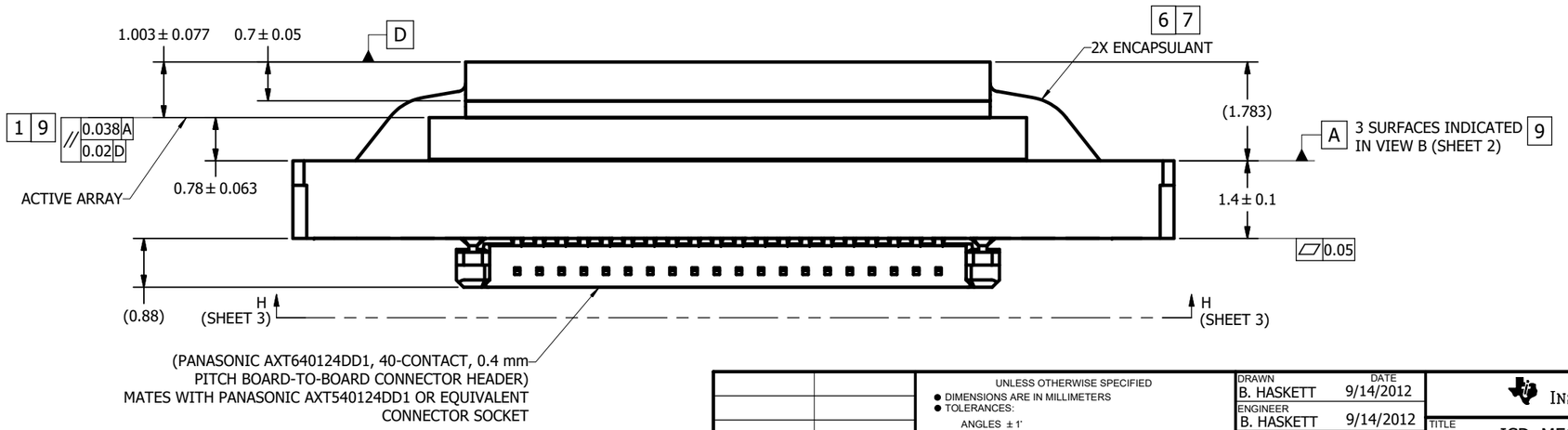
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

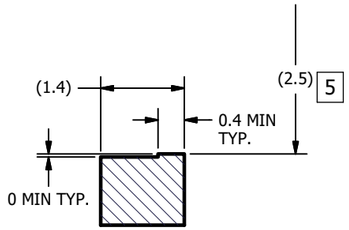
REVISIONS			
REV	DESCRIPTION	DATE	BY
A	ECO 2127544: INITIAL RELEASE	9/14/2012	BMH
B	ECO 2129552: ENLARGE APERTURE ON RIGHT SIDE; MOVE ACTIVE ARRAY Y-LOCATION DIM, SH. 3	12/10/2012	BMH
C	ECO 2131252: ENLARGE APERTURE ALONG BOTTOM EDGE	2/20/2013	BMH
D	ECO 2135244: CORRECT WINDOW THK TOL, ZONE B6	8/5/2013	BMH
E	ECO 2138016: INCREASE WINDOW THK NOMINAL	11/21/2013	BMH
F	ECO 2186532: ADD APERTURE SLOTS PICTORIALLY	3/31/2020	BMH

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. DMD MARKING TO APPEAR IN CONNECTOR RECESS.
5. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
6. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW C (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
7. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
8. DATUM B IS DEFINED BY A DIA. 2.5 PIN, WITH A FLAT ON THE SIDE FACING TOWARD THE CENTER OF THE ACTIVE ARRAY, AS SHOWN IN VIEW B (SHEET 2).
9. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.







SECTION A-A
NOTCH OFFSETS

THIRD ANGLE PROJECTION

NEXT ASSY	USED ON
	0314DA
APPLICATION	

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL UNITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	9/14/2012
ENGINEER	B. HASKETT	9/14/2012
QA/CE	P. KONRAD	9/26/2012
CM	F. ARMSTRONG	9/26/2012
	M. DORAK	9/18/2012
APPROVED	M. SOUCEK	9/18/2012

TEXAS INSTRUMENTS
Dallas Texas

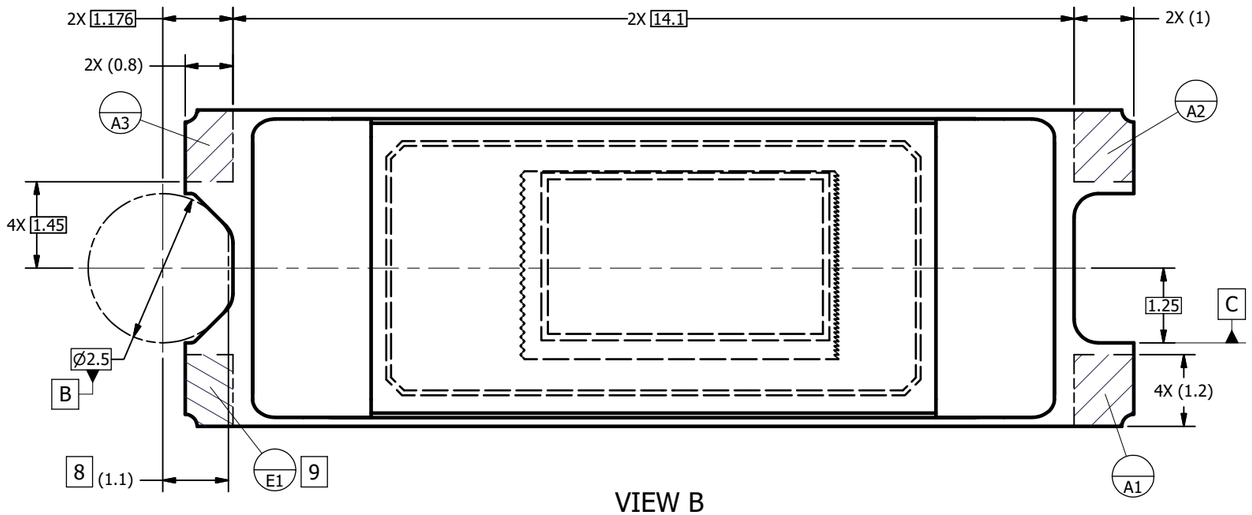
TITLE: ICD, MECHANICAL, DMD, .2 WVGA SERIES 244 (FQJ PACKAGE)

SIZE	DWG NO	REV
D	2512515	F

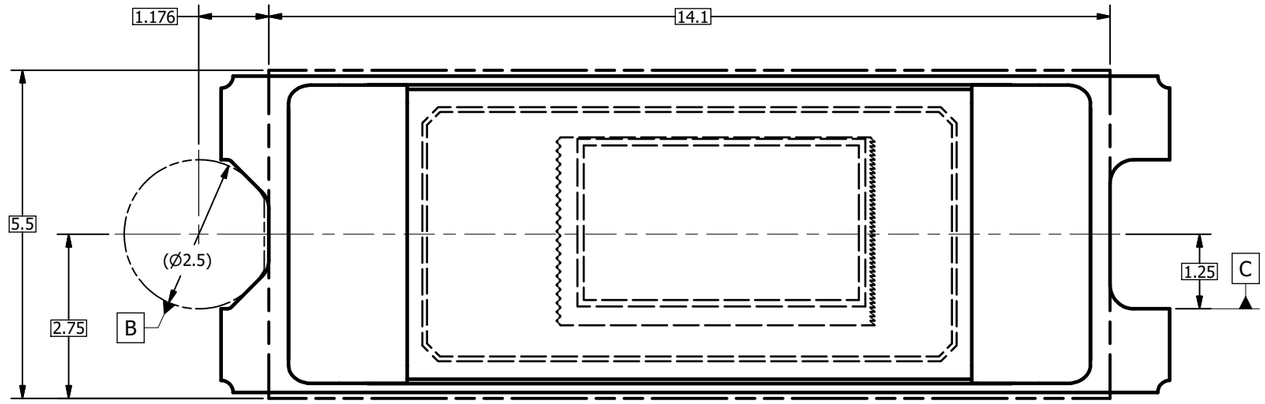
SCALE 20:1 SHEET 1 OF 3

DWG NO. 2512515 SH 1

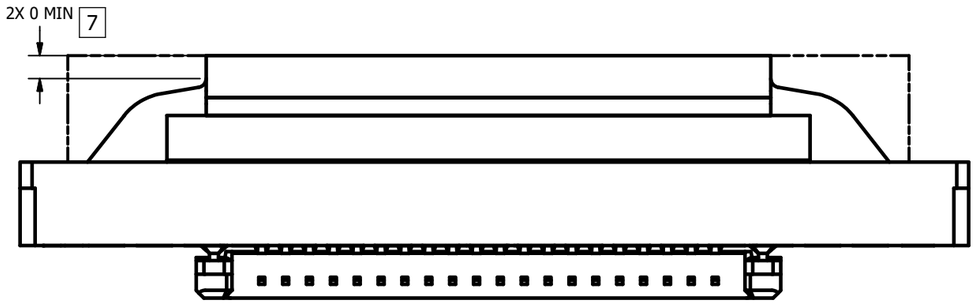
INV11-2006a



VIEW B
DATUMS A, B, C, AND E
(FROM SHEET 1)



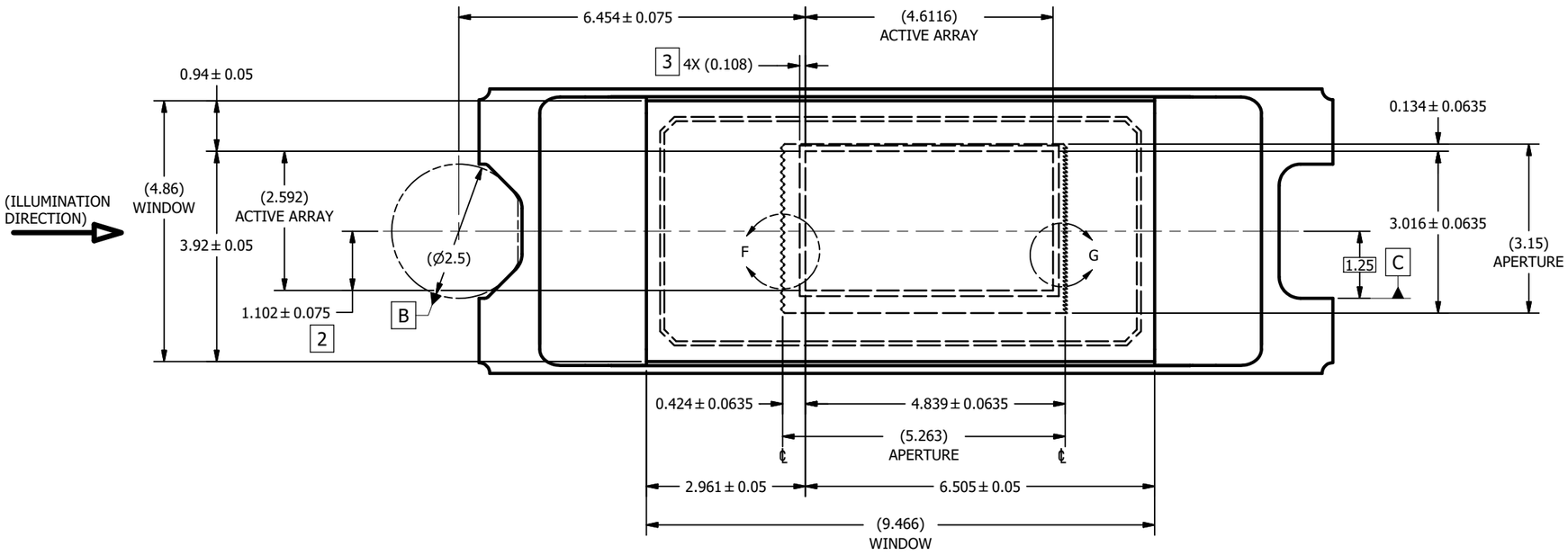
VIEW C 6
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
(FROM SHEET 1)



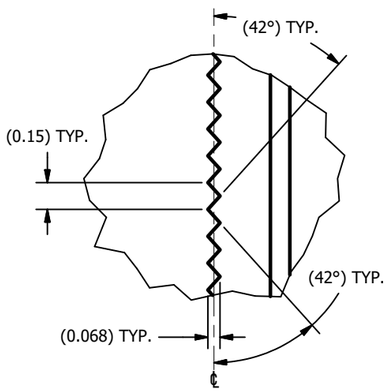
VIEW D
ENCAPSULANT MAXIMUM HEIGHT

Texas Instruments, Dallas Texas	DRAWN B. HASKETT	DATE 9/14/2012	SIZE D	DWG NO 2512515	REV F
			SCALE	SHEET 2 OF 3	

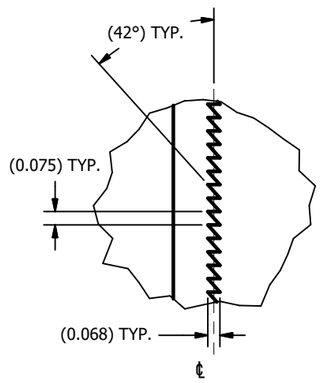
INV11-2006a



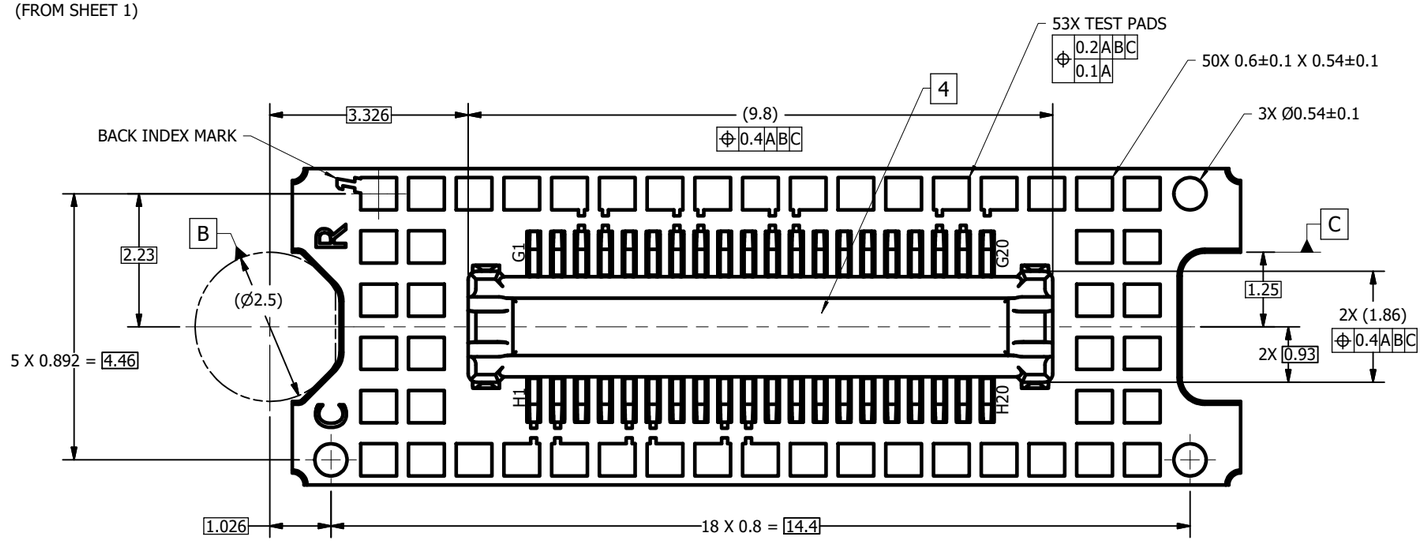
VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL F
APERTURE LEFT EDGE
SCALE 60 : 1



DETAIL G
APERTURE RIGHT EDGE
(POND OF MIRRORS OMITTED FOR CLARITY)
SCALE 60 : 1



VIEW H-H
TEST PADS AND CONNECTOR
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 9/14/2012	SIZE D		DWG NO 2512515	REV F
			SCALE		SHEET 3 OF 3	

INV11-2006a

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Display Drivers & Controllers ***category:***

Click to view products by Texas Instruments ***manufacturer:***

Other Similar products are found below :

TW8819AT-NA2-GR LX27901IDW DLPC3421ZVB BD83854MUV-E2 SN55LVDS32W HV857LK7-G DLPA1000YFFT DLPC3435CZEZ DLPC3430CZVBR SC401U PAD1000YFFR S1D13746F01A600 FIN324CMLX HV850MG-G BL8023C DLPC6421ZPC HV852K7-G HV859K7-G HV857K7-G DIO2133CT14 DLP4500NIRAFQD S1D13515F00A100 S1D13517F00A100 S1D13705F00A200 S1D13L01F00A100 S1D13700F02A100 S1D13706F00A200 IRS2982STRPBF S1D13743F00A200 S1D13742F01A200 TW8804-LC3-GRSH TW8816-LA3-GRS TW8816-LB3-CR TW8816-LB3-GRS TW8823-LC2-CE S1D13513B01B100 MAX4820EUP+T S1D13748B00B100 S1D13A05B00B200 HV518PJ-G-M903 HV5812P-G TW8817-TA3-GRS HV518P-G HV5812PJ-G HV518PJ-G HV7022PJ-C-G HV7224PG-G HV633PG-G HV860K7-G HV892K7-G