

DRV3901-Q1 Single Channel Squib Driver For Automotive EV Pyro-Fuse

1 Features

- AEC-Q100 qualified for automotive applications
 - Temperature grade 1: –40°C to +125°C, T_A
- **Functional Safety-Compliant**
 - Developed for functional safety applications
 - Documentation to aid ISO26262 system design up to ASIL C
- Highly integrated squib driver solution targeted at automotive EV pyro-fuse application
 - Integration of power supplies, current regulation, diagnostics, and safety functions
 - SPI or HW pin-based triggering for flexible interface options and rapid firing reaction
 - Diagnostic functions for system energy reservoir capacitor and squib health monitoring
 - Built-in-self-test and diagnostic functions for power supplies, interfaces, drivers, and monitors
 - Architecture for reliable operation with redundant power supplies, low-side and high-driver drivers, and secondary monitoring logic
- Up to 28-V (40-V abs. max) operating voltage
- Compact HVSSOP-28 (DGQ) leaded package
- Two-wire load interface with protected, current controlled high-side and protected secondary low-side switches
- Integrated charge pump for minimal MOSFET drop out voltage
- 4-wire, addressable, 24-bit SPI with CRC protection
 - Allows multiple device to operate on the same SPI
 - Allows for broadcast commands to multiple devices.
- Configurable deployment currents (1.2 A / 2 ms, 1.75 A / 0.5 ms, up to 3.4 A / 0.5 ms)
- Configurable deployment interface options
 - 2-pin HW trigger with PWM or level signaling
 - Protected SPI command with CRC
- Comprehensive off-state diagnostics
 - Device built-in-self-test
 - Driver output and switch test
 - Interface test
 - Energy reservoir capacitor test
 - Squib resistance test
- Configurable fault indicator (nFAULT)

2 Applications

- Squib driver
- Automotive EV pyro-fuse
- [Battery disconnect unit](#)
- [Battery junction box](#)

Package Information

PART NUMBER ⁽¹⁾	PACKAGE	PACKAGE SIZE (NOM) ⁽²⁾
DRV3901-Q1	HVSSOP (28)	7.3 mm X 4.9 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length x width) is a nominal value and includes pins, where applicable.

Device Information

KEY FEATURES
Protected High-Side and Low-Side Architecture
Configurable Deploy Current Options
Direct Hardware Pin Trigger Interface
Energy Reservoir Capacitor Diagnostic
Comprehensive Off-State Diagnostics
Addressable 24-Bit SPI



3 Description

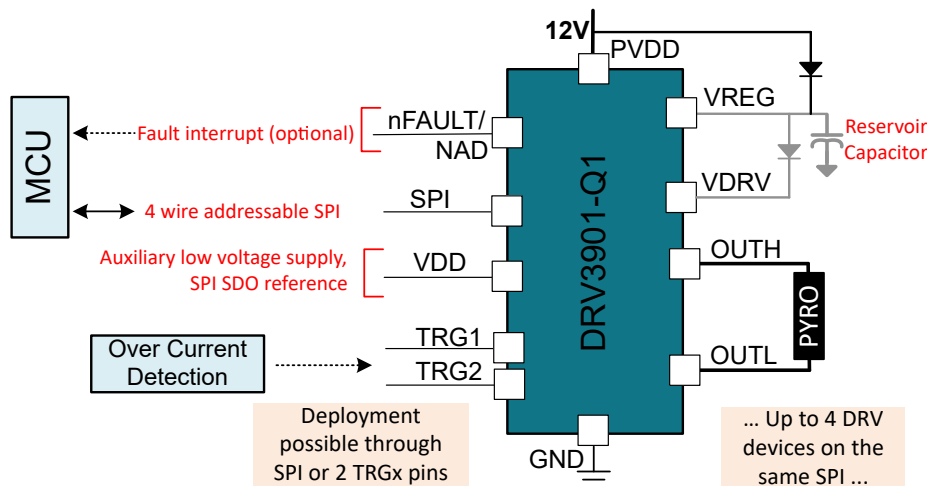
The DRV3901-Q1 is a highly integrated squib driver intended for automotive EV pyro-fuse applications. It includes the power supplies, current sensing and regulation, and diagnostics and protection functions needed to drive a squib load. It incorporates several key functions unique to the device that are different from traditional squib drivers. These functions include a hardware pin trigger interface, an energy reservoir capacitor diagnostic, an addressable SPI, and optimized driver stage with integrated charge pump and additional deployment current options.

The hardware pin trigger (TRGx) interface allows for a deployment command to be issued directly in hardware to the DRV3901-Q1. This allows the flexibility to either trigger the deployment with MCU hardware pins, directly with an overcurrent sensor, or through other external hardware circuit monitors. The hardware trigger pins support a 2-pin interface with both threshold or PWM based options to ensure robustness against miss deployment while still providing flexibility to support a variety of interface options. Additionally, CRC protected deployment commands can be sent through the SPI bus as a secondary method.

To support a diagnostic for the system energy reservoir capacitor, the DRV3901-Q1 integrates a switch and monitor circuit to be able to bias and monitor the discharge voltage of the reservoir capacitor. This enables the device and the external MCU to detect a loss/failure of the reservoir capacitor or its approximate value in normal operation.

An addressable SPI, allow multiple devices to be controlled on a shared SPI bus. In addition to reducing required MCU resources, the addressable SPI incorporates a broadcast command structure that allows multiple drivers to be coordinated to trigger simultaneously or with staggered delays. The SPI incorporate multiple robustness functions including a CRC, address readback capability, and various bus fault detection mechanisms.

The power stage utilizes a protected high-side and low-side switch to ensure robustness against unintended driving due to a variety of fault conditions. An integrated charge pump ensures minimal drop out voltage across the switches during deployment to enable operation down to low supply voltages. A wide variety of deployment options are available to optimize for different types of squib loads or for specific application requirements.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2023	*	Initial Release

5 Mechanical Packaging and Orderable Information

5.1 Package Option Addendum

Packaging Information

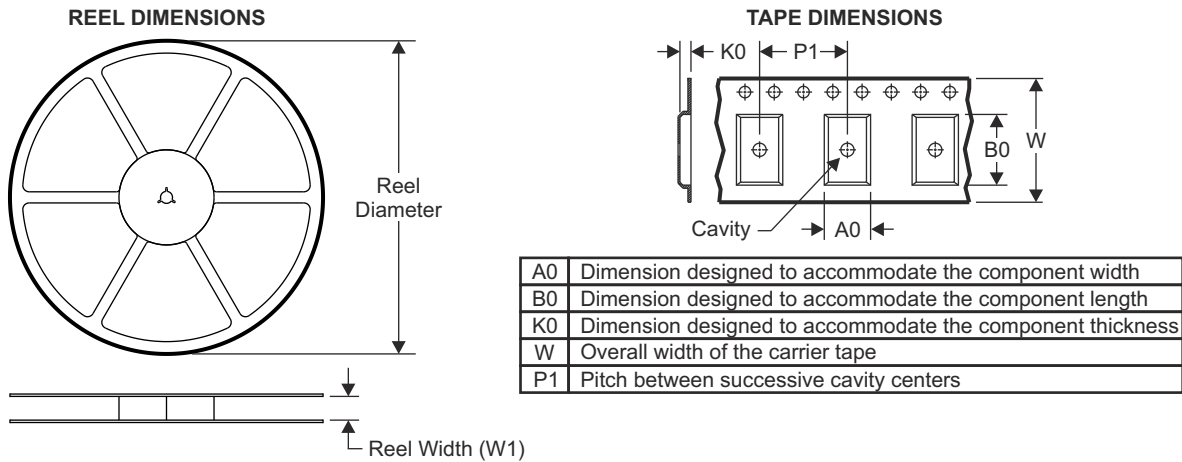
Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁶⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^{(4) (5)}
DRV3901QDG QRQ1	ACTIVE	HVSSOP	DGQ	28	2500	RoHS & Green	NIPDAU	Level-3-260C-1 68 HR	-40 to 125	3901

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

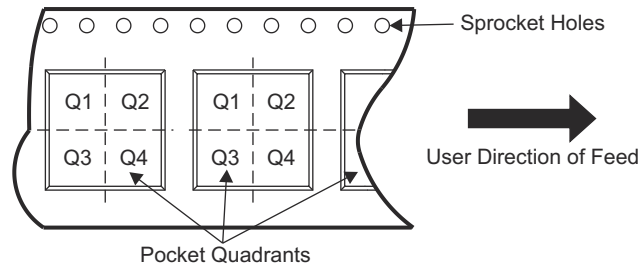
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5.2 Tape and Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




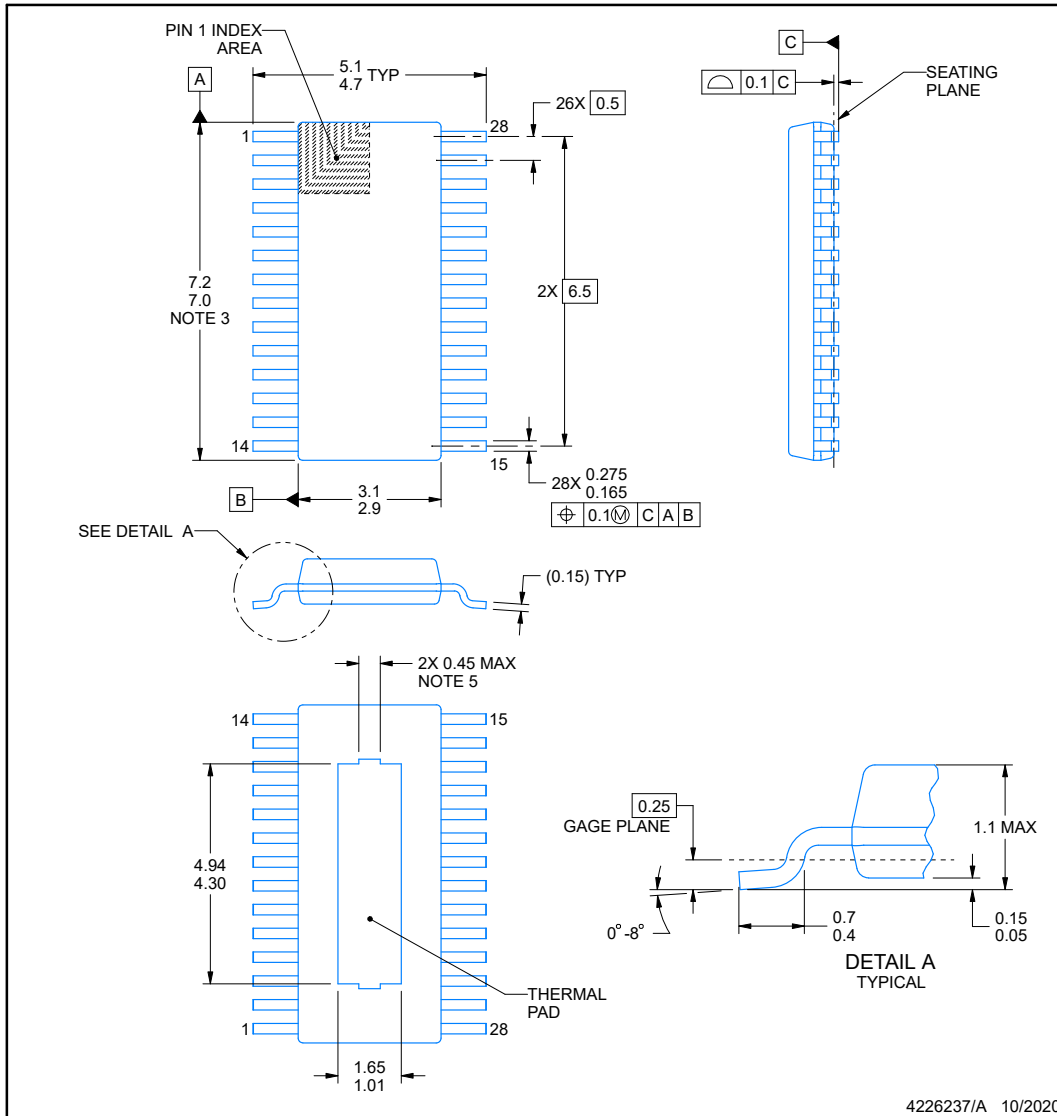
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV3901QDGQRQ1	HVSSOP	DGQ	28	2500	330.00	16.40	5.50	7.40	1.45	8.00	16.00	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV3901QDGQRQ1	HVSSOP	DGQ	28	2500	356	356	35

DGQ0028A  **PowerPAD™ VSSOP - 1.1 mm max height**
SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

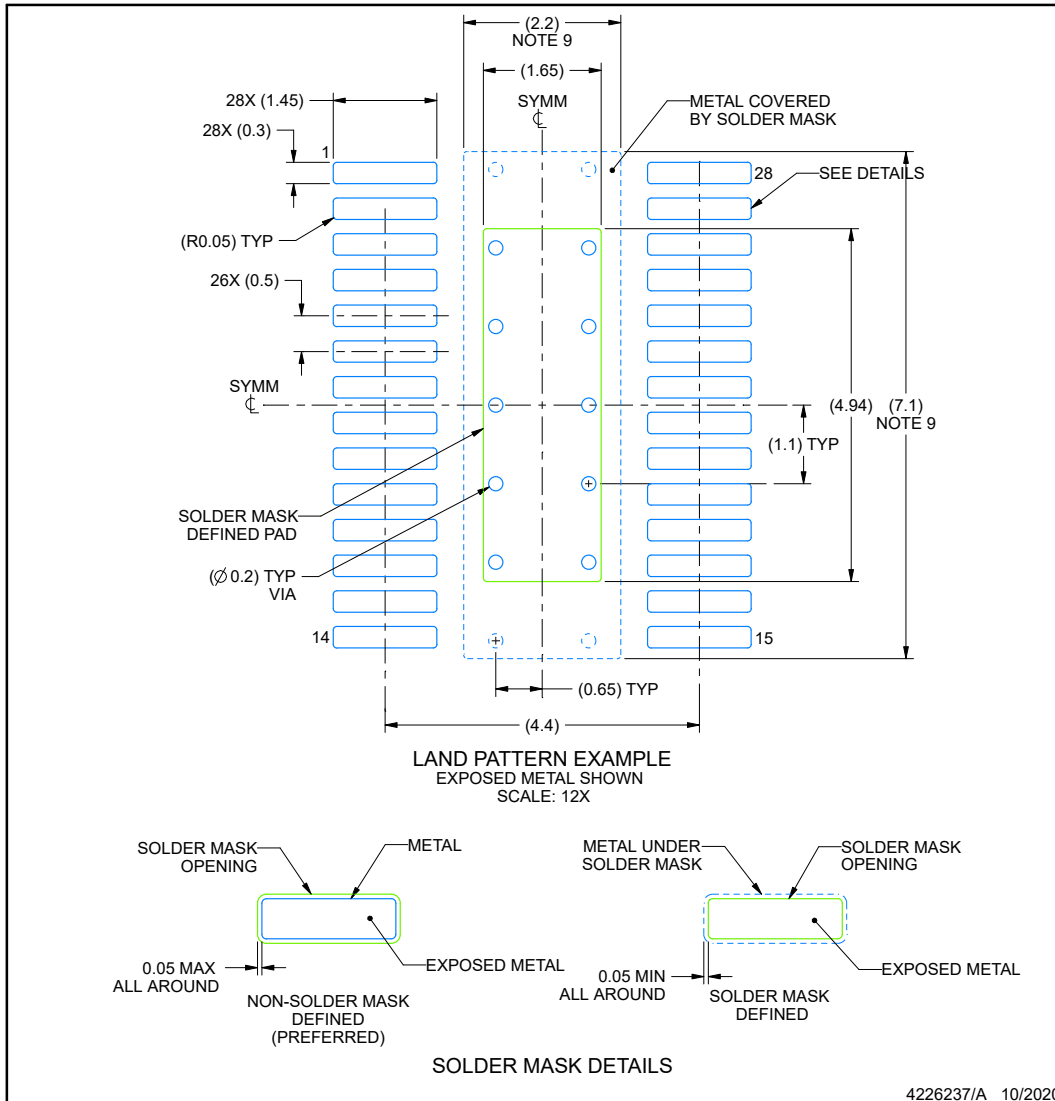
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGQ0028A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

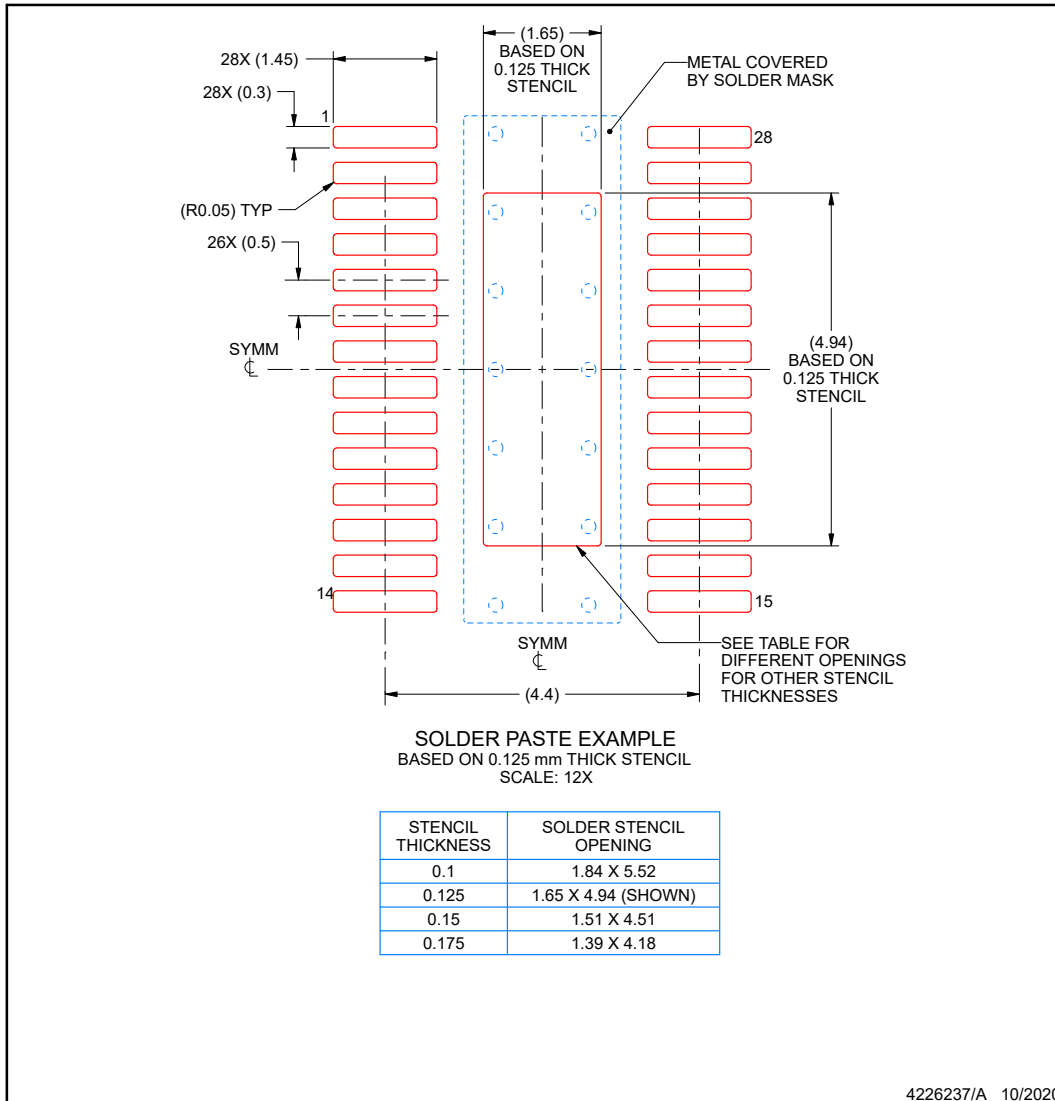
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGQ0028A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV3901QDGRQ1	ACTIVE	HVSSOP	DGQ	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	3901	Samples

(1) The marketing status values are defined as follows:

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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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GENERIC PACKAGE VIEW

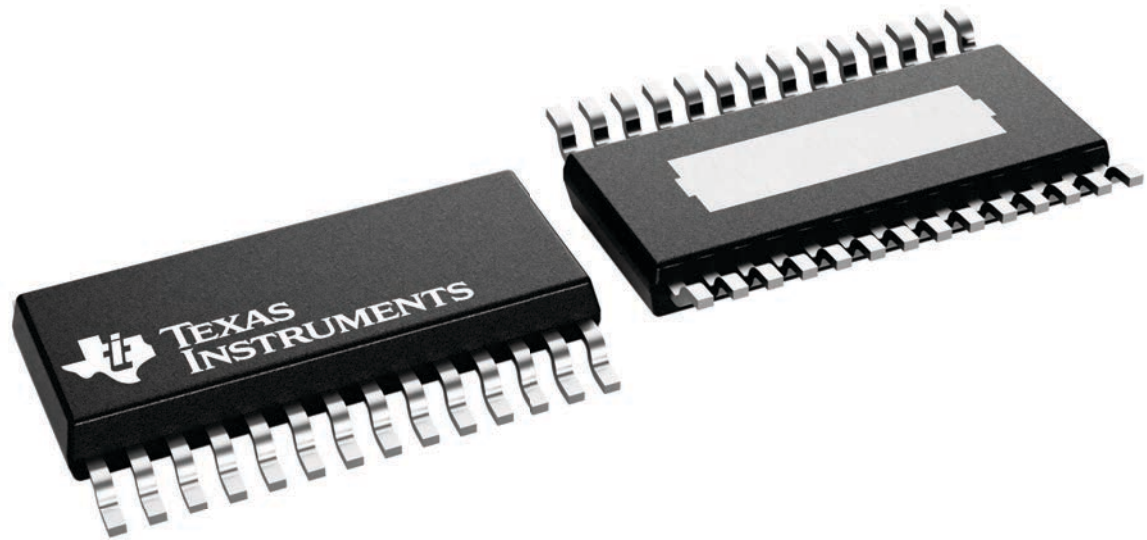
DGQ 28

HVSSOP - 1.1 mm max height

3 x 7.1, 0.5 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226530/A

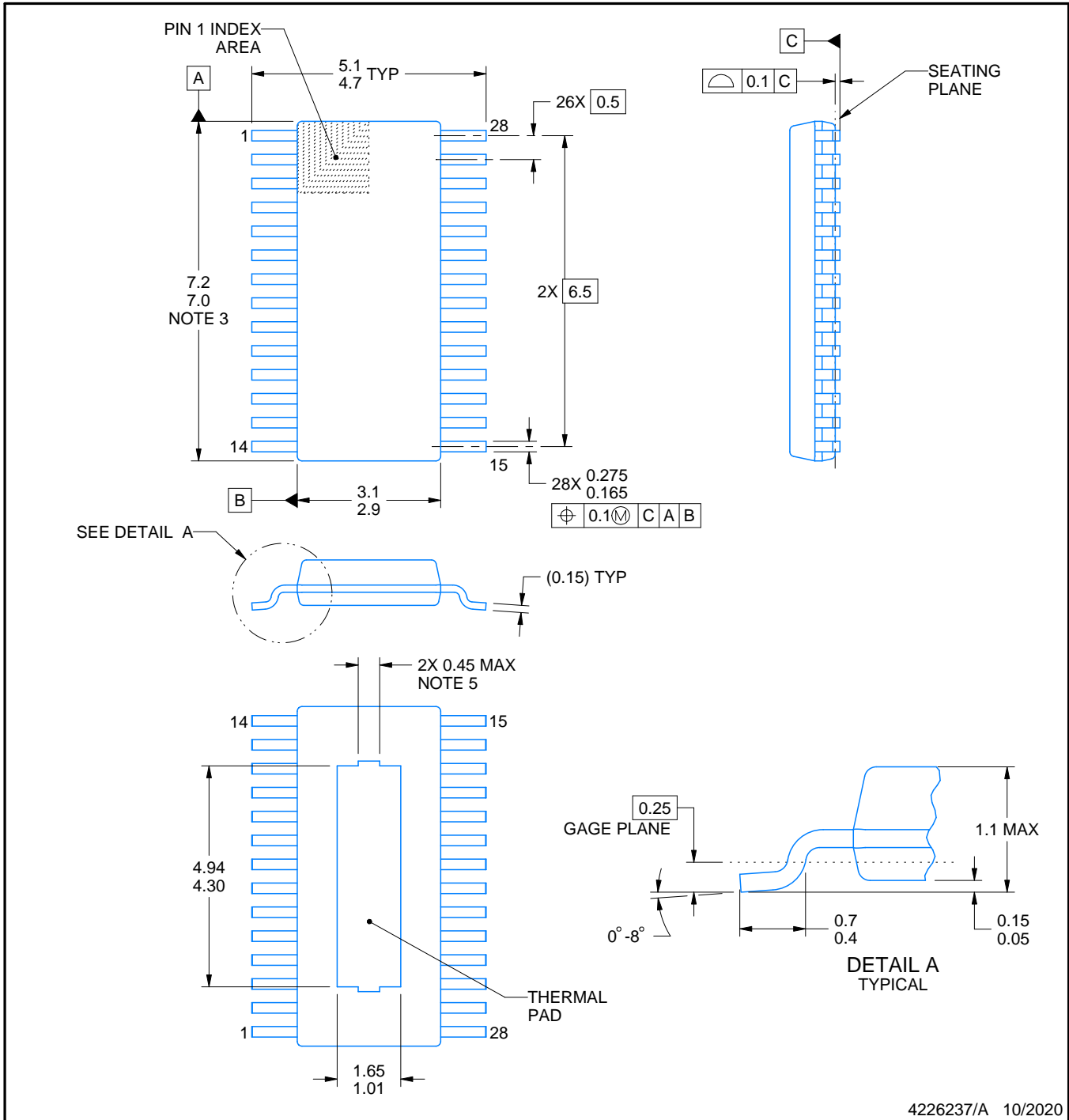
DGQ0028A



PACKAGE OUTLINE

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226237/A 10/2020

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PowerPAD is a trademark of Texas Instruments.

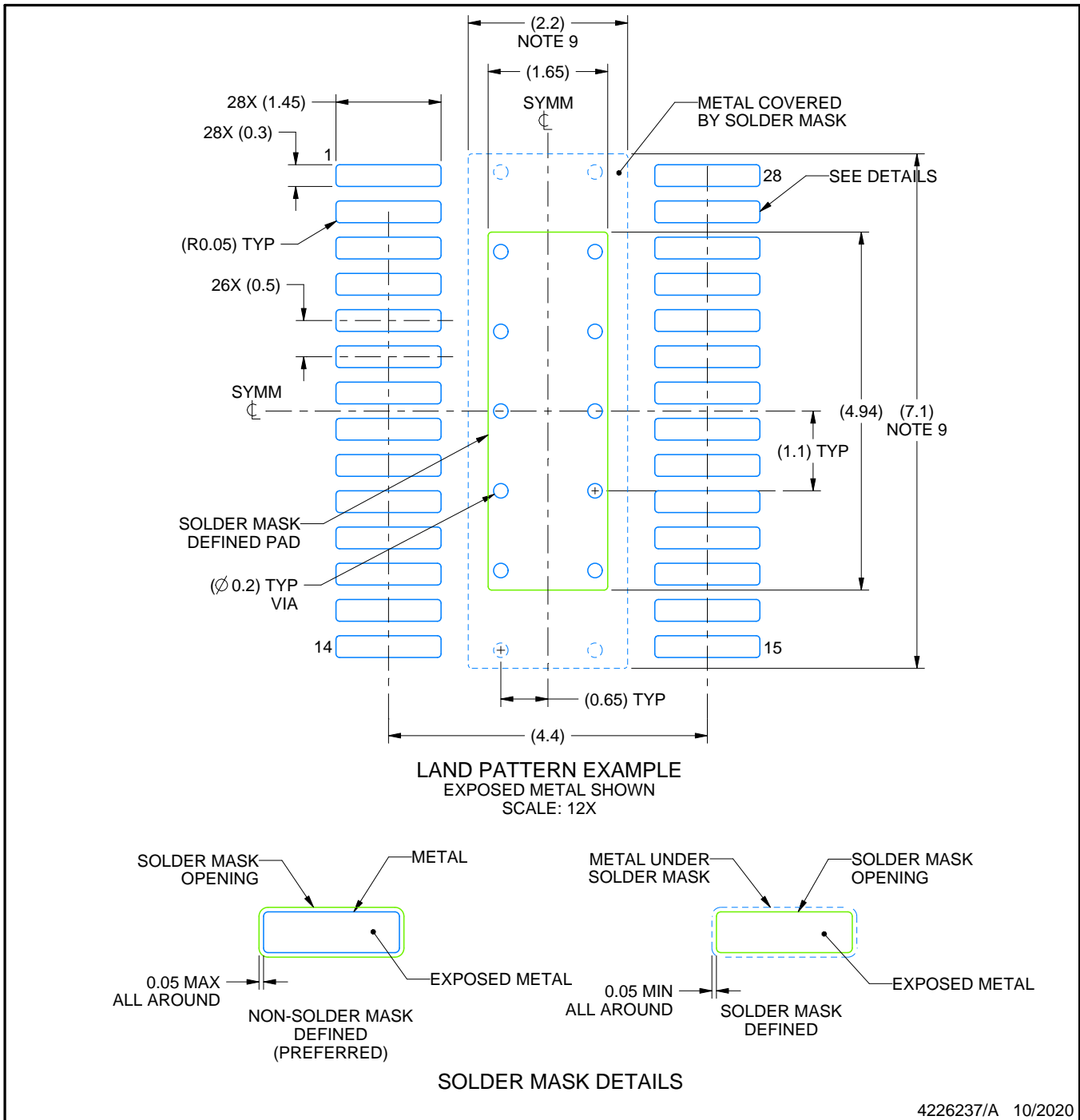
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGQ0028A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

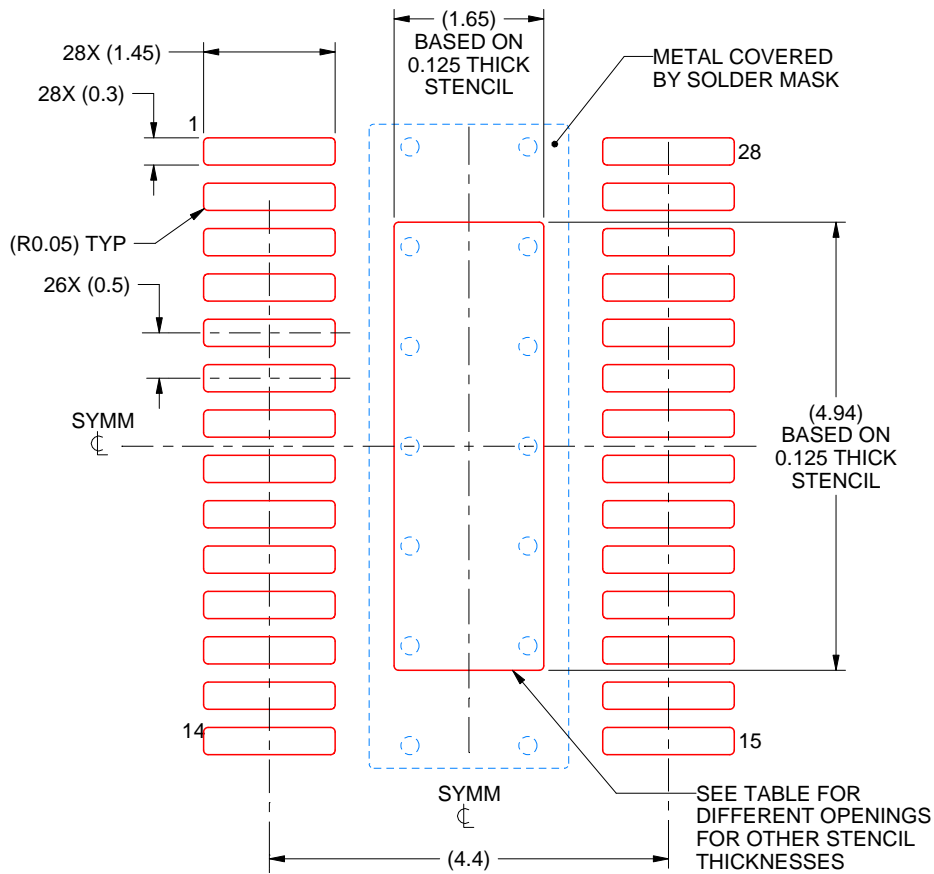
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGQ0028A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.84 X 5.52
0.125	1.65 X 4.94 (SHOWN)
0.15	1.51 X 4.51
0.175	1.39 X 4.18

4226237/A 10/2020

NOTES: (continued)

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12. Board assembly site may have different recommendations for stencil design.

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