

# DRV8849: 38 V, 1.5 A Dual Stepper Driver with Integrated Current Sense, 1/256 Microstepping, STEP/DIR Interface and Smart Tune

## 1 Features

- Dual stepper motor driver
  - STEP/DIR interface
  - Up to 1/256 microstepping indexer
- 4.5 to 38-V Operating supply voltage range
- 900 mΩ HS + LS  $R_{DS(ON)}$  at 24 V, 25°C
- 1.5 A full-scale, 1.1 A rms current per H-bridge
- Integrated current sense functionality
  - ±5% full-scale current accuracy
  - No sense resistors required
- Smart tune decay technology
- Configurable off-time PWM chopping in Smart tune
  - 8-μs, 16-μs, or 32-μs
- Supports 3.3-V, 5.0-V logic inputs
- Low-current sleep mode (1.3 μA)
- Protection features for each Stepper
  - VM undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)
  - Fault condition output (nFAULT)

## 2 Applications

- [IP Network Camera](#)
- [Printers and scanners](#)
- [ATM and money handling machines](#)
- Sewing machines
- [Medical Imaging, Diagnostics and Equipment](#)
- [3D Printer](#)

## 3 Description

The DRV8849 is a dual stepper motor driver for industrial and consumer applications. The device is fully integrated with four N-channel power MOSFET H-bridge drivers, one microstepping indexer for each stepper, and integrated current sensing. The DRV8849 is capable of driving up to 1.5-A full-scale output current (dependent on PCB design).

The DRV8849 uses an internal current sense architecture to eliminate the need for four external power sense resistors, saving PCB area and system cost. The device uses an internal PWM current regulation scheme with smart tune decay mode. Smart tune automatically adjusts for desired current regulation, compensates for motor variation and aging effects and reduces audible noise and vibration from the motor.

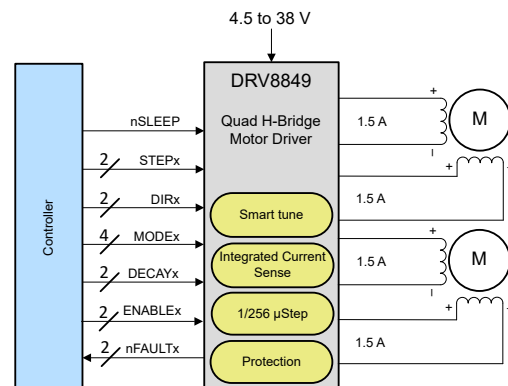
Simple STEP/DIR interfaces allow an external controller to manage the direction and step rate of the stepper motors. The device can be configured in full-step to 1/256 microstepping. A low-power sleep mode is provided using a dedicated nSLEEP pin. Protection features are provided for supply undervoltage, charge pump faults, overcurrent, short circuits, and overtemperature. Fault conditions are indicated by one nFAULT pin for each stepper.

### Device Information

PART NUMBER	PACKAGE <sup>1</sup>	BODY SIZE (NOM) ( <sup>2</sup> )
DRV8849RHHHR	QFN (36)	6 mm x 6 mm

(1) See the orderable addendum at the end of the data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Simplified Schematic**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (May 2023) to Revision A (October 2023)</b>	<b>Page</b>
• Typo corrections throughout data sheet.....	1

## 5 Device Comparison

**Table 5-1. Device Comparison Table**

Device Name	Drives DC motor	Drives Stepper	Interface	Microstep	Current sensing
DRV8849	No	Yes	STEP/DIR	Up to 1/256	Internal sensing
DRV8845	Yes	Yes	PHASE/!xx	Up to 1/4, higher microstepping by VREF pin	Sense Resistor

## 6 Pin Configuration and Functions

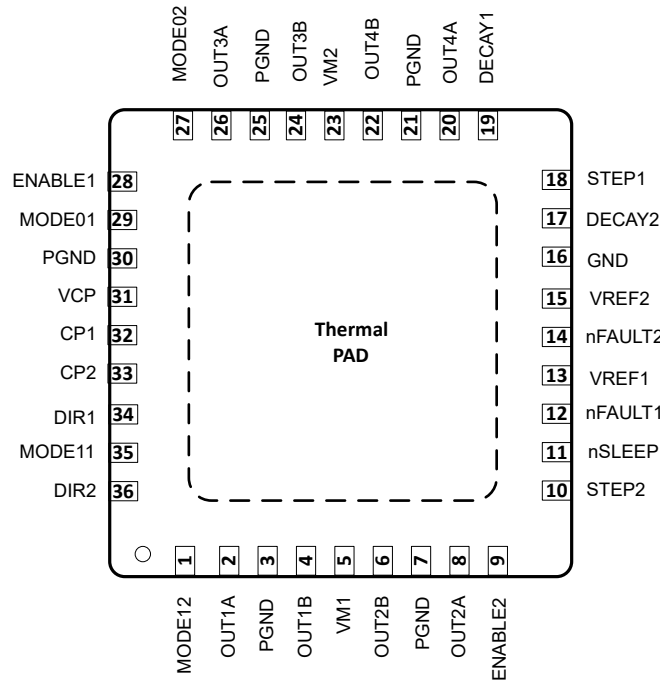


Figure 6-1. RHH Package, 36-Pin QFN, Top View

Table 6-1. Pin Functions

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
OUT1A	2	O	H-Bridge 1 Output A
OUT1B	4	O	H-Bridge 1 Output B
OUT2A	8	O	H-Bridge 2 Output A
OUT2B	6	O	H-Bridge 2 Output B
OUT3A	26	O	H-Bridge 3 Output A
OUT3B	24	O	H-Bridge 3 Output B
OUT4A	20	O	H-Bridge 4 Output A
OUT4B	22	O	H-Bridge 4 Output B
PGND1	3	G	Power ground pin for H-Bridge 1. Connect all ground pins together near the IC.
PGND2	7	G	Power ground pin for H-Bridge 2. Connect all ground pins together near the IC.
PGND3	25	G	Power ground pin for H-Bridge 3. Connect all ground pins together near the IC.
PGND4	21	G	Power ground pin for H-Bridge 4. Connect all ground pins together near the IC.
GND	16, 30	G	Analog ground. Connect all ground pins together near the IC.
VM1	5	P	Supply Voltage. VM1 should be connected to VM2 pin close to the device.
VM2	23	P	Supply Voltage. VM2 should be connected to VM1 pin close to the device.
VCP	31	P	Reservoir Capacitor Terminal
CP1	32	P	Charge Pump Capacitor Terminal
CP2	33	P	Charge Pump Capacitor Terminal
DECAY1	19	I	Decay mode setting pin for Stepper 1

**Table 6-1. Pin Functions (continued)**

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
DECAY2	17	I	Decay mode setting pin for Stepper 2
STEP1	18	I	Step input signal for Stepper 1
STEP2	10	I	Step input signal for Stepper 2
DIR1	34	I	Direction input signal for Stepper 1
DIR2	36	I	Direction input signal for Stepper 2
nSLEEP	11	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode. An nSLEEP low pulse clears latched faults.
VREF1	13	I	Reference voltage input to set the full scale chopping current for Stepper 1
VREF2	15	I	Reference voltage input to set the full scale chopping current for Stepper 2
ENABLE1	28	I	Enable input for Stepper 1. Logic low on this input disables (Hi-Z) the outputs of Stepper 1.
ENABLE2	9	I	Enable input for Stepper 2. Logic low on this input disables (Hi-Z) the outputs of Stepper 2.
MODE01	29	I	Microstep setting inputs for Stepper 1
MODE11	35	I	
MODE02	27	I	Microstep setting inputs for Stepper 2
MODE12	1	I	
nFAULT1	12	O	Fault diagnostics output for Stepper 1
nFAULT2	14	O	Fault diagnostics output for Stepper 2
PAD	-	-	Exposed pad for enhanced thermal performance. Should be soldered to the PCB.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted) <sup>(1)</sup>

	MIN	MAX	UNIT
Power supply voltage (VMx)	-0.3	40	V
Charge pump voltage (VCP, CP1)	-0.3	$V_{VM} + 7$	V
Charge pump negative switching pin (CP2)	-0.3	$V_{VM}$	V
Sleep mode input voltage (nSLEEP)	-0.3	5.75	V
Control input voltage	-0.3	5.75	V
PGND pin voltage	-0.5	0.5	V
PGND pin voltages for < 1 $\mu$ s	-2.5	2.5	V
Reference input pin voltage (VREFx)	-0.3	5.75	V
Open drain output current (nFAULTx)	0	10	mA
Continuous phase node pin voltage (OUTxA, OUTxB)	-1	$V_{VM} + 1$	V
Transient 100 ns phase node pin voltage (OUTxA, OUTxB)	-3	$V_{VM} + 3$	V
Output current	0	1.5	A
Operating ambient temperature, $T_A$	-40	125	°C
Operating junction temperature, $T_J$	-40	150	°C
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 2000$	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(1)</sup>	$\pm 500$	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{VM}$	Supply voltage range for normal (DC) operation	4.5	38	V
$V_I$	Control input voltage	0	5.5	V
$V_{REFx}$	Reference voltage (VREFx)	0	3.3	V
$f_{STEP}$	Applied STEP signal <sup>(1)</sup>	0	500	kHz
$I_{RMS}$	Motor RMS current ( $xOUTx$ ) <sup>(2)</sup>	0	1.1	A
$T_A$	Operating ambient temperature	-40	125	°C
$T_J$	Operating junction temperature	-40	150	°C

- (1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load

(2) Power dissipation and thermal limits must be observed

## 7.4 Thermal Information

THERMAL METRIC		QFN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.6	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	0.3	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	11.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	°C/W

## 7.5 Electrical Characteristics

Typical values are at  $T_A = 25^\circ\text{C}$  and  $V_{VM} = 24\text{ V}$ . All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES (VM)</b>						
$I_{VM}$	VM operating supply current	ENABLE = 1, nSLEEP = 1, No motor load		6	8	mA
		nSLEEP = 1, Outputs off		5.5	7	mA
		nSLEEP = 0		1.3	3	μA
$t_{SLEEP}$	Sleep time	nSLEEP = 0 to sleep mode	120			μs
$t_{RESET}$	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	μs
$t_{ON}$	Turn-on time	VM > UVLO to output transition		0.62	0.8	ms
$t_{WAKE}$	Wake-up time	nSLEEP = 1 to output transition		0.62	0.8	ms
$t_{EN}$	Enable time	ENABLE = 0/1 to output transition			1	μs
<b>CHARGE PUMP (VCP, CP1, CP2)</b>						
$V_{VCP}$	VCP operating voltage	$6\text{ V} < V_{VM} < 38\text{ V}$		$V_{VM} + 5$		V
$f_{(VCP)}$	Charge pump switching frequency	$V_{VM} > UVLO$ , nSLEEP = 1		380		kHz
<b>LOGIC-LEVEL INPUTS (STEP, DIR, nSLEEP)</b>						
$V_{IL}$	Input logic-low voltage		0		0.8	V
$V_{IH}$	Input logic-high voltage		2		5.5	V
$V_{HYS}$	Input logic hysteresis		150	300	500	mV
$I_{INL}$	Logic input low current	$V_{IN} = 0\text{ V}$	-1		1	μA
$I_{INH}$	Logic input high current	$V_{IN} = 5\text{ V}$			30	μA
<b>TRI-LEVEL INPUTS (MODE0x, ENABLE)</b>						
$V_{I1}$	Input logic-low voltage	Tied to GND	0		0.6	V
$V_{I2}$	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
$V_{I3}$	Input logic-high voltage	Tied to 5 V	2.7		5.5	V
$I_O$	Input pull-up current			10		μA
<b>QUAD-LEVEL INPUTS (MODE1x, DECAYx)</b>						

Typical values are at  $T_A = 25^\circ\text{C}$  and  $V_{VM} = 24\text{ V}$ . All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I1}$	Input logic-low voltage	Tied to GND	0		0.6	V
$V_{I2}$		$330\text{k}\Omega \pm 5\%$ to GND	1	1.25	1.4	V
$V_{I3}$	Input Hi-Z voltage	Hi-Z	1.8	2	2.2	V
$V_{I4}$	Input logic-high voltage	Tied to 5 V	2.7		5.5	V
$I_O$	Input pull-up current			10		$\mu\text{A}$
<b>CONTROL OUTPUTS (nFAULTx)</b>						
$V_{OL}$	Output logic-low voltage	$I_O = 5\text{ mA}$			0.2	V
$I_{OH}$	Output logic-high leakage	$V_{Mx} = 24\text{ V}$	-1		1	$\mu\text{A}$
<b>MOTOR DRIVER OUTPUTS</b>						
$R_{DS(ONH)}$	High-side FET on resistance	$T_J = 25^\circ\text{C}, I_O = -1.2\text{ A}$		450	550	$\text{m}\Omega$
		$T_J = 125^\circ\text{C}, I_O = -1.2\text{ A}$		700	850	$\text{m}\Omega$
		$T_J = 150^\circ\text{C}, I_O = -1.2\text{ A}$		780	950	$\text{m}\Omega$
$R_{DS(ONL)}$	Low-side FET on resistance	$T_J = 25^\circ\text{C}, I_O = 1.2\text{ A}$		450	550	$\text{m}\Omega$
		$T_J = 125^\circ\text{C}, I_O = 1.2\text{ A}$		700	850	$\text{m}\Omega$
		$T_J = 150^\circ\text{C}, I_O = 1.2\text{ A}$		780	950	$\text{m}\Omega$
$V_f$ , Outputs		$I_O = \pm 1.2\text{ A}$			1.2	V
$I_{DSS}$	Output Leakage	Outputs, $V_{OUT} = 0$ to $V_M$	-2		7	$\mu\text{A}$
$t_{SR}$	Output rise/fall time	$V_M = 24\text{V}, I_O = 1.2\text{ A}$ , Between 10% and 90%		100		ns
$t_D$	Dead time			425		ns
$t_{BLANK}$	Current sense blanking time <sup>(1)</sup>			1		$\mu\text{s}$
<b>PWM CURRENT CONTROL (VREFx)</b>						
$K_V$	Transimpedance gain	$V_{REF} = 3.3\text{ V}$	2.09	2.2	2.31	V/A
$I_{VREFx}$	VREFx pin reference input Current		-1		1	$\mu\text{A}$
$t_{OFF}$	PWM off-time	DECAYx = 1		16		$\mu\text{s}$
		DECAYx = Hi-Z		32		
		DECAYx = $330\text{ k}\Omega$ to GND		8		
$I_{O,CH}$	AOUT and BOUT current matching	$I_O = 1.5\text{ A}$	-2.5		2.5	%
$\Delta I_{TRIP}$	Current trip accuracy	$I_O = 1.5\text{ A}$ , 68% to 100% current setting	-5		5	%
		$I_O = 1.5\text{ A}$ , 20% to 67% current setting	-10		10	
		$I_O = 1.5\text{ A}$ , 10% to 20% current setting	-15		15	
<b>PROTECTION CIRCUITS</b>						
$V_{MUVLO}$	VM UVLO threshold	VM falling	4.1	4.25	4.35	V
		VM rising	4.2	4.34	4.45	
$V_{MUVLO,HYS}$	VM UVLO hysteresis	Rising to falling threshold		90		mV



Typical values are at  $T_A = 25^\circ\text{C}$  and  $V_{VM} = 24\text{ V}$ . All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CPUV}$	Charge pump undervoltage	VCP falling		$V_{VM} + 2$		V
$I_{OCP}$	Overcurrent protection	Current through any FET	2.5			A
$t_{OCP}$	Overcurrent deglitch time			2.1		$\mu\text{s}$
$t_{RETRY}$	Overcurrent retry time			4		ms
$T_{OTSD}$	Thermal shutdown	Die temperature $T_J$	155	165	175	$^\circ\text{C}$
$T_{HYS\_OTSD}$	Thermal shutdown hysteresis	Die temperature $T_J$		20		$^\circ\text{C}$ Guaranteed by design.

(1) Guaranteed by design.

### 7.6 Indexer Timing Requirements

Typical limits are at  $T_J = 25^\circ\text{C}$  and  $V_{VM} = 24\text{ V}$ . Over recommended operating conditions unless otherwise noted.

NO.			MIN	MAX	UNIT
1	$f_{STEP}$	Step frequency		500 <sup>(1)</sup>	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	970		ns
3	$t_{WL(STEP)}$	Pulse duration, STEP low	970		ns
4	$t_{SU(DIR, Mx)}$	Setup time, DIR or MODEx to STEP rising	200		ns
5	$t_{H(DIR, Mx)}$	Hold time, STEP rising to DIR or MODEx change	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load.

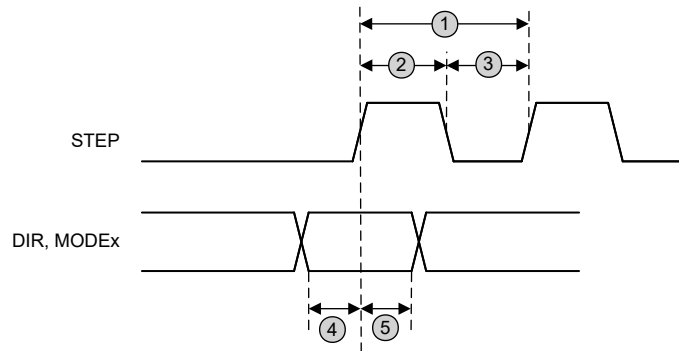
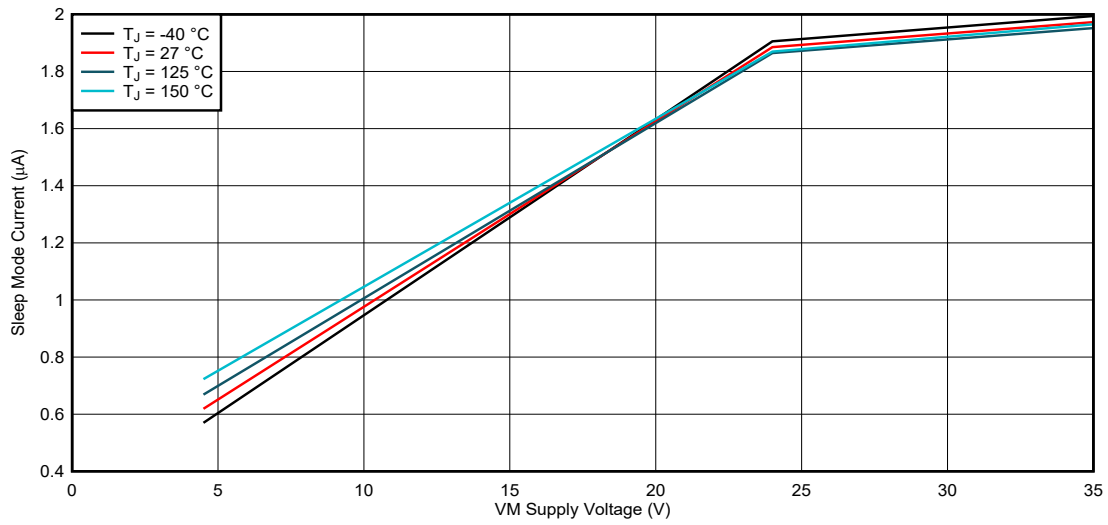
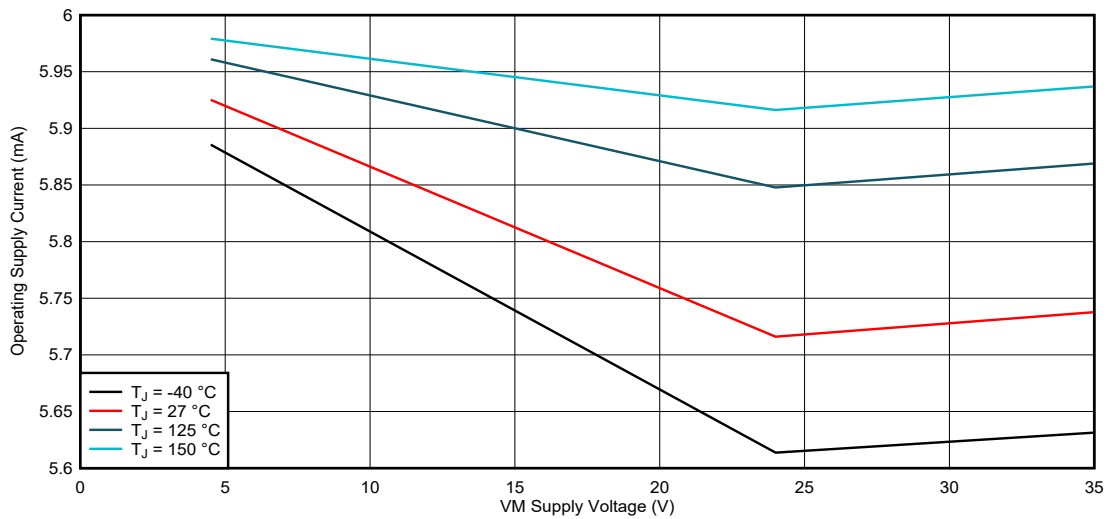


Figure 7-1. STEP and DIR Timing Diagram

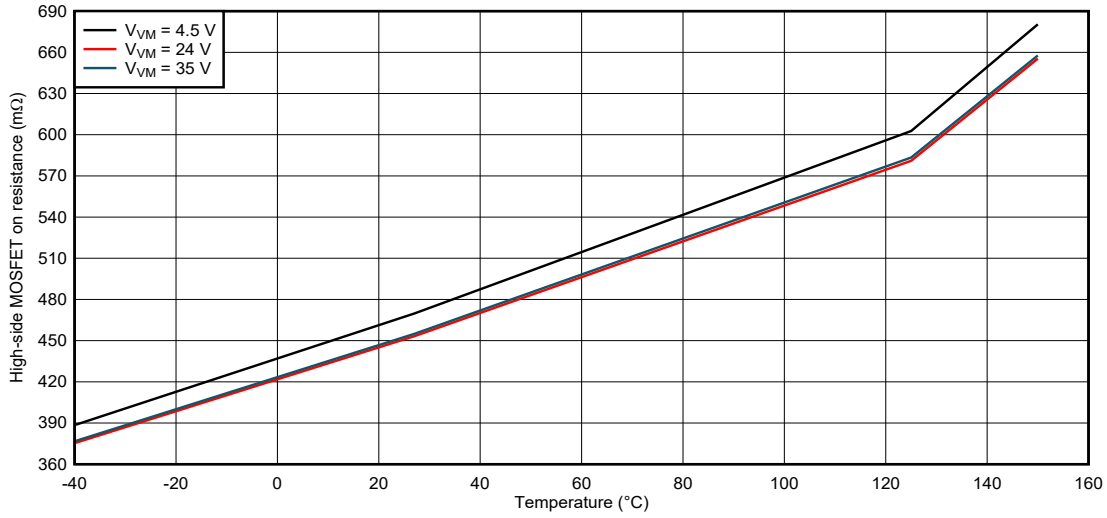
## 7.7 Typical Operating Characteristics



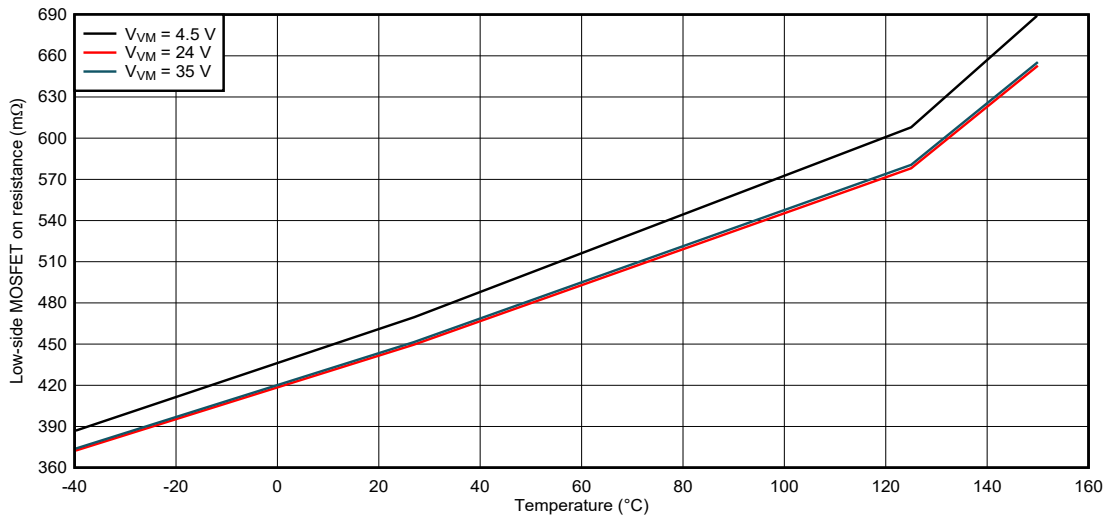
**Figure 7-2. Sleep Mode Supply Current**



**Figure 7-3. Operating Supply Current with Outputs OFF**



**Figure 7-4. High-side FET on resistance**



**Figure 7-5. Low-side FET on resistance**

## 8 Detailed Description

### 8.1 Overview

The DRV8849 is an integrated motor-driver solution for driving two bipolar stepper motors. The device provides the maximum integration by integrating four N-channel power MOSFET H-bridges, current sense resistors and regulation circuitry, and one microstepping indexer for each stepper. The DRV8849 is capable of supporting wide supply voltage of 4.5 to 38 V. The device provides an output current up to 2.5-A peak, 1.5-A full-scale, or 1.1-A root mean square (rms) on each output. The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The DRV8849 uses an integrated current-sense architecture which eliminates the need for four external power sense resistors, hence saving significant board space, BOM cost, design efforts and reduces significant power consumption. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted by the voltage at the VREF pins.

A simple STEP/DIR interface allows for an external controller to manage the direction and step rate of the stepper motor. The internal microstepping indexer can execute high-accuracy micro-stepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping. High microstepping contributes to significant audible noise reduction and smooth motion. In addition to a standard half stepping mode, a noncircular half stepping mode is available for increased torque output at higher motor RPM.

Stepper motor drivers need to re-circulate the winding current by implementing several types of decay modes, like slow decay, mixed decay and fast decay. The DRV8849 comes with smart tune decay modes. The smart tune is an innovative decay mechanism that automatically adjusts for optimal current regulation performance agnostic of voltage, motor speed, variation and aging effects. Smart tune Ripple Control uses a variable off-time, ripple current control scheme to minimize distortion of the motor winding current. Smart tune Dynamic Decay uses a fixed off-time, dynamic fast decay percentage scheme to minimize distortion of the motor winding current while minimizing frequency content and significantly reducing design efforts.

A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

## 8.2 Functional Block Diagram

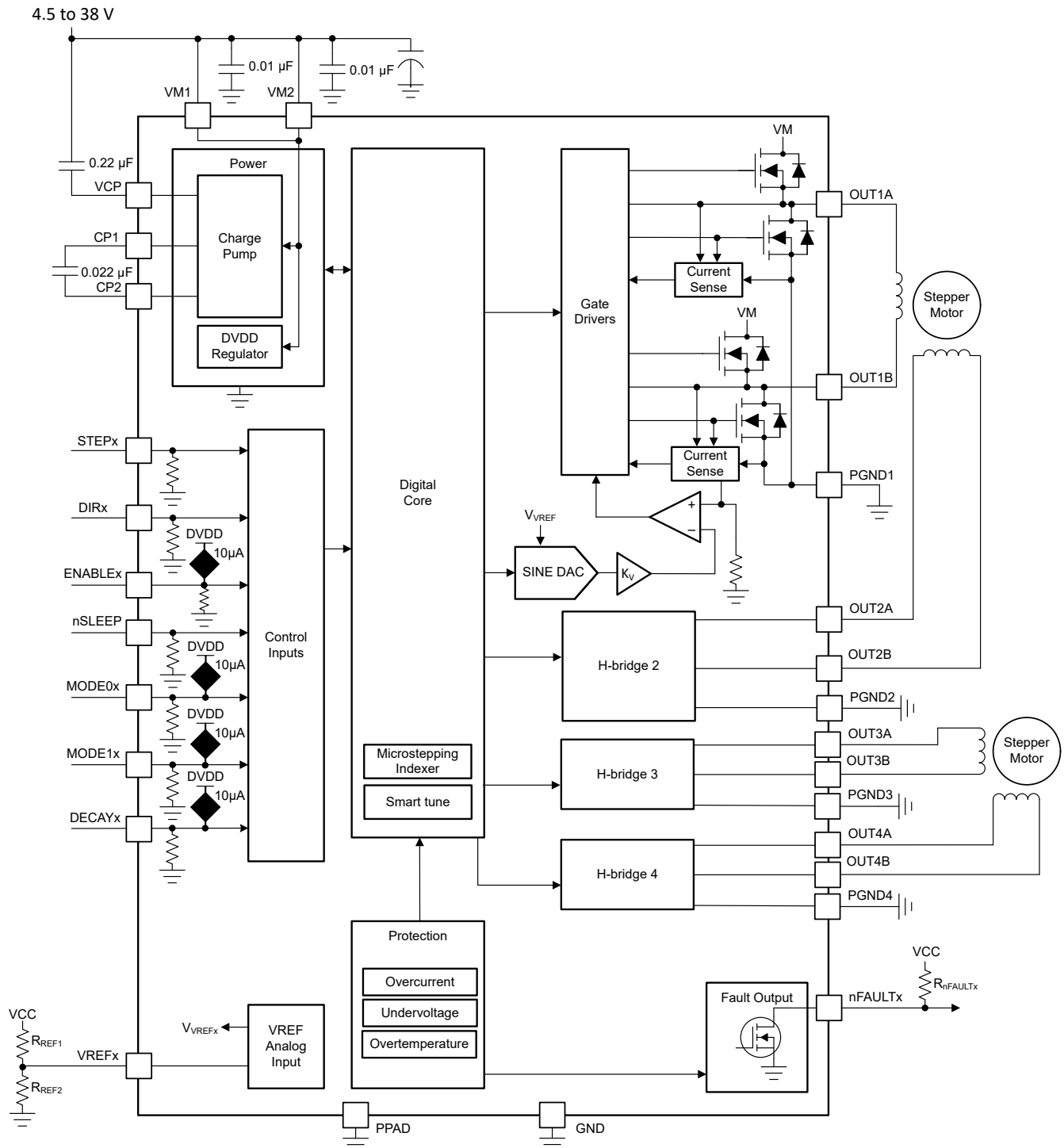


Figure 8-1. Functional Block Diagram

## 8.3 Feature Description

The following table shows the recommended values of the external components for the driver.

**Table 8-1. DRV8849 External Components**

COMPONENT	PIN 1	PIN 2	RECOMMENDED
$C_{VM1}$	VM1	PGND	X7R, 0.01- $\mu$ F, VM-rated ceramic capacitor
$C_{VM2}$	VM2	PGND	X7R, 0.01- $\mu$ F, VM-rated ceramic capacitor
$C_{VCP}$	VCP	VM1	X7R, 0.22- $\mu$ F, 16-V ceramic capacitor
$C_{SW}$	CP1	CP2	X7R, 0.022- $\mu$ F, VM-rated ceramic capacitor
$R_{nFAULTx}$	VCC <sup>(1)</sup>	nFAULTx	>4.7-k $\Omega$ resistor
$R_{REF1x}$	VREFx	VCC	Resistor to limit chopping current.
$R_{REF2x}$	VREFx	GND	

(1) VCC is not a pin of the DRV8849, but a VCC supply voltage pullup is required for open-drain nFAULT outputs.

### 8.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, RMS, and full-scale.

#### 8.3.1.1 Peak Current Rating

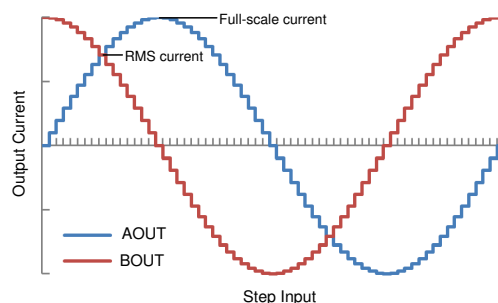
The peak current in a stepper driver is limited by the overcurrent protection trip threshold  $I_{OCP}$ . The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general the minimum value of  $I_{OCP}$  specifies the peak current rating of the stepper motor driver. For the DRV8849, the peak current rating is 2.5 A per bridge.

#### 8.3.1.2 RMS Current Rating

The RMS (average) current is determined by the thermal considerations of the IC. The RMS current is calculated based on the  $R_{DS(ON)}$ , rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The actual operating RMS current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8849, the RMS current rating is 1.1 A per bridge.

#### 8.3.1.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the RMS current, the full-scale current is also determined by the thermal considerations of the device. The full-scale current rating is approximately  $\sqrt{2} \times I_{RMS}$  for a sinusoidal current waveform, and  $I_{RMS}$  for a square wave current waveform (full step).

**Figure 8-2. Full-Scale and RMS Current**

### 8.3.2 Microstepping Indexer

Built-in indexer logic in the DRV8849 allows a number of different step modes. The MODE0 and MODE1 pins are used to configure the step mode as shown in Table 8-2. The settings can be changed on the fly.

**Table 8-2. Microstepping Indexer Settings**

MODE0x	MODE1x	STEP MODE
0	0	Full step (2-phase excitation) with 100% current
0	330 kΩ to GND	Full step (2-phase excitation) with 71% current
1	0	Non-circular 1/2 step
Hi-Z	0	1/2 step
0	1	1/4 step
1	1	1/8 step
Hi-Z	1	1/16 step
0	Hi-Z	1/32 step
Hi-Z	330 kΩ to GND	1/64 step
Hi-Z	Hi-Z	1/128 step
1	Hi-Z	1/256 step

Table 8-3 shows the relative current and step directions for full-step (71% current), 1/2 step, 1/4 step and 1/8 step operation. Higher microstepping resolutions follow the same pattern. The OUTxA current is the sine of the electrical angle and the OUTxB current is the cosine of the electrical angle. Positive current is defined as current flowing from the OUTxA pin to the OUTxB pin while driving.

At each rising edge of the STEP input the indexer travels to the next state in the table. The direction is shown with the DIR pin logic high. If the DIR pin is logic low, the sequence is reversed.

**Note**

If the step mode is changed on the fly while stepping, the indexer advances to the next valid state for the new step mode setting at the rising edge of STEP.

The initial excitation state is an electrical angle of 45°, corresponding to 71% of full-scale current in both coils. This state is entered after power-up, after exiting logic undervoltage lockout, or after exiting sleep mode.

**Table 8-3. Relative Current and Step Directions**

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	OUTxA CURRENT (% FULL-SCALE)	OUTxB CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	1	1		0%	100%	0.00
2				20%	98%	11.25
3	2			38%	92%	22.50
4				56%	83%	33.75
5	3	2	1	71%	71%	45.00
6				83%	56%	56.25
7	4			92%	38%	67.50
8				98%	20%	78.75
9	5	3		100%	0%	90.00
10				98%	-20%	101.25
11	6			92%	-38%	112.50
12				83%	-56%	123.75
13	7	4	2	71%	-71%	135.00
14				56%	-83%	146.25
15	8			38%	-92%	157.50

**Table 8-3. Relative Current and Step Directions (continued)**

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	OUTxA CURRENT (% FULL-SCALE)	OUTxB CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
16				20%	-98%	168.75
17	9	5		0%	-100%	180.00
18				-20%	-98%	191.25
19	10			-38%	-92%	202.50
20				-56%	-83%	213.75
21	11	6	3	-71%	-71%	225.00
22				-83%	-56%	236.25
23	12			-92%	-38%	247.50
24				-98%	-20%	258.75
25	13	7		-100%	0%	270.00
26				-98%	20%	281.25
27	14			-92%	38%	292.50
28				-83%	56%	303.75
29	15	8	4	-71%	71%	315.00
30				-56%	83%	326.25
31	16			-38%	92%	337.50
32				-20%	98%	348.75

Table 8-4 shows the full step operation with 100% full-scale current. This stepping mode consumes more power than full-step mode with 71% current, but provides a higher torque at high motor RPM.

**Table 8-4. Full Step with 100% Current**

FULL STEP 100%	OUTxA CURRENT (% FULL-SCALE)	OUTxB CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	100	100	45
2	100	-100	135
3	-100	-100	225
4	-100	100	315

Table 8-5 shows the noncircular 1/2-step operation. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

**Table 8-5. Non-Circular 1/2-Stepping Current**

NON-CIRCULAR 1/2-STEP	OUTxA CURRENT (% FULL-SCALE)	OUTxB CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	-100	135
5	0	-100	180
6	-100	-100	225
7	-100	0	270
8	-100	100	315



### 8.3.3 Controlling VREF with an MCU DAC

In some cases, the full-scale output current may need to be changed between many different values, depending on motor speed and loading. The voltage of the VREF pin can be adjusted in the system to change the full-scale current.

In this mode of operation, as the DAC voltage increases, the full-scale regulation current increases as well. For proper operation, the output of the DAC should not rise above 3.3 V for DRV8849.

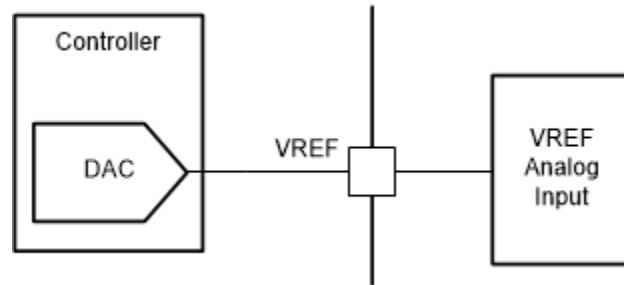


Figure 8-3. Controlling VREF with a DAC Resource

The VREF pin can also be adjusted using a PWM signal and low-pass filter.

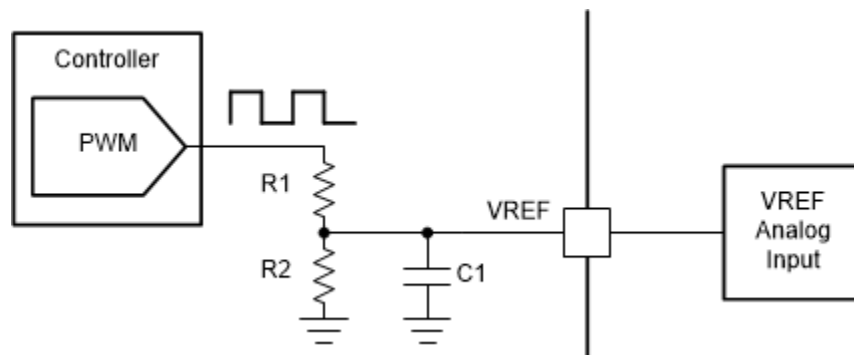


Figure 8-4. Controlling VREF With a PWM Resource

### 8.3.4 Current Regulation and Decay Modes

The current through the motor windings is regulated by an adjustable, off-time PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold (as shown in Figure 8-6, Item 1), the bridge enters a decay mode determined by the DECAY pin setting to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

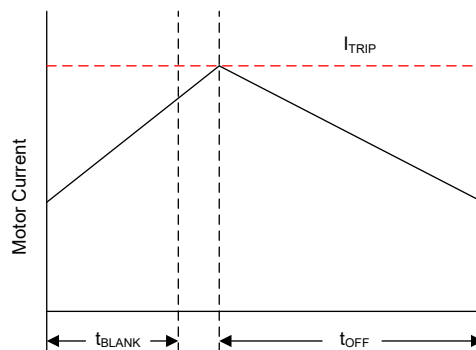
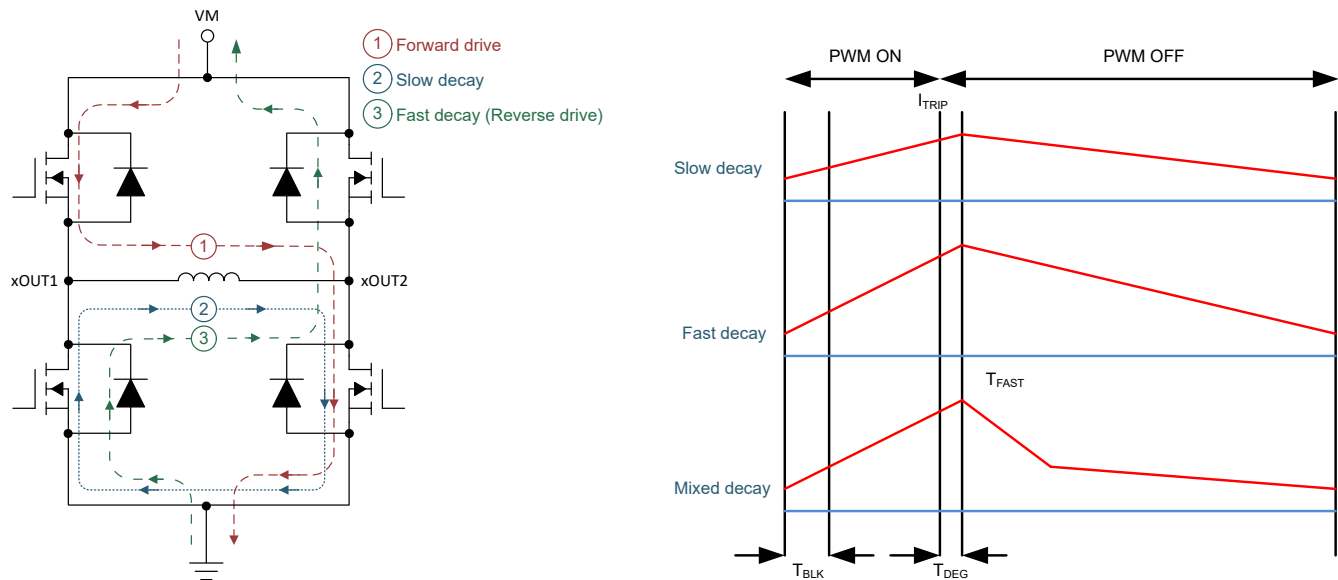


Figure 8-5. Current Chopping Waveform

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

- In fast decay mode, as soon as the PWM chopping current level is reached, the H-bridge reverses state by switching on the opposite arm MOSFETs to allow the winding current to flow in the opposite direction. As the winding current approaches zero, the H-bridge is disabled to prevent further reverse current flow. Fast decay mode is shown in Figure 8-6, item 3.
- In slow decay mode, the winding current is re-circulated by enabling both low-side MOSFETs in the H-bridge. This is shown in Figure 8-6, Item 2.



**Figure 8-6. Decay Modes**

The PWM regulation current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. The current sense MOSFETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the voltage at the VREF pins.

The full-scale regulation current ( $I_{FS}$ ) can be calculated as -

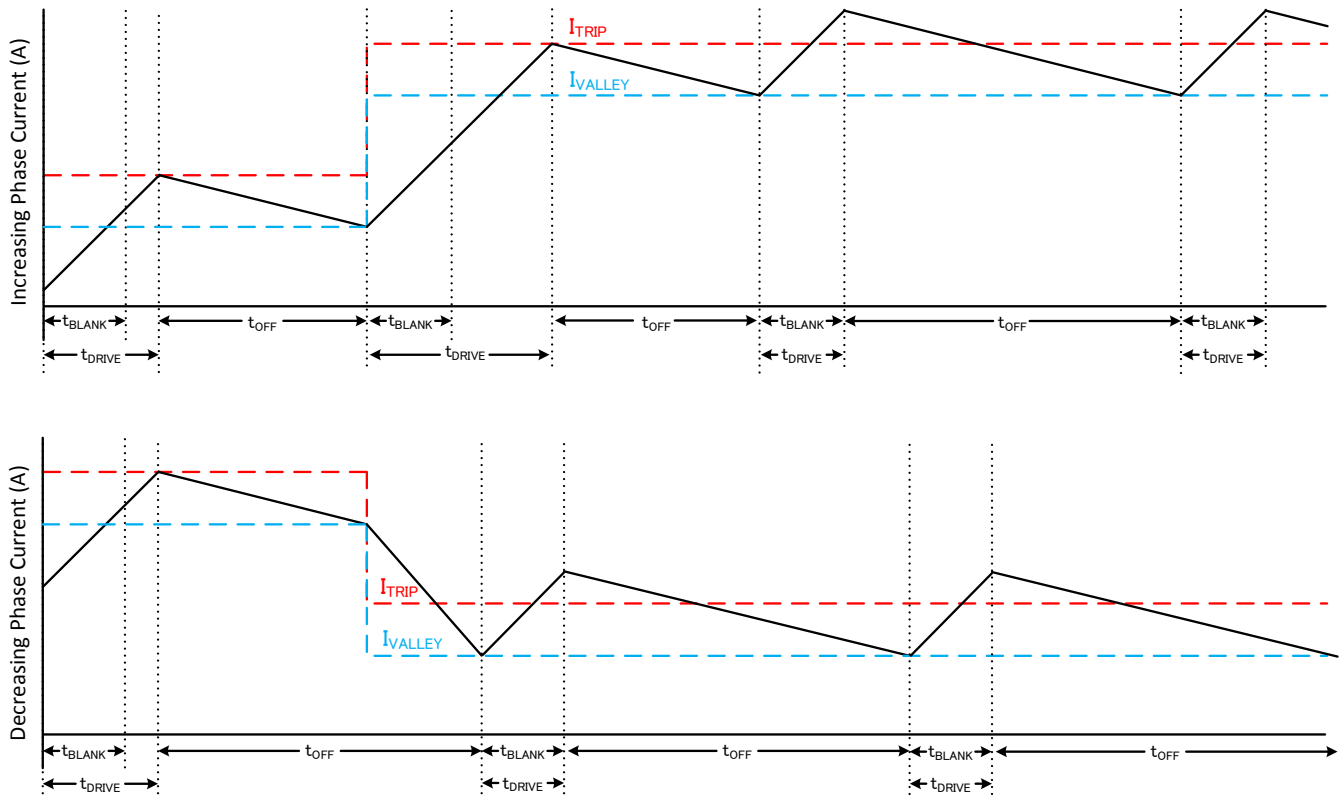
$$I_{FS} (A) = V_{REFx} (V) / K_V (V/A) = V_{REFx} (V) / 2.2 (V/A).$$

The decay mode of the DRV8849 is selected by the DECAY pins as shown in Table 8-6. The decay modes can not be changed on the fly - they are latched after power-up.

**Table 8-6. Decay Mode Settings**

DECAYx	DECAY MODE
0	Smart tune Ripple Control
1	Smart tune Dynamic Decay, 16 $\mu$ s OFF time
Hi-Z	Smart tune Dynamic Decay, 32 $\mu$ s OFF time
330k to GND	Smart tune Dynamic Decay, 8 $\mu$ s OFF time

### 8.3.4.1 Smart tune Ripple Control



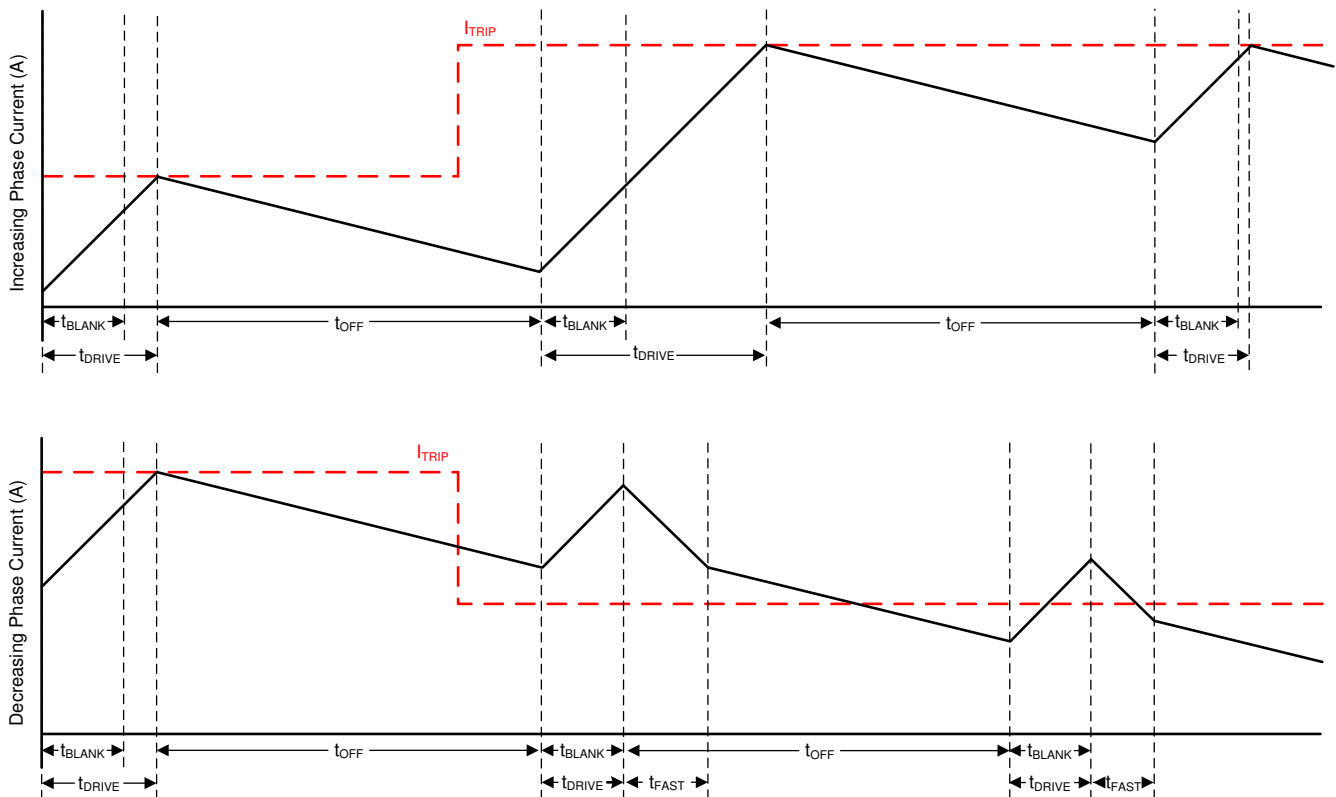
**Figure 8-7. Smart tune Ripple Control Decay Mode**

Smart tune Ripple Control operates by setting an  $I_{VALLEY}$  level alongside the  $I_{TRIP}$  level. When the current level reaches  $I_{TRIP}$ , instead of entering slow decay until the  $t_{OFF}$  time expires, the driver enters slow decay until  $I_{VALLEY}$  is reached. Slow decay operates by turning on both low-side MOSFETs, allowing the current to recirculate. In this mode,  $t_{OFF}$  varies depending on the current level and operating conditions.

The ripple current in this decay mode is  $11 \text{ mA} + 1\%$  of  $I_{TRIP}$ , where  $I_{TRIP}$  is the regulation current of a particular microstep level.

The ripple control method allows much tighter regulation of the current level, thereby increasing motor efficiency and reducing audible noise and vibration. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve small current ripple in the current regulation.

### 8.3.4.2 Smart tune Dynamic Decay



**Figure 8-8. Smart tune Dynamic Decay Mode**

Unlike smart tune Ripple Control, smart tune Dynamic Decay operates with fixed OFF time. Smart tune Dynamic Decay dynamically adjusts the fast decay percentage of the total mixed decay time. This eliminates the need for motor decay tuning by automatically determining the best mixed decay setting that results in the lowest ripple and best performance for the motor.

The fast decay percentage is optimized iteratively each PWM cycle. If the motor current overshoots the target  $I_{TRIP}$  level, then the mixed decay mode becomes more aggressive (by increasing fast decay percentage) on the next cycle to prevent loss of current regulation. If a long drive time must occur to reach the target  $I_{TRIP}$  level, the decay mode becomes less aggressive (by reducing fast decay percentage) on the next cycle to operate with less ripple. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly. Smart tune Dynamic Decay operates with fixed 8  $\mu$ s, 16  $\mu$ s or 32  $\mu$ s OFF time.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

#### 8.3.4.3 Blanking time

This function blanks the output of the current sense comparator when the outputs are switched by the internal current control circuitry. The comparator output is blanked to prevent false detections of overcurrent conditions, due to reverse recovery currents, or to switching transients related to the capacitance of the load. The blank time,  $t_{BLANK}$ , is approximately 1  $\mu$ s.

#### 8.3.5 Charge Pump

A charge pump is integrated to supply a high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CP1 and CP2 pins to act as the flying capacitor.

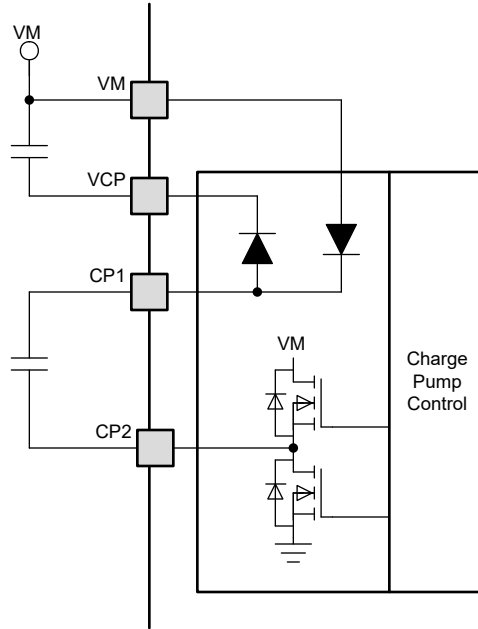


Figure 8-9. Charge pump

### 8.3.6 Logic Level, tri-level and quad-level Pin Diagrams

The following diagram shows the input structure for MODE0x, and ENABLE pins.

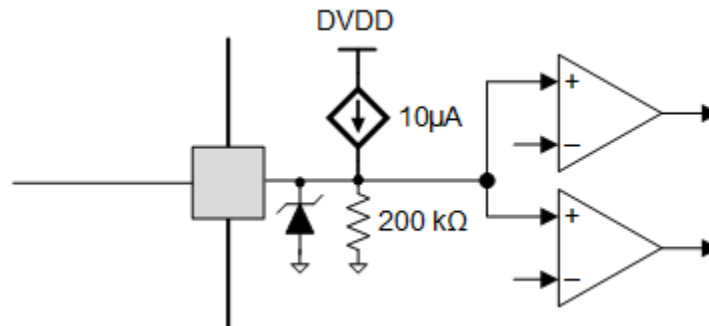


Figure 8-10. Tri-Level Input Pin Diagram

Figure 8-11 shows the input structure for MODE1x and DECAYx pins.

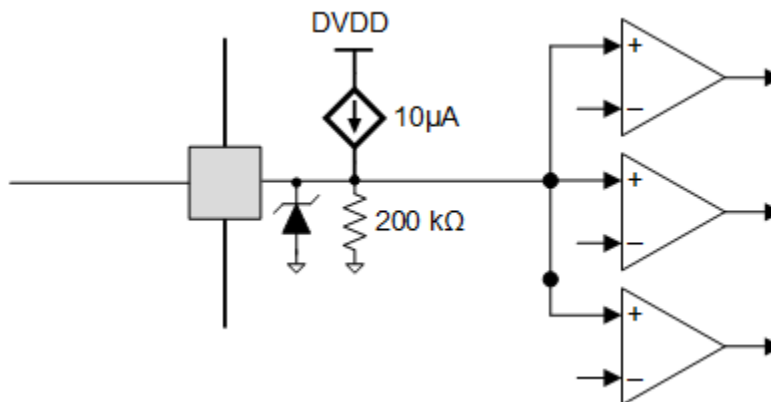


Figure 8-11. Quad-Level Input Pin Diagram

Figure 8-12 shows the input structure for STEP, DIR and nSLEEP pins.

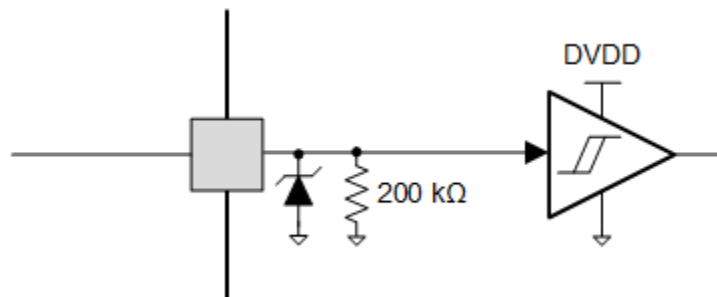


Figure 8-12. Logic-Level Input Pin Diagram

### 8.3.7 nFAULT Pins

The nFAULT pins have open-drain outputs and should be pulled up to a 5-V or 3.3-V supply. When a fault is detected, the nFAULT pin of the corresponding stepper will be logic low. nFAULT pin will be high after power-up. An external supply must be used for pulling up the nFAULT pins.

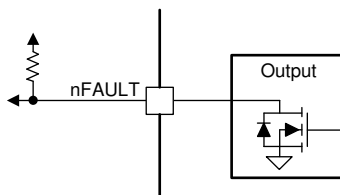


Figure 8-13. nFAULT Pins

### 8.3.8 Protection Circuits

The DRV8849 is fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

#### 8.3.8.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins fall below the UVLO-threshold voltage for the voltage supply, all the outputs are disabled, and the nFAULT pins are driven low. The charge pump is disabled in this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VM undervoltage condition is removed.

#### 8.3.8.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pins are driven low. The charge pump remains active during this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed.

#### 8.3.8.3 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the  $t_{OCP}$  time, the FETs in both H-bridges for that stepper driver are disabled and the corresponding nFAULT pin is driven low. The charge pump remains active during this condition. The overcurrent protection can operate in two different modes: latched shutdown and automatic retry.

The ENABLE pin for a particular stepper driver should be Hi-Z to select latched shutdown mode, and should be HIGH (>2.7 V) to select automatic retry mode. ENABLE1 pin controls the OCP recovery method for Stepper 1, and ENABLE2 pin controls the OCP recovery method for Stepper 2.

### 8.3.8.3.1 Latched Shutdown

In this mode, after an OCP event, the outputs of the affected stepper driver are disabled and the corresponding nFAULT pin is driven low. Once the OCP condition is removed, normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

### 8.3.8.3.2 Automatic Retry

In this mode, after an OCP event the outputs of the affected stepper are disabled and the corresponding nFAULT pin is driven low. Normal operation resumes automatically (motor-driver operation and nFAULT released) after the  $t_{RETRY}$  time has elapsed and the fault condition is removed.

### 8.3.8.4 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit ( $T_{OTSD}$ ), all MOSFETs are disabled, and the nFAULT pins are driven low. The charge pump is disabled during this condition. The thermal shutdown protection can operate in two different modes: latched shutdown and automatic retry.

The ENABLE1 pin should be Hi-Z to select latched shutdown mode, and should be HIGH ( $>2.7V$ ) to select automatic retry mode. ENABLE1 pin controls the OTSD recovery method for both Stepper drivers.

#### 8.3.8.4.1 Latched Shutdown

In this mode, after an OTSD event, all the outputs are disabled and the nFAULT pins are driven low. After the junction temperature falls below the overtemperature threshold limit minus the hysteresis ( $T_{OTSD} - T_{HYS\_OTSD}$ ), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

#### 8.3.8.4.2 Automatic Retry

In this mode, after an OTSD event, all the outputs are disabled and the nFAULT pins are driven low. Normal operation resumes (motor-driver operation and the nFAULT lines released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis ( $T_{OTSD} - T_{HYS\_OTSD}$ ).

### 8.3.8.5 Fault Condition Summary

**Table 8-7. Fault Condition Summary**

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	$VM < V_{UVLO}$	—	nFAULT1, nFAULT2	Disabled	Disabled	Disabled	Reset ( $VM < 3.9V$ )	Automatic: $VM > V_{UVLO}$
VCP undervoltage (CPUV)	$VCP < V_{CPUV}$	—	nFAULT1, nFAULT2	Disabled	Operating	Operating	Operating	$VCP > V_{CPUV}$
Overcurrent (OCP)	$I_{OUT1} > I_{OCP}$	ENABLE1 = Hi-Z	nFAULT1	Disabled (Stepper 1)	Operating	Operating	Operating	Latched (Stepper 1)
		ENABLE1 = 1	nFAULT1	Disabled (Stepper 1)	Operating	Operating	Operating	Automatic retry (Stepper 1): $t_{RETRY}$
	$I_{OUT2} > I_{OCP}$	ENABLE2 = Hi-Z	nFAULT2	Disabled (Stepper 2)	Operating	Operating	Operating	Latched (Stepper 2)
		ENABLE2 = 1	nFAULT2	Disabled (Stepper 2)	Operating	Operating	Operating	Automatic retry (Stepper 2): $t_{RETRY}$
Thermal Shutdown (OTSD)	$T_J > T_{TSD}$	ENABLE1 = Hi-Z	nFAULT1, nFAULT2	Disabled	Disabled	Operating	Operating	Latched
		ENABLE1 = 1	nFAULT1, nFAULT2	Disabled	Disabled	Operating	Operating	Automatic: $T_J < T_{OTSD} - T_{HYS\_OTSD}$

## 8.4 Device Functional Modes

### 8.4.1 Sleep Mode (nSLEEP = 0)

The device state is managed by the nSLEEP pin. When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled and the charge pump is disabled. The  $t_{\text{SLEEP}}$  time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The  $t_{\text{WAKE}}$  time must elapse before the device is ready for inputs.

### 8.4.2 Disable Mode (nSLEEP = 1, ENABLE = 0)

The ENABLE pin is used to enable or disable the device. When the ENABLE pin is low, the corresponding output drivers are disabled in the Hi-Z state.

### 8.4.3 Operating Mode (nSLEEP = 1, ENABLE = Hi-Z/1)

When the nSLEEP pin is high, the ENABLE pin is Hi-Z or 1, and  $V_M > UVLO$ , the corresponding stepper enters the active mode. The  $t_{\text{WAKE}}$  time must elapse before the stepper is ready for inputs.

### 8.4.4 nSLEEP Reset Pulse

A fault can be cleared through a quick nSLEEP pulse. This pulse width must be greater than 20  $\mu\text{s}$  and shorter than 40  $\mu\text{s}$ . If nSLEEP is low for longer than 40  $\mu\text{s}$  but less than 120  $\mu\text{s}$ , the faults are cleared and the device may or may not shutdown, as shown in the timing diagram. This reset pulse does not affect the status of the charge pump or other functional blocks.

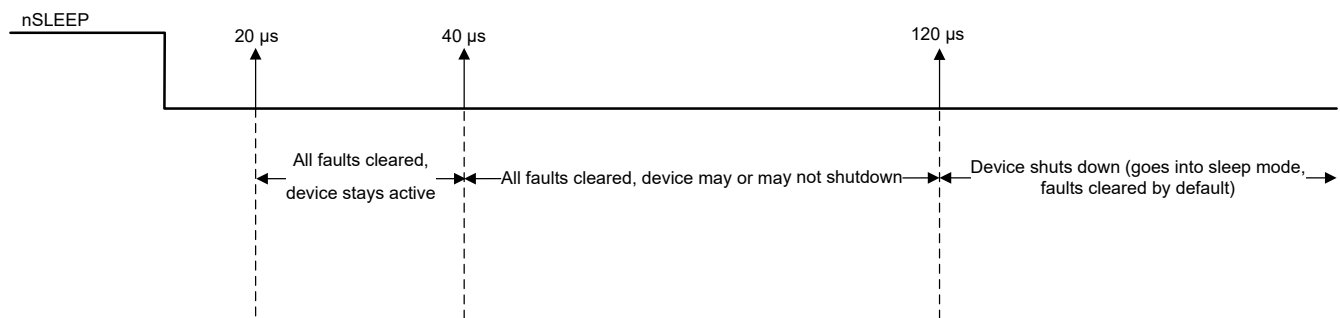


Figure 8-14. nSLEEP Reset Pulse

### 8.4.5 Functional Modes Summary

Table 8-8 lists a summary of the functional modes.

Table 8-8. Functional Modes Summary

	CONDITION	CONFIGURATION	H-BRIDGE	CHARGE PUMP	INDEXER	Logic
Sleep mode	$4.5\text{ V} < V_M < 38\text{ V}$	nSLEEP pin = 0	Disabled	Disabled	Disabled	Disabled
Operating	$4.5\text{ V} < V_M < 38\text{ V}$	nSLEEP pin = 1 ENABLE pin = 1 or Hi-Z	Operating	Operating	Operating	Operating
Disabled	$4.5\text{ V} < V_M < 38\text{ V}$	nSLEEP pin = 1 ENABLE pin = 0	Disabled	Operating	Operating	Operating



## 9 Application and Implementation

### Note

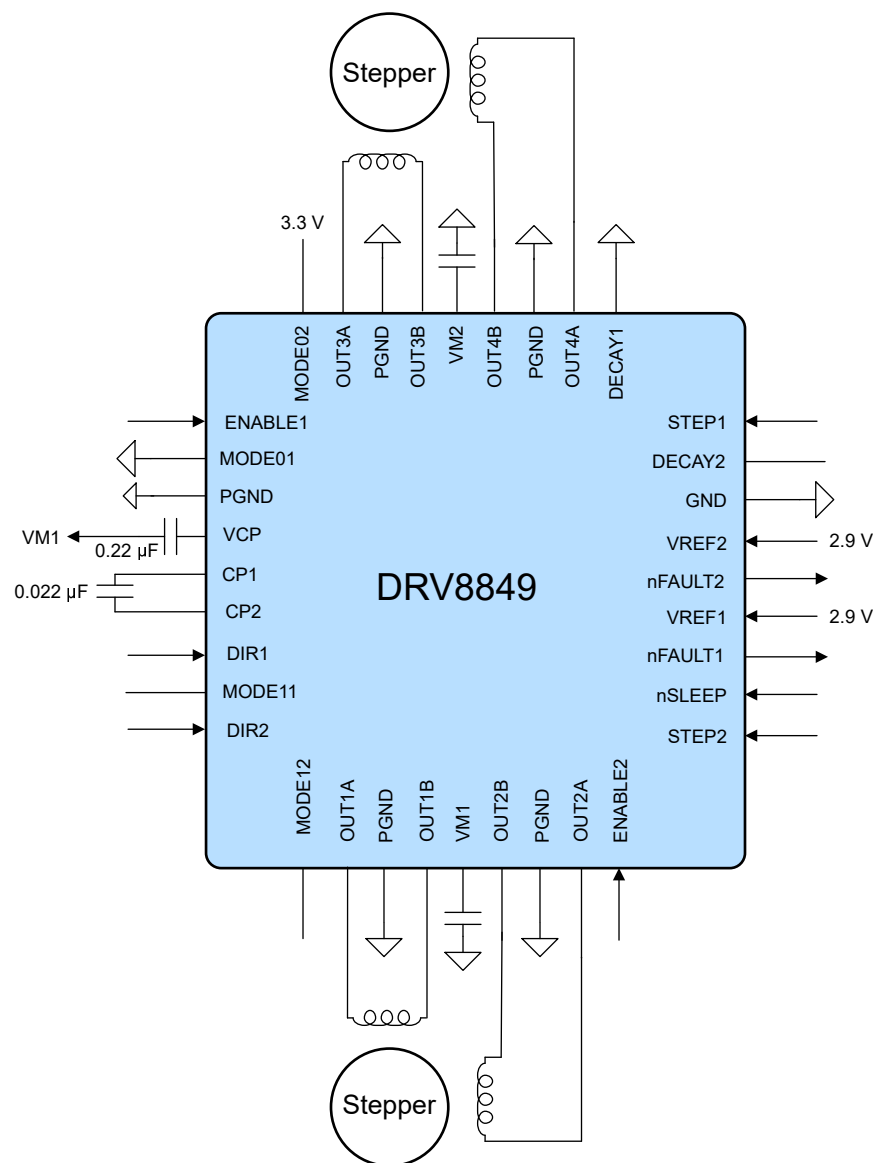
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The DRV8849 is used to control two bipolar stepper motors.

### 9.2 Typical Application

The following design procedure can be used to configure the DRV8849 to drive two stepper motors.



**Figure 9-1. Typical Application Schematic**

## 9.2.1 Design Requirements

Table 9-1 lists the design input parameters for a typical application.

**Table 9-1. Design Parameters**

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor 1 winding resistance	R <sub>L1</sub>	2.4 Ω/phase
Motor 2 winding resistance	R <sub>L2</sub>	2 Ω/phase
Motor 1 winding inductance	L <sub>L1</sub>	5.8 mH/phase
Motor 2 winding inductance	L <sub>L2</sub>	4.7 mH/phase
Motor 1 full step angle	θ <sub>step1</sub>	1.8°/step
Motor 2 full step angle	θ <sub>step2</sub>	1.8°/step
Target microstepping level (motor 1)	n <sub>m1</sub>	1/32 step
Target microstepping level (motor 2)	n <sub>m2</sub>	1/256 step
Target motor 1 speed	v <sub>1</sub>	46.8 rpm
Target motor 2 speed	v <sub>2</sub>	23.4 rpm
Target full-scale current (motor 1)	I <sub>FS1</sub>	1.3 A
Target full-scale current (motor 2)	I <sub>FS2</sub>	1.3 A

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8849 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency  $f_{\text{step}}$  must be applied to the corresponding STEP pin. If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target speed. Use Equation 1 to calculate  $f_{\text{step}}$  for a desired motor speed ( $v$ ), microstepping level ( $n_m$ ), and motor full step angle ( $\theta_{\text{step}}$ )

$$f_{\text{step}} \text{ (steps / s)} = \frac{v \text{ (rpm)} \times 360 \text{ (}^\circ \text{ / rot)}}{\theta_{\text{step}} \text{ (}^\circ \text{ / step)} \times n_m \text{ (steps / microstep)} \times 60 \text{ (s / min)}} \quad (1)$$

The value of  $\theta_{\text{step}}$  can be found in the stepper motor data sheet, or written on the motor. For example, the motors in this application are required to rotate at 1.8°/step for a target of 46.8 rpm at 1/32 microstep mode (for Motor 1); and for a target of 23.4 rpm at 1/256 microstep mode (for Motor 2). Using Equation 1,  $f_{\text{step}}$  can be calculated as 5 kHz for Motor 1 and 20 kHz for Motor 2.

The microstepping level is set by the MODE0x and MODE1x pins and can be any of the settings listed in Table 8-2. Higher microstepping results in a smoother motor motion and less audible noise, but requires a higher  $f_{\text{step}}$  to achieve the same motor speed.

### 9.2.2.2 Current Regulation

In a stepper motor, the full-scale current ( $I_{\text{FS}}$ ) is the maximum current driven through either winding. This quantity depends on the VREF voltage. The maximum allowable voltage on the VREF pin is 3.3 V for DRV8849. During stepping,  $I_{\text{FS}}$  defines the current chopping threshold ( $I_{\text{TRIP}}$ ) for the maximum current step.  $I_{\text{FS}} \text{ (A)} = V_{\text{REF}} \text{ (V)} / 2.2 \text{ (V/A)}$

### 9.2.2.3 Decay Modes

The DRV8849 supports two different smart tune decay modes, as shown in Table 8-6. In this example, motor 1 is driven with smart tune ripple control decay mode, whereas the motor 2 is driven with smart tune dynamic decay mode with 32 μs OFF time.

### 9.2.2.4 Application Curves

CH2: STEP2 (5 V/div), CH3: STEP1 (5 V/div), CH7: IOUT\_1 (1 A/div), CH8: IOUT\_4 (1 A/div)

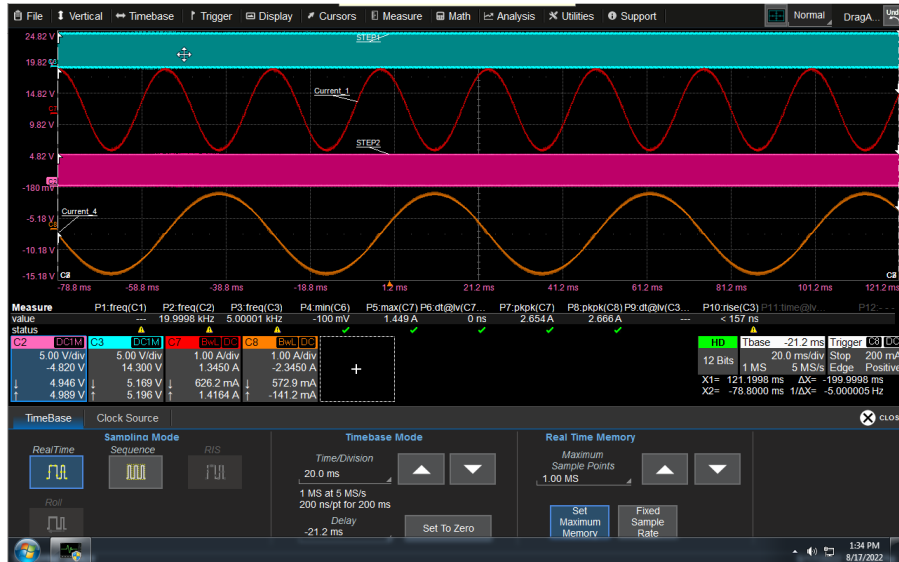


Figure 9-2. DRV8849 driving two Stepper Motors

## 10 Layout

- A low-ESR ceramic capacitor must be placed in between the CP1 and CP2 pins. A value of 0.022  $\mu\text{F}$  rated for VM is recommended. Place this component as close to the pins as possible.
- A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22  $\mu\text{F}$  rated for 16 V is recommended. Place this component as close to the pins as possible.
- The device must be soldered directly onto the PCB. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias should be used to transfer heat to other layers of the PCB.
- It is important to have a low impedance single-point ground located very close to the device. Connect the exposed pad and the ground plane directly under the device ground.
- The input capacitors should be placed as close to the device supply pins as possible. The ceramic capacitor should be closer to the pins than the bulk capacitor.

### 10.1 Layout Guidelines

Follow the layout example of the DRV8849 EVM. The design files can be downloaded from the [DRV8849EVM](#) product folder.

### 10.2 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

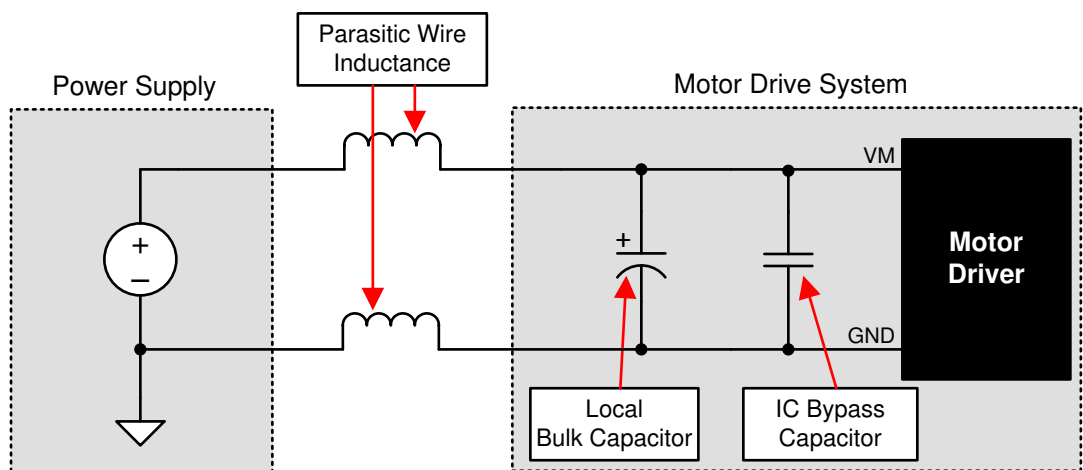
The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.



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**Figure 10-1. Example Setup of Motor Drive System With External Power Supply**

## 11 Device and Documentation Support

### 11.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [How to Reduce Audible Noise in Stepper Motors](#) application report
- Texas Instruments, [How to Improve Motion Smoothness and Accuracy](#) application report
- Texas Instruments, [How to Drive Unipolar Stepper Motors with DRV8xxx](#) application report
- Texas Instruments, [Calculating Motor Driver Power Dissipation](#) application report
- Texas Instruments, [Current Recirculation and Decay Modes](#) application report
- Texas Instruments, [Understanding Motor Driver Current Ratings](#) application report
- Texas Instruments, [Motor Drives Layout Guide](#) application report

## 12 Mechanical, Packaging, and Orderable Information

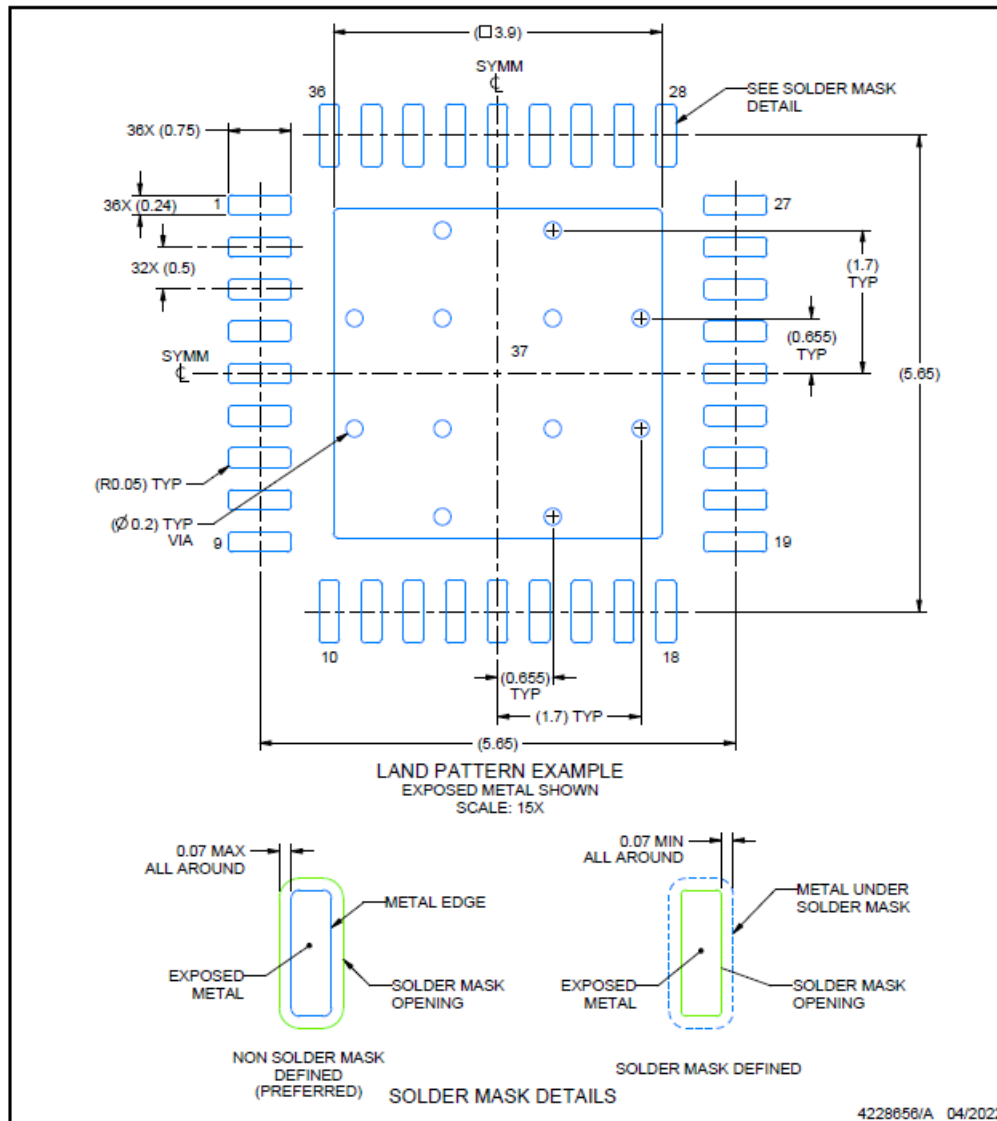
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### EXAMPLE BOARD LAYOUT

RHH0036H

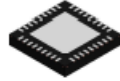
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

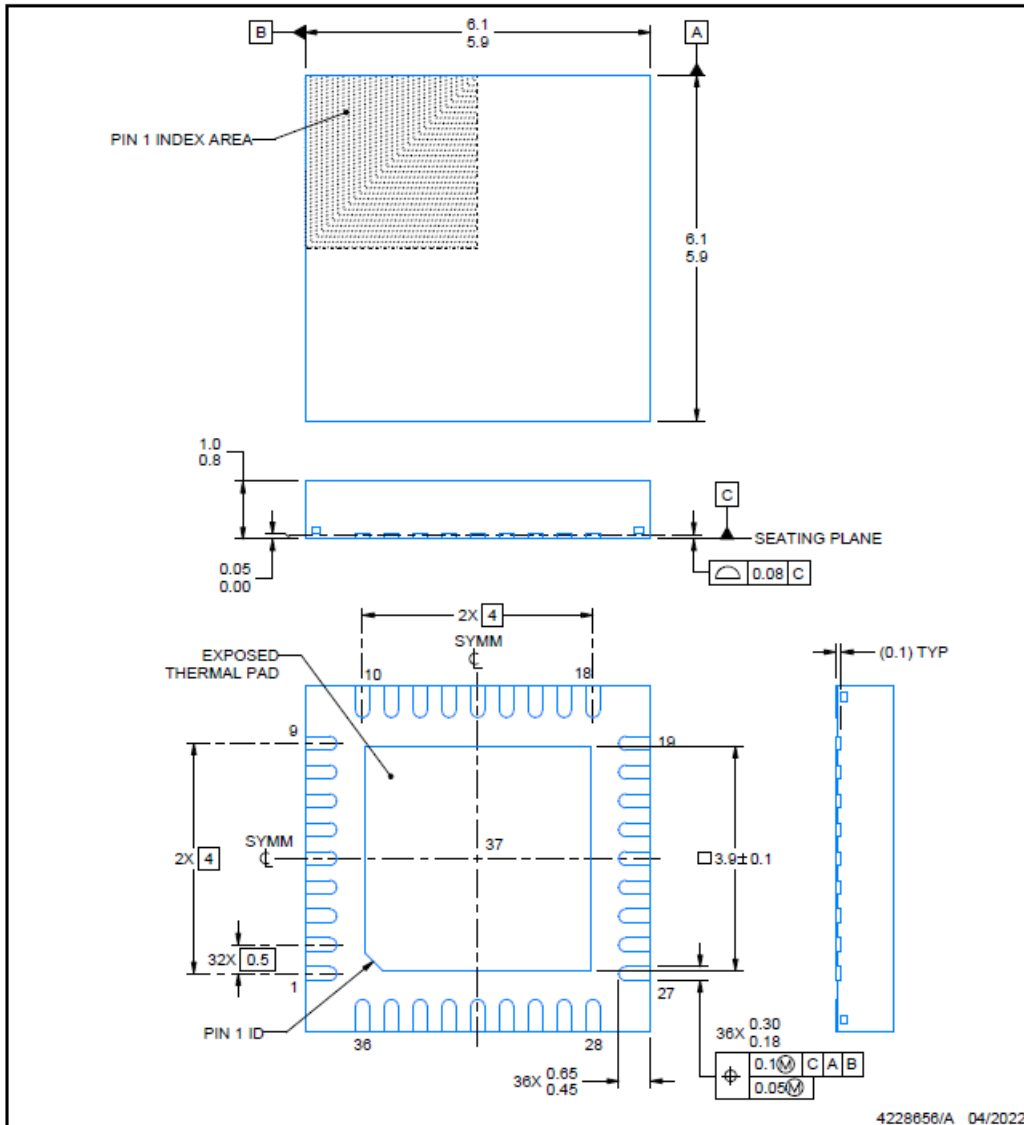
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



**RHH0036H**

**PACKAGE OUTLINE**  
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

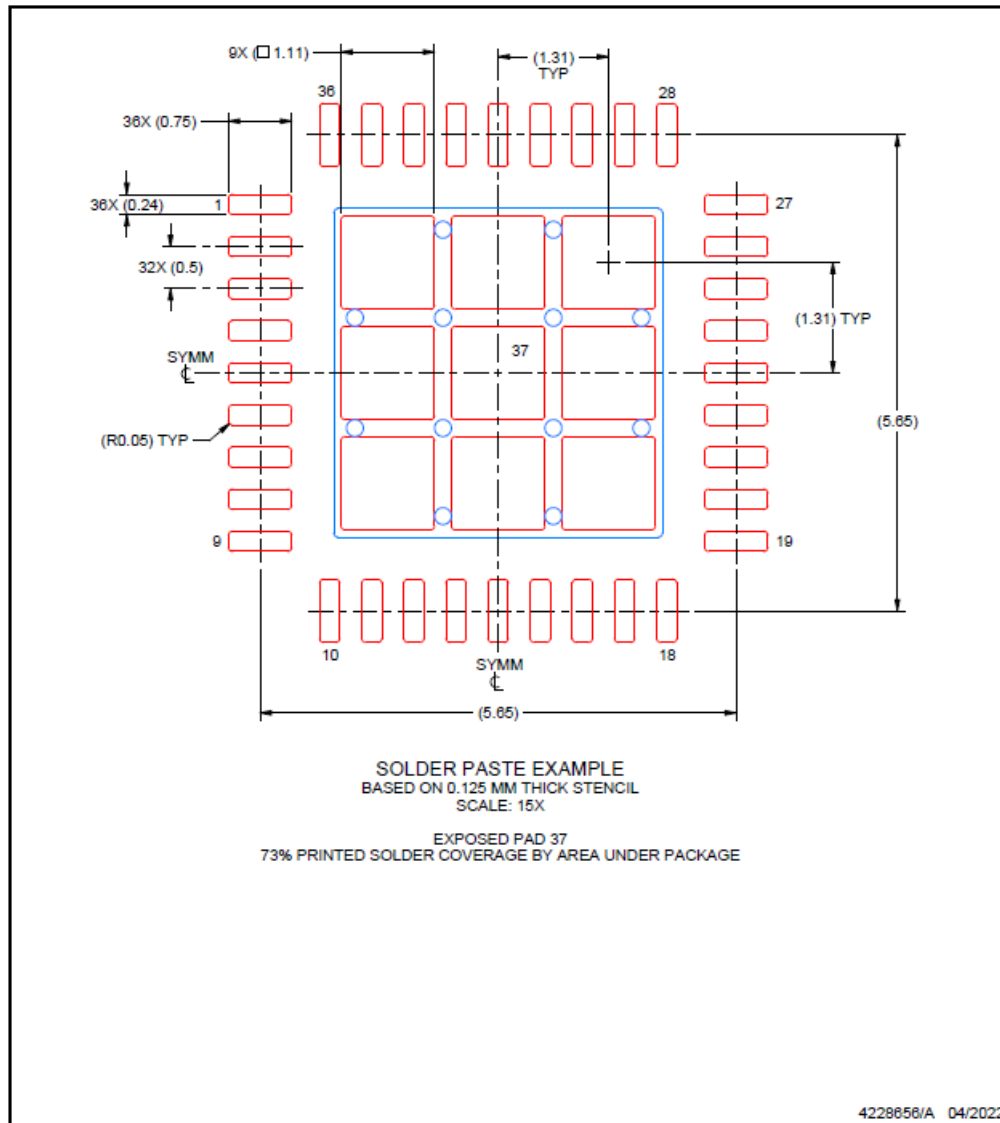
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

**EXAMPLE STENCIL DESIGN**

**RHH0036H**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8849RHHR	ACTIVE	VQFN	RHH	36	4000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8849	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8849RHHR	VQFN	RHH	36	4000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8849RHHR	VQFN	RHH	36	4000	367.0	367.0	35.0

## GENERIC PACKAGE VIEW

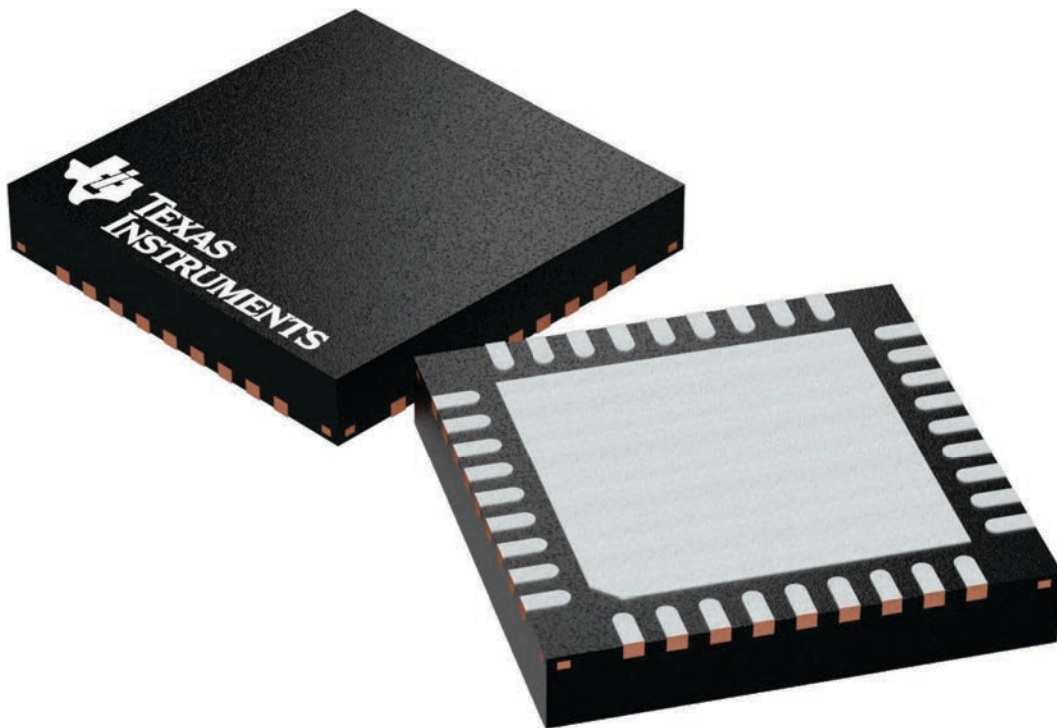
**RHH 36**

**VQFN - 1 mm max height**

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



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[AM4967GSTR-G1](#) [TB6562AFG\(O,8,EL\)](#) [LA6584JA-AH](#) [LB11961-W-AH](#) [LC898212XD-SH](#) [NCV70501DW002R2G](#) [VNH5200ASTR-E](#)  
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