DS25CP104A / DS25CP114 3.125 Gbps 4x4 LVDS Crosspoint Switch with Transmit Pre-Emphasis and Receive Equalization

Check for Samples: DS25CP104A, DS25CP114

FEATURES

- **DC - 3.125 Gbps Low Jitter, Low Skew, Low Power Operation**
- **Pin and SMBus Configurable, Fully Differential, Non-Blocking Architecture**
- **Pin (Two Levels) and SMBus (Four Levels) Selectable Pre-Emphasis and Equalization Eliminate ISI Jitter**
- **Wide Input Common Mode Range Enables Easy Interface to CML and LVPECL Drivers**
- **$\overline{\text{LOS}}$ Circuitry Detects Open Inputs Fault Condition**
- **On-Chip 100Ω Input and Output Termination Minimizes Insertion and Return Losses, Reduces Component Count, Minimizes Board Space The DS25CP114 Eliminates the On-Chip Input Termination for Added Design Flexibility.**
- **8 kV ESD on LVDS I/O Pins Protects Adjoining Components**
- **Small 6 mm x 6 mm WQFN-40 Space Saving Package**

APPLICATIONS

- **SD/HD/3G HD SDI Routers**
- **OC-48 / STM-16**
- **InfiniBand and FireWire**

DESCRIPTION

The DS25CP104A and DS25CP114 are 3.125 Gbps 4x4 LVDS crosspoint switches optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity. The non-blocking architecture allows connections of any input to any output or outputs. The switch configuration can be accomplished via external pins or the System Management Bus (SMBus) interface.

The DS25CP104A and DS25CP114 feature four levels (Off, Low, Medium, High) of transmit pre-emphasis (PE) and four levels (Off, Low, Medium, High) of receive equalization (EQ) settable via the SMBus interface. Off and Medium PE levels and Off and Low EQ levels are settable with the external pins. In addition, the SMBus circuitry enables the loss of signal ($\overline{\text{LOS}}$) monitors that can inform a system of the presence of an open inputs condition (e.g. disconnected cable).

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. On the DS25CP104A each differential input and output is internally terminated with a 100Ω resistor to lower return losses, reduce component count and further minimize board space. For added design flexibility the 100Ω input terminations on the DS25CP114 have been eliminated. This enables a designer to build custom crosspoint configurations and distribution circuits that require a limited multidrop signaling topology.

Typical Application

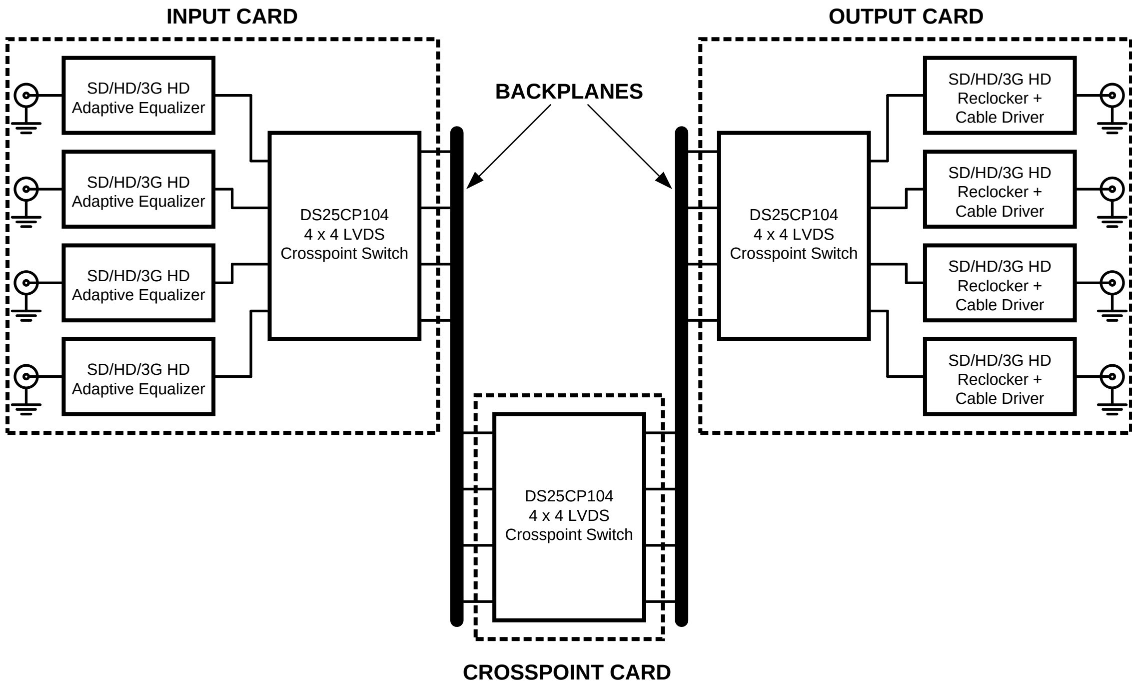
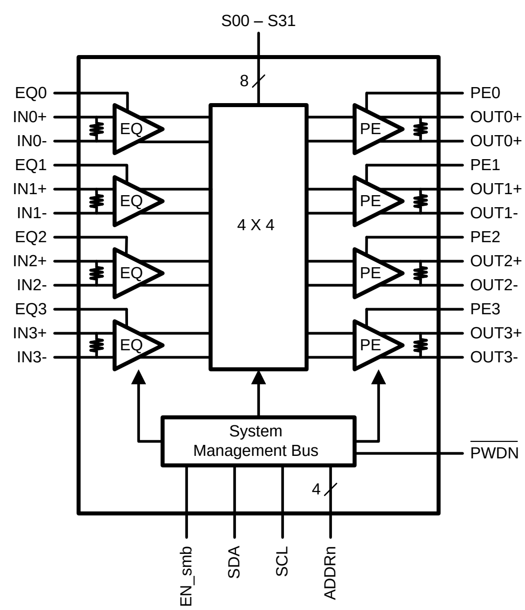


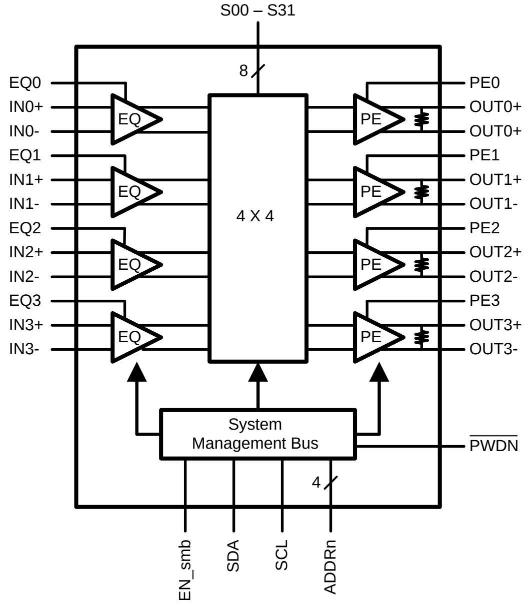
Table 1. Device Information

Device	Function	Termination Option	Available Signal Conditioning
DS25CP104A	4x4 Crosspoint Switch	Internal 100Ω for LVDS inputs	4 Levels: PE and EQ
DS25CP114	4x4 Crosspoint Switch	None: Requires external termination	4 Levels : PE and EQ

Block Diagram

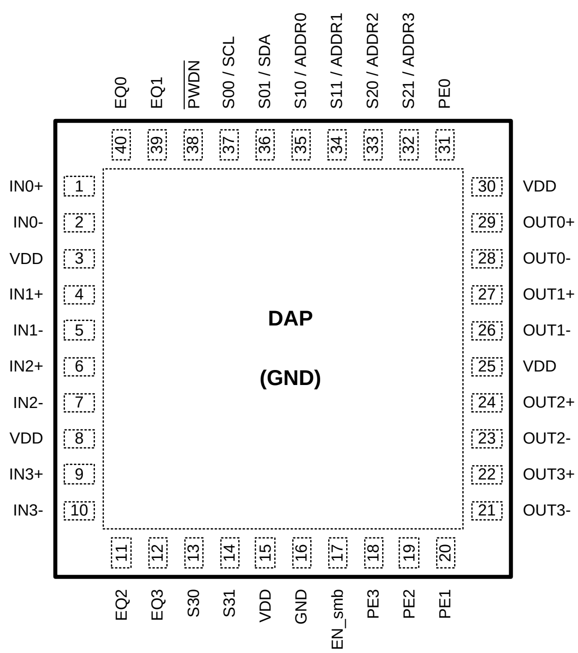


DS25CP104A



DS25CP114

Connection Diagram



DS25CP104A / DS25CP114 Pin Diagram

PIN DESCRIPTIONS[(1)]

Pin Name	Pin Number	I/O, Type	Pin Description
IN0+, IN0- , IN1+, IN1-, IN2+, IN2-, IN3+, IN3-	1, 2, 4, 5, 6, 7, 9, 10	I, LVDS	Inverting and non-inverting high speed LVDS input pins. These 4 input pairs have a 100 Ohm differential input termination on the CP104A device. The CP114 eliminates the input termination for added design flexibility.
OUT0+, OUT0-, OUT1+, OUT1-, OUT2+, OUT2-, OUT3+, OUT3-	29, 28, 27, 26, 24, 23, 22, 21	O, LVDS	Inverting and non-inverting high speed LVDS output pins. Each output pair has an internal 100 Ohm termination to improve device return loss characteristics.
EQ0, EQ1, EQ2, EQ3	40, 39, 11, 12	I, LVCMOS	Receive equalization level select pins. These pins are functional regardless of the EN_smb pin state.
PE0, PE1, PE2, PE3	31, 20, 19, 18	I, LVCMOS	Transmit pre-emphasis level select pins. These pins are functional regardless of the EN_smb pin state.
EN_smb	17	I, LVCMOS	System Management Bus (SMBus) enable pin. The pin has an internal pull down. When the pin is set to a [1], the device is in the SMBus mode. All SMBus registers are reset when this pin is toggled. There is a 20k pulldown device on this pin.
S00/SCL	37	I, LVCMOS	For EN_smb = [0], these pins select which LVDS input is routed to the OUT0. In the SMBus mode, when the EN_smb = [1], these pins are SMBus clock input and data input pins respectively.
S01/SDA	36	I/O, LVCMOS	
S10/ADDR0, S11/ADDR1	35, 34	I, LVCMOS	For EN_smb = [0], these pins select which LVDS input is routed to the OUT1. In the SMBus mode, when the EN_smb = [1], these pins are the User-Set SMBus Slave Address inputs.
S20/ADDR2, S21/ADDR3	33, 32	I, LVCMOS	For EN_smb = [0], these pins select which LVDS input is routed to the OUT2. In the SMBus mode, when the EN_smb = H, these pins are the User-Set SMBus Slave Address inputs.
S30, S31	13, 14	I, LVCMOS	For EN_smb = [0], these pins select which LVDS input is routed to the OUT3. In the SMBus mode, when the EN_smb = [1], these pins are non-functional and should be tied to either logic H or L.
$\overline{\text{PWDN}}$	38	I, LVCMOS	For EN_smb = [0], this is the power down pin. When the $\overline{\text{PWDN}}$ is set to a [0], the device is in the power down mode. The SMBus circuitry can still be accessed provided the EN_smb pin is set to a [1]. In the SMBus mode, the device is powered up by either setting the $\overline{\text{PWDN}}$ pin to [1] **OR** by writing a [1] to the Control Register D[7] bit ($\overline{\text{SoftPWDN}}$). The device will be powered down by setting the $\overline{\text{PWDN}}$ pin to [0] **AND** by writing a [0] to the Control Register D[7] bit ($\overline{\text{SoftPWDN}}$).
VDD	3, 8, 15,25, 30	Power	Power supply pins.
GND	16, DAP	Power	Ground pin and a pad (DAP - die attach pad).

(1) Center DAP connection must be made to GND for optimum electrical and thermal performance.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)(2)]

Supply Voltage	−0.3V to +4V
LVCMOS Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVCMOS Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Input Voltage	−0.3V to +4V
Differential Input Voltage |VID| (DS25CP104A)	1.0V
LVDS Differential Input Voltage (DS25CP114)	V_{CC} + 0.6V
LVDS Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Differential Output Voltage	0V to 1.0V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
RTA0040A Package	4.65W
Derate RTA0040A Package	37.2 mW/°C above +25°C
Package Thermal Resistance	
θ_{JA}	+26.9°C/W
θ_{JC}	+3.8°C/W
ESD Susceptibility	
HBM [(3)]	≥8 kV
MM [(4)]	≥250V
CDM [(5)]	≥1250V

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114C
(4) Machine Model, applicable std. JESD22-A115-A
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID}) (DS25CP104A only)	0		1	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C
SMBus (SDA, SCL)			3.6	V

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.[(1)(2)(3)]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V

(1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
(3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current	V_{IN} = 3.6V V_{CC} = 3.6V			0	±10	μA
			EN_smb pin	40	175	250	μA
I_{IL}	Low Level Input Current	V_{IN} = GND V_{CC} = 3.6V			0	±10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA, V_{CC} = 0V			−0.9	−1.5	V
V_{OL}	Low Level Output Voltage	I_{OL}= 4 mA	SDA pin			0.4	V
LVDS INPUT DC SPECIFICATIONS							
V_{ID}	Input Differential Voltage(4)			0		1	V
V_{TH}	Differential Input High Threshold	V_{CM} = +0.05V or V_{CC}-0.05V			0	+100	mV
V_{TL}	Differential Input Low Threshold			−100	0		mV
V_{CMR}	Input Common Mode Voltage Range	V_{ID} = 100 mV		0.05		V_{CC} - 0.05	V
I_{IN}	Input Current(5)	V_{IN} = +3.6V or 0V V_{CC} = 3.6V or 0V			±1	±10	μA
C_{IN}	Input Capacitance	Any LVDS Input Pin to GND			1.7		pF
R_{IN}	Input Termination Resistor(6)	Between IN+ and IN-			100		Ω
LVDS OUTPUT DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States			-35		35	mV
V_{OS}	Offset Voltage	R_L = 100Ω		1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States			-35		35	mV
I_{OS}	Output Short Circuit Current (7)	OUT to GND			-35	-55	mA
		OUT to V_{CC}			7	55	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND			1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT-			100		Ω
SUPPLY CURRENT							
I_{CC1}	Supply Current	$\overline{PWDN}$ = 0			40	50	mA
I_{CC2}	Supply Current	$\overline{PWDN}$ = 1 PE = Off, EQ = Off Broadcast (1:4) Mode			145	175	mA
I_{CC3}	Supply Current	$\overline{PWDN}$ = 1 PE = Off, EQ = Off Quad Buffer (4:4) Mode			157	190	mA

(4) Input Differential Voltage (V_{ID}) The DS25CP104A limits input amplitude to 1 volt. The DS25CP114 supports any V_{ID} within the supply voltage to GND range.
(5) I_{IN} is applied to both pins of the LVDS input pair at the same time.
(6) Input Termination Resistor (R_{IN}) The DS25CP104A provides an integrated 100 ohm input termination for each high speed LVDS pair. The DS25CP114 eliminates this internal termination.
(7) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS (3)							
t_{PLHD}	Differential Propagation Delay Low to High	$R_L = 100\Omega$			480	650	ps
t_{PHLD}	Differential Propagation Delay High to Low				460	650	ps
t_{SKD1}	Pulse Skew $\|t_{PLHD} - t_{PHLD}\|$, (4)				20	100	ps
t_{SKD2}	Channel to Channel Skew , (5)				40	125	ps
t_{SKD3}	Part to Part Skew , (6)				50	200	ps
t_{LHT}	Rise Time	$R_L = 100\Omega$			80	150	ps
t_{HLT}	Fall Time				80	150	ps
t_{ON}	Power Up Time	Time from $\overline{PWDN}$ =LH to OUTn active			6	20	µs
t_{OFF}	Power Down Time	Time from $\overline{PWDN}$ =HL to OUTn inactive			8	25	ns
t_{SEL}	Select Time	Time from Sn =LH or HL to new signal at OUTn			8	12	ns
JITTER PERFORMANCE WITH EQ = Off, PE = Off (3)(Figure 5)							
t_{RJ1}	Random Jitter (RMS Value) No Test Channels (7)	V_{ID} = 350 mV, V_{CM} = 1.2V, Clock (RZ)	1.25 GHz		0.5	1.1	ps
t_{RJ2}			1.5625 GHz		0.5	1.1	ps
t_{DJ1}	Deterministic Jitter (Peak to Peak) No Test Channels (8)	V_{ID} = 350 mV, V_{CM} = 1.2V, K28.5 (NRZ)	2.5 Gbps		10	22	ps
t_{DJ2}			3.125 Gbps		10	27	ps
t_{TJ1}	Total Jitter (Peak to Peak) No Test Channels (9)	V_{ID} = 350 mV, V_{CM} = 1.2V, PRBS-23 (NRZ)	2.5 Gbps		0.07	0.11	UI_{P-P}
t_{TJ2}			3.125 Gbps		0.13	0.16	UI_{P-P}
JITTER PERFORMANCE WITH EQ = Off, PE = Low(3) (Figure 6, Figure 9)							
t_{RJ1A}	Random Jitter (RMS Value) Test Channels A (7)	V_{ID} = 350 mV, V_{CM} = 1.2V, Clock (RZ)	1.25 GHz		0.5	1.1	ps
t_{RJ2A}			1.5625 GHz		0.5	1.1	ps
t_{DJ1A}	Deterministic Jitter (Peak to Peak) Test Channels A (8)	V_{ID} = 350 mV, V_{CM} = 1.2V, K28.5 (NRZ)	2.5 Gbps		10	22	ps
t_{DJ2A}			3.125 Gbps		10	27	ps
JITTER PERFORMANCE WITH EQ = Off, PE = Medium (3) (Figure 6, Figure 9)							
t_{RJ1B}	Random Jitter (RMS Value) Test Channels B (7)	V_{ID} = 350 mV, V_{CM} = 1.2V, Clock (RZ)	1.25 GHz		0.5	1.1	ps
t_{RJ2B}			1.5625 GHz		0.5	1.1	ps
t_{DJ1B}	Deterministic Jitter (Peak to Peak) Test Channels B (8)	V_{ID} = 350 mV, V_{CM} = 1.2V, K28.5 (NRZ)	2.5 Gbps		12	30	ps
t_{DJ2B}			3.125 Gbps		12	30	ps
t_{TJ1B}	Total Jitter (Peak to Peak) Test Channels B (9)	V_{ID} = 350 mV, V_{CM} = 1.2V, PRBS-23 (NRZ)	2.5 Gbps		0.08	0.10	UI_{P-P}
t_{TJ2B}			3.125 Gbps		0.10	0.15	UI_{P-P}

(1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
(2) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operating Conditions at the time of product characterization and are not guaranteed.
(3) Specification is guaranteed by characterization and is not tested in production.
(4) t_{SKD1}, $|t_{PLHD} - t_{PHLD}|$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(5) t_{SKD2}, Channel to Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Broadcast mode (any one input to all outputs).
(6) t_{SKD3}, Part to Part Skew, is defined as the difference between the same signal path of any two devices running at the same V_{CC} and within 5°C of each other within the operating temperature range.
(7) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
(8) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
(9) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.[1][2]

Symbol	Parameter	Conditions		Min	Typ	Max	Units
JITTER PERFORMANCE WITH EQ = Off, PE = High[3] **(Figure 6, Figure 9)**							
t_{RJ1C}	Random Jitter (RMS Value) Test Channels C [7]	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ)	1.25 GHz		0.5	1.1	ps
t_{RJ2C}			1.5625 GHz		0.5	1.1	ps
t_{DJ1C}	Deterministic Jitter (Peak to Peak) Test Channels C [8]	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ)	2.5 Gbps		30	60	ps
t_{DJ2C}			3.125 Gbps		30	65	ps
JITTER PERFORMANCE WITH PE = Off, EQ = Low[3] **(Figure 7, Figure 9)**							
t_{RJ1D}	Random Jitter (RMS Value) Test Channels D [7]	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ)	1.25 GHz		0.5	1.1	ps
t_{RJ2D}			1.5625 GHz		0.5	1.1	ps
t_{DJ1D}	Deterministic Jitter (Peak to Peak) Test Channels D [8]	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ)	2.5 Gbps		20	40	ps
t_{DJ2D}			3.125 Gbps		20	40	ps
t_{TJ1D}	Total Jitter (Peak to Peak) Test Channels D [9]	V_{ID} = 350 mV V_{CM} = 1.2V PRBS-23 (NRZ)	2.5 Gbps		0.08	0.15	UI_{P-P}
t_{TJ2D}			3.125 Gbps		0.09	0.20	UI_{P-P}
JITTER PERFORMANCE WITH PE = Off, EQ = Medium[3] **(Figure 7, Figure 9)**							
t_{RJ1E}	Random Jitter (RMS Value) Test Channels E [7]	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ)	1.25 GHz		0.5	1.1	ps
t_{RJ2E}			1.5625 GHz		0.5	1.1	ps
t_{DJ1E}	Residual Deterministic Jitter (Peak to Peak) Test Channels E [8]	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ)	2.5 Gbps		35	60	ps
t_{DJ2E}			3.125 Gbps		28	55	ps
JITTER PERFORMANCE WITH PE = Off, EQ = High[3] **(Figure 7, Figure 9)**							
t_{RJ1F}	Random Jitter (RMS Value) Test Channels F [7]	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ)	1.25 GHz		1.3	1.8	ps
t_{RJ2F}			1.5625 GHz		1.4	2.4	ps
t_{DJ1F}	Residual Deterministic Jitter (Peak to Peak) Test Channels F [10]	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ)	2.5 Gbps		30	75	ps
t_{DJ2F}			3.125 Gbps		35	90	ps
JITTER PERFORMANCE WITH PE = Medium, EQ = Low[11] **(Figure 7, Figure 9)**							
t_{RJ1G}	Random Jitter (RMS Value) Input Test Channels D Output Test Channels B [12]	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ)	1.25 GHz		0.5	1.1	ps
t_{RJ2G}			1.5625 GHz		0.5	1.1	ps
t_{DJ1G}	Deterministic Jitter (Peak to Peak) Input Test Channels D Output Test Channels B [10]	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ)	2.5 Gbps		25		ps
t_{DJ2G}			3.125 Gbps		20		ps
SMBus AC SPECIFICATIONS							
f_{SMB}	SMBus Operating Frequency			10		100	kHz
t_{BUF}	Bus free time between Stop and Start Conditions			4.7			µs
$t_{HD:SDA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.			4.0			µs
$t_{SU:SDA}$	Repeated Start Condition setup time.			4.7			µs
$t_{SU:SDO}$	Stop Condition setup time			4.0			µs
$t_{HD:DAT}$	Data hold time			300			ns

(10) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
(11) Specification is guaranteed by characterization and is not tested in production.
(12) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{SU:DAT}$	Data setup time		250			ns
$t_{TIMEOUT}$	Detect clock low timeout		25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period		4.0		50	µs
t_{POR}	Time in which a device must be operational after power-on reset				500	ms

DC TEST CIRCUITS

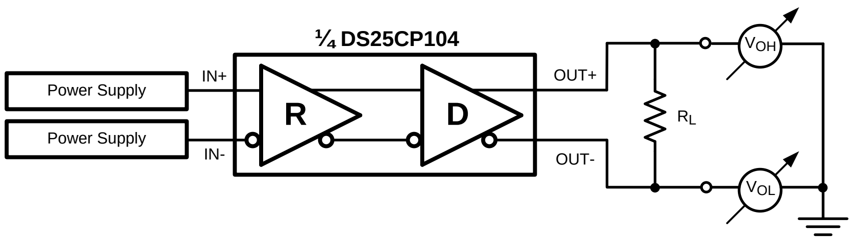
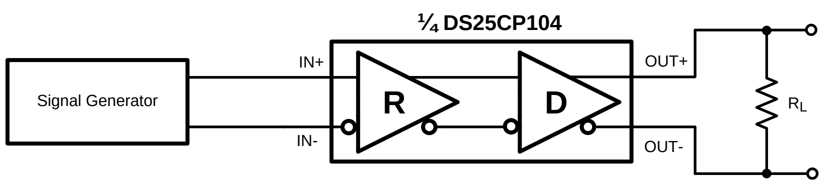


Figure 1. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams



DS25CP114 requires external 100Ω input termination.

Figure 2. Differential Driver AC Test Circuit

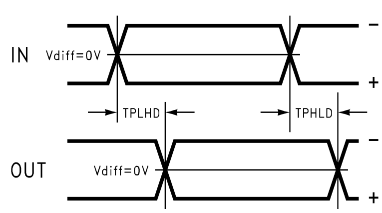


Figure 3. Propagation Delay Timing Diagram

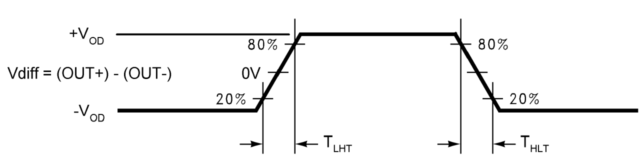
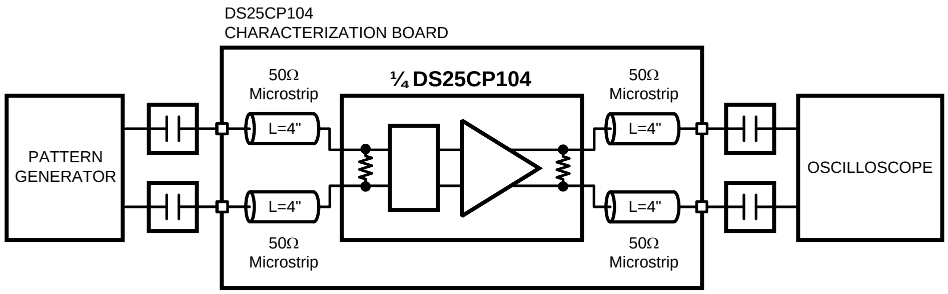


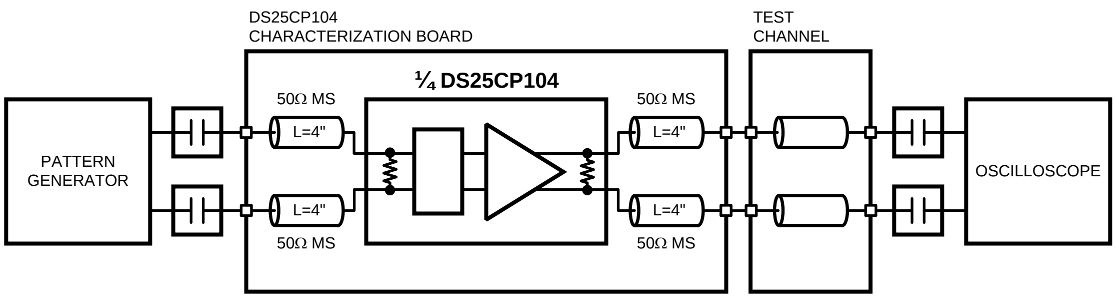
Figure 4. LVDS Output Transition Times

Pre-Emphasis and Equalization Test Circuits



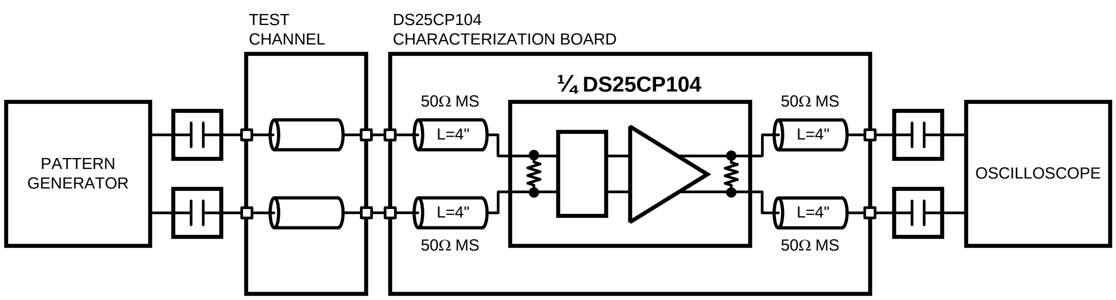
DS25CP114 requires external 100Ω input termination.

Figure 5. Jitter Performance Test Circuit



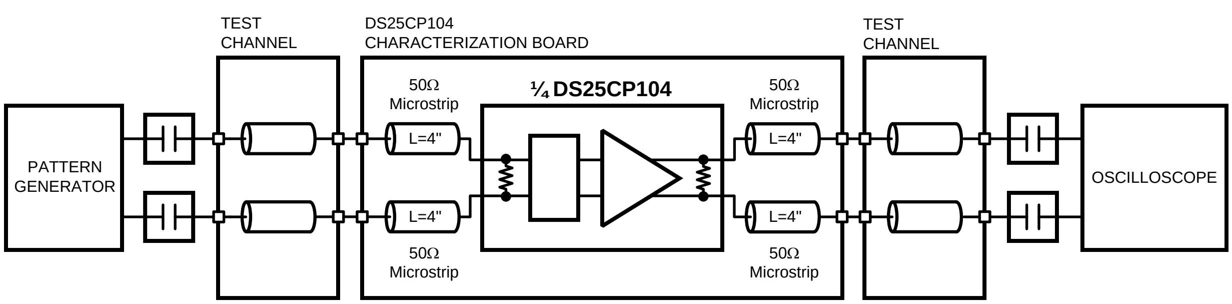
DS25CP114 requires external 100Ω input termination.

Figure 6. Pre-Emphasis Performance Test Circuit



DS25CP114 requires external 100Ω input termination.

Figure 7. Equalization Performance Test Circuit



DS25CP114 requires external 100Ω input termination.

Figure 8. Pre-Emphasis and Equalization Performance Test Circuit

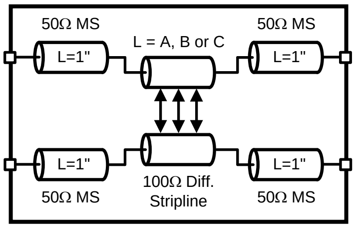


Figure 9. Test Channel Block Diagram

Test Channel Loss Characteristics

The test channel was fabricated with Polyclad PCL-FR-370-Laminate/PCL-FRP-370 Prepreg materials (Dielectric constant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.

Test Channel	Length (inches)	Insertion Loss (dB)					
		500 MHz	750 MHz	1000 MHz	1250 MHz	1500 MHz	1560 MHz
A	10	-1.2	-1.7	-2.0	-2.4	-2.7	-2.8
B	20	-2.6	-3.5	-4.1	-4.8	-5.5	-5.6
C	30	-4.3	-5.7	-7.0	-8.2	-9.4	-9.7
D	15	-1.6	-2.2	-2.7	-3.2	-3.7	-3.8
E	30	-3.4	-4.5	-5.6	-6.6	-7.7	-7.9
F	60	-7.8	-10.3	-12.4	-14.5	-16.6	-17.0

Functional Description

The DS25CP104A and DS25CP114 are 3.125 Gbps 4x4 LVDS digital crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. The DS25CP104A and DS25CP114 operate in two modes: Pin Mode (EN_smb = 0) and SMBus Mode (EN_smb = 1).

When in the Pin Mode, the switch is fully configurable with external pins. This is possible with two input select pins per output (e.g. S00 and S01 pins for OUT0). There is also one transmit pre-emphasis (PE) level select pin per output for switching the PE levels between Medium and Off settings and one receive equalization (EQ) level select pin per input for switching the EQ levels between Low and Off settings.

In the Pin Mode, feedback from the $\overline{\text{LOS}}$ (**L**oss **O**f **S**ignal) monitor circuitry is not available (there is not an $\overline{\text{LOS}}$ output pin).

When in the SMBus Mode, the full switch configuration, four levels of transmit pre-emphasis (Off, Low, Medium and High), four levels of receive equalization (Off, Low, Medium and High) and SoftPWDN can be programmed via the SMBus interface. In addition, by using the SMBus interface, a user can obtain the feedback from the built-in $\overline{\text{LOS}}$ circuitry which detects an open inputs fault condition.

In the SMBus Mode, the S00 and S01 pins become SMBus clock (SCL) input and data (SDA) input pins respectively; the S10, S11, S21 and S21 pins become the User-Set SMBus Slave Address input pins (ADDR0, 1, 2 and 3) while the S30 and S31 pins become non-functional (tieing these two pins to either H or L is recommended if the device will function only in the SMBus mode).

In the SMBus Mode, the PE and EQ select pins as well as the $\overline{\text{PWDN}}$ pin remain functional. How these pins function in each mode is explained in the following sections.

OPERATION IN PIN MODE

Power Up

In the Pin Mode, when the power is applied to the device power suppy pins, the DS25CP104A/DS25CP114 enters the Power Up mode when the PWDN pin is set to logic H. When in the Power Down mode (PWDN pin is set to logic L), all circuitry is shut down except the minimum required circuitry for the LOS and SMBus Slave operation.

Switch Configuration

In the Pin Mode, the DS25CP104A/DS25CP114 operates as a fully pin-configurable crosspoint switch. The following truth tables illustrate how the swich can be configured with external pins.

Switch Configuration Truth Tables

Table 2. Input Select Pins Configuration for the Output OUT0

S01	S00	INPUT SELECTED
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Table 3. Input Select Pins Configuration for the Output OUT1

S11	S10	INPUT SELECTED
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Table 4. Input Select Pins Configuration for the Output OUT2

S21	S20	INPUT SELECTED
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Table 5. Input Select Pins Configuration for the Output OUT3

S31	S30	INPUT SELECTED
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Setting Pre-Emphasis Levels

The DS25CP104A/DS25CP114 has one PE level select pin per output for setting the transmit pre-emphasis to either Medium or Off level. The following is the transmit pre-emphasis truth table.

Table 6. Transmit Pre-Emphasis Truth Table

OUTPUT OUTn, n = {0, 1, 2, 3}	
Pre-Emphasis Control Pin (PEn) State	**Pre-Emphasis Level**
0	Off
1	Medium

Setting Equalization Levels

The DS25CP104A/DS25CP114 has one EQ level select pin per input for setting the receive equalization to either Low or Off level. The following is the receive equalization truth table.

Table 7. Receive Equalization Truth Table

INPUT INn, n = {0, 1, 2, 3}	
Equalization Control Pin (EQn) State	**Equalization Level**
0	Off
1	Low

OPERATION IN SMBUS MODE

The DS25CP104A/DS25CP114 operates as a slave on the System Management Bus (SMBus) when the EN_smb pin is set to a high (1). Under these conditions, the SCL pin is a clock input while the SDA pin is a serial data input pin.

Device Address

Based on the SMBus 2.0 specification, the DS25CP104A/DS25CP114 has a 7-bit slave address. The three most significant bits of the slave address are hard wired inside the DS25CP104A/DS25CP114 and are “101”. The four least significant bits of the address are assigned to pins ADDR3-ADDR0 and are set by connecting these pins to GND for a low (0) or to VCC for a high (1). The complete slave address is shown in the following table:

Table 8. Slave Address

1	0	1	ADDR3	ADDR2	ADDR1	ADDR0
MSB						LSB

This slave address configuration allows up to sixteen DS25CP104A/DS25CP114 devices on a single SMBus bus.

Transfer of Data via the SMBus

During normal operation the data on SDA must be stable during the time when SCK is high.

There are three unique states for the SMBus:

START: A HIGH to LOW transition on SDA while SCK is high indicates a message START condition.

STOP: A LOW to HIGH transition on SDA while SCK is high indicates a message STOP condition.

IDLE: If SCK and SDA are both high for a time exceeding tBUF from the last detected STOP condition or if they are high for a total exceeding the maximum specification for tHIGH then the bus will transfer to the IDLE state.

SMBus Transactions

A transaction begins with the host placing the DS25CP104A SMBus into the START condition, then a byte (8 bits) is transferred, MSB first, followed by a ninth ACK bit. ACK bits are ‘0’ to signify an ACK, or ‘1’ to signify NACK, after this the host holds the SCL line low, and waits for the receiver to raise the SDA line as an ACKnowledge that the byte has been received.

Writing to a Register

To write a register, the following protocol is used (see SMBus 2.0 specification):

1) The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.

2) The Device (Slave) drives an ACK bit (“0”).

3) The Host drives the 8-bit Register Address.

4) The Device drives an ACK bit (“0”).

5) The Host drives the 8-bit data byte.

6) The Device drives an ACK bit “0”.

7) The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes Idle and communication with other SMBus devices may now occur.

Reading From a Register

To read a register, the following protocol is used (see SMBus 2.0 specification):

1) The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.

2) The Device (Slave) drives an ACK bit (“0”).

3) The Host drives the 8-bit Register Address.

4) The Device drives an ACK bit (“0”).

5) The Host drives a START condition.

6) The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.

7) The Device drives an ACK bit “0”.

8) The Device drives the 8-bit data value (register contents).

9) The Host drives a NACK bit “1” indicating end of READ transfer.

10) The Host drives a STOP condition.

The READ transaction is completed, the bus goes Idle and communication with other SMBus devices may now occur.

Register Descriptions

There are five data registers in the DS25CP104A/DS25CP114 accessible via the SMBus interface.

Table 9. SMBus Data Registers

Address (hex)	Name	Access	Description
0	Switch Configuration	R/W	Switch Configuration Register
1	PE Level Select	R/W	Transmit Pre-emphasis Level Select Register
2	EQ Level Select	R/W	Receive Equalization Level Select Register
3	Control	R/W	Powerdown, $\overline{\text{LOS}}$ Enable and Pin Control Register

Table 9. SMBus Data Registers (continued)

Address (hex)	Name	Access	Description
4	$\overline{\text{LOS}}$	RO	**L**oss **O**f **S**ignal ($\overline{\text{LOS}}$) Reporting Register

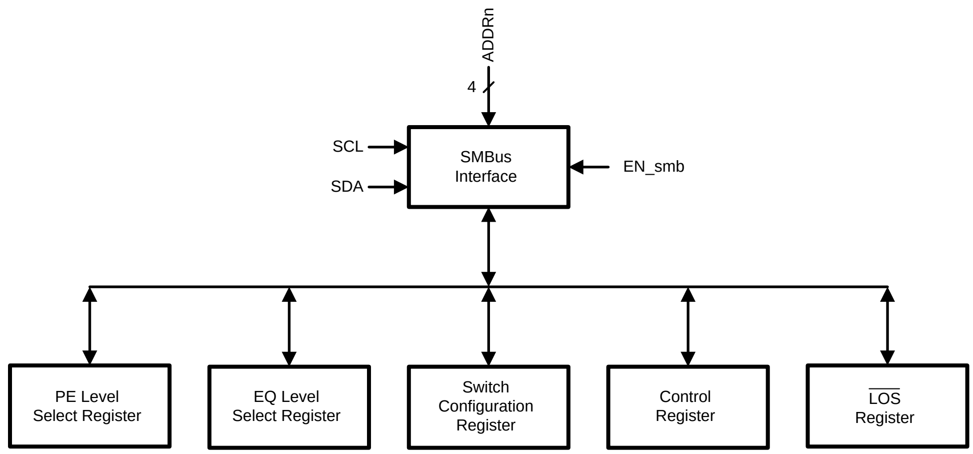


Figure 10. Registers Block Diagram

SWITCH CONFIGURATION REGISTER

The Switch Configuration register is utilized to configure the switch. The following two tables show the Switch Configuration Register mapping and associated truth table.

Switch Configuration Register Mapping

Bit	Default	Bit Name	Access	Description
D[1:0]	00	Input Select 0	R/W	Selects which input is routed to the OUT0.
D[3:2]	00	Input Select 1	R/W	Selects which input is routed to the OUT1.
D[5:4]	00	Input Select 2	R/W	Selects which input is routed to the OUT2.
D[7:6]	00	Input Select 3	R/W	Selects which input is routed to the OUT3.

Switch Configuration Register Truth Table

D1	D0	Input Routed to the OUT0
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

The switch configuration logic has a SmartPWDN circuitry which automatically optimizes the device's power consumption based on the switch configuration (i.e. It places unused I/O blocks and other unused circuitry in the power down state).

PE LEVEL SELECT REGISTER

The PE Level Select register selects the pre-emphasis level for each of the outputs. The following two tables show the register mapping and associated truth table.

PE Level Select Register Table

Bit	Default	Bit Name	Access	Description
D[1:0]	00	PE Level Select 0	R/W	Sets pre-emphasis level on the OUT0.

PE Level Select Register Table (continued)

Bit	Default	Bit Name	Access	Description
D[3:2]	00	PE Level Select 1	R/W	Sets pre-emphasis level on the OUT1.
D[5:4]	00	PE Level Select 2	R/W	Sets pre-emphasis level on the OUT2.
D[7:6]	00	PE Level Select 3	R/W	Sets pre-emphasis level on the OUT3.

PE Level Select Register Truth Table

D1	D0	Pre-Emphasis Level for the OUT0
0	0	Off
0	1	Low
1	0	Medium
1	1	High

EQ LEVEL SELECT REGISTER

The EQ Level Select register selects the equalization level for each of the inputs. The following two tables show the register mapping and associated truth table.

Bit	Default	Bit Name	Access	Description
D[1:0]	00	EQ Level Select 0	R/W	Sets equalization level on the IN0.
D[3:2]	00	EQ Level Select 1	R/W	Sets equalization level on the IN1.
D[5:4]	00	EQ Level Select 2	R/W	Sets equalization level on the IN2.
D[7:6]	00	EQ Level Select 3	R/W	Sets equalization level on the IN3.

Table 10. EQ Level Select Register Truth Table

D1	D0	Equalization Level for the IN0
0	0	Off
0	1	Low
1	0	Medium
1	1	High

CONTROL REGISTER

The Control register enables $\overline{\text{SoftPWDN}}$ control, individual output power down ($\overline{\text{PWDNn}}$) control, $\overline{\text{LOS}}$ Circuitry Enable control, PE Level Select Enable control and EQ Level Select Enable control via the SMBus. The following table shows the register mapping.

Table 11. Register Mapping Table

Bit	Default	Bit Name	Access	Description
D[3:0]	1111	$\overline{\text{PWDNn}}$	R/W	Writing a [0] to the bit D[n] will power down the output OUTn when either the $\overline{\text{PWDN}}$ pin OR the Control Register bit D[7] ($\overline{\text{SoftPWDN}}$) is set to a high [1].
D[4]	0	Ignore_External_EQ	R/W	Writing a [1] to the bit D[4] will ignore the state of the external EQ pins and will allow setting the EQ levels via the SMBus interface.
D[5]	0	Ignore_External_PE	R/W	Writing a [1] to the bit D[5] will ignore the state of the external PE pins and will allow setting the PE levels via the SMBus interface.
D[6]	0	EN_$\overline{\text{LOS}}$	R/W	Writing a [1] to the bit D[6] will enable the $\overline{\text{LOS}}$ circuitry and receivers on all four inputs. The SmartPWDN circuitry will not disable any of the inputs nor any supporting $\overline{\text{LOS}}$ circuitry depending on the switch configuration.

Table 11. Register Mapping Table (continued)

Bit	Default	Bit Name	Access	Description
D[7]	0	$\overline{\text{SoftPWDN}}$	R/W	Writing a [0] to the bit D[7] will place the device into the power down mode. This pin is ORed together with the $\overline{\text{PWDN}}$ pin.

Table 12. Power Modes Truth Table

$\overline{\text{PWDN}}$	$\overline{\text{SoftPWDN}}$	$\overline{\text{PWDNn}}$	Power Mode
0	0	x	Power Down Mode. In this mode, all circuitry is shut down except the minimum required circuitry for the $\overline{\text{LOS}}$ and SMBus Slave operation. The SMBus circuitry allows enabling the $\overline{\text{LOS}}$ circuitry and receivers on all inputs in this mode by setting the EN_$\overline{\text{LOS}}$ bit to a [1].
0 1 1	1 0 1	x x x	Power Up Mode. In this mode, the SmartPWDN circuitry will automatically power down any unused I/O and logic blocks and other supporting circuitry depending on the switch configuration. An output will be enabled **only** when the SmartPWDN circuitry indicates that that particular output is needed for the particular switch configuration **and** the respective $\overline{\text{PWDNn}}$ bit has logic high [1]. An input will be enabled when the SmartPWDN circuitry indicates that that particular input is needed for the particular switch configuration **or** the EN_$\overline{\text{LOS}}$ bit is set to a [1].

$\overline{\text{LOS}}$ REGISTER

The $\overline{\text{LOS}}$ register reports an open inputs fault condition for each of the inputs. The following table shows the register mapping.

Bit	Default	Bit Name	Access	Description
D[0]	0	$\overline{\text{LOS0}}$	RO	Reading a [0] from the bit D[0] indicates an open inputs fault condition on the IN0. A [1] indicates presence of a valid signal.
D[1]	0	$\overline{\text{LOS1}}$	RO	Reading a [0] from the bit D[1] indicates an open inputs fault condition on the IN1. A [1] indicates presence of a valid signal.
D[2]	0	$\overline{\text{LOS2}}$	RO	Reading a [0] from the bit D[2] indicates an open inputs fault condition on the IN2. A [1] indicates presence of a valid signal.
D[3]	0	$\overline{\text{LOS3}}$	RO	Reading a [0] from the bit D[3] indicates an open inputs fault condition on the IN3. A [1] indicates presence of a valid signal.
D[7:4]	0000	Reserved	RO	Reserved for future use. Returns undefined value when read.

INPUT INTERFACING

The DS25CP104A/DS25CP114 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25CP104A/DS25CP114 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers.

The DS25CP104A inputs are internally terminated with a 100Ω resistor for optimal device performance, reduced component count, and minimum board space. External input terminations on the DS25CP114 need to be placed as close as possible to the device inputs to achieve equivalent AC performance. When all four inputs are utilized it may be necessary to alternate between the top and bottom layers to achieve the minimum device input to termination distance. It is recommended that SMT resistors sized 0402 or smaller be used and the mounting distance to the DS25CP114 pins kept under 200 mils.

When using the DS25CP114 in a limited multi-drop topology, any transmission line stubs should be kept very short to minimize any negative effects on signal quality. A single termination resistor or resistor network that matches the differential line impedance should be used. If DS25CP114 input pairs from two separate devices are to be connected to a single differential output, it is recommended that the DS25CP114 devices are mounted directly opposite of each other. One on top of the PCB and the other directly under the first on the bottom of the PCB, this keeps the distance between inputs equal to the PCB thickness.

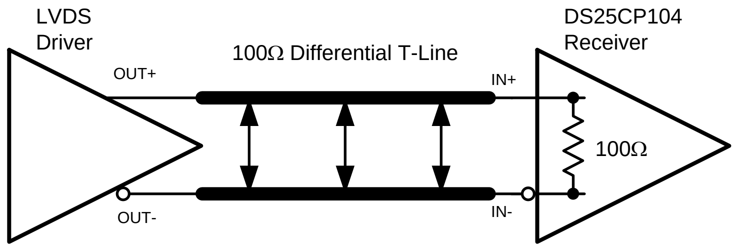


Figure 11. Typical LVDS Driver DC-Coupled Interface to DS25CP104A Input

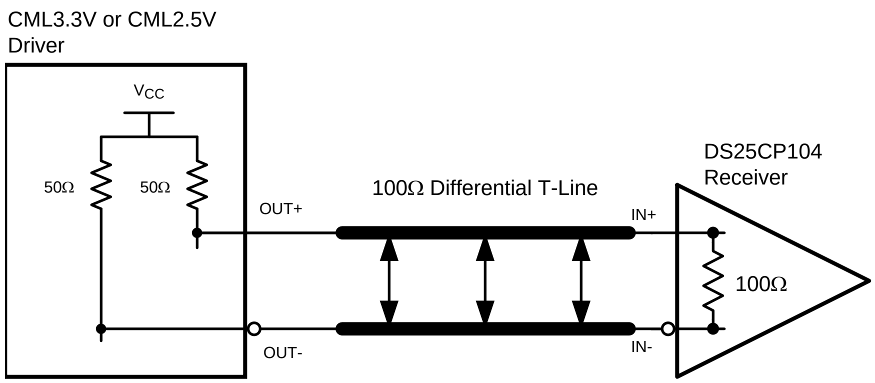
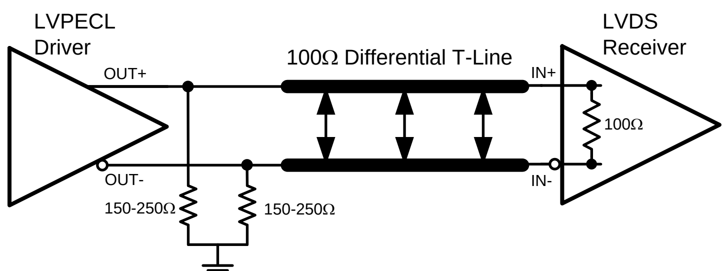


Figure 12. Typical CML Driver DC-Coupled Interface to DS25CP104A Input



DS25CP114 requires external 100Ω input termination.

Figure 13. Typical LVPECL Driver DC-Coupled Interface to DS25CP104A Input

OUTPUT INTERFACING

The DS25CP104A/DS25CP114 outputs signals that are compliant to the LVDS standard. Its outputs can be DC-coupled to most common differential receivers. The following figure illustrates a typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check the respective receiver's data sheet prior to implementing the suggested interface implementation.

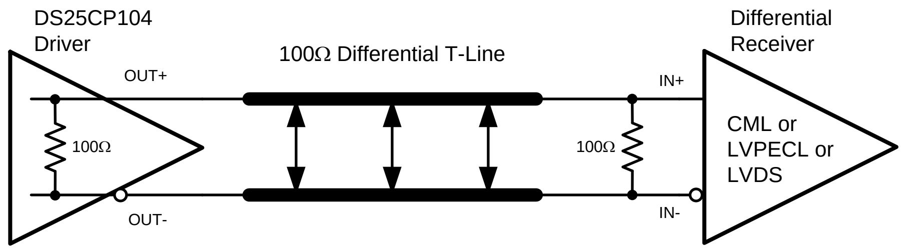


Figure 14. Typical Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance Characteristics

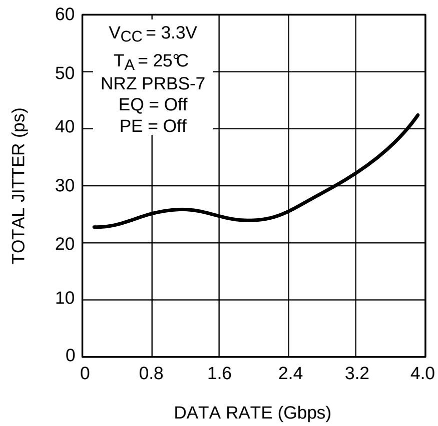


Figure 15. Total Jitter as a Function of Data Rate

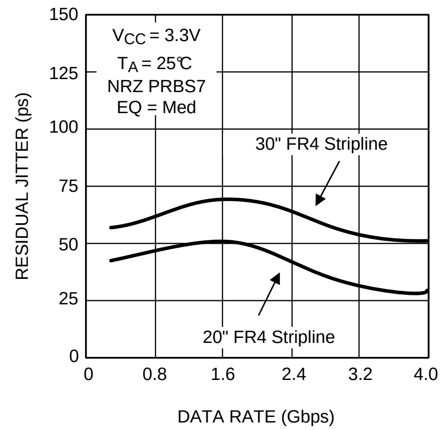


Figure 16. Residual Jitter as a Function of Data Rate, FR4 Stripline Length and EQ Level

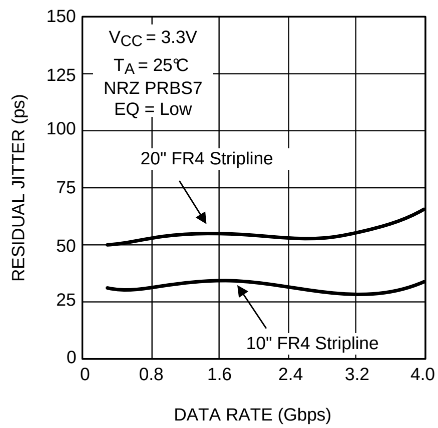


Figure 17. Residual Jitter as a Function of Data Rate, FR4 Stripline Length and EQ Level

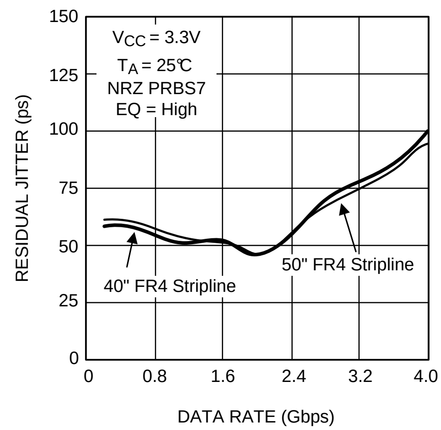


Figure 18. Residual Jitter as a Function of Data Rate, FR4 Stripline Length and EQ Level

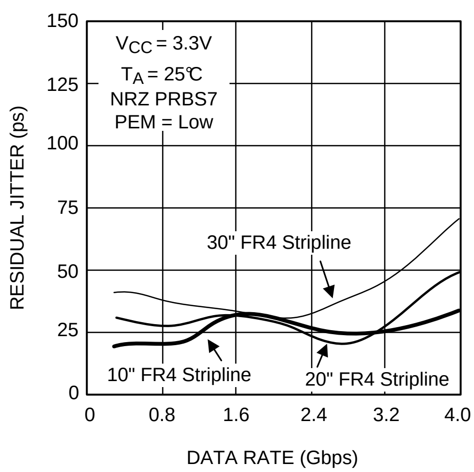


Figure 19. Residual Jitter as a Function of Data Rate, FR4 Stripline Length and PE Level

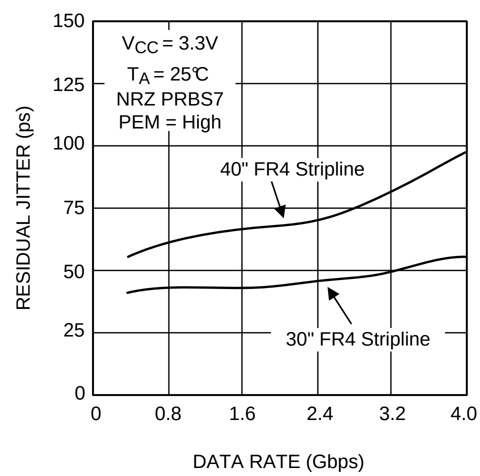


Figure 20. Residual Jitter as a Function of Data Rate, FR4 Stripline Length and PE Level

Typical Performance Characteristics (continued)

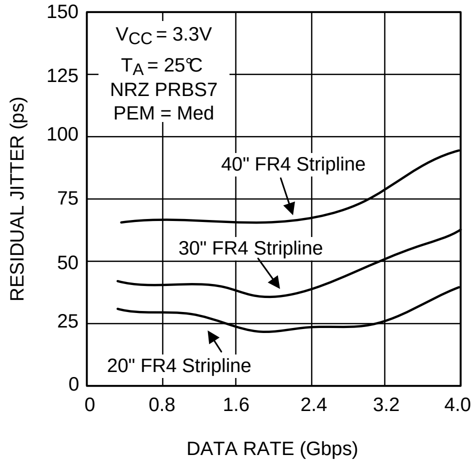


Figure 21. Residual Jitter as a Function of Data Rate, FR4 Stripline Length and PE Level

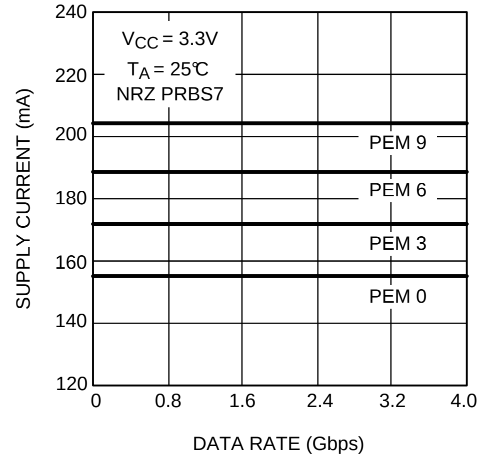


Figure 22. Supply Current as a Function of Data Rate and PE Level

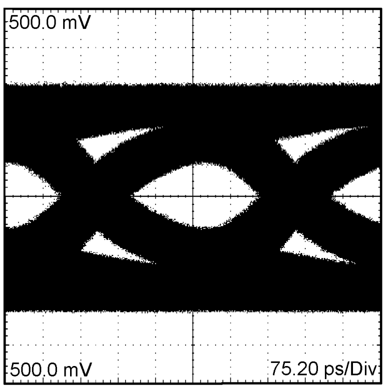


Figure 23. A 2.5 Gbps NRZ PRBS-23 without PE After 30" Differential FR-4 Stripline H: 75 ps / DIV, V: 100 mV / DIV

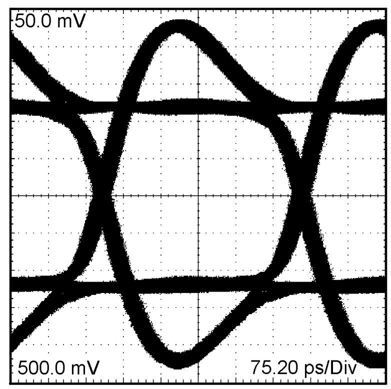


Figure 24. A 2.5 Gbps NRZ PRBS-23 with High PE After 2" Differential FR-4 Microstrip H: 75 ps / DIV, V: 100 mV / DIV

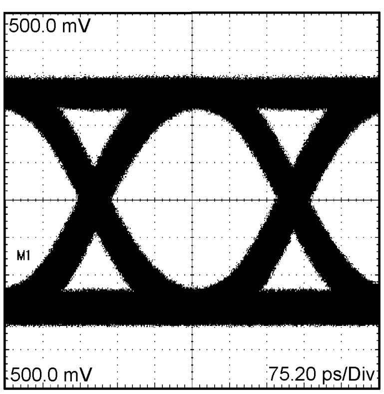


Figure 25. A 2.5 Gbps NRZ PRBS-23 with High PE After 30" Differential FR-4 Stripline H: 75 ps / DIV, V: 100 mV / DIV

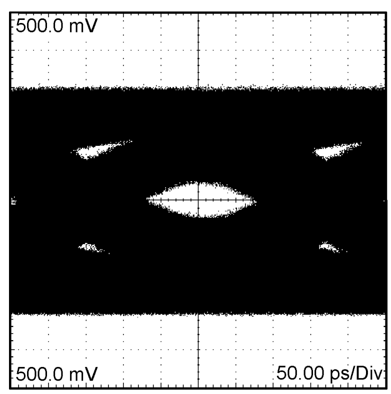


Figure 26. A 3.125 Gbps NRZ PRBS-23 without PE After 30" Differential FR-4 Stripline H: 50 ps / DIV, V: 100 mV / DIV

Typical Performance Characteristics (continued)

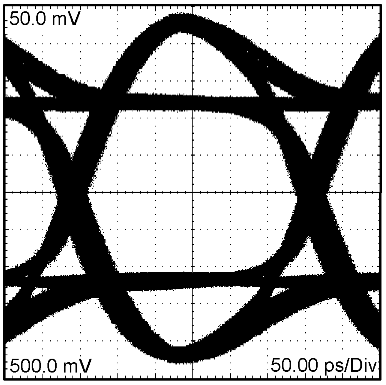


Figure 27. A 3.125 Gbps NRZ PRBS-23 with High PE After 2" Differential FR-4 Microstrip H: 50 ps / DIV, V: 100 mV / DIV

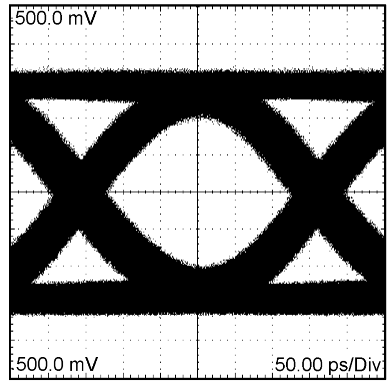


Figure 28. A 3.125 Gbps NRZ PRBS-23 with High PE After 30" Differential FR-4 Stripline H: 50 ps / DIV, V: 100 mV / DIV

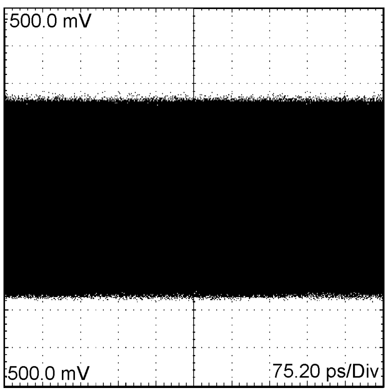


Figure 29. A 2.5 Gbps NRZ PRBS-23 without EQ After 60" Differential FR-4 Stripline H: 75 ps / DIV, V: 100 mV / DIV

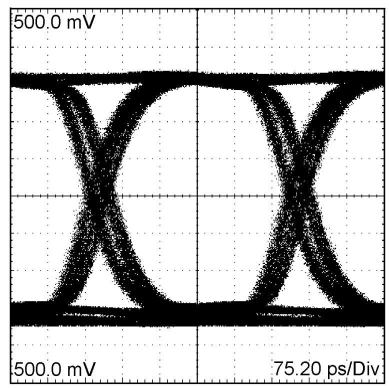


Figure 30. A 2.5 Gbps NRZ PRBS-23 with High EQ After 60" Differential FR-4 Stripline H: 75 ps / DIV, V: 100 mV / DIV

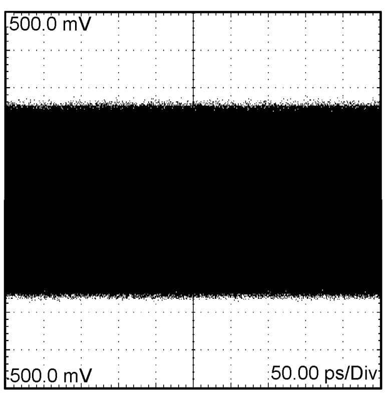


Figure 31. A 3.125 Gbps NRZ PRBS-23 without EQ After 60" Differential FR-4 Stripline H: 50 ps / DIV, V: 100 mV / DIV

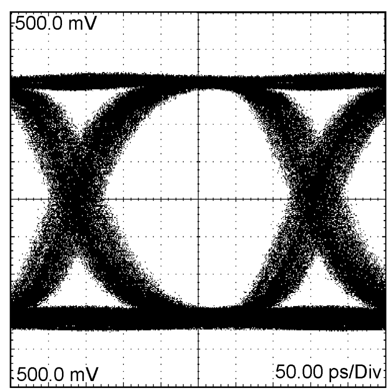


Figure 32. A 3.125 Gbps NRZ PRBS-23 with High EQ After 60" Differential FR-4 Stripline H: 50 ps / DIV, V: 100 mV / DIV

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	22

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS25CP104ATSQ/NOPB	ACTIVE	WQFN	RTA	40	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	2CP104AS	Samples
DS25CP104ATSQX/NOPB	ACTIVE	WQFN	RTA	40	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	2CP104AS	Samples
DS25CP114TSQ/NOPB	ACTIVE	WQFN	RTA	40	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	2CP114SQ	Samples
DS25CP114TSQE/NOPB	ACTIVE	WQFN	RTA	40	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	2CP114SQ	Samples
DS25CP114TSQX/NOPB	ACTIVE	WQFN	RTA	40	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	2CP114SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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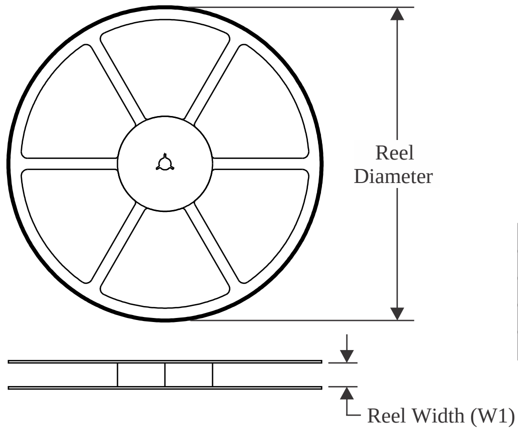
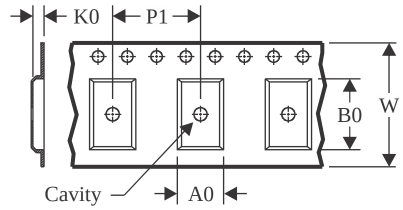
TAPE AND REEL INFORMATION

REEL DIMENSIONS

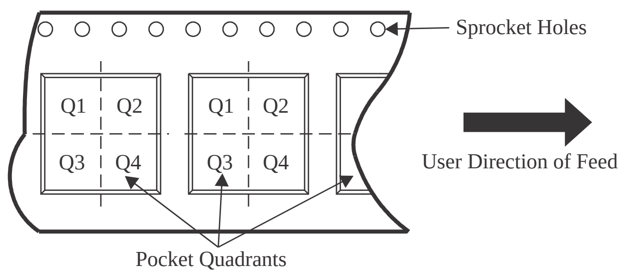


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

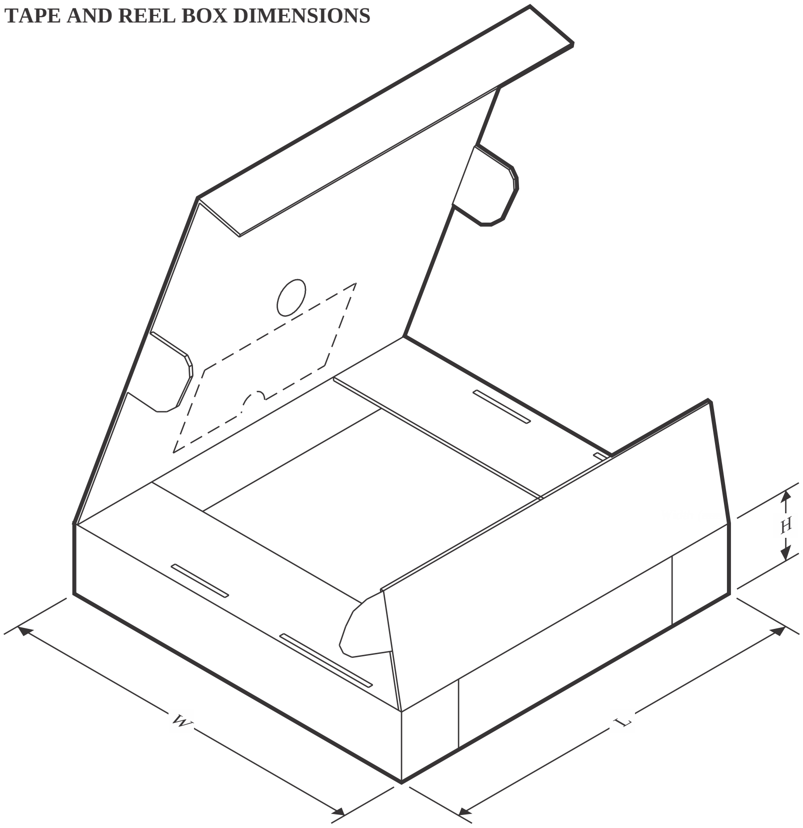
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

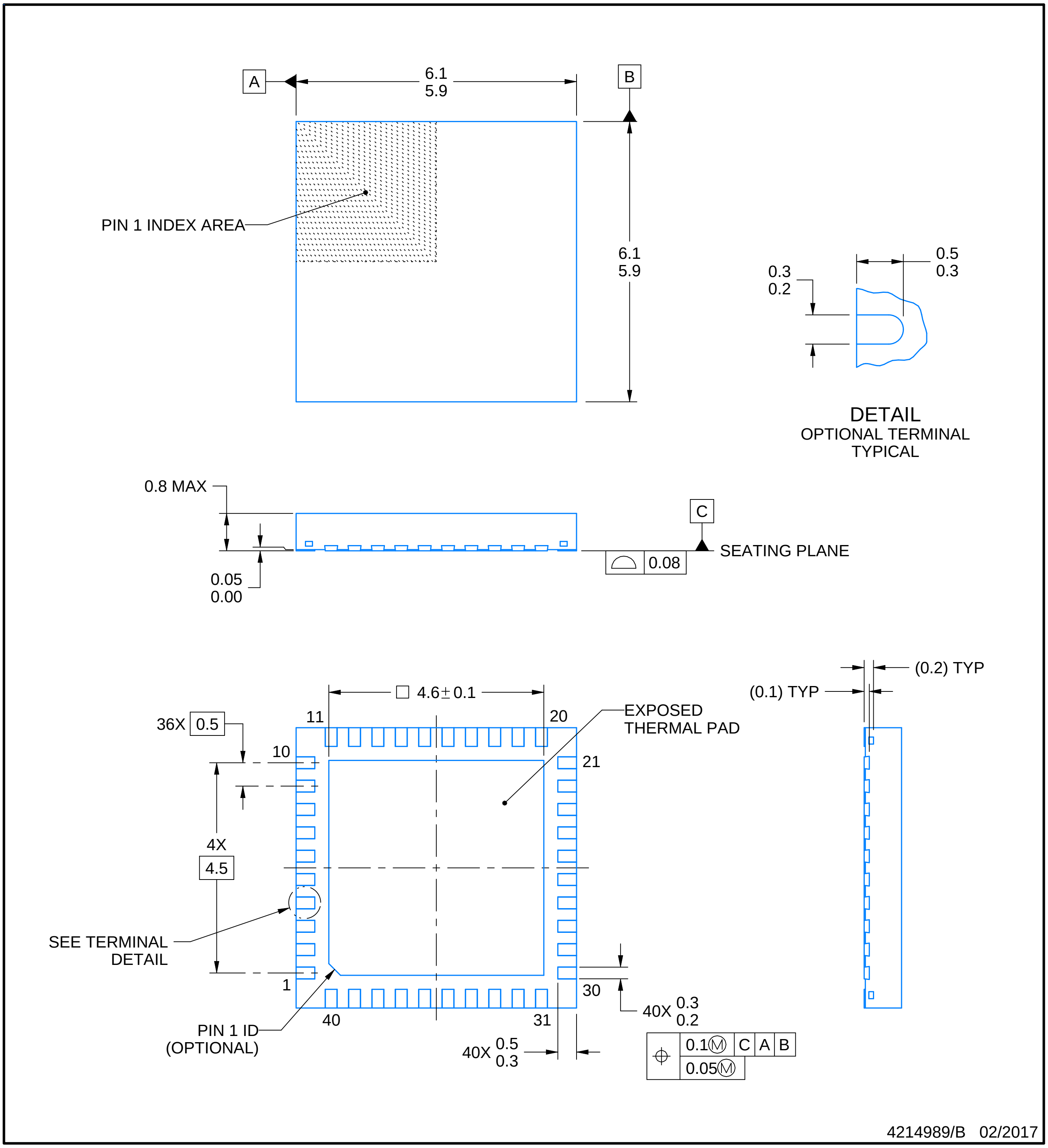
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS25CP104ATSQ/NOPB	WQFN	RTA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS25CP104ATSQX/ NOPB	WQFN	RTA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS25CP114TSQ/NOPB	WQFN	RTA	40	1000	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS25CP114TSQE/NOPB	WQFN	RTA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS25CP114TSQX/NOPB	WQFN	RTA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



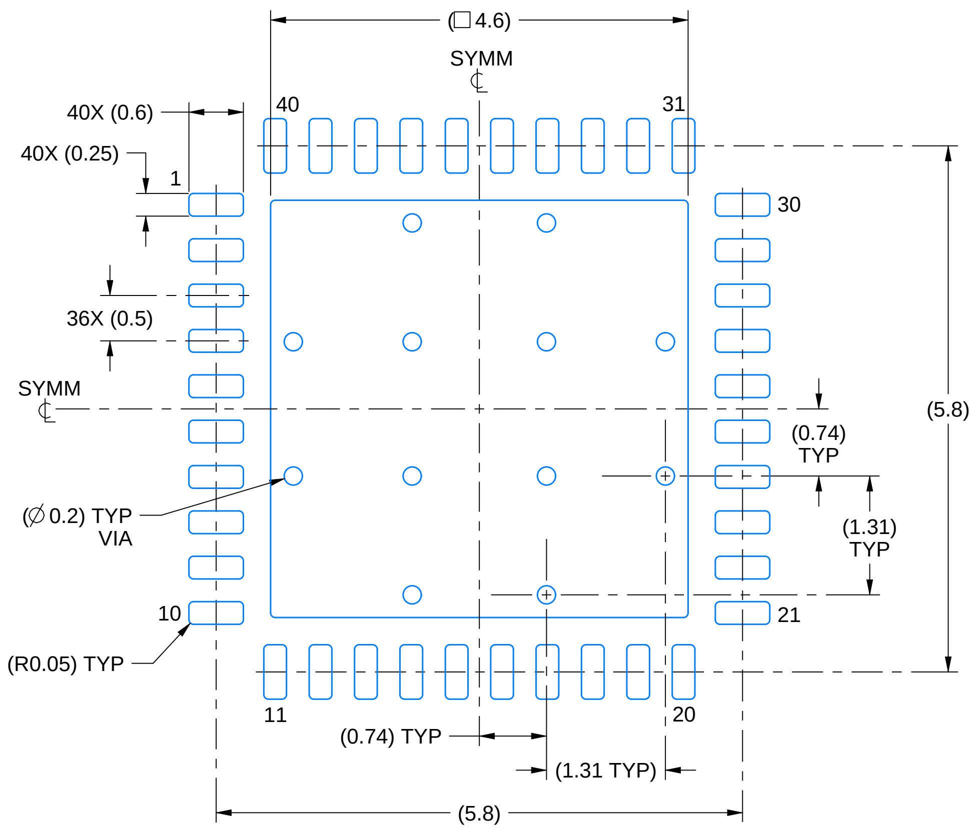
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS25CP104ATSQ/NOPB	WQFN	RTA	40	250	208.0	191.0	35.0
DS25CP104ATSQX/NOPB	WQFN	RTA	40	2500	356.0	356.0	35.0
DS25CP114TSQ/NOPB	WQFN	RTA	40	1000	356.0	356.0	35.0
DS25CP114TSQE/NOPB	WQFN	RTA	40	250	208.0	191.0	35.0
DS25CP114TSQX/NOPB	WQFN	RTA	40	2500	356.0	356.0	35.0

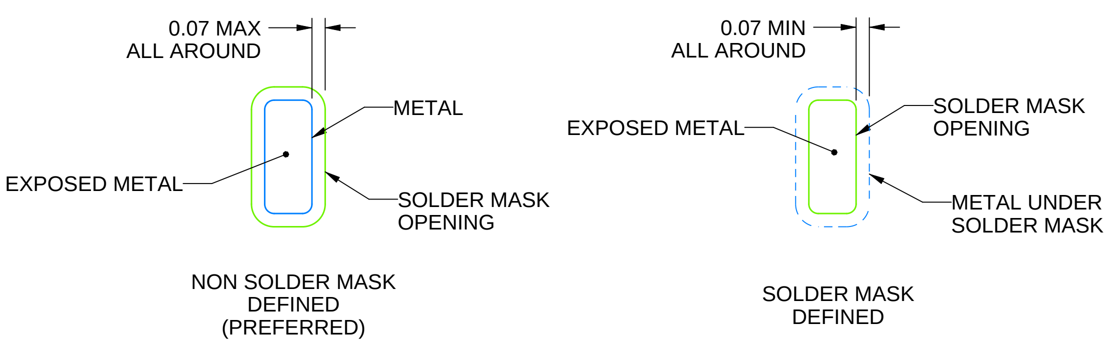


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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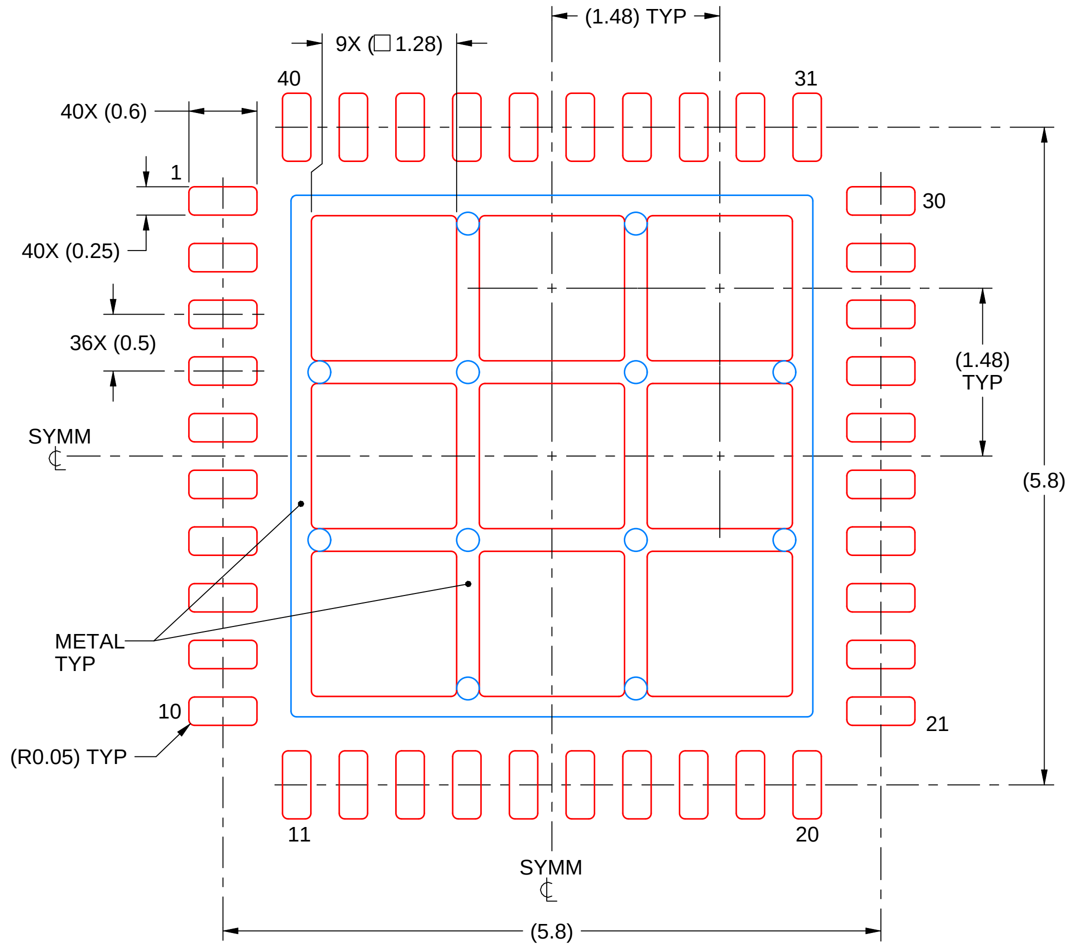
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.