DS320PR1601 32Gbps 16 通道 PCIe® 5.0、CXL 2.0 线性转接驱动器

1 特性

- 支持 PCIe® 5.0、CXL 2.0、CCIX 和 UPI 2.0 的 16 通道线性转接驱动器
- 支持高达 32Gbps 的数据速率
- 与 Intel 重定时器通用封装兼容
- 封装内 Tx 引脚上有 64 个集成交流耦合电容器，可节省布板空间
- CTLE 在 16GHz 时提升 21dB
- 130 ps 的超低延迟
- PRBS 数据的 50fs 低附加随机抖动
- 3.3V 单电源
- 164mW/通道的低有功功率
- I²C/SMBus 或 EEPROM 编程
- 针对 PCIe 用例的自动接收器检测
- 无缝支持 PCIe 链路训练
- 内部稳压器具有抗电源噪声能力
- 支持 x4、x8、x16 总线宽度
- 8.90mm × 22.80mm BGA 封装

2 应用

- 机架式服务器、微服务器和塔式服务器
- 高性能计算
- 硬件加速器
- 网络连接存储
- 存储区域网络 (SAN) 和主机总线适配器 (HBA) 卡
- 网络接口卡 (NIC)
- 台式计算机或主板

3 说明

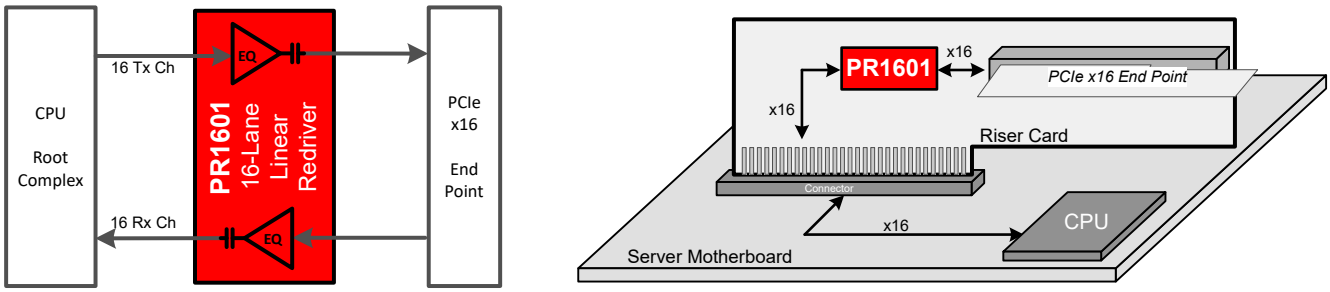
DS320PR1601 是一款 32 通道（每个方向 16 通道）或 x16（16 通道）低功耗高性能线性中继器或转接驱动器，设计用于支持 PCIe 5.0、CXL 2.0、UPI 2.0 和其他接口，最高可支持 32Gbps 的传输速率。

DS320PR1601 接收器部署了连续时间线性均衡器 (CTLE)，用以提供可编程高频增强功能。均衡器可以打开由于 PCB 布线等互连介质引起的码间串扰 (ISI) 而完全关闭的输入眼图。CTLE 接收器后跟一个线性输出驱动器。DS320PR1601 的线性数据路径保留了发射预设信号特性。线性转接驱动器成为无源通道的一部分，该通道作为一个整体进行链路训练，可获得更优发送和接收均衡设置。对这种链路训练协议进行透明管理可实现更优的电气链路和尽可能低的延迟。该器件具有低通道间串扰、低附加抖动和超低的回波损耗，因此在链路中几乎可用作无源元件，而又具有均衡功能。

封装信息

器件型号	封装(1)	封装尺寸(2)
DS320PR1601	ZDG（nfBGA、354）	22.89 mm × 8.9 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



典型应用

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4 Revision History

DATE	REVISION	NOTES
June 2023	*	Initial Release

5 Pin Configuration and Functions

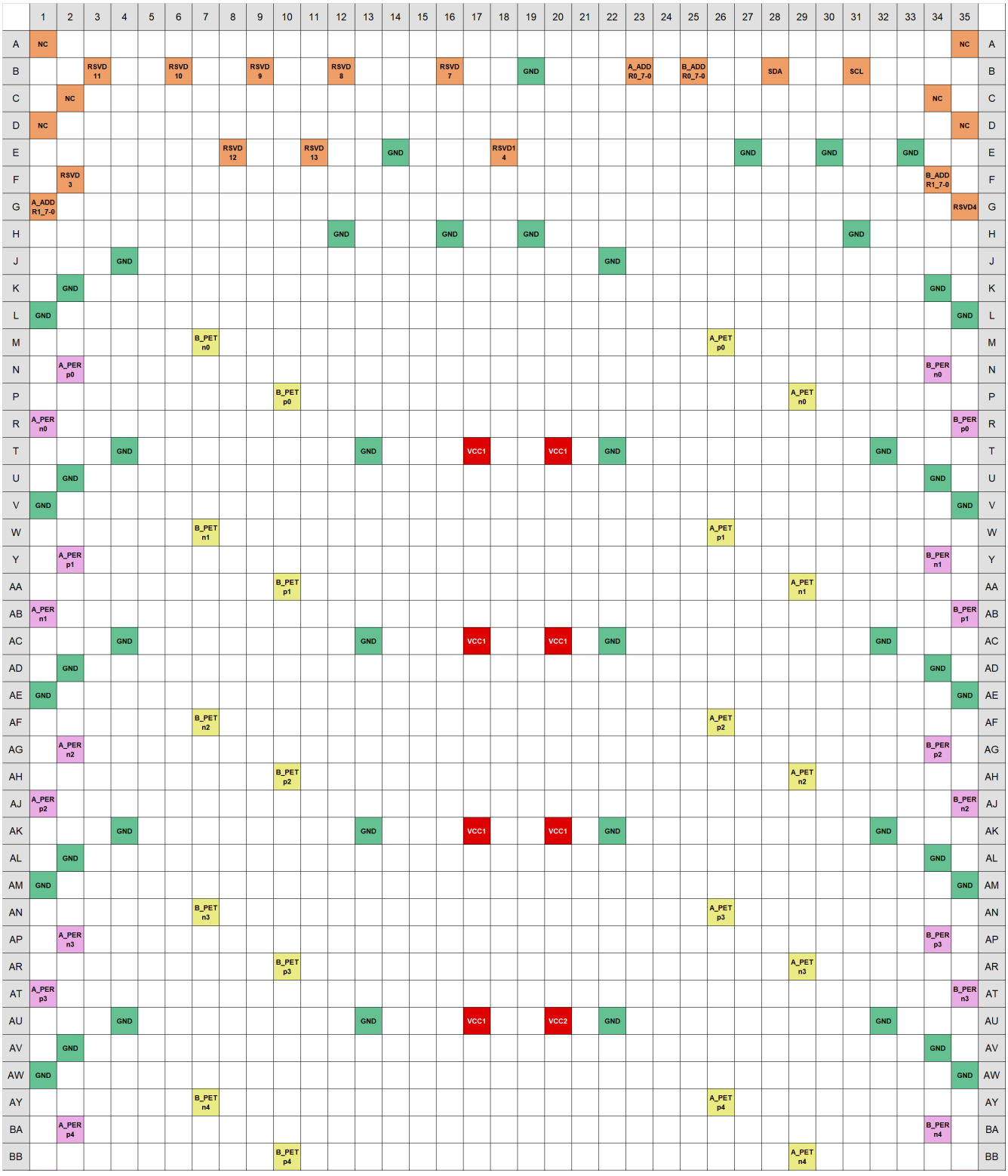


图 5-1. ZDG Package, 354-Pin BGA (Top View 1/3)

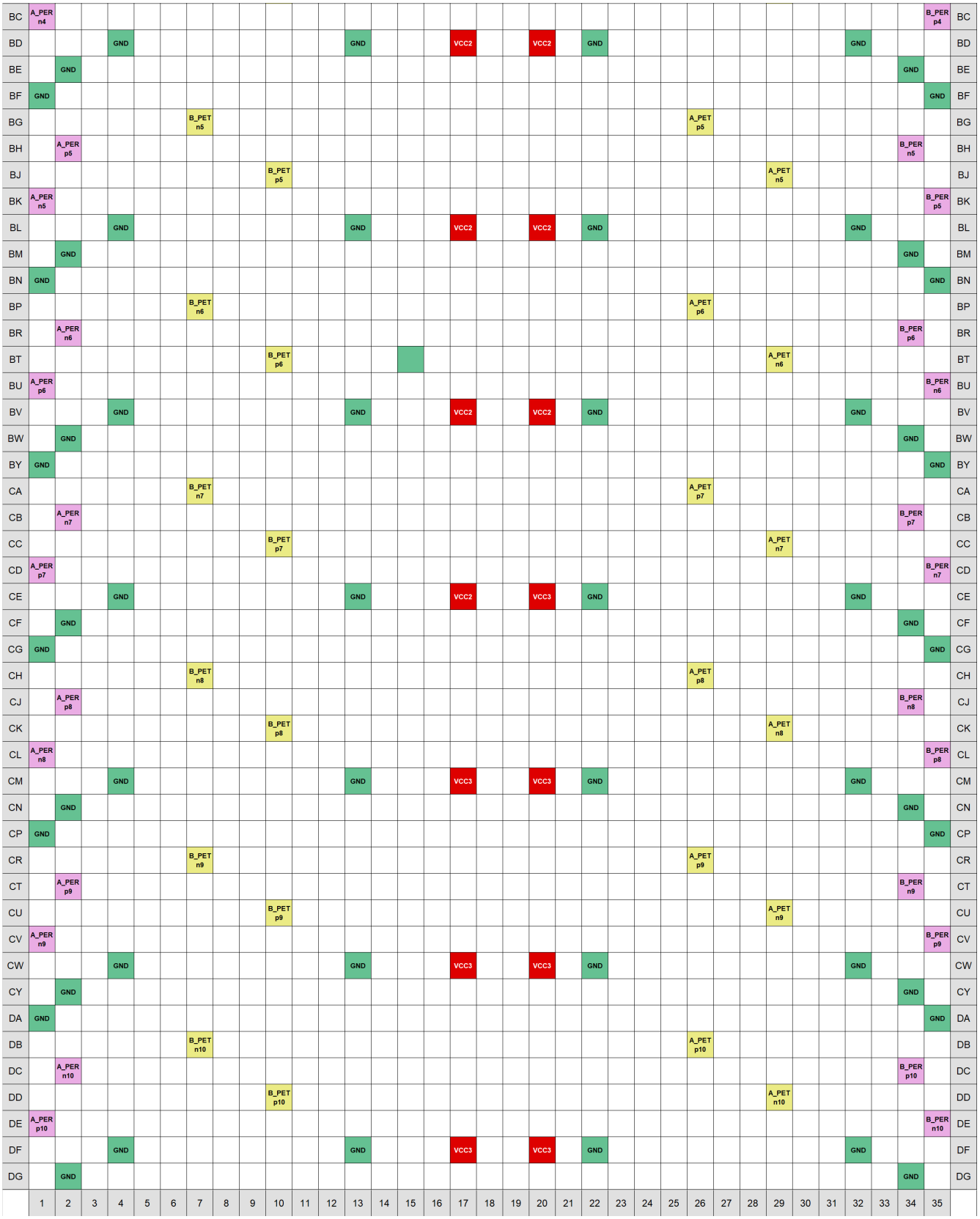


图 5-2. ZDG Package, 354-Pin BGA (Top View 2/3)

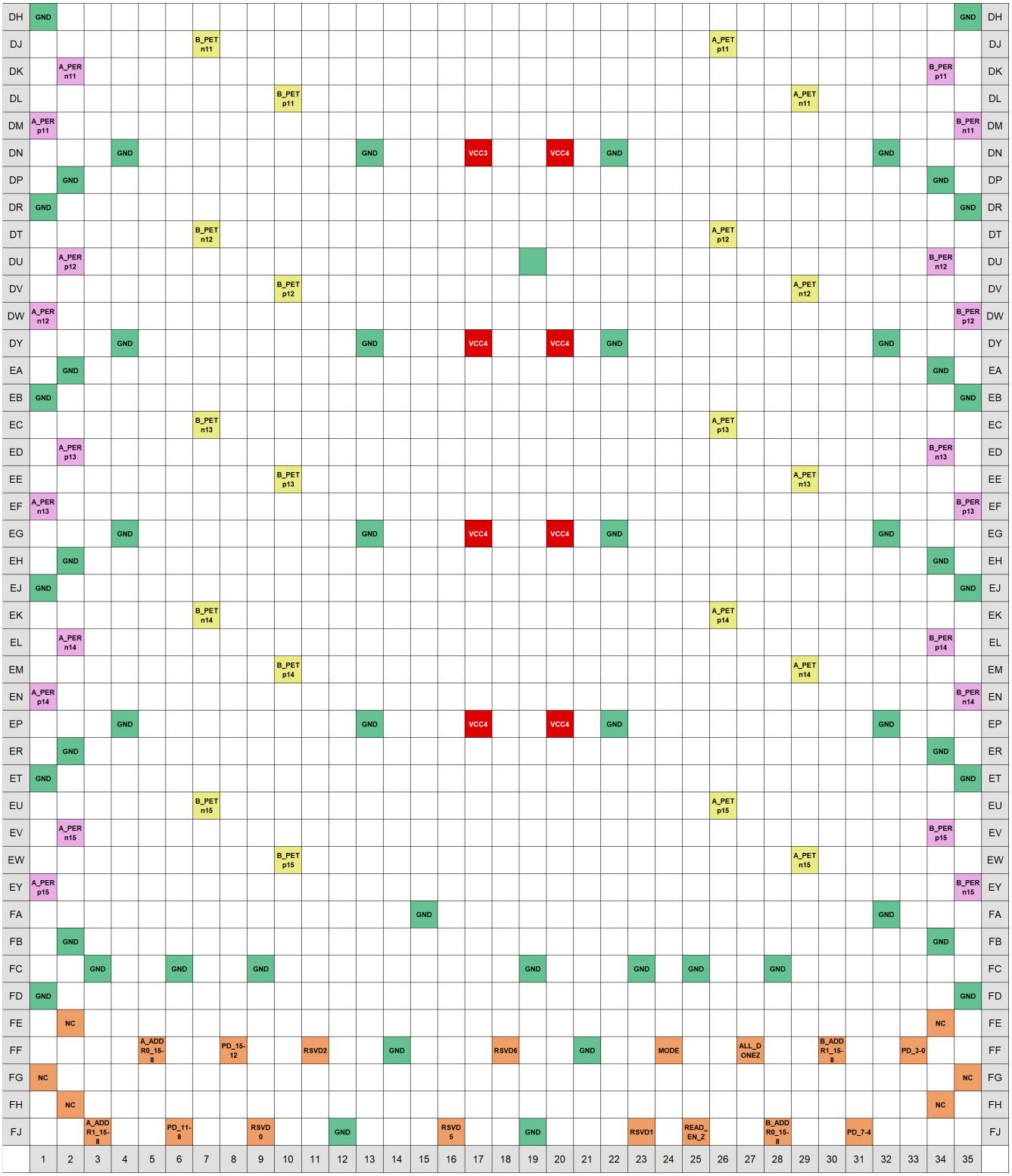


图 5-3. ZDG Package 354-Pin BGA Top View 3/3

Legend				
Ground	Power	IOs, RSVD /NC	Differential Input	Differential Output

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	N/C	—	No internal connection.
A35	N/C	—	No internal connection.
B12	RSVD8	—	Reserved for future use. No internal connection.
B16	RSVD7	—	Reserved for future use. No internal connection.
B19	GND	Ground	Ground
B23	A_ADDR0_7-0	Input	5-level input strap pins, as provided in 表 7-3. Sets SMBus/I^{2}C target address, as provided in 表 8-1 and 表 8-2.
B25	B_ADDR0_7-0	Input	5-level input strap pins, as provided in 表 7-3. Sets SMBus/I^{2}C target address, as provided in 表 8-1 and 表 8-2.
B28	SDA	Input / Output	3.3 V SMBus/I^{2}C data IO pin SDA. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus / I^{2}C interface standard. The device can alter between SMBus/I^{2}C controller and target mode through exercising MODE pin.
B3	RSVD11	—	Reserved for future use. No internal connection.
B31	SCL	Input / Output	3.3 V SMBus/I^{2}C clock IO pin SCL. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus / I^{2}C interface standard. The device can alter between SMBus/I^{2}C controller and target mode through exercising MODE pin.
B6	RSVD10	—	Reserved for future use. No internal connection.
B9	RSVD9	—	Reserved for future use. No internal connection.
C2	N/C	—	No internal connection.
C34	N/C	—	No internal connection.
D1	N/C	—	No internal connection.
D35	N/C	—	No internal connection.
E11	RSVD13	—	Reserved for future use. No internal connection.
E14	GND	Ground	Ground
E18	RSVD14	—	Reserved for future use. No internal connection.
E27	GND	Ground	Ground
E30	GND	Ground	Ground
E33	GND	Ground	Ground
E8	RSVD12	—	Reserved for future use. No internal connection.
F2	RSVD3	—	Reserved for future use. No internal connection.
F34	B_ADDR1_7-0	Input	5-level input strap pins, as provided in 表 7-3. Sets SMBus/I^{2}C target address, as provided in 表 8-1 and 表 8-2.
G1	A_ADDR1_7-0	Input	5-level input strap pins, as provided 表 7-3. Sets SMBus/I^{2}C target address, as provided in 表 8-1 and 表 8-2.
G35	RSVD4	—	Reserved for future use. No internal connection.
H12	GND	Ground	Ground
H16	GND	Ground	Ground
H19	GND	Ground	Ground
H31	GND	Ground	Ground
J22	GND	Ground	Ground
J4	GND	Ground	Ground
K2	GND	Ground	Ground
K34	GND	Ground	Ground
L1	GND	Ground	Ground
L35	GND	Ground	Ground
M26	A_PETp0	Diff Output	Differential transmit signal, side A, channel 0, positive

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
M7	B_PETn0	Diff Output	Differential transmit signal, side B, channel 0, negative
N2	A_PERp0	Diff Input	Differential receive signal, side A, channel 0, positive
N34	B_PERn0	Diff Input	Differential receive signal, side B, channel 0, negative
P10	B_PETp0	Diff Output	Differential transmit signal, side B, channel 0, positive
P29	A_PETn0	Diff Output	Differential transmit signal, side A, channel 0, negative
R1	A_PERn0	Diff Input	Differential receive signal, side A, channel 0, negative
R35	B_PERp0	Diff Input	Differential receive signal, side B, channel 0, positive
T13	GND	Ground	Ground
T17	VCC1	Power	3.3 V Supply Voltage
T20	VCC1	Power	3.3 V Supply Voltage
T22	GND	Ground	Ground
T32	GND	Ground	Ground
T4	GND	Ground	Ground
U2	GND	Ground	Ground
U34	GND	Ground	Ground
V1	GND	Ground	Ground
V35	GND	Ground	Ground
W26	A_PETp1	Diff Output	Differential transmit signal, side A, channel 1, positive
W7	B_PETn1	Diff Output	Differential transmit signal, side B, channel 1, negative
Y2	A_PERp1	Diff Input	Differential receive signal, side A, channel 1, positive
Y34	B_PERn1	Diff Input	Differential receive signal, side B, channel 1, negative
AA10	B_PETp1	Diff Output	Differential transmit signal, side B, channel 1, positive
AA29	A_PETn1	Diff Output	Differential transmit signal, side B, channel 1, negative
AB1	A_PERn1	Diff Input	Differential receive signal, side A, channel 1, negative
AB35	B_PERp1	Diff Input	Differential receive signal, side B, channel 1, positive
AC13	GND	Ground	Ground
AC17	VCC1	Power	3.3 V Supply Voltage
AC20	VCC1	Power	3.3 V Supply Voltage
AC22	GND	Ground	Ground
AC32	GND	Ground	Ground
AC4	GND	Ground	Ground
AD2	GND	Ground	Ground
AD34	GND	Ground	Ground
AE1	GND	Ground	Ground
AE35	GND	Ground	Ground
AF26	A_PETp2	Diff Output	Differential transmit signal, side A, channel 2, positive
AF7	B_PETn2	Diff Output	Differential transmit signal, side B, channel 2, negative
AG2	A_PERn2	Diff Input	Differential receive signal, side A, channel 2, negative
AG34	B_PERp2	Diff Input	Differential receive signal, side B, channel 2, positive
AH10	B_PETp2	Diff Output	Differential transmit signal, side B, channel 2, positive
AH29	A_PETn2	Diff Output	Differential transmit signal, side A, channel 2, negative
AJ1	A_PERp2	Diff Input	Differential receive signal, side A, channel 2, positive
AJ35	B_PERn2	Diff Input	Differential receive signal, side B, channel 2, negative
AK13	GND	Ground	Ground

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
AK17	VCC1	Power	3.3 V Supply Voltage
AK20	VCC1	Power	3.3 V Supply Voltage
AK22	GND	Ground	Ground
AK32	GND	Ground	Ground
AK4	GND	Ground	Ground
AL2	GND	Ground	Ground
AL34	GND	Ground	Ground
AM1	GND	Ground	Ground
AM35	GND	Ground	Ground
AN26	A_PETp3	Diff Output	Differential transmit signal, side A, channel 3, positive
AN7	B_PETn3	Diff Output	Differential transmit signal, side B, channel 3, negative
AP2	A_PERn3	Diff Input	Differential receive signal, side A, channel 3, negative
AP34	B_PERp3	Diff Input	Differential receive signal, side B, channel 3, positive
AR10	B_PETp3	Diff Output	Differential transmit signal, side B, channel 3, positive
AR29	A_PETn3	Diff Output	Differential transmit signal, side A, channel 3, negative
AT1	A_PERp3	Diff Input	Differential receive signal, side A, channel 3, positive
AT35	B_PERn3	Diff Input	Differential receive signal, side B, channel 3, negative
AU13	GND	Ground	Ground
AU17	VCC1	Power	3.3 V Supply Voltage
AU20	VCC2	Power	3.3 V Supply Voltage
AU22	GND	Ground	Ground
AU32	GND	Ground	Ground
AU4	GND	Ground	Ground
AV2	GND	Ground	Ground
AV34	GND	Ground	Ground
AW1	GND	Ground	Ground
AW35	GND	Ground	Ground
AY26	A_PETp4	Diff Output	Differential transmit signal, side A, channel 4, positive
AY7	B_PETn4	Diff Output	Differential transmit signal, side B, channel 4, negative
BA2	A_PERp4	Diff Input	Differential receive signal, side A, channel 4, positive
BA34	B_PERn4	Diff Input	Differential receive signal, side B, channel 4, negative
BB10	B_PETp4	Diff Output	Differential transmit signal, side B, channel 4, positive
BB29	A_PETn4	Diff Output	Differential transmit signal, side A, channel 4, negative
BC1	A_PERn4	Diff Input	Differential receive signal, side A, channel 4, negative
BC35	B_PERp4	Diff Input	Differential receive signal, side B, channel 4, positive
BD13	GND	Ground	Ground
BD17	VCC2	Power	3.3 V Supply Voltage
BD20	VCC2	Power	3.3 V Supply Voltage
BD22	GND	Ground	Ground
BD32	GND	Ground	Ground
BD4	GND	Ground	Ground
BE2	GND	Ground	Ground
BE34	GND	Ground	Ground
BF1	GND	Ground	Ground

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
BF35	GND	Ground	Ground
BG26	A_PETp5	Diff Output	Differential transmit signal, side A, channel 5, positive
BG7	B_PETn5	Diff Output	Differential transmit signal, side B, channel 5, negative
BH2	A_PERp5	Diff Input	Differential receive signal, side A, channel 5, positive
BH34	B_PERn5	Diff Input	Differential receive signal, side B, channel 5, negative
BJ10	B_PETp5	Diff Output	Differential transmit signal, side B, channel 5, positive
BJ29	A_PETn5	Diff Output	Differential transmit signal, side A, channel 5, negative
BK1	A_PERn5	Diff Input	Differential receive signal, side A, channel 5, negative
BK35	B_PERp5	Diff Input	Differential receive signal, side B, channel 5, positive
BL13	GND	Ground	Ground
BL17	VCC2	Power	3.3 V Supply Voltage
BL20	VCC2	Power	3.3 V Supply Voltage
BL22	GND	Ground	Ground
BL32	GND	Ground	Ground
BL4	GND	Ground	Ground
BM2	GND	Ground	Ground
BM34	GND	Ground	Ground
BN1	GND	Ground	Ground
BN35	GND	Ground	Ground
BP26	A_PETp6	Diff Output	Differential transmit signal, side A, channel 6, positive
BP7	B_PETn6	Diff Output	Differential transmit signal, side B, channel 6, negative
BR2	A_PERn6	Diff Input	Differential receive signal, side A, channel 6, negative
BR34	B_PERp6	Diff Input	Differential receive signal, side B, channel 6, positive
BT10	B_PETp6	Diff Output	Differential transmit signal, side B, channel 6, positive
BT29	A_PETn6	Diff Output	Differential transmit signal, side A, channel 6, negative
BU1	A_PERp6	Diff Input	Differential receive signal, side A, channel 6, positive
BU35	B_PERn6	Diff Input	Differential receive signal, side B, channel 6, negative
BV13	GND	Ground	Ground
BV17	VCC2	Power	3.3 V Supply Voltage
BV20	VCC2	Power	3.3 V Supply Voltage
BV22	GND	Ground	Ground
BV32	GND	Ground	Ground
BV4	GND	Ground	Ground
BW2	GND	Ground	Ground
BW34	GND	Ground	Ground
BY1	GND	Ground	Ground
BY35	GND	Ground	Ground
CA26	A_PETp7	Diff Output	Differential transmit signal, side A, channel 7, positive
CA7	B_PETn7	Diff Output	Differential transmit signal, side B, channel 7, negative
CB2	A_PERn7	Diff Input	Differential receive signal, side A, channel 7, negative
CB34	B_PERp7	Diff Input	Differential receive signal, side B, channel 7, positive
CC10	B_PETp7	Diff Output	Differential transmit signal, side B, channel 7, positive
CC29	A_PETn7	Diff Output	Differential transmit signal, side A, channel 7, negative
CD1	A_PERp7	Diff Input	Differential receive signal, side A, channel 7, positive

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
CD35	B_PERn7	Diff Input	Differential receive signal, side B, channel 7, negative
CE13	GND	Ground	Ground
CE17	VCC2	Power	3.3 V Supply Voltage
CE20	VCC3	Power	3.3 V Supply Voltage
CE22	GND	Ground	Ground
CE32	GND	Ground	Ground
CE4	GND	Ground	Ground
CF2	GND	Ground	Ground
CF34	GND	Ground	Ground
CG1	GND	Ground	Ground
CG35	GND	Ground	Ground
CH26	A_PETp8	Diff Output	Differential transmit signal, side A, channel 8, positive
CH7	B_PETn8	Diff Output	Differential transmit signal, side B, channel 8, negative
CJ2	A_PERp8	Diff Input	Differential receive signal, side A, channel 8, positive
CJ34	B_PERn8	Diff Input	Differential receive signal, side B, channel 8, negative
CK10	B_PETp8	Diff Output	Differential transmit signal, side B, channel 8, positive
CK29	A_PETn8	Diff Output	Differential transmit signal, side A, channel 8, negative
CL1	A_PERn8	Diff Input	Differential receive signal, side A, channel 8, negative
CL35	B_PERp8	Diff Input	Differential receive signal, side B, channel 8, positive
CM13	GND	Ground	Ground
CM17	VCC3	Power	3.3 V Supply Voltage
CM20	VCC3	Power	3.3 V Supply Voltage
CM22	GND	Ground	Ground
CM32	GND	Ground	Ground
CM4	GND	Ground	Ground
CN2	GND	Ground	Ground
CN34	GND	Ground	Ground
CP1	GND	Ground	Ground
CP35	GND	Ground	Ground
CR26	A_PETp9	Diff Output	Differential transmit signal, side A, channel 9, positive
CR7	B_PETn9	Diff Output	Differential transmit signal, side B, channel 9, negative
CT2	A_PERp9	Diff Input	Differential receive signal, side A, channel 9, positive
CT34	B_PERn9	Diff Input	Differential receive signal, side B, channel 9, negative
CU10	B_PETp9	Diff Output	Differential transmit signal, side B, channel 9, positive
CU29	A_PETn9	Diff Output	Differential transmit signal, side A, channel 9, negative
CV1	A_PERn9	Diff Input	Differential receive signal, side A, channel 9, negative
CV35	B_PERp9	Diff Input	Differential receive signal, side B, channel 9, positive
CW13	GND	Ground	Ground
CW17	VCC3	Power	3.3 V Supply Voltage
CW20	VCC3	Power	3.3 V Supply Voltage
CW22	GND	Ground	Ground
CW32	GND	Ground	Ground
CW4	GND	Ground	Ground
CY2	GND	Ground	Ground

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
CY34	GND	Ground	Ground
DA1	GND	Ground	Ground
DA35	GND	Ground	Ground
DB26	A_PETp10	Diff Output	Differential transmit signal, side A, channel 10, positive
DB7	B_PETn10	Diff Output	Differential transmit signal, side B, channel 10, negative
DC2	A_PERn10	Diff Input	Differential receive signal, side A, channel 10, negative
DC34	B_PERp10	Diff Input	Differential receive signal, side B, channel 10, positive
DD10	B_PETp10	Diff Output	Differential transmit signal, side B, channel 10, positive
DD29	A_PETn10	Diff Output	Differential transmit signal, side A, channel 10, negative
DE1	A_PERp10	Diff Input	Differential receive signal, side A, channel 10, positive
DE35	B_PERn10	Diff Input	Differential receive signal, side B, channel 10, negative
DF13	GND	Ground	Ground
DF17	VCC3	Power	3.3 V Supply Voltage
DF20	VCC3	Power	3.3 V Supply Voltage
DF22	GND	Ground	Ground
DF32	GND	Ground	Ground
DF4	GND	Ground	Ground
DG2	GND	Ground	Ground
DG34	GND	Ground	Ground
DH1	GND	Ground	Ground
DH35	GND	Ground	Ground
DJ26	A_PETp11	Diff Output	Differential transmit signal, side A, channel 11, positive
DJ7	B_PETn11	Diff Output	Differential transmit signal, side B, channel 11, negative
DK2	A_PERn11	Diff Input	Differential receive signal, side A, channel 11, negative
DK34	B_PERp11	Diff Input	Differential receive signal, side B, channel 11, positive
DL10	B_PETp11	Diff Output	Differential transmit signal, side B, channel 11, positive
DL29	A_PETn11	Diff Output	Differential transmit signal, side A, channel 11, negative
DM1	A_PERp11	Diff Input	Differential receive signal, side A, channel 11, positive
DM35	B_PERn11	Diff Input	Differential receive signal, side B, channel 11, negative
DN13	GND	Ground	Ground
DN17	VCC3	Power	3.3 V Supply Voltage
DN20	VCC4	Power	3.3 V Supply Voltage
DN22	GND	Ground	Ground
DN32	GND	Ground	Ground
DN4	GND	Ground	Ground
DP2	GND	Ground	Ground
DP34	GND	Ground	Ground
DR1	GND	Ground	Ground
DR35	GND	Ground	Ground
DT26	A_PETp12	Diff Output	Differential transmit signal, side A, channel 12, positive
DT7	B_PETn12	Diff Output	Differential transmit signal, side B, channel 12, negative
DU2	A_PERp12	Diff Input	Differential receive signal, side A, channel 12, positive
DU34	B_PERn12	Diff Input	Differential receive signal, side B, channel 12, negative
DV10	B_PETp12	Diff Output	Differential transmit signal, side B, channel 12, positive

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
DV29	A_PETn12	Diff Output	Differential transmit signal, side A, channel 12, negative
DW1	A_PERn12	Diff Input	Differential receive signal, side A, channel 12, negative
DW35	B_PERp12	Diff Input	Differential receive signal, side B, channel 12, positive
DY13	GND	Ground	Ground
DY17	VCC4	Power	3.3 V Supply Voltage
DY20	VCC4	Power	3.3 V Supply Voltage
DY22	GND	Ground	Ground
DY32	GND	Ground	Ground
DY4	GND	Ground	Ground
EA2	GND	Ground	Ground
EA34	GND	Ground	Ground
EB1	GND	Ground	Ground
EB35	GND	Ground	Ground
EC26	A_PETp13	Diff Output	Differential transmit signal, side A, channel 13, positive
EC7	B_PETn13	Diff Output	Differential transmit signal, side B, channel 13, negative
ED2	A_PERp13	Diff Input	Differential receive signal, side A, channel 13, positive
ED34	B_PERn13	Diff Input	Differential receive signal, side B, channel 13, negative
EE10	B_PETp13	Diff Output	Differential transmit signal, side B, channel 13, positive
EE29	A_PETn13	Diff Output	Differential transmit signal, side A, channel 13, negative
EF1	A_PERn13	Diff Input	Differential receive signal, side A, channel 13, negative
EF35	B_PERp13	Diff Input	Differential receive signal, side B, channel 13, positive
EG13	GND	Ground	Ground
EG17	VCC4	Power	3.3 V Supply Voltage
EG20	VCC4	Power	3.3 V Supply Voltage
EG22	GND	Ground	Ground
EG32	GND	Ground	Ground
EG4	GND	Ground	Ground
EH2	GND	Ground	Ground
EH34	GND	Ground	Ground
EJ1	GND	Ground	Ground
EJ35	GND	Ground	Ground
EK26	A_PETp14	Diff Output	Differential transmit signal, side A, channel 14, positive
EK7	B_PETn14	Diff Output	Differential transmit signal, side B, channel 14, negative
EL2	A_PERn14	Diff Input	Differential receive signal, side A, channel 14, negative
EL34	B_PERp14	Diff Input	Differential receive signal, side B, channel 14, positive
EM10	B_PETp14	Diff Output	Differential transmit signal, side B, channel 14, positive
EM29	A_PETn14	Diff Output	Differential transmit signal, side A, channel 14, negative
EN1	A_PERp14	Diff Input	Differential receive signal, side A, channel 14, positive
EN35	B_PERn14	Diff Input	Differential receive signal, side B, channel 14, negative
EP13	GND	Ground	Ground
EP17	VCC4	Power	3.3 V Supply Voltage
EP20	VCC4	Power	3.3 V Supply Voltage
EP22	GND	Ground	Ground
EP32	GND	Ground	Ground

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
EP4	GND	Ground	Ground
ER2	GND	Ground	Ground
ER34	GND	Ground	Ground
ET1	GND	Ground	Ground
ET35	GND	Ground	Ground
EU26	A_PETp15	Diff Output	Differential transmit signal, side A, channel 15, positive
EU7	B_PETn15	Diff Output	Differential transmit signal, side B, channel 15, negative
EV2	A_PERn15	Diff Input	Differential receive signal, side A, channel 15, positive
EV34	B_PERp15	Diff Input	Differential receive signal, side B, channel 15, positive
EW10	B_PETp15	Diff Output	Differential transmit signal, side B, channel 15, negative
EW29	A_PETn15	Diff Output	Differential transmit signal, side A, channel 15, negative
EY1	A_PERp15	Diff Input	Differential receive signal, side A, channel 15, positive
EY35	B_PERn15	Diff Input	Differential receive signal, side B, channel 15, negative
FA15	GND	Ground	Ground
FA32	GND	Ground	Ground
FB2	GND	Ground	Ground
FB34	GND	Ground	Ground
FC19	GND	Ground	Ground
FC23	GND	Ground	Ground
FC25	GND	Ground	Ground
FC28	GND	Ground	Ground
FC3	GND	Ground	Ground
FC6	GND	Ground	Ground
FC9	GND	Ground	Ground
FD1	GND	Ground	Ground
FD35	GND	Ground	Ground
FE2	N/C	—	No internal connection.
FE34	N/C	—	No internal connection.
FF11	RSVD2	—	Reserved for future use. No internal connection.
FF14	GND	Ground	Ground
FF18	RSVD6	—	Reserved for future use. No internal connection.
FF21	GND	Ground	Ground
FF24	MODE	Input	5-level input strap pin. Sets device control configuration modes. The pin can be exercised at device power up or in normal operation mode. Note the pull-down resistor values as outlined below are different than other 5-level pins of the device. L1: SMBus/I^{2}C controller mode - device control configuration is read from external EEPROM. When the device has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I^{2}C target operation is available in this mode before, during or after EEPROM reading. Note during EEPROM reading if the external SMBus/I^{2}C controller wants to access the device registers it must support arbitration. To set the pin for L1 pull-down with 2.062 kΩ±10% resistor. L2: SMBus/I^{2}C target mode – device control configuration is done by an external controller with SMBus/I^{2}C controller. To set the pin for L2 pull-down with 6.225 kΩ±10% resistor. L0, L3 and L4: RESERVED – TI internal test modes.

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
FF27	ALL_DONE#	Output	EEPROM loading is done. Active low 3.3 V open drain output pin. The pin can be left unconnected. In *SMBus/I²C controller mode*: Indicates the completion of a valid EEPROM register load operation. External pullup resistor such as 4.7 kΩ required for operation. • High: External EEPROM load failed or incomplete • Low: External EEPROM load successful and complete In *SMBus/I²C target*: The pin is High-Z.
FF30	B_ADDR1_15-8	Input	5-level input strap pins, as provided in 表 7-3. Sets SMBus/I²C target address, as provided in 表 8-1 and 表 8-2.
FF33	PD_3-0	Input	3.3 V LVCMOS input. Implements device power-down or reset, as provided in 表 8-1.
FF5	A_ADDR0_15-8	Input	5-level input strap pins, as provided in 表 7-3. Sets SMBus/I²C target address, as provided in 表 8-1 and 表 8-2.
FF8	PD_15-12	Input	3.3 V LVCMOS input. Implements device power-down or reset, as provided in 表 8-1.
FG1	N/C	—	No internal connection.
FG35	N/C	—	No internal connection.
FH2	N/C	—	No internal connection.
FH34	N/C	—	No internal connection.
FJ12	GND	Ground	Ground
FJ16	RSVD5	—	Reserved for future use. No internal connection.
FJ19	GND	Ground	Ground
FJ23	RSVD1	Input	TI internal use. Leave unconnected.
FJ25	READ_EN_#	Input	Initiate EEPROM load. Active low 3.3 V LVCMOS input.. In *SMBus/I²C controller mode*: After device power up, when the pin is low, it initiates the EEPROM read function. Once EEPROM read is complete (indicated by ALL_DONE# asserted low), this pin can be held low for normal device operation. During the EEPROM load process the device’s signal path is disabled. In *SMBus/I²C target*: In these modes the pin is not used. The pin can be left floating. The pin has internal 1-MΩ weak pull-down resistor.
FJ28	B_ADDR0_15-8	Input	5-level input strap pins, as provided in 表 7-3. Sets SMBus/I²C target address, as provided in 表 8-1 and 表 8-2.
FJ3	A_ADDR1_15-8	Input	5-level input strap pins as provided in 表 7-3. Sets SMBus/I²C target address, as provided in 表 8-1 and 表 8-2.
FJ31	PD_7-4	Input	3.3 V LVCMOS input. Implements device power-down or reset, as provided in 表 8-1.
FJ6	PD_11-8	Input	3.3 V LVCMOS input. Implements device power-down or reset, as provided in 表 8-1.
FJ9	RSVD0	Input	TI internal use. Leave unconnected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC_{ABSMAX}	Supply voltage (VCC)	–0.5	4.0	V
$VIO_{CMOS,ABSMAX}$	3.3 V LVCMOS and open drain I/O voltage	–0.5	4.0	V
$VIO_{5LVL,ABSMAX}$	5-level input I/O voltage	–0.5	2.75	V
$VIO_{HS-RX,ABSMAX}$	High-speed I/O voltage (RXnP, RXnN)	–0.5	3.2	V
$VIO_{HS-TX,ABSMAX}$	High-speed I/O voltage (TXnP, TXnN)	–0.5	2.75	V
$T_{J,ABSMAX}$	Junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD and Latchup Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	
$V_{(Signal)}$	Signal pin latch-up	Signal pin test, per JESD78F class II, immunity level A	±100	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage, VCC to GND	DC plus AC power should not exceed these limits	3.0	3.3	3.6	V
N_{VCC}	Supply noise tolerance	DC to <50 Hz, sinusoidal[1]			250	mVpp
		50 Hz to 500 kHz, sinusoidal[1]			100	mVpp
		500 kHz to 2.5 MHz, sinusoidal[1]			33	mVpp
		Supply noise, >2.5 MHz, sinusoidal[1]			10	mVpp
$T_{RampVCC}$	VCC supply ramp time	From 0 V to 3.0 V	0.150		100	ms
T_J	Operating junction temperature		–40		120	°C
PW_{LVCMOS}	Minimum pulse width required for the device to detect a valid signal on LVCMOS inputs	PDx, and READ_EN_N	200			µs
VCC_{SMBUS}	SMBus/I²C SDA and SCL open drain termination voltage	Supply voltage for open drain pull-up resistor			3.6	V
F_{SMBus}	SMBus/I²C clock (SCL) frequency in target mode		10		400	kHz
VID_{LAUNCH}	Source differential launch amplitude		800		1200	mVpp
DR	Data rate		1		32	Gbps

6.4 Thermal Information

THERMAL METRIC(1)		DS320PR1601 ZDG (nfBGA, 354)	UNIT
$R_{\theta JA\text{-}High\ K}$	Junction-to-ambient thermal resistance	17.4	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.5	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.1	℃/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	℃/W
ψ_{JB}	Junction-to-board characterization parameter	5.9	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	℃/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
P_{ACT}	Device active power	32-channels (16-lanes), EQ = 0-2		4.7	6.0	W
P_{ACT}	Device active power	32-channels (16-lanes), EQ = 5-19		5.8	7.0	W
P_{RXDET}	Device power consumption while waiting for far end receiver terminations	All channels enabled but no far end receiver detected		660		mW
P_{STBY}	Device power consumption in standby power mode	All channels disabled		92		mW
Control IO						
V_{IH}	High level input voltage	SDA, SCL, PD, READ_EN_N pins	2.1			V
V_{IL}	Low level input voltage	SDA, SCL, PD, READ_EN_N, SEL pins			1.08	V
V_{OH}	High level output voltage	$R_{pull\text{-}up}$ = 4.7 kΩ (SDA, SCL, ALL_DONE_N pins)	2.1			V
V_{OL}	Low level output voltage	I_{OL} = – 4 mA (SDA, SCL, ALL_DONE_N pins)			0.4	V
I_{IH}	Input high leakage current	V_{Input} = VCC, (SCL, SDA, PD, READ_EN_N pins)			40	µA
I_{IL}	Input low leakage current	V_{Input} = 0 V, (SCL, SDA, PD, READ_EN_N pins)	-40			µA
$I_{IH,FS}$	Input high leakage current for fail safe input pins	V_{Input} = 3.6 V, VCC = 0 V, (SCL, SDA, PD, READ_EN_N pins)			800	µA
$C_{IN\text{-}CTRL}$	Input capacitance	SDA, SCL, PD, READ_EN_Npins		1.2		pF
5 Level IOs (MODE, A/B_ADDR pins)						
I_{IH_5L}	Input high leakage current, 5-level IOs	VIN = 2.5 V			40	µA
I_{IL_5L}	Input low leakage current for all 5-level IOs except MODE.	VIN = GND	-40			µA
$I_{IL\_5L,MODE}$	Input low leakage current for MODE pin	VIN = GND	-800			µA
Receiver						
$V_{RX\text{-}DC\text{-}CM}$	Rx DC common mode voltage	Device is in active or standby state		1.4		V
$Z_{RX\text{-}DC}$	Rx DC single-ended impedance			50		Ω
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	DC input CM input impedance during Reset or power-down	Inputs are at $V_{RX\text{-}DC\text{-}CM}$ voltage	15			kΩ
Transmitter						

6.5 DC Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Z_{TX-DIFF-DC}$	DC differential Tx impedance	Impedance of Tx during active signaling, VID,diff = 1Vpp		100		Ω
$V_{TX-DC-CM}$	Tx DC common mode Voltage			1.0		V
$I_{TX-SHORT}$	Tx short Circuit Current	Total current the Tx can supply when shorted to GND		70		mA

6.6 High Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
$RL_{RX-DIFF}$	Input differential return loss	50 MHz		-32		dB
		4 GHz		-22		dB
		8 GHz		-14		dB
		16 GHz		-9		dB
RL_{RX-CM}	Input common-mode return loss	50 MHz		-24		dB
		4 GHz		-18		dB
		8 GHz		-14		dB
		16 GHz		-8		dB
XT_{RX}	Receive-side pair-to-pair isolation	Pair-to-pair isolation (SDD21) between two adjacent receiver pairs from 10 MHz to 16 GHz.		-50		dB
Transmitter						
$V_{TX-AC-CM-PP}$	Tx AC peak-to-peak common mode voltage	Measured with lowest EQ, flat_gain = 101			50	mVpp
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during receiver detection	Measured while Tx is sensing whether a low-impedance receiver is present. No load is connected to the driver output	0		600	mV
$RL_{TX-DIFF}$	Output differential return loss	50 MHz		-30		dB
		4 GHz		-14		dB
		8 GHz		-11		dB
		16.0 GHz		-9		dB
RL_{TX-CM}	Output common-mode return loss	50 MHz		-22		dB
		4 GHz		-16		dB
		8 GHz		-8		dB
		16 GHz		-8		dB
XT_{TX}	Transmit-side pair-to-pair isolation	Minimum pair-to-pair isolation (SDD21) between two adjacent transmitter pairs from 10 MHz to 16 GHz.		-45		dB
$C_{AC,TX}$	AC coupling capacitors on transmit pins (integrated inside device package)			220		nF
Device Datapath						
$T_{PLHD/PHLD}$	Input-to-output latency (propagation delay) through a data channel	For either Low-to-High or High-to-Low transition.		130	170	ps
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	Between any two lanes within a single transmitter.			24	ps

6.6 High Speed Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{RJ-DATA}$	Additive random jitter with data	Jitter through redriver minus the calibration trace. 32 Gbps PRBS15. 800 mVpp-diff input swing.		50		fs
$T_{RJ-INTRINSIC}$	Intrinsic additive random jitter with clock	Jitter through redriver minus the calibration trace. 16 GHz CK. 800 mVpp-diff input swing.		30		fs
$JITTER_{TOTAL-DATA}$	Additive total jitter with data	Jitter through redriver minus the calibration trace. 32 Gbps PRBS15. 800 mVpp-diff input swing.		2.3		ps
$JITTER_{TOTAL-INTRINSIC}$	Intrinsic additive total jitter with clock	Jitter through redriver minus the calibration trace. 16 GHz CK. 800 mVpp-diff input swing.		1		ps
$EQ\text{-}MIN_{16G}$	EQ boost at min setting (EQ INDEX = 0)	AC gain at 16 GHz relative to gain at 100 MHz.		2.9		dB
$EQ\text{-}MAX_{16G}$	EQ boost at max setting (EQ INDEX = 19)	AC gain at 16 GHz relative to gain at 100 MHz.		21		dB
$FLAT\text{-}GAIN_{VAR}$	Flat gain variation across PVT measured at DC	Flat_gain = 000, 001, 011, 101 or 111, at minimum EQ setting. Max-Min for a single channel.	-1.0		1.0	dB
$EQ\text{-}GAIN_{VAR,16G}$	EQ boost variation across PVT	At 16 GHz. Flat_gain = 101, maximum EQ setting. Max-Min.	-4		3	dB
LINEARITY-DC	Output DC linearity	Flat_gain = 101. 128T pattern at 2.5 Gbps.		1800		mVpp
LINEARITY-AC	Output AC linearity	Flat_gain = 101. 1T pattern at 32 Gbps.		770		mVpp

6.7 SMBUS/I^{2}C Timing Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Target Mode						
t_{SP}	Pulse width of spikes which must be suppressed by the input filter				50	ns
t_{HD-STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated		0.6			µs
t_{LOW}	LOW period of the SCL clock		1.3			µs
T_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU-STA}	Set-up time for a repeated START condition		0.6			µs
t_{HD-DAT}	Data hold time		0			µs
T_{SU-DAT}	Data setup time		0.1			µs
t_r	Rise time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10 pF		120		ns
t_f	Fall time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10 pF		2		ns
t_{SU-STO}	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
t_{VD-DAT}	Data valid time				0.9	µs
t_{VD-ACK}	Data valid acknowledge time				0.9	µs
C_b	Capacitive load for each bus line				400	pF

6.7 SMBUS/I²C Timing Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Controller Mode						
f_{SCL-M}	SCL clock frequency	MODE = L1 (controller mode)		303		kHz
t_{LOW-M}	SCL low period			1.90		µs
T_{HIGH-M}	SCL high period			1.40		µs
$t_{SU-STA-M}$	Set-up time for a repeated START condition			2		µs
$t_{HD-STA-M}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated			1.5		µs
$T_{SU-DAT-M}$	Data setup time			1.4		µs
$t_{HD-DAT-M}$	Data hold time			0.5		µs
t_{R-M}	Rise time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10 pF		120		ns
T_{F-M}	Fall time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10 pF		2		ns
$t_{SU-STO-M}$	Stop condition setup time			1.5		µs
EEPROM Timing						
T_{EEPROM}	EEPROM configuration load time	Time to assert ALL_DONE_N after READ_EN_N has been asserted.		30		ms
T_{POR}	Time to first SMBus access	Power supply stable after initial ramp. Includes initial power-on reset time.		50		ms

6.8 Typical Characteristics

图 6-1 shows typical EQ gain curves versus frequency for different EQ settings for the DS320PR1601. 图 6-2 shows typical differential return loss for Rx and Tx pins - smoothing window applied.

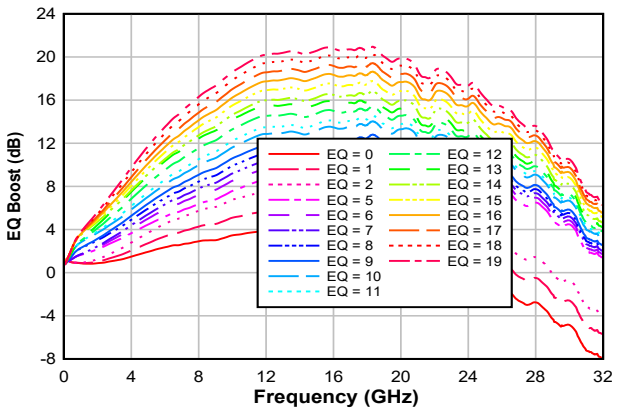


图 6-1. Typical EQ Boost vs Frequency

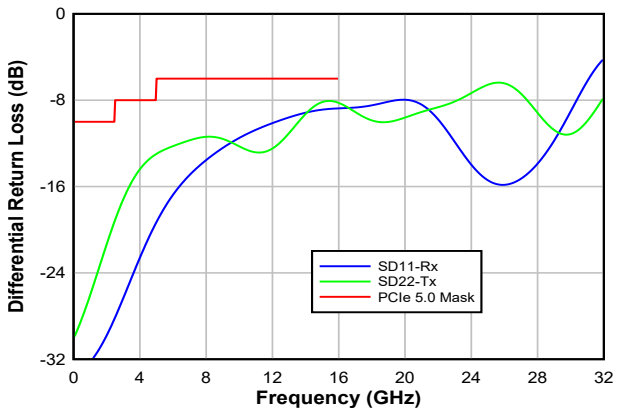


图 6-2. Typical Differential Return Loss

6.9 Typical Jitter Characteristics

图 6-3 and 图 6-4 show eye diagrams through calibration traces, and through the DS320PR1601 (DUT) respectively. Note: DS320PR1601 adds almost no random or deterministic jitter.

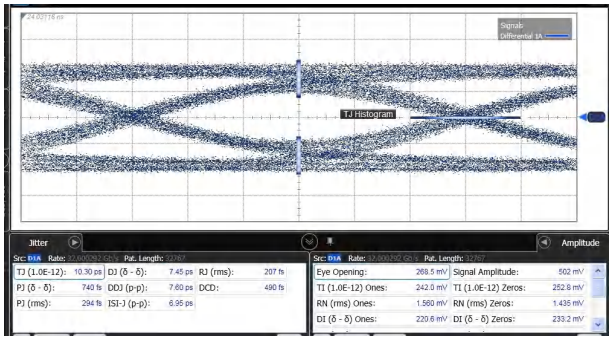


图 6-3. Through Baseline Calibration Trace Setup

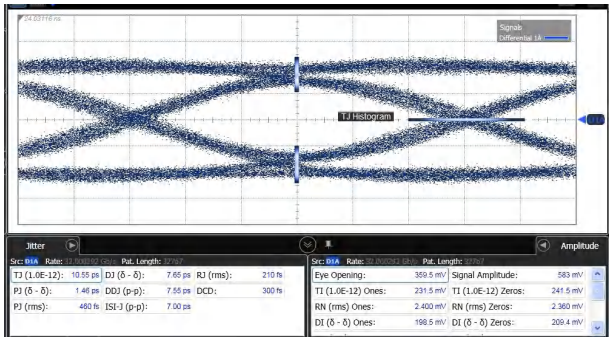


图 6-4. Through the DS320PR1601 with DUT EQ = 0

7 Detailed Description

7.1 Overview

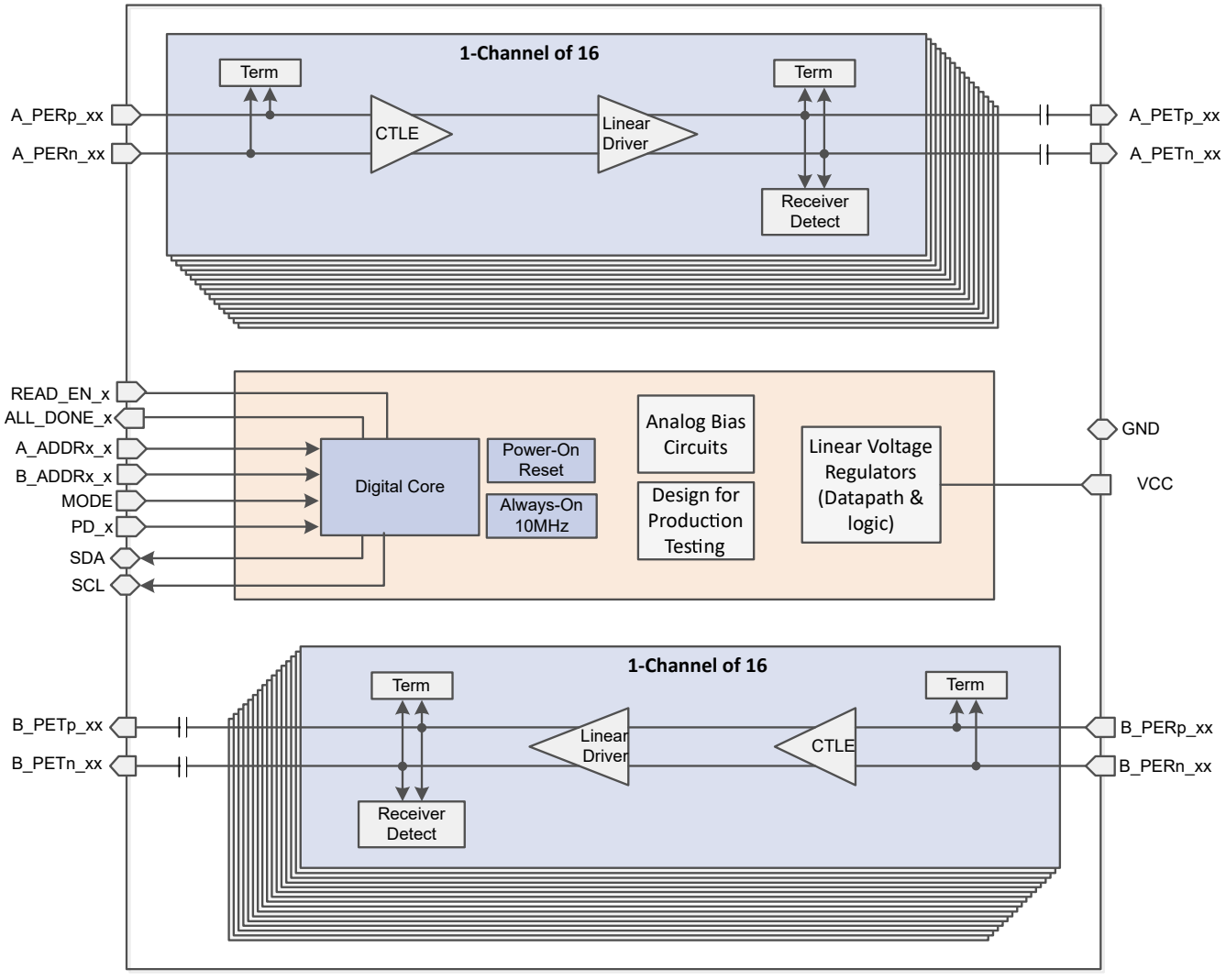
The DS320PR1601 is a 16-lane multi-rate linear repeater with integrated signal conditioning. The device's signal channels operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver. The linearity of the data path is specifically designed to preserve any transmit equalization while keeping receiver equalization effective.

The DS320PR1601 can be configured two different ways:

SMBus/I²C controller mode – device control configuration is read from external EEPROM. When the DS320PR1601 has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I²C target operation is available in this mode before, during or after EEPROM reading. Note during EEPROM reading if the external SMBus/I²C controller wants to access DS320PR1601 registers it must support arbitration. The mode is preferred when software implementation is not desired.

SMBus/I²C target mode – provides most flexibility. Requires a SMBus/I²C controller device to configure DS320PR1601 though writing to its target address.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Linear Equalization

The DS320PR1601 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. The device has 18 available equalization boost settings that can be set though SMBus/I^{2}C registers. 表 7-1 provides the device EQ settings.

Refer to the *DS160PR1601 and DS320PR1601 Programming Guide* for detail register sets and control configuration procedures.

表 7-1. Equalization Control Settings

EQUALIZATION SETTING	TYPICAL EQ BOOST (dB)		
EQ INDEX	at 4 GHz	at 8 GHz	at 16 GHz
0	1.5	2.9	2.9
1	2.1	4.3	4.9
2	2.8	5.7	6.9
5	3.7	6.4	9.2
6	4.1	7.2	10.1
7	4.4	7.8	10.9
8	4.9	8.5	11.5
9	5.3	9.1	12.2
10	5.9	10.1	13.5
11	6.2	10.5	14.0
12	6.9	11.5	15.0
13	7.5	12.4	15.8
14	7.7	12.7	16.5
15	8.1	13.5	17.5
16	8.4	14.1	18.3
17	8.9	14.9	19.2
18	9.3	15.6	20.0
19	9.8	16.3	21.0

Note in I^{2}C mode default EQ setting does not map one of the EQ index, as provided in 表 7-1. EQ Boost values are same as EQ INDEX = 5 with slightly different EQ profile.

EQ profile selection option available through I^{2}C shared register 0x03 provides subtle EQ gain curve modification option to match board trace or cable loss profile. The fine tuning alters mid frequency EQ boost values. EQ profile controls are thermometer coded and increase boost at 1 GHz by about 0.5 dB per setting increase. The equalization boost values for the range of 4-16 GHz are mostly unchanged with this subtle EQ gain profile change.

7.3.2 Flat-Gain

The overall datapath Flat-Gain (DC and AC) of the DS320PR1601 can be programmed through SMBus/I^{2}C registers. 表 7-2 provides five available flat gain settings to configure the DS320PR1601 datapaths.

表 7-2. Flat Gain Settings

Flat_gain	SETTING
000	-6 dB (-5.6 dB actual)
001	-4 dB (-3.8 dB actual)
011	-2 dB (-1.2 dB actual)

表 7-2. Flat Gain Settings (continued)

Flat_gain	SETTING
101	0 dB (0.6 dB actual, default / recommended)
111	+ 2dB (+2.6 dB actual)

The default recommendation for most systems will be 0 dB.

The Flat-Gain and equalization of the DS320PR1601 must be set such that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively.

Refer to the *DS160PR1601 and DS320PR1601 Programming Guide* for detail register sets and control configuration procedures.

7.3.3 Receiver Detect State Machine

The DS320PR1601 deploys an Rx detect state machine that governs the Rx detection cycle as defined in the PCI express specifications. At power up, after a manually triggered event through PDx pins, or writing to the relevant I^2C/SMBus register, the redriver determines whether or not a valid PCI express termination is present at the far end of the link. The Rx Detect Registers provide additional flexibility for system designers to appropriately set the device in desired mode through SMBus/I^2C control interface.

7.3.4 Five-Level Control Inputs

The DS320PR1601 has 5-level inputs pins that are used to control the configuration of the device. These 5-level inputs use a resistor divider (internal pull-up and external pull-down resistor) to help set the 5 valid levels and provide a wider range of control settings. External resistors must be of 10% tolerance or better. The pins are sampled at power-up only. 表 7-3 lists the pull-down resistor values to set the control logic levels for all 5-level control pins except MODE pin. For MODE pin refer to pin definition.

表 7-3. 5-level Control Pin Settings

LEVEL	SETTING
L0	1 kΩ to GND
L1	8.25 kΩ to GND
L2	24.9 kΩ to GND
L3	75 kΩ to GND
L4	F (Float)

7.3.5 Integrated Capacitors

The DS320PR1601 has integrated AC coupling capacitors for all Tx pins (64 count). The capacitors are 220 nF each with 2.5 V voltage rating and 20% tolerance.

7.4 Device Functional Modes

7.4.1 Active PCIe Mode

The device is in normal operation with PCIe state machine enabled through SMBus/I^2C registers. In this mode PDx pins are driven low in a system (by PCIe connector PRSNTx# or fundamental reset PERST# signal). In this mode, the DS320PR1601 equalizes PCIe Rx or Tx signals to provide better signal integrity.

7.4.2 Active Buffer Mode

The device is in normal operation with PCIe state machine disabled through I^2C registers. This mode is recommended for non-PCIe use cases. In this mode the device is working as a buffer to provide linear equalization to improve signal integrity.

7.4.3 Standby Mode

The device is in standby mode invoked by PDx pins. In this mode, the device is in standby mode conserving power.

8 Programming

8.1 Pin Configurations for Lanes

The DS320PR1601 has 16 data lanes with 16-Tx channels and 16-Rx channels. The data channels are grouped for I²C configurations and PCIe state machine grouping as provided in 表 8-1 using xADDRx and PDx pins. 表 8-1 provides the channel grouping.

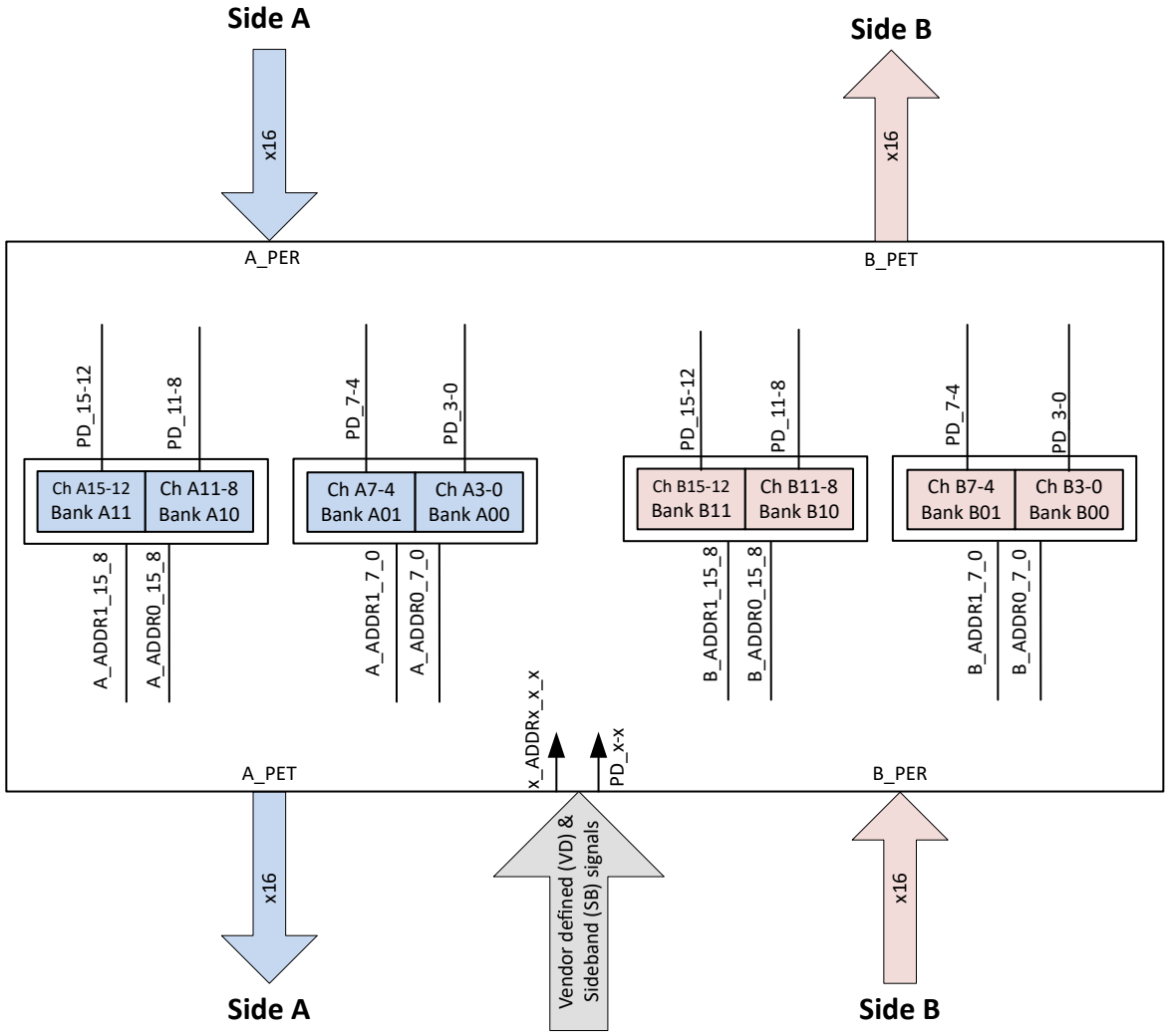


图 8-1. Pin Configurations for Lanes

表 8-1. Definition of PDx and xADDRx pins

Pin Name	Description
PD_15-12 PD_11-8 PD_7-4 PD_3-0	Active in all device control modes. The pin has internal 1-MΩ weak pulldown resistor. The pin triggers PCIe Rx detect state machine when toggled. • High: power down • Low: power up normal operation. Each PD pin sets control for a bank of 8 lanes (4 from Side A and 4 from Side B) to provide flexibility for x4 and x8 bifurcation: • PD_15-12: channels x15-12, both Side A and B • PD_11-8: channels x11-8, both Side A and B • PD_7-4: channels x7-4, both Side A and B • PD_3-0: channels x3-0, both Side A and B PCIe hot plug insertion implementation varies from system to system. PDx pins are driven low in a system (for example, by PCIe CEM interface PRSNTx# or fundamental reset PERST# signal with appropriate polarity). For PCIe x16 application all four PD signals can be shorted together.
A_ADDR1_15-8 A_ADDR0_15-8 A_ADDR1_7-0 A_ADDR0_7-0 B_ADDR1_15-8 B_ADDR0_15-8 B_ADDR1_7-0 B_ADDR0_7-0	5-level input pins as implemented by pull-down resistor on the pin as provided in 表 7-3. These pins are sampled at device power-up only. Sets SMBus / I²C target address as provided in 表 8-2. Each set of ADDR1 and ADDR0 pins defines the addresses for bank of 8 lanes: • A_ADDR1_15-8, A_ADDR0_15-8: channels A15-8 of Side A • A_ADDR1_7-0, A_ADDR0_7-0: channels A7-0 of Side A • B_ADDR1_15-8, B_ADDR0_15-8: channels B15-8 of Side B • B_ADDR1_7-0, B_ADDR0_7-0: channels B7-0 of Side B 图 8-1 shows how I²C target addresses are accessed for specific lanes.

8.2 SMBUS/I²C Register Control Interface

If MODE = L2 (SMBus / I²C target control mode), the DS320PR1601 is configured through a standard I²C or SMBus interface that may operate up to 400 kHz. The device also can be configured through loading settings from EEPROM. The SMBus / I²C target address of the DS320PR1601 is determined by the pin strap settings on the xADDRx pins. Note addresses to access differential channels are different. To illustrate A_ADDR1_15_8 and A_ADDR0_15_8 sets the target address for bank of lanes 15-12 and 11-8 of Side A, while A_ADDR1_7_0 and A_ADDR0_7_0 sets for bank of lanes 7-4 and 3-0 of Side A. B side address is also set similarly. 表 8-2 provides SMBus / I²C target addresses.

表 8-2. SMBus / I²C Target Address

x_ADDR1_x	x_ADDR0_x	7-bit address Upper (for Side A) / Lower (for Side B) 4 Lanes of each Bank	7-bit address Lower (for Side A) / Upper (for Side B) 4 Lanes of each Bank
L0	L0	0x19	0x18
L0	L1	0x1B	0x1A
L0	L2	0x1D	0x1C
L0	L3	0x1F	0x1E
L0	L4	Reserved	Reserved
L1	L0	0x21	0x20
L1	L1	0x23	0x22
L1	L2	0x25	0x24
L1	L3	0x27	0x26
L1	L4	Reserved	Reserved
L2	L0	0x29	0x28
L2	L1	0x2B	0x2A
L2	L2	0x2D	0x2C
L2	L3	0x2F	0x2E
L2	L4	Reserved	Reserved
L3	L0	0x31	0x30
L3	L1	0x33	0x32
L3	L2	0x35	0x34
L3	L3	0x37	0x36
L3	L4	Reserved	Reserved

In SMBus/I²C modes the SCL, SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

Refer to the *DS160PR1601 and DS320PR1601 Programming Guide* for detail register sets and control configuration procedures.

8.2.1 Shared Registers

表 8-3. General Registers (Offset = 0xE2)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	rst_i2c_regs	R/W/SC	0x0	Device reset control: Reset all I²C registers to default values (self-clearing).
5	rst_i2c_mas	R	0x0	Reserved
4-1	RESERVED	R	0x0	Reserved
0	frc_eeprm_rd	R/W/SC	0x0	Override MODE and READ_EN_N status to force manual EEPROM configuration load.

表 8-4. DEVICE_ID0 Register (Offset = 0xF0)

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x1	Reserved
3	device_id0_3	R	0x0	Device ID0 [3:1]: 011
2	device_id0_2	R	0x1	see MSB

表 8-4. DEVICE_ID0 Register (Offset = 0xF0) (continued)

Bit	Field	Type	Reset	Description
1	device_id0_1	R	0x1	see MSB
0	RESERVED	R	0	Reserved

表 8-5. *DEVICE_ID1 Register (Offset = 0xF1)*

Bit	Field	Type	Reset	Description
7	device_id[7]	R	0x0	Device ID 0010 1001: DS320PR1601
6	device_id[6]	R	0x0	see MSB
5	device_id[5]	R	0x1	see MSB
4	device_id[4]	R	0x0	see MSB
3	device_id[3]	R	0x1	see MSB
2	device_id[2]	R	0x0	see MSB
1	device_id[1]	R	0x0	see MSB
0	device_id[0]	R	0x1	see MSB

8.2.2 Channel Registers

表 8-6. RX Detect Status Register (Channel Register Base + Offset = 0x00)

Bit	Field	Type	Reset	Description
7	rx_det_comp_p	R	0x0	Rx detect positive data pin status: 0: not detected 1: detected – the value is latched
6	rx_det_comp_n	R	0x0	Rx detect negative data pin status: 0: not detected 1: detected – the value is latched
5-0	RESERVED	R	0x0	Reserved

表 8-7. EQ Gain Control Register (Channel Register Base + Offset = 0x01)

Bit	Field	Type	Reset	Description
7	eq_stage1_bypass	R/W	0x0	Enable EQ stage 1 bypass: 0: bypass disabled 1: bypass enabled
6	eq_stage1_3	R/W	0x0	EQ boost stage 1 control See 表 7-1 for details
5	eq_stage1_2	R/W	0x0	
4	eq_stage1_1	R/W	0x0	
3	eq_stage1_0	R/W	0x0	
2	eq_stage2_2	R/W	0x0	EQ boost stage 2 control See 表 7-1 for details
1	eq_stage2_1	R/W	0x0	
0	eq_stage2_0	R/W	0x0	

表 8-8. Mute EQ Control Register (Channel register base + Offset = 0x02)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-4	RESERVED	R/W	0x0	Reserved
3	mute_eq	R/W	0x0	Mute EQ output
2-0	RESERVED	R	0x0	Reserved

表 8-9. EQ Gain / Flat Gain Control Register (Channel Register Base + Offset = 0x03)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	eq_profile_3	R/W	0x0	EQ mid-frequency boost profile See 节 7.3.1 for details
5	eq_profile_2	R/W	0x0	
4	eq_profile_1	R/W	0x0	
3	eq_profile_0	R/W	0x0	
2	flat_gain_2	R/W	0x1	Flat gain select: See 表 7-2 for details
1	flat_gain_1	R/W	0x0	
0	flat_gain_0	R/W	0x1	

表 8-10. Rx Detect Control Register (Channel Register Base + Offset = 0x04)

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	Reserved
2	mr_rx_det_man	R/W	0x0	Manual override of rx_detect_p/n decision: 0: Rx detect state machine is enabled 1: Rx detect state machine is overridden – always valid RX termination detected
1	en_rx_det_count	R/W	0x0	Enable additional Rx detect polling 0: additional Rx detect polling disabled 1: additional Rx detect polling enabled
0	sel_rx_det_count	R/W	0x0	Select number of valid Rx detect polls – gated by en_rx_det_count = 1 0: device transmitters poll until 2 consecutive valid detections 1: device transmitters poll until 3 consecutive valid detections

表 8-11. PD Override Register (Channel Register Base + Offset = 0x05)

Bit	Field	Type	Reset	Description
7	device_en_override	R/W	0x0	Enable power down overrides through SMBus/I^{2}C 0: manual override disabled 1: manual override enabled
6-0	device_en	R/W	0b111111	Manual power down of redriver various blocks – gated by device_en_override = 1 111111: all blocks are enabled 000000: all blocks are disabled

表 8-12. Bias Register (Channel Register Base + Offset = 0x06)

Bit	Field	Type	Reset	Description
5-3	Bias current	R/W	0b100	Control bias current
7,6,2-0	Reserved	R/W	0b00000	Reserved

8.3 SMBus/I^{2}C Controller Mode Configuration (EEPROM Self Load)

The DS320PR1601 can also be configured by reading from EEPROM. To enter into this mode MODE pin must be set to L1. The EEPROM load operation only happens once after the device's initial power-up. If the DS320PR1601 is configured for SMBus controller mode, then it will remain in the SMBus IDLE state until the READ_EN_N pin is asserted to LOW. After the READ_EN_N pin is driven LOW, the DS320PR1601 becomes an SMBus controller and attempts to self-configure by reading device settings stored in an external EEPROM (SMBus 8-bit address 0xA0). When the DS320PR1601 has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I^{2}C target operation is available in this mode before, during or after EEPROM reading. Note during EEPROM reading if the external SMBus/I^{2}C controller wants to access DS320PR1601 registers it must support arbitration.

When designing a system for using the external EEPROM, the user must follow these specific guidelines:

- EEPROM size of 2Kb (256 × 8-bit) is recommended.
- Set MODE = L1, configure for SMBus controller mode
- The external EEPROM device address byte must be 0xA0 and capable of 400 kHz operation at 3.3 V supply
- In SMBus/I^2C modes the SCL, SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

Refer to the *DS160PR1601 and DS320PR1601 Programming Guide* for detail register sets and control configuration procedures.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS320PR1601 is a high-speed linear repeater which extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. It can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

9.2 Typical Applications

The DS320PR1601 is a 16-lane protocol agnostic PCI Express linear redriver. Its protocol agnostic nature allows it to be used in PCI Express x4, x8, and x16 applications. 图 9-1 shows how single DS320PR1601 can be used in four x4, two x8 or single x16 links.

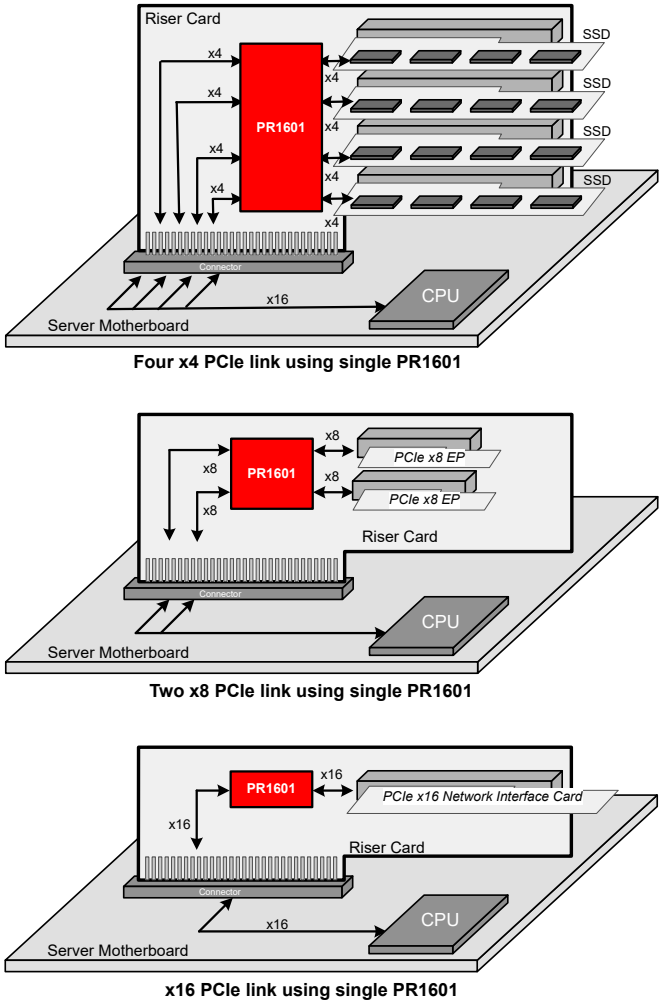


图 9-1. PCI Express x4, x8, and x16 Implementation Using DS320PR1601

9.2.1 PCIe x16 Lane Configuration

The DS320PR1601 can be used in server or motherboard applications to boost transmit and receive signals to increase the reach of the host or root complex processor to PCI Express slots or connectors. The section outlines detailed procedure and design requirement for a typical PCIe x16 lane configuration. However, the design recommendations can also be used in x4 or x8 lane configuration.

9.2.1.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design.

- Use 85 Ω impedance traces when interfacing with PCIe CEM connectors. Length matching on the P and N traces should be done on the single-end segments of the differential pair.
- Use a uniform trace width and trace spacing for differential pairs.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias for a low inductance path for the return current.

9.2.1.2 Detailed Design Procedure

In PCIe Gen 3.0 , 4.0 and 5.0 applications, the specification requires Rx-Tx (of root-complex and endpoint) link training to establish and optimize signal conditioning settings. In link training, the Rx partner requests a series of FIR – preshoot and deemphasis coefficients (10 presets) from the Tx partner. The Rx partner includes 7-levels of CTLE followed by a single tap DFE. The link training would pre-condition the signal, with an equalized link between the root-complex and endpoint resulting an optimized link. Note that there is no link training in PCIe Gen 1.0 (2.5 Gbps) or PCIe Gen 2.0 (5.0 Gbps) applications.

The DS320PR1601 is designed with linear datapath to pass the Tx Preset signaling (by root complex and end point) onto the Rx (of root complex and end point) for a PCIe link to train and optimize for the Rx equalization settings. The linear redriver helps extend the PCB trace reach distance by boosting the attenuated signals with its own equalization, which allows the Rx to recover signals more easily. The device must be placed in between the Tx and Rx (of root complex and end point) such a way that signal swing of both upstream and downstream signals stays within the linearity range of the device. Adjustments to the DS320PR1601 EQ setting should be performed based on the channel loss to optimize the eye opening in the Rx partner. The available EQ gain settings are provided in 表 7-1. For most PCIe systems the default flat gain setting of 0 dB (flat_gain = 101) would be sufficient.

The DS320PR1601 can be optimized for a given system utilizing its two configuration modes – SMBus/I^{2}C controller mode and SMBus/I^{2}C target mode. In SMBus/I^{2}C modes the SCL, SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

图 9-2 shows a simplified schematic for x16 lane configuration in SMBus/I²C controller mode.

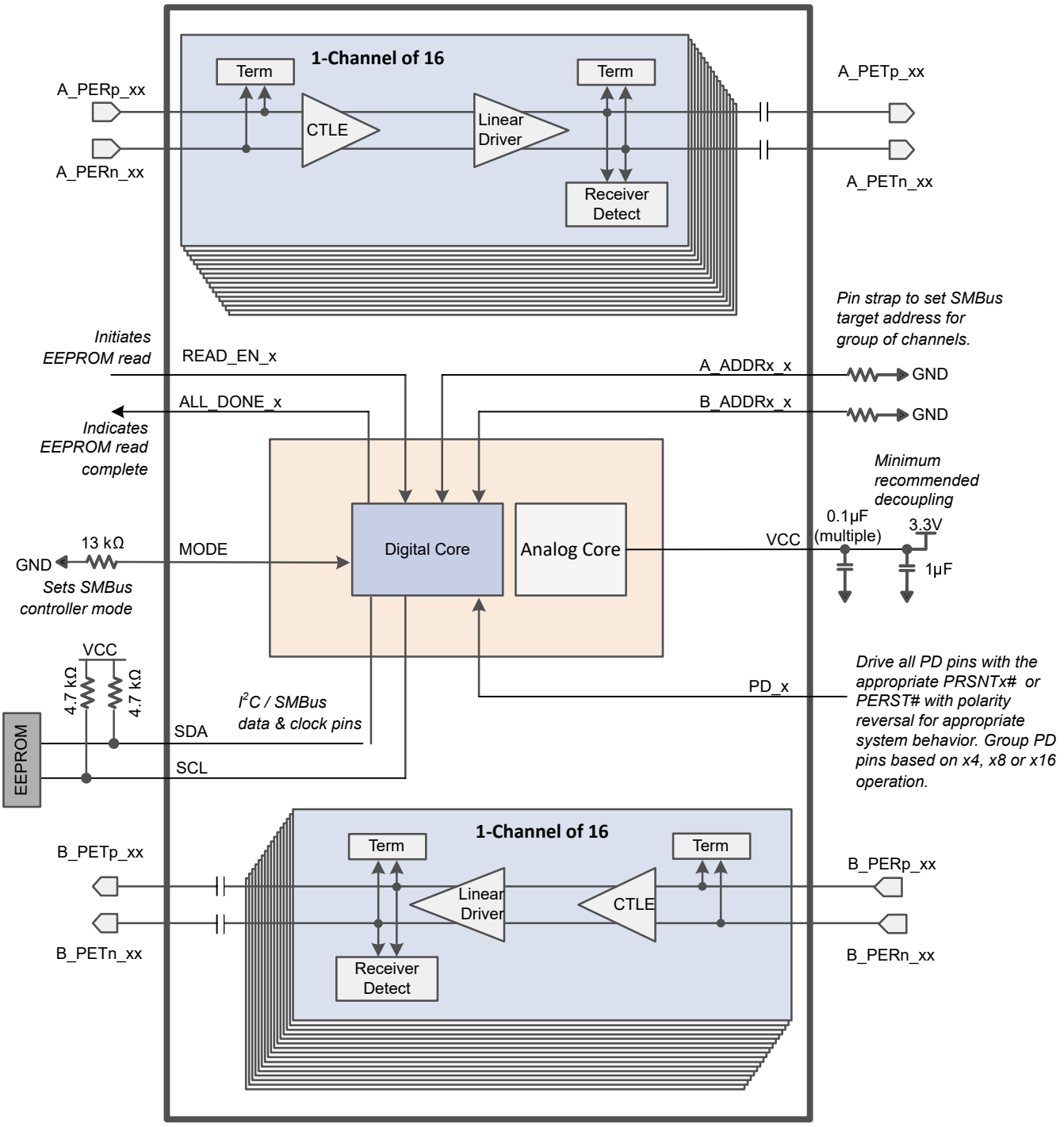


图 9-2. Simplified Schematic for PCIe x16 Lane Configuration in SMBus/I²C Controller Mode

9.2.1.3 Application Curves

The DS320PR1601 is a linear redriver that can be used to extend channel reach of a PCIe link. Normally, PCIe-compliant Tx and Rx are equipped with signal-conditioning functions and can handle channel losses of up to 36 dB at 32 Gbps (16 GHz) PCIe 5.0. With the DS320PR1601, the total channel loss between a PCIe root complex and an end point can be extended up to 52 dB (18 dB additional) at 16 GHz.

To demonstrate the reach extension capability of the DS320PR1601, two comparative setups are constructed. In first setup as shown in 图 9-3 there is no redriver in the PCIe 5.0 link. 图 9-4 shows eye diagram at the end of the link using SigTest. In second setup as shown in 图 9-5, the DS320PR1601 is inserted in the middle to extend link reach. 图 9-6 shows SigTest eye diagram.

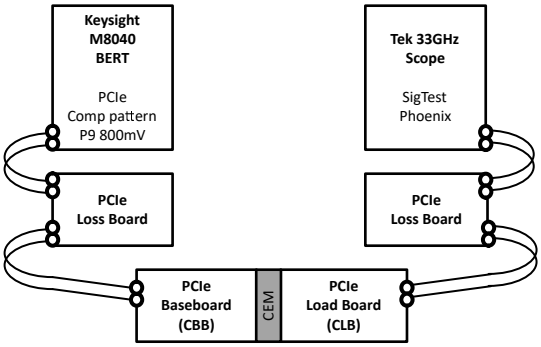


图 9-3. PCIe 5.0 Link Baseline Setup Without Redriver – the Link Elements

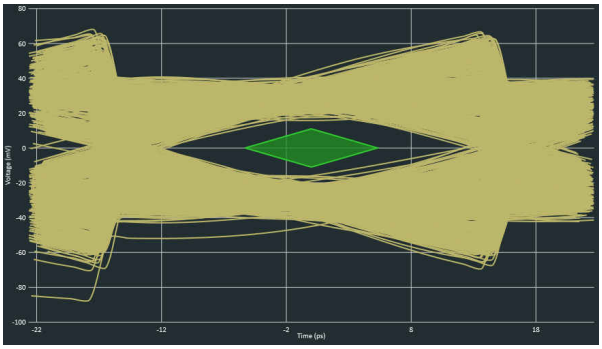


图 9-4. PCIe 5.0 link Baseline Setup Without Redriver – Eye Diagram Using SigTest

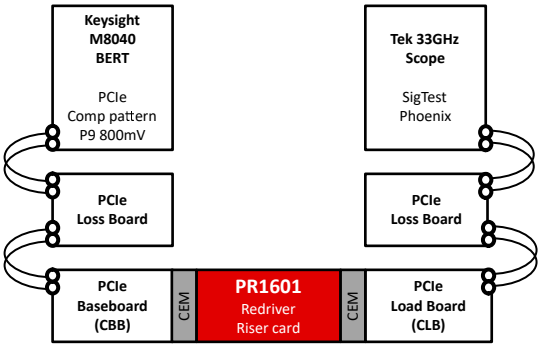


图 9-5. PCIe 5.0 Link Setup with the DS320PR1601 – the Link Elements

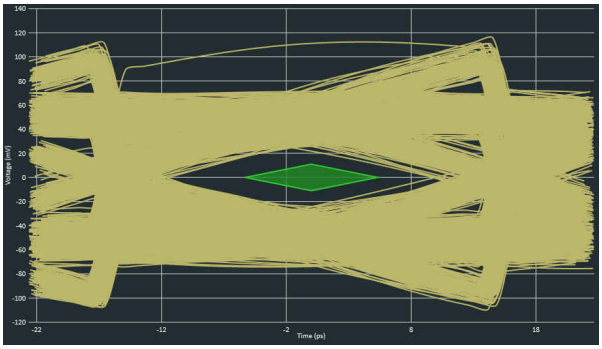


图 9-6. PCIe 5.0 Link Setup with the DS320PR1601 – Eye Diagram Using SigTest

表 9-1 provides the PCIe 5.0 links without and with the DS320PR1601. The illustration shows that redriver is capable of ≅18 dB (additional) reach extension at PCIe 5.0 speed with EQ = 12 (15 dB) and flat_gain = 011 (-1.2 dB). Note: actual reach extension depends on various signal integrity factors. It is recommended to run signal integrity simulations with all the components in the link to get any guidance.

表 9-1. PCIe 5.0 Reach Extension Using the DS320PR1601

Setup	Pre Channel Loss	Post Channel Loss	Total Loss	Eye at BER 1E-12	SigTest Pass?
Baseline – no DUT	—	—	≅36 dB	13.0 ps, 27.8 mV	Pass
With DUT (DS320PR1601)	≅27 dB	≅25 dB	≅52 dB	13.5 ps, 31.2 mV	Pass

9.3 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the operating conditions outlined in the *Recommended Operating Conditions* section in terms of DC voltage, AC noise, and start-up ramp time.
2. The DS320PR1601 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of adequate numbers of 0.1 µF capacitors near device VCC pins, several 1.0 µF and 10.0 bulk capacitors on VCC power plane. The local decoupling (0.1 µF) capacitors must be connected as close to the V_{CC} pins as possible and with minimal path to the DS320PR1601 ground pad. For more specific guidance, refer to *DS320PR1601RSC-EVM User's Guide*.

9.4 Layout

9.4.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VCC pins as possible. Placing the decoupling capacitors directly underneath the device is recommended if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most or all layers or by back drilling.
4. GND relief can be used (but is not required) beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.

9.4.2 Layout Example

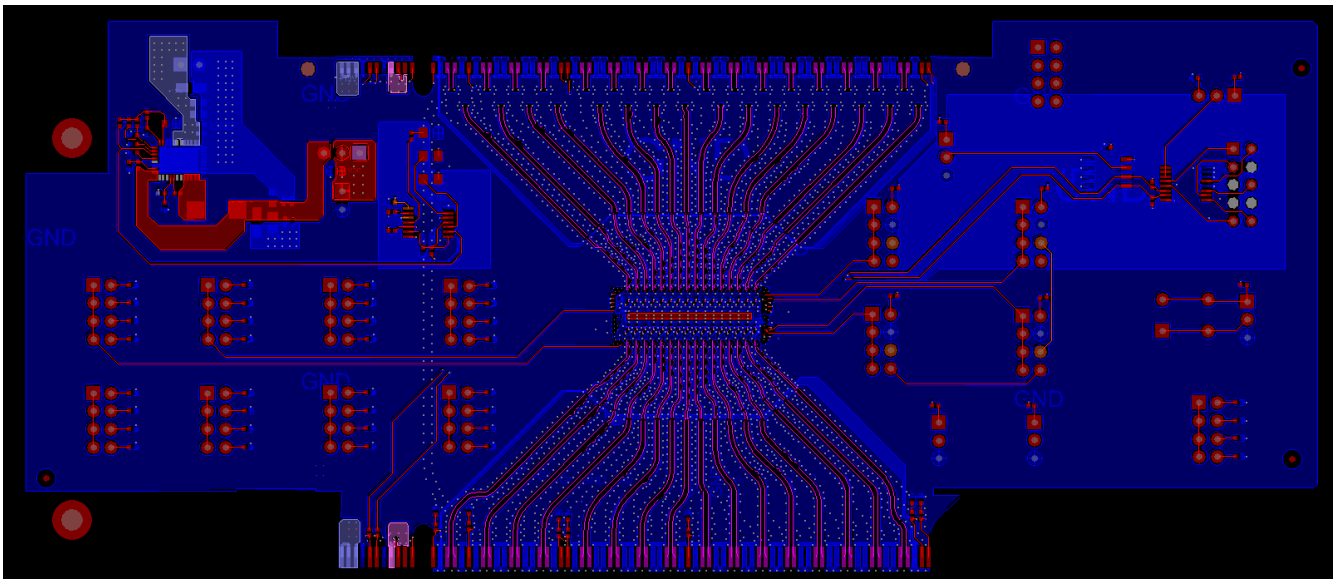


图 9-7. Top Layer View of TI PCIe Riser Card Using DS320PR1601 with CEM Connectors

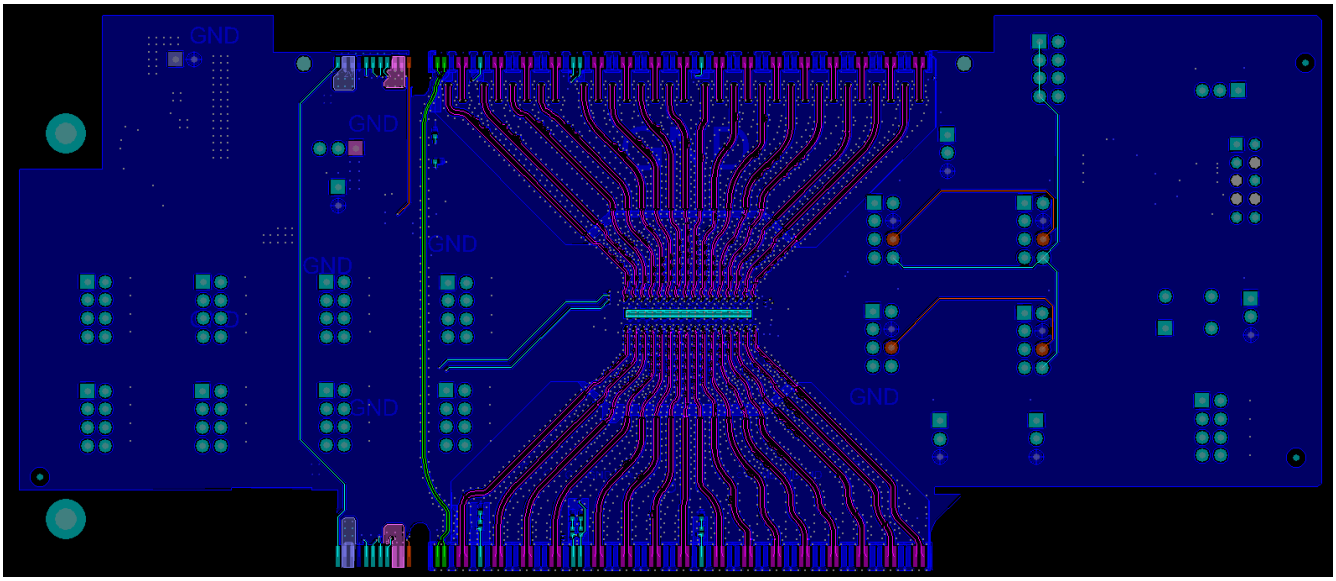


图 9-8. Bottom Layer View of TI PCIe Riser Card Using DS320PR1601 with CEM Connectors

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *DS320PR1601RSC-EVM User's Guide*
- Texas Instruments, *DS160PR1601 and DS320PR1601 Programming Guide*

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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所有商标均为其各自所有者的财产。

10.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS320PR1601ZDGR	ACTIVE	NFBGA	ZDG	354	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	PR16X	Samples
DS320PR1601ZDGT	ACTIVE	NFBGA	ZDG	354	250	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	PR16X	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

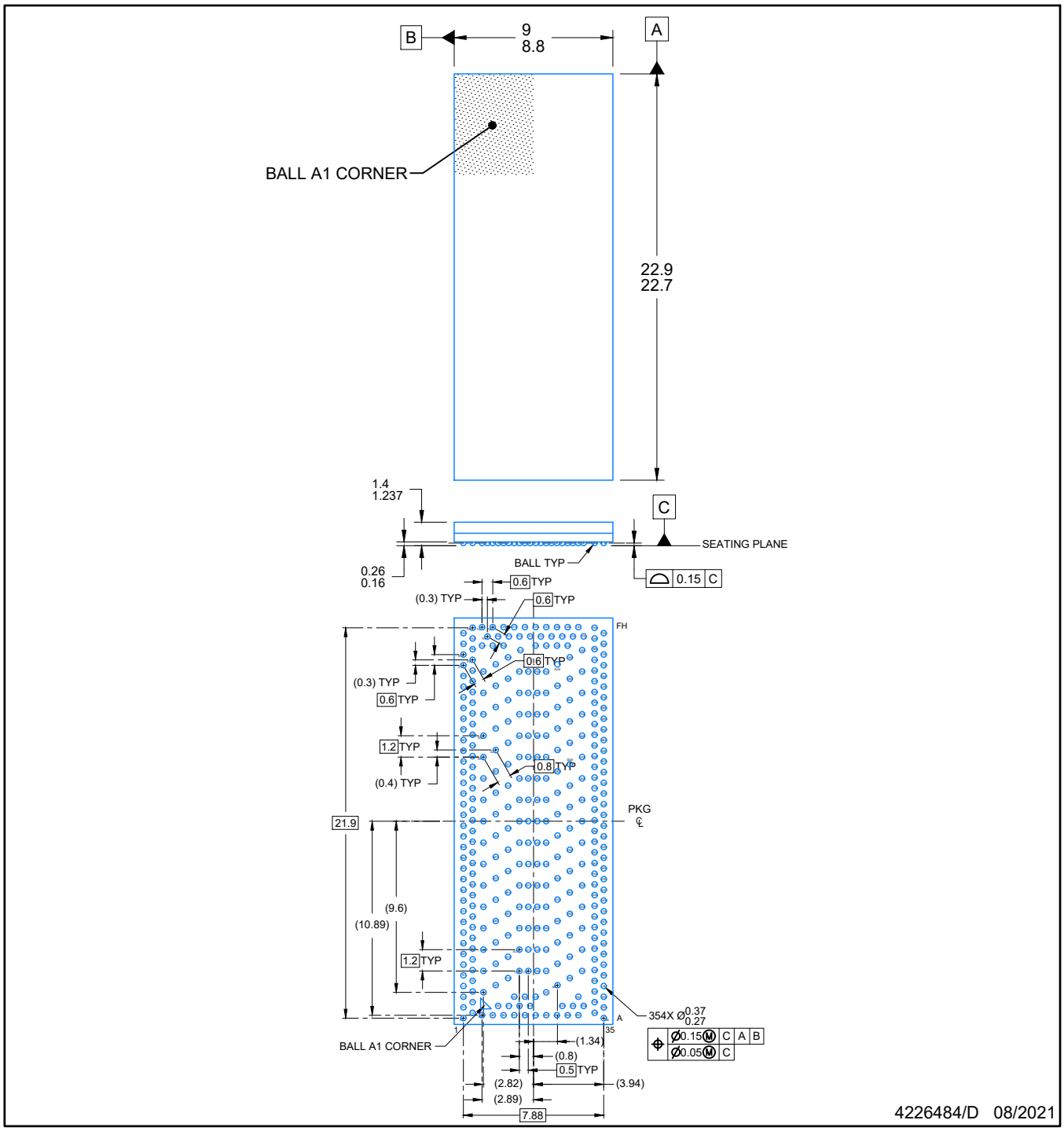
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

ZDG0354A

NFBGA - 1.4 mm max height

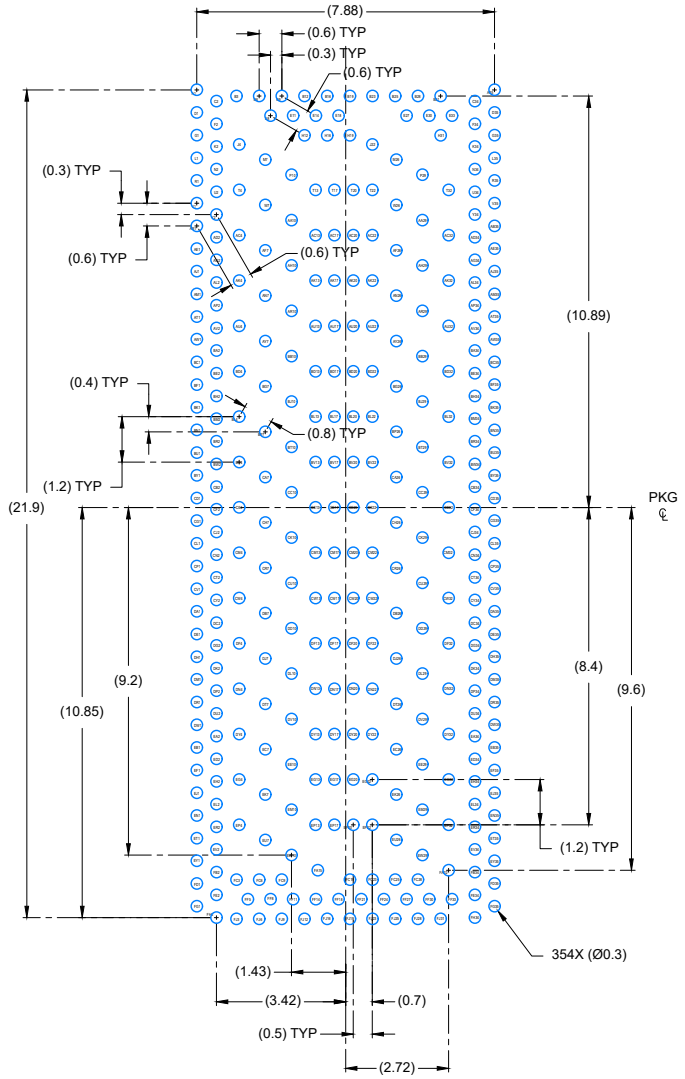
PLASTIC BALL GRID ARRAY



NOTES:

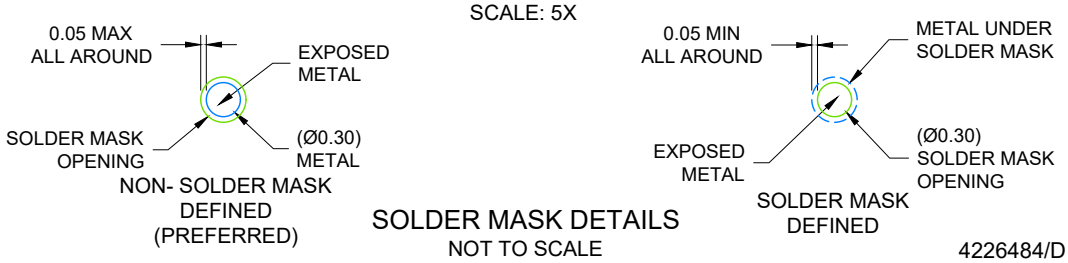
NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 5X



SOLDER MASK DETAILS

NOT TO SCALE

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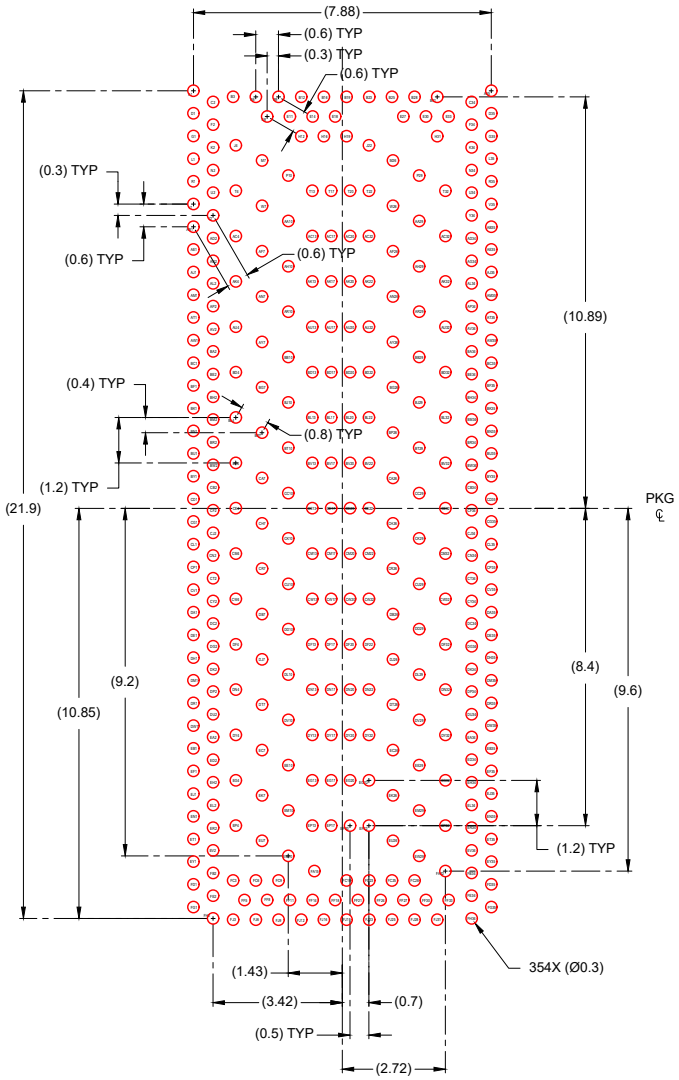
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL
SCALE: 5X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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