适用于高速接口的 ESDS302、ESDS304 数据线路浪涌和 ESD 保护器件

1 特性

- IEC 61000-4-2 4 级静电放电 (ESD) 保护
  - ±30kV 接触放电
  - ±30kV 气隙放电
- IEC 61000-4-4 瞬态放电 (EFT) 保护
  - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
  - 12A (8/20μs)
  - 低浪涌钳位电压在 12A Ipp 下为 6V
- IO 电容：
  - 2.3pF（典型值）
- 直流击穿电压：4.5V（最小值）
- 超低泄漏电流：3nA（典型值）
- 支持速率高达 1Gbps 的高速接口
- 工业温度范围：-40°C 至 +125°C
- 简易直通布线封装 (ESDS302)

2 应用

- 终端设备
  - 以太网交换机
  - 接入点
  - 网关
  - 打印机
  - 数字视频录像机 (DVR) 和网络视频录像机 (NVR)
- 接口
  - 以太网 10/100/1000Mbps
  - USB 2.0
  - 通用输入/输出 (GPIO)

3 说明

ESDS302、ESDS304 器件是分别采用两通道和四通道配置的双向 TVS ESD 保护二极管阵列，用于高达 12A (8/20μs) 的以太网和 USB 浪涌保护。ESDS302、ESDS304 器件的额定 ESD 冲击消散值高达 30kV，符合 IEC 61000-4-2 国际标准（> 4 级）。

这些器件 每通道 具有 2.3pF IO 电容，因此非常适用于保护高速接口（如以太网 1G 和 USB 2.0）。低动态电阻和低钳位电压确保系统级抗瞬变事件保护。

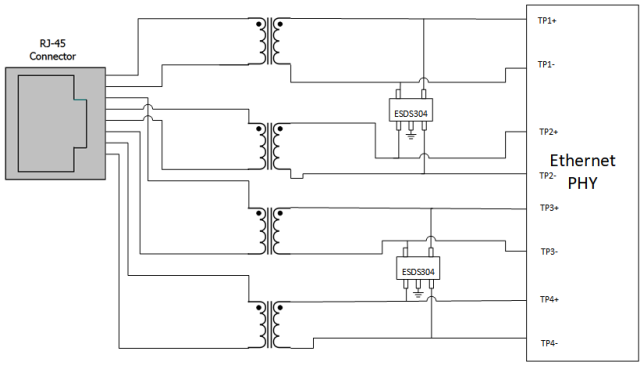
ESDS302、ESDS304 器件采用符合行业标准的 5 引脚 SOT23 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ESDS302	SOT23 (5)；2 NC 引脚	2.90mm x 1.6mm x 1.25mm
ESDS304	SOT23 (5)	2.90mm x 1.6mm x 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用原理图



目录

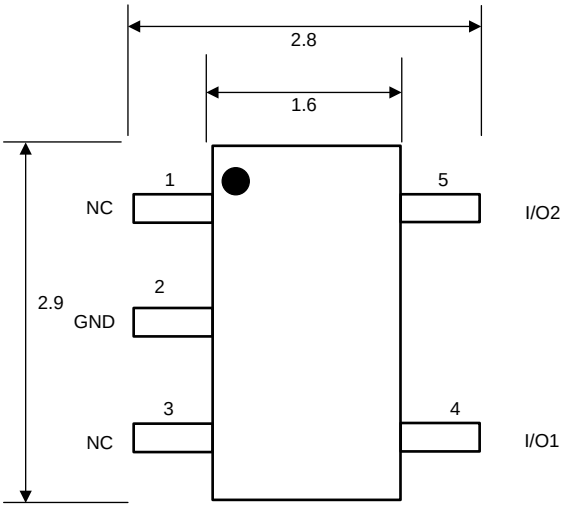
4 修订历史记录

Changes from Original (May 2018) to Revision A **Page**

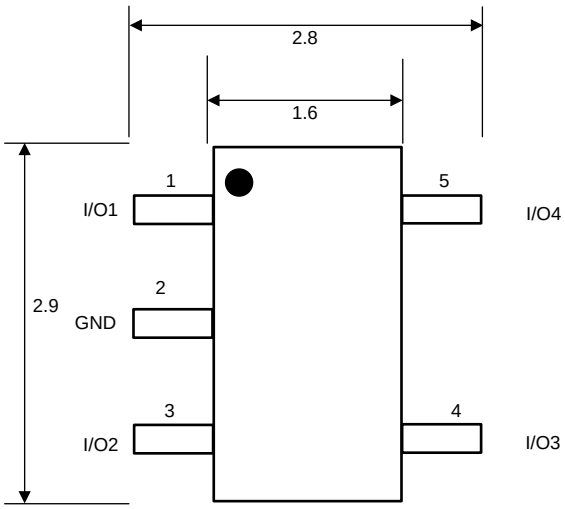
- 将数据表状态从“产品预览”更改成了“生产数据” ... 1
- 将 ESDS03802 和 ESDS03804 器件型号更改成了 ESDS302 和 ESDS304 ... 1

5 Pin Configuration and Functions

ESDS302 DBV Package
5-Pin SOT23
Top View



ESDS304 DBV Package
5-Pin SOT23
Top View



Pin Functions for ESDS302

PIN		TYPE	DESCRIPTION
NAME	NO.		
I/O1	4	I/O	Surge/ESD protected channels. Connect to the lines being protected.
I/O2	5		
GND	2	GND	Ground. Connect to ground
NC	1	NC	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	3		

Pin Functions for ESDS304

PIN		TYPE	DESCRIPTION
NAME	NO.		
I/O1	1	I/O	Surge/ESD protected channels. Connect to the lines being protected.
I/O2	3		
I/O3	4		
I/O4	5		
GND	2	GND	Ground. Connect to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IEC 61000-4-4 Electrical Fast Transient	Peak Power at 25 °C		80	A
IEC 61000-4-5 Surge (t_p 8/20 µs	Peak Power at 25 °C		85	W
	Peak Current at 25 °C		12	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings -JEDEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±2500	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 500-V HBM is possible with the necessary precautions. [Following sentence optional; see the wiki.] Pins listed as ±WWW V and/or ±XXX V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 250-V CDM is possible with the necessary precautions. [Following sentence optional; see the wiki.] Pins listed as ±YYY V and/or ±ZZZ V may actually have higher performance.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0		3.6	V
T_A	Operating Free Air Temperature	–40		125	°C

6.5 Thermal Information

THERMAL METRIC(1)		ESDS302 DBV (SOT-23) 5 PINS	ESDS304 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	176.2	133.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	125.7	85.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	88.4	49.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	71.4	30.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	88.2	49.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

At TA = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 500 nA, across operating temperature range			3.6	V
$I_{LEAKAGE}$	Leakage current at 3.6 V	V_{IO} = 3.6 V, Any IO pin to GND		3	50	nA
V_{BRF}	Breakdown voltage, Any IO pin to GND (1)	I_{IO} = 1 mA	4.5		7.5	V
V_{FWD}	Diode forward voltage, GND to IO pin	I_{IO} = 1 mA		0.8		V
V_{HOLD}	Holding voltage, Any IO pin to GND (2)	I_{IO} = 1 mA		5		V
V_{CLAMP}	Surge Clamping voltage, t_p = 8/20 µs	I_{PP} = 1 A, Any IO pin to GND		5.1		V
		I_{PP} = 12 A, Any IO pin to GND		6		V
		I_{PP} = 1 A, GND to any IO pin		1.2		V
		I_{PP} = 12 A, GND to any IO pin		3		V
	TLP Clamping Voltage, t_p = 100 ns	I_{PP} = 16 A, any IO to GND pin		5.8		V
		I_{PP} = 16 A, GND to any IO pin		3.1		V
C_{LINE}	Line capacitance, any IO to GND	V_{IO} = 0 V, V_{p-p} = 30 mV, f = 1 MHz		2.3	2.8	pF
ΔC_{LINE}	Variation of line capacitance	C_{LINE1} - C_{LINE2}, V_{IO} = 0 V, Vp-p = 30 mV, f = 1 MHz		0.05	0.1	pF
C_{CROSS}	Line-to-line capacitance	V_{IO} = 0V, V_{rms} = 30 mV, f = 1 MHz		1.25	1.5	pF

(1) V_{BRF} is defined as the max voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state
(2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

6.7 Typical Characteristics

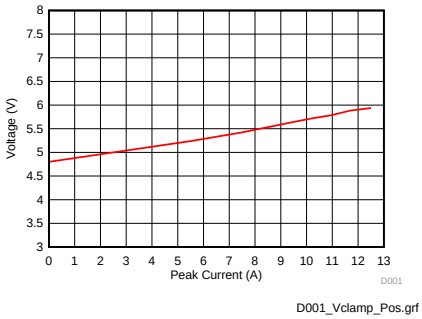


图 1. Surge Clamping Voltage vs. Peak Pulse Current (IEC 61000-4-5, tp = 8/20 µs), Any IO Pin to GND

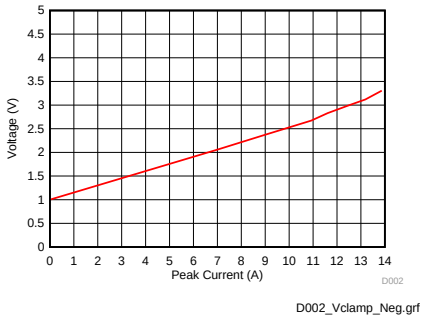


图 2. Surge Clamping Voltage vs. Peak Pulse Current (IEC 61000-4-5, tp = 8/20 µs), GND to IO Pin

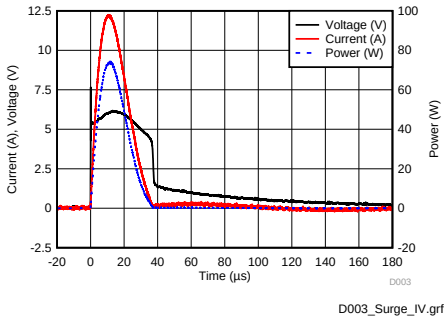


图 3. Surge Current, Clamping Voltage and Power Waveform (IEC-61000-4-5, t_p = 8/20 µs), Any IO Pin to GND

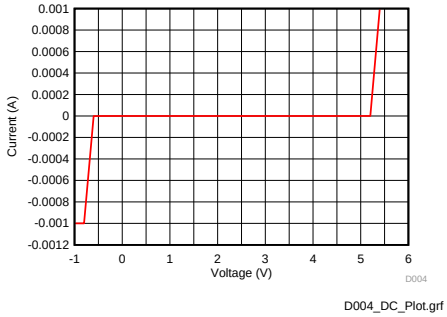


图 4. DC I-V Curve

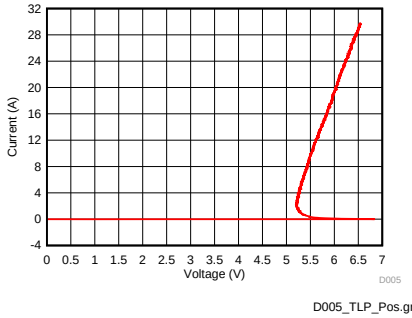


图 5. TLP I-V Curve, IO to GND, t_p = 100 ns

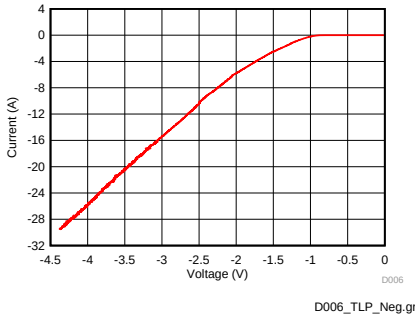


图 6. TLP I-V Curve, IO to GND Negative, t_p = 100 ns

Typical Characteristics (接下页)

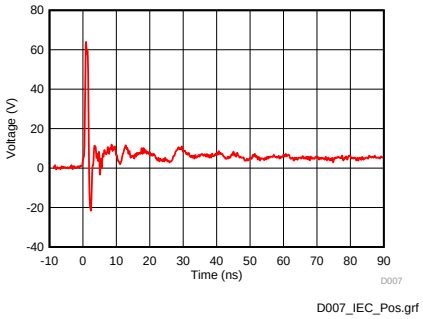


图 7. +8 kV IEC 61000-4-2 Clamping Voltage Waveform, IO Pin to GND

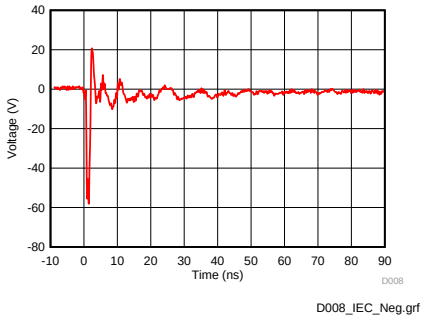


图 8. -8 kV IEC 61000-4-2 Clamping Voltage Waveform, IO Pin to GND

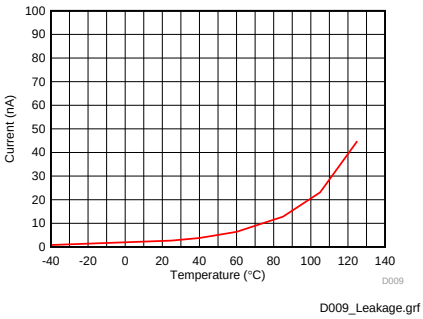


图 9. DC Leakage Current vs. Ambient Temperature, Bias Voltage = 3.6 V

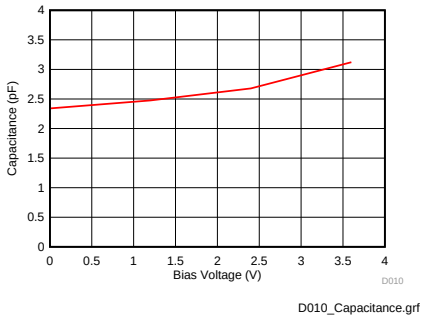


图 10. Capacitance vs. Bias Voltage at 25°C

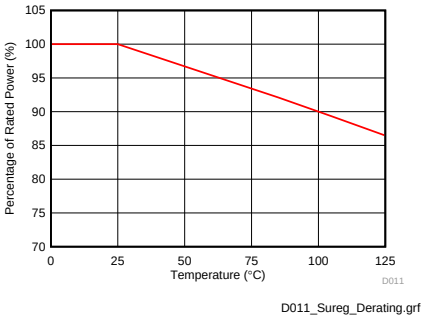


图 11. Surge Power Derating with Respect to Ambient Temperature

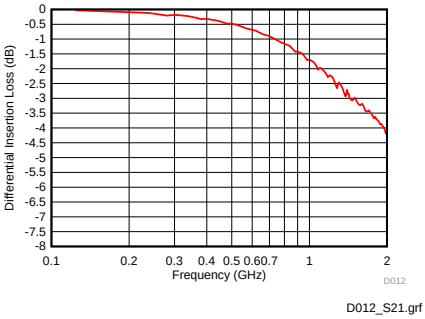


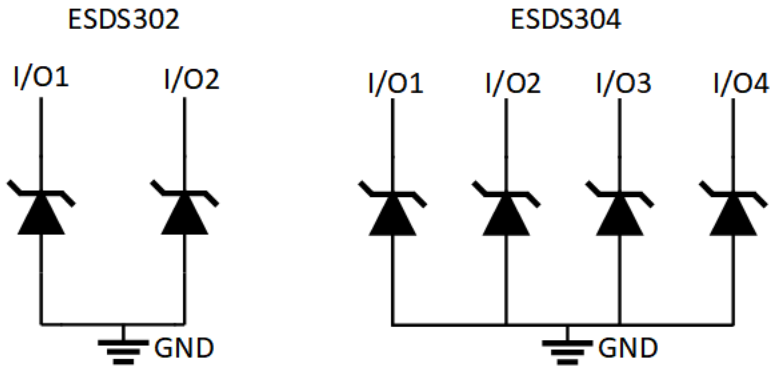
图 12. Differential Insertion Loss vs. Frequency

7 Detailed Description

7.1 Overview

The ESDS304, ESDS302 devices are uni-directional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins.

7.2 Functional Block Diagram



7.3 Feature Description

The I/O pins of ESDS304 and ESDS302 can withstand surge events (IEC 61000-4-5, 8/20 μs waveform) up to 12 A and 85 W. These devices also provide ESD protection up to ±30-kV contact and ±30-kV air gap per IEC 61000-4-2 standard. The I/O pins can withstand an electrical fast transient burst of up to 80 A (IEC 61000-4-4 5/50 ns waveform, 4 kV with 50-Ω impedance). The capacitance between each I/O pin to ground is 2.3 pF (typical) and 2.8 pF (maximum). This device supports data rates up to 1 Gbps. The reverse DC breakdown voltage of each I/O pin is a minimum of 4.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 3.6 V. The I/O pins feature an ultra-low leakage current of 50 nA (maximum) with a bias of 3.6 V. This device features an industrial operating range of –40°C to +125°C.

7.4 Device Functional Modes

The ESDS304, ESDS302 devices are a passive integrated circuit that triggers when voltages are above V_{BRF} or below 0.7 V. During ESD events, voltages as high as ±30 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESDS304, ESDS302 (usually within a few nano-seconds) the devices reverts to passive.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ESDS304, ESDS302 devices are diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

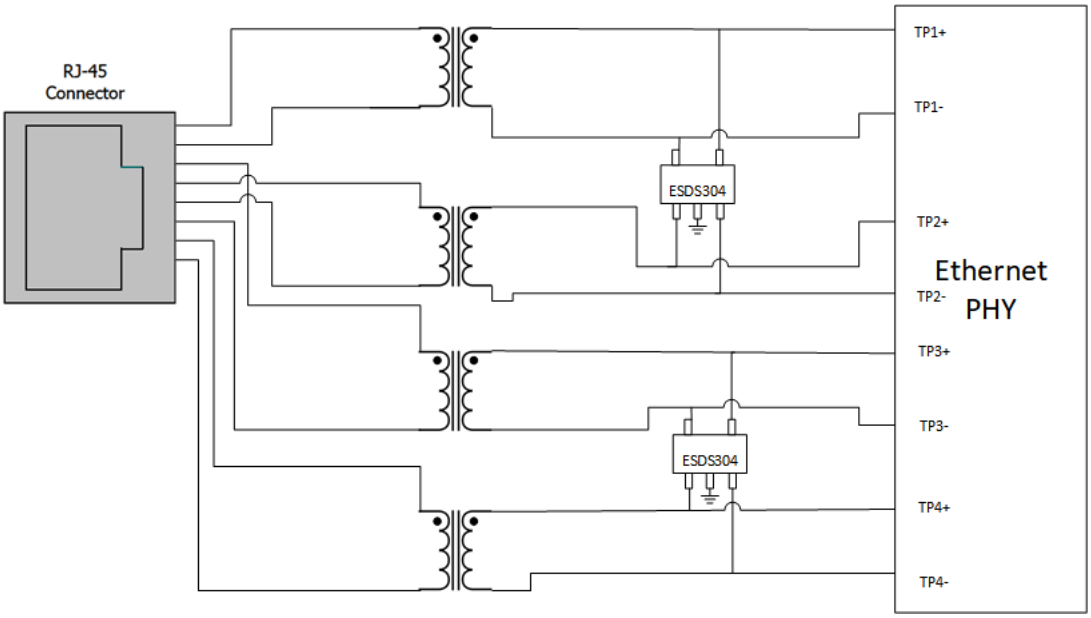


图 13. ESDS304 Protecting the Ethernet 1G Interface

8.2.1 Design Requirements

A typical operation for the ESDS304 would be protecting a high speed dataline similar to one shown in 图 13. In this example, the ESDS304 is protecting an Ethernet PHY's data lines that has a nominal operating voltage of 3.6 V. Many of the Ethernet interfaces that connect to long cables require protection against ±1 kV surge test through a 42-Ω coupling resistor and a 0.5 μF capacitor, equaling roughly 24 A of surge current. Without any input protection, if a surge event is caused by lightning, coupling, ringing, or any other fault condition, this input voltage will rise to hundreds of volts for multiple microseconds, harming the device. For Ethernet 1000Base-T (1Gbps), application design parameters listed in 表 1 are known.

表 1. Design Parameters

DESIGN PARAMETER	VALUE
Single ended signal voltage range on differential data line pairs	0 to 3.6 V
Operating Frequency	125 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The ESDS304 has 4 identical surge protection channels with each channel supporting a signal range of 0 to 3.6 V. The device will work well with any Ethernet PHY that drives the single ended voltage on the data line up to a 3.6 V.

8.2.2.2 Operating Frequency

The ESDS304 has a capacitance of 2.3 pF (typical) and can support the 125 MHz operation of Ethernet 1000Base-T application

8.2.3 Application Curves

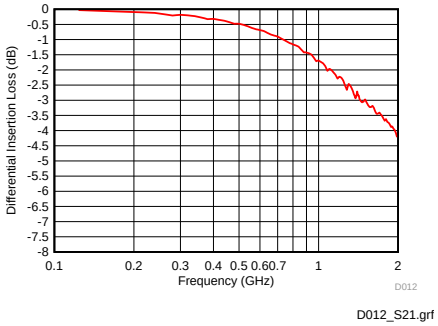


图 14. Differential Insertion Loss vs. Frequency

9 Power Supply Recommendations

The ESDS304, ESDS302 devices are passive ESD devices and there is no need to power them. Take care not to violate the recommended I/O specification (0 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Examples

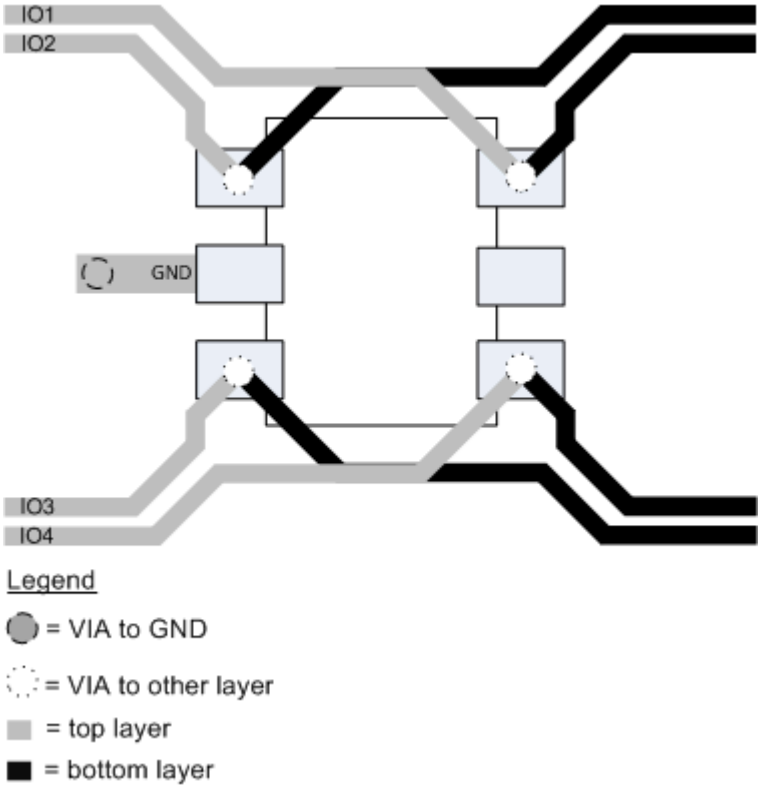


图 15. Layout Example for the 4-channel Device, ESDS304

11 器件和文档支持

11.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
ESDS302	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ESDS304	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

E2E is a trademark of Texas Instruments.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESDS302DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1R5B	Samples
ESDS304DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1R3B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

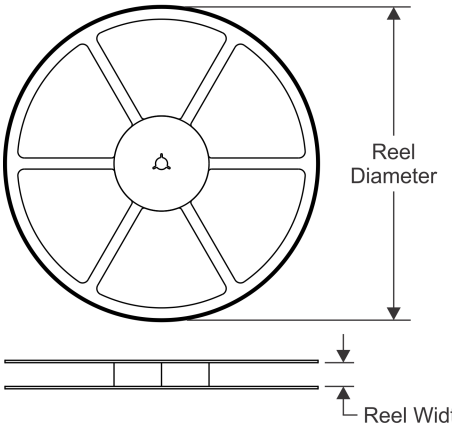
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

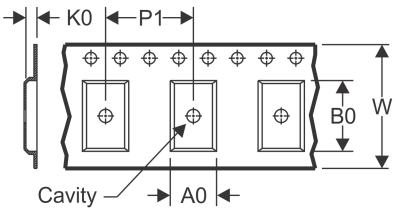
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

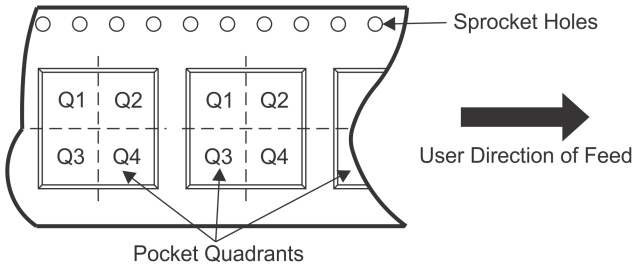


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

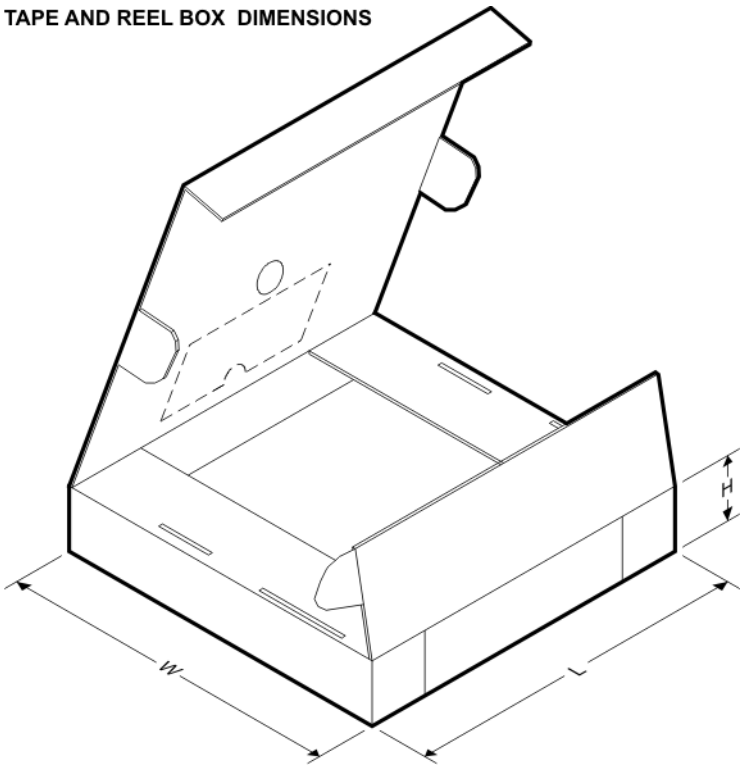
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESDS302DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
ESDS304DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

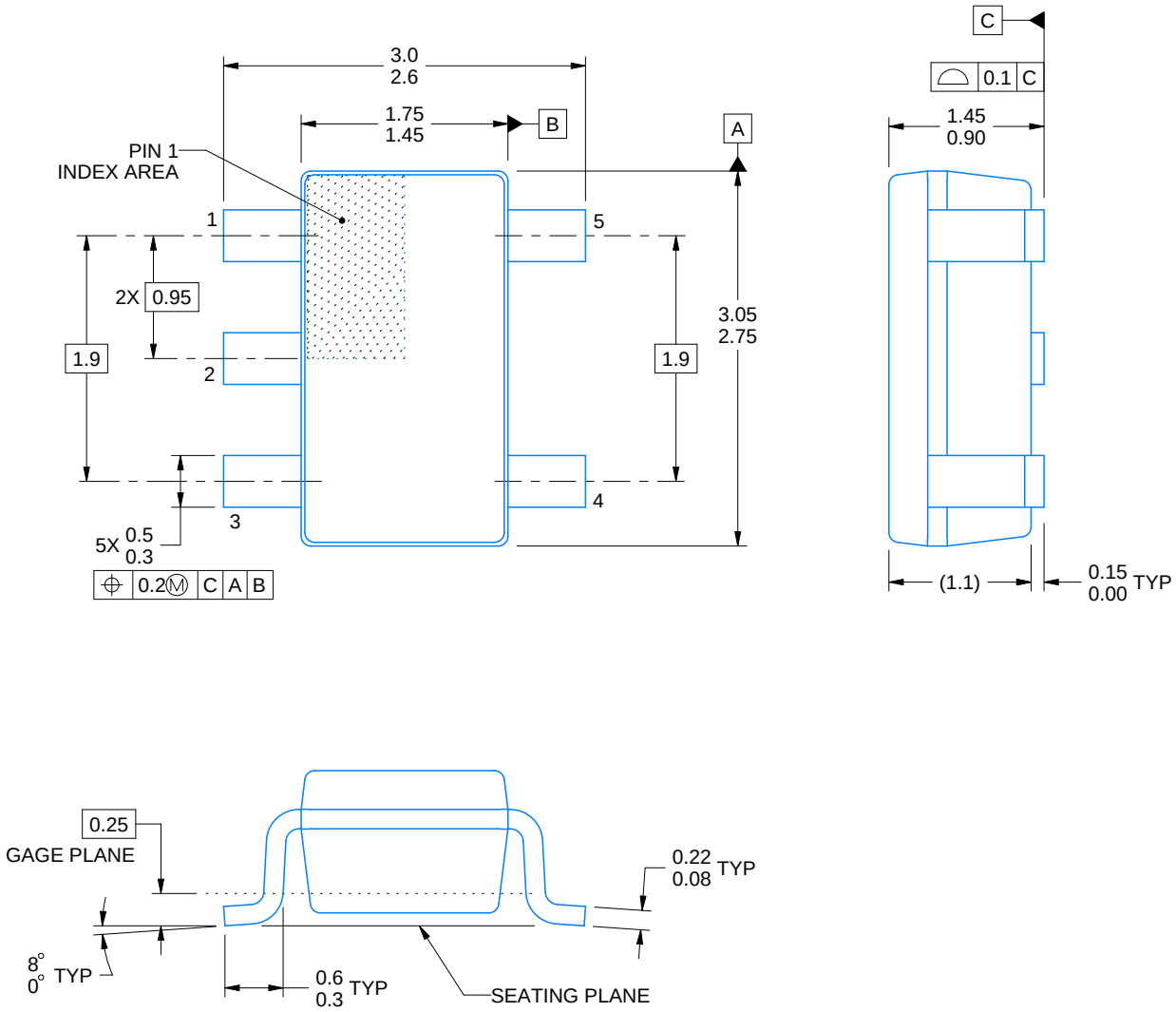
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESDS302DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
ESDS304DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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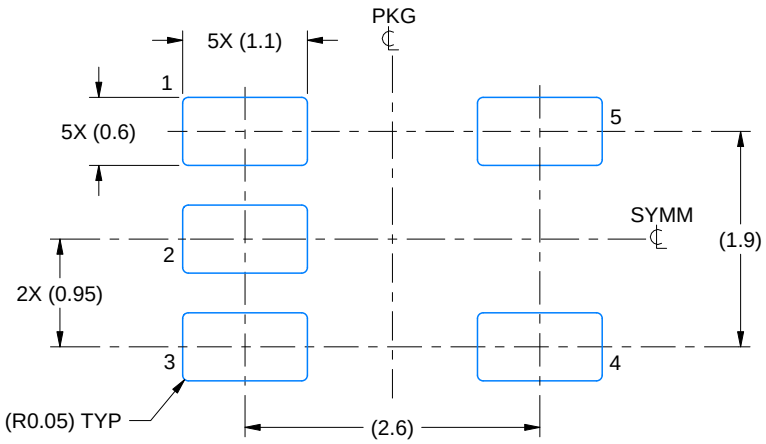
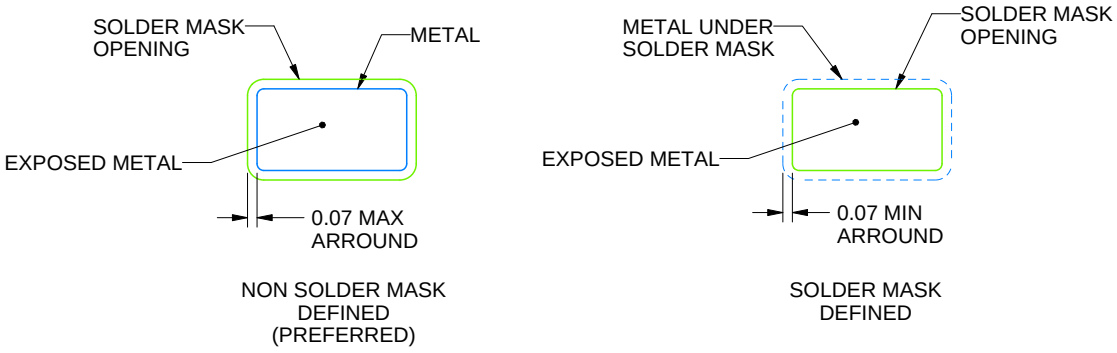
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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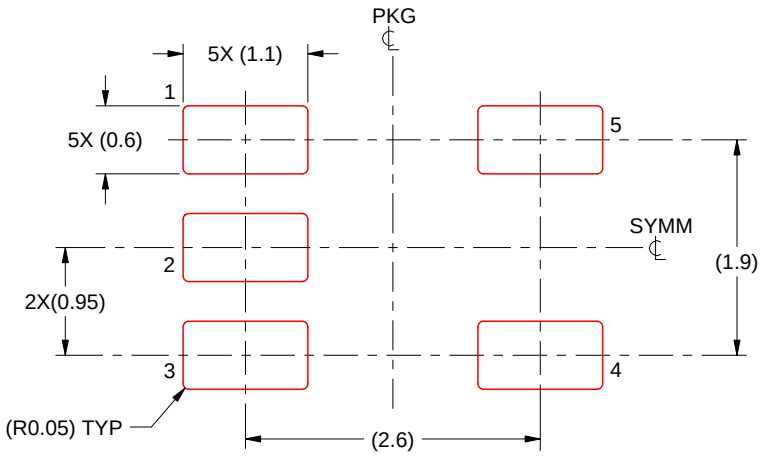
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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