TMS320F280013x Real-Time Microcontrollers

1 Features

- Real-time processing
  - 120-MHz C28x 32-bit DSP CPU
  - Equivalent to 240-MHz Arm® Cortex®-M7 based device on real-time signal chain performance (see the *Real-time Benchmarks Showcasing C2000™ Control MCU's Optimized Signal Chain* Application Note)
  - Floating Point Unit (FPU) for more precise mathematical calculations
  - Trigonometric Math Unit (TMU) speeds up algorithms key to real-time control systems
- On-chip memory
  - 256KB (128KW) of single bank flash (ECC-protected)
  - 36KB (18KW) of RAM (ECC/Parity-protected)
  - Security
    - JTAGLOCK
    - Zero-pin boot
    - Dual-zone security
- Clock and system control
  - Two internal 10-MHz oscillators
  - External resistor support for improved internal oscillator performance (ExtR)
  - Crystal oscillator or external clock input
  - Windowed watchdog timer module
  - Missing clock detection circuitry
  - Dual-clock Comparator (DCC)
- 3.3-V I/O design
  - Internal VREG generation
  - Brownout reset (BOR) circuit
- System peripherals
  - 38 individually programmable multiplexed General-Purpose Input/Output (GPIO) pins (11 shared with Analog)
  - 10 digital inputs on analog pins
  - Enhanced Peripheral Interrupt Expansion (ePIE)
  - Multiple low-power mode (LPM) support
  - Unique Identification (UID) number
- Communications peripherals
  - Two Inter-integrated Circuit (I2C) interfaces
  - One Controller Area Network (CAN/DCAN) bus port
  - One Serial Peripheral Interface (SPI) port
  - Three UART-compatible Serial Communication Interface (SCI)
- Analog system
  - Two 4-MSPS, 12-bit Analog-to-Digital Converters (ADCs)
    - Up to 21 external channels (11 shared with GPIO)
    - Four integrated Post-Processing Blocks (PPB) per ADC
  - One windowed comparator (CMPSS) with 12-bit reference Digital-to-Analog Converters (DACs)
    - Digital glitch filters
    - COMPDACOUT (11-bit)
  - Three windowed comparators (CMPSS_LITE) with 9.5-bit effective reference DACs
    - Digital glitch filters
- Enhanced control peripherals
  - 14 ePWM channels with two channels that have high-resolution capability (150-ps resolution)
    - Integrated dead-band support
    - Integrated hardware trip zones (TZs)
  - Two Enhanced Capture (eCAP) modules
  - One Enhanced Quadrature Encoder Pulse (eQEP) module with support for CW/CCW operation modes
  - Embedded Pattern Generator (EPG)
- CMAC Keys (128-bits) for SW AES
- Package options:
  - 64-pin Low-profile Quad Flatpack (LQFP) [PM suffix]
  - 48-pin LQFP [PT suffix]
  - 48-pin Very Thin Quad Flatpack No Lead (VQFN) [RGZ suffix]
  - 32-pin VQFN [RHB suffix]
- Temperature options:
  - Ambient (T_A): –40°C to 125°C

2 Applications

- Appliances
  - Air conditioner outdoor unit
    - For C2000 solution, see the Air-conditioner Outdoor Unit section.
  - Washer & dryer
    - For C2000 solution, see the Washer and Dryer section.
  - Robotic lawn mower
    - For C2000 solution, see the Robotic Lawn Mower section.

  - Merchant telecom rectifiers
    - For C2000 solution, see the Merchant Telecom Rectifiers section.
  - Appliances pumps & fans
  - Appliances: compressor
  - Cordless handheld garden tool
  - Cordless power tool
  - Lawn mower
  - Mains powered tools
  - Cooker hood
  - Dishwasher
  - Refrigerator & freezer
  - Air conditioner indoor unit
  - Vacuum robot
  - Air purifier & humidifier
  - Cordless vacuum cleaner
  - Mixer, blender & food processor
  - Residential & living fan
- Building automation
  - Automated door & gate
  - HVAC motor control
- Factory automation & control
  - Actuator
  - Automated sorting equipment
- Mobile robot motor controller
  - Textile machine
- Motor drives
  - AC drive control module
  - AC drive power stage module
  - Linear motor power stage
  - Drone propeller ESC
  - Servo drive control module
  - Servo drive power stage module
  - AC-input BLDC motor drive
  - DC-input BLDC motor drive
  - Closed loop stepper
  - Open loop stepper
- Industrial power
  - Industrial AC-DC
- Portable power station
  - UPS
- Single-phase line interactive UPS
  - Single-phase online UPS
- Telecom & server power
  - Merchant DC/DC
  - Merchant network & server PSU
  - Merchant telecom rectifiers
    - See Merchant Telecom Rectifiers section.
- Grid infrastructure
  - Micro inverter
  - Rapid shutdown
  - Solar arc protection
  - Solar charge controller
  - Solar power optimizer

3 Description

The TMS320F280013x (F280013x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics.

The real-time control subsystem is based on TI's 32-bit C28x DSP core, which provides 120 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the Trigonometric Math Unit (TMU), speeding up common algorithms key to real-time control systems.

The F280013x supports up to 256KB (128KW) of flash memory. Up to 36KB (18KW) of on-chip SRAM is also available to supplement the flash memory.

High-performance analog blocks are integrated into the F280013x real-time microcontroller (MCU) and are closely coupled with the processing and PWM units to provide optimal real-time signal chain performance. Fourteen PWM channels enable control of various power stages from a 3-phase inverter to power-factor correction and other advanced multilevel power topologies.

Interfacing is supported through various industry-standard communication ports (such as SPI, SCI, I2C, and CAN) and offers multiple pin-muxing options for optimal signal placement.

Want to learn more about features that make C2000 MCUs the right choice for your real-time control system? Check out *The Essential Guide for Developing With C2000™ Real-Time Microcontrollers* and visit the C2000™ real-time control MCUs page.

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the TMDSCNCD2800137 evaluation board and download C2000Ware.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
TMS320F2800137	PM (LQFP, 64)	12 mm × 12 mm	10 mm × 10 mm
	PT (LQFP, 48)	9 mm × 9 mm	7 mm × 7 mm
	RGZ (VQFN, 48)	7 mm × 7 mm	7 mm × 7 mm
	RHB (VQFN, 32)	5 mm × 5 mm	5 mm × 5 mm
TMS320F2800135	PM (LQFP, 64)	12 mm × 12 mm	10 mm × 10 mm
	PT (LQFP, 48)	9 mm × 9 mm	7 mm × 7 mm
	RGZ (VQFN, 48)	7 mm × 7 mm	7 mm × 7 mm
	RHB (VQFN, 32)	5 mm × 5 mm	5 mm × 5 mm
TMS320F2800133	PM (LQFP, 64)	12 mm × 12 mm	10 mm × 10 mm
	PT (LQFP, 48)	9 mm × 9 mm	7 mm × 7 mm
	RGZ (VQFN, 48)	7 mm × 7 mm	7 mm × 7 mm
	RHB (VQFN, 32)	5 mm × 5 mm	5 mm × 5 mm
TMS320F2800132	PT (LQFP, 48)	9 mm × 9 mm	7 mm × 7 mm
	RGZ (VQFN, 48)	7 mm × 7 mm	7 mm × 7 mm
	RHB (VQFN, 32)	5 mm × 5 mm	5 mm × 5 mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER(1)	PACKAGE OPTIONS	FREQUENCY	FLASH SIZE	INTERNAL VOLTAGE REGULATOR	EXTERNAL VOLTAGE REGULATOR
TMS320F2800137	64 PM 48 PT 48 RGZ 32 RHB	120	256KB	Yes	No
TMS320F2800135	64 VPM 64 PM 48 PT 48 RGZ 32 RHB	120	128KB	Yes	64 VPM only
TMS320F2800133	64 PM 48 PT 48 RGZ 32 RHB	120	64KB	Yes	No
TMS320F2800132	48 PT 48 RGZ 32 RHB	100	64KB	Yes	No

(1) For more information on these devices, see the Device Comparison table.

3.1 Functional Block Diagram

The Functional Block Diagram shows the CPU system and associated peripherals.

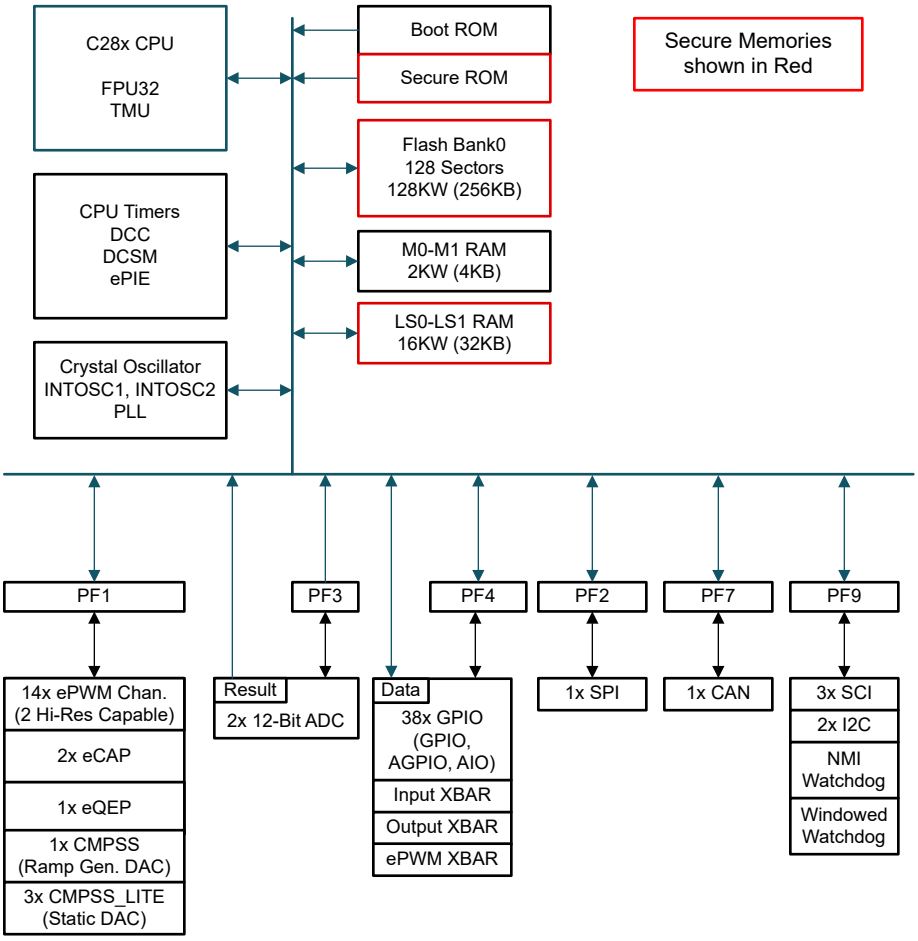

Figure 3-1. Functional Block Diagram

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4 Device Comparison

Table 4-1 lists the features of the TMS320F280013x devices.

Table 4-1. Device Comparison

FEATURE[1]		F2800137	F2800135	F2800133	F2800132
PROCESSOR AND ACCELERATORS					
C28x	Frequency (MHz)	120			100
	FPU32 - Type 0	Yes			
	TMU – Type 0	Yes			
MEMORY					
Flash		256KB (128KW)	128KB (64KW)	64KB (32KW)	
RAM		36KB (18KW)			
Security: JTAGLOCK, Zero-pin boot, Dual-zone security		Yes			
SYSTEM					
32-bit CPU timers		3			
Watchdog-timer		1			
Dual Clock Compare (DCC)		1			
External Interrupts		5			
Embedded Pattern Generator (EPG)		1			
Nonmaskable Interrupt Watchdog (NMIWD) timers		1			
Crystal oscillator/External clock input		1			
INTOSC with ExtR accuracy[4]		+/- 1%			
Internal oscillator accuracy (2 INTOSC)		See Section 6.11.3.5			
Internal 3.3-V to 1.2-V Voltage Regulator (VREG)		Yes			
External VREG Support Using VREGENZ		-	64 VPM only	-	
GPIO		See Section 5.5			
ANALOG PERIPHERALS					
ADC 12-bit	Number of ADCs	2			
	Conversion-time (ns)[2]	250 ns / 4.00 MSPS			290 ns / 3.45 MSPS
	ADC channels	See Section 5.5			
Temperature sensor		1			
Comparator Subsystem	CMPSS (each includes two comparators and two internal dynamic 12-bit DACs)	1			
	CMPSS_LITE (each includes two comparators and two static 9.5-bit effective DACs)	3			
CONTROL PERIPHERALS[3]					
eCAP modules – Type 2		2			
ePWM/HRPWM – Type 4	Total Channels	14			6
	Channels with high-resolution capability	2 (ePWM1)			
eQEP modules – Type 2		1			

Table 4-1. Device Comparison (continued)

FEATURE(1)	F2800137	F2800135	F2800133	F2800132
COMMUNICATION PERIPHERALS(3)				
CAN – Type 0	1			–
I2C – Type 1	2			
SCI – Type 0 (UART-Compatible)	3			
SPI – Type 2	1			
PACKAGE, TEMPERATURE, AND QUALIFICATION OPTIONS				
64 PM	Yes	Yes		-
64 PM with VREGENZ (64 VPM)	-	Yes	-	
48 PT	Yes	Yes		
48 RGZ	Yes	Yes		
32 RHB	Yes	Yes		
Junction temperature (T_J)	–40°C to 140°C			
Free-Air temperature (T_A)	–40°C to 125°C			

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module.
(2) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.
(3) For devices that are available in more than one package, the peripheral count listed in the smaller package is reduced because the smaller package has fewer device pins available. The number of peripherals internally present on the device is not reduced compared to the largest package offered within a part number. See Section 5 to identify which peripheral instances are accessible on pins in the smaller package.
(4) See Section 6.11.3.5 for INTOSC accuracy values

4.1 Related Products

TMS320F2803x Real-Time Microcontrollers
The F2803x series increases the pin count and memory size options. The F2803x series also introduces the parallel control law accelerator (CLA) option.

TMS320F2807x Real-Time Microcontrollers
The F2807x series offers the most performance, largest pin counts, flash memory sizes, and peripheral options. The F2807x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

TMS320F28004x Real-Time Microcontrollers
The F28004x series is a reduced version of the F2807x series with the latest generational enhancements.

TMS320F2838x Real-Time Microcontrollers
The F2838x series offers more performance, larger pin counts, flash memory sizes, peripherals and a wide variety of connectivity options. The F2838x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

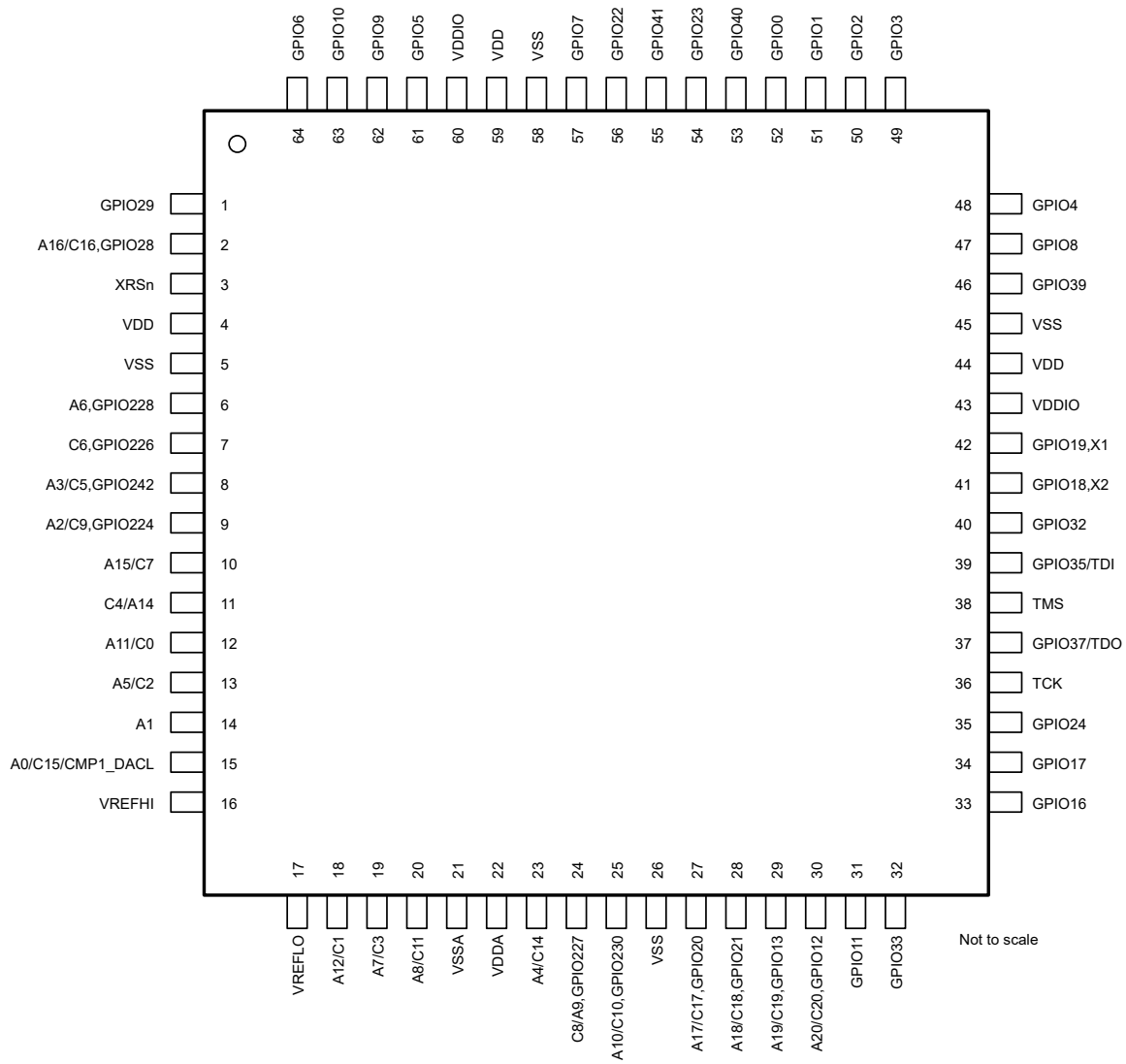
TMS320F28002x Real-Time Microcontrollers
The F28002x series is a reduced version of the F28004x series with the latest generational enhancements.

TMS320F28003x Real-Time Microcontrollers
The F28003x series builds upon the F28002x series offering higher frequency, more memory, and more peripheral options. CAN-FD and security features are introduced from the F2838x series.

5 Pin Configuration and Functions

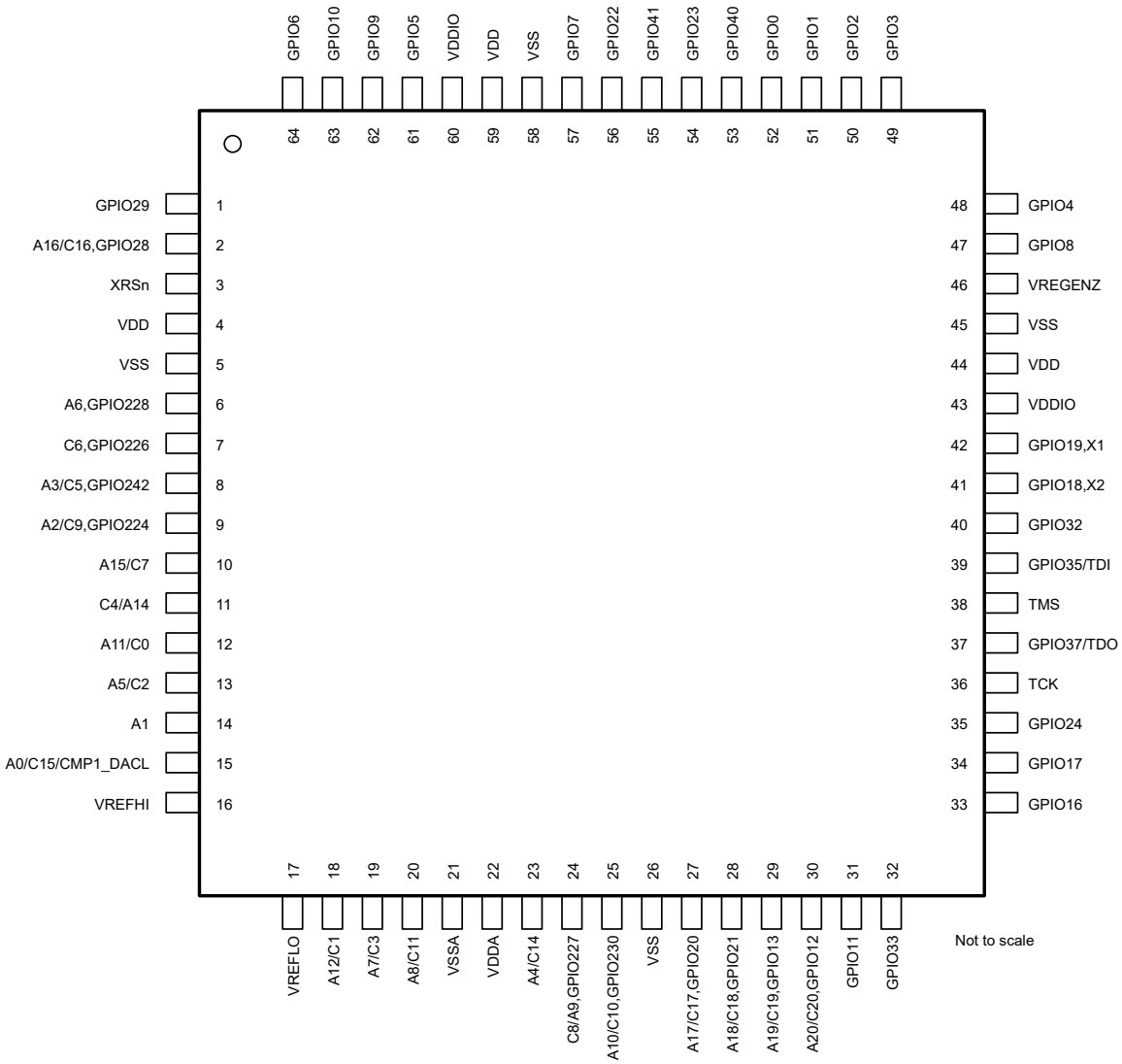
5.1 Pin Diagrams

Figure 5-1 shows the pin assignments on the 64-pin PM low-profile quad flatpack (LQFP). Figure 5-2 shows the pin assignments on the 64-pin PM LQFP *with VREGENZ*. Figure 5-3 shows the pin assignments on the 48-pin PT LQFP. Figure 5-4 shows the pin assignments on the 48-pin RGZ very thin quad flatpack no lead (VQFN). Figure 5-5 shows the pin assignments on the 32-pin RHB VQFN.



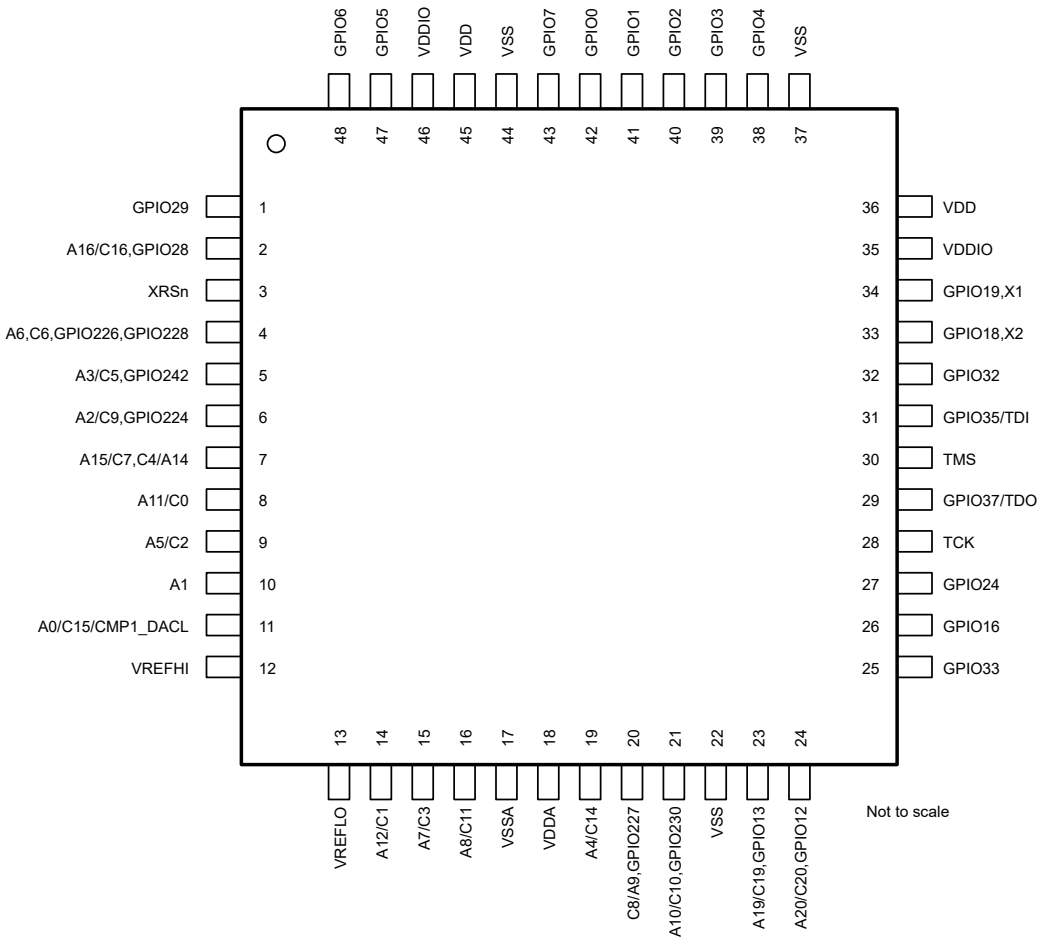
A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-1. 64-Pin PM Low-Profile Quad Flatpack (Top View)



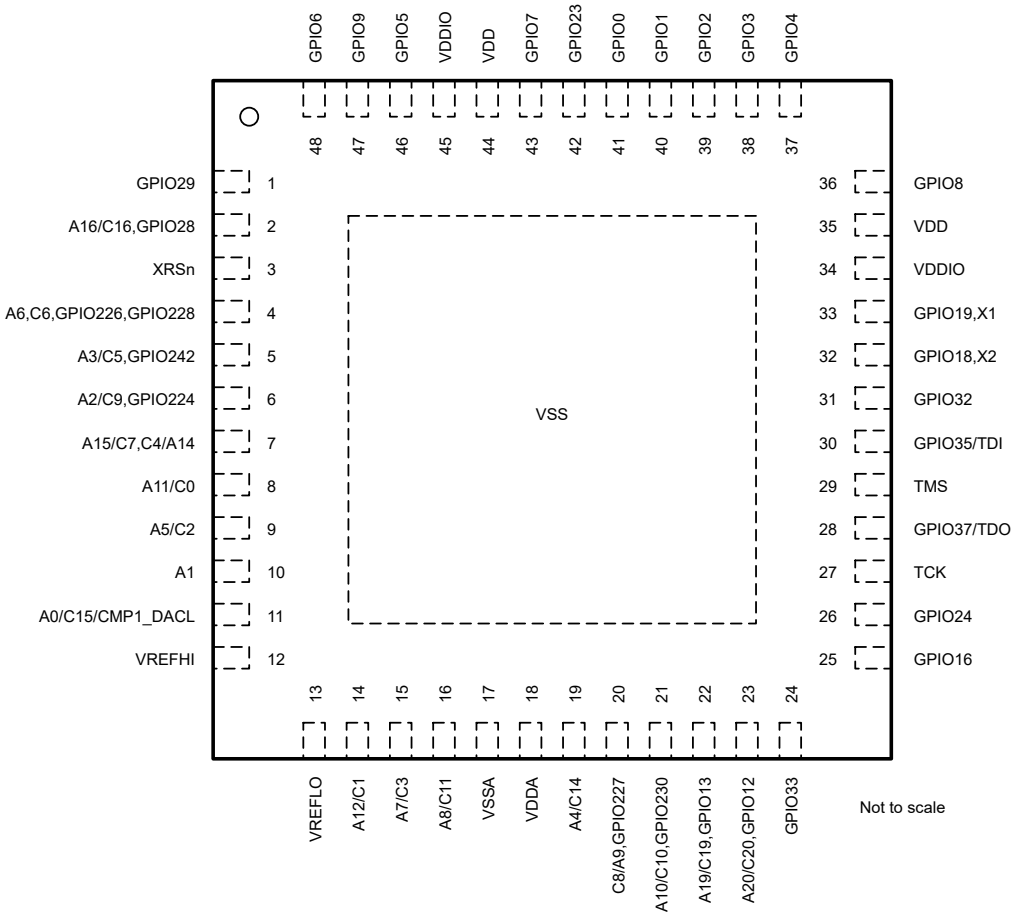
A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-2. 64-Pin PM Low-Profile Quad Flatpack *with VREGENZ* (Top View)



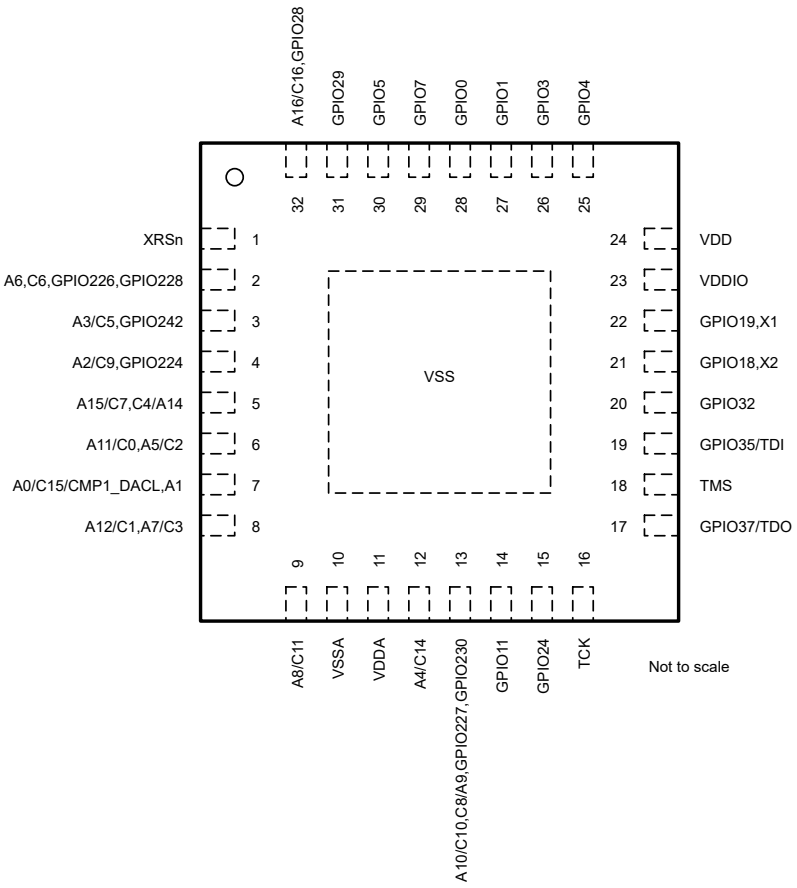
A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-3. 48-Pin PT Low-Profile Quad Flatpack (Top View)



A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-4. 48-Pin RGZ Very Thin Quad Flatpack No Lead (Top View)



A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-5. 32-Pin RHB Very Thin Quad Flatpack No Lead (Top View)

5.2 Pin Attributes

Table 5-1. Pin Attributes

SIGNAL NAME	MUX POSITION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB	PIN TYPE	DESCRIPTION
ANALOG								
A0							I	ADC-A Input 0
C15							I	ADC-C Input 15
CMP1_DACL		15	15	11	11	7	I	CMPSS-1 Low DAC Output
CMP3_HP2							I	CMPSS-3 High Comparator Positive Input 2
CMP3_LP2							I	CMPSS-3 Low Comparator Positive Input 2
AIO231	0, 4, 8, 12						I	Analog Pin Used For Digital Input 231
A1							I	ADC-A Input 1
CMP1_HP4		14	14	10	10	7	I	CMPSS-1 High Comparator Positive Input 4
CMP1_LP4							I	CMPSS-1 Low Comparator Positive Input 4
AIO232	0, 4, 8, 12						I	Analog Pin Used For Digital Input 232
A2							I	ADC-A Input 2
C9							I	ADC-C Input 9
CMP1_HP0		9	9	6	6	4	I	CMPSS-1 High Comparator Positive Input 0
CMP1_LP0							I	CMPSS-1 Low Comparator Positive Input 0
GPIO224							I/O	General-Purpose Input Output 224 This pin also has digital mux functions which are described in the GPIO section of this table.
A3							I	ADC-A Input 3
C5							I	ADC-C Input 5
CMP3_HN0							I	CMPSS-3 High Comparator Negative Input 0
CMP3_HP3							I	CMPSS-3 High Comparator Positive Input 3
CMP3_LN0		8	8	5	5	3	I	CMPSS-3 Low Comparator Negative Input 0
CMP3_LP3							I	CMPSS-3 Low Comparator Positive Input 3
GPIO242							I/O	General-Purpose Input Output 242 This pin also has digital mux functions which are described in the GPIO section of this table.
A4							I	ADC-A Input 4
C14							I	ADC-C Input 14
CMP2_HP0							I	CMPSS-2 High Comparator Positive Input 0
CMP2_LP0							I	CMPSS-2 Low Comparator Positive Input 0
CMP4_HN0		23	23	19	19	12	I	CMPSS-4 High Comparator Negative Input 0
CMP4_HP3							I	CMPSS-4 High Comparator Positive Input 3
CMP4_LN0							I	CMPSS-4 Low Comparator Negative Input 0
CMP4_LP3							I	CMPSS-4 Low Comparator Positive Input 3
AIO225	0, 4, 8, 12						I	Analog Pin Used For Digital Input 225
A5							I	ADC-A Input 5
C2							I	ADC-C Input 2
CMP3_HN1							I	CMPSS-3 High Comparator Negative Input 1
CMP3_HP1		13	13	9	9	6	I	CMPSS-3 High Comparator Positive Input 1
CMP3_LN1							I	CMPSS-3 Low Comparator Negative Input 1
CMP3_LP1							I	CMPSS-3 Low Comparator Positive Input 1
AIO244	0, 4, 8, 12						I	Analog Pin Used For Digital Input 244
A6							I	ADC-A Input 6
CMP1_HP2							I	CMPSS-1 High Comparator Positive Input 2
CMP1_LP2		6	6	4	4	2	I	CMPSS-1 Low Comparator Positive Input 2
GPIO228							I/O	General-Purpose Input Output 228 This pin also has digital mux functions which are described in the GPIO section of this table.

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB	PIN TYPE	DESCRIPTION
A7							I	ADC-A Input 7
C3							I	ADC-C Input 3
CMP4_HN1							I	CMPSS-4 High Comparator Negative Input 1
CMP4_HP1		19	19	15	15	8	I	CMPSS-4 High Comparator Positive Input 1
CMP4_LN1							I	CMPSS-4 Low Comparator Negative Input 1
CMP4_LP1							I	CMPSS-4 Low Comparator Positive Input 1
AIO245	0, 4, 8, 12						I	Analog Pin Used For Digital Input 245
A8							I	ADC-A Input 8
C11							I	ADC-C Input 11
CMP2_HP4							I	CMPSS-2 High Comparator Positive Input 4
CMP2_LP4		20	20	16	16	9	I	CMPSS-2 Low Comparator Positive Input 4
CMP4_HP4							I	CMPSS-4 High Comparator Positive Input 4
CMP4_LP4							I	CMPSS-4 Low Comparator Positive Input 4
AIO241	0, 4, 8, 12						I	Analog Pin Used For Digital Input 241
A10							I	ADC-A Input 10
C10							I	ADC-C Input 10
CMP2_HN0							I	CMPSS-2 High Comparator Negative Input 0
CMP2_HP3							I	CMPSS-2 High Comparator Positive Input 3
CMP2_LN0		25	25	21	21	13	I	CMPSS-2 Low Comparator Negative Input 0
CMP2_LP3							I	CMPSS-2 Low Comparator Positive Input 3
GPIO230							I/O	General-Purpose Input Output 230 This pin also has digital mux functions which are described in the GPIO section of this table.
A11							I	ADC-A Input 11
C0							I	ADC-C Input 0
CMP1_HN1							I	CMPSS-1 High Comparator Negative Input 1
CMP1_HP1		12	12	8	8	6	I	CMPSS-1 High Comparator Positive Input 1
CMP1_LN1							I	CMPSS-1 Low Comparator Negative Input 1
CMP1_LP1							I	CMPSS-1 Low Comparator Positive Input 1
AIO237	0, 4, 8, 12						I	Analog Pin Used For Digital Input 237
A12							I	ADC-A Input 12
C1							I	ADC-C Input 1
CMP2_HN1							I	CMPSS-2 High Comparator Negative Input 1
CMP2_HP1							I	CMPSS-2 High Comparator Positive Input 1
CMP2_LN1		18	18	14	14	8	I	CMPSS-2 Low Comparator Negative Input 1
CMP2_LP1							I	CMPSS-2 Low Comparator Positive Input 1
CMP4_HP2							I	CMPSS-4 High Comparator Positive Input 2
CMP4_LP2							I	CMPSS-4 Low Comparator Positive Input 2
AIO238	0, 4, 8, 12						I	Analog Pin Used For Digital Input 238
A15							I	ADC-A Input 15
C7							I	ADC-C Input 7
CMP1_HN0							I	CMPSS-1 High Comparator Negative Input 0
CMP1_HP3		10	10	7	7	5	I	CMPSS-1 High Comparator Positive Input 3
CMP1_LN0							I	CMPSS-1 Low Comparator Negative Input 0
CMP1_LP3							I	CMPSS-1 Low Comparator Positive Input 3
AIO233	0, 4, 8, 12						I	Analog Pin Used For Digital Input 233
A16							I	ADC-A Input 16
C16							I	ADC-C Input 16
GPIO28		2	2	2	2	32	I/O	General-Purpose Input Output 28 This pin also has digital mux functions which are described in the GPIO section of this table.

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB	PIN TYPE	DESCRIPTION
A17							I	ADC-A Input 17
C17							I	ADC-C Input 17
GPIO20		27	27				I/O	General-Purpose Input Output 20 This pin also has digital mux functions which are described in the GPIO section of this table.
A18							I	ADC-A Input 18
C18							I	ADC-C Input 18
GPIO21		28	28				I/O	General-Purpose Input Output 21 This pin also has digital mux functions which are described in the GPIO section of this table.
A19							I	ADC-A Input 19
C19							I	ADC-C Input 19
GPIO13		29	29	22	23		I/O	General-Purpose Input Output 13 This pin also has digital mux functions which are described in the GPIO section of this table.
A20							I	ADC-A Input 20
C20							I	ADC-C Input 20
GPIO12		30	30	23	24		I/O	General-Purpose Input Output 12 This pin also has digital mux functions which are described in the GPIO section of this table.
A14							I	ADC-A Input 14
C4							I	ADC-C Input 4
CMP3_HP4		11	11	7	7	5	I	CMPSS-3 High Comparator Positive Input 4
CMP3_LP4							I	CMPSS-3 Low Comparator Positive Input 4
AIO239	0, 4, 8, 12						I	Analog Pin Used For Digital Input 239
C6							I	ADC-C Input 6
CMP3_HP0							I	CMPSS-3 High Comparator Positive Input 0
CMP3_LP0		7	7	4	4	2	I	CMPSS-3 Low Comparator Positive Input 0
GPIO226							I/O	General-Purpose Input Output 226 This pin also has digital mux functions which are described in the GPIO section of this table.
A9							I	ADC-A Input 9
C8							I	ADC-C Input 8
CMP2_HP2							I	CMPSS-2 High Comparator Positive Input 2
CMP2_LP2							I	CMPSS-2 Low Comparator Positive Input 2
CMP4_HP0		24	24	20	20	13	I	CMPSS-4 High Comparator Positive Input 0
CMP4_LP0							I	CMPSS-4 Low Comparator Positive Input 0
GPIO227							I/O	General-Purpose Input Output 227 This pin also has digital mux functions which are described in the GPIO section of this table.
VREFHI		16	16	12	12		I	ADC- High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2-µF capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. On the 32 RHB package, VREFHI is internally tied to VDDA.
VREFLO		17	17	13	13		I	ADC- Low Reference

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB	PIN TYPE	DESCRIPTION
GPIO								
GPIO0	0, 4, 8, 12	52	52	41	42	28	I/O	General-Purpose Input Output 0
EPWM1_A	1						O	ePWM-1 Output A
CANA_RX	2						I	CAN-A Receive
OUTPUTXBAR7	3						O	Output X-BAR Output 7
SCIA_RX	5						I	SCI-A Receive Data
I2CA_SDA	6						I/OD	I2C-A Open-Drain Bidirectional Data
SPIA_STE	7						I/O	SPI-A Slave Transmit Enable (STE)
EQEP1_INDEX	13						I/O	eQEP-1 Index
EPWM3_A	15						O	ePWM-3 Output A
GPIO1	0, 4, 8, 12	51	51	40	41	27	I/O	General-Purpose Input Output 1
EPWM1_B	1						O	ePWM-1 Output B
SCIA_TX	5						O	SCI-A Transmit Data
I2CA_SCL	6						I/OD	I2C-A Open-Drain Bidirectional Clock
SPIA_SOMI	7						I/O	SPI-A Slave Out, Master In (SOMI)
EQEP1_STROBE	9						I/O	eQEP-1 Strobe
EPWM3_B	15						O	ePWM-3 Output B
GPIO2	0, 4, 8, 12	50	50	39	40		I/O	General-Purpose Input Output 2
EPWM2_A	1						O	ePWM-2 Output A
OUTPUTXBAR1	5						O	Output X-BAR Output 1
SPIA_SIMO	7						I/O	SPI-A Slave In, Master Out (SIMO)
SCIA_TX	9						O	SCI-A Transmit Data
I2CB_SDA	11						I/OD	I2C-B Open-Drain Bidirectional Data
CANA_TX	14						O	CAN-A Transmit
EPWM4_A	15						O	ePWM-4 Output A
GPIO3	0, 4, 8, 12	49	49	38	39	26	I/O	General-Purpose Input Output 3
EPWM2_B	1						O	ePWM-2 Output B
OUTPUTXBAR2	2, 5						O	Output X-BAR Output 2
SPIA_CLK	7						I/O	SPI-A Clock
SCIA_RX	9						I	SCI-A Receive Data
I2CB_SCL	11						I/OD	I2C-B Open-Drain Bidirectional Clock
CANA_RX	14						I	CAN-A Receive
EPWM4_B	15						O	ePWM-4 Output B
GPIO4	0, 4, 8, 12	48	48	37	38	25	I/O	General-Purpose Input Output 4
EPWM3_A	1						O	ePWM-3 Output A
I2CA_SCL	2						I/OD	I2C-A Open-Drain Bidirectional Clock
OUTPUTXBAR3	5						O	Output X-BAR Output 3
CANA_TX	6						O	CAN-A Transmit
SPIA_SOMI	14						I/O	SPI-A Slave Out, Master In (SOMI)
EPWM1_A	15						O	ePWM-1 Output A
GPIO5	0, 4, 8, 12	61	61	46	47	30	I/O	General-Purpose Input Output 5
EPWM3_B	1						O	ePWM-3 Output B
I2CA_SDA	2						I/OD	I2C-A Open-Drain Bidirectional Data
OUTPUTXBAR3	3						O	Output X-BAR Output 3
CANA_RX	6						I	CAN-A Receive
SPIA_STE	7						I/O	SPI-A Slave Transmit Enable (STE)
SCIA_RX	11						I	SCI-A Receive Data
EPWM1_B	15						O	ePWM-1 Output B

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB	PIN TYPE	DESCRIPTION
GPIO6	0, 4, 8, 12	64	64	48	48		I/O	General-Purpose Input Output 6
EPWM4_A	1						O	ePWM-4 Output A
OUTPUTXBAR4	2						O	Output X-BAR Output 4
SYNCOUT	3						O	External ePWM Synchronization Pulse
EQEP1_A	5						I	eQEP-1 Input A
EPWM2_A	15						O	ePWM-2 Output A
GPIO7	0, 4, 8, 12	57	57	43	43	29	I/O	General-Purpose Input Output 7
EPWM4_B	1						O	ePWM-4 Output B
EPWM2_A	2						O	ePWM-2 Output A
OUTPUTXBAR5	3						O	Output X-BAR Output 5
EQEP1_B	5						I	eQEP-1 Input B
SPIA_SIMO	7						I/O	SPI-A Slave In, Master Out (SIMO)
SCIA_TX	11						O	SCI-A Transmit Data
CANA_TX	14						O	CAN-A Transmit
EPWM2_B	15						O	ePWM-2 Output B
GPIO8	0, 4, 8, 12	47	47	36			I/O	General-Purpose Input Output 8
EPWM5_A	1						O	ePWM-5 Output A
ADCSOCAO	3						O	ADC Start of Conversion A for External ADC
EQEP1_STROBE	5						I/O	eQEP-1 Strobe
SCIA_TX	6						O	SCI-A Transmit Data
SPIA_SIMO	7						I/O	SPI-A Slave In, Master Out (SIMO)
I2CA_SCL	9						I/OD	I2C-A Open-Drain Bidirectional Clock
GPIO9	0, 4, 8, 12	62	62	47			I/O	General-Purpose Input Output 9
EPWM5_B	1						O	ePWM-5 Output B
SCIB_TX	2						O	SCI-B Transmit Data
OUTPUTXBAR6	3						O	Output X-BAR Output 6
EQEP1_INDEX	5						I/O	eQEP-1 Index
SCIA_RX	6						I	SCI-A Receive Data
SPIA_CLK	7						I/O	SPI-A Clock
I2CB_SCL	14						I/OD	I2C-B Open-Drain Bidirectional Clock
GPIO10	0, 4, 8, 12	63	63				I/O	General-Purpose Input Output 10
EPWM6_A	1						O	ePWM-6 Output A
ADCSOCBO	3						O	ADC Start of Conversion B for External ADC
EQEP1_A	5						I	eQEP-1 Input A
SCIB_TX	6						O	SCI-B Transmit Data
SPIA_SOMI	7						I/O	SPI-A Slave Out, Master In (SOMI)
I2CA_SDA	9						I/OD	I2C-A Open-Drain Bidirectional Data
GPIO11	0, 4, 8, 12	31	31			14	I/O	General-Purpose Input Output 11
EPWM6_B	1						O	ePWM-6 Output B
CANA_RX	2						I	CAN-A Receive
OUTPUTXBAR7	3						O	Output X-BAR Output 7
EQEP1_B	5						I	eQEP-1 Input B
SCIB_RX	6						I	SCI-B Receive Data
SPIA_STE	7						I/O	SPI-A Slave Transmit Enable (STE)
SPIA_SIMO	13						I/O	SPI-A Slave In, Master Out (SIMO)

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB	PIN TYPE	DESCRIPTION
GPIO12	0, 4, 8, 12	30	30	23	24		I/O	General-Purpose Input Output 12 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM7_A	1						O	ePWM-7 Output A
EQEP1_STROBE	5						I/O	eQEP-1 Strobe
SCIB_TX	6						O	SCI-B Transmit Data
SPIA_CLK	11						I/O	SPI-A Clock
CANA_RX	13						I	CAN-A Receive
GPIO13	0, 4, 8, 12	29	29	22	23		I/O	General-Purpose Input Output 13 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM7_B	1						O	ePWM-7 Output B
EQEP1_INDEX	5						I/O	eQEP-1 Index
SCIB_RX	6						I	SCI-B Receive Data
SPIA_SOMI	11						I/O	SPI-A Slave Out, Master In (SOMI)
CANA_TX	13						O	CAN-A Transmit
GPIO16	0, 4, 8, 12	33	33	25	26		I/O	General-Purpose Input Output 16
SPIA_SIMO	1						I/O	SPI-A Slave In, Master Out (SIMO)
OUTPUTXBAR7	3						O	Output X-BAR Output 7
EPWM5_A	5						O	ePWM-5 Output A
SCIA_TX	6						O	SCI-A Transmit Data
EQEP1_STROBE	9						I/O	eQEP-1 Strobe
XCLKOUT	11						O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
GPIO17	0, 4, 8, 12	34	34				I/O	General-Purpose Input Output 17
SPIA_SOMI	1						I/O	SPI-A Slave Out, Master In (SOMI)
OUTPUTXBAR8	3						O	Output X-BAR Output 8
EPWM5_B	5						O	ePWM-5 Output B
SCIA_RX	6						I	SCI-A Receive Data
EQEP1_INDEX	9						I/O	eQEP-1 Index
CANA_TX	11						O	CAN-A Transmit
EPWM6_A	14						O	ePWM-6 Output A
GPIO18	0, 4, 8, 12	41	41	32	33	21	I/O	General-Purpose Input Output 18
SPIA_CLK	1						I/O	SPI-A Clock
SCIB_TX	2						O	SCI-B Transmit Data
CANA_RX	3						I	CAN-A Receive
EPWM6_A	5						O	ePWM-6 Output A
I2CA_SCL	6						I/OD	I2C-A Open-Drain Bidirectional Clock
XCLKOUT	11						O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
X2	ALT						I/O	Crystal oscillator output.

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB	PIN TYPE	DESCRIPTION
GPIO19	0, 4, 8, 12	42	42	33	34	22	I/O	General-Purpose Input Output 19
SPIA_STE	1						I/O	SPI-A Slave Transmit Enable (STE)
SCIB_RX	2						I	SCI-B Receive Data
CANA_TX	3						O	CAN-A Transmit
EPWM6_B	5						O	ePWM-6 Output B
I2CA_SDA	6						I/OD	I2C-A Open-Drain Bidirectional Data
X1	ALT						I/O	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock.
ExtR	ALT2						I	External resistor for internal oscillator. This can be used for greater clock accuracy.
GPIO20	0, 4, 8, 12	27	27				I/O	General-Purpose Input Output 20 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP1_A	1						I	eQEP-1 Input A
CANA_TX	3						O	CAN-A Transmit
SPIA_SIMO	6						I/O	SPI-A Slave In, Master Out (SIMO)
I2CA_SCL	11						I/OD	I2C-A Open-Drain Bidirectional Clock
SCIC_TX	15						O	SCI-C Transmit Data
GPIO21	0, 4, 8, 12	28	28				I/O	General-Purpose Input Output 21 This pin also has analog functions which are described in the ANALOG section of this table.
EQEP1_B	1						I	eQEP-1 Input B
CANA_RX	3						I	CAN-A Receive
SPIA_SOMI	6						I/O	SPI-A Slave Out, Master In (SOMI)
I2CA_SDA	11						I/OD	I2C-A Open-Drain Bidirectional Data
SCIC_RX	15						I	SCI-C Receive Data
GPIO22	0, 4, 8, 12	56	56				I/O	General-Purpose Input Output 22
EQEP1_STROBE	1						I/O	eQEP-1 Strobe
SCIB_TX	3						O	SCI-B Transmit Data
SCIC_TX	9						O	SCI-C Transmit Data
EPWM4_A	14						O	ePWM-4 Output A
GPIO23	0, 4, 8, 12	54	54	42			I/O	General-Purpose Input Output 23
EQEP1_INDEX	1						I/O	eQEP-1 Index
SCIB_RX	3						I	SCI-B Receive Data
SCIC_RX	9						I	SCI-C Receive Data
EPWM4_B	14						O	ePWM-4 Output B
GPIO24	0, 4, 8, 12	35	35	26	27	15	I/O	General-Purpose Input Output 24
OUTPUTXBAR1	1						O	Output X-BAR Output 1
SPIA_STE	3						I/O	SPI-A Slave Transmit Enable (STE)
EPWM4_A	5						O	ePWM-4 Output A
SPIA_SIMO	6						I/O	SPI-A Slave In, Master Out (SIMO)
SCIA_TX	11						O	SCI-A Transmit Data
ERRORSTS	13						O	Error Status Output. This signal requires an external pulldown.

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB	PIN TYPE	DESCRIPTION
GPIO28	0, 4, 8, 12	2	2	2	2	32	I/O	General-Purpose Input Output 28 This pin also has analog functions which are described in the ANALOG section of this table.
SCIA_RX	1						I	SCI-A Receive Data
EPWM7_A	3						O	ePWM-7 Output A
OUTPUTXBAR5	5						O	Output X-BAR Output 5
EQEP1_A	6						I	eQEP-1 Input A
SCIC_TX	10						O	SCI-C Transmit Data
SPIA_CLK	11						I/O	SPI-A Clock
ERRORSTS	13						O	Error Status Output. This signal requires an external pulldown.
I2CB_SDA	14						I/OD	I2C-B Open-Drain Bidirectional Data
GPIO29	0, 4, 8, 12	1	1	1	1	31	I/O	General-Purpose Input Output 29
SCIA_TX	1						O	SCI-A Transmit Data
EPWM7_B	3						O	ePWM-7 Output B
OUTPUTXBAR6	5						O	Output X-BAR Output 6
EQEP1_B	6						I	eQEP-1 Input B
SCIC_RX	10						I	SCI-C Receive Data
SPIA_STE	11						I/O	SPI-A Slave Transmit Enable (STE)
ERRORSTS	13						O	Error Status Output. This signal requires an external pulldown.
I2CB_SCL	14						I/OD	I2C-B Open-Drain Bidirectional Clock
GPIO32	0, 4, 8, 12	40	40	31	32	20	I/O	General-Purpose Input Output 32
I2CA_SDA	1						I/OD	I2C-A Open-Drain Bidirectional Data
EQEP1_INDEX	2						I/O	eQEP-1 Index
SPIA_CLK	3						I/O	SPI-A Clock
EPWM4_B	5						O	ePWM-4 Output B
SCIC_TX	6						O	SCI-C Transmit Data
CANA_TX	10						O	CAN-A Transmit
ADCSOCBO	13						O	ADC Start of Conversion B for External ADC
GPIO33	0, 4, 8, 12	32	32	24	25		I/O	General-Purpose Input Output 33
I2CA_SCL	1						I/OD	I2C-A Open-Drain Bidirectional Clock
OUTPUTXBAR4	5						O	Output X-BAR Output 4
SCIC_RX	6						I	SCI-C Receive Data
CANA_RX	10						I	CAN-A Receive
ADCSOCAO	13						O	ADC Start of Conversion A for External ADC
GPIO35	0, 4, 8, 12	39	39	30	31	19	I/O	General-Purpose Input Output 35
SCIA_RX	1						I	SCI-A Receive Data
SPIA_SOMI	2						I/O	SPI-A Slave Out, Master In (SOMI)
I2CA_SDA	3						I/OD	I2C-A Open-Drain Bidirectional Data
CANA_RX	5						I	CAN-A Receive
SCIC_RX	7						I	SCI-C Receive Data
EQEP1_A	9						I	eQEP-1 Input A
EPWM5_B	11						O	ePWM-5 Output B
TDI	15						I	JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input.

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB	PIN TYPE	DESCRIPTION
GPIO37	0, 4, 8, 12	37	37	28	29	17	I/O	General-Purpose Input Output 37
OUTPUTXBAR2	1						O	Output X-BAR Output 2
SPIA_STE	2						I/O	SPI-A Slave Transmit Enable (STE)
I2CA_SCL	3						I/OD	I2C-A Open-Drain Bidirectional Clock
SCIA_TX	5						O	SCI-A Transmit Data
CANA_TX	6						O	CAN-A Transmit
SCIC_TX	7						O	SCI-C Transmit Data
EQEP1_B	9						I	eQEP-1 Input B
EPWM5_A	11						O	ePWM-5 Output A
TDO	15						O	JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input.
GPIO39	0, 4, 8, 12		46				I/O	General-Purpose Input Output 39
SYNCOUT	13						O	External ePWM Synchronization Pulse
EQEP1_INDEX	14						I/O	eQEP-1 Index
GPIO40	0, 4, 8, 12	53	53				I/O	General-Purpose Input Output 40
EPWM2_B	5						O	ePWM-2 Output B
SCIB_TX	9						O	SCI-B Transmit Data
EQEP1_A	10						I	eQEP-1 Input A
GPIO41	0, 4, 8, 12	55	55				I/O	General-Purpose Input Output 41
EPWM7_A	1						O	ePWM-7 Output A
EPWM2_A	5						O	ePWM-2 Output A
SCIB_RX	9						I	SCI-B Receive Data
EQEP1_B	10						I	eQEP-1 Input B
GPIO224	0, 4, 8, 12	9	9	6	6	4	I/O	General-Purpose Input Output 224 This pin also has analog functions which are described in the ANALOG section of this table.
OUTPUTXBAR3	5						O	Output X-BAR Output 3
SPIA_SIMO	6						I/O	SPI-A Slave In, Master Out (SIMO)
EPWM1_A	9						O	ePWM-1 Output A
CANA_TX	10						O	CAN-A Transmit
EQEP1_A	11						I	eQEP-1 Input A
SCIC_TX	14						O	SCI-C Transmit Data
GPIO226	0, 4, 8, 12	7	7	4	4	2	I/O	General-Purpose Input Output 226 This pin also has analog functions which are described in the ANALOG section of this table.
EPWM6_A	5						O	ePWM-6 Output A
SPIA_CLK	6						I/O	SPI-A Clock
EPWM1_B	9						O	ePWM-1 Output B
EQEP1_STROBE	11						I/O	eQEP-1 Strobe
SCIC_RX	14						I	SCI-C Receive Data
GPIO227	0, 4, 8, 12	24	24	20	20	13	I/O	General-Purpose Input Output 227 This pin also has analog functions which are described in the ANALOG section of this table.
I2CB_SCL	1						I/OD	I2C-B Open-Drain Bidirectional Clock
EPWM3_A	3						O	ePWM-3 Output A
OUTPUTXBAR1	5						O	Output X-BAR Output 1
EPWM2_B	6						O	ePWM-2 Output B

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB	PIN TYPE	DESCRIPTION
GPIO228	0, 4, 8, 12	6	6	4	4	2	I/O	General-Purpose Input Output 228 This pin also has analog functions which are described in the ANALOG section of this table.
ADCSOCAO	3						O	ADC Start of Conversion A for External ADC
CANA_TX	5						O	CAN-A Transmit
SPIA_SOMI	6						I/O	SPI-A Slave Out, Master In (SOMI)
EPWM2_B	9						O	ePWM-2 Output B
EQEP1_B	11						I	eQEP-1 Input B
GPIO230	0, 4, 8, 12	25	25	21	21	13	I/O	General-Purpose Input Output 230 This pin also has analog functions which are described in the ANALOG section of this table.
I2CB_SDA	1						I/OD	I2C-B Open-Drain Bidirectional Data
EPWM3_B	3						O	ePWM-3 Output B
CANA_RX	5						I	CAN-A Receive
EPWM2_A	6						O	ePWM-2 Output A
I2CA_SDA	7						I/OD	I2C-A Open-Drain Bidirectional Data
GPIO242	0, 4, 8, 12	8	8	5	5	3	I/O	General-Purpose Input Output 242 This pin also has analog functions which are described in the ANALOG section of this table.
OUTPUTXBAR2	5						O	Output X-BAR Output 2
SPIA_STE	6						I/O	SPI-A Slave Transmit Enable (STE)
EPWM4_A	9						O	ePWM-4 Output A
CANA_RX	10						I	CAN-A Receive
EQEP1_INDEX	11						I/O	eQEP-1 Index
TEST, JTAG, AND RESET								
TCK		36	36	27	28	16	I	JTAG test clock with internal pullup.
TMS		38	38	29	30	18	I/O	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.
XRSn		3	3	3	3	1	I/OD	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.
POWER AND GROUND								
VDD		4, 44, 59	4, 44, 59	35, 44	36, 45	24		1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a total capacitance of approximately 10 µF.
VDDA		22	22	18	18	11		3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor on each pin. On the 32 RHB package, VREFHI is internally tied to VDDA.
VDDIO		43, 60	43, 60	34, 45	35, 46	23		3.3-V Digital I/O Power Pins. Place a minimum 0.1-µF decoupling capacitor on each pin.
VREGENZ		46					I	Internal voltage regulator enable with internal pulldown. Tie low to VSS to enable internal VREG. Tie high to VDDIO to use an external supply.

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB	PIN TYPE	DESCRIPTION
VSS		5, 26, 45, 58	5, 26, 45, 58	PAD	22, 37, 44	PAD		Digital Ground. For QFN packages, the ground pad on the bottom of the package must be soldered to the ground plane of the PCB.
VSSA		21	21	17	17	10		Analog Ground

5.3 Signal Descriptions

5.3.1 Analog Signals

Table 5-2. Analog Signals

SIGNAL NAME	PIN TYPE	DESCRIPTION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB
A0	I	ADC-A Input 0	15	15	11	11	7
A1	I	ADC-A Input 1	14	14	10	10	7
A2	I	ADC-A Input 2	9	9	6	6	4
A3	I	ADC-A Input 3	8	8	5	5	3
A4	I	ADC-A Input 4	23	23	19	19	12
A5	I	ADC-A Input 5	13	13	9	9	6
A6	I	ADC-A Input 6	6	6	4	4	2
A7	I	ADC-A Input 7	19	19	15	15	8
A8	I	ADC-A Input 8	20	20	16	16	9
A9	I	ADC-A Input 9	24	24	20	20	13
A10	I	ADC-A Input 10	25	25	21	21	13
A11	I	ADC-A Input 11	12	12	8	8	6
A12	I	ADC-A Input 12	18	18	14	14	8
A14	I	ADC-A Input 14	11	11	7	7	5
A15	I	ADC-A Input 15	10	10	7	7	5
A16	I	ADC-A Input 16	2	2	2	2	32
A17	I	ADC-A Input 17	27	27			
A18	I	ADC-A Input 18	28	28			
A19	I	ADC-A Input 19	29	29	22	23	
A20	I	ADC-A Input 20	30	30	23	24	
AIO225	I	Analog Pin Used For Digital Input 225	23	23	19	19	12
AIO231	I	Analog Pin Used For Digital Input 231	15	15	11	11	7
AIO232	I	Analog Pin Used For Digital Input 232	14	14	10	10	7
AIO233	I	Analog Pin Used For Digital Input 233	10	10	7	7	5
AIO237	I	Analog Pin Used For Digital Input 237	12	12	8	8	6
AIO238	I	Analog Pin Used For Digital Input 238	18	18	14	14	8
AIO239	I	Analog Pin Used For Digital Input 239	11	11	7	7	5
AIO241	I	Analog Pin Used For Digital Input 241	20	20	16	16	9
AIO244	I	Analog Pin Used For Digital Input 244	13	13	9	9	6
AIO245	I	Analog Pin Used For Digital Input 245	19	19	15	15	8
C0	I	ADC-C Input 0	12	12	8	8	6
C1	I	ADC-C Input 1	18	18	14	14	8
C2	I	ADC-C Input 2	13	13	9	9	6
C3	I	ADC-C Input 3	19	19	15	15	8
C4	I	ADC-C Input 4	11	11	7	7	5
C5	I	ADC-C Input 5	8	8	5	5	3
C6	I	ADC-C Input 6	7	7	4	4	2
C7	I	ADC-C Input 7	10	10	7	7	5
C8	I	ADC-C Input 8	24	24	20	20	13
C9	I	ADC-C Input 9	9	9	6	6	4
C10	I	ADC-C Input 10	25	25	21	21	13
C11	I	ADC-C Input 11	20	20	16	16	9

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB
C14	I	ADC-C Input 14	23	23	19	19	12
C15	I	ADC-C Input 15	15	15	11	11	7
C16	I	ADC-C Input 16	2	2	2	2	32
C17	I	ADC-C Input 17	27	27			
C18	I	ADC-C Input 18	28	28			
C19	I	ADC-C Input 19	29	29	22	23	
C20	I	ADC-C Input 20	30	30	23	24	
CMP1_DACL	I	CMPSS-1 Low DAC Output	15	15	11	11	7
CMP1_HN0	I	CMPSS-1 High Comparator Negative Input 0	10	10	7	7	5
CMP1_HN1	I	CMPSS-1 High Comparator Negative Input 1	12	12	8	8	6
CMP1_HP0	I	CMPSS-1 High Comparator Positive Input 0	9	9	6	6	4
CMP1_HP1	I	CMPSS-1 High Comparator Positive Input 1	12	12	8	8	6
CMP1_HP2	I	CMPSS-1 High Comparator Positive Input 2	6	6	4	4	2
CMP1_HP3	I	CMPSS-1 High Comparator Positive Input 3	10	10	7	7	5
CMP1_HP4	I	CMPSS-1 High Comparator Positive Input 4	14	14	10	10	7
CMP1_LN0	I	CMPSS-1 Low Comparator Negative Input 0	10	10	7	7	5
CMP1_LN1	I	CMPSS-1 Low Comparator Negative Input 1	12	12	8	8	6
CMP1_LP0	I	CMPSS-1 Low Comparator Positive Input 0	9	9	6	6	4
CMP1_LP1	I	CMPSS-1 Low Comparator Positive Input 1	12	12	8	8	6
CMP1_LP2	I	CMPSS-1 Low Comparator Positive Input 2	6	6	4	4	2
CMP1_LP3	I	CMPSS-1 Low Comparator Positive Input 3	10	10	7	7	5
CMP1_LP4	I	CMPSS-1 Low Comparator Positive Input 4	14	14	10	10	7
CMP2_HN0	I	CMPSS-2 High Comparator Negative Input 0	25	25	21	21	13
CMP2_HN1	I	CMPSS-2 High Comparator Negative Input 1	18	18	14	14	8
CMP2_HP0	I	CMPSS-2 High Comparator Positive Input 0	23	23	19	19	12
CMP2_HP1	I	CMPSS-2 High Comparator Positive Input 1	18	18	14	14	8
CMP2_HP2	I	CMPSS-2 High Comparator Positive Input 2	24	24	20	20	13
CMP2_HP3	I	CMPSS-2 High Comparator Positive Input 3	25	25	21	21	13
CMP2_HP4	I	CMPSS-2 High Comparator Positive Input 4	20	20	16	16	9

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB
CMP2_LN0	I	CMPSS-2 Low Comparator Negative Input 0	25	25	21	21	13
CMP2_LN1	I	CMPSS-2 Low Comparator Negative Input 1	18	18	14	14	8
CMP2_LP0	I	CMPSS-2 Low Comparator Positive Input 0	23	23	19	19	12
CMP2_LP1	I	CMPSS-2 Low Comparator Positive Input 1	18	18	14	14	8
CMP2_LP2	I	CMPSS-2 Low Comparator Positive Input 2	24	24	20	20	13
CMP2_LP3	I	CMPSS-2 Low Comparator Positive Input 3	25	25	21	21	13
CMP2_LP4	I	CMPSS-2 Low Comparator Positive Input 4	20	20	16	16	9
CMP3_HN0	I	CMPSS-3 High Comparator Negative Input 0	8	8	5	5	3
CMP3_HN1	I	CMPSS-3 High Comparator Negative Input 1	13	13	9	9	6
CMP3_HP0	I	CMPSS-3 High Comparator Positive Input 0	7	7	4	4	2
CMP3_HP1	I	CMPSS-3 High Comparator Positive Input 1	13	13	9	9	6
CMP3_HP2	I	CMPSS-3 High Comparator Positive Input 2	15	15	11	11	7
CMP3_HP3	I	CMPSS-3 High Comparator Positive Input 3	8	8	5	5	3
CMP3_HP4	I	CMPSS-3 High Comparator Positive Input 4	11	11	7	7	5
CMP3_LN0	I	CMPSS-3 Low Comparator Negative Input 0	8	8	5	5	3
CMP3_LN1	I	CMPSS-3 Low Comparator Negative Input 1	13	13	9	9	6
CMP3_LP0	I	CMPSS-3 Low Comparator Positive Input 0	7	7	4	4	2
CMP3_LP1	I	CMPSS-3 Low Comparator Positive Input 1	13	13	9	9	6
CMP3_LP2	I	CMPSS-3 Low Comparator Positive Input 2	15	15	11	11	7
CMP3_LP3	I	CMPSS-3 Low Comparator Positive Input 3	8	8	5	5	3
CMP3_LP4	I	CMPSS-3 Low Comparator Positive Input 4	11	11	7	7	5
CMP4_HN0	I	CMPSS-4 High Comparator Negative Input 0	23	23	19	19	12
CMP4_HN1	I	CMPSS-4 High Comparator Negative Input 1	19	19	15	15	8
CMP4_HP0	I	CMPSS-4 High Comparator Positive Input 0	24	24	20	20	13
CMP4_HP1	I	CMPSS-4 High Comparator Positive Input 1	19	19	15	15	8
CMP4_HP2	I	CMPSS-4 High Comparator Positive Input 2	18	18	14	14	8

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB
CMP4_HP3	I	CMPSS-4 High Comparator Positive Input 3	23	23	19	19	12
CMP4_HP4	I	CMPSS-4 High Comparator Positive Input 4	20	20	16	16	9
CMP4_LN0	I	CMPSS-4 Low Comparator Negative Input 0	23	23	19	19	12
CMP4_LN1	I	CMPSS-4 Low Comparator Negative Input 1	19	19	15	15	8
CMP4_LP0	I	CMPSS-4 Low Comparator Positive Input 0	24	24	20	20	13
CMP4_LP1	I	CMPSS-4 Low Comparator Positive Input 1	19	19	15	15	8
CMP4_LP2	I	CMPSS-4 Low Comparator Positive Input 2	18	18	14	14	8
CMP4_LP3	I	CMPSS-4 Low Comparator Positive Input 3	23	23	19	19	12
CMP4_LP4	I	CMPSS-4 Low Comparator Positive Input 4	20	20	16	16	9
GPIO12	I/O	General-Purpose Input Output 12	30	30	23	24	
GPIO13	I/O	General-Purpose Input Output 13	29	29	22	23	
GPIO20	I/O	General-Purpose Input Output 20	27	27			
GPIO21	I/O	General-Purpose Input Output 21	28	28			
GPIO28	I/O	General-Purpose Input Output 28	2	2	2	2	32
GPIO224	I/O	General-Purpose Input Output 224	9	9	6	6	4
GPIO226	I/O	General-Purpose Input Output 226	7	7	4	4	2
GPIO227	I/O	General-Purpose Input Output 227	24	24	20	20	13
GPIO228	I/O	General-Purpose Input Output 228	6	6	4	4	2
GPIO230	I/O	General-Purpose Input Output 230	25	25	21	21	13
GPIO242	I/O	General-Purpose Input Output 242	8	8	5	5	3
VREFHI	I	ADC- High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2-µF capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. On the 32 RHB package, VREFHI is internally tied to VDDA.	16	16	12	12	
VREFLO	I	ADC- Low Reference	17	17	13	13	

5.3.2 Digital Signals

Table 5-3. Digital Signals

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	64 VPM	64 PM	48 RGZ	48 PT	32 RHB
ADCSOCAO	O	ADC Start of Conversion A for External ADC	8, 33, 228	6, 32, 47	6, 32, 47	4, 24, 36	4, 25	2
ADCSOCBO	O	ADC Start of Conversion B for External ADC	10, 32	40, 63	40, 63	31	32	20
CANA_RX	I	CAN-A Receive	0, 3, 5, 11, 12, 18, 21, 33, 35, 230, 242	8, 25, 28, 30, 31, 32, 39, 41, 49, 52, 61	8, 25, 28, 30, 31, 32, 39, 41, 49, 52, 61	5, 21, 23, 24, 30, 32, 38, 41, 46	5, 21, 24, 25, 31, 33, 39, 42, 47	3, 13, 14, 19, 21, 26, 28, 30
CANA_TX	O	CAN-A Transmit	2, 4, 7, 13, 17, 19, 20, 32, 37, 224, 228	6, 9, 27, 29, 34, 37, 40, 42, 48, 50, 57	6, 9, 27, 29, 34, 37, 40, 42, 48, 50, 57	4, 6, 22, 28, 31, 33, 37, 39, 43	4, 6, 23, 29, 32, 34, 38, 40, 43	2, 4, 17, 20, 22, 25, 29
EPWM1_A	O	ePWM-1 Output A	0, 4, 224	9, 48, 52	9, 48, 52	6, 37, 41	6, 38, 42	4, 25, 28
EPWM1_B	O	ePWM-1 Output B	1, 5, 226	7, 51, 61	7, 51, 61	4, 40, 46	4, 41, 47	2, 27, 30
EPWM2_A	O	ePWM-2 Output A	2, 6, 7, 41, 230	25, 50, 55, 57, 64	25, 50, 55, 57, 64	21, 39, 43, 48	21, 40, 43, 48	13, 29
EPWM2_B	O	ePWM-2 Output B	3, 7, 40, 227, 228	6, 24, 49, 53, 57	6, 24, 49, 53, 57	4, 20, 38, 43	4, 20, 39, 43	2, 13, 26, 29
EPWM3_A	O	ePWM-3 Output A	0, 4, 227	24, 48, 52	24, 48, 52	20, 37, 41	20, 38, 42	13, 25, 28
EPWM3_B	O	ePWM-3 Output B	1, 5, 230	25, 51, 61	25, 51, 61	21, 40, 46	21, 41, 47	13, 27, 30
EPWM4_A	O	ePWM-4 Output A	2, 6, 22, 24, 242	8, 35, 50, 56, 64	8, 35, 50, 56, 64	5, 26, 39, 48	5, 27, 40, 48	3, 15
EPWM4_B	O	ePWM-4 Output B	3, 7, 23, 32	40, 49, 54, 57	40, 49, 54, 57	31, 38, 42, 43	32, 39, 43	20, 26, 29
EPWM5_A	O	ePWM-5 Output A	8, 16, 37	33, 37, 47	33, 37, 47	25, 28, 36	26, 29	17
EPWM5_B	O	ePWM-5 Output B	9, 17, 35	34, 39, 62	34, 39, 62	30, 47	31	19
EPWM6_A	O	ePWM-6 Output A	10, 17, 18, 226	7, 34, 41, 63	7, 34, 41, 63	4, 32	4, 33	2, 21
EPWM6_B	O	ePWM-6 Output B	11, 19	31, 42	31, 42	33	34	14, 22
EPWM7_A	O	ePWM-7 Output A	12, 28, 41	2, 30, 55	2, 30, 55	2, 23	2, 24	32
EPWM7_B	O	ePWM-7 Output B	13, 29	1, 29	1, 29	1, 22	1, 23	31
EQEP1_A	I	eQEP-1 Input A	6, 10, 20, 28, 35, 40, 224	2, 9, 27, 39, 53, 63, 64	2, 9, 27, 39, 53, 63, 64	2, 6, 30, 48	2, 6, 31, 48	4, 19, 32
EQEP1_B	I	eQEP-1 Input B	7, 11, 21, 29, 37, 41, 228	1, 6, 28, 31, 37, 55, 57	1, 6, 28, 31, 37, 55, 57	1, 4, 28, 43	1, 4, 29, 43	2, 14, 17, 29, 31
EQEP1_INDEX	I/O	eQEP-1 Index	0, 9, 13, 17, 23, 32, 39, 242	8, 29, 34, 40, 52, 54, 62	8, 29, 34, 40, 46, 52, 54, 62	5, 22, 31, 41, 42, 47	5, 23, 32, 42	3, 20, 28
EQEP1_STROBE	I/O	eQEP-1 Strobe	1, 8, 12, 16, 22, 226	7, 30, 33, 47, 51, 56	7, 30, 33, 47, 51, 56	4, 23, 25, 36, 40	4, 24, 26, 41	2, 27
ERRORSTS	O	Error Status Output. This signal requires an external pulldown.	24, 28, 29	1, 2, 35	1, 2, 35	1, 2, 26	1, 2, 27	15, 31, 32
ExtR	I	External resistor for internal oscillator. This can be used for greater clock accuracy.	19	42	42	33	34	22
GPIO0	I/O	General-Purpose Input Output 0	0	52	52	41	42	28
GPIO1	I/O	General-Purpose Input Output 1	1	51	51	40	41	27
GPIO2	I/O	General-Purpose Input Output 2	2	50	50	39	40	
GPIO3	I/O	General-Purpose Input Output 3	3	49	49	38	39	26
GPIO4	I/O	General-Purpose Input Output 4	4	48	48	37	38	25
GPIO5	I/O	General-Purpose Input Output 5	5	61	61	46	47	30
GPIO6	I/O	General-Purpose Input Output 6	6	64	64	48	48	
GPIO7	I/O	General-Purpose Input Output 7	7	57	57	43	43	29
GPIO8	I/O	General-Purpose Input Output 8	8	47	47	36		
GPIO9	I/O	General-Purpose Input Output 9	9	62	62	47		
GPIO10	I/O	General-Purpose Input Output 10	10	63	63			
GPIO11	I/O	General-Purpose Input Output 11	11	31	31			14
GPIO12	I/O	General-Purpose Input Output 12	12	30	30	23	24	
GPIO13	I/O	General-Purpose Input Output 13	13	29	29	22	23	
GPIO16	I/O	General-Purpose Input Output 16	16	33	33	25	26	
GPIO17	I/O	General-Purpose Input Output 17	17	34	34			
GPIO18	I/O	General-Purpose Input Output 18	18	41	41	32	33	21
GPIO19	I/O	General-Purpose Input Output 19	19	42	42	33	34	22
GPIO20	I/O	General-Purpose Input Output 20	20	27	27			
GPIO21	I/O	General-Purpose Input Output 21	21	28	28			

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	64 VPM	64 PM	48 RGZ	48 PT	32 RHB
GPIO22	I/O	General-Purpose Input Output 22	22	56	56			
GPIO23	I/O	General-Purpose Input Output 23	23	54	54	42		
GPIO24	I/O	General-Purpose Input Output 24	24	35	35	26	27	15
GPIO28	I/O	General-Purpose Input Output 28	28	2	2	2	2	32
GPIO29	I/O	General-Purpose Input Output 29	29	1	1	1	1	31
GPIO32	I/O	General-Purpose Input Output 32	32	40	40	31	32	20
GPIO33	I/O	General-Purpose Input Output 33	33	32	32	24	25	
GPIO35	I/O	General-Purpose Input Output 35	35	39	39	30	31	19
GPIO37	I/O	General-Purpose Input Output 37	37	37	37	28	29	17
GPIO39	I/O	General-Purpose Input Output 39	39		46			
GPIO40	I/O	General-Purpose Input Output 40	40	53	53			
GPIO41	I/O	General-Purpose Input Output 41	41	55	55			
GPIO224	I/O	General-Purpose Input Output 224	224	9	9	6	6	4
GPIO226	I/O	General-Purpose Input Output 226	226	7	7	4	4	2
GPIO227	I/O	General-Purpose Input Output 227	227	24	24	20	20	13
GPIO228	I/O	General-Purpose Input Output 228	228	6	6	4	4	2
GPIO230	I/O	General-Purpose Input Output 230	230	25	25	21	21	13
GPIO242	I/O	General-Purpose Input Output 242	242	8	8	5	5	3
I2CA_SCL	I/OD	I2C-A Open-Drain Bidirectional Clock	1, 4, 8, 18, 20, 33, 37	27, 32, 37, 41, 47, 48, 51	27, 32, 37, 41, 47, 48, 51	24, 28, 32, 36, 37, 40	25, 29, 33, 38, 41	17, 21, 25, 27
I2CA_SDA	I/OD	I2C-A Open-Drain Bidirectional Data	0, 5, 10, 19, 21, 32, 35, 230	25, 28, 39, 40, 42, 52, 61, 63	25, 28, 39, 40, 42, 52, 61, 63	21, 30, 31, 33, 41, 46	21, 31, 32, 34, 42, 47	13, 19, 20, 22, 28, 30
I2CB_SCL	I/OD	I2C-B Open-Drain Bidirectional Clock	3, 9, 29, 227	1, 24, 49, 62	1, 24, 49, 62	1, 20, 38, 47	1, 20, 39	13, 26, 31
I2CB_SDA	I/OD	I2C-B Open-Drain Bidirectional Data	2, 28, 230	2, 25, 50	2, 25, 50	2, 21, 39	2, 21, 40	13, 32
OUTPUTXBAR1	O	Output X-BAR Output 1	2, 24, 227	24, 35, 50	24, 35, 50	20, 26, 39	20, 27, 40	13, 15
OUTPUTXBAR2	O	Output X-BAR Output 2	3, 37, 242	8, 37, 49	8, 37, 49	5, 28, 38	5, 29, 39	3, 17, 26
OUTPUTXBAR3	O	Output X-BAR Output 3	4, 5, 224	9, 48, 61	9, 48, 61	6, 37, 46	6, 38, 47	4, 25, 30
OUTPUTXBAR4	O	Output X-BAR Output 4	6, 33	32, 64	32, 64	24, 48	25, 48	
OUTPUTXBAR5	O	Output X-BAR Output 5	7, 28	2, 57	2, 57	2, 43	2, 43	29, 32
OUTPUTXBAR6	O	Output X-BAR Output 6	9, 29	1, 62	1, 62	1, 47	1	31
OUTPUTXBAR7	O	Output X-BAR Output 7	0, 11, 16	31, 33, 52	31, 33, 52	25, 41	26, 42	14, 28
OUTPUTXBAR8	O	Output X-BAR Output 8	17	34	34			
SCIA_RX	I	SCI-A Receive Data	0, 3, 5, 9, 17, 28, 35	2, 34, 39, 49, 52, 61, 62	2, 34, 39, 49, 52, 61, 62	2, 30, 38, 41, 46, 47	2, 31, 39, 42, 47	19, 26, 28, 30, 32
SCIA_TX	O	SCI-A Transmit Data	1, 2, 7, 8, 16, 24, 29, 37	1, 33, 35, 37, 47, 50, 51, 57	1, 33, 35, 37, 47, 50, 51, 57	1, 25, 26, 28, 36, 39, 40, 43	1, 26, 27, 29, 40, 41, 43	15, 17, 27, 29, 31
SCIB_RX	I	SCI-B Receive Data	11, 13, 19, 23, 41	29, 31, 42, 54, 55	29, 31, 42, 54, 55	22, 33, 42	23, 34	14, 22
SCIB_TX	O	SCI-B Transmit Data	9, 10, 12, 18, 22, 40	30, 41, 53, 56, 62, 63	30, 41, 53, 56, 62, 63	23, 32, 47	24, 33	21
SCIC_RX	I	SCI-C Receive Data	21, 23, 29, 33, 35, 226	1, 7, 28, 32, 39, 54	1, 7, 28, 32, 39, 54	1, 4, 24, 30, 42	1, 4, 25, 31	2, 19, 31
SCIC_TX	O	SCI-C Transmit Data	20, 22, 28, 32, 37, 224	2, 9, 27, 37, 40, 56	2, 9, 27, 37, 40, 56	2, 6, 28, 31	2, 6, 29, 32	4, 17, 20, 32
SPIA_CLK	I/O	SPI-A Clock	3, 9, 12, 18, 28, 32, 226	2, 7, 30, 40, 41, 49, 62	2, 7, 30, 40, 41, 49, 62	2, 4, 23, 31, 32, 38, 47	2, 4, 24, 32, 33, 39	2, 20, 21, 26, 32
SPIA_SIMO	I/O	SPI-A Slave In, Master Out (SIMO)	2, 7, 8, 11, 16, 20, 24, 224	9, 27, 31, 33, 35, 47, 50, 57	9, 27, 31, 33, 35, 47, 50, 57	6, 25, 26, 36, 39, 43	6, 26, 27, 40, 43	4, 14, 15, 29
SPIA_SOMI	I/O	SPI-A Slave Out, Master In (SOMI)	1, 4, 10, 13, 17, 21, 35, 228	6, 28, 29, 34, 39, 48, 51, 63	6, 28, 29, 34, 39, 48, 51, 63	4, 22, 30, 37, 40	4, 23, 31, 38, 41	2, 19, 25, 27
SPIA_STE	I/O	SPI-A Slave Transmit Enable (STE)	0, 5, 11, 19, 24, 29, 37, 242	1, 8, 31, 35, 37, 42, 52, 61	1, 8, 31, 35, 37, 42, 52, 61	1, 5, 26, 28, 33, 41, 46	1, 5, 27, 29, 34, 42, 47	3, 14, 15, 17, 22, 28, 30, 31
SYNCOUT	O	External ePWM Synchronization Pulse	6, 39	64	46, 64	48	48	
TDI	I	JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input.	35	39	39	30	31	19

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	64 VPM	64 PM	48 RGZ	48 PT	32 RHB
TDO	O	JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input.	37	37	37	28	29	17
X1	I/O	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock.	19	42	42	33	34	22
X2	I/O	Crystal oscillator output.	18	41	41	32	33	21
XCLKOUT	O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.	16, 18	33, 41	33, 41	25, 32	26, 33	21

5.3.3 Power and Ground

Table 5-4. Power and Ground

SIGNAL NAME	PIN TYPE	DESCRIPTION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB
VDD		1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a total capacitance of approximately 10 µF.	4, 44, 59	4, 44, 59	35, 44	36, 45	24
VDDA		3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor on each pin. On the 32 RHB package, VREFHI is internally tied to VDDA.	22	22	18	18	11
VDDIO		3.3-V Digital I/O Power Pins. Place a minimum 0.1-µF decoupling capacitor on each pin.	43, 60	43, 60	34, 45	35, 46	23
VREGENZ	I	Internal voltage regulator enable with internal pulldown. Tie low to VSS to enable internal VREG. Tie high to VDDIO to use an external supply.	46				
VSS		Digital Ground. For QFN packages, the ground pad on the bottom of the package must be soldered to the ground plane of the PCB.	5, 26, 45, 58	5, 26, 45, 58	PAD	22, 37, 44	PAD
VSSA		Analog Ground	21	21	17	17	10

5.3.4 Test, JTAG, and Reset

Table 5-5. Test, JTAG, and Reset

SIGNAL NAME	PIN TYPE	DESCRIPTION	64 VPM	64 PM	48 RGZ	48 PT	32 RHB
TCK	I	JTAG test clock with internal pullup.	36	36	27	28	16
TMS	I/O	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.	38	38	29	30	18
XRSn	I/OD	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.	3	3	3	3	1

5.4 Pin Multiplexing

5.4.1 GPIO Muxed Pins

Section 5.4.1.1 lists the GPIO muxed pins.

5.4.1.1 GPIO Muxed Pins

Table 5-6. GPIO Muxed Pins

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO0	EPWM1_A	CANA_RX	OUTPUTXBAR7	SCIA_RX	I2CA_SDA	SPIA_STE				EQEP1_INDEX		EPWM3_A	
GPIO1	EPWM1_B			SCIA_TX	I2CA_SCL	SPIA_SOMI	EQEP1_STROBE					EPWM3_B	
GPIO2	EPWM2_A			OUTPUTXBAR1		SPIA_SIMO	SCIA_TX		I2CB_SDA		CANA_TX	EPWM4_A	
GPIO3	EPWM2_B	OUTPUTXBAR2		OUTPUTXBAR2		SPIA_CLK	SCIA_RX		I2CB_SCL		CANA_RX	EPWM4_B	
GPIO4	EPWM3_A	I2CA_SCL		OUTPUTXBAR3	CANA_TX						SPIA_SOMI	EPWM1_A	
GPIO5	EPWM3_B	I2CA_SDA	OUTPUTXBAR3		CANA_RX	SPIA_STE			SCIA_RX			EPWM1_B	
GPIO6	EPWM4_A	OUTPUTXBAR4	SYNCOUT	EQEP1_A								EPWM2_A	
GPIO7	EPWM4_B	EPWM2_A	OUTPUTXBAR5	EQEP1_B		SPIA_SIMO			SCIA_TX		CANA_TX	EPWM2_B	
GPIO8	EPWM5_A		ADCSOCAO	EQEP1_STROBE	SCIA_TX	SPIA_SIMO	I2CA_SCL						
GPIO9	EPWM5_B	SCIB_TX	OUTPUTXBAR6	EQEP1_INDEX	SCIA_RX	SPIA_CLK					I2CB_SCL		
GPIO10	EPWM6_A		ADCSOCBO	EQEP1_A	SCIB_TX	SPIA_SOMI	I2CA_SDA						
GPIO11	EPWM6_B	CANA_RX	OUTPUTXBAR7	EQEP1_B	SCIB_RX	SPIA_STE				SPIA_SIMO			
GPIO12	EPWM7_A			EQEP1_STROBE	SCIB_TX				SPIA_CLK	CANA_RX			
GPIO13	EPWM7_B			EQEP1_INDEX	SCIB_RX				SPIA_SOMI	CANA_TX			
GPIO16	SPIA_SIMO		OUTPUTXBAR7	EPWM5_A	SCIA_TX		EQEP1_STROBE		XCLKOUT				
GPIO17	SPIA_SOMI		OUTPUTXBAR8	EPWM5_B	SCIA_RX		EQEP1_INDEX		CANA_TX		EPWM6_A		
GPIO18	SPIA_CLK	SCIB_TX	CANA_RX	EPWM6_A	I2CA_SCL				XCLKOUT				X2
GPIO19	SPIA_STE	SCIB_RX	CANA_TX	EPWM6_B	I2CA_SDA								X1
GPIO20	EQEP1_A		CANA_TX		SPIA_SIMO				I2CA_SCL			SCIC_TX	
GPIO21	EQEP1_B		CANA_RX		SPIA_SOMI				I2CA_SDA			SCIC_RX	
GPIO22	EQEP1_STROBE		SCIB_TX				SCIC_TX				EPWM4_A		
GPIO23	EQEP1_INDEX		SCIB_RX				SCIC_RX				EPWM4_B		
GPIO24	OUTPUTXBAR1		SPIA_STE	EPWM4_A	SPIA_SIMO				SCIA_TX	ERRORSTS			
GPIO28	SCIA_RX		EPWM7_A	OUTPUTXBAR5	EQEP1_A			SCIC_TX	SPIA_CLK	ERRORSTS	I2CB_SDA		
GPIO29	SCIA_TX		EPWM7_B	OUTPUTXBAR6	EQEP1_B			SCIC_RX	SPIA_STE	ERRORSTS	I2CB_SCL		
GPIO32	I2CA_SDA	EQEP1_INDEX	SPIA_CLK	EPWM4_B	SCIC_TX			CANA_TX		ADCSOCBO			
GPIO33	I2CA_SCL			OUTPUTXBAR4	SCIC_RX			CANA_RX		ADCSOCAO			
GPIO35	SCIA_RX	SPIA_SOMI	I2CA_SDA	CANA_RX		SCIC_RX	EQEP1_A		EPWM5_B			TDI	
GPIO37	OUTPUTXBAR2	SPIA_STE	I2CA_SCL	SCIA_TX	CANA_TX	SCIC_TX	EQEP1_B		EPWM5_A			TDO	
GPIO39										SYNCOUT	EQEP1_INDEX		
GPIO40				EPWM2_B			SCIB_TX	EQEP1_A					
GPIO41	EPWM7_A			EPWM2_A			SCIB_RX	EQEP1_B					
GPIO224				OUTPUTXBAR3	SPIA_SIMO		EPWM1_A	CANA_TX	EQEP1_A		SCIC_TX		
GPIO226				EPWM6_A	SPIA_CLK		EPWM1_B		EQEP1_STROBE		SCIC_RX		
GPIO227	I2CB_SCL		EPWM3_A	OUTPUTXBAR1	EPWM2_B								
GPIO228			ADCSOCAO	CANA_TX	SPIA_SOMI		EPWM2_B		EQEP1_B				
GPIO230	I2CB_SDA		EPWM3_B	CANA_RX	EPWM2_A	I2CA_SDA							

Table 5-6. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO242				OUTPUTXBAR2	SPIA_STE		EPWM4_A	CANA_RX	EQEP1_INDEX				
AIO225													
AIO231													
AIO232													
AIO233													
AIO237													
AIO238													
AIO239													
AIO241													
AIO244													
AIO245													

5.4.2 Digital Inputs on ADC Pins (AIOs)

GPIOs on port H are multiplexed with analog pins. These are also referred to as AIOs. These pins can only function in input mode. By default, these pins will function as analog pins and the GPIOs are in a high-Z state. The GPHAMSEL register is used to configure these pins for digital or analog operation.

Note

If digital signals with sharp edges (high dv/dt) are connected to the AIOs, cross-talk can occur with adjacent analog signals. The user should therefore limit the edge rate of signals connected to AIOs if adjacent channels are being used for analog functions.

5.4.3 Digital Inputs and Outputs on ADC Pins (AGPIOs)

Some GPIOs are multiplexed with analog pins and have digital input and output functionality. These are also referred to as AGPIOs. Unlike AIOs, AGPIOs have full input and output capability.

By default, the AGPIOs are not connected and must be configured. Table 5-7 shows how to configure the AGPIOs. To enable the analog functionality, set the register AGPIOCTRLx from analog subsystem. To enable the digital functionality, set the register GPxAMSEL from the *General-Purpose Input/Output (GPIO)* chapter.

Table 5-7. AGPIO Configuration

AGPIOCTRLx.GPIOy (Default = 0)	GPxAMSEL.GPIOy (Default = 1)	Pin Connected To:	
		ADC	GPIOy
0	0	-	Yes
0	**1**	**-** (1)	**-** (1)
1	0	-	Yes
1	1	Yes	-

(1) By default there are no signals connected to AGPIO pins. One of the other rows in the table must be chosen for pin functionality.

Note

If digital signals with sharp edges (high dv/dt) are connected to the AGPIOs, cross-talk can occur with adjacent analog signals. The user can therefore limit the edge rate of signals connected to AGPIOs, if adjacent channels are being used for analog functions.

5.4.4 GPIO Input X-BAR

The Input X-BAR is used to route signals from a GPIO to many different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts (see Figure 5-6). Table 5-8 lists the input X-BAR destinations. For details on configuring the Input X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*.

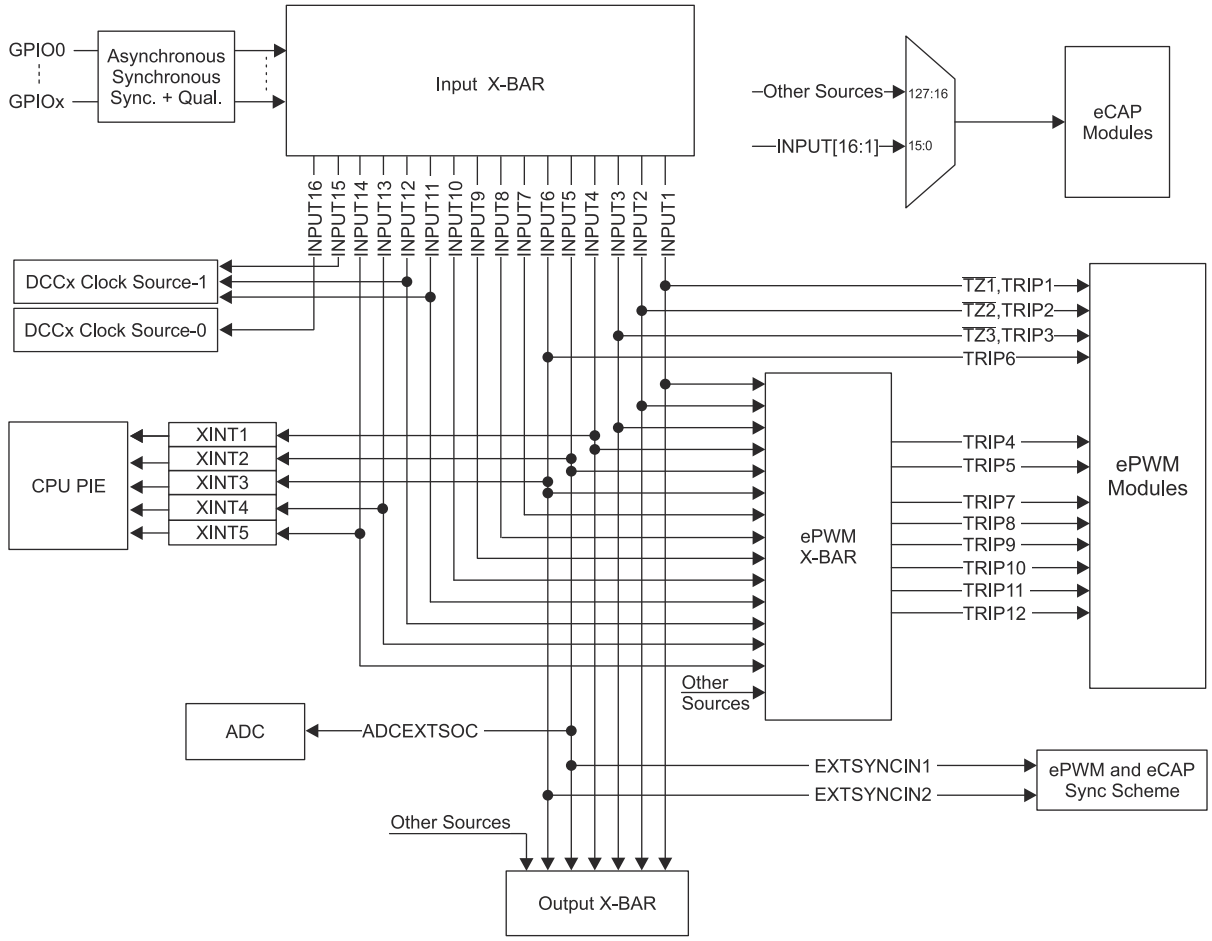


Figure 5-6. Input X-BAR

Table 5-8. Input X-BAR Destinations

INPUT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ECAP	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
EPWM X-BAR	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes		
OUTPUT X-BAR	Yes	Yes	Yes	Yes	Yes	Yes										
CPU XINT				XINT1	XINT2	XINT3							XINT4	XINT5		
EPWM TRIP	TZ1, TRIP1	TZ2, TRIP2	TZ3, TRIP3			TRIP6										
ADC START OF CONVERSION					ADCEX TSOC											
EPWM / ECAP SYNC					EXTSY NCIN1	EXTSY NCIN2										
DCCx											CLK 1	CLK 1			CLK1	CLK0
EPG													EPG1 IN1	EPG1 IN2	EPG1 IN3	EPG1 IN4

5.4.5 GPIO Output X-BAR and ePWM X-BAR

The Output X-BAR has eight outputs that can be selected on the GPIO mux as OUTPUTXBARx. The ePWM X-BAR has eight outputs that are connected to the TRIPx inputs of the ePWM. The sources for the Output X-BAR and ePWM X-BAR are shown in Figure 5-7.

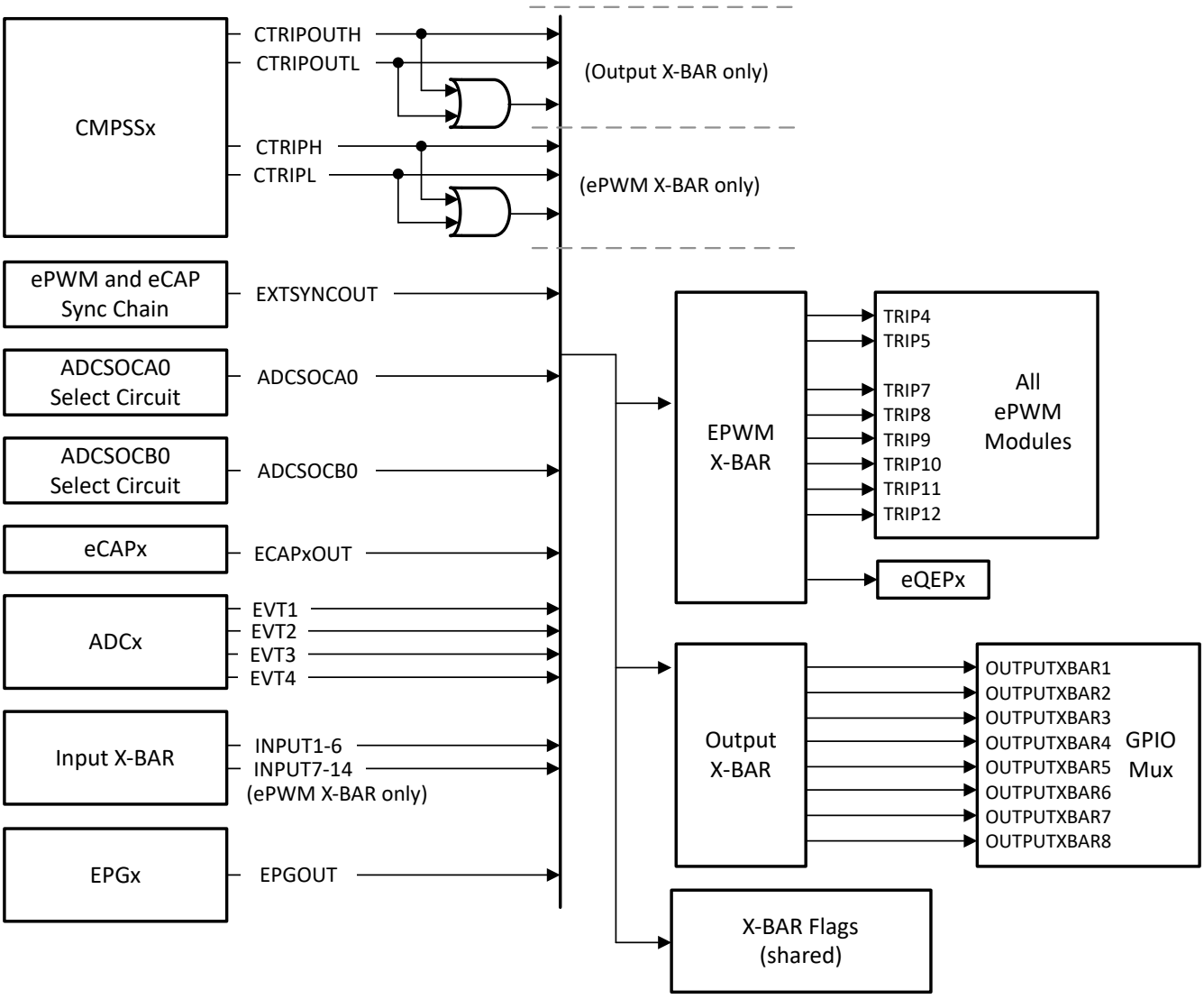


Figure 5-7. Output X-BAR and ePWM X-BAR Sources

5.5 GPIO and ADC Allocation

Table 5-9. GPIO and ADC Allocation

FEATURE	64 PM	64 PM with VREGENZ (64 VPM)	48 PT	48 RGZ	32 RHB
GPIO					
GPIO	23	22	13	16	10
AGPIO	11	11	8	8	5
JTAG and Oscillator GPIO	4 (TDI, TDO, X1, X2)				
Total GPIO	38	37	25	28	19
AIO	10	10	9	9	6
Total GPIO and AIO	48	47	34	37	25
ADC					
ADC channels	10	10	9	9	6
AGPIO	11	11	8	8	5
Total ADC channels (single-ended)	21	21	17	17	11

5.6 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. Table 5-10 lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. To avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in Table 5-10 with pullups and pulldowns are always on and cannot be disabled.

Table 5-10. Pins With Internal Pullup and Pulldown

PIN	RESET (XRSn = 0)	DEVICE BOOT	APPLICATION
GPIOx	Pullup disabled	Pullup disabled(1)	Application defined
GPIO35/TDI	Pullup disabled		Application defined
GPIO37/TDO	Pullup disabled		Application defined
TCK	Pullup active		
TMS	Pullup active		
XRSn	Pullup active		
Other pins (including AIOs)	No pullup or pulldown present		

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

5.7 Connections for Unused Pins

For applications that do not need to use all functions of the device, Table 5-11 lists acceptable conditioning for any unused pins. When multiple options are listed in Table 5-11, any option is acceptable. Pins not listed in Table 5-11 must be connected according to Section 5.

Table 5-11. Connections for Unused Pins

SIGNAL NAME	ACCEPTABLE PRACTICE
ANALOG	
VREFHI	Tie to VDDA (applies only if ADC is not used in the application)
VREFLO	Tie to VSSA
Analog input pins	• No Connect • Tie to VSSA • Tie to VSSA through resistor
Analog input pins (shared with GPIO)	• No Connect • Tie to VSSA through resistor
DIGITAL	
GPIOx	• No connection (input mode with internal pullup enabled) • No connection (output mode with internal pullup disabled) • Pullup or pulldown resistor (any value resistor, input mode, and with internal pullup disabled)
GPIO35/TDI	When TDI mux option is selected (default), the GPIO is in Input mode. • Internal pullup enabled • External pullup resistor
GPIO37/TDO	When TDO mux option is selected (default), the GPIO is in Output mode only during JTAG activity; otherwise, it is in a tri-state condition. The pin must be biased to avoid extra current on the input buffer. • Internal pullup enabled • External pullup resistor
TCK	• No Connect • Pullup resistor
TMS	Pullup resistor
GPIO19/X1	Turn XTAL off and: • Input mode with internal pullup enabled • Input mode with external pullup or pulldown resistor • Output mode with internal pullup disabled
GPIO18/X2	Turn XTAL off and: • Input mode with internal pullup enabled • Input mode with external pullup or pulldown resistor • Output mode with internal pullup disabled
POWER AND GROUND	
VDD	All VDD pins must be connected per Section 5.3. Pins should not be used to bias any external circuits.
VDDA	If a dedicated analog supply is not used, tie to VDDIO.
VDDIO	All VDDIO pins must be connected per Section 5.3.
VSS	All VSS pins must be connected to board ground.
VSSA	If an analog ground is not used, tie to VSS.

6 Specifications

6.1 Absolute Maximum Ratings

over recommended operating conditions (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage	VDD with respect to VSS	–0.3	1.5	V
	VDDIO with respect to VSS	–0.3	4.6	
	VDDA with respect to VSSA	–0.3	4.6	
Input voltage	V_{IN} (3.3 V)	–0.3	4.6	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current	Digital/analog input (per pin), I_{IK} (V_{IN} < VSS/VSSA or V_{IN} > VDDIO/VDDA)(4)	–20	20	mA
	Total for all inputs, $I_{IKTOTAL}$ (V_{IN} < VSS/VSSA or V_{IN} > VDDIO/VDDA)	–20	20	
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Operating junction temperature	T_J	–40	155	°C
Storage temperature(3)	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.
(4) Continuous clamp current per pin is ±2 mA. Do not operate in this condition continuously as V_{DDIO}/V_{DDA} voltage may internally rise and impact other electrical specifications.

6.2 ESD Ratings

				VALUE	UNIT
F2800137, F2800135, F2800133 in 64-pin PM package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 64-pin PM: 1, 16, 17, 32, 33, 48, 49, 64	±750	
F2800137, F2800135, F2800133, F2800132 in 48-pin PT package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 48-pin PT: 1, 12, 13, 24, 25, 36, 37, 48	±750	
F2800137, F2800135, F2800133, F2800132 in 48-pin RGZ package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 48-pin RGZ: 1, 12, 13, 24, 25, 36, 37, 48	±750	
F2800137, F2800135, F2800133, F2800132 in 32-pin RHB package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 32-pin RHB: 1, 8, 9, 16, 17, 24, 25, 32	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, VDDIO and VDDA	Internal BOR enabled(3)	$V_{BOR-VDDIO}$(MAX) + V_{BOR-GB} (2)	3.3	3.63	V
	Internal BOR disabled	2.8	3.3	3.63	
Device supply voltage, VDD		1.14	1.2	1.32	V
Device ground, VSS			0		V
Analog ground, VSSA			0		V
SR_{SUPPLY}	Supply ramp rate of VDDIO, VDD, VDDA with respect to VSS.(4)				
V_{IN}	Digital input voltage	VSS – 0.3		VDDIO + 0.3	V
	Analog input voltage	VSSA – 0.3		VDDA + 0.3	V
Junction temperature, T_J (1)		–40		140	°C
Free-Air temperature, T_A		–40		125	°C

(1) Operation above T_J = 105°C for extended duration will reduce the lifetime of the device. See *Calculating Useful Lifetimes of Embedded Processors* for more information.
(2) See the *Power Management Module (PMM)* section.
(3) Internal BOR is enabled by default.
(4) See the Power Management Module Operating Conditions table.

6.4 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations. Section 6.4.1 lists the system current consumption values.

6.4.1 System Current Consumption - VREG Enable - Internal Supply

Over recommended operating conditions (unless otherwise noted)
TYP : V_{nom}

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPERATING MODE							
I_{DDIO} (3)	VDDIO current consumption during operational usage	This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency. This includes Core supply current with Internal Vreg Enabled. - CPU is running from RAM - Flash is powered up - X1/X2 crystal is powered up - PLL is enabled, SYSCLK=Max Device frequency - Analog modules are powered up - Outputs are static without DC Load - Inputs are static high or low	30 ℃		36		mA
			85 ℃			44	mA
			125 ℃			50	mA
I_{DDA}	VDDA current consumption during operational usage		30 ℃		1.6		mA
			85 ℃			2	mA
			125 ℃			2.5	mA
IDLE MODE							
I_{DDIO}	VDDIO current consumption while device is in Idle mode	- CPU is in IDLE mode - Flash is powered down - PLL is Enabled, SYSCLK=Max Device Frequency, CPUCLK is gated - X1/X2 crystal is powered up - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low	30 ℃		17		mA
			85 ℃			21	mA
			125 ℃			27	mA
I_{DDA}	VDDA current consumption while device is in Idle mode		30 ℃		0.01		mA
			85 ℃			0.1	mA
			125 ℃			0.1	mA
STANDBY MODE (PLL Enabled)							
I_{DDIO}	VDDIO current consumption while device is in Standby mode	- CPU is in STANDBY mode - Flash is powered down - PLL is Enabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low	30 ℃		7		mA
			85 ℃			11	mA
			125 ℃			17	mA
I_{DDA}	VDDA current consumption while device is in Standby mode		30 ℃		0.01		mA
			85 ℃			0.1	mA
			125 ℃			0.1	mA

6.4.1 System Current Consumption - VREG Enable - Internal Supply (continued)

Over recommended operating conditions (unless otherwise noted)
TYP : V_{nom}

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STANDBY MODE (PLL Disabled)							
I_{DDIO}	VDDIO current consumption while device is in Standby mode	- CPU is in STANDBY mode - Flash is powered down - PLL is Disabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low	30 ℃		5.8		mA
			85 ℃			9	mA
			125 ℃			15.5	mA
I_{DDA}	VDDA current consumption while device is in Standby mode		30 ℃		0.01		mA
			85 ℃			0.1	mA
			125 ℃			0.1	mA
HALT MODE							
I_{DDIO}	VDDIO current consumption while device is in Halt mode	- CPU is in HALT mode - Flash is powered down - PLL is Disabled, SYSCLK and CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low	30 ℃		5		mA
			85 ℃			8.2	mA
			125 ℃			15	mA
I_{DDA}	VDDA current consumption while device is in Halt mode		30 ℃		0.01		mA
			85 ℃			0.1	mA
			125 ℃			0.1	mA
FLASH ERASE/PROGRAM							
I_{DDIO}	VDDIO current consumption during Erase/Program cycle(1)	- CPU is running from RAM - Flash going through continuous Program/Erase operation - PLL is enabled, SYSCLK at 120 MHz. - Peripheral clocks are turned OFF. - X1/X2 crystal is powered up - Analog is powered down - Outputs are static without DC Load - Inputs are static high or low			45	65	mA
I_{DDA}	VDDA current consumption during Erase/Program cycle				0.1	2.5	mA
RESET MODE							
I_{DDIO}	VDDIO current consumption while reset is active(2)	Device is under Reset	30 ℃		7		mA
			85 ℃		10.7		mA
			125 ℃		17		mA
I_{DDA}	VDDA current consumption while reset is active(2)		30 ℃		0.01		mA
			85 ℃		0.01		mA
			125 ℃		0.01		mA

(1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.
(2) This is the current consumption while reset is active (that is, XRSn is low).
(3) *Internal Supply* table I_{DDIO} current consumption values are lower than I_{DDIO} + I_{DD} current consumption from *External Supply* table. This is because MAX column of *Internal Supply* table has the core regulated to VDD NOM, while MAX column of *External Supply* table has the core regulated to VDD MAX (from *Recommended Operating Conditions* table).

6.4.2 System Current Consumption - VREG Disable - External Supply

Over recommended operating conditions (unless otherwise noted)
TYP : V_{nom}

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPERATING MODE							
I_{DD}	VDD current consumption during operational usage	This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency. This includes Core supply current with Internal Vreg Enabled. - CPU is running from RAM - Flash is powered up - X1/X2 crystal is powered up - PLL is enabled, SYSCLK=Max Device frequency - Analog modules are powered up - Outputs are static without DC Load - Inputs are static high or low	30 ℃		35		mA
			85 ℃			42	mA
			125 ℃			49.5	mA
I_{DDIO}	VDDIO current consumption during operational usage		30 ℃		5.8		mA
			85 ℃		5.8		mA
			125 ℃		5.8		mA
I_{DDA}	VDDA current consumption during operational usage		30 ℃		1.6		mA
			85 ℃			2	mA
			125 ℃			2.5	mA
IDLE MODE							
I_{DD}	VDD current consumption while device is in Idle mode	- CPU is in IDLE mode - Flash is powered down - PLL is Enabled, SYSCLK=Max Device Frequency, CPUCLK is gated - X1/X2 crystal is powered up - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low	30 ℃		14		mA
			85 ℃			19	mA
			125 ℃			26	mA
I_{DDIO}	VDDIO current consumption while device is in Idle mode		30 ℃		3.9		mA
			85 ℃		3.9		mA
			125 ℃		3.9		mA
I_{DDA}	VDDA current consumption while device is in Idle mode		30 ℃		0.01		mA
			85 ℃			0.1	mA
			125 ℃			0.1	mA
STANDBY MODE (PLL Enabled)							
I_{DD}	VDD current consumption while device is in Standby mode	- CPU is in STANDBY mode - Flash is powered down - PLL is Enabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low	30 ℃		3.6		mA
			85 ℃			7.6	mA
			125 ℃			17	mA
I_{DDIO}	VDDIO current consumption while device is in Standby mode		30 ℃		3.9		mA
			85 ℃		3.9		mA
			125 ℃		3.9		mA
I_{DDA}	VDDA current consumption while device is in Standby mode		30 ℃		0.01		mA
			85 ℃			0.1	mA
			125 ℃			0.1	mA

6.4.2 System Current Consumption - VREG Disable - External Supply (continued)

Over recommended operating conditions (unless otherwise noted)
TYP : V_{nom}

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STANDBY MODE (PLL Disabled)							
I_{DD}	VDD current consumption while device is in Standby mode	- CPU is in STANDBY mode - Flash is powered down - PLL is Disabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low	30 ℃		2.6		mA
			85 ℃			6.6	mA
			125 ℃			13.5	mA
I_{DDIO}	VDDIO current consumption while device is in Standby mode		30 ℃		3.1		mA
			85 ℃		3.1		mA
			125 ℃		3.1		mA
I_{DDA}	VDDA current consumption while device is in Standby mode		30 ℃		0.01		mA
			85 ℃			0.1	mA
			125 ℃			0.1	mA
HALT MODE							
I_{DD}	VDD current consumption while device is in Halt mode	- CPU is in HALT mode - Flash is powered down - PLL is Disabled, SYSCLK and CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low	30 ℃		2.4		mA
			85 ℃			6.2	mA
			125 ℃			13.2	mA
I_{DDIO}	VDDIO current consumption while device is in Halt mode		30 ℃		3.1		mA
			85 ℃		3.1		mA
			125 ℃		3.1		mA
I_{DDA}	VDDA current consumption while device is in Halt mode		30 ℃		0.01		mA
			85 ℃			0.1	mA
			125 ℃			0.1	mA
FLASH ERASE/PROGRAM							
I_{DD}	VDD current consumption during Erase/Program cycle(1)	- CPU is running from RAM - Flash going through continuous Program/Erase operation - PLL is enabled, SYSCLK at 100 MHz. - Peripheral clocks are turned OFF. - X1/X2 crystal is powered up - Analog is powered down - Outputs are static without DC Load - Inputs are static high or low			32	50	mA
I_{DDIO}	VDDIO current consumption during Erase/Program cycle(1)				13	17	mA
I_{DDA}	VDDA current consumption during Erase/Program cycle				0.1	2.5	mA

6.4.2 System Current Consumption - VREG Disable - External Supply (continued)

Over recommended operating conditions (unless otherwise noted)
TYP : V_{nom}

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RESET MODE							
I_{DD}	VDD current consumption while reset is active(2)	Device is under Reset	30 ℃		2.2		mA
			85 ℃		4.2		mA
			125 ℃		8.7		mA
I_{DDIO}	VDDIO current consumption while reset is active(2)		30 ℃		5		mA
			85 ℃		5		mA
			125 ℃		5		mA
I_{DDA}	VDDA current consumption while reset is active(2)		30 ℃		0.01		mA
			85 ℃		0.01		mA
			125 ℃		0.01		mA

(1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.
(2) This is the current consumption while reset is active (that is, XRSn is low).

6.4.3 Operating Mode Test Description

Section 6.4.1, Section 6.4.2, and Section 6.4.5.1 list the current consumption values for the operational mode of the device. The operational mode provides an estimation of what an application might encounter. The test condition for these measurements has the following properties:

- Code is executing from RAM.
- FLASH is read and kept in active state.
- No external components are driven by I/O pins.
- All peripherals have clocks enabled.
- All CPUs are actively executing code.
- All analog peripherals are powered up. ADCs and DACs are periodically converting.

6.4.4 Current Consumption Graphs

The below graphs show a typical representation of the relationship between frequency, temperature, supply, and current consumption on the device. Actual results vary based on the system implementation and conditions.

Figure 6-2 shows the typical operating current profile across temperature and operating mode for internal supply, with data based on the *System Current Consumption - VREG Enable - Internal Supply* table (30 °C data is taken at VNOM with higher temperature data points taken at VMAX). Figure 6-3 shows the typical operating current profile across temperature and operating mode for external supply, with data based on the *System Current Consumption - VREG Enable - External Supply* table (30 °C data is taken at VNOM with higher temperature data points taken at VMAX).

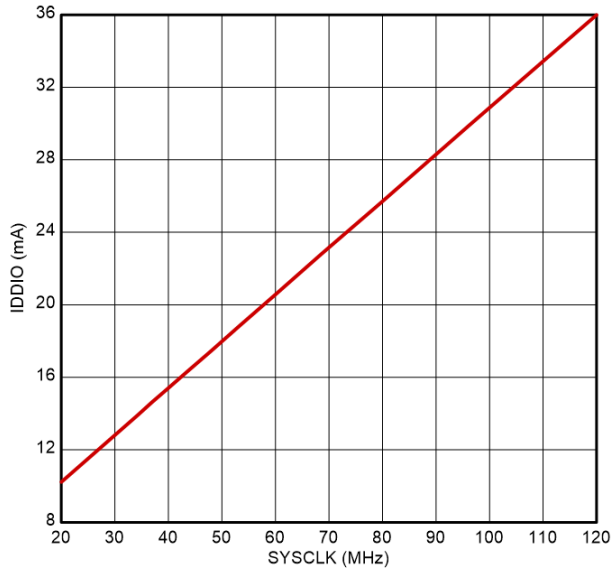


Figure 6-1. Operating Current Versus Frequency

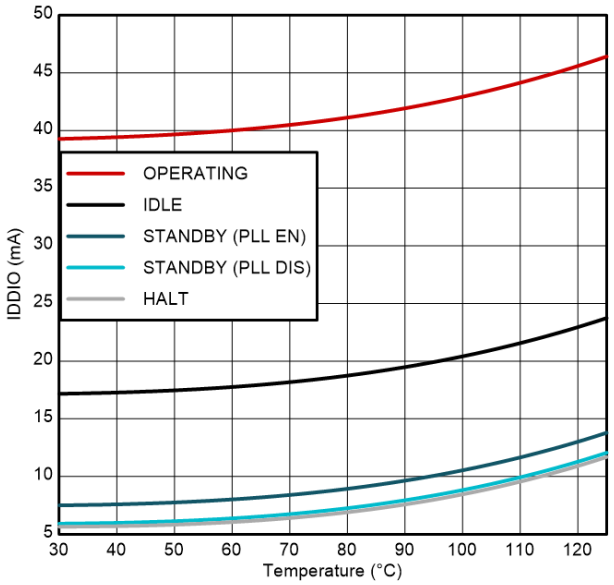


Figure 6-2. Current Versus Temperature - Internal Supply

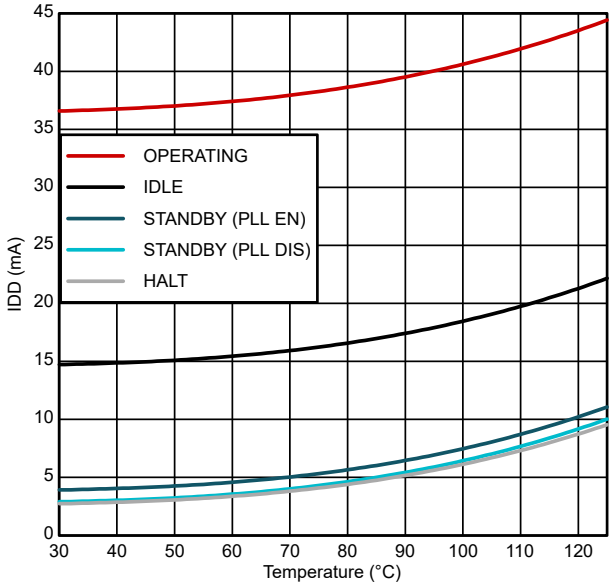


Figure 6-3. Current Versus Temperature - External Supply

6.4.5 Reducing Current Consumption

The F280013x devices provide some methods to reduce the device current consumption:

- One of the two low-power modes—IDLE or STANDBY—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- Each peripheral has an individual clock-enable bit (PCLKCRx). Reduced current consumption may be achieved by turning off the clock to any peripheral that is not used in a given application. Section 6.4.5.1 lists the typical current reduction that may be achieved by disabling the clocks using the PCLKCRx register.
- To realize the lowest VDDA current consumption in an LPM, see the Analog-to-Digital Converter (ADC) chapter of the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual* to ensure each module is powered down as well.

6.4.5.1 Typical Current Reduction per Disabled Peripheral

For peripherals with multiple instances, the current quoted is for all modules combined.

PERIPHERAL	I_{DDIO} CURRENT REDUCTION (mA)
ADC(1)	1.32
CMPSS_LITE(1)	0.57
CMPSS(1)	0.31
CPU TIMER	0.06
DCAN	1.25
DCC	0.08
eCAP	0.12
EPG	0.32
ePWM	4.13
HRPWM	1.98
eQEP	0.18
SCI	0.50
I2C	0.51
SPI	0.11

(1) This current represents the current drawn by the digital portion of the each module.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital and Analog IO							
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MIN	VDDIO * 0.8			V
			I_{OH} = –100 µA	VDDIO – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX			0.4	V
			I_{OL} = 100 µA			0.2	
I_{OH}	High-level output source current for all output pins			–4			mA
I_{OL}	Low-level output sink current for all output pins					4	mA
R_{OH}	High-level output impedance for all output pins		VOH=VDDS-0.4V	50	65	96	Ω
R_{OL}	Low-level output impedance for all output pins		VOL=0.4V	48	60	84	Ω
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
$V_{HYSTERESIS}$	Input hysteresis (AIO)			125			mV
	Input hysteresis (GPIO)			125			
$I_{PULLDOWN}$	Input current	Pins with pulldown	VDDIO = 3.3 V V_{IN} = VDDIO		120		µA
I_{PULLUP}	Input current	Digital inputs with pullup enabled(1)	VDDIO = 3.3 V V_{IN} = 0 V		160		µA
$R_{PULLDOWN}$	Weak pulldown resistance			22.66	31.49	61.55	kΩ
R_{PULLUP}	Weak pullup resistance			19.89	29.45	53.63	kΩ
I_{LEAK}	Pin leakage	Digital inputs	Pullups and outputs disabled 0 V ≤ V_{IN} ≤ VDDIO			0.1	µA
		Analog pins	Analog drivers disabled 0 V ≤ V_{IN} ≤ VDDA			0.1	
C_I	Input capacitance	Digital inputs			2		pF
		Analog pins(2)					
VREG and BOR							
VREG, POR, BOR(4)							

(1) See Pins With Internal Pullup and Pulldown table for a list of pins with a pullup or pulldown.
(2) The analog pins are specified separately; see the Per-Channel Parasitic Capacitance tables that are in the ADC Input Model section.
(3) See the *Power Management Module (PMM)* section.

6.6 Thermal Resistance Characteristics for PM Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	21.9
	Junction-to-case thermal resistance, bottom	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	39.6
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	62.5
Psi_{JT}	Junction-to-package top	1.1
Psi_{JB}	Junction-to-board	39.2

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.7 Thermal Resistance Characteristics for PT Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	21.2
	Junction-to-case thermal resistance, bottom	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	35.1
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	60.1
Psi_{JT}	Junction-to-package top	0.9
Psi_{JB}	Junction-to-board	34.7

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.8 Thermal Resistance Characteristics for RGZ Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	18.6
	Junction-to-case thermal resistance, bottom	2.8
$R\Theta_{JB}$	Junction-to-board thermal resistance	10.7
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	28.4
Psi_{JT}	Junction-to-package top	0.2
Psi_{JB}	Junction-to-board	10.7

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.9 Thermal Resistance Characteristics for RHB Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	22.5
	Junction-to-case thermal resistance, bottom	2.8
$R\Theta_{JB}$	Junction-to-board thermal resistance	12.3
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	31.3
Psi_{JT}	Junction-to-package top	0.3
Psi_{JB}	Junction-to-board	12.2

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.10 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report *Semiconductor and IC Package Thermal Metrics* helps to understand the thermal metrics and definitions.

6.11 System

6.11.1 Power Management Module (PMM)

6.11.1.1 Introduction

The Power Management Module (PMM) handles all the power management functions required for device operation.

6.11.1.2 Overview

The block diagram of the PMM is shown in Figure 6-4. As can be seen, the PMM comprises of various subcomponents, which are described in the subsequent sections.

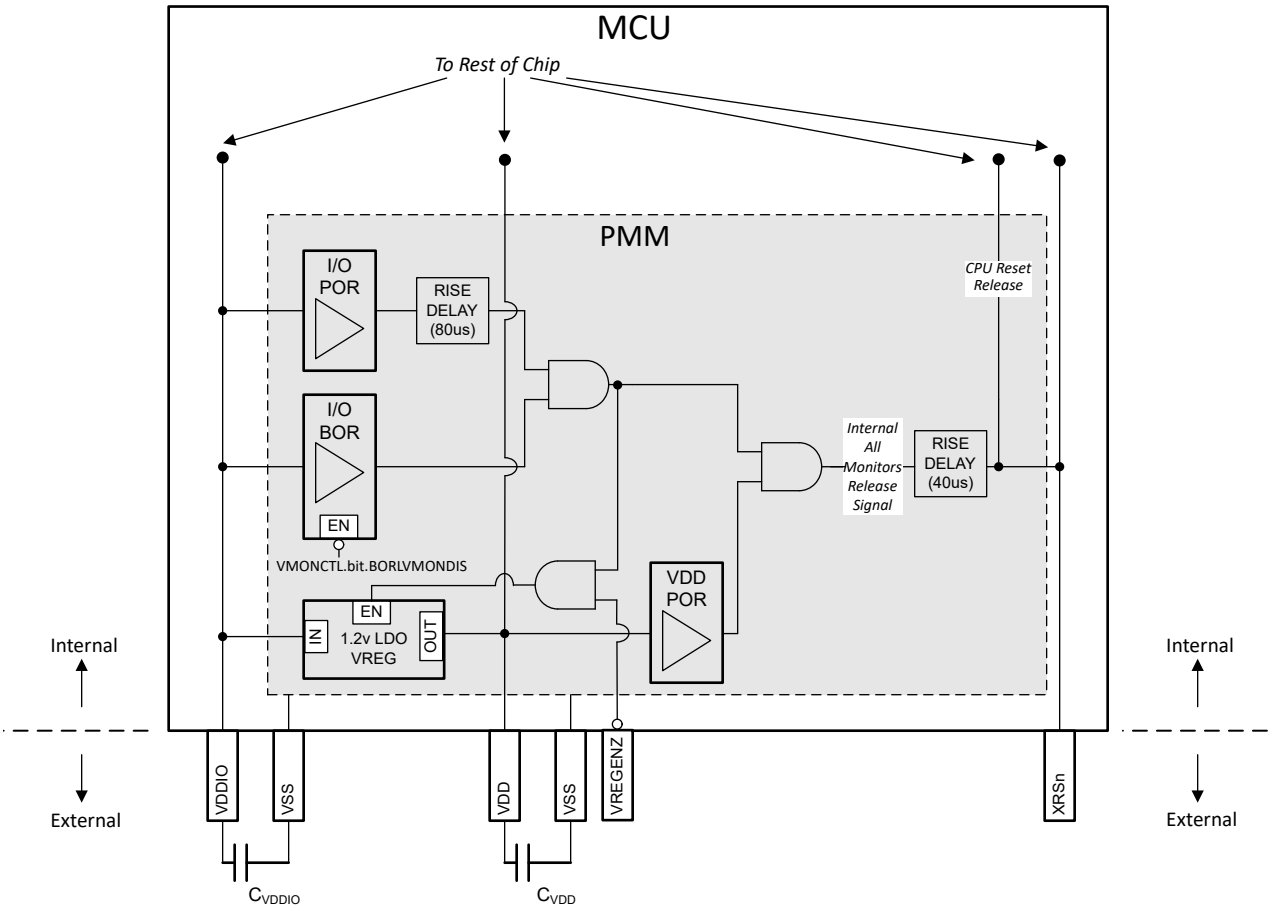


Figure 6-4. PMM Block Diagram

6.11.1.2.1 Power Rail Monitors

The PMM has voltage monitors on the supply rails that release the XRSn signal high once the voltages cross the set threshold during power up. They also function to trip the XRSn signal low if any of the voltages drop below the programmed levels. The various voltage monitors are described in subsequent sections.

Note

Not all the voltage monitors are supported for device operation in an application after boot up. In the case where a voltage monitor is not supported, an external supervisor is recommended if the device needs supply voltage monitoring while the application is running.

The three voltage monitors (I/O POR, I/O BOR, VDD POR) all have to release their respective outputs before the device begins operation (that is, XRSn goes high). However, if any of the voltage monitors trips, XRSn is driven low. The I/Os are held in high impedance when any of the voltage monitors trip.

6.11.1.2.1.1 I/O POR (Power-On Reset) Monitor

The I/O POR monitor supervises the VDDIO rail. During power up, this is the first monitor to release (that is, first to untrip) on VDDIO.

6.11.1.2.1.2 I/O BOR (Brown-Out Reset) Monitor

The I/O BOR monitor also supervises the VDDIO rail. During power up, this is the second monitor to release (that is, second to untrip) on VDDIO. This monitor has a tighter tolerance compared to the I/O POR.

Any drop in voltage below the recommended operating voltages will trip the I/O BOR and reset the device but this can be disabled by setting VMONCTL.bit.BORLVMONDIS to 1. The I/O BOR can only be disabled after the device has fully booted up. If the I/O BOR is disabled, the I/O POR will reset the device for voltage drops.

Note

The level at which the I/O POR trips is well below the minimum recommended voltage for VDDIO, and therefore should not be used for device supervision.

Figure 6-5 shows the operating region of the I/O BOR.

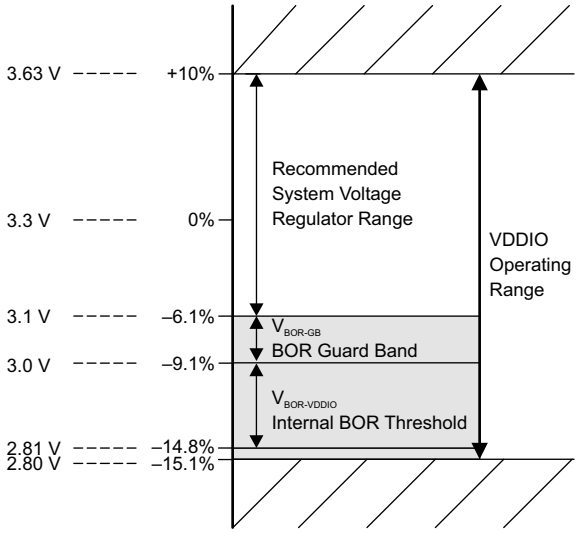


Figure 6-5. I/O BOR Operating Region

6.11.1.2.1.3 VDD POR (Power-On Reset) Monitor

The VDD POR monitor supervises the VDD rail. During power up, this monitor releases (that is, untrips) once the voltage crosses the programmed trip level on VDD.

Note

VDD POR is programmed at a level below the minimum recommended voltage for VDD, and therefore it should not be relied upon for VDD supervision if that is required in the application.

6.11.1.2.2 External Supervisor Usage

VDDIO Monitoring: The I/O BOR is supported for application use, so an external supervisor is not required to monitor the I/O rail.

VDD Monitoring:

- VDD supplied from the internal VREG: The VDD supply is derived from the VDDIO supply. The VREG is designed in such a way that a valid VDDIO supply(monitored by the IO BOR) implies a valid VDD supply.
- VDD supplied from an external supply: The VDD POR is not supported for application use. If VDD monitoring is required by the application, an external supervisor can be used to monitor the VDD rail.

Note

The use of an external supervisor with the internal VREG is not supported.If VDD monitoring is required by the application, a package with a VREGENZ pin must be used to power VDD externally.

6.11.1.2.3 Delay Blocks

The delay blocks in the path of the voltage monitors work together to delay the release time between the voltage monitors and XRSn. These delays are designed to make sure that the voltages are stable when XRSn releases in external VREG mode. The delay blocks are only active during power up (that is, when VDDIO and VDD are ramping up).

The delay blocks contribute to the minimum slew rates specified in Power Management Module Electrical Data and Timing for the power rails.

Note

The delay numbers specified in the block diagram are typical numbers.

6.11.1.2.4 Internal 1.2-V LDO Voltage Regulator (VREG)

The internal VREG is supplied by the VDDIO rail and can generate the 1.2 V required to power the VDD pins. It is enabled by tying the VREGENZ pin low. Although the internal VREG eliminates the need to use an external supply for VDD, decoupling capacitors are still required on the VDD pins for VREG stability and transients. See the *VDD Decoupling* section for details.

6.11.1.2.5 VREGENZ

The VREGENZ (VREG disable) pin controls the state of the internal VREG. To enable the internal VREG, connect the VREGENZ pin to a logic low voltage. For applications supplying VDD externally (external VREG), disable the internal VREG by tying the VREGENZ pin high.

Note

Not all device packages have VREGENZ pinned out. For packages without VREGENZ, external VREG mode is not supported.

6.11.1.3 External Components

6.11.1.3.1 Decoupling Capacitors

VDDIO and VDD require decoupling capacitors for correct operation. The requirements are outlined in subsequent sections.

6.11.1.3.1.1 VDDIO Decoupling

Place a minimum amount of decoupling capacitance on VDDIO. See the C_{VDDIO} parameter in Power Management Module Electrical Data and Timing. The actual amount of decoupling capacitance to use is a requirement of the power supply driving VDDIO. Either of the configurations outlined below is acceptable:

- **Configuration 1:** Place a decoupling capacitor on each VDDIO pin per the C_{VDDIO} parameter.
- **Configuration 2:** Install a single decoupling capacitor that is the equivalent of C_{VDDIO} * VDDIO pins.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.11.1.3.1.2 VDD Decoupling

Place a minimum amount of decoupling capacitance on VDD. See the C_{VDD} TOTAL parameter in Power Management Module Electrical Data and Timing.

In external VREG mode, the actual amount of decoupling capacitance to use is a requirement of the power supply driving VDD.

Either of the configurations outlined below is acceptable:

- **Configuration 1:** Divide C_{VDD} TOTAL across the VDD pins.
- **Configuration 2:** Install a single decoupling capacitor with value of C_{VDD} TOTAL.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.11.1.4 Power Sequencing

6.11.1.4.1 Supply Pins Ganging

Connecting all 3.3-V rails together and supplying from a single source are strongly recommended. This list includes:

- VDDIO
- VDDA

In addition, connect all power pins to avoid leaving any unconnected.

In external VREG mode, the VDD pins should be tied together and supplied from a single source.

In internal VREG mode, tying the VDD pins together is optional as long as each VDD pin has a capacitor connected to pin. See the *VDD Decoupling* section for VDD decoupling configurations.

The analog modules on the device have fairly high PSRR; therefore, in most cases, noise on VDDA will have to exceed the recommended operating conditions of the supply rails before the analog modules see performance degradation. Therefore, supplying VDDA separately typically offers minimal benefits. Nevertheless, for the purposes of noise improvement, placing a pi filter between VDDIO and VDDA is acceptable.

Note

All the supply pins per rail are tied together internally. For example, all VDDIO pins are tied together internally, all VDD pins are tied together internally, and so forth.

6.11.1.4.2 Signal Pins Power Sequence

Before powering the device, do not apply voltage larger than 0.3 V above VDDIO or 0.3 V below VSS to any digital pin and 0.3 V above VDDA or 0.3 V below VSSA to any analog pin (including VREFHI). Simply, the signal pins should only be driven after XRSn goes high, provided all the 3.3-V rails are tied together. This sequencing is still required even if VDDIO and VDDA are not tied together.

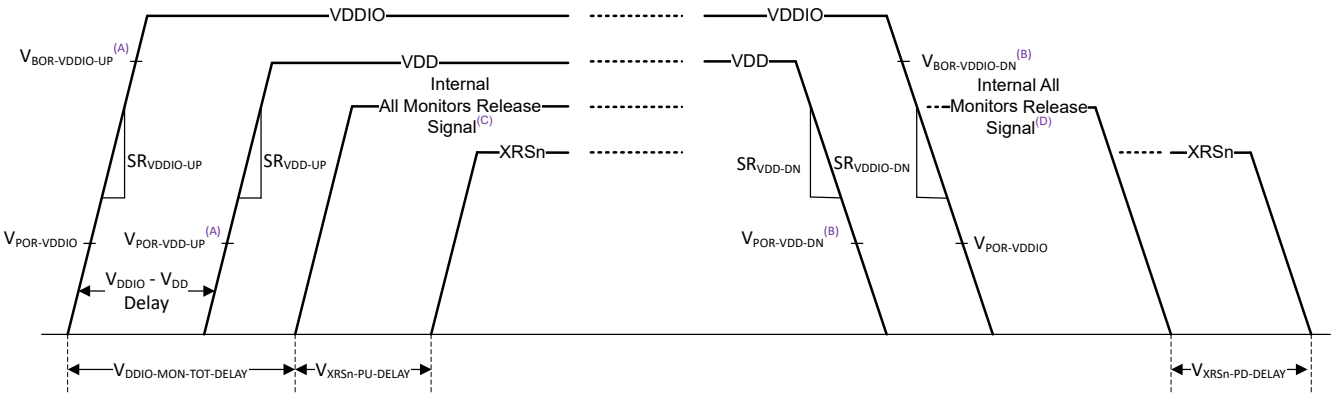
CAUTION

If the above sequence is violated, device malfunction and possibly damage can occur as current will flow through unintended parasitic paths in the device.

6.11.1.4.3 Supply Pins Power Sequence

6.11.1.4.3.1 External VREG/VDD Mode Sequence

Figure 6-6 depicts the power sequencing requirements for external VREG mode. The values for all the parameters indicated can be found in Power Management Module Electrical Data and Timing.



A. This trip point is the trip point before XRSn releases. See the Power Management Module Characteristics table.
B. This trip point is the trip point after XRSn releases. See the Power Management Module Characteristics table.
C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the PMM Block Diagram.
D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the PMM Block Diagram.

Figure 6-6. External VREG Power Up Sequence

- **For Power Up:**
  1. VDDIO (that is, the 3.3-V rail) should come up first with the minimum slew rate specified.
  2. VDD (that is, the 1.2-V rail) should come up next with the minimum slew rate specified.
  3. The time delta between the VDDIO rail coming up and when the VDD rail can come up is also specified.
  4. After the times specified by $V_{DDIO\text{-}MON\text{-}TOT\text{-}DELAY}$ and $V_{XRSN\text{-}PD\text{-}DELAY}$, XRSn will be released and the device starts the boot-up sequence.
  5. The I/O BOR monitor has different release points during power up and power down.
  6. During power up, both VDDIO and VDD rails have to be up before XRSn releases.
- **For Power Down:**
  1. There is no requirement between VDDIO and VDD on which should power down first; however, there is a minimum slew rate specification.
  2. The I/O BOR monitor has different release points during power up and power down.
  3. Any of the POR or BOR monitors that trips during power down will cause XRSn to go low after $V_{XRSN\text{-}PD\text{-}DELAY}$.

Note

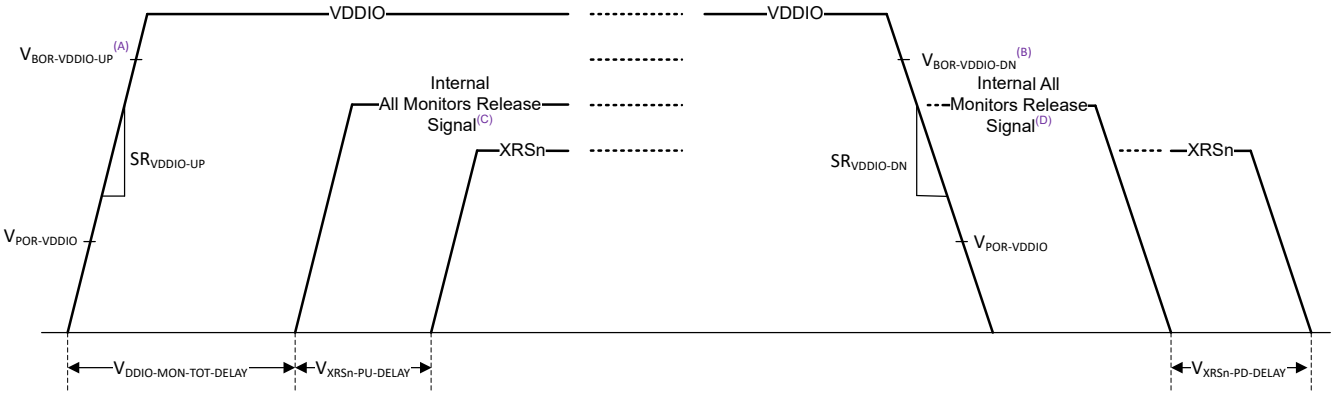
The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.11.1.4.3.2 Internal VREG/VDD Mode Sequence

Figure 6-7 depicts the power sequencing requirements for internal VREG mode. The values for all the parameters indicated can be found in Power Management Module Electrical Data and Timing.



A. This trip point is the trip point before XRSn releases. See the Power Management Module Characteristics table.
B. This trip point is the trip point after XRSn releases. See the Power Management Module Characteristics table.
C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the PMM Block Diagram.
D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the PMM Block Diagram.

Figure 6-7. Internal VREG Power Up Sequence

- **For Power Up:**
  1. VDDIO (that is, the 3.3-V rail) should come up with the minimum slew rate specified.
  2. The Internal VREG powers up after the I/O monitors (I/O POR and I/O BOR) are released.
  3. After the times specified by $V_{DDIO\text{-}MON\text{-}TOT\text{-}DELAY}$ and $V_{XRSN\text{-}PU\text{-}DELAY}$, XRSn will be released and the device starts the boot-up sequence.
  4. The I/O BOR monitor has different release points during power up and power down.
- **For Power Down:**
  1. The only requirement on VDDIO during power down is the slew rate.
  2. The I/O BOR monitor has different release points during power up and power down.
  3. The I/O BOR tripping will cause XRSn to go low after $V_{XRSN\text{-}PD\text{-}DELAY}$ and also power down the Internal VREG.

Note

The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.11.1.4.3.3 Supply Sequencing Summary and Effects of Violations

The acceptable power-up sequence for the rails is summarized below. "Power up" here means the rail in question has reached the minimum recommended operating voltage.

CAUTION
Non-acceptable sequences leads to reliability concerns and possibly damage.

For simplicity, connecting all 3.3-V rails together and following the descriptions in Supply Pins Power Sequence is recommended.

Table 6-1. External VREG Sequence Summary

CASE	RAILS POWER-UP ORDER			ACCEPTABLE
	VDDIO	VDDA	VDD	
A	1	2	3	Yes
B	1	3	2	Yes
C	2	1	3	-
D	2	3	1	-
E	3	2	1	-
F	3	1	2	-
G	1	1	2	Yes
H	2	2	1	-

Table 6-2. Internal VREG Sequence Summary

CASE	RAILS POWER-UP ORDER		ACCEPTABLE
	VDDIO	VDDA	
A	1	2	Yes
B	2	1	-
C	1	1	Yes

Note
The analog modules on the device should only be powered after VDDA has reached the minimum recommended operating voltage.

6.11.1.4.3.4 Supply Slew Rate

VDDIO has a minimum slew rate requirement. If the minimum slew rate is not met, XRSn might toggle a few times until VDDIO crosses the I/O BOR region.

Note
The toggling on XRSn has no adverse effect on the device as boot only starts once XRSn is steadily high. However if XRSn from the device is used to gate the reset signal of other ICs, then the slew rate requirement should be met to prevent this toggling.

VDD has a minimum slew rate requirement in external VREG mode. If the minimum slew rate is not met, the VDD POR may release before the VDD operational minimum voltage is met and the device may not start in a properly reset state.

6.11.1.5 Recommended Operating Conditions Applicability to the PMM

As noted in the *Recommended Operating Conditions* table, the voltage (V_{IN}) of all pins on the device should be kept above VSS – 0.3 V. Negative voltages below this value will inject current into the device, which could cause

abnormal operation. Specific care should be taken for pins near the PMM. A negative voltage on these pins can cause the POR or BOR blocks to unexpectedly assert XRSn or disable the internal VREG (see the *PMM Block Diagram*). Pins near the PMM on this device are shown in the *Pins Near PMM* table below.

Table 6-3. Pins Near PMM

PIN NAME	PIN NUMBER				
	64V PM	64 PM	48 PT	48 RGZ	32 RHB
GPIO39	–	46	–	–	–
GPIO8	47	47	–	36	–
GPIO4	48	48	38	37	25
GPIO3	49	49	39	38	26

Methods to avoid negative noise on pins include (in order of importance):

1. Reduce or eliminate noise at the source.
2. Avoid coupling between noise sources on these pins.
3. Filters near the device pin to isolate any noise.

6.11.1.6 Power Management Module Electrical Data and Timing

6.11.1.6.1 Power Management Module Operating Conditions

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
C_{VDDIO} (1) (2)	VDDIO Capacitance Per Pin(7)		0.1			uF
C_{VDDA} (1) (2)	VDDA Capacitance Per Pin(7)		2.2			uF
SR_{VDD33} (3)	Supply Ramp Rate of 3.3V Rails (VDDIO, VDDA)		20		100	mV/us
$V_{BOR-VDDIO-GB}$ (5)	VDDIO Brown Out Reset Voltage Guardband			0.1		V
External VREG						
$C_{VDD\ TOTAL}$ (1) (4)	Total VDD Capacitance(7)			10		uF
SR_{VDD12} (3)	Supply Ramp Rate of 1.2V Rail (VDD)		10		100	mV/us
V_{DDIO} - V_{DD} Delay(6)	Ramp Delay Between VDDIO and VDD		0			us
Internal VREG						
$C_{VDD\ TOTAL}$ (1) (4)	Total VDD Capacitance(7)			10		uF

(1) A bulk capacitor should also be used. The exact value of the decoupling capacitance depends on the system voltage regulation solution that is supplying these pins.
(2) It is recommended to tie the 3.3V rails (VDDIO, VDDA) together and supply them from a single source.
(3) See the *Supply Slew Rate* section. Supply ramp rate faster than the maximum can trigger the on-chip ESD protection.
(4) See the *Power Management Module (PMM)* section on possible configurations for the total decoupling capacitance.
(5) TI recommends $V_{BOR-VDDIO-GB}$ to avoid BOR-VDDIO resets due to normal supply noise or load-transient events on the 3.3-V VDDIO system regulator. Good system regulator design and decoupling capacitance (following the system regulator specifications) are important to prevent activation of the BOR-VDDIO during normal device operation. The value of $V_{BOR-VDDIO-GB}$ is a system-level design consideration; the voltage listed here is typical for many applications.
(6) Delay between when the 3.3-V rail ramps up and when the 1.2-V rail ramps up. See the *VREG Sequence Summary* table for the allowable supply ramp sequences.
(7) Max capacitor tolerance should be 20%.

6.11.1.6.2 Power Management Module Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VREG}	Internal Voltage Regulator Output		1.152	1.2	1.248	V
$V_{VREG-PU}$	Internal Voltage Regulator Power Up Time				350	us
$V_{VREG-INRUSH}$ (5)	Internal Voltage Regulator Inrush Current			650		mA
$V_{POR-VDDIO}$	VDDIO Power on Reset Voltage	Before and After XRSn Release		2.3		V
$V_{BOR-VDDIO-UP}$ (1)	VDDIO Brown Out Reset Voltage on Ramp Up	Before XRSn Release		2.7		V
$V_{BOR-VDDIO-DOWN}$ (1)	VDDIO Brown Out Reset Voltage on Ramp Down	After XRSn Release	2.81		3.0	V
$V_{POR-VDD-UP}$ (2)	VDD Power on Reset Voltage on Ramp-Up	Before XRSn Release		1		V
$V_{POR-VDD-DOWN}$ (2)	VDD Power on Reset Voltage on Ramp-Down	After XRSn Release		1		V

6.11.1.6.2 Power Management Module Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{XRSn-PU-DELAY}$ (3)	XRSn Release Delay after Supplies are Ramped Up During Power-Up			40		us
$V_{XRSn-PD-DELAY}$ (4)	XRSn Trip Delay after Supplies are Ramped Down During Power-Down			2		us
$V_{DDIO-MON-TOT-DELAY}$	Total Delays in Path of VDDIO Monitors (POR, BOR)			80		us
$V_{XRSn-MON-RELEASE-DELAY}$	XRSn Release Delay after a VDD POR Event	Supplies Within Operating Range		40		us
	XRSn Release Delay after a VDDIO BOR Event			40		us
	XRSn Release Delay after a VDDIO POR Event			120		us

(1) See the *Supply Voltages* figure.
(2) $V_{POR-VDD}$ is significantly below the recommended operating conditions. If monitoring of VDD is needed, an external supervisor is required.
(3) Supplies are considered fully ramped up after they cross the minimum recommended operating conditions for the respective rail. All POR and BOR monitors need to be released before this delay takes effect. RC network delay will add to this.
(4) On power down, any of the POR or BOR monitors that trips will immediately trip XRSn. This delay is the time between any of the POR, BOR monitors tripping and XRSn going low. It is variable and depends on the ramp down rate of the supply. RC network delay will add to this.
(5) This is the transient current drawn on the VDDIO rail when the internal VREG turns on. Due to this, there might be some voltage drops on the VDDIO rail when the VREG turns on which could cause the VREG to ramp up in steps. There is no detriment to the device from this but the effect can be reduced if desired by using sufficient decoupling capacitors on VDDIO or picking an LDO/DC-DC that can supply this transient current.

Supply Voltages

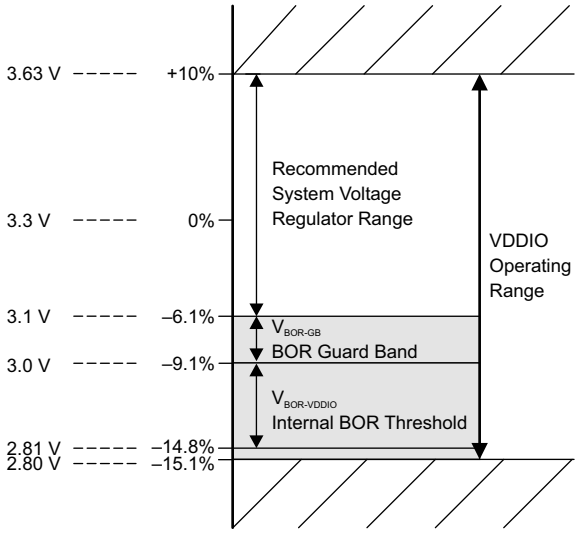


Figure 6-8. Supply Voltages

6.11.2 Reset Timing

XRSn is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR) and brown-out reset (BOR) monitors. During power up, the monitor circuits keep the XRSn pin low. For more details, see the *Power Management Module (PMM)* section. A watchdog or NMI watchdog reset will also drive the pin low. An external open-drain circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between XRSn and VDDIO. A capacitor should be placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Figure 6-9 shows the recommended reset circuit.

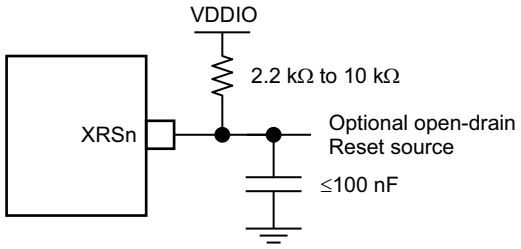


Figure 6-9. Reset Circuit

6.11.2.1 Reset Sources

The Reset Signals table summarizes the various reset signals and their effect on the device.

Table 6-4. Reset Signals

Reset Source	CPU Core Reset (C28x, FPU, TMU)	Peripherals Reset	JTAG / Debug Logic Reset	IOs	$\overline{\text{XRS}}$ Output
POR	Yes	Yes	Yes	Hi-Z	Yes
BOR	Yes	Yes	Yes	Hi-Z	Yes
$\overline{\text{XRS}}$ Pin	Yes	Yes	No	Hi-Z	-
$\overline{\text{WDRS}}$	Yes	Yes	No	Hi-Z	Yes
$\overline{\text{NMIWDRS}}$	Yes	Yes	No	Hi-Z	Yes
$\overline{\text{SYSRS}}$ (Debugger Reset)	Yes	Yes	No	Hi-Z	No
$\overline{\text{SCCRESET}}$	Yes	Yes	No	Hi-Z	No
SIMRESET. $\overline{\text{XRS}}$	Yes	Yes	No	Hi-Z	Yes
SIMRESET. $\overline{\text{CPU1RS}}$	Yes	Yes	No	Hi-Z	No

The parameter $t_{h(boot\text{-}mode)}$ must account for a reset initiated from any of these sources.

See the Resets section of the System Control chapter in the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*.

CAUTION

Some reset sources are internally driven by the device. Some of these sources will drive XRSn low, use this to disable any other devices driving the boot pins. The SCCRESET and debugger reset sources do not drive XRSn; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP.

6.11.2.2 Reset Electrical Data and Timing

6.11.2.2.1 Reset - XRSn - Timing Requirements

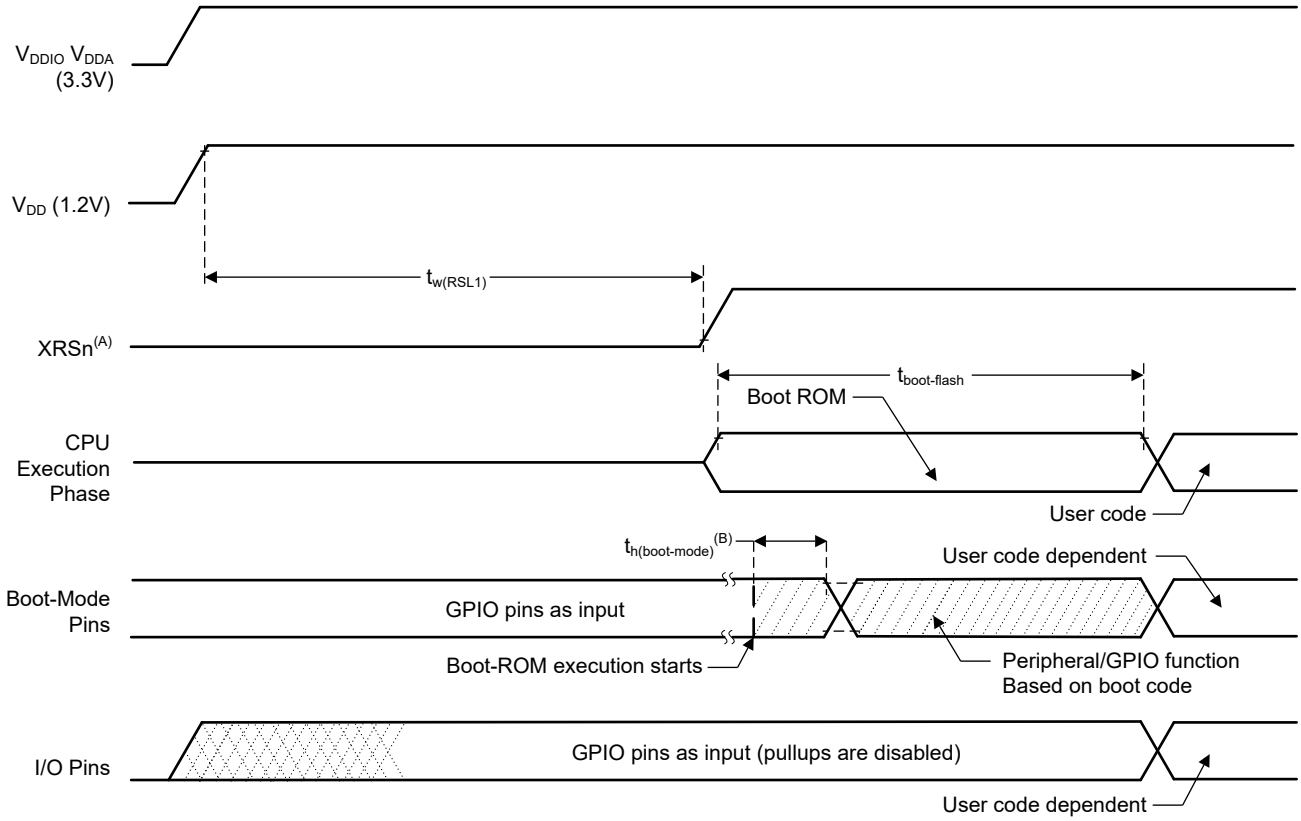
		MIN	MAX	UNIT
$t_{h(boot-mode)}$	Hold time for boot-mode pins	1.5		ms
$t_{w(RSL2)}$	Pulse duration, XRSn low on warm reset	3.2		µs

6.11.2.2.2 Reset - XRSn - Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, XRSn driven low by device after supplies are stable		100		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog		$512t_{c(OSCCLK)}$		cycles
$t_{boot-flash}$	Boot-ROM execution time to first instruction fetch in flash			1.2	ms

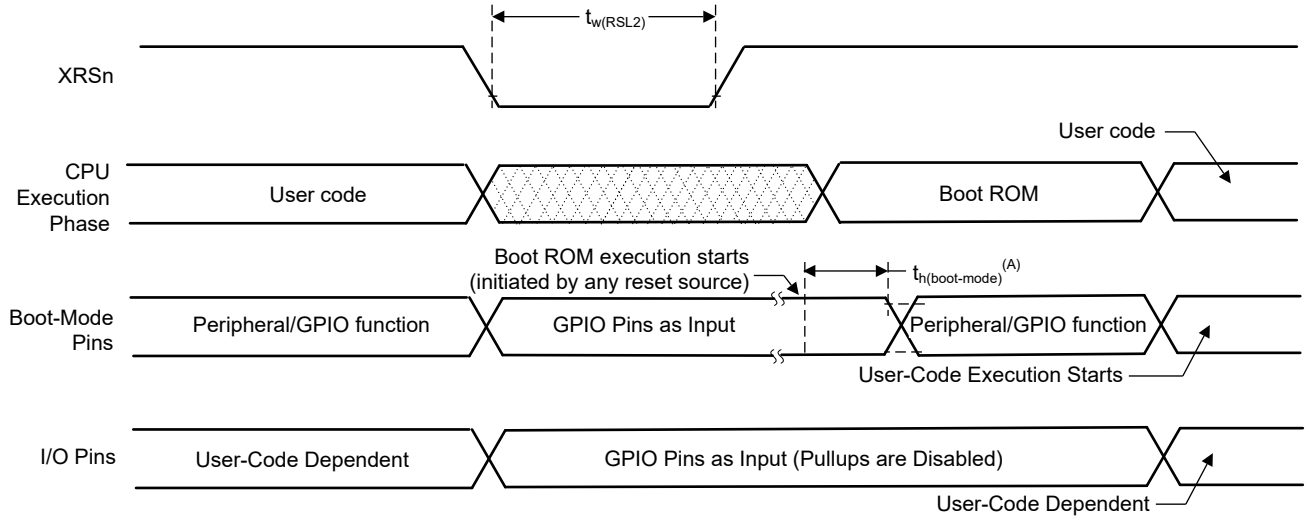
6.11.2.2.3 Reset Timing Diagrams



A. The XRSn pin can be driven externally by a supervisor or an external pullup resistor, see the Pin Attributes table. On-chip monitors will hold this pin low until the supplies are in a valid range.

B. After reset from any source (see the Reset Sources section), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-10. Power-on Reset



A. After reset from any source (see the Reset Sources section), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-11. Warm Reset

6.11.3 Clock Specifications

6.11.3.1 Clock Sources

Table 6-5. Possible Reference Clock Sources

CLOCK SOURCE	DESCRIPTION
INTOSC1	Internal oscillator 1. 10-MHz internal oscillator.
INTOSC2(1)	Internal oscillator 2. 10-MHz internal oscillator.
X1 (XTAL)	External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin.

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for the PLL (OSCCLK).

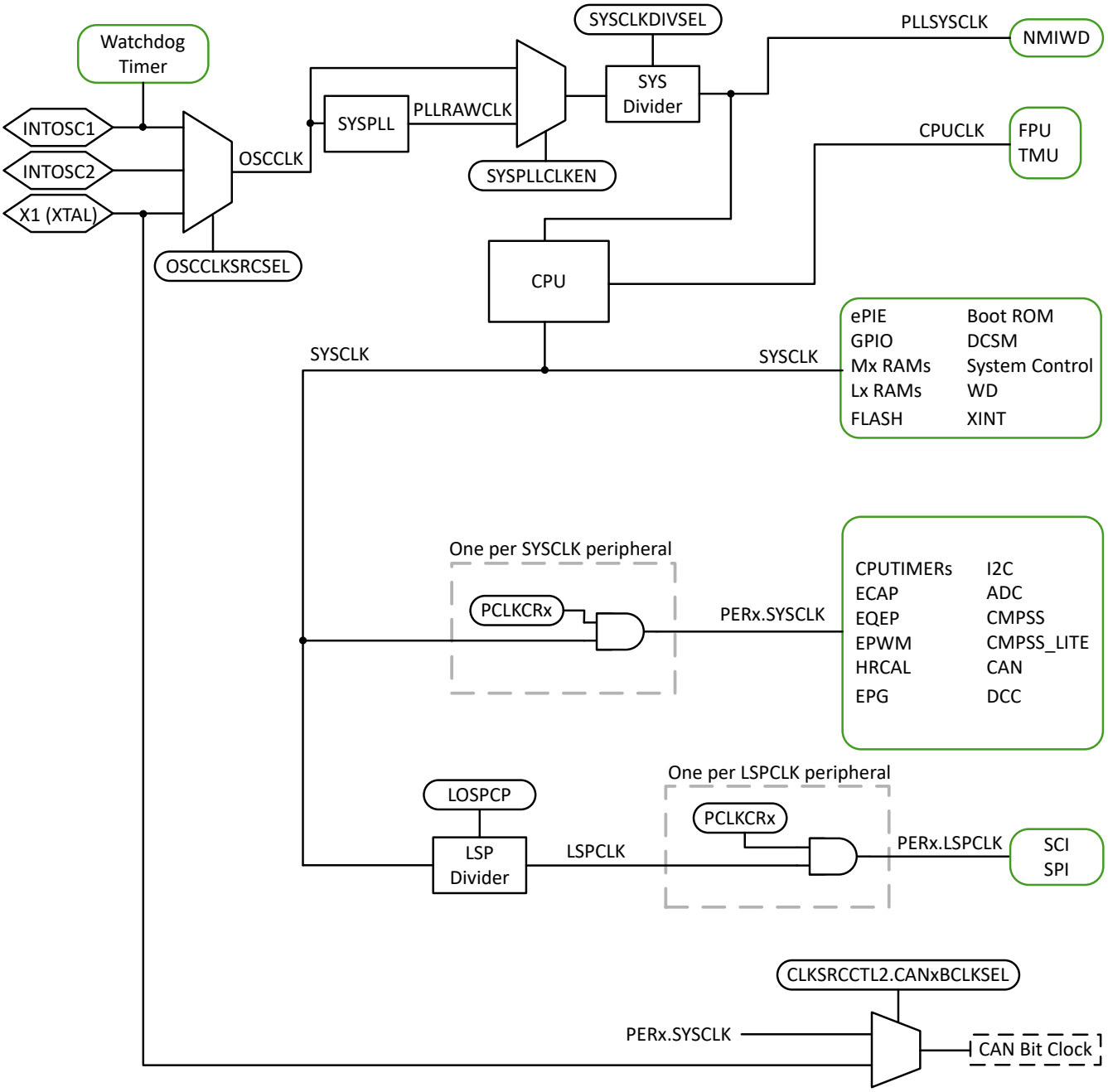


Figure 6-12. Clocking System

SYSPLL

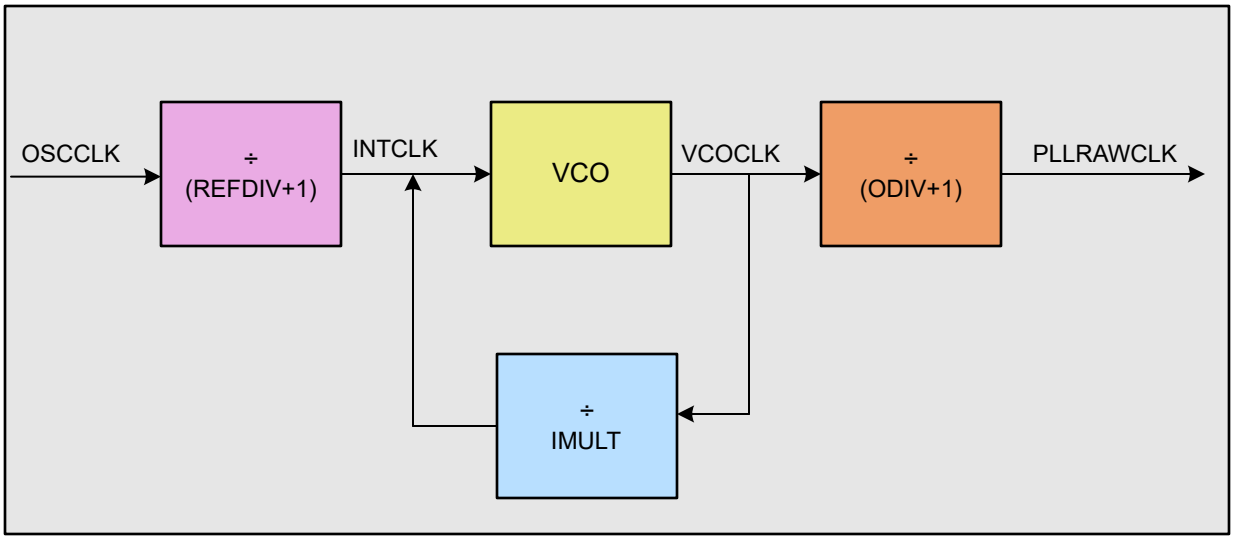


Figure 6-13. System PLL

In the *System PLL* figure,

$$f_{PLLRAWCLK} = \frac{f_{OSCCLK}}{(REFDIV + 1)} \times \frac{IMULT}{(ODIV + 1)} \quad (1)$$

6.11.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

6.11.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

6.11.3.2.1.1 Input Clock Frequency

		MIN	MAX	UNIT
$f_{(XTAL)}$	Frequency, X1/X2, from external crystal or resonator	10	20	MHz
$f_{(X1)}$	Frequency, X1, from external oscillator	10	25	MHz

6.11.3.2.1.2 XTAL Oscillator Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage	–0.3		0.3 * VDDIO	V
X1 V_{IH}	Valid high-level input voltage	0.7 * VDDIO		VDDIO + 0.3	V

6.11.3.2.1.3 X1 Input Level Characteristics When Using an External Clock Source - Not a Crystal

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage (Buffer)	–0.3	0.3 * VDDIO	V
X1 V_{IH}	Valid high-level input voltage (Buffer)	0.7 * VDDIO	VDDIO + 0.3	V

6.11.3.2.1.4 X1 Timing Requirements

		MIN	MAX	UNIT
$t_{f(X1)}$	Fall time, X1		6	ns
$t_{r(X1)}$	Rise time, X1		6	ns
$t_{w(X1L)}$	Pulse duration, X1 low as a percentage of $t_{c(X1)}$	45%	55%	
$t_{w(X1H)}$	Pulse duration, X1 high as a percentage of $t_{c(X1)}$	45%	55%	

6.11.3.2.1.5 AUXCLKIN Timing Requirements

		MIN	MAX	UNIT
$t_{f(AUXI)}$	Fall time, AUXCLKIN		6	ns
$t_{r(AUXI)}$	Rise time, AUXCLKIN		6	ns
$t_{w(AUXL)}$	Pulse duration, AUXCLKIN low as a percentage of $t_{c(XCI)}$	45%	55%	
$t_{w(AUXH)}$	Pulse duration, AUXCLKIN high as a percentage of $t_{c(XCI)}$	45%	55%	

6.11.3.2.1.6 APLL Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
PLL Lock time				
SYS PLL Lock Time(1)			5µs + (1024 * (REFDIV + 1) * $t_{c(OSCCLK)}$)	us

(1) The PLL lock time here defines the typical time that takes for the PLL to lock once PLL is enabled (SYSPLLCTL1[PLLENA]=1). Additional time to verify the PLL clock using Dual Clock Comparator (DCC) is not accounted here. TI recommends using the latest example software from C2000Ware for initializing the PLLs. For the system PLL, see InitSysPll() or SysCtl_setClock().

6.11.3.2.1.7 XCLKOUT Switching Characteristics - PLL Bypassed or Enabled

over recommended operating conditions (unless otherwise noted)

PARAMETER(1)		MIN	MAX	UNIT
$t_{f(XCO)}$	Fall time, XCLKOUT		6	ns
$t_{r(XCO)}$	Rise time, XCLKOUT		6	ns

6.11.3.2.1.7 XCLKOUT Switching Characteristics - PLL Bypassed or Enabled (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER[1]		MIN	MAX	UNIT
$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2[2]	H + 2[2]	ns
$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2[2]	H + 2[2]	ns
$f_{(XCO)}$	Frequency, XCLKOUT		50	MHz

(1) A load of 6 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$

6.11.3.2.1.8 Internal Clock Frequencies

		MIN	NOM	MAX	UNIT
$f_{(SYSCLK)}$	Frequency, device (system) clock	2		120	MHz
$t_{c(SYSCLK)}$	Period, device (system) clock	8.33		500	ns
$f_{(INTCLK)}$	Frequency, system PLL going into VCO (after REFDIV)	2		20	MHz
$f_{(VCOCLK)}$	Frequency, system PLL VCO (before ODIV)	220		600	MHz
$f_{(PLLRAWCLK)}$	Frequency, system PLL output (before SYSCLK divider)	6		240	MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		120	MHz
$f_{(PLL\_LIMP)}$	Frequency, PLL Limp Frequency [1]		45/(ODIV+1)		MHz
$f_{(LSP)}$	Frequency, LSPCLK	2		120	MHz
$t_{c(LSPCLK)}$	Period, LSPCLK	8.33		500	ns
$f_{(OSCCLK)}$	Frequency, OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1)		See respective clock		MHz
$f_{(EPWM)}$	Frequency, EPWMCLK			120	MHz
$f_{(HRPWM)}$	Frequency, HRPWMCLK	60		120	MHz

(1) PLL output frequency when OSCCLK is dead (Loss of OSCCLK causes PLL to Limp).

6.11.3.3 Input Clocks and PLLs

In addition to the internal 0-pin oscillators, three types of external clock sources are supported:

- A single-ended 3.3-V external clock. The clock signal should be connected to X1, as shown in Figure 6-14, with the XTALCR.SE bit set to 1.
- An external crystal. The crystal should be connected across X1 and X2 with its load capacitors connected to VSS as shown in Figure 6-15.
- An external resonator. The resonator should be connected across X1 and X2 with its ground connected to VSS as shown in Figure 6-16.

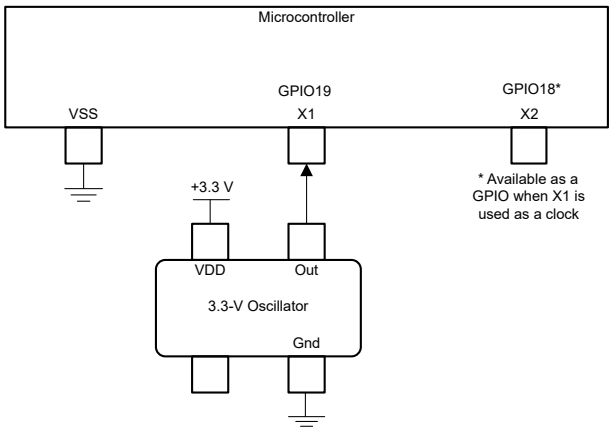


Figure 6-14. Single-ended 3.3-V External Clock

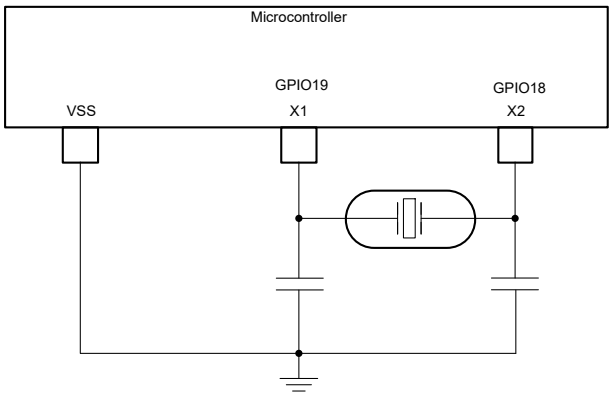


Figure 6-15. External Crystal

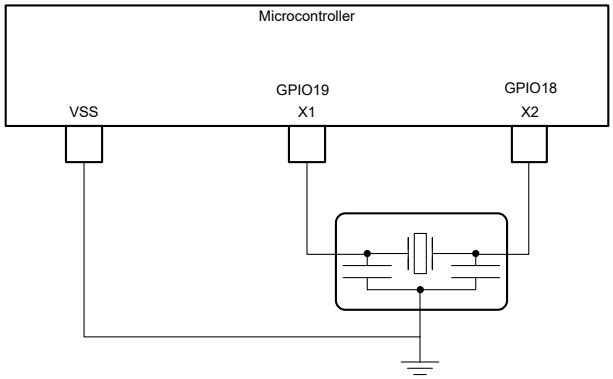


Figure 6-16. External Resonator

6.11.3.4 XTAL Oscillator

6.11.3.4.1 Introduction

The crystal oscillator in this device is an embedded electrical oscillator that, when paired with a compatible quartz crystal (or a ceramic resonator), can generate the system clock required by the device.

6.11.3.4.2 Overview

The following sections describe the components of the electrical oscillator and crystal.

6.11.3.4.2.1 Electrical Oscillator

The electrical oscillator in this device is a Pierce oscillator. It is a positive feedback inverter circuit that requires a tuning circuit in order to oscillate. When this oscillator is paired with a compatible crystal, a tank circuit is formed. This tank circuit oscillates at the fundamental frequency of the crystal. On this device, the oscillator is designed to operate in parallel resonance mode due to the shunt capacitor (C0) and required load capacitors (CL). Figure 6-17 illustrates the components of the electrical oscillator and the tank circuit.

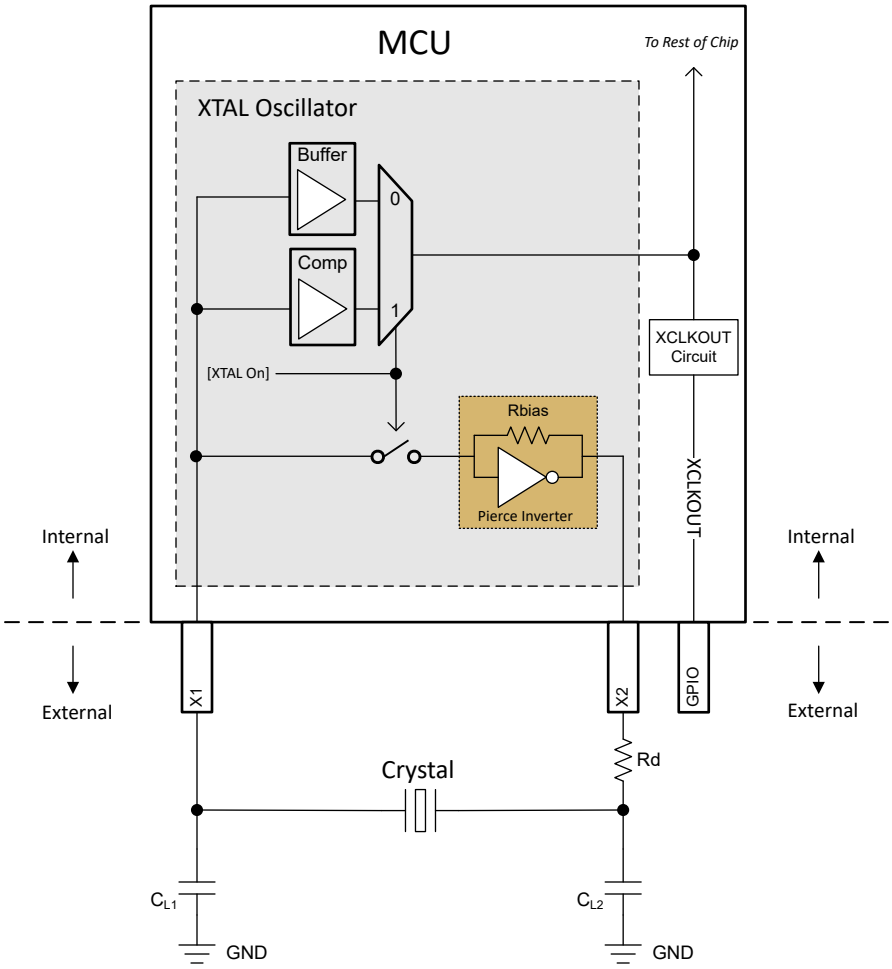


Figure 6-17. Electrical Oscillator Block Diagram

6.11.3.4.2.1.1 Modes of Operation

The electrical oscillator in this device has two modes of operation: crystal mode and single-ended mode.

6.11.3.4.2.1.1.1 Crystal Mode of Operation

In the crystal mode of operation, a quartz crystal with load capacitors has to be connected to X1 and X2.

This mode of operation is engaged when [XTAL On] = 1, which is achieved by setting XTALCR.OSCOFF = 0 and XTALCR.SE = 0. There is an internal bias resistor for the feedback loop so an external one should not be used. Adding an external bias resistor will create a parallel resistance with the internal Rbias, moving the bias point of operation and possibly leading to clipped waveforms, out-of-specification duty cycle, and reduction in the effective negative resistance.

In this mode of operation, the resultant clock on X1 is passed through a comparator (Comp) to the rest of the chip. The clock on X1 needs to meet the VIH and VIL of the comparator. See the *XTAL Oscillator Characteristics* table for the VIH and VIL requirements of the comparator.

6.11.3.4.2.1.1.2 Single-Ended Mode of Operation

In the single-ended mode of operation, a clock signal is connected to X1 with X2 left unconnected. A quartz crystal should not be used in this mode.

This mode is enabled when [XTAL On] = 0, which can be achieved by setting XTALCR.OSCOFF = 1 and XTALCR.SE = 1.

In this mode of operation, the clock on X1 is passed through a buffer (Buffer) to the rest of the chip. See the *X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)* table for the input requirements of the buffer.

6.11.3.4.2.1.2 XTAL Output on XCLKOUT

The output of the electrical oscillator that is fed to the rest of the chip can be brought out on XCLKOUT for observation by configuring the CLKSRCCTL3.XCLKOUTSEL and XCLKOUTDIVSEL.XCLKOUTDIV registers. See the GPIO Muxed Pins table for a list of GPIOs that XCLKOUT comes out on.

6.11.3.4.2.2 Quartz Crystal

Electrically, a quartz crystal can be represented by an LCR (Inductor-Capacitor-Resistor) circuit. However, unlike an LCR circuit, crystals have very high Q due to the low motional resistance and are also very underdamped. Components of the crystal are shown in Figure 6-18 and explained below.

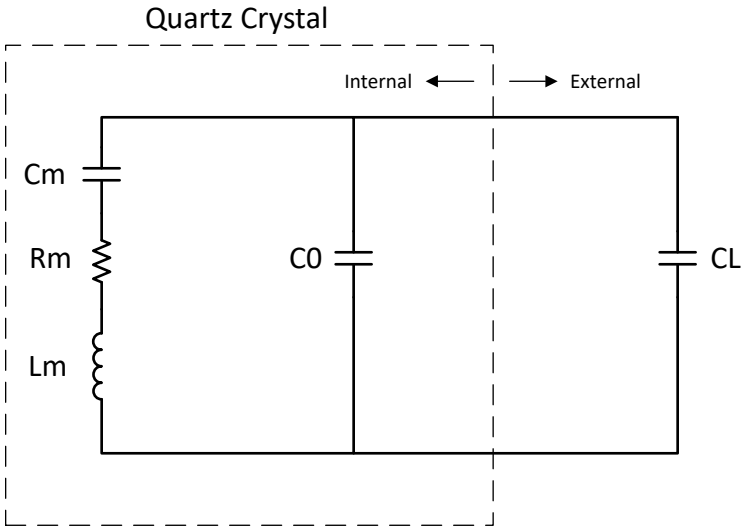


Figure 6-18. Crystal Electrical Representation

Cm (Motional capacitance): Denotes the elasticity of the crystal.

Rm (Motional resistance): Denotes the resistive losses within the crystal. This is not the ESR of the crystal but can be approximated as such depending on the values of the other crystal components.

Lm (Motional inductance): Denotes the vibrating mass of the crystal.

C0 (Shunt capacitance): The capacitance formed from the two crystal electrodes and stray package capacitance.

CL (Load capacitance): This is the effective capacitance seen by the crystal at its electrodes. It is external to the crystal. The frequency ppm specified in the crystal data sheet is usually tied to the CL parameter.

Note that most crystal manufacturers specify CL as the effective capacitance seen at the crystal pins, while some crystal manufacturers specify CL as the capacitance on just one of the crystal pins. Check with the crystal manufacturer for how the CL is specified in order to use the correct values in calculations.

From Figure 6-17, CL1 and CL2 are in series; so, to find the equivalent total capacitance seen by the crystal, the capacitance series formula has to be applied which simply evaluates to [CL1]/2 if CL1 = CL2.

It is recommended that a stray PCB capacitance be added to this value. 3 pF to 5 pF are reasonable estimates, but the actual value will depend on the PCB in question.

Note that the load capacitance is a requirement of both the electrical oscillator and crystal. The value chosen has to satisfy both the electrical oscillator and the crystal.

The effect of CL on the crystal is frequency-pulling. If the effective load capacitance is lower than the target, the crystal frequency will increase and vice versa. However, the effect of frequency-pulling is usually very minimal and typically results in less than 10-ppm variation from the nominal frequency.

6.11.3.4.2.3 GPIO Modes of Operation

On this device, X1 and X2 can be used as GPIO19 and GPIO18, respectively, depending on the operating mode of the XTAL. Refer to the External Oscillator (XTAL) section of the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual* .

6.11.3.4.3 Functional Operation

6.11.3.4.3.1 ESR – Effective Series Resistance

Effective Series Resistance is the resistive load the crystal presents to the electrical oscillator at resonance. The higher the ESR, the lower the Q, and less likely the crystal will start up or maintain oscillation. The relationship between ESR and the crystal components is indicated below.

$$ESR = Rm * \left(1 + \frac{C0}{CL}\right)^2 \quad (2)$$

Note that ESR is not the same as motional resistance of the crystal, but can be approximated as such if the effective load capacitance is much greater than the shunt capacitance.

6.11.3.4.3.2 Rneg – Negative Resistance

Negative resistance is the impedance presented by the electrical oscillator to the crystal. It is the amount of energy the electrical oscillator must supply to the crystal to overcome the losses incurred during oscillation. Rneg depicts a circuit that provides rather than consume energy and can also be viewed as the overall gain of the circuit.

The generally accepted practice is to have Rneg > 3x ESR to 5x ESR to ensure the crystal starts up under all conditions. Note that it takes slightly more energy to start up the crystal than it does to sustain oscillation; therefore, if it can be ensured that the negative resistance requirement is met at start-up, then oscillation sustenance will not be an issue.

Figure 6-19 and Figure 6-20 show the variation between negative resistance and the crystal components for this device. As can be seen from the graphs, the crystal shunt capacitance (C0) and effective load capacitance (CL) greatly influence the negative resistance of the electrical oscillator. Note that these are typical graphs; so, refer to Table 6-6 for minimum and maximum values for design considerations.

6.11.3.4.3.3 Start-up Time

Start-up time is an important consideration when selecting the components of the crystal circuit. As mentioned in the Rneg – Negative Resistance section, for reliable start-up across all conditions, it is recommended that the Rneg > 3x ESR to 5x ESR of the crystal.

Crystal ESR and the dampening resistor (Rd) greatly affect the start-up time. The higher the two values, the longer the crystal takes to start up. Longer start-up times are usually a sign that the crystal and components are not a correct match.

Refer to Crystal Oscillator Specifications for the typical start-up times. Note that the numbers specified here are typical numbers provided for guidance only. Actual start-up time depends heavily on the crystal in question and the external components.

6.11.3.4.3.3.1 X1/X2 Precondition

On this device, the GPIO19/18 alternate functionality on X1/X2 can be used to speed up the start-up time of the crystal if needed. This functionality is achieved by preconditioning the load capacitors CL1 and CL2 to a known state before the XTAL is turned on. See the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual* for details.

6.11.3.4.3.4 DL – Drive Level

Drive level refers to how much power is provided by the electrical oscillator and dissipated by the crystal. The maximum drive level specified in the crystal manufacturer's data sheet is usually the maximum the crystal can dissipate without damage or significant reduction in operating life. On the other hand, the drive level specified by the electrical oscillator is the maximum power it can provide. The actual power provided by the electrical oscillator is not necessarily the maximum power and depends on the crystal and board components.

For cases where the actual drive level from the electrical oscillator exceeds the maximum drive level specification of the crystal, a dampening resistor (Rd) should be installed to limit the current and reduce the power dissipated by the crystal. Note that Rd reduces the circuit gain; and therefore, the actual value to use should be evaluated to make sure all other conditions for start-up and sustained oscillation are met.

6.11.3.4.4 How to Choose a Crystal

Using Crystal Oscillator Specifications as a reference:

1. Pick a crystal frequency (for example, 20 MHz).
2. Check that the ESR of the crystal <=50 Ω per specifications for 20 MHz.
3. Check that the load capacitance requirement of the crystal manufacturer is within 6 pF and 12 pF per specifications for 20 MHz.
   - As mentioned, CL1 and CL2 are in series; so, provided CL1 = CL2, effective load capacitance CL = [CL1]/2.
   - Adding board parasitics to this results in CL = [CL1]/2 + Cstray
4. Check that the maximum drive level of the crystal >= 1 mW. If this requirement is not met, a dampening resistor Rd can be used. Refer to DL – Drive Level on other points to consider when using Rd.

6.11.3.4.5 Testing

It is recommended that the user have the crystal manufacturer completely characterize the crystal with their board to ensure the crystal always starts up and maintains oscillation.

Below is a brief overview of some measurements that can be performed:

Due to how sensitive the crystal circuit is to capacitance, it is recommended that scope probes not be connected to X1 and X2. If scope probes must be used to monitor X1/X2, an active probe with less than 1pF input capacitance should be used.

Frequency

1. Bring out the XTAL on XCLKOUT.
2. Measure this frequency as the crystal frequency.

Negative Resistance

1. Bring out the XTAL on XCLKOUT.
2. Place a potentiometer in series with the crystal between the load capacitors.
3. Increase the resistance of the potentiometer until the clock on XCLKOUT stops.
4. This resistance plus the crystal's actual ESR is the negative resistance of the electrical oscillator.

Start-Up Time

1. Turn off the XTAL.
2. Bring out the XTAL on XCLKOUT.
3. Turn on the XTAL and measure how long it takes the clock on XCLKOUT to stay within 45% and 55% duty cycle.

6.11.3.4.6 Common Problems and Debug Tips

Crystal Fails to Start Up

- Go through the How to Choose a Crystal section and make sure there are no violations.

Crystal Takes a Long Time to Start Up

- If a dampening resistor Rd is installed, it is too high.
- If no dampening resistor is installed, either the crystal ESR is too high or the overall circuit gain is too low due to high load capacitance.

6.11.3.4.7 Crystal Oscillator Specifications

6.11.3.4.7.1 Crystal Oscillator Parameters

		MIN	MAX	UNIT
CL1, CL2	Load capacitance	12	24	pF
C0	Crystal shunt capacitance		7	pF

6.11.3.4.7.2 Crystal Equivalent Series Resistance (ESR) Requirements

For the Crystal Equivalent Series Resistance (ESR) Requirements table:

1. Crystal shunt capacitance (C0) should be less than or equal to 7 pF.
2. ESR = Negative Resistance/3

Table 6-6. Crystal Equivalent Series Resistance (ESR) Requirements

CRYSTAL FREQUENCY (MHz)	MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF)	MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF)
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

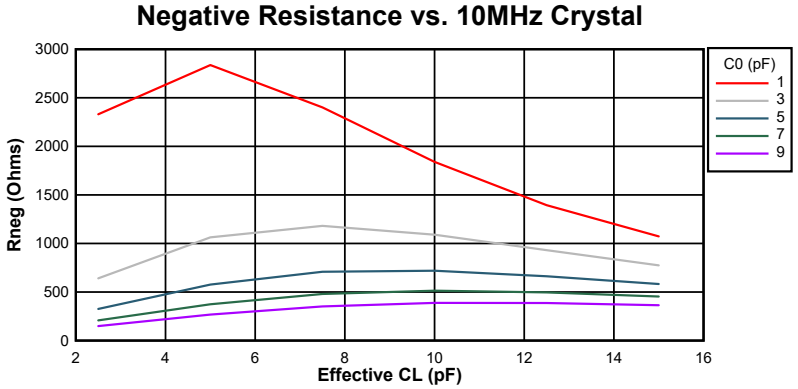


Figure 6-19. Negative Resistance Variation at 10 MHz

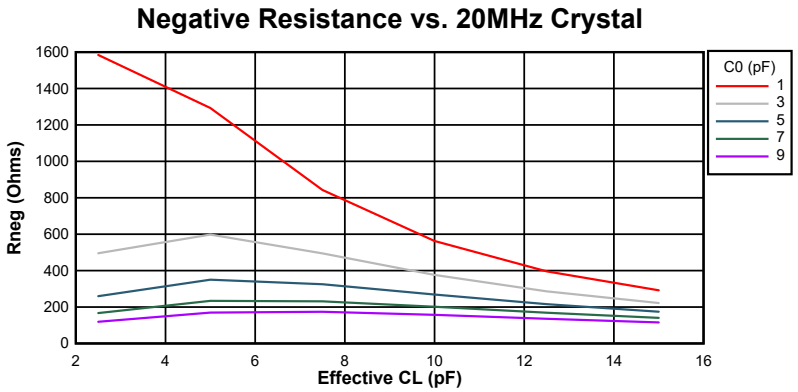


Figure 6-20. Negative Resistance Variation at 20 MHz

6.11.3.4.7.3 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time[1]	f = 10 MHz	ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF		4		ms
	f = 20 MHz	ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF		2		ms
Crystal drive level (DL)					1	mW

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

6.11.3.5 Internal Oscillators

To reduce production board costs and application development time, all F280013x devices contain two independent internal oscillators, referred to as INTOSC1 and INTOSC2. By default, INTOSC2 is set as the source for the system reference clock (OSCCLK) and INTOSC1 is set as the backup clock source.

Applications requiring tighter **SCI baud rate matching** can use the SCI baud tuning example (baud_tune_via_uart) available in C2000Ware.

6.11.3.5.1 INTOSC Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		PART	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{INTOSC}	Frequency, INTOSC1 and INTOSC2(1)	F2800137, F2800135	-40°C to 125°C	9.82 (–1.8%)	10	10.1 (1.0%)	MHz
			-30°C to 90°C	9.86 (–1.4%)	10	10.1 (1.0%)	
			-10°C to 85°C	9.9 (–1.0%)	10	10.1 (1.0%)	
		F2800133, F2800132	-40°C to 125°C	9.7 (-3.0%)	10	10.3 (3.0%)	
$f_{INTOSC-STABILITY}$	Frequency stability at room temperature	All	30°C, Nominal VDD		±0.1		%
$t_{INTOSC-ST}$	Start-up and settling time	All				20	µs

(1) INTOSC frequency may shift due to the thermal and mechanical stress of solder reflow. A post-reflow bake can restore the unit to its original data sheet performance.

6.11.3.5.2 INTOSC2 with External Precision Resistor – ExtR

To achieve better accuracy, an external precision resistor can be used with INTOSC2.

The external components required are:

- 100-kΩ precision resistor between ExtR pin and VSS
- 10-nF capacitor for noise filtering
- 20-µF VDDIO capacitance minimum for low noise supply and load transients

Figure 6-21 shows an example illustration of these required external components.

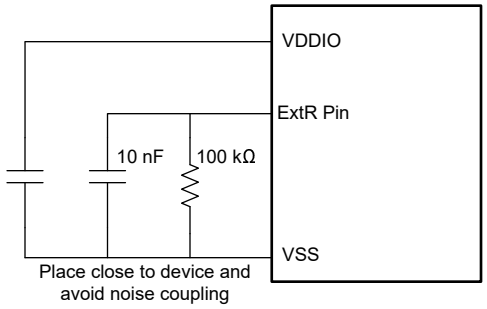


Figure 6-21. ExtR Example Schematic

In ExtR mode, the oscillator frequency error is directly proportional to the accuracy of the ExtR resistor.

The quality of the VDDIO supply directly affects the ExtR INTOSC performance. VDDIO capacitance values and circuit design must be decided with care to provide the cleanest supply possible to avoid jitter, noise, and other performance issues.

Placing a resistor on the ExtR pin prevents the pin from being used as a GPIO or X1.

Table 6-7 provides the ExtR specification values.

Table 6-7. ExtR Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{INTOSC2\text{-}ExtR\text{-}ERR\text{-}PERC}$	Ideal 0% error 100 kΩ ExtR resistor	-0.7	0	+0.7	%
$f_{INTOSC2\text{-}ExtR}$	Ideal 0% error 100 kΩ ExtR resistor	9.93	10	10.07	MHz
$f_{ExtR\text{-}SETTLING}$	Switch to ExtR Mode		1		ms
ExtR Resistance, R_{ExtR}			100		kΩ
ExtR Decoupling Capacitance, C_{ExtR}			10		nF
VDDIO Decoupling Capacitance, C_{VDDIO}		20			µF

Table 6-8 provides an example calculation for determining the total error of INTOSC2 given the parameters of a resistor.

Table 6-8. Sample Total Error Calculation

PARAMETER	VALUE	UNIT
INTOSC2 Ideal Frequency Variation	0.70	%
ExtR Resistor Tolerance	$R_{TOLERANCE}$	%
ExtR Resistor Temperature Coefficient	R_{TEMPCO}	ppm/°C
Operating Temperature	$T_{OPERATING\_POINT}$	°C
ExtR Data Sheet Ambient Temperature	$T_{AMBIENT}$	°C
Total Frequency Error	$[(0.70/100) + (R_{TOLERANCE}/100) + ((R_{TEMPCO}/1E6) * abs(T_{OPERATING\_POINT}-T_{AMBIENT}))]*100$	%

Table 6-9 provides example values using the above calculation.

Table 6-9. Total Error Example Values

PARAMETER	VALUE	UNIT
INTOSC2 Ideal Frequency Variation	0.70	%
ExtR Resistor Tolerance	0.10	%
ExtR Resistor Temperature Coefficient	25	ppm/°C
Operating Temperature	90	°C
ExtR Data Sheet Ambient Temperature	25	°C
Total Frequency Error Calculation	((0.70/100) + (0.10/100) + ((25/1E6) * abs(90-25)))*100	%
Total Frequency Error Calculation	0.96	%

For best performance, use the following board layout guidelines:

- Route ExtR trace as short as possible
- Route ExtR to the nearest VSS pin
- Place ExtR (R_{ExtR}) and C_{ExtR} on the same side as the C2000 device, with routing on the same layer only
- Any adjacent GPIO pin (GPIO18, X2 for example) can be routed using the opposite side and in a different layer so as to reduce adjacent GPIO coupling
- VSS connection must be tied both to VSS plane and directly to C2000 device VSS pin
- VSS guard trace is recommended around the ExtR trace as shown in Figure 6-22
- Fill VSS or VDDIO plane in layer below ExtR and C_{ExtR} to avoid routing signal traces in adjacent layer

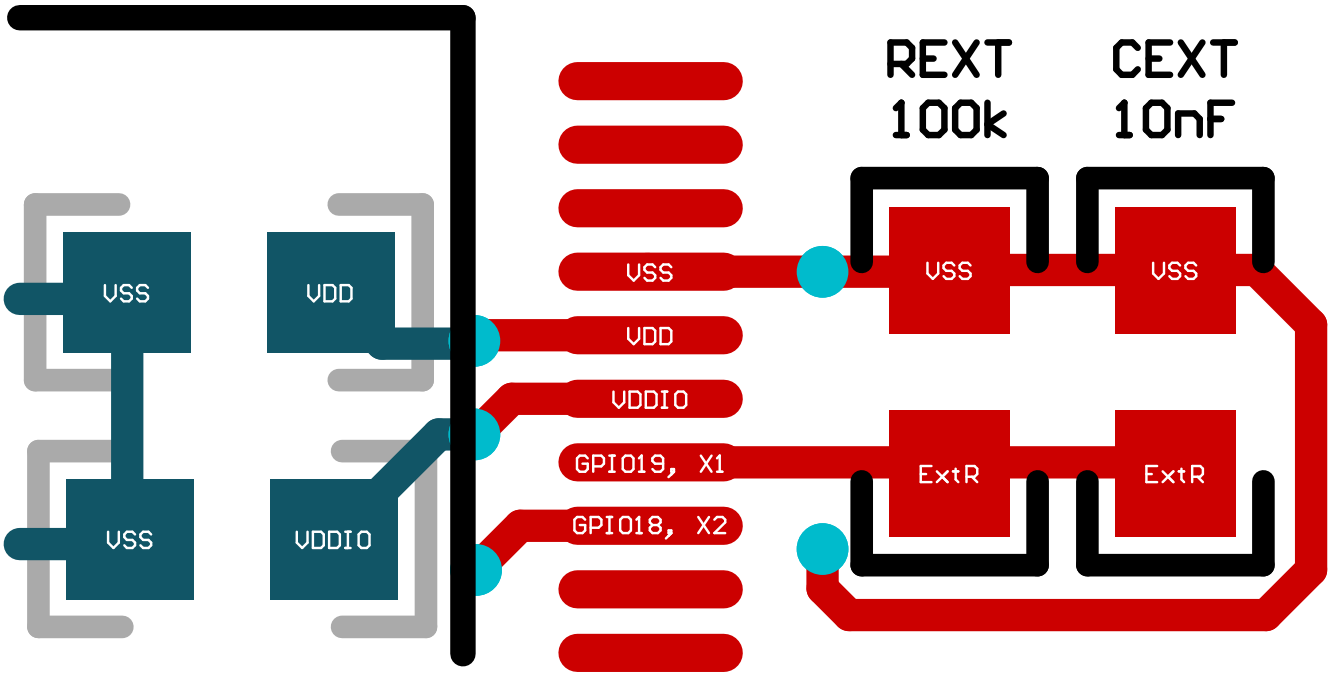


Figure 6-22. ExtR PCB Layout Example

6.11.4 Flash Parameters

Table 6-10 lists the minimum required Flash wait states with different clock sources and frequencies. Wait state is the value set in register FRDCNTL[RWAIT].

Table 6-10. Minimum Required Flash Wait States with Different Clock Sources and Frequencies

CPUCLK (MHz)	Wait States (FRDCNTL[RWAIT](1))
80 < CPUCLK ≤ 120	2
0 < CPUCLK ≤ 80	1

(1) Minimum required FRDCNTL[RWAIT] is 1, RWAIT=0 is not supported.

The F280013x devices have an improved 128-bit prefetch buffer that provides high flash code execution efficiency across wait states. Figure 6-23 and Figure 6-24 illustrate typical efficiency across wait-state settings compared to previous-generation devices with a 64-bit prefetch buffer. Wait-state execution efficiency with a prefetch buffer will depend on how many branches are present in application software. Two examples of linear code and if-then-else code are provided.

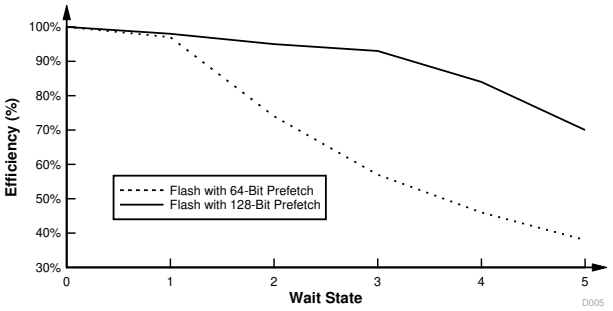


Figure 6-23. Application Code With Heavy 32-Bit Floating-Point Math Instructions

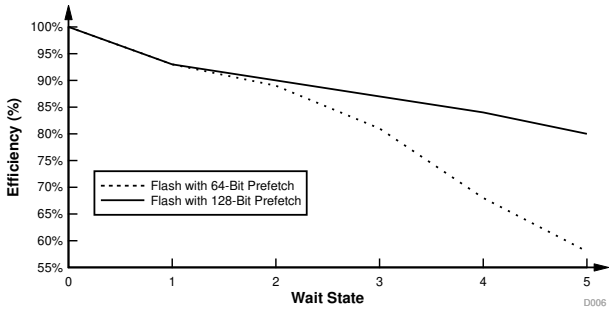


Figure 6-24. Application Code With 16-Bit If-Else Instructions

Note

The Main Array flash programming must be aligned to 64-bit address boundaries and each 64-bit word may only be programmed once per write/erase cycle.

6.11.4.1 Flash Parameters

PARAMETER		MIN	TYP	MAX	UNIT
Program Time(1)	128 data bits + 16 ECC bits		62.5	625	µs
	2KB (Sector)		8	80	ms
Erase Time(2) (3) at < 25 cycles	2KB (Sector)		15	55	ms
	64KB		17	61	ms
	128KB		18	66	ms
	256KB		21	78	ms
Erase Time(2) (3) at 1000 cycles	2KB (Sector)		25	130	ms
	64KB		28	143	ms
	128KB		30	157	ms
	256KB		35	183	ms
Erase Time(2) (3) at 2000 cycles	2KB (Sector)		30	221	ms
	64KB		33	243	ms
	128KB		36	265	ms
	256KB		42	310	ms
Erase Time(2) (3) at 20K cycles	2KB (Sector)		120	1003	ms
	64KB		132	1102	ms
	128KB		145	1205	ms
	256KB		169	1410	ms
N_{wec} Write/Erase Cycles per Bank(4)				100000	cycles
$t_{retention}$ Data retention duration at T_J = 85°C		20			years

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
- Code that uses flash API to program the flash
- Flash API itself
- Flash data to be programmed

In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the JTAG debug probe used.
Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.
Erase time includes Erase verify by the CPU and does not involve any data transfer.

(2) Erase time includes Erase verify by the CPU.

(3) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

(4) The combined total of bank and sector write/erase cycles is limited to this number.

6.11.5 RAM Specifications

Table 6-11. RAM Parameters

RAM TYPE	SIZE EACH	FETCH TIME (CYCLES)	READ TIME (CYCLES)	STORE TIME (CYCLES)	SUPPORTED BUS WIDTHS (BITS)	HOST ACCESS LIST	WAIT STATES	BURST ACCESS SUPPORT
LS RAM	32KB	2	2	1	16/32	C28x	0	No
M0	2KB							
M1								

6.11.6 ROM Specifications

Table 6-12. ROM Parameters

RAM TYPE	SIZE EACH	FETCH TIME (CYCLES)	READ TIME (CYCLES)	STORE TIME (CYCLES)	SUPPORTED BUS WIDTHS (BITS)	HOST ACCESS LIST	WAIT STATES	BURST ACCESS SUPPORT
Boot ROM + Secure ROM	64KB	2	2	1	16/32	C28x	0	No

6.11.7 Emulation/JTAG

The JTAG (IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture) port has four dedicated pins: TMS, TDI, TDO, and TCK. The cJTAG (IEEE Standard 1149.7-2009 for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture) port is a compact JTAG interface requiring only two pins (TMS and TCK), which allows other device functionality to be muxed to the traditional GPIO35 (TDI) and GPIO37 (TDO) pins.

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most JTAG debug probe operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22-Ω resistors should be placed in series on each JTAG signal.

The PD (Power Detect) pin of the JTAG debug probe header should be connected to the board's 3.3-V supply. Header GND pins should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output pin back to the RTCK input pin of the header (to sense clock continuity by the JTAG debug probe). This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 kΩ to 4.7 kΩ (depending on the drive strength of the debugger ports). Typically, a 2.2-kΩ value is used.

Header pin $\overline{\text{RESET}}$ is an open-drain output from the JTAG debug probe header that enables board components to be reset through JTAG debug probe commands (available only through the 20-pin header). Figure 6-25 shows how the 14-pin JTAG header connects to the MCU's JTAG port signals. Figure 6-26 shows how to connect to the 20-pin JTAG header. The 20-pin JTAG header pins EMU2, EMU3, and EMU4 are not used and should be grounded.

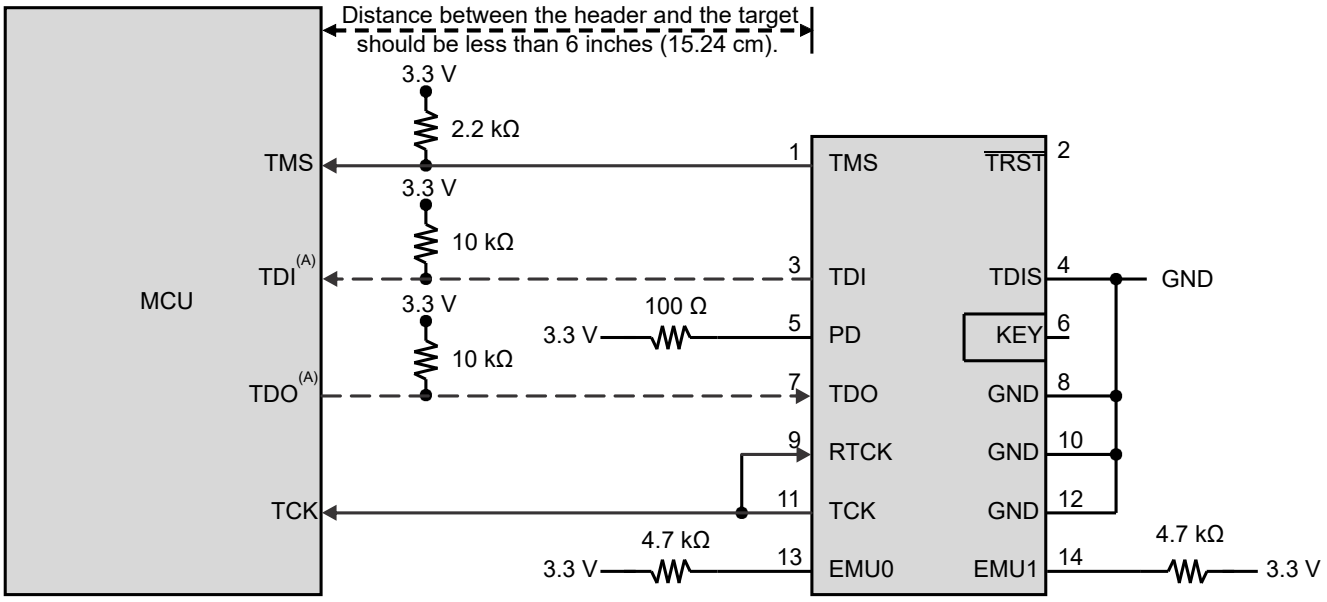
For more information about hardware breakpoints and watchpoints, see Hardware Breakpoints and Watchpoints in CCS for C2000 devices.

For more information about JTAG emulation, see the *XDS Target Connection Guide*.

Note

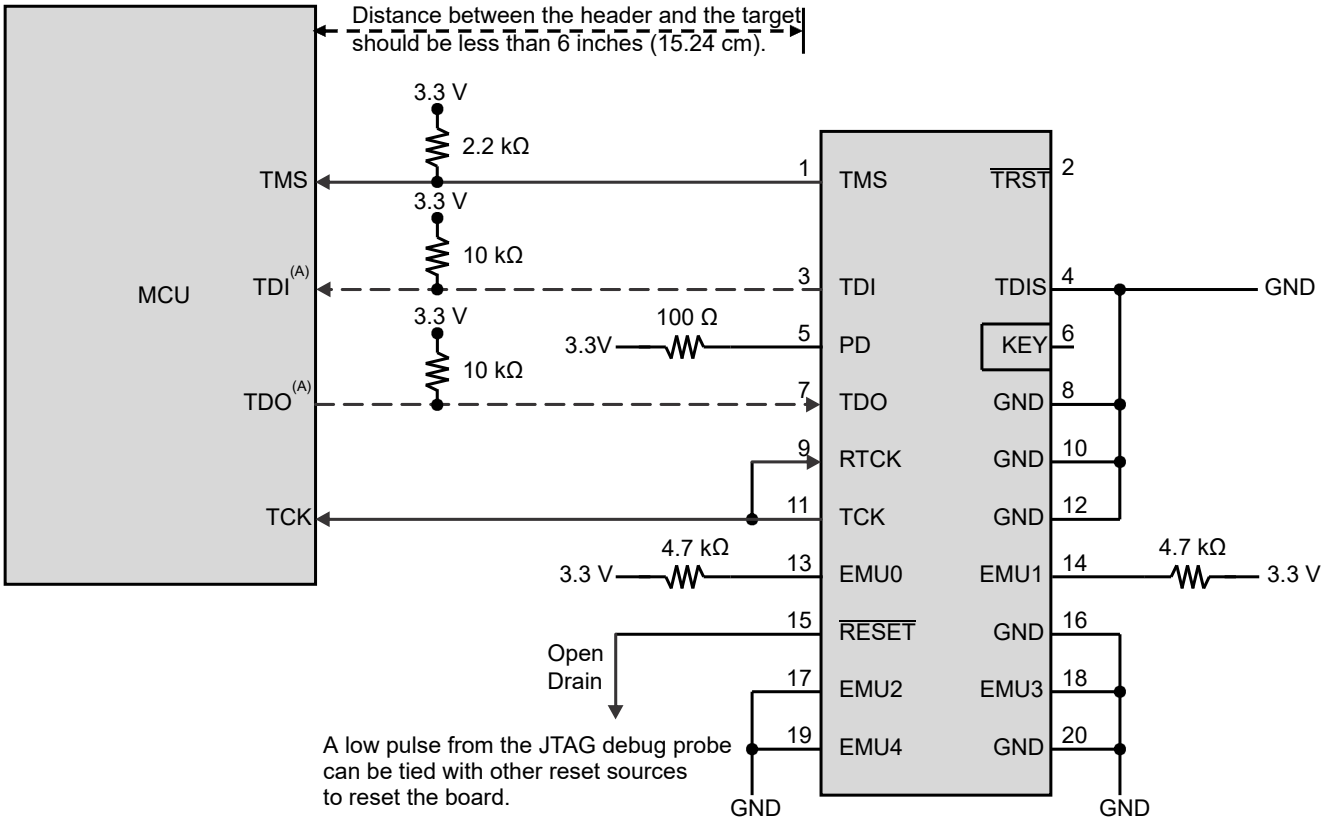
JTAG Test Data Input (TDI) is the default mux selection for the pin. The internal pullup is disabled by default. If this pin is used as JTAG TDI, the internal pullup should be enabled or an external pullup added on the board to avoid a floating input. In the cJTAG option, this pin can be used as GPIO.

JTAG Test Data Output (TDO) is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating. The internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. In the cJTAG option, this pin can be used as GPIO.



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-25. Connecting to the 14-Pin JTAG Header



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-26. Connecting to the 20-Pin JTAG Header

6.11.7.1 JTAG Electrical Data and Timing

6.11.7.1.1 JTAG Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	66.66		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	26.66		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	26.66		ns
3	$t_{su(TDI-TCKH)}$	Input setup time, TDI valid to TCK high	7		ns
	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	7		
4	$t_{h(TCKH-TDI)}$	Input hold time, TDI valid from TCK high	7		ns
	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	7		

6.11.7.1.2 JTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(TCKL-TDO)}$	Delay time, TCK low to TDO valid	6	20	ns

6.11.7.1.3 JTAG Timing Diagram

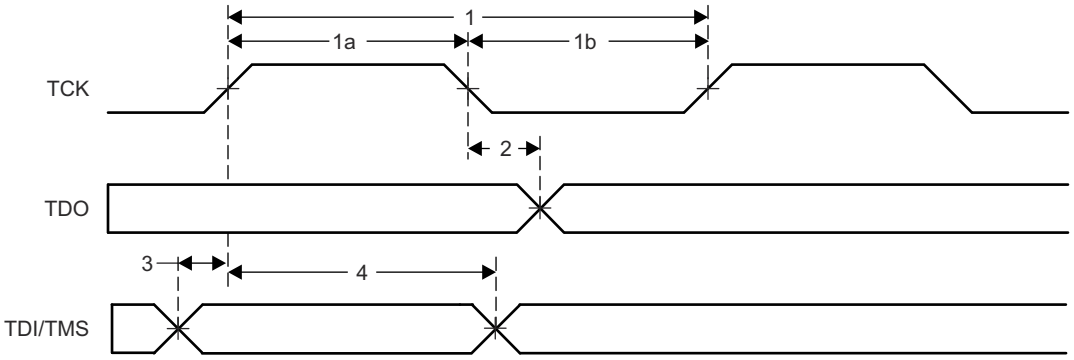


Figure 6-27. JTAG Timing

6.11.7.2 cJTAG Electrical Data and Timing

6.11.7.2.1 cJTAG Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	100		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	40		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	40		ns
3	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	7		ns
	$t_{su(TMS-TCKL)}$	Input setup time, TMS valid to TCK low	7		ns
4	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	2		ns
	$t_{h(TCKL-TMS)}$	Input hold time, TMS valid from TCK low	2		ns

6.11.7.2.2 cJTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(TCKL-TMS)}$	Delay time, TCK low to TMS valid	6	20	ns
5	$t_{dis(TCKH-TMS)}$	Delay time, TCK high to TMS disable		20	ns

6.11.7.2.3 cJTAG Timing Diagram

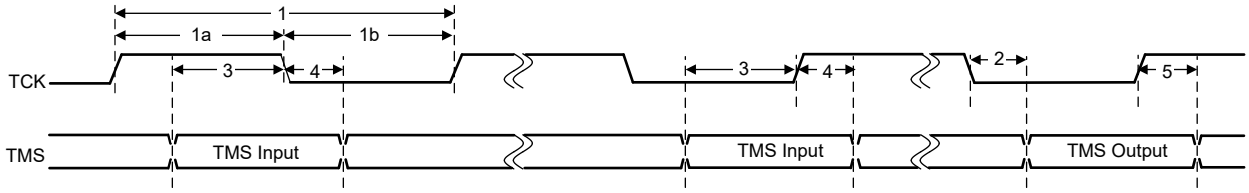


Figure 6-28. cJTAG Timing

6.11.8 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

The GPIO module contains an Output X-BAR which allows an assortment of internal signals to be routed to a GPIO in the GPIO mux positions denoted as OUTPUTXBARx. The GPIO module also contains an Input X-BAR which is used to route signals from any GPIO input to different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts. For more details, see the X-BAR chapter in the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*.

6.11.8.1 GPIO – Output Timing

6.11.8.1.1 General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		6(1)	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		6(1)	ns
t_{fGPO}	Toggling frequency, GPIO pins			50	MHz

(1) Rise time and fall time vary with load. These values assume a 6-pF load.

6.11.8.1.2 General-Purpose Output Timing Diagram

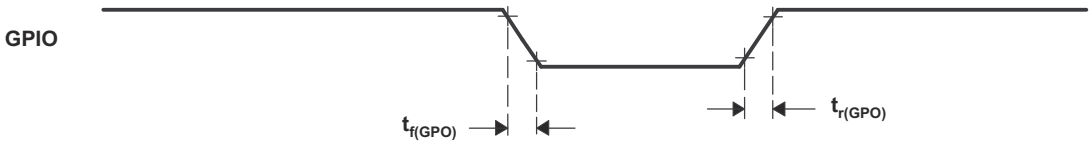


Figure 6-29. General-Purpose Output Timing

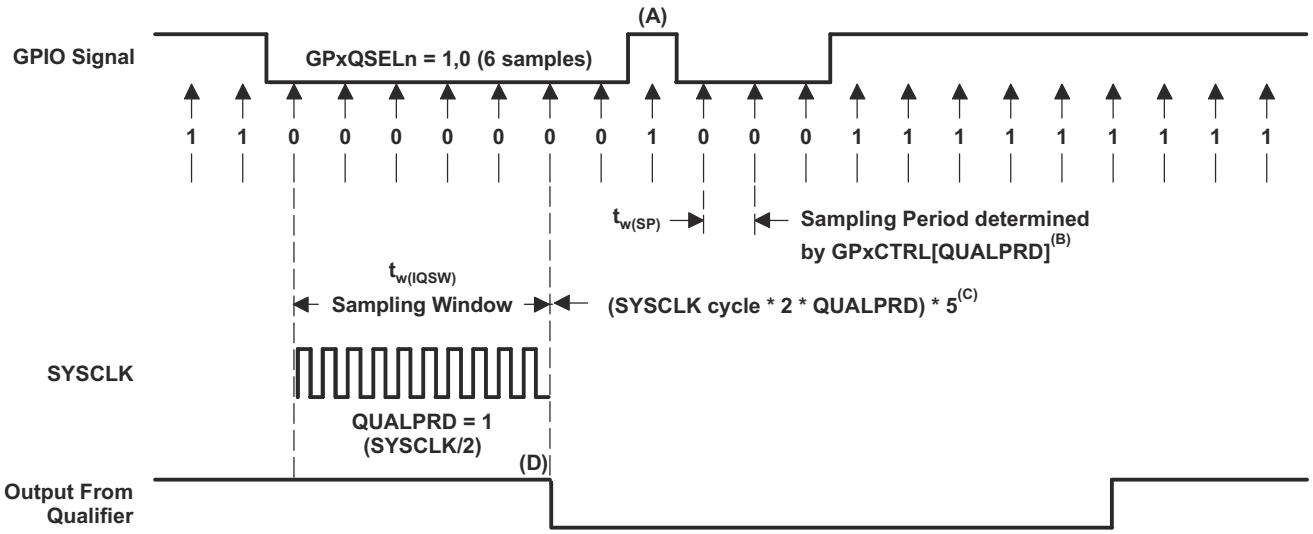
6.11.8.2 GPIO – Input Timing

6.11.8.2.1 General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SYSCLK)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SYSCLK)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n(1) – 1)		cycles
$t_{w(GPI)}$ (2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.

6.11.8.2.2 Sampling Mode



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLK cycle. For any other value "n", the qualification sampling period in 2n SYSCLK cycles (that is, at every 2n SYSCLK cycles, the GPIO pin will be sampled).
B. The qualification period selected through the GPxCTRL register applies to groups of eight GPIO pins.
C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLK cycles or greater. In other words, the inputs should be stable for (5 × QUALPRD × 2) SYSCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYSCLK-wide pulse ensures reliable recognition.

Figure 6-30. Sampling Mode

6.11.8.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

Sampling frequency = SYSCLK/(2 × QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLK, if QUALPRD = 0

Sampling period = SYSCLK cycle × 2 × QUALPRD, if QUALPRD ≠ 0

In the previous equations, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 5, if QUALPRD = 0

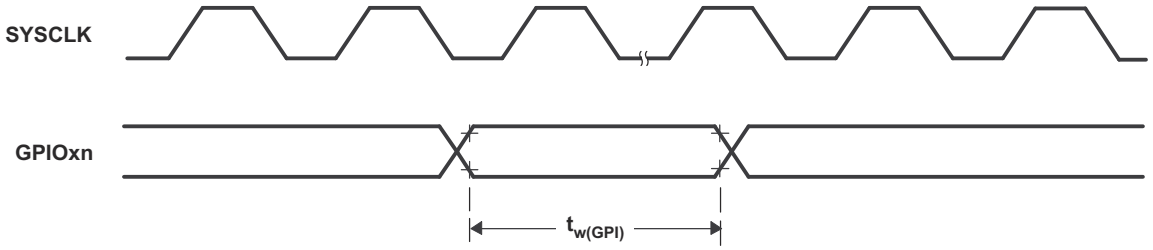


Figure 6-31. General-Purpose Input Timing

6.11.9 Interrupts

The C28x CPU has fourteen peripheral interrupt lines. Two of them (INT13 and INT14) are connected directly to CPU timers 1 and 2, respectively. The remaining twelve are connected to peripheral interrupt signals through the enhanced Peripheral Interrupt Expansion (ePIE) module. The ePIE multiplexes up to sixteen peripheral interrupts into each CPU interrupt line. It also expands the vector table to allow each interrupt to have its own ISR. This allows the CPU to support a large number of peripherals.

An interrupt path is divided into three stages—the peripheral, the ePIE, and the CPU. Each stage has its own enable and flag registers. This system allows the CPU to handle one interrupt while others are pending, implement and prioritize nested interrupts in software, and disable interrupts during certain critical tasks.

Figure 6-32 shows the interrupt architecture for this device.

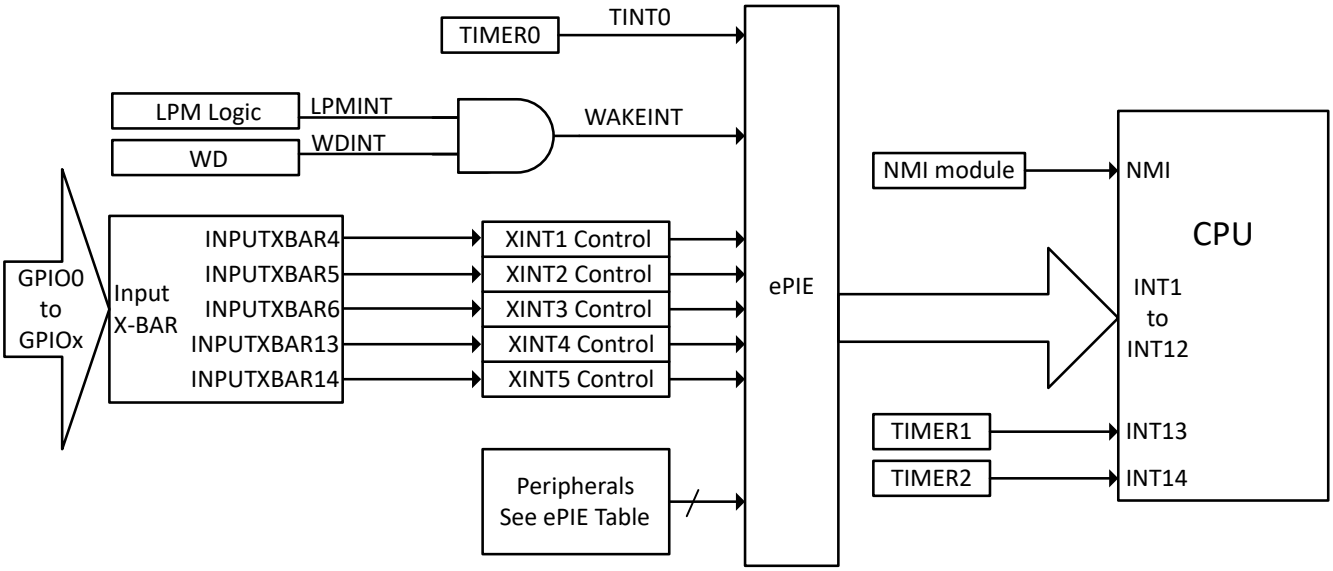


Figure 6-32. Device Interrupt Architecture

6.11.9.1 External Interrupt (XINT) Electrical Data and Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.11.9.1.1 External Interrupt Timing Requirements

			MIN	MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

6.11.9.1.2 External Interrupt Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch(1)	$t_{w(IQSW)} + 14t_{c(SYSCLK)}$	$t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCLK)}$	cycles

(1) This assumes that the ISR is in a single-cycle memory.

6.11.9.1.3 External Interrupt Timing

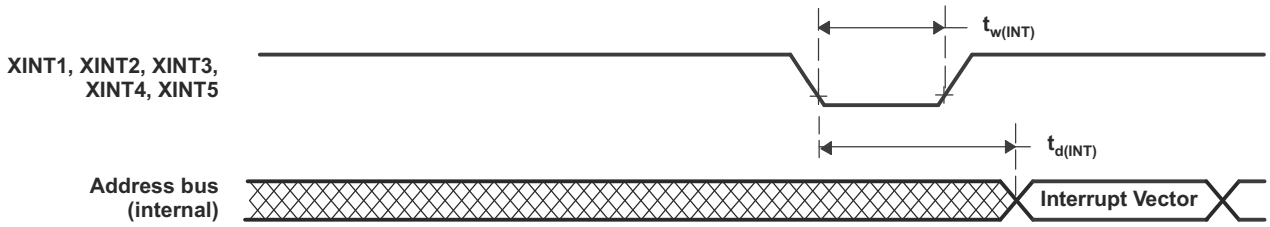


Figure 6-33. External Interrupt Timing

6.11.10 Low-Power Modes

This device has HALT, IDLE and STANDBY as clock-gating low-power modes.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the Low-Power Modes section of the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*.

6.11.10.1 Clock-Gating Low-Power Modes

IDLE and HALT modes on this device are similar to those on other C28x devices. Table 6-13 describes the effect on the system when any of the clock-gating low-power modes are entered.

Table 6-13. Effect of Clock-Gating Low-Power Modes on the Device

MODULES/ CLOCK DOMAIN	IDLE	STANDBY	HALT
SYSCLK	Active	Gated	Gated
CPUCLK	Gated	Gated	Gated
Clock to modules connected to PERx.SYSCLK	Active	Gated	Gated
WDCLK	Active	Active	Gated if CLKSRCCTL1.WDHALTI = 0
PLL	Powered	Powered	Software must power down PLL before entering HALT.
INTOSC1	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
INTOSC2	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
Flash(1)	Powered	Powered	Powered
XTAL(2)	Powered	Powered	Powered

(1) The Flash module is not powered down by hardware in any LPM. It may be powered down using software if required by the application. For more information, see the Flash and OTP Memory section of the System Control chapter in the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*.
(2) The XTAL is not powered down by hardware in any LPM. It may be powered down by software setting the XTALCR.OSCOFF bit to 1. This can be done at any time during the application if the XTAL is not required.

6.11.10.2 Low-Power Mode Wake-up Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.11.10.2.1 IDLE Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		

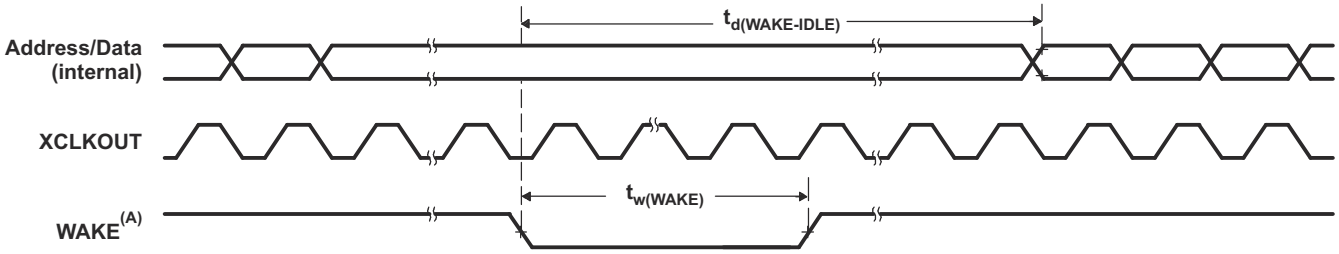
6.11.10.2.2 IDLE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume(1)	From Flash (active state)	Without input qualifier		$40t_{c(SYSCLK)}$	cycles
			With input qualifier		$40t_{c(SYSCLK)} + t_{w(WAKE)}$	cycles
		From RAM	Without input qualifier		$25t_{c(SYSCLK)}$	cycles
			With input qualifier		$25t_{c(SYSCLK)} + t_{w(WAKE)}$	cycles

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.

6.11.10.2.3 IDLE Entry and Exit Timing Diagram



A. WAKE can be any enabled interrupt, $\overline{\text{WDINT}}$ or XRSn. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

Figure 6-34. IDLE Entry and Exit Timing Diagram

6.11.10.2.4 STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	QUALSTDBY = 0 | $2t_{c(OSCCLK)}$	$3t_{c(OSCCLK)}$		cycles
		QUALSTDBY > 0 | (2 + QUALSTDBY)$t_{c(OSCCLK)}$ (1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$		

(1) QUALSTDBY is a 6-bit field in the LPMCR register.

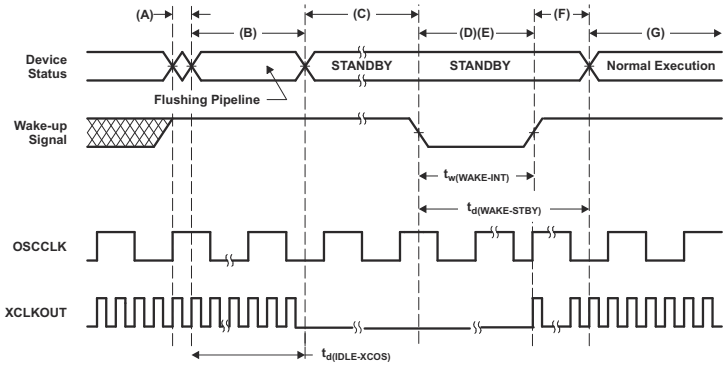
6.11.10.2.5 STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop			$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume(1)	Wakeup from flash (Flash module in active state)		$175t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	cycles
$t_{d(WAKE-STBY)}$		Wakeup from RAM		$3t_{c(OSC)} + 15t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	cycles

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.

6.11.10.2.6 STANDBY Entry and Exit Timing Diagram



A. IDLE instruction is executed to put the device into STANDBY mode.
B. The LPM block responds to the STANDBY signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. The external wake-up signal is driven active.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
F. After a latency period, the STANDBY mode is exited.
G. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 6-35. STANDBY Entry and Exit Timing Diagram

6.11.10.2.7 HALT Mode Timing Requirements

		MIN	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal(1)	t_{oscst} + $2t_{c(OSCCLK)}$		cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wake-up signal(1)	t_{oscst} + $8t_{c(OSCCLK)}$		cycles

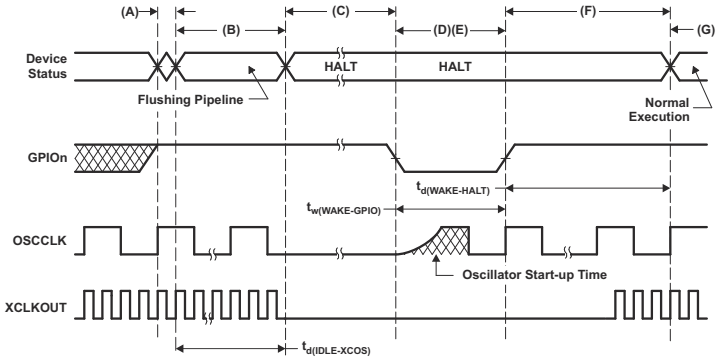
(1) For applications using X1/X2 for OSCCLK, the user must characterize their specific oscillator start-up time as it is dependent on circuit/layout external to the device. See *Crystal Oscillator (XTAL)* section for more information. For applications using INTOSC1 or INTOSC2 for OSCCLK, see the Internal Oscillators section for t_{oscst}. Oscillator start-up time does not apply to applications using a single-ended crystal on the X1 pin, as it is powered externally to the device.

6.11.10.2.8 HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop		$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-HALT)}$	Delay time, external wake signal end to CPU1 program execution resume			cycles
	Wakeup from Flash - Flash module in active state		$75t_{c(OSCCLK)}$	
	Wakeup from RAM		$75t_{c(OSCCLK)}$	

6.11.10.2.9 HALT Entry and Exit Timing Diagram



A. IDLE instruction is executed to put the device into HALT mode.
B. The LPM block responds to the HALT signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes very little power. It is possible to keep the internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT MODE. This is done by writing 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wake-up procedure, care should be taken to maintain a low noise environment before entering and during HALT mode.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after some latency. The HALT mode is now exited.
G. Normal operation resumes.
H. The user must relock the PLL upon HALT wakeup to ensure a stable PLL lock.

Figure 6-36. HALT Entry and Exit Timing Diagram

6.12 Analog Peripherals

The analog subsystem module is described in this section.

The analog modules on this device include the Analog-to-Digital Converter (ADC), Temperature Sensor, Comparator Subsystem (CMPSS), and Lite Comparator Subsystem variant (CMPSS_LITE).

The analog subsystem has the following features:

- Flexible voltage references
  - The ADCs are referenced to VREFHI and VSSA pins
    - VREFHI pin voltage can be driven in externally or can be generated by an internal bandgap voltage reference
    - The internal voltage reference range can be selected to be 0 V to 3.3 V or 0 V to 2.5 V
  - The comparator DACs are referenced to VDDA and VSSA
- Flexible pin usage
  - Comparator subsystem inputs and digital inputs (AIOs)/outputs (AGPIOs) are multiplexed with ADC inputs
  - Low comparator DAC (CMPx_DACL) can optionally be brought out to a multiplexed ADC pin for external use (mutually exclusive with use of CMPSS compare functions and only available on some CMPSS instances)
  - Internal connection to VREFLO on all ADCs for offset self-calibration

Figure 6-37 shows the Analog Subsystem Block Diagram for all packages. Figure 6-38 shows the analog group connections. Section 6.12.1 lists the analog pins and internal connections. Section 6.12.2 lists descriptions of analog signals.

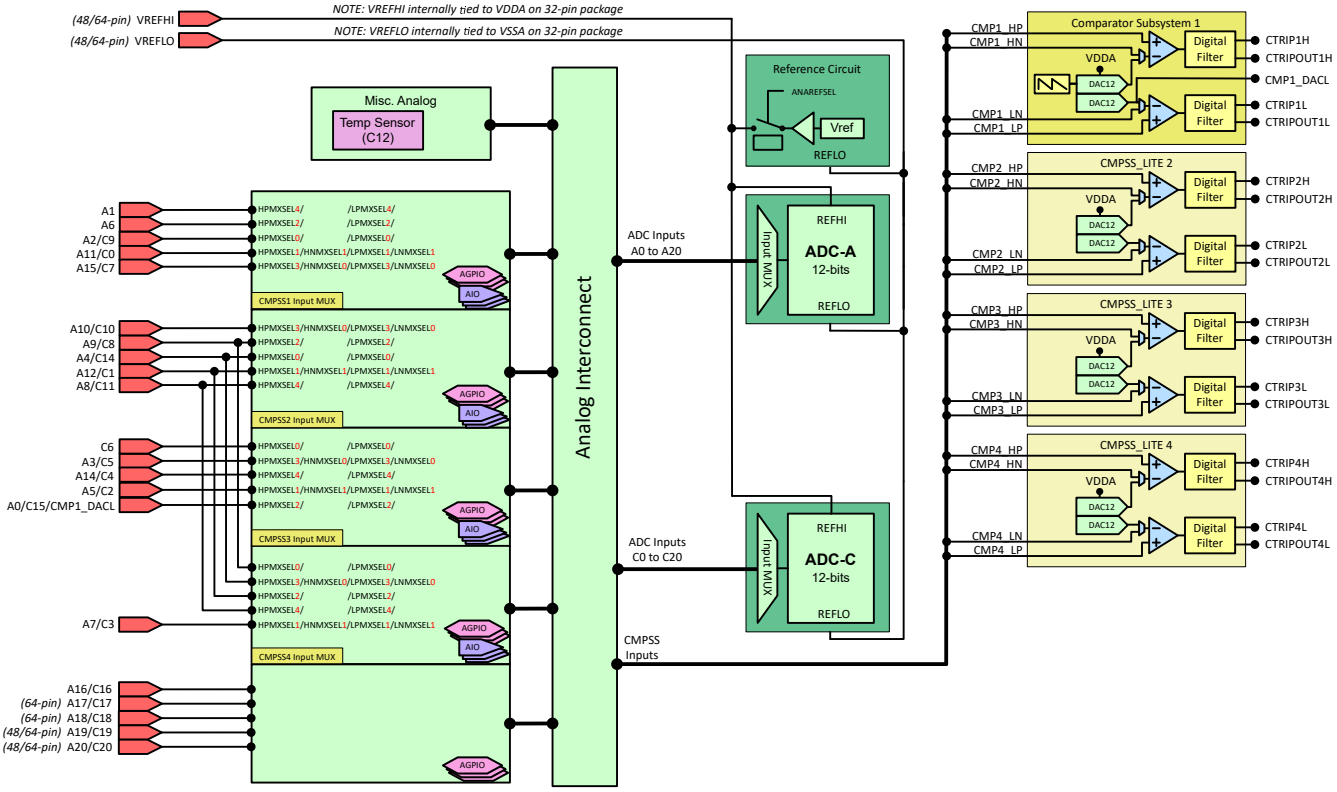
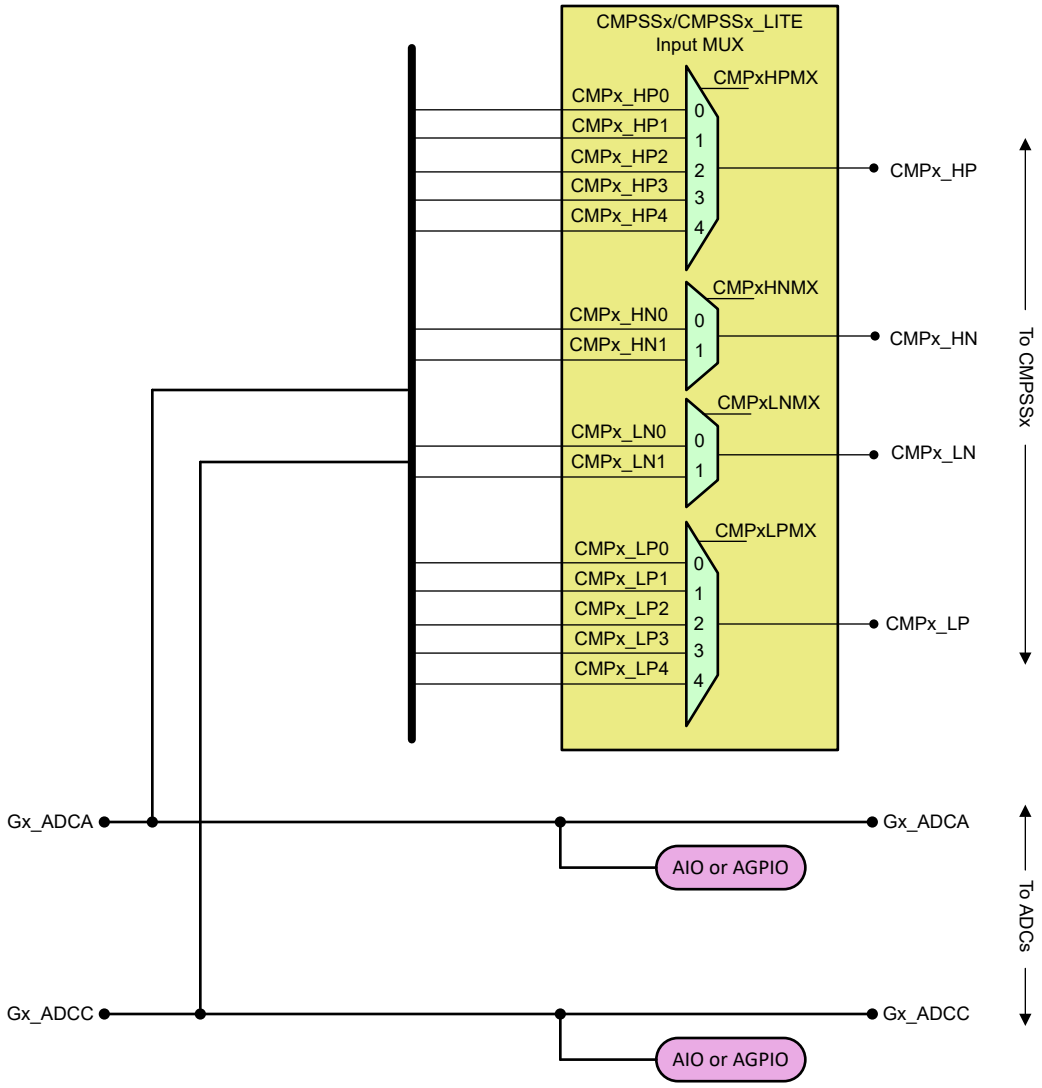


Figure 6-37. Analog Subsystem Block Diagram



Note: AIOs support digital input mode only.

Figure 6-38. Analog Group Connections

6.12.1 Analog Pins and Internal Connections

Table 6-14. Analog Pins and Internal Connections

Pin Name	Pins/Package				ADC		DAC	Comparator Subsystem (Mux)				AIO Input/ GPIO
	64 QFP[5]	48 QFP	48 QFN	32 QFN	A	C		High Positive	High Negative	Low Positive	Low Negative	
VREFHI	16	12	12	-[4]								
VREFLO	17	13	13	-[4]	A13	C13						
Analog Group 1								**CMP1**				
A6	6	4[1]	4[1]	2[1]	A6	-		CMP1 (HPMXSEL=2)		CMP1 (LPMXSEL=2)		GPIO228[3]
A2/C9	9	6	6	4	A2	C9		CMP1 (HPMXSEL=0)		CMP1 (LPMXSEL=0)		GPIO224[3]
A15/C7	10	7[1]	7[1]	5[1]	A15	C7		CMP1 (HPMXSEL=3)	CMP1 (HNMXSEL=0)	CMP1 (LPMXSEL=3)	CMP1 (LNMXSEL=0)	AIO233
A11/C0	12	8	8	6[1]	A11	C0		CMP1 (HPMXSEL=1)	CMP1 (HNMXSEL=1)	CMP1 (LPMXSEL=1)	CMP1 (LNMXSEL=1)	AIO237
A1	14	10	10	7[1]	A1	-		CMP1 (HPMXSEL=4)		CMP1 (LPMXSEL=4)		AIO232
Analog Group 2								**CMP2**				
A10/C10	25	21	21	13[1]	A10	C10		CMP2 (HPMXSEL=3)	CMP2 (HNMXSEL=0)	CMP2 (LPMXSEL=3)	CMP2 (LNMXSEL=0)	GPIO230[3]
Analog Group 3								**CMP3**				
C6	7	4[1]	4[1]	2[1]	-	C6		CMP3 (HPMXSEL=0)		CMP3 (LPMXSEL=0)		GPIO226[3]
A3/C5	8	5	5	3	A3	C5		CMP3 (HPMXSEL=3)	CMP3 (HNMXSEL=0)	CMP3 (LPMXSEL=3)	CMP3 (LNMXSEL=0)	GPIO242[3]
A14/C4	11	7[1]	7[1]	5[1]	A14	C4		CMP3 (HPMXSEL=4)		CMP3 (LPMXSEL=4)		AIO239
A5/C2	13	9	9	6[1]	A5	C2		CMP3 (HPMXSEL=1)	CMP3 (HNMXSEL=1)	CMP3 (LPMXSEL=1)	CMP3 (LNMXSEL=1)	AIO244
A0/C15/CMP1_DACL	15	11	11	7[1]	A0	C15	CMP1_ DACL	CMP3 (HPMXSEL=2)		CMP3 (LPMXSEL=2)		AIO231
Analog Group 4								**CMP4**				
A7/C3	19	15	15	8[1]	A7	C3		CMP4 (HPMXSEL=1)	CMP4 (HNMXSEL=1)	CMP4 (LPMXSEL=1)	CMP4 (LNMXSEL=1)	AIO245
Combined Analog Group 2/4								**CMP2/4**				
A12/C1	18	14	14	8[1]	A12	C1		CMP2 (HPMXSEL=1) CMP4 (HPMXSEL=2)	CMP2 (HNMXSEL=1)	CMP2 (LPMXSEL=1) CMP4 (LPMXSEL=2)	CMP2 (LNMXSEL=1)	AIO238
A8/C11	20	16	16	9	A8	C11		CMP2 (HPMXSEL=4) CMP4 (HPMXSEL=4)		CMP2 (LPMXSEL=4) CMP4 (LPMXSEL=4)		AIO241
A4/C14	23	19	19	12	A4	C14		CMP2 (HPMXSEL=0) CMP4 (HPMXSEL=3)	CMP4 (HNMXSEL=0)	CMP2 (LPMXSEL=0) CMP4 (LPMXSEL=3)	CMP4 (LNMXSEL=0)	AIO225
A9/C8	24	20	20	13[1]	A9	C8		CMP2 (HPMXSEL=2) CMP4 (HPMXSEL=0)		CMP2 (LPMXSEL=2) CMP4 (LPMXSEL=0)		GPIO227[3]
Other Analog												
TempSensor[2]	-	-	-	-	-	C12		CMP2 (HPMXSEL=5)				
A16/C16	2	2	2	32	A16	C16						GPIO28[3]
A17/C17	27	-	-	-	A17	C17						GPIO20[3]
A18/C18	28	-	-	-	A18	C18						GPIO21[3]
A19/C19	29	23	22	-	A19	C19						GPIO13[3]

Table 6-14. Analog Pins and Internal Connections (continued)

Pin Name	Pins/Package				ADC		DAC	Comparator Subsystem (Mux)				AIO Input/ GPIO
	64 QFP[5]	48 QFP	48 QFN	32 QFN	A	C		High Positive	High Negative	Low Positive	Low Negative	
A20/C20	30	24	23	-	A20	C20						GPIO12[3]

(1) Signal is bonded together with another signal as a single pin on this package.
(2) Internal connection only; does not come to a device pin.
(3) The GPIOs on these analog pins support full digital input and output functionality and are referred to as AGPIOs. By default, the AGPIOs are unconnected; that is, the analog and digital functions are both disabled. For configuration details, see the *Digital Inputs and Outputs on ADC Pins (AGPIOs)* section.
(4) On 32 RHB package, VREFHI is internally connected to VDDA and VREFLO is internally connected to VSSA.
(5) Column applies to both 64 PM and 64 PM with VREGENZ (VPM) variants.

6.12.2 Analog Signal Descriptions

Table 6-15. Analog Signal Descriptions

Signal Name	Description
AIOx	Digital input on ADC pin
Ax	ADC A Input
Cx	ADC C Input
CMPx_HNy	Comparator subsystem high comparator negative input
CMPx_HPy	Comparator subsystem high comparator positive input
CMPx_LNy	Comparator subsystem low comparator negative input
CMPx_LPy	Comparator subsystem low comparator positive input
CMPx_DACL	DAC output from the lower CMPSS DAC (can be brought to an external pin)
TempSensor	Internal temperature sensor

6.12.3 Analog-to-Digital Converter (ADC)

The ADC module described here is a successive approximation (SAR) style ADC with resolution of 12 bits. This section refers to the analog circuits of the converter as the “core,” and includes the channel-select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The digital circuits of the converter are referred to as the “wrapper” and include logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module consists of a single sample-and-hold (S/H) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is start-of-conversion (SOC)-based (see the SOC Principle of Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*).

Each ADC has the following features:

- Resolution of 12 bits
- Ratiometric external reference set by VREFHI/VREFLO
- Selectable internal reference of 2.5 V or 3.3 V
- Single-ended signal mode
- Input multiplexer with up to 21 channels
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
  - Software immediate start
  - All ePWMs: ADCSOC A or B
  - GPIO XINT2
  - CPU Timers 0/1/2
  - ADCINT1/2
- Four flexible PIE interrupts
- Burst-mode triggering option
- Four post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
  - Trigger-to-sample delay capture

Note

Not every channel can be pinned out from all ADCs. See the Pin Configuration and Functions section to determine which channels are available.

The block diagram for the ADC core and ADC wrapper are shown in Figure 6-39.

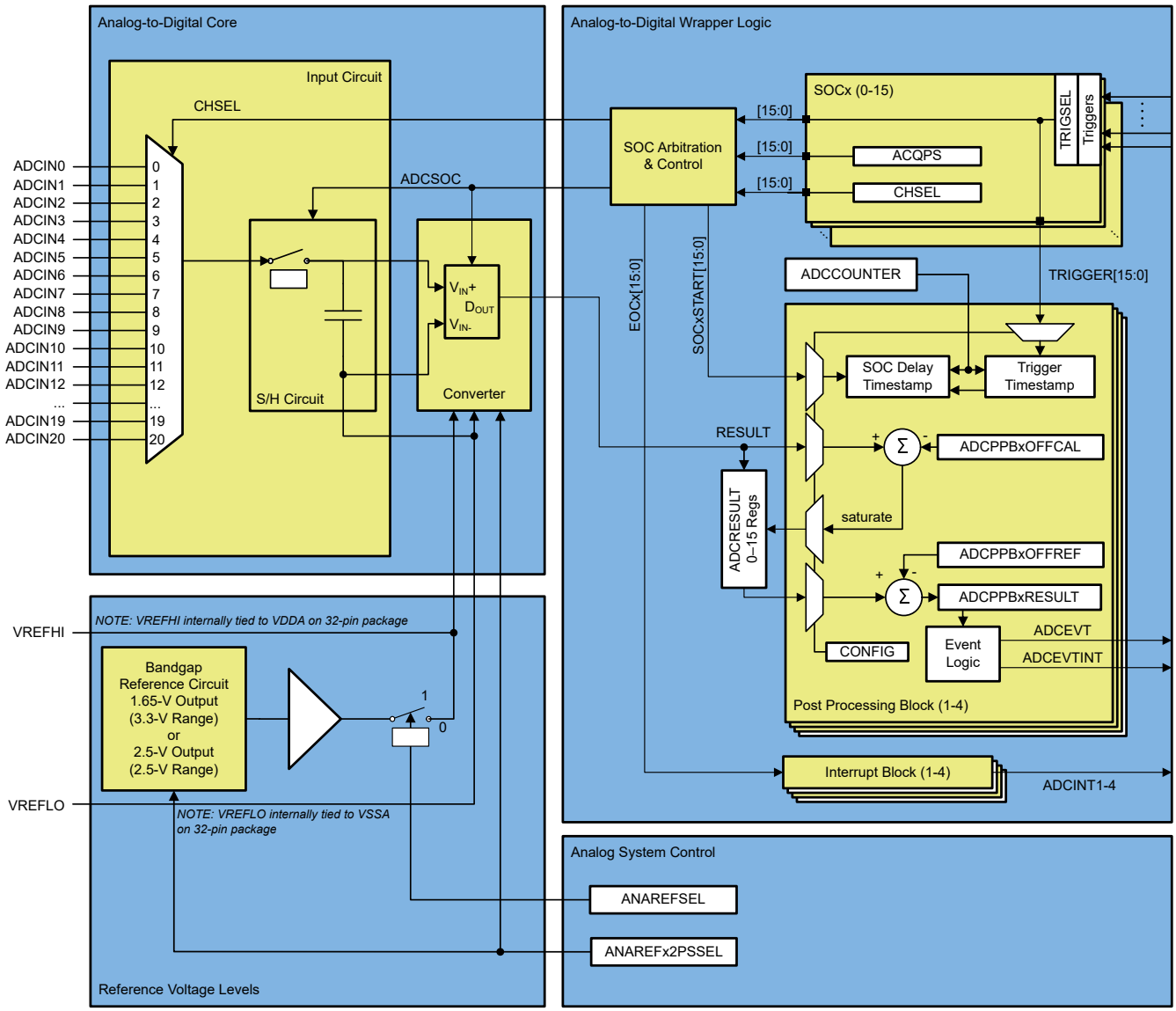


Figure 6-39. ADC Module Block Diagram

6.12.3.1 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are globally controlled per ADC module. Table 6-16 summarizes the basic ADC options and their level of configurability.

Table 6-16. ADC Options and Configuration Levels

OPTIONS	CONFIGURABILITY
Clock	Per module(1)
Resolution	Not configurable (12-bit resolution only)
Signal mode	Not configurable (single-ended signal mode only)
Reference voltage source	Either external or internal for all modules
Trigger source	Per SOC(1)
Converted channel	Per SOC
Acquisition window duration	Per SOC(1)
EOC location	Per module
Burst mode	Per module(1)

(1) Writing these values differently to different ADC modules could cause the ADCs to operate asynchronously. For guidance on when the ADCs are operating synchronously or asynchronously, see the Ensuring Synchronous Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*.

6.12.3.1.1 Signal Mode

The ADC supports single-ended signaling. The input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO.

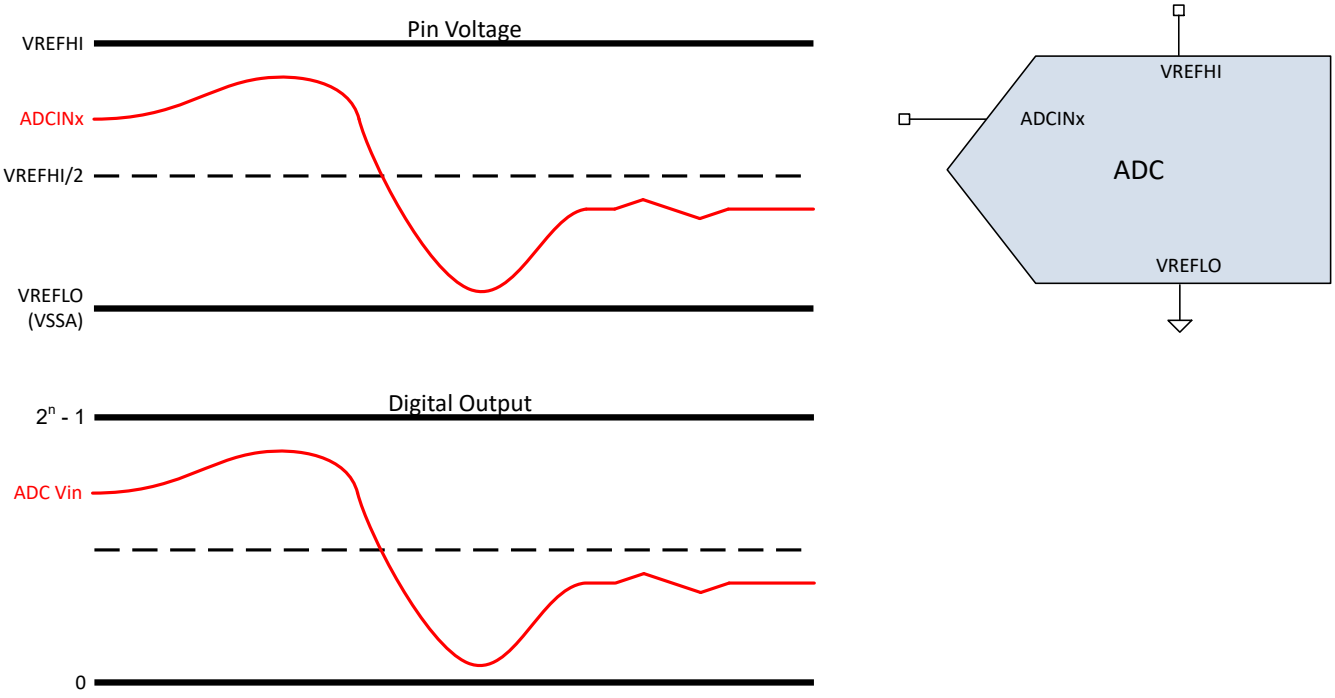


Figure 6-40. Single-ended Signaling Mode

6.12.3.2 ADC Electrical Data and Timing

Note

The ADC inputs should be kept below VDDA + 0.3 V. If an ADC input goes above this level ADC disturbances to other channels may occur by two mechanisms:

- ADC input over-voltage will overdrive the CMPSS mux, disturbing all other channels which share a common CMPSS mux. This disturbance will be continuous regardless of if the over-voltage input is sampled by the ADC
- When the ADC samples the over-voltage ADC input, VREFHI will be pulled up to a higher level. This will disturb subsequent ADC conversions on any channel until the V_{REF} stabilizes

Note

The VREFHI pin must be kept below VDDA + 0.3 V to ensure proper functional operation. If the VREFHI pin exceeds this level, a blocking circuit may activate, and the internal value of VREFHI may float to 0 V internally, giving improper ADC conversion.

6.12.3.2.1 ADC Operating Conditions

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)	F2800137, F2800135, F2800133	5		60	MHz
	F2800132	5		50	
Sample rate	120-MHz SYSCLK F2800137, F2800135, F2800133			4	MSPS
	100-MHz SYSCLK F2800132			3.45	
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	With 50 Ω or less R_s	75			ns
	Internal VREFLO Connection	75			
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI(2)	Internal Reference = 3.3V Range		1.65		V
	Internal Reference = 2.5V Range		2.5		V
VREFHI	Package = 32QFN	VDDA	VDDA	VDDA	V
VREFLO		VSSA		VSSA	V
VREFHI - VREFLO		2.4		VDDA	V
Conversion range	Internal Reference = 3.3 V Range	0		3.3	V
	Internal Reference = 2.5 V Range	0		2.5	
	External Reference	VREFLO		VREFHI	
	Package = 32QFN	0		VDDA(3)	

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.
(3) On 32QFN package, VREFHI is internally tied to VDDA and VREFLO is internally tied to VSSA. Internal reference mode is not supported on 32QFN package.

6.12.3.2.2 ADC Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles	120-MHz SYSCLK	10.1		11	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5-V range and 3.3-V range.			5000	µs
VREFHI input current(1)			130		µA
Internal Reference Capacitor Value(2)		2.2			µF
External Reference Capacitor Value(2)		2.2			µF
DC Characteristics					
Gain Error	Internal reference	–45		45	LSB
	External reference	–5	±3	5	
Offset Error		–5	±2	5	LSB
Channel-to-Channel Gain Error(4)			2		LSB
Channel-to-Channel Offset Error(4)			2		LSB
ADC-to-ADC Gain Error(5)	Identical VREFHI and VREFLO for all ADCs		4		LSB
ADC-to-ADC Offset Error(5)	Identical VREFHI and VREFLO for all ADCs		2		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–2	±1.0	2	LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–1		1	LSBs
AC Characteristics					
SNR(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		68.8		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC		60.1		
THD(3)	VREFHI = 2.5 V, fin = 100 kHz		–80.6		dB
SFDR(3)	VREFHI = 2.5 V, fin = 100 kHz		79.2		dB
SINAD(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		68.5		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC		60.0		
ENOB(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC		11.0		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs		11.0		
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs		Not Supported		

6.12.3.2.2 ADC Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz		60		dB
	VDD = 1.2-V DC + 100 mV DC up to Sine at 300 kHz		57		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		60		
	VDDA = 3.3-V DC + 200 mV Sine at 900 kHz		57		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(4) Variation across all channels belonging to the same ADC module.
(5) Worst case variation compared to other ADC modules.

6.12.3.2.3 ADC Performance Per Pin

ADC performance of each pin is affected by adjacent pins. The following plots provide details on how these pins differ in performance.

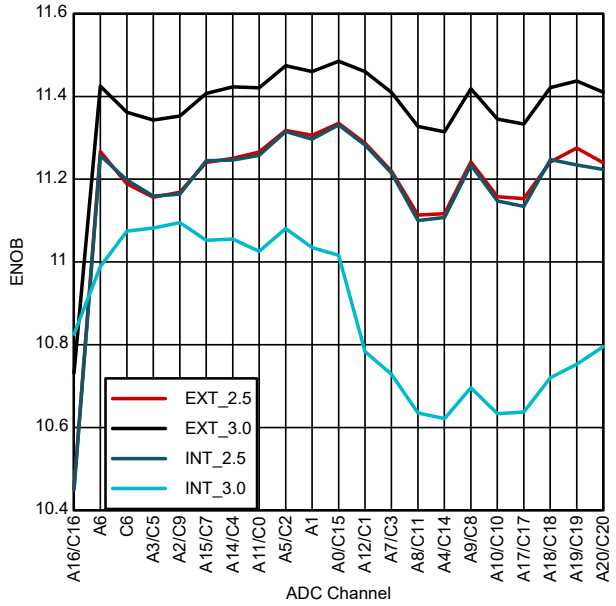


Figure 6-41. Per-Channel ENOB for 64-Pin PM LQFP

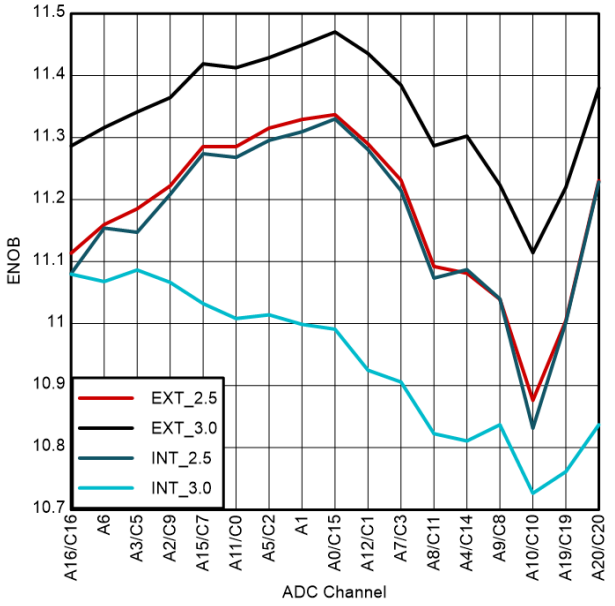


Figure 6-42. Per-Channel ENOB for 48-Pin PT LQFP

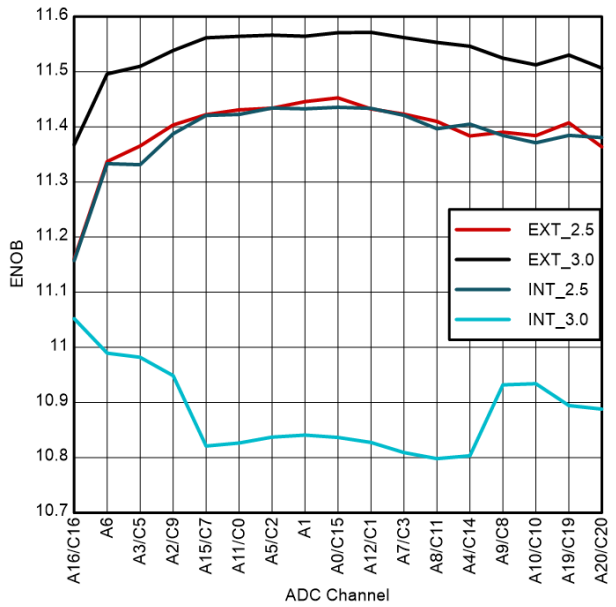


Figure 6-43. Per-Channel ENOB for 48-Pin RGZ VQFN

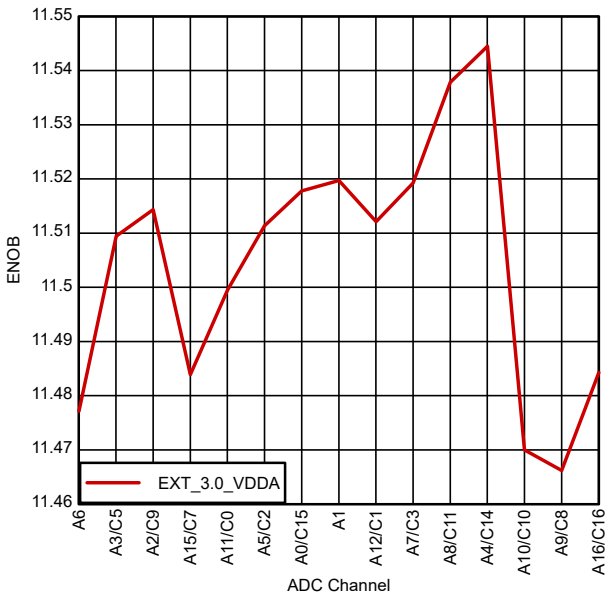


Figure 6-44. Per-Channel ENOB for 32-Pin RHB VQFN

6.12.3.2.4 ADC Input Model

The ADC input characteristics are given by Table 6-17 and Figure 6-45.

Table 6-17. Input Model Parameters

	DESCRIPTION	REFERENCE MODE	VALUE
C_p	Parasitic input capacitance	All	See Table 6-18 to Table 6-21
R_{on}	Sampling switch resistance	External Reference, 2.5-V Internal Reference	500 Ω
		3.3-V Internal Reference	860 Ω
C_h	Sampling capacitor	External Reference, 2.5-V Internal Reference	12.5 pF
		3.3-V Internal Reference	7.5 pF
R_s	Nominal source impedance	All	50 Ω

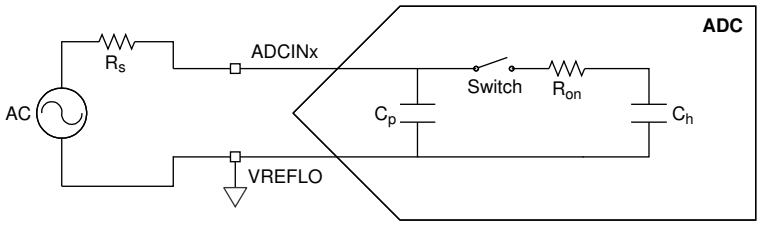


Figure 6-45. Input Model

This input model should be used with actual signal source impedance to determine the acquisition window duration. For more information, see the Choosing an Acquisition Window Duration section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*. For recommendations on improving ADC input circuits, see the *ADC Input Circuit Evaluation for C2000 MCUs* Application Report.

Table 6-18. Per-Channel Parasitic Capacitance for 64-Pin PM LQFP

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A0/C15/CMP1_DACL	7.7	10.2
A1	1.6	4.1
A2/C9	1.5	4
A3/C5	1.8	4.3
A4/C14	2.4	4.9
A5/C2	2	4.5
A6	1.4	3.9
A7/C3	1.9	4.4
A8/C11	2.2	4.7
A9/C8	2.3	4.8
A10/C10	2	4.5
A11/C0	2.4	4.9
A12/C1	3.2	5.7
A14/C4/ADCINCAL	2.4	4.9
A15/C7	3	5.5
A16/C16	2.4	4.9
A17/C17	2.7	5.2
A18/C18	2.7	5.2
A19/C19	2.7	5.2

Table 6-18. Per-Channel Parasitic Capacitance for 64-Pin PM LQFP (continued)

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A20/C20	2.7	5.2
C6	1.7	4.2

Table 6-19. Per-Channel Parasitic Capacitance for 48-Pin PT LQFP

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A0/C15/CMP1_DACL	7.7	10.2
A1	1.6	4.1
A2/C9	1.5	4
A3/C5	1.8	4.3
A4/C14	2.4	4.9
A5/C2	2	4.5
A6/C6	3.1	8.1
A7/C3	1.9	4.4
A8/C11	2.2	4.7
A9/C8	2.3	4.8
A10/C10	2	4.5
A11/C0	2.4	4.9
A12/C1	3.2	5.7
A14/A15/C4/C7/ADCINCAL	5.4	10.4
A16/C16	2.4	4.9
A19/C19	2.7	5.2
A20/C20	2.7	5.2

Table 6-20. Per-Channel Parasitic Capacitance for 48-Pin RGZ VQFN

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A0/C15/CMP1_DACL	7.7	10.2
A1	1.6	4.1
A2/C9	1.5	4
A3/C5	1.8	4.3
A4/C14	2.4	4.9
A5/C2	2	4.5
A6/C6	3.1	8.1
A7/C3	1.9	4.4
A8/C11	2.2	4.7
A9/C8	2.3	4.8
A10/C10	2	4.5
A11/C0	2.4	4.9
A12/C1	3.2	5.7
A14/A15/C4/C7/ADCINCAL	5.4	10.4
A16/C16	2.4	4.9
A19/C19	2.7	5.2
A20/C20	2.7	5.2

Table 6-21. Per-Channel Parasitic Capacitance for 32-Pin RHB VQFN

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A0/A1/C15/CMP1_DACL	9.3	14.3
A2/C9	1.5	4
A3/C5	1.8	4.3
A4/C14	2.4	4.9
A5/C2/A11/C0	4.4	9.4
A6/C6	3.1	8.1
A7/C3/A12/C1	5.1	10.1
A8/C11	2.2	4.7
A9/C8/A10/C10	4.3	9.3
A14/A15/C4/C7/ADCINCAL	5.4	10.4
A16/C16	2.4	4.9

6.12.3.2.5 ADC Timing Diagrams

Figure 6-46 shows the ADC conversion timings for two SOCs given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOCs are converting or pending when the trigger occurs.
- The round-robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the PIE module).

Table 6-22 lists the descriptions of the ADC timing parameters. Table 6-23 lists the ADC timings.

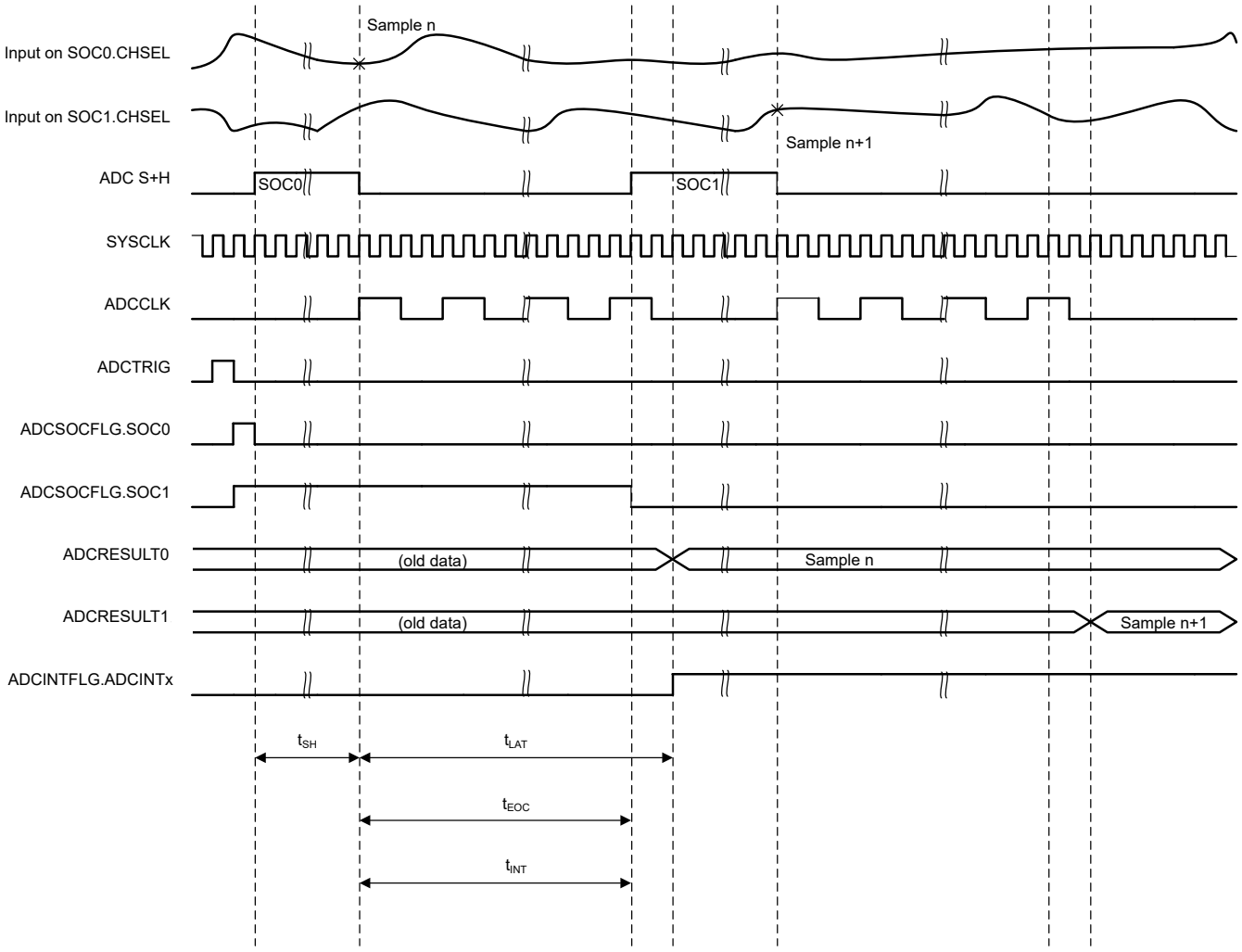


Figure 6-46. ADC Timings

Table 6-22. ADC Timing Parameter Descriptions

Parameter	Description
t_{SH}	The duration of the S+H window. At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by (ACQPS + 1) SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} is not necessarily the same for different SOCs. **Note:** The value on the S+H capacitor is captured approximately 5 ns before the end of the S+H window regardless of device clock settings.
t_{LAT}	The time from the end of the S+H window until the ADC results latch in the ADCRESULTx register. If the ADCRESULTx register is read before this time, the previous conversion results are returned.

Table 6-22. ADC Timing Parameter Descriptions (continued)

Parameter	Description
t_{EOC}	The time from the end of the S+H window until the S+H window for the next ADC conversion can begin. The subsequent sample can start before the conversion results are latched.
t_{INT}	The time from the end of the S+H window until an ADCINT flag is set (if configured). If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} coincides with the end of conversion (EOC) signal. If the INTPULSEPOS bit is 0, t_{INT} coincides with the end of the S+H window. If t_{INT} triggers a read of the ADC result register (by triggering an ISR that reads the result), care must be taken to make sure the read occurs after the results latch (otherwise, the previous results are read). If the INTPULSEPOS bit is 0, and the OFFSET field in the ADCINTCYCLE register is not 0, then there is a delay of OFFSET SYSCLK cycles before the ADCINT flag is set. This delay can be used to enter the ISR exactly when the sample is ready.

Table 6-23. ADC Timings in 12-bit Mode

ADCCLK Prescale		SYSCLK Cycles			
ADCCTL2. PRESCALE	Prescale Ratio	t_{EOC}	t_{LAT}	t_{INT} (Early)(1)	t_{INT} (Late)
0	1	11	13	0	11
2	2	21	23	0	21
4	3	31	34	0	31
6	4	41	44	0	41
8	5	51	55	0	51
10	6	61	65	0	61
12	7	71	76	0	71
14	8	81	86	0	81

(1) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

6.12.4 Temperature Sensor

6.12.4.1 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time in the Temperature Sensor Characteristics table.

6.12.4.1.1 Temperature Sensor Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{acc}	Temperature Accuracy	Internal reference (-40°C to 30°C)	-15	±2	15	°C
		Internal reference (30°C to 85°C)	-9	±2	7	°C
		Internal reference (85°C to 125°C)	-5	±2	8	°C
		Internal reference (125°C to 140°C)	-6	±2	12	°C
		External reference (-40°C to 30°C)	-8	±2	10	°C
		External reference (30°C to 140°C)	-5	±2	8	°C
$t_{startup}$	Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor)			500		µs
t_{acq}	ADC acquisition time		450			ns

6.12.5 Comparator Subsystem (CMPSS)

The Comparator Subsystem (CMPSS) consists of analog comparators and supporting circuits that are useful for power applications such as peak current mode control, switched-mode power supply, power factor correction, voltage trip monitoring, and so forth.

This device contains two variants of the CMPSS module: CMPSS and CMPSS_LITE. These modules share a common architecture, but some features are supported only by the full CMPSS variant and not the CMPSS_LITE variant.

The comparator subsystem is built around a number of modules. Each subsystem contains two comparators, two reference 12-bit DACs (CMPSS_LITE instances are 9.5-bit effective reference DACs), and two digital filters. The subsystem also includes one ramp generator (full CMPSS modules only; not supported by CMPSS_LITE instances). Comparators are denoted "H" or "L" within each module where “H” and “L” represent high and low, respectively. Each comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator is driven from an external pin (see the *Analog Subsystem* chapter of the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual* for mux options available to the CMPSS). The negative input can be driven by an external pin or by the programmable reference 12-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required. A ramp generator circuit is optionally available to control the reference 12-bit DAC value for the high comparator in the subsystem (full CMPSS modules only; not supported by CMPSS_LITE instances).

Each CMPSS includes:

- Two analog comparators
- Two programmable reference 12-bit DACs (9.5-bit effective DACs on CMPSS_LITE instances)
- One ramp generator (full CMPSS only; not available on CMPSS_LITE instances)
- Two digital filters, 65536 max filter clock prescale
- Ability to synchronize submodules with EPWMSYNCPER
- Ability to extend clear signal with EPWMBLANK
- Ability to synchronize output with SYSCLK
- Ability to latch output
- Ability to invert output
- Option to use hysteresis on the input
- Option for negative input of comparator to be driven by an external signal or by the reference DAC
- Option to use the low comparator DAC output, CMPx_DACL, on an external pin (select instances only, mutually exclusive with use of compare functionality)

6.12.5.1 CMPSS Module Variants

This device contains two different variants of the CMPSS module: CMPSS (full module) and the CMPSS_LITE (reduced functionality and performance). The differences in features between the two variants are summarized in Table 6-24.

Table 6-24. CMPSS and CMPSS_LITE Feature Comparison

FEATURE	CMPSS	CMPSS_LITE
High and low comparators	Yes	Yes
Dual 12-bit reference DACs	Yes	Yes (9.5-bit effective)
DAC ramp generation	Yes	No
Low DAC output on external pin	Yes (Some instances)	No
Digital filters	Yes	Yes
Performance	Full performance (see the CMPSS Comparator Electrical Characteristics table)	Some reduced performance (see the CMPSS_LITE Comparator Electrical Characteristics table)

6.12.5.2 CMPx_DACL

Some CMPSS module instances have support for DAC output buffered to a pin. This CMPx_DACL output from the CMPSS module uses the low-side DAC of the CMPSS module specified. When using DAC output from a CMPSS instance, all other CMPSS module features for that instance are unavailable.

For CMPx_DACL instances available for a particular device, please see the DAC column of the *Analog Pins and Internal Connections* table.

See the *Buffered Output from CMPx_DACL Electrical Characteristics* section for DAC output capabilities.

6.12.5.3 CMPSS Connectivity Diagram

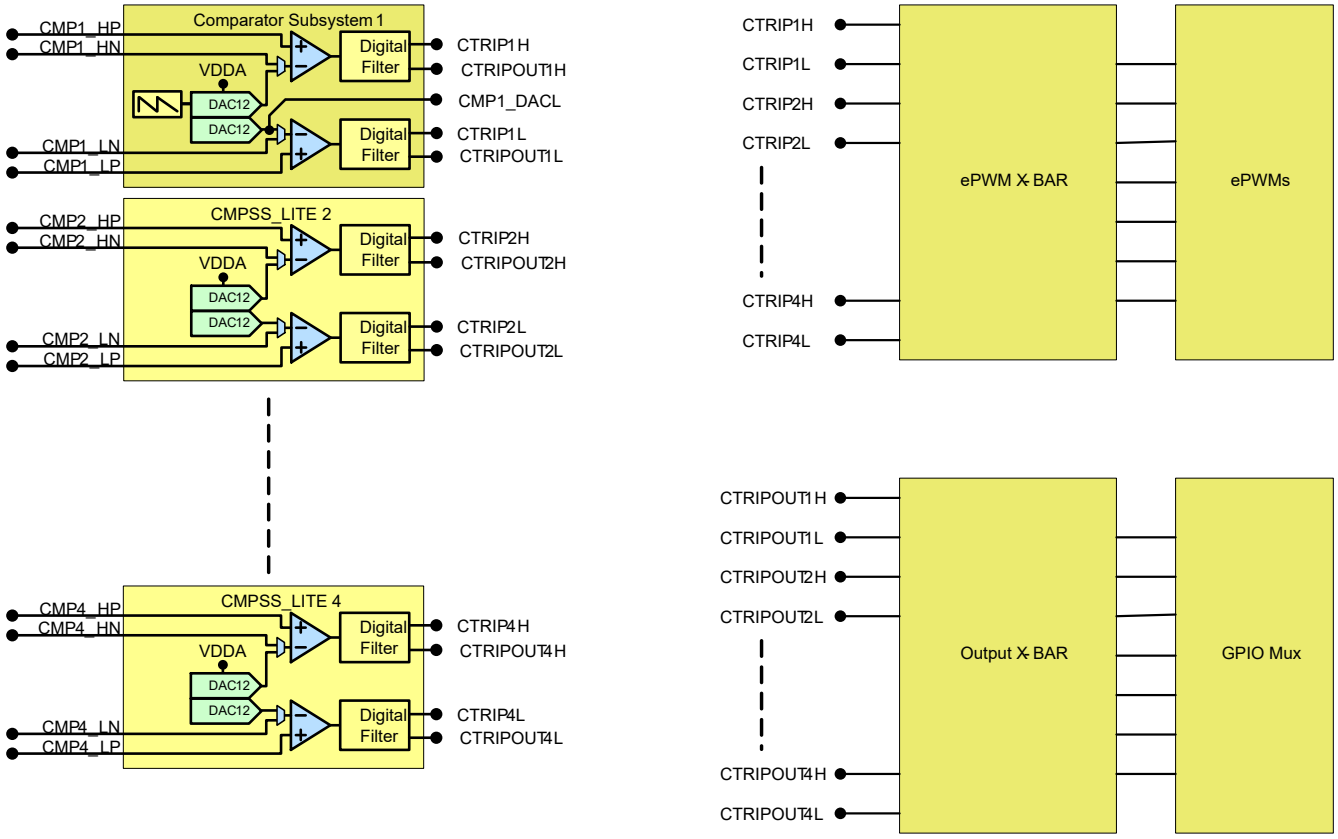


Figure 6-47. CMPSS Connectivity

6.12.5.4 Block Diagrams

The block diagram for the CMPSS is shown in Figure 6-48.The block diagram for the CMPSS_LITE is shown in Figure 6-49.

- CTRIPx(x= "H" or "L") signals are connected to the ePWM X-BAR for ePWM trip response. See the *Enhanced Pulse Width Modulator (ePWM)* chapter of the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual* for more details on the ePWM X-BAR mux configuration.
- CTRIPxOUTx(x= "H" or "L") signals are connected to the Output X-BAR for external signaling. See the *General-Purpose Input/Output (GPIO)* chapter of the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual* for more details on the Output X-BAR mux configuration.

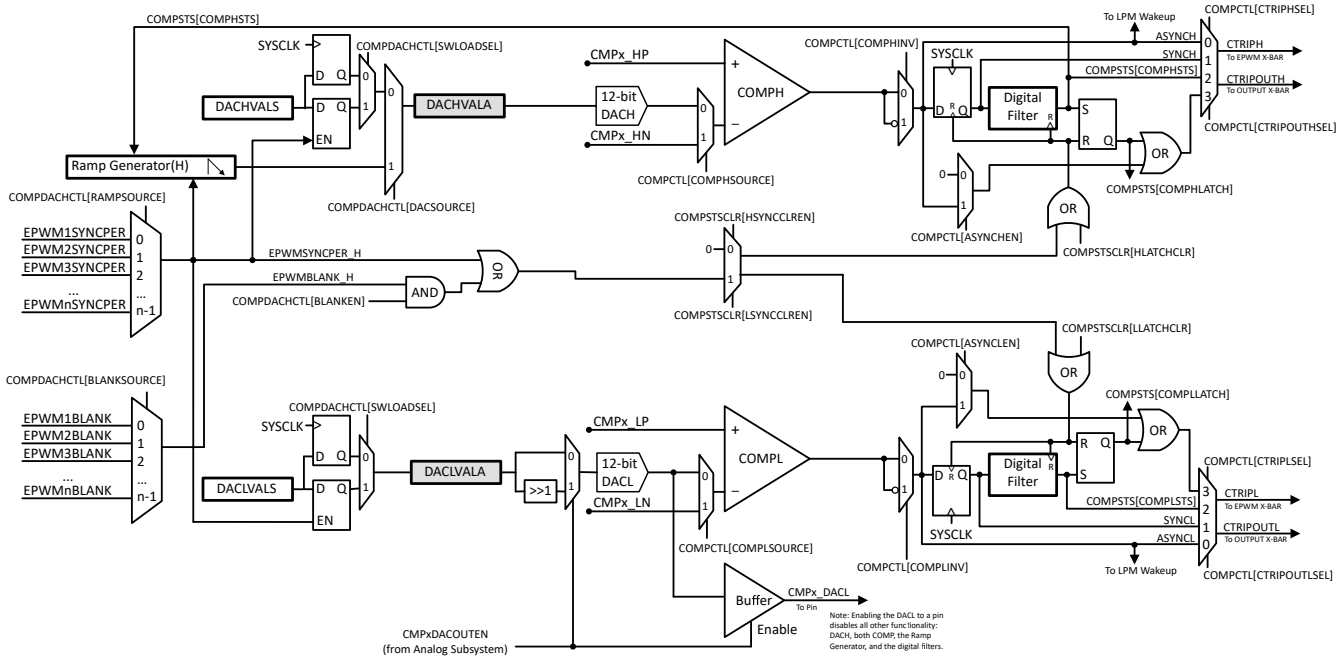


Figure 6-48. CMPSS Module Block Diagram

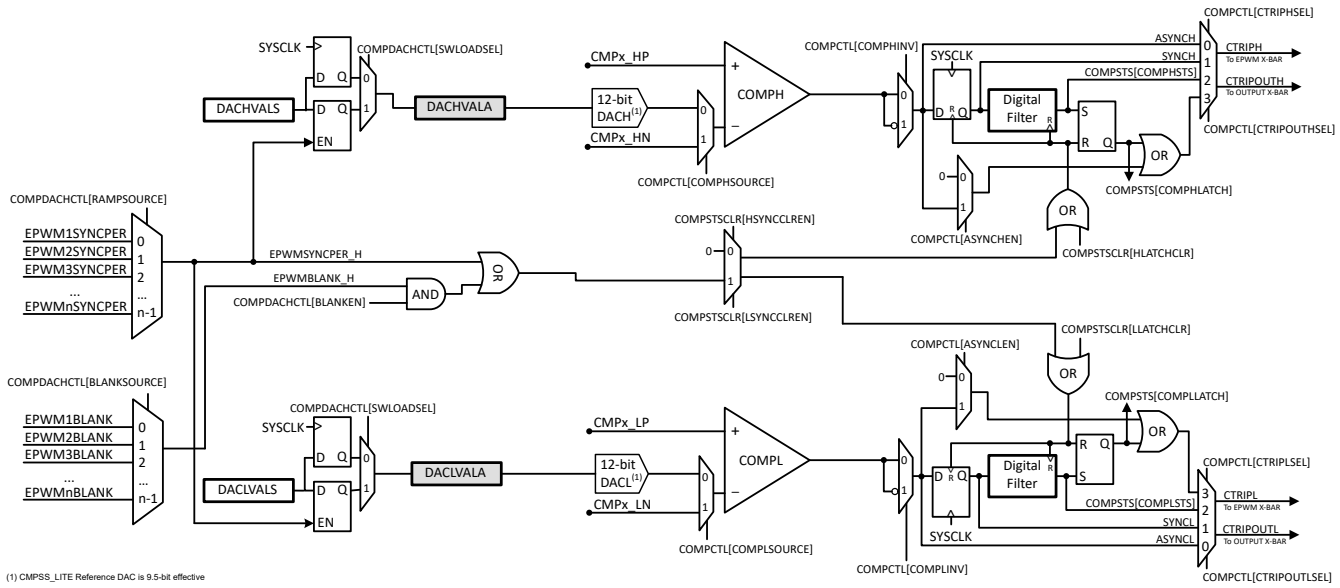


Figure 6-49. CMPSS_LITE Module Block Diagram

Each reference 12-bit DAC can be configured to drive a reference voltage into the negative input of the respective comparator. Some CMPSS instances also allow the low DAC output to be routed to a pin to act as an external DAC. In this case, all other CMPSS module functionality is not useable, including the high DAC, both comparators, ramp generation, and the digital filters. The reference 12-bit DAC is illustrated in Figure 6-50.

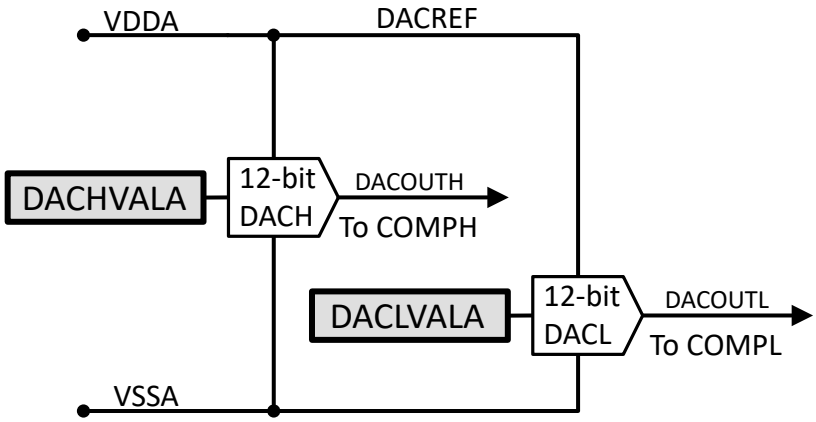


Figure 6-50. Reference DAC Block Diagram

6.12.5.5 CMPSS Electrical Data and Timing

6.12.5.5.1 CMPSS Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPU	Power-up time				500	µs
Comparator input (CMPINxx) range			0		VDDA	V
Input referred offset error		Low common mode, inverting input set to 50mV	–20		20	mV
Hysteresis[1]		1x	4	12	20	LSB
		2x	17	24	33	
		3x	25	36	50	
		4x	30	48	67	
Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR)		Step response		21	60	ns
		Ramp response (1.65V/µs)		26		
		Ramp response (8.25mV/µs)		30		ns
PSRR	Power Supply Rejection Ratio	Up to 250 kHz		46		dB
CMRR	Common Mode Rejection Ratio		40			dB

(1) The CMPSS DAC is used as the reference to determine how much hysteresis to apply. Therefore, hysteresis will scale with the CMPSS DAC reference voltage. Hysteresis is available for all comparator input source configurations.

6.12.5.5.2 CMPSS_LITE Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPU	Power-up time	Bandgap Not Enabled			500	µs
Comparator input (CMPINxx) range			0		VDDA	V
Input referred offset error		Via AIO/AGPIO, Input common mode = 5% to 95% of VDDA	–20		20	mV
Hysteresis[1]		1x	2	10	19	mV
		2x	8	20	34	
		3x	15	30	51	
		4x	20	41	70	
		5x	26	52	88	
		6x	32	64	109	
		7x	38	77	131	
Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR)		Step response		21	40	ns
		Ramp response (1.65V/µs)		26		
		Ramp response (8.25mV/µs)		30		
PSRR	Power Supply Rejection Ratio	Up to 250 kHz		46		dB
CMRR	Common Mode Rejection Ratio		40			dB

(1) Hysteresis is available for all comparator input source configurations.

CMPSS Comparator Input Referred Offset and Hysteresis

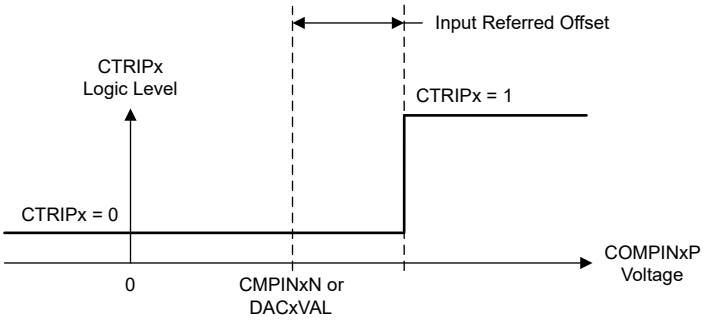


Figure 6-51. CMPSS Comparator Input Referred Offset

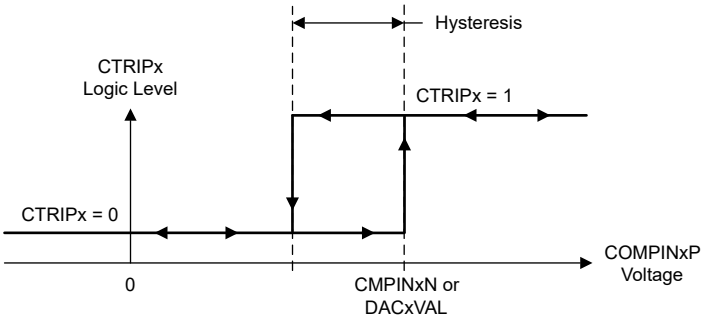


Figure 6-52. CMPSS Comparator Hysteresis

6.12.5.5.3 CMPSS DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMPSS DAC output range	Internal reference	0		VDDA	V
Static offset error(1)		–25		25	mV
Static gain error(1)		–2		2	% of FSR
Static DNL	Endpoint corrected	>–1		4	LSB
Static INL	Endpoint corrected	–16		16	LSB
Settling time	Settling to 1LSB after full-scale output change			1	µs
Resolution			12		bits
CMPSS DAC output disturbance(2)	Error induced by comparator trip or CMPSS DAC code change within the same CMPSS module	–100		100	LSB
CMPSS DAC disturbance time(2)				200	ns

(1) Includes comparator input referred errors.
(2) Disturbance error may be present on the CMPSS DAC output for a certain amount of time after a comparator trip.

6.12.5.5.4 CMPSS_LITE DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMPSS DAC output range		0		VDDA	V
Static offset error(1)		–25		25	mV
Static gain error(1)		–0.5		0.5	% of FSR
Static DNL	Endpoint corrected	–5		5	LSB (12-bit)
Static INL	Endpoint corrected	–7		7	LSB (12-bit)
Static TUE (Total Unadjusted Error)			35		mV
Settling time	Settling to 1LSB after full-scale output change		1		µs

6.12.5.5.4 CMPSS_LITE DAC Static Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution[2]			12		bits

(1) Includes comparator input referred errors.
(2) 9.5-bit effective resolution for monotonic response

6.12.5.5.5 CMPSS Illustrative Graphs

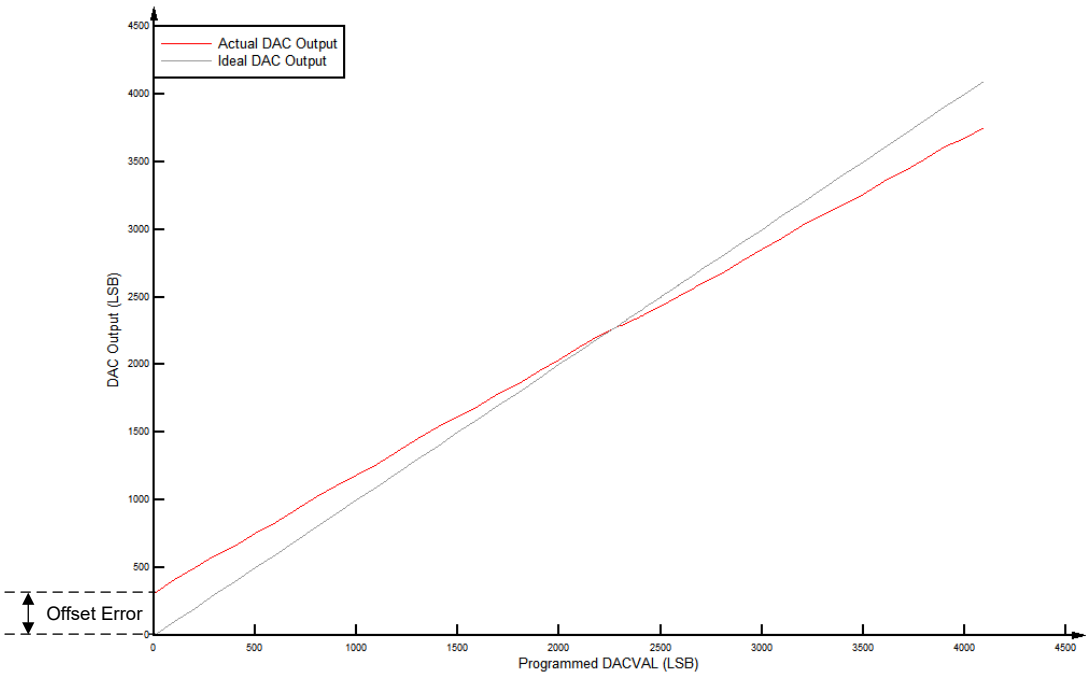


Figure 6-53. CMPSS DAC Static Offset

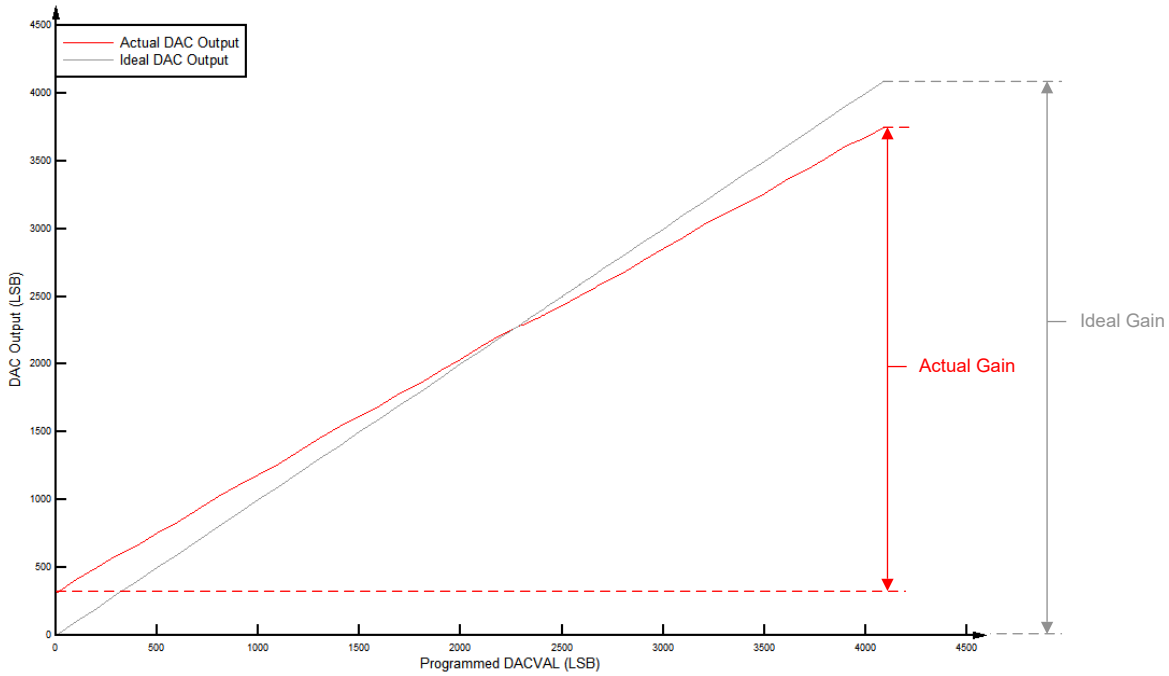


Figure 6-54. CMPSS DAC Static Gain

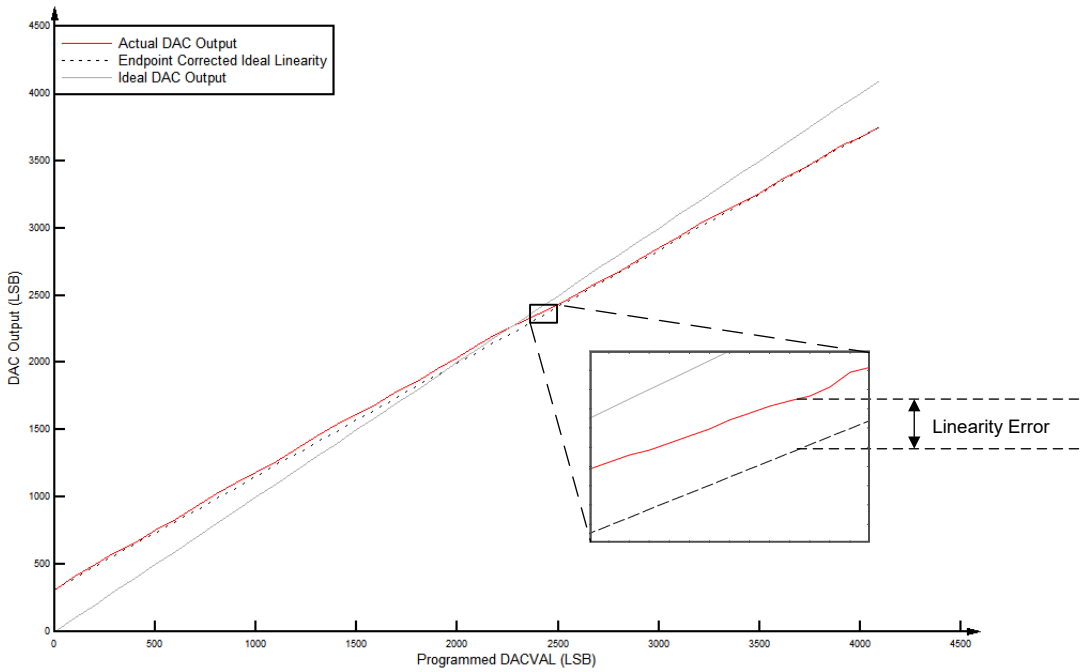


Figure 6-55. CMPSS DAC Static Linearity

6.12.5.5.6 CMPSS DAC Dynamic Error

When using the ramp generator to control the internal DAC, the step size can vary based on the application need. Since the step size of the DAC is less than a full scale transition, the settling time is improved from the electrical specification listed in the *CMPSS DAC Static Electrical Characteristics* table. The equation below and Figure 6-56 can give guidance on the expected voltage error from ideal based on different RAMPxDECVALA values.

$$DYNAMICERROR = (m \times RAMPxDECVALA) + b \quad (3)$$

Table 6-25. DAC Max Dynamic Error Terms

EQUATION PARAMETER	MIN (LSB)	MAX (LSB)
m	0.10	0.18
b	3.7	5.6

Note

Above error terms are based on the max SYSCLK of the target device. If operating below the max SYSCLK then the "m" error term should be scaled accordingly.

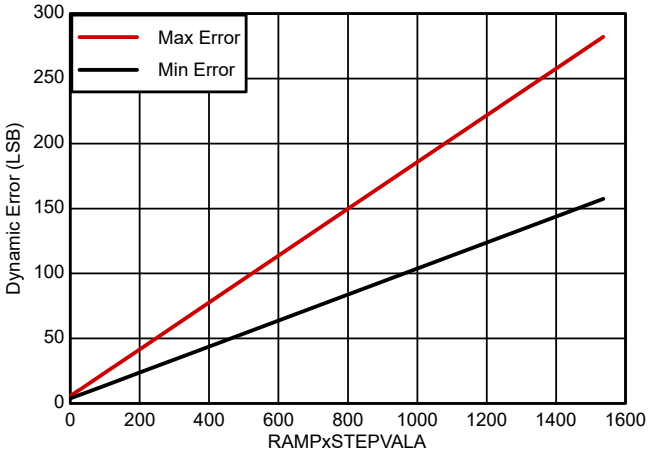


Figure 6-56. CMPSS DAC Dynamic Error

6.12.5.5.7 Buffered Output from CMPx_DACL Operating Conditions

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_L	Resistive Load(2)		5			kΩ
C_L	Capacitive Load				100	pF
V_{OUT}	Valid Output Voltage Range(3)	R_L = 5 kΩ	0.3		VDDA – 0.3	V
		R_L = 1 kΩ	0.6		VDDA – 0.6	V
Reference Voltage(4)		VREFHI	2.4	2.5 or 3.0	VDDA	V

(1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
(2) DAC can drive a minimum resistive load of 1 kΩ, but the output range will be limited.
(3) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
(4) For best PSRR performance, VREFHI should be less than VDDA.

6.12.5.5.8 Buffered Output from CMPx_DACL Electrical Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
Resolution(4)			12		bits
Load Regulation		–1		1	mV/V
Glitch Energy			1.5		V-ns
Voltage Output Settling Time Full-Scale	Settling to 2 LSBs after 0.3V-to-3V transition			2	µs

6.12.5.5.8 Buffered Output from CMPx_DACL Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Output Settling Time 1/4th Full-Scale		Settling to 2 LSBs after 0.3V-to-0.75V transition			1.6	µs
Voltage Output Slew Rate		Slew rate from 0.3V-to-3V transition	2.8		4.5	V/µs
Load Transient Settling Time		5-kΩ Load			328	ns
TPU	Power Up Time	Bandgap Not Enabled			500	µs
DC Characteristics						
Offset	Offset Error		–100		100	mV
Gain	Gain Error(2)		–1.5		1.5	% of FSR
DNL	Differential Non Linearity	Endpoint corrected	–2		2	LSB (12-bit)
INL	Integral Non Linearity	Endpoint corrected	–7		7	LSB (12-bit)
AC Characteristics						
Output Noise		Integrated noise from 100 Hz to 100 kHz		600		µVrms
		Noise density at 10 kHz		800		nVrms/√Hz
SNR	Signal to Noise Ratio	1 kHz, 200 KSPS		64		dB
THD	Total Harmonic Distortion	1 kHz, 200 KSPS		–64.2		dB
SFDR	Spurious Free Dynamic Range	1 kHz, 200 KSPS		66		dB
SINAD	Signal to Noise and Distortion Ratio	1 kHz, 200 KSPS		61.7		dB
PSRR	Power Supply Rejection Ratio(3)	DC		70		dB
		100 kHz		30		dB

(1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
(2) Gain error is calculated for linear output range.
(3) VREFHI = 3.2 V, VDDA = 3.3 V DC + 100 mV Sine.
(4) 11-bit effective (monotonic response).

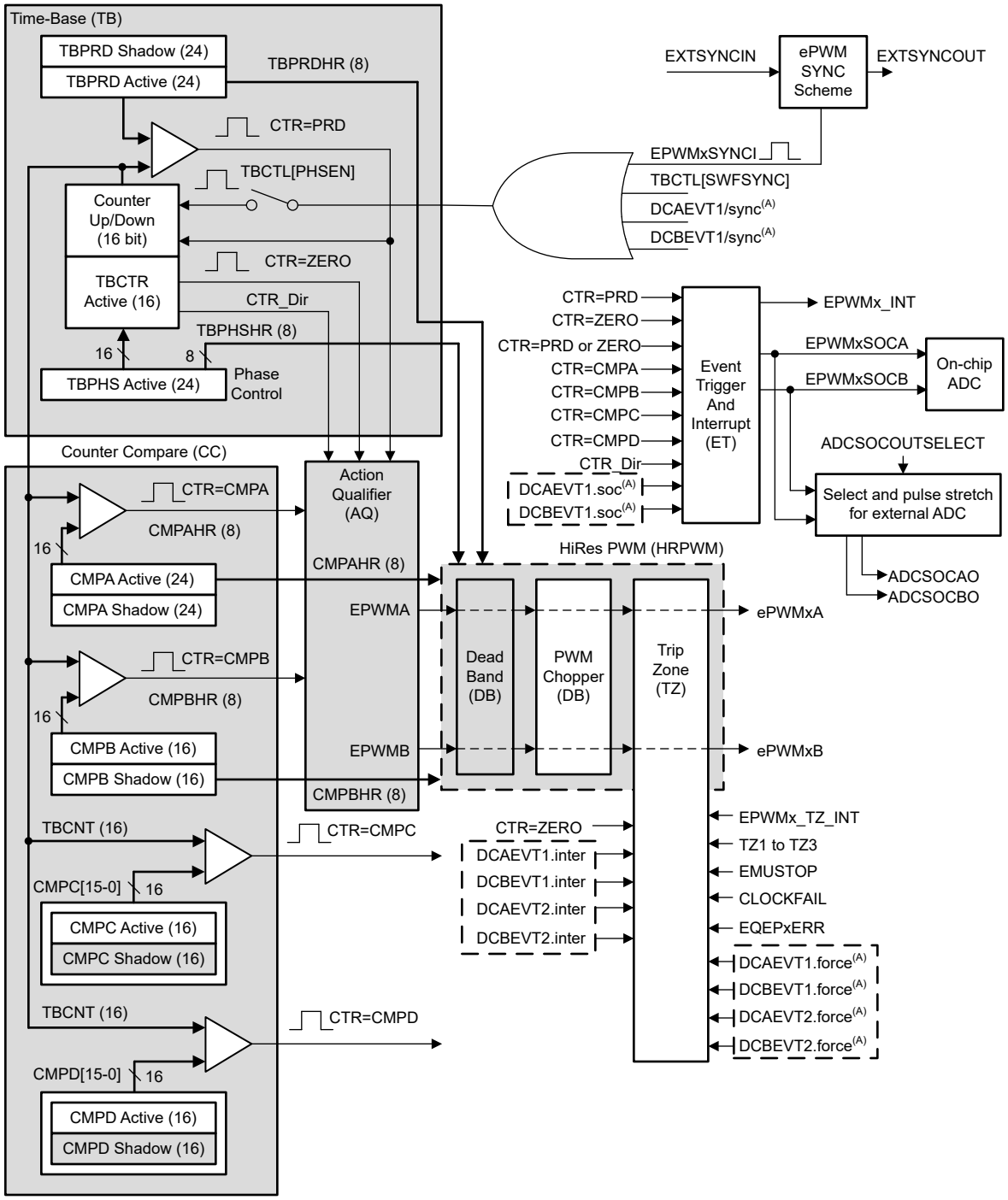
6.13 Control Peripherals

6.13.1 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules.

Figure 6-57 shows the ePWM module. Figure 6-58 shows the ePWM trip input connectivity.



A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

Figure 6-57. ePWM Submodules and Critical Internal Signal Interconnects

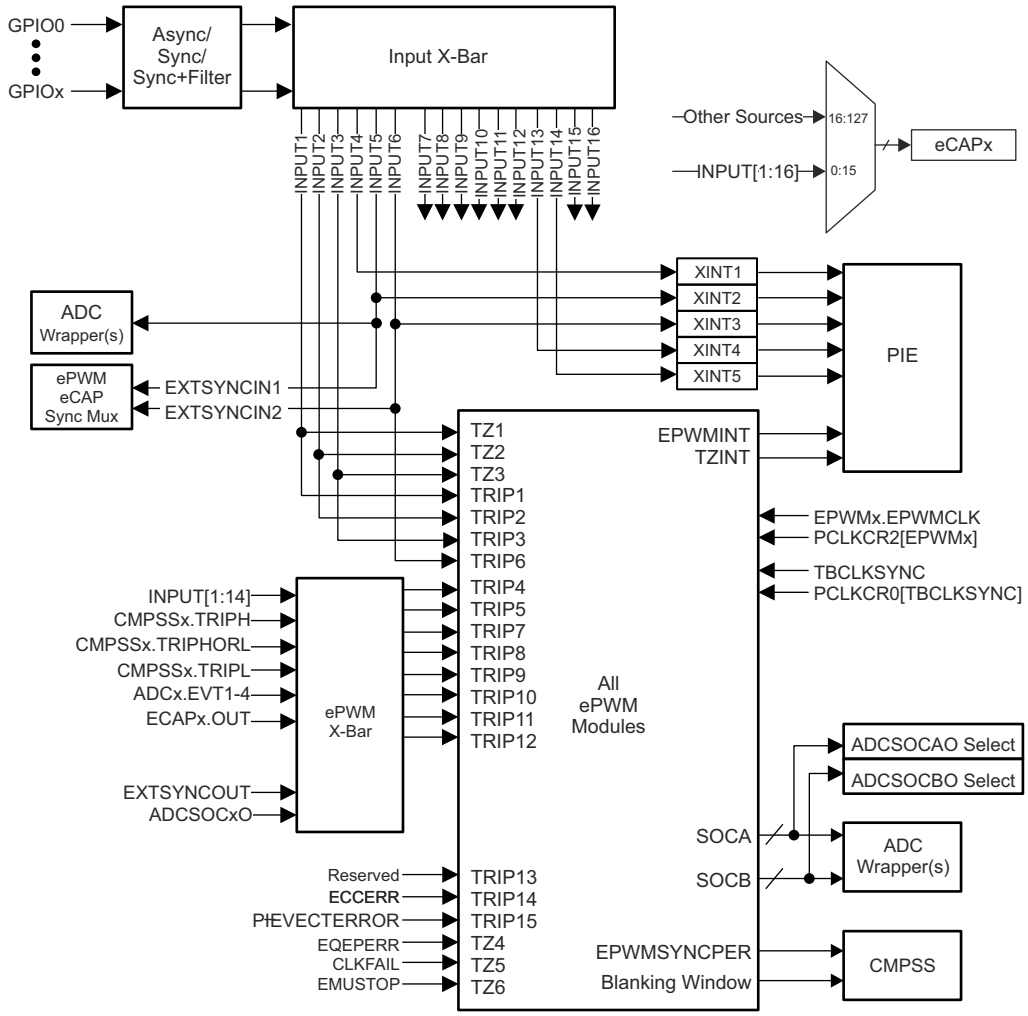


Figure 6-58. ePWM Trip Input Connectivity

6.13.1.1 Control Peripherals Synchronization

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules. Figure 6-59 shows the synchronization scheme.

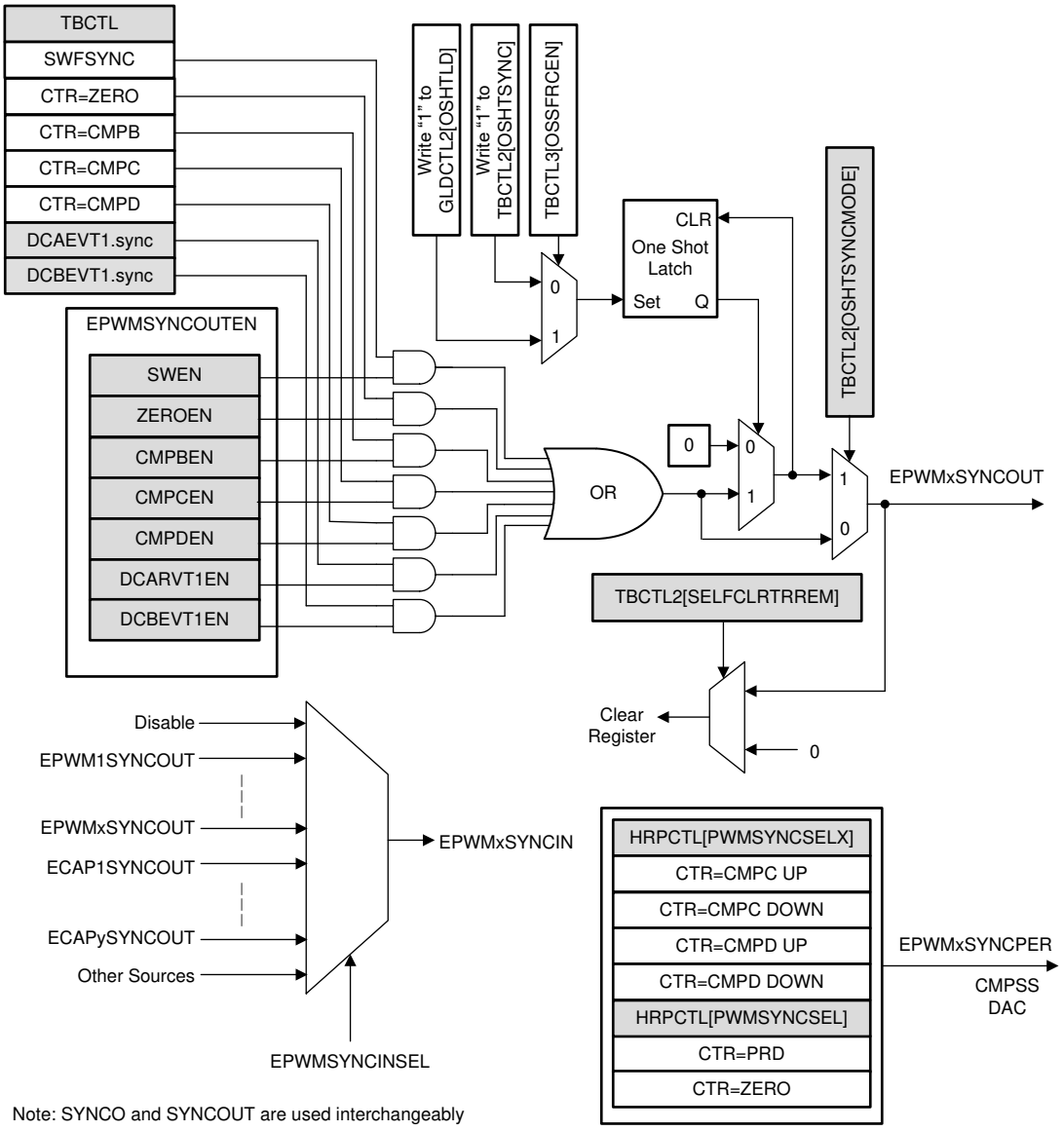


Figure 6-59. Synchronization Chain Architecture

6.13.1.2 ePWM Electrical Data and Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.13.1.2.1 ePWM Timing Requirements

			MIN	MAX	UNIT
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		

6.13.1.2.2 ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER[1]		MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low	20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width	$8t_{c(SYSCLK)}$		cycles
$t_{d(TZ-PWM)}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z		25	ns

(1) 20-pF load on pin.

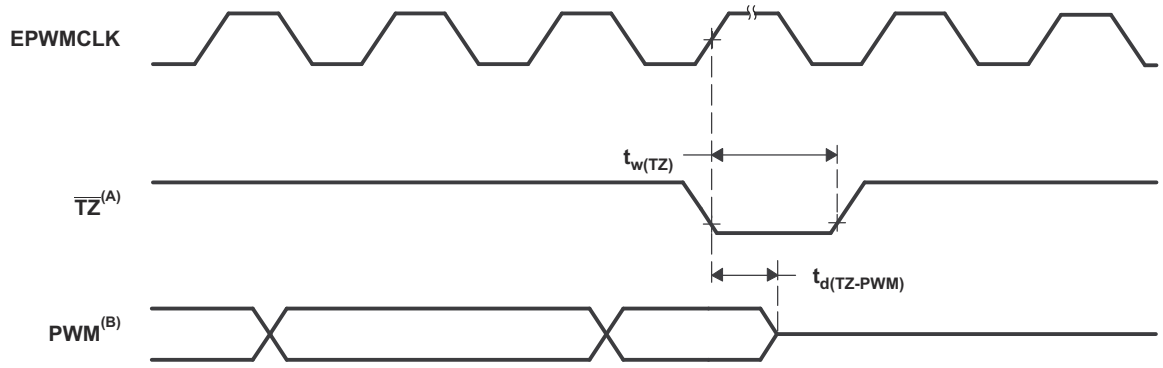
6.13.1.2.3 Trip-Zone Input Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.13.1.2.3.1 Trip-Zone Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZx}$ input low	Asynchronous	$1t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		cycles
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		cycles

6.13.1.2.3.2 PWM Hi-Z Characteristics Timing Diagram



A. $\overline{TZ}$: $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, TRIP1–TRIP12

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-60. PWM Hi-Z Characteristics

6.13.2 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period and deadband registers of the ePWM module.

6.13.2.1 HRPWM Electrical Data and Timing

6.13.2.1.1 High-Resolution PWM Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)		150	310	ps

(1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD}. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

6.13.3 External ADC Start-of-Conversion Electrical Data and Timing

6.13.3.1 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{ADCSOCxO}$ low	$32t_{c(SYSCLK)}$		cycles

6.13.3.2 $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing Diagram

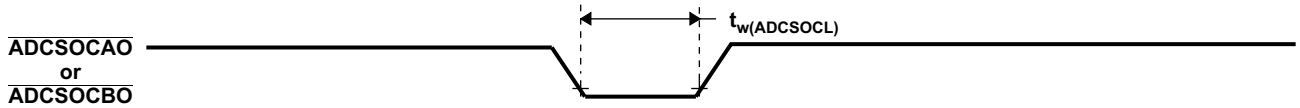


Figure 6-61. $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing

6.13.4 Enhanced Capture (eCAP)

The features of the eCAP module include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed by way of Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module features described in this chapter include:

- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single-shot capture of up to four event time-stamps
- Continuous mode capture of time stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output

The capture functionality of the Type 1 eCAP is enhanced from the Type 0 eCAP with the following added features:

- Event filter reset bit
  - Writing a 1 to ECCTL2[CTRFILTRESET] clears the event filter, the modulo counter, and any pending interrupts flags. Resetting the bit is useful for initialization and debug.
- Modulo counter status bits
  - The modulo counter (ECCTL2 [MODCNTRSTS]) indicates which capture register is loaded next. In the Type 0 eCAP, to know the current state of the modulo counter was not possible
- Input multiplexer
  - ECCTL0 [INPUTSEL] selects one of 128 input signals, which are detailed in the Configuring Device Pins for the eCAP section of the Enhanced Capture (eCAP) chapter in the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*.
- EALLOW protection
  - EALLOW protection was added to critical registers. To maintain software compatibility with Type-0, configure DEV_CFG_REGS.ECAPTYPE to make these registers unprotected.

The capture functionality of the Type 2 eCAP is enhanced from the Type 1 eCAP with the following added features:

- Added ECAPxSYNCINSEL register
  - ECAPxSYNCINSEL register is added for each eCAP to select an external SYNCIN. Every eCAP can have a separate SYNCIN signal.

6.13.4.1 eCAP Block Diagram

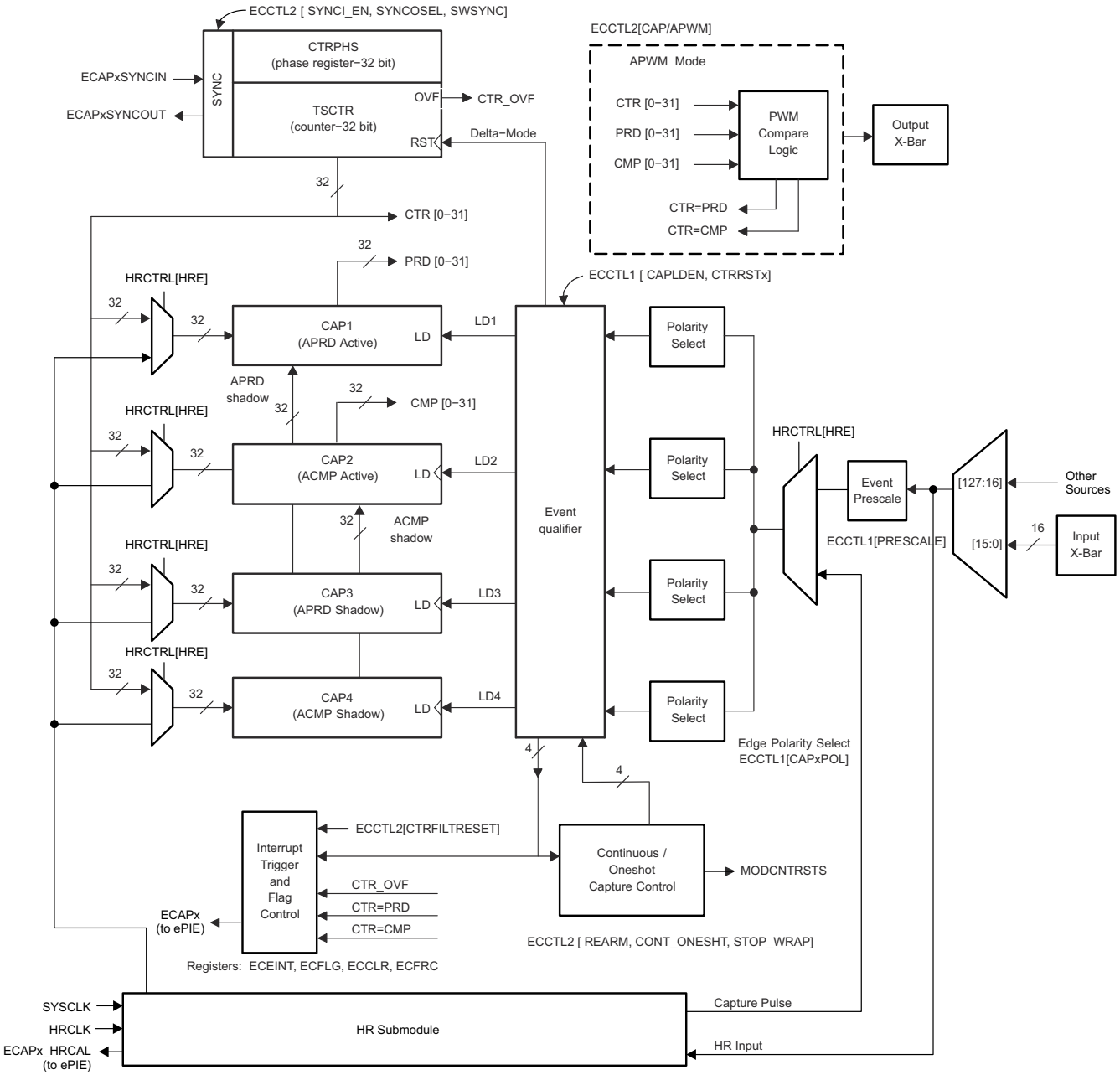


Figure 6-62. eCAP Block Diagram

6.13.4.2 eCAP Synchronization

The eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from EPWM, eCAP, or X-Bar. The SYNC signal is defined by the selection in the ECAPxSYNCINSEL[SEL] bit for ECAPx as shown in Figure 6-63.

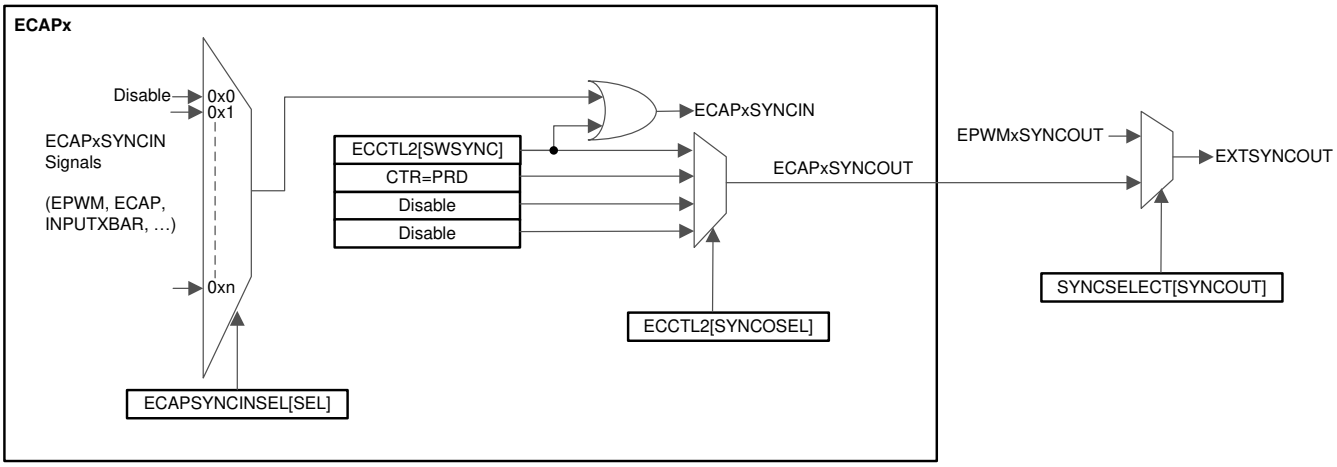


Figure 6-63. eCAP Synchronization Scheme

6.13.4.3 eCAP Electrical Data and Timing

6.13.4.3.1 eCAP Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SYSCLK)}$			ns
		Synchronous	$2t_{c(SYSCLK)}$			
		With input qualifier	$1t_{c(SYSCLK)} + t_{w\_(IQSW)}$			

6.13.4.3.2 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20			ns

6.13.5 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module on this device is Type-2. The eQEP interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position control systems.

The eQEP peripheral contains the following major functional units (see Figure 6-64):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)
- Quadrature Mode Adapter (QMA)

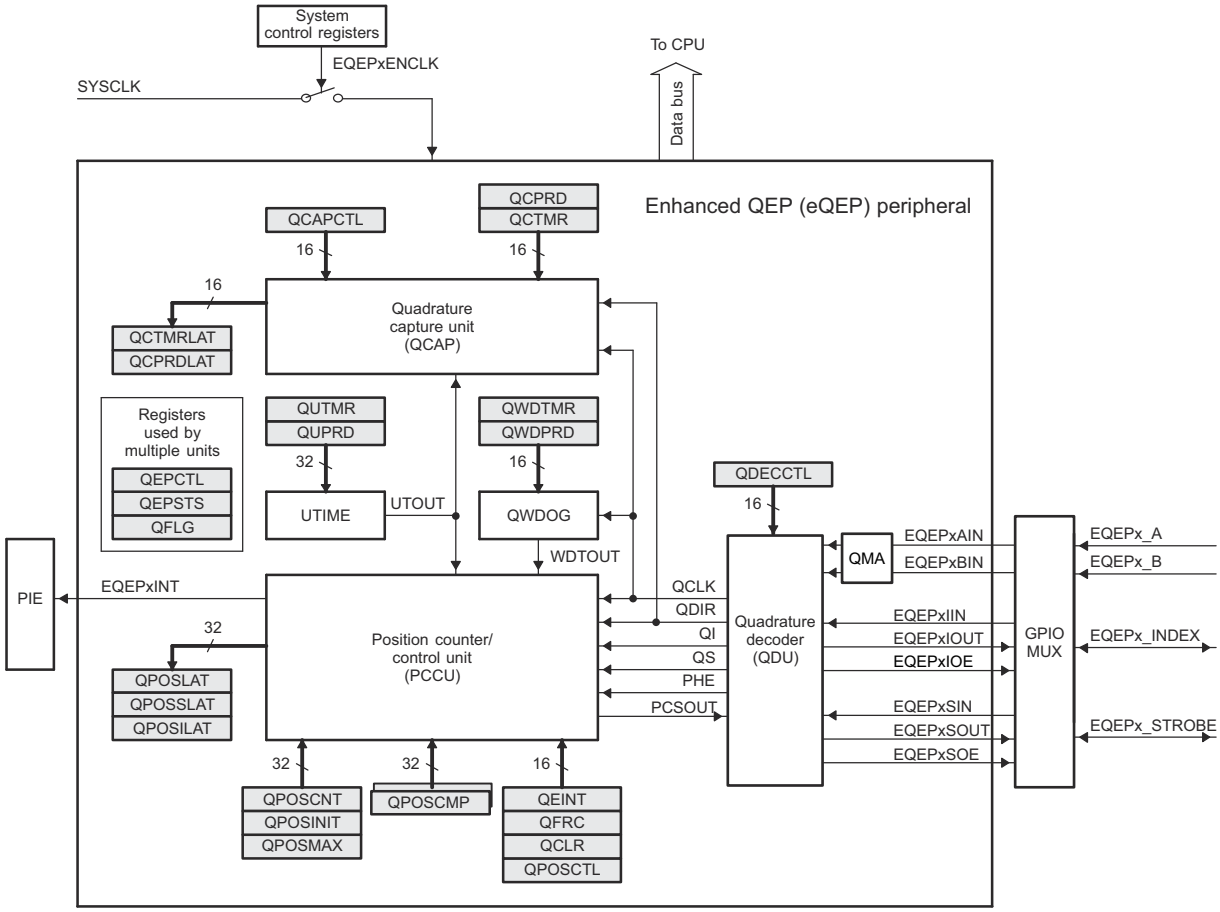


Figure 6-64. eQEP Block Diagram

6.13.5.1 eQEP Electrical Data and Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.13.5.1.1 eQEP Timing Requirements

			MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$		
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		

(1) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.

6.13.5.1.2 eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		$5t_{c(SYSCLK)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		$7t_{c(SYSCLK)}$	cycles

6.14 Communications Peripherals

6.14.1 Controller Area Network (CAN)

Note

The CAN module uses the IP known as *DCAN*. This document uses the names *CAN* and *DCAN* interchangeably to reference this peripheral.

The CAN module implements the following features:

- Complies with ISO11898-1 (Bosch® CAN protocol specification 2.0 A and B)
- Bit rates up to 1 Mbps
- Multiple clock sources
- 32 message objects (mailboxes), each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard (11-bit) or extended (29-bit) identifier
  - Supports programmable identifier receive mask
  - Supports data and remote frames
  - Holds 0 to 8 bytes of data
  - Parity-checked configuration and data RAM
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loopback modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after bus-off state by a programmable 32-bit timer
- Two interrupt lines

Note

For a CAN bit clock of 100 MHz, the smallest bit rate possible is 3.90625Kbps.

Note

The accuracy of the on-chip oscillator is in the INTOSC Characteristics table. Depending on parameters such as the CAN bit timing settings, bit rate, bus length, and propagation delay, the accuracy of this oscillator may not meet the requirements of the CAN protocol. In this situation, an external clock source must be used.

Figure 6-65 shows the CAN block diagram.

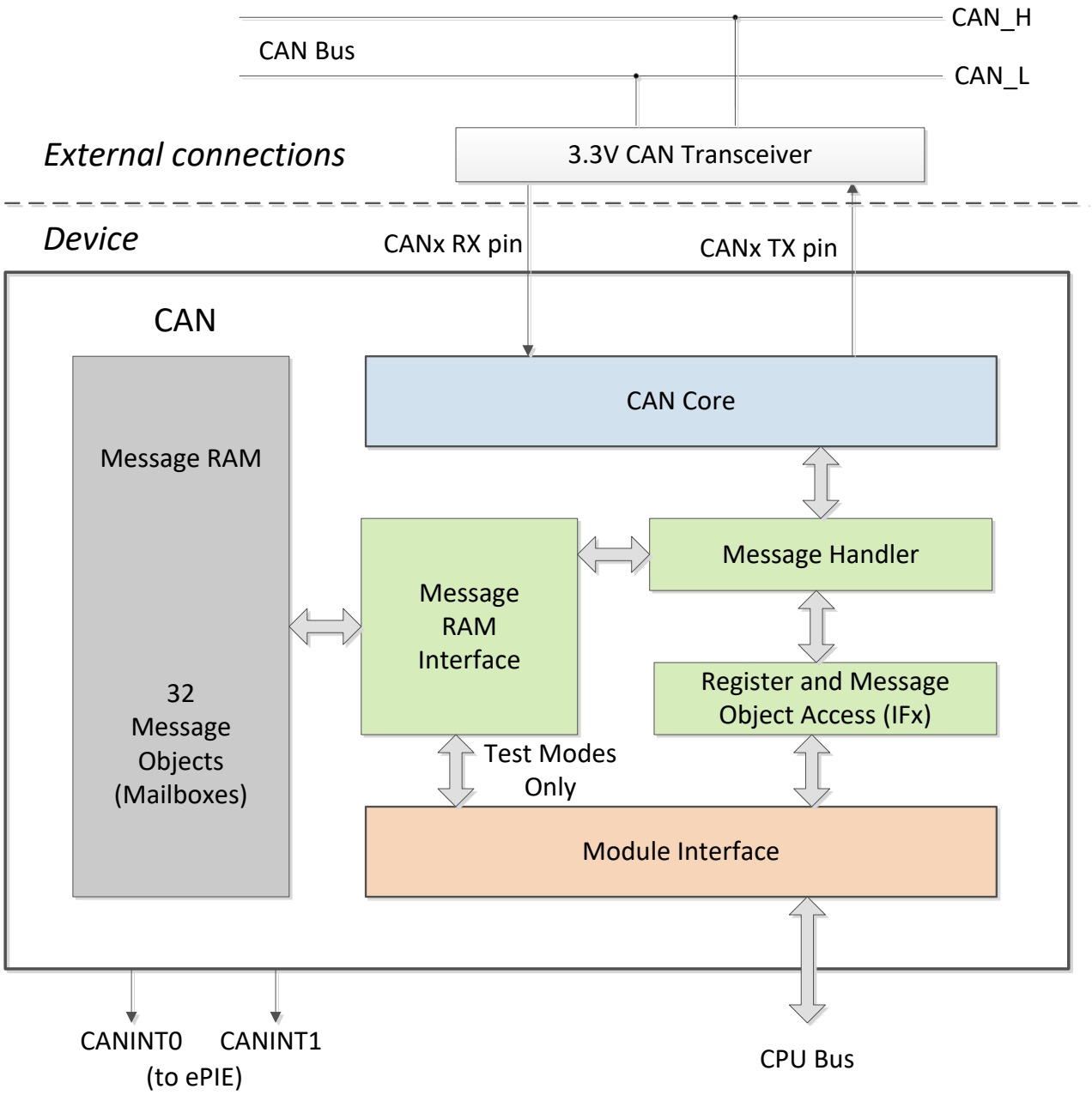


Figure 6-65. CAN Block Diagram

6.14.2 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the NXP Semiconductors I^2C-bus specification (version 2.1):
  - Support for 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate from 10Kbps up to 400Kbps (Fast-mode)
- Supports voltage thresholds compatible to:
  - SMBus 2.0 and below
  - PMBus 1.2 and below
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- Supports two ePIE interrupts
  - I2Cx interrupt – Any of the below conditions can be configured to generate an I2Cx interrupt:
    - Transmit Ready
    - Receive Ready
    - Register-Access Ready
    - No-Acknowledgment
    - Arbitration-Lost
    - Stop Condition Detected
    - Addressed-as-Slave
  - I2Cx_FIFO interrupts:
    - Transmit FIFO interrupt
    - Receive FIFO interrupt
- Module enable and disable capability
- Free data format mode

Figure 6-66 shows how the I2C peripheral module interfaces within the device.

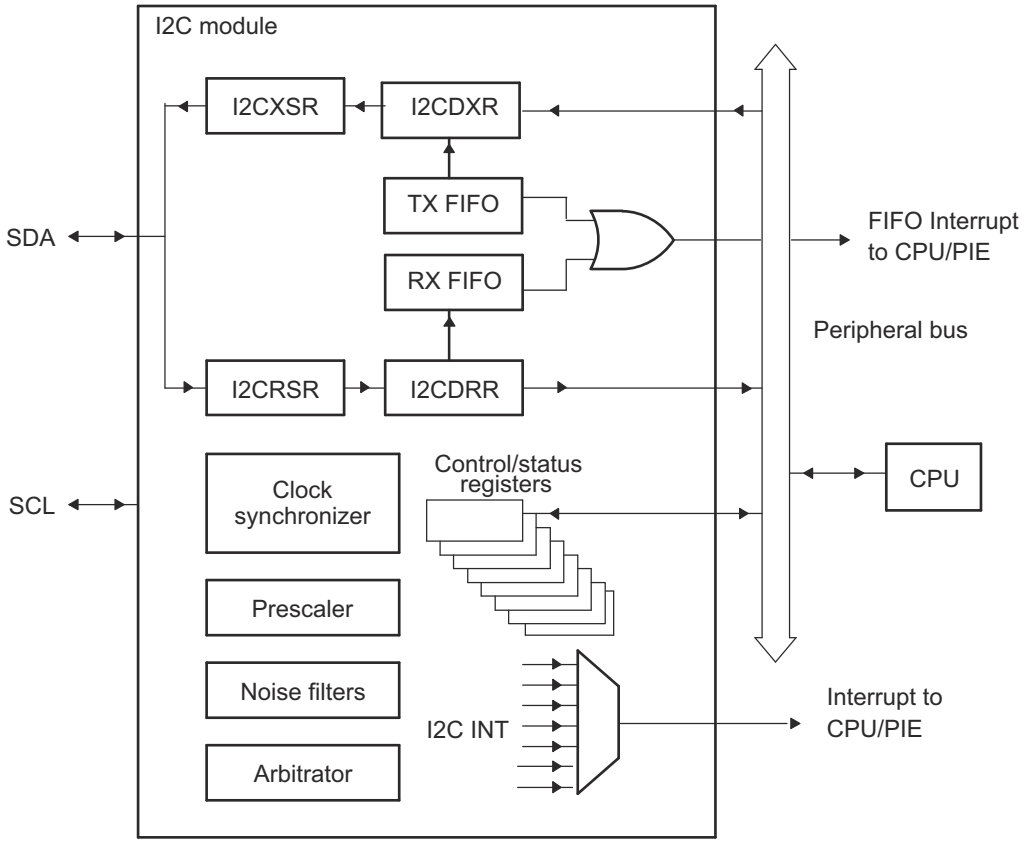


Figure 6-66. I2C Peripheral Module Interfaces

6.14.2.1 I2C Electrical Data and Timing

Note

To meet all of the I2C protocol timing specifications, the I2C module clock must be configured in the range from 7 MHz to 12 MHz.

A pullup resistor must be chosen to meet the I2C standard timings. In most circumstances, 2.2 kΩ of total bus resistance to VDDIO is sufficient. For evaluating pullup resistor values for a particular design, see the *I2C Bus Pullup Resistor Calculation* Application Report.

6.14.2.1.1 I2C Timing Requirements

NO.			MIN	MAX	UNIT
Standard mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	4.0		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	4.0		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	250 (2)		ns
T5	$t_{r(SDA)}$	Rise time, SDA		1000 (1)	ns
T6	$t_{r(SCL)}$	Rise time, SCL		1000 (1)	ns
T7	$t_{f(SDA)}$	Fall time, SDA		300	ns
T8	$t_{f(SCL)}$	Fall time, SCL		300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	4.0		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF
Fast mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	0.6		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	0.6		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	100		ns
T5	$t_{r(SDA)}$	Rise time, SDA	20	300	ns
T6	$t_{r(SCL)}$	Rise time, SCL	20	300	ns
T7	$t_{f(SDA)}$	Fall time, SDA	11.4	300	ns
T8	$t_{f(SCL)}$	Fall time, SCL	11.4	300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	0.6		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF

(1) In order to minimize the rise time, TI recommends using a strong pullup on both the SDA and SCL bus lines on the order of 2.2-kΩ net pullup resistance. It is also recommended that the value of the pullup resistance used on both SCL and SDA pins be matched.
(2) The C2000 I2C is a Fast-mode device. There is a limitation when using the I2C as a target transmitter with a standard mode host. For more information, see the *TMS320F280013x Real-Time MCUs Silicon Errata*.

6.14.2.1.2 I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Standard mode						
S1	f_{SCL}	SCL clock frequency		0	100	kHz
S2	T_{SCL}	SCL clock period		10		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		4.7		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		4.0		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		4.7		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			3.45	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			3.45	µs
S8	I_I	Input current on pins	$0.1\ V_{bus} < V_i < 0.9\ V_{bus}$	–10	10	µA
Fast mode						
S1	f_{SCL}	SCL clock frequency		0	400	kHz
S2	T_{SCL}	SCL clock period		2.5		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		1.3		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		0.6		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		1.3		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			0.9	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			0.9	µs
S8	I_I	Input current on pins	$0.1\ V_{bus} < V_i < 0.9\ V_{bus}$	–10	10	µA

6.14.2.1.3 I2C Timing Diagram

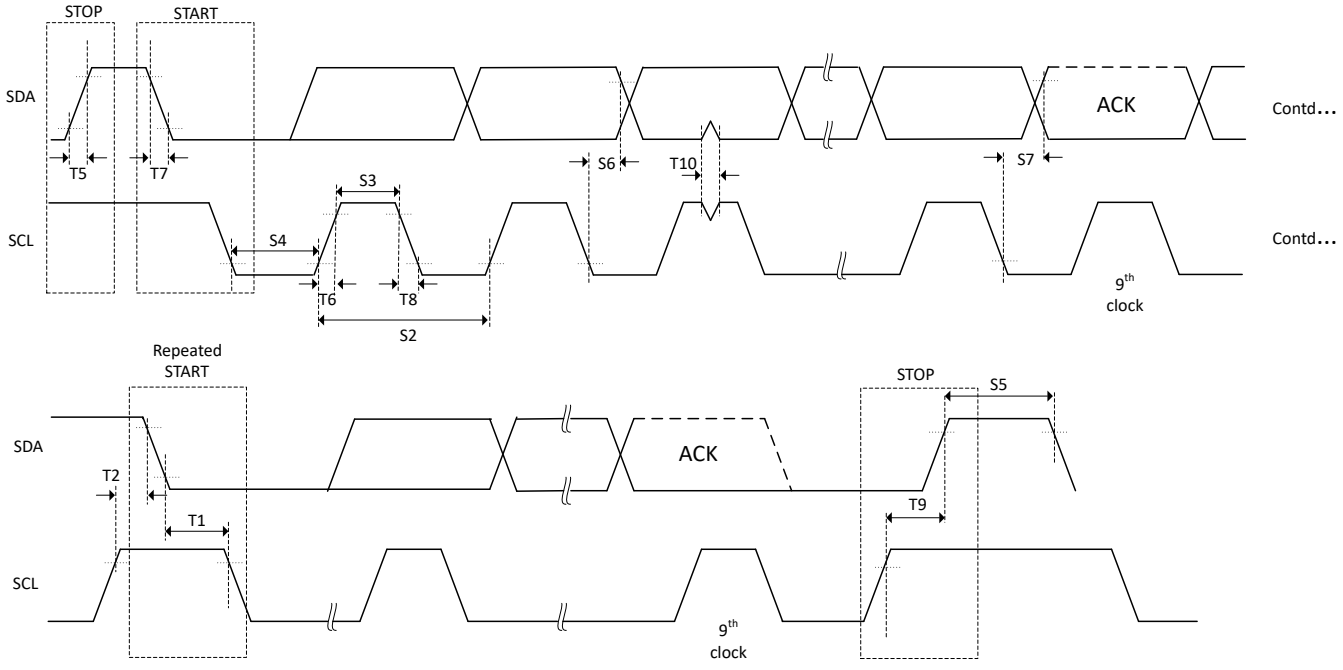


Figure 6-67. I2C Timing Diagram

6.14.3 Serial Communications Interface (SCI)

The SCI is a 2-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register.

Features of the SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin
  - Baud rate programmable to 64K different rates
- Data-word format
  - 1 start bit
  - Data-word length programmable from 1 to 8 bits
  - Optional even/odd/no parity bit
  - 1 or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

Note

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

Figure 6-68 shows the SCI block diagram.

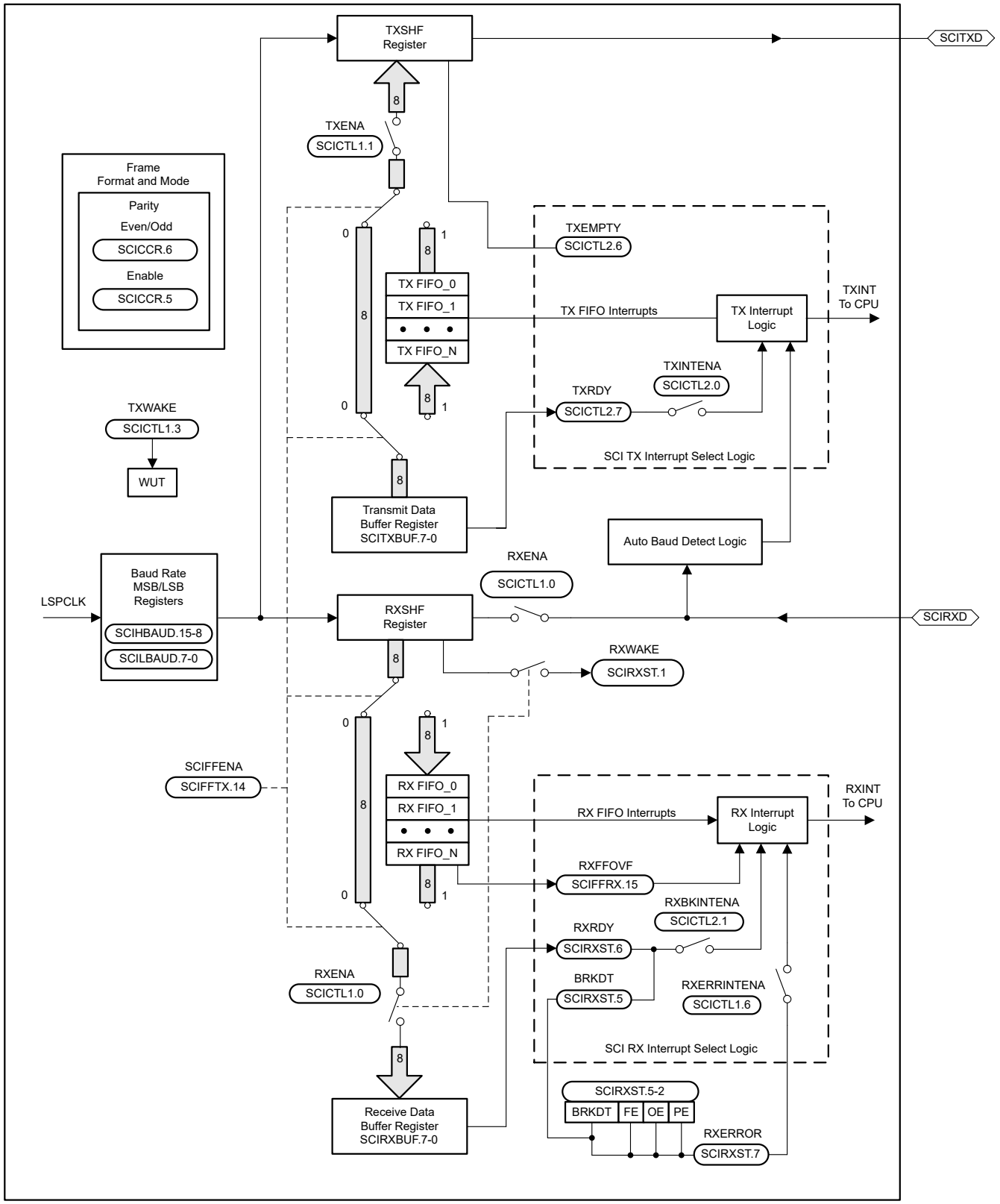


Figure 6-68. SCI Block Diagram

6.14.4 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input and output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the MCU controller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and analog-to-digital converters (ADCs). Multidevice communications are supported by the master or slave operation of the SPI. The port supports a 16-level, receive and transmit FIFO for reducing CPU servicing overhead.

The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: Master and Slave
- Baud rate: 125 different programmable rates. The maximum baud rate that can be employed is limited by the maximum speed of the I/O buffers used on the SPI pins.
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithm
- 16-level transmit/receive FIFO
- High-speed mode
- Delayed transmit control
- 3-wire SPI mode
- $\overline{\text{SPISTE}}$ inversion for digital audio interface receive mode on devices with two SPI modules

Figure 6-69 shows the SPI CPU interfaces.

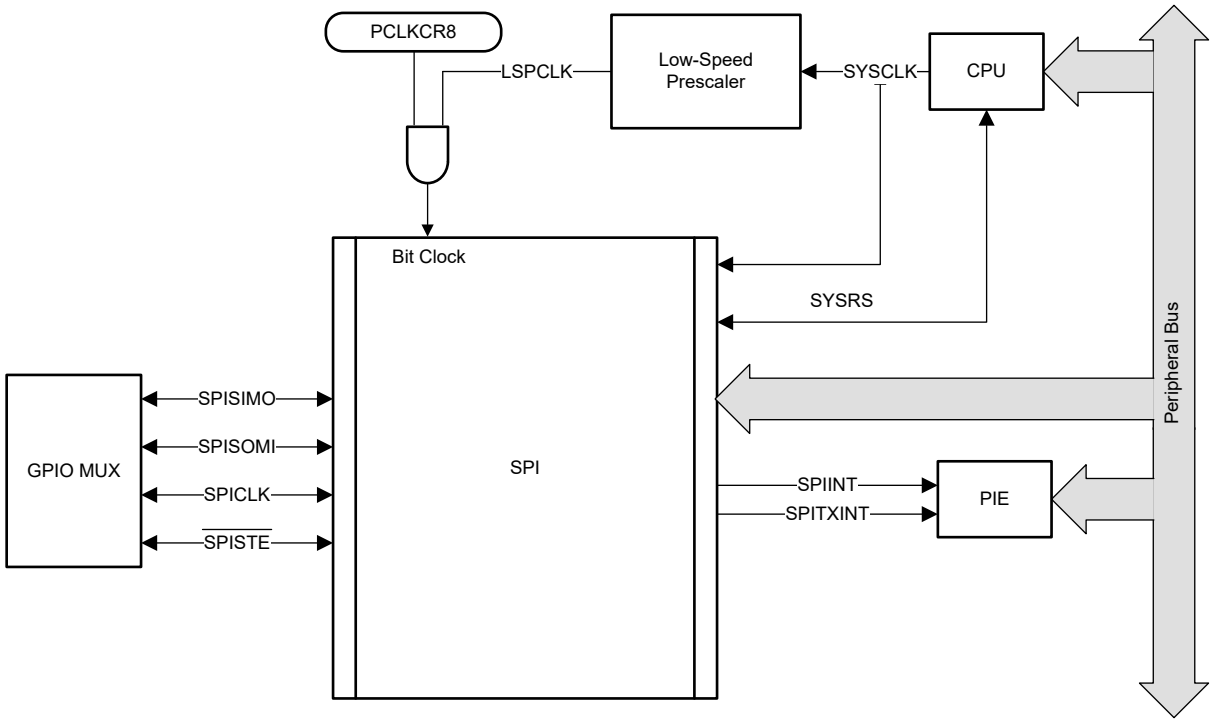


Figure 6-69. SPI CPU Interface

6.14.4.1 SPI Master Mode Timings

The following section contains the SPI Master Mode Timings. For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*.

Note

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPISIMO, and SPISOMI.

6.14.4.1.1 SPI Master Mode Timing Requirements

NO.			(BRR + 1) [1]	MIN	MAX	UNIT
High-Speed Mode						
8	$t_{su(SOMI)M}$	Setup time, SPISOMI valid before SPICLK	Even, Odd	1		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	Even, Odd	6.5		ns
Normal Mode						
8	$t_{su(SOMI)M}$	Setup time, SPISOMI valid before SPICLK	Even, Odd	15		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	Even, Odd	0		ns

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

6.14.4.1.2 SPI Master Mode Switching Characteristics - Clock Phase 0

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER[1] [2]		(BRR + 1)[3]	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{SPISTE}$ active to SPICLK	Even	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$	ns
			Odd	$1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} - 3$	$1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} + 3$	
24	$t_{v(STE)M}$	Valid time, SPICLK to $\overline{SPISTE}$ inactive	Even	$0.5t_{c(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$	
High-Speed Mode						
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid	Even, Odd		1	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		
Normal Mode						
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid	Even, Odd		2	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	0.5tc(SPC)M – 0.5tc(LSPCLK) – 3		

(1) 10-pF load on pin for High-Speed Mode.
(2) 20-pF load on pin for Normal Mode.
(3) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

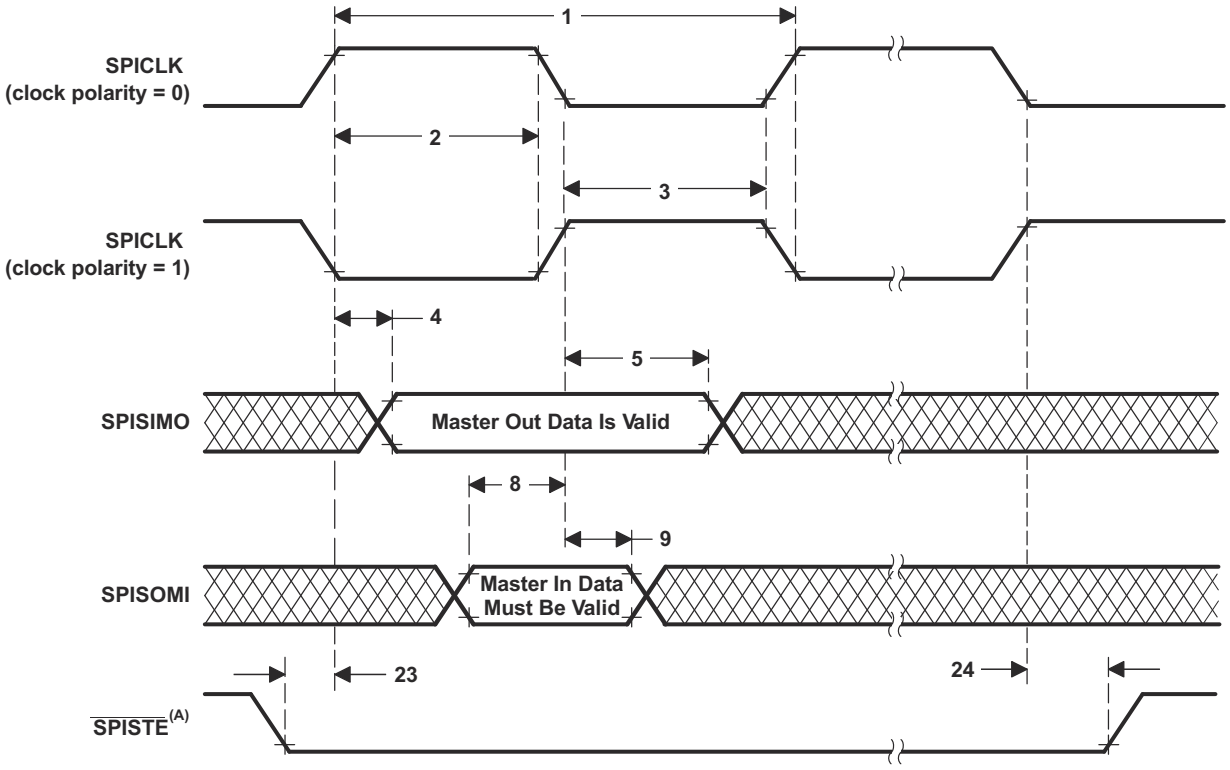
6.14.4.1.3 SPI Master Mode Switching Characteristics - Clock Phase 1

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER[1] [2]		(BRR + 1)	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{SPISTE}$ valid to SPICLK	Even, Odd	$2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$	$2t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$	ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{SPISTE}$ invalid	Even	–3	3	ns
			Odd	–3	3	
High-Speed Mode						
4	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 2$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 2$		
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		
Normal Mode						
4	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 2$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 2$		
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		

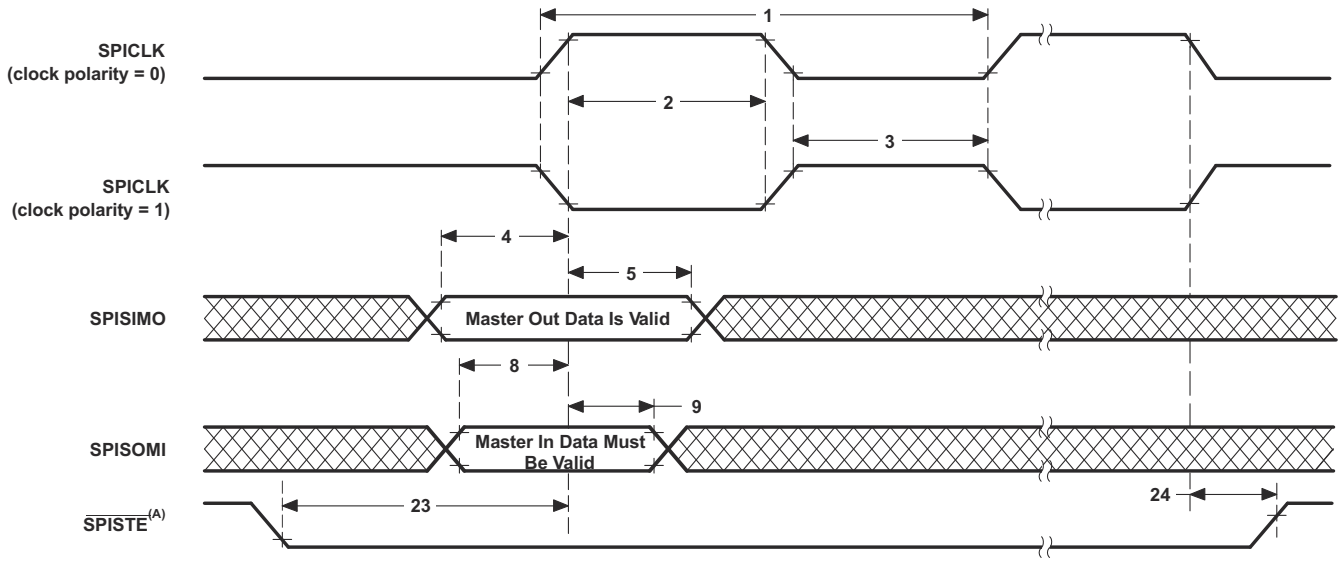
(1) 10-pF load on pin for High-Speed Mode.
(2) 20-pF load on pin for Normal Mode.

6.14.4.1.4 SPI Master Mode Timing Diagrams



A. On the trailing end of the word, SPISTE will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-70. SPI Master Mode External Timing (Clock Phase = 0)



A. On the trailing end of the word, SPISTE will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-71. SPI Master Mode External Timing (Clock Phase = 1)

6.14.4.2 SPI Slave Mode Timings

The following section contains the SPI Slave Mode Timings. For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*.

6.14.4.2.1 SPI Slave Mode Timing Requirements

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK, first pulse	$2t_{c(SYSCLK)} – 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, second pulse	$2t_{c(SYSCLK)} – 1$		ns
19	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(SIMO)S}$	Hold time, SPISIMO valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK (Clock Phase = 0)	$2t_{c(SYSCLK)} + 15$		ns
		Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK (Clock Phase = 1)	$2t_{c(SYSCLK)} + 15$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK	$1.5t_{c(SYSCLK)}$		ns

6.14.4.2.2 SPI Slave Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER(1)		MIN	MAX	UNIT
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		12.5	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI valid after SPICLK	0		ns

(1) 20-pF load on pin.

6.14.4.2.3 SPI Slave Mode Timing Diagrams

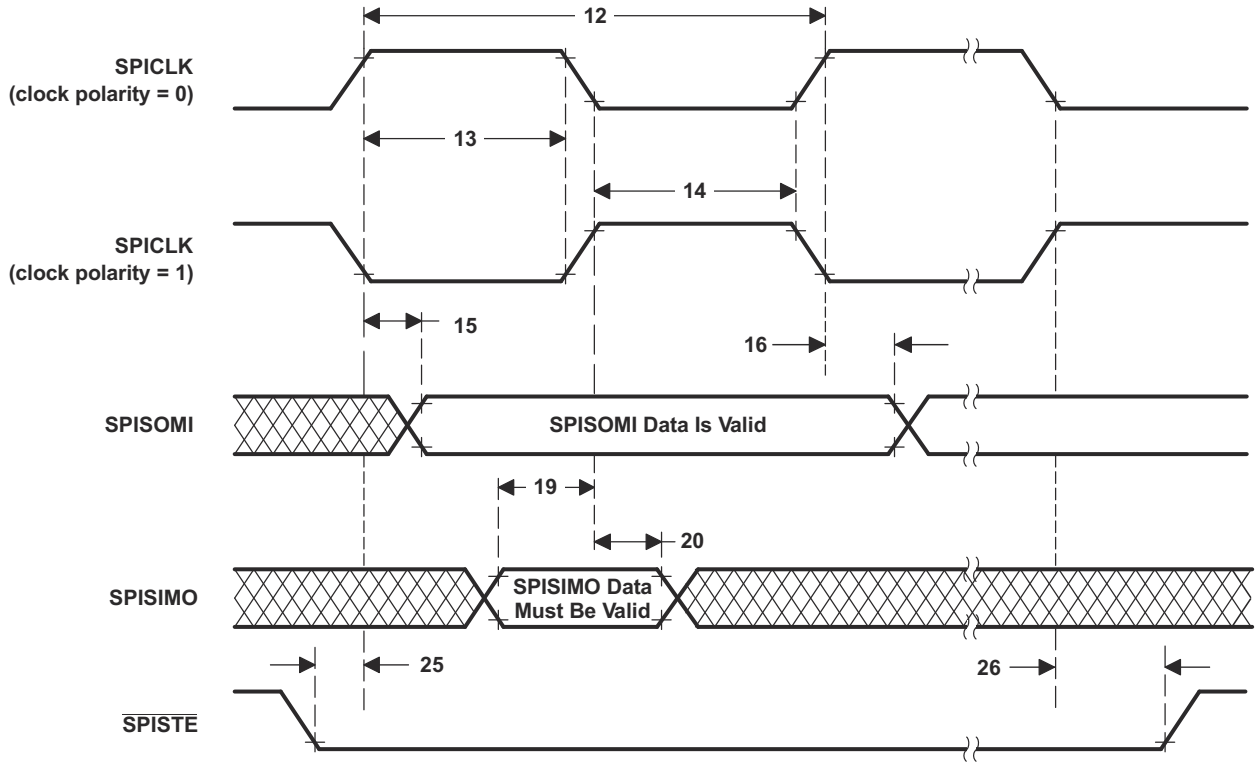


Figure 6-72. SPI Slave Mode External Timing (Clock Phase = 0)

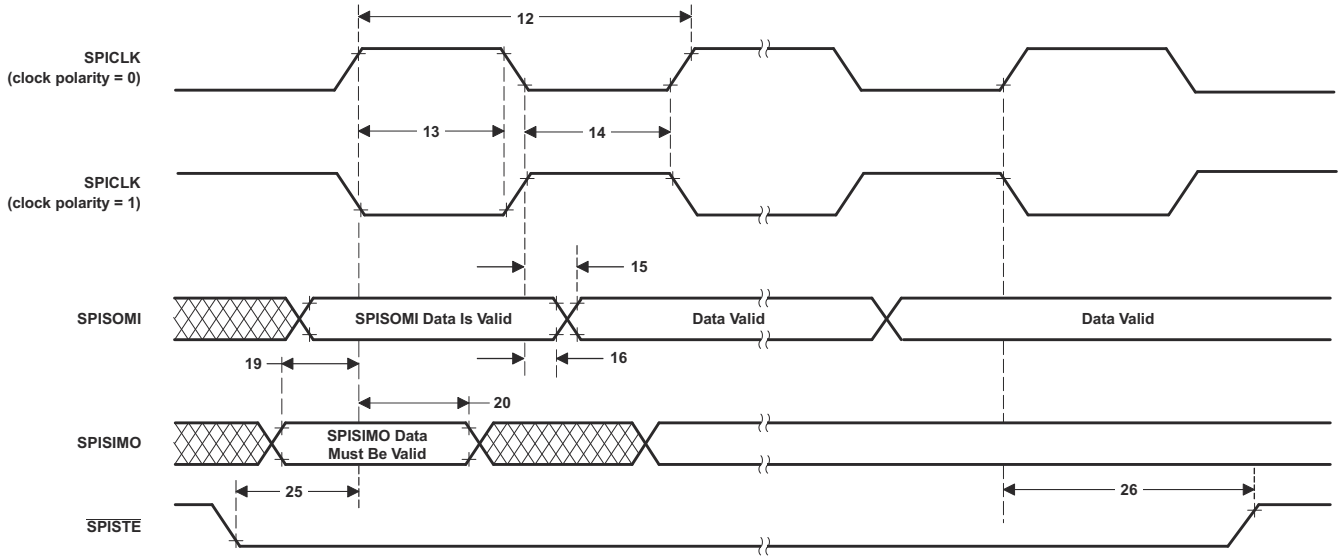


Figure 6-73. SPI Slave Mode External Timing (Clock Phase = 1)

7 Detailed Description

7.1 Overview

The TMS320F280013x (F280013x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics.

The real-time control subsystem is based on TI's 32-bit C28x DSP core, which provides 120 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the Trigonometric Math Unit (TMU), speeding up common algorithms key to real-time control systems.

The F280013x supports up to 256KB (128KW) of flash memory. Up to 36KB (18KW) of on-chip SRAM is also available to supplement the flash memory.

High-performance analog blocks are integrated into the F280013x real-time microcontroller (MCU) and are closely coupled with the processing and PWM units to provide optimal real-time signal chain performance. Fourteen PWM channels enable control of various power stages from a 3-phase inverter to power-factor correction and other advanced multilevel power topologies.

Interfacing is supported through various industry-standard communication ports (such as SPI, SCI, I2C, and CAN) and offers multiple pin-muxing options for optimal signal placement.

Want to learn more about features that make C2000 MCUs the right choice for your real-time control system? Check out *The Essential Guide for Developing With C2000™ Real-Time Microcontrollers* and visit the C2000™ real-time control MCUs page.

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the TMDSCNCD2800137 evaluation board and download C2000Ware.

7.2 Functional Block Diagram

The Functional Block Diagram shows the CPU system and associated peripherals.

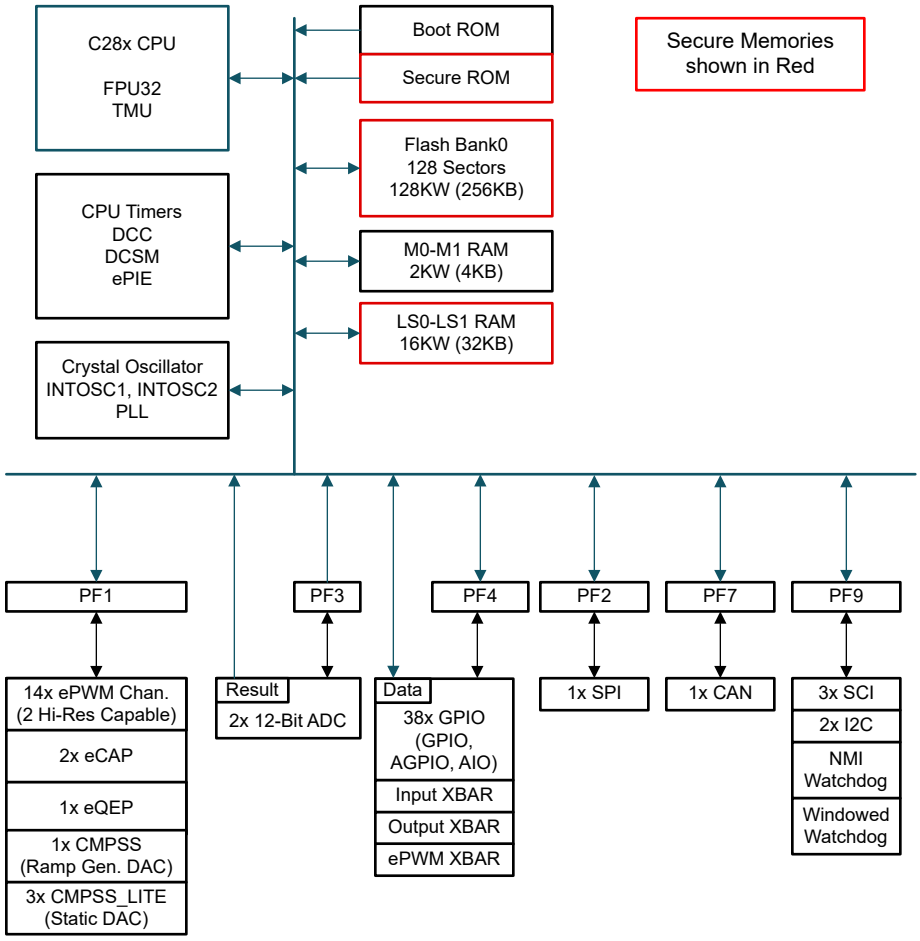


Figure 7-1. Functional Block Diagram

7.3 Memory

7.3.1 Memory Map

Table 7-1. Memory Map

MEMORY	SIZE	START ADDRESS	END ADDRESS	ECC/ PARITY	ACCESS PROTECTION	SECURITY
M0 RAM	1K x 16	0x0000 0000	0x0000 03FF	ECC	Yes	-
M1 RAM	1K x 16	0x0000 0400	0x0000 07FF	ECC	Yes	-
PieVectTable	256 x 16	0x0000 0D00	0x0000 0DFF	-	-	-
LS0 RAM	8K x 16	0x0000 8000	0x0000 9FFF	Parity	Yes	Yes
LS1 RAM	8K x 16	0x0000 A000	0x0000 BFFF	Parity	Yes	Yes
TI OTP [1]	1.5K x 16	0x0007 1000	0x0007 15FF	ECC	-	Yes [2]
User OTP	1K x 16	0x0007 8000	0x0007 83FF	ECC	-	Yes [2]
Flash	128K x 16	0x0008 0000	0x0009 FFFF	ECC	-	Yes
Boot ROM	32K x 16	0x003F 8000	0x003F FFFF	Parity	-	-
Pie Vector Fetch Error (part of Boot ROM)	1 x 16	0x003F FFBE	0x003F FFBF	Parity	-	-
Default Vectors (part of Boot ROM)	64 x 16	0x003F FFC0	0x003F FFFF	Parity	-	-

(1) TI OTP is for TI internal use only.
(2) Only a subset is secure.

7.3.1.1 Dedicated RAM (Mx RAM)

The CPU subsystem has two dedicated ECC-capable RAM blocks: M0 and M1. These memories are small nonsecure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them).

7.3.1.2 Local Shared RAM (LSx RAM)

Local shared RAMs (LSx RAMs) are accessible to the CPU. All LSx RAM blocks have Parity. These memories are secure and have CPU access protection (CPU write/CPU fetch).

7.3.2 Flash Memory Map

On the F280013x devices, one flash bank (256KB [128KW]) is available. Code to program the flash should be executed out of RAM, there should not be any kind of access to the flash bank when an erase or program operation is in progress.

Table 7-2. Flash Memory Map

PART NUMBER	SECTOR	ADDRESS			ECC ADDRESS		
		SIZE	START	END	SIZE	START	END
OTP Sectors							
ALL	TI OTP Bank 0 (Unsecure)	1520 x 16	0x0007 1000	0x0007 15EF	128 x 16	0x0107 0200	0x0107 02BD
	TI OTP Bank 0 (Secure)	16 x 16	0x0007 15F0	0x0007 15FF	128 x 16	0x0107 02BE	0x0107 02BF
	User configurable DCSM OTP Bank 0	1K x 16	0x0007 8000	0x0007 83FF	128 x 16	0x0107 1000	0x0107 107F
Bank 0 Sectors							
ALL	Sector 0	1K x 16	0x0008 0000	0x0008 03FF	128 x 16	0x0108 0000	0x0108 007F
	Sector 1	1K x 16	0x0008 0400	0x0008 07FF	128 x 16	0x0108 0080	0x0108 00FF
	Sector 2	1K x 16	0x0008 0800	0x0008 0BFF	128 x 16	0x0108 0100	0x0108 017F
	Sector 3	1K x 16	0x0008 0C00	0x0008 0FFF	128 x 16	0x0108 0180	0x0108 01FF
	Sector 4	1K x 16	0x0008 1000	0x0008 13FF	128 x 16	0x0108 0200	0x0108 027F
	Sector 5	1K x 16	0x0008 1400	0x0008 17FF	128 x 16	0x0108 0280	0x0108 02FF
	Sector 6	1K x 16	0x0008 1800	0x0008 1BFF	128 x 16	0x0108 0300	0x0108 037F
	Sector 7	1K x 16	0x0008 1C00	0x0008 1FFF	128 x 16	0x0108 0380	0x0108 03FF
	Sector 8	1K x 16	0x0008 2000	0x0008 23FF	128 x 16	0x0108 0400	0x0108 047F
	Sector 9	1K x 16	0x0008 2400	0x0008 27FF	128 x 16	0x0108 0480	0x0108 04FF
	Sector 10	1K x 16	0x0008 2800	0x0008 2BFF	128 x 16	0x0108 0500	0x0108 057F
	Sector 11	1K x 16	0x0008 2C00	0x0008 2FFF	128 x 16	0x0108 0580	0x0108 05FF
	Sector 12	1K x 16	0x0008 3000	0x0008 33FF	128 x 16	0x0108 0600	0x0108 067F
	Sector 13	1K x 16	0x0008 3400	0x0008 37FF	128 x 16	0x0108 0680	0x0108 06FF
	Sector 14	1K x 16	0x0008 3800	0x0008 3BFF	128 x 16	0x0108 0700	0x0108 077F
	Sector 15	1K x 16	0x0008 3C00	0x0008 3FFF	128 x 16	0x0108 0780	0x0108 07FF
	Sector 16	1K x 16	0x0008 4000	0x0008 43FF	128 x 16	0x0108 0800	0x0108 087F
	Sector 17	1K x 16	0x0008 4400	0x0008 47FF	128 x 16	0x0108 0880	0x0108 08FF
	Sector 18	1K x 16	0x0008 4800	0x0008 4BFF	128 x 16	0x0108 0900	0x0108 097F
	Sector 19	1K x 16	0x0008 4C00	0x0008 4FFF	128 x 16	0x0108 0980	0x0108 09FF
	Sector 20	1K x 16	0x0008 5000	0x0008 53FF	128 x 16	0x0108 0A00	0x0108 0A7F
	Sector 21	1K x 16	0x0008 5400	0x0008 57FF	128 x 16	0x0108 0A80	0x0108 0AFF
	Sector 22	1K x 16	0x0008 5800	0x0008 5BFF	128 x 16	0x0108 0B00	0x0108 0B7F
	Sector 23	1K x 16	0x0008 5C00	0x0008 5FFF	128 x 16	0x0108 0B80	0x0108 0BFF
	Sector 24	1K x 16	0x0008 6000	0x0008 63FF	128 x 16	0x0108 0C00	0x0108 0C7F
	Sector 25	1K x 16	0x0008 6400	0x0008 67FF	128 x 16	0x0108 0C80	0x0108 0CFF
	Sector 26	1K x 16	0x0008 6800	0x0008 6BFF	128 x 16	0x0108 0D00	0x0108 0D7F
	Sector 27	1K x 16	0x0008 6C00	0x0008 6FFF	128 x 16	0x0108 0D80	0x0108 0DFF
	Sector 28	1K x 16	0x0008 7000	0x0008 73FF	128 x 16	0x0108 0E00	0x0108 0E7F
	Sector 29	1K x 16	0x0008 7400	0x0008 77FF	128 x 16	0x0108 0E80	0x0108 0EFF
	Sector 30	1K x 16	0x0008 7800	0x0008 7BFF	128 x 16	0x0108 0F00	0x0108 0F7F
	Sector 31	1K x 16	0x0008 7C00	0x0008 7FFF	128 x 16	0x0108 0F80	0x0108 0FFF

Table 7-2. Flash Memory Map (continued)

PART NUMBER	SECTOR	ADDRESS			ECC ADDRESS		
		SIZE	START	END	SIZE	START	END
F2800137, F2800135	Sector 32	1K x 16	0x0008 8000	0x0008 83FF	128 x 16	0x0108 1000	0x0108 107F
	Sector 33	1K x 16	0x0008 8400	0x0008 87FF	128 x 16	0x0108 1080	0x0108 10FF
	Sector 34	1K x 16	0x0008 8800	0x0008 8BFF	128 x 16	0x0108 1100	0x0108 117F
	Sector 35	1K x 16	0x0008 8C00	0x0008 8FFF	128 x 16	0x0108 1180	0x0108 11FF
	Sector 36	1K x 16	0x0008 9000	0x0008 93FF	128 x 16	0x0108 1200	0x0108 127F
	Sector 37	1K x 16	0x0008 9400	0x0008 97FF	128 x 16	0x0108 1280	0x0108 12FF
	Sector 38	1K x 16	0x0008 9800	0x0008 9BFF	128 x 16	0x0108 1300	0x0108 137F
	Sector 39	1K x 16	0x0008 9C00	0x0008 9FFF	128 x 16	0x0108 1380	0x0108 13FF
	Sector 40	1K x 16	0x0008 A000	0x0008 A3FF	128 x 16	0x0108 1400	0x0108 147F
	Sector 41	1K x 16	0x0008 A400	0x0008 A7FF	128 x 16	0x0108 1480	0x0108 14FF
	Sector 42	1K x 16	0x0008 A800	0x0008 ABFF	128 x 16	0x0108 1500	0x0108 157F
	Sector 43	1K x 16	0x0008 AC00	0x0008 AFFF	128 x 16	0x0108 1580	0x0108 15FF
	Sector 44	1K x 16	0x0008 B000	0x0008 B3FF	128 x 16	0x0108 1600	0x0108 167F
	Sector 45	1K x 16	0x0008 B400	0x0008 B7FF	128 x 16	0x0108 1680	0x0108 16FF
	Sector 46	1K x 16	0x0008 B800	0x0008 BBFF	128 x 16	0x0108 1700	0x0108 177F
	Sector 47	1K x 16	0x0008 BC00	0x0008 BFFF	128 x 16	0x0108 1780	0x0108 17FF
	Sector 48	1K x 16	0x0008 C000	0x0008 C3FF	128 x 16	0x0108 1800	0x0108 187F
	Sector 49	1K x 16	0x0008 C400	0x0008 C7FF	128 x 16	0x0108 1880	0x0108 18FF
	Sector 50	1K x 16	0x0008 C800	0x0008 CBFF	128 x 16	0x0108 1900	0x0108 197F
	Sector 51	1K x 16	0x0008 CC00	0x0008 CFFF	128 x 16	0x0108 1980	0x0108 19FF
	Sector 52	1K x 16	0x0008 D000	0x0008 D3FF	128 x 16	0x0108 1A00	0x0108 1A7F
	Sector 53	1K x 16	0x0008 D400	0x0008 D7FF	128 x 16	0x0108 1A80	0x0108 1AFF
	Sector 54	1K x 16	0x0008 D800	0x0008 DBFF	128 x 16	0x0108 1B00	0x0108 1B7F
	Sector 55	1K x 16	0x0008 DC00	0x0008 DFFF	128 x 16	0x0108 1B80	0x0108 1BFF
	Sector 56	1K x 16	0x0008 E000	0x0008 E3FF	128 x 16	0x0108 1C00	0x0108 1C7F
	Sector 57	1K x 16	0x0008 E400	0x0008 E7FF	128 x 16	0x0108 1C80	0x0108 1CFF
	Sector 58	1K x 16	0x0008 E800	0x0008 EBFF	128 x 16	0x0108 1D00	0x0108 1D7F
	Sector 59	1K x 16	0x0008 EC00	0x0008 EFFF	128 x 16	0x0108 1D80	0x0108 1DFF
	Sector 60	1K x 16	0x0008 F000	0x0008 F3FF	128 x 16	0x0108 1E00	0x0108 1E7F
	Sector 61	1K x 16	0x0008 F400	0x0008 F7FF	128 x 16	0x0108 1E80	0x0108 1EFF
	Sector 62	1K x 16	0x0008 F800	0x0008 FBFF	128 x 16	0x0108 1F00	0x0108 1F7F
	Sector 63	1K x 16	0x0008 FC00	0x0008 FFFF	128 x 16	0x0108 1F80	0x0108 1FFF

Table 7-2. Flash Memory Map (continued)

PART NUMBER	SECTOR	ADDRESS			ECC ADDRESS		
		SIZE	START	END	SIZE	START	END
F2800137	Sector 64	1K x 16	0x0009 0000	0x0009 03FF	128 x 16	0x0108 2000	0x0108 207F
	Sector 65	1K x 16	0x0009 0400	0x0009 07FF	128 x 16	0x0108 2080	0x0108 20FF
	Sector 66	1K x 16	0x0009 0800	0x0009 0BFF	128 x 16	0x0108 2100	0x0108 217F
	Sector 67	1K x 16	0x0009 0C00	0x0009 0FFF	128 x 16	0x0108 2180	0x0108 21FF
	Sector 68	1K x 16	0x0009 1000	0x0009 13FF	128 x 16	0x0108 2200	0x0108 227F
	Sector 69	1K x 16	0x0009 1400	0x0009 17FF	128 x 16	0x0108 2280	0x0108 22FF
	Sector 70	1K x 16	0x0009 1800	0x0009 1BFF	128 x 16	0x0108 2300	0x0108 237F
	Sector 71	1K x 16	0x0009 1C00	0x0009 1FFF	128 x 16	0x0108 2380	0x0108 23FF
	Sector 72	1K x 16	0x0009 2000	0x0009 23FF	128 x 16	0x0108 2400	0x0108 247F
	Sector 73	1K x 16	0x0009 2400	0x0009 27FF	128 x 16	0x0108 2480	0x0108 24FF
	Sector 74	1K x 16	0x0009 2800	0x0009 2BFF	128 x 16	0x0108 2500	0x0108 257F
	Sector 75	1K x 16	0x0009 2C00	0x0009 2FFF	128 x 16	0x0108 2580	0x0108 25FF
	Sector 76	1K x 16	0x0009 3000	0x0009 33FF	128 x 16	0x0108 2600	0x0108 267F
	Sector 77	1K x 16	0x0009 3400	0x0009 37FF	128 x 16	0x0108 2680	0x0108 26FF
	Sector 78	1K x 16	0x0009 3800	0x0009 3BFF	128 x 16	0x0108 2700	0x0108 277F
	Sector 79	1K x 16	0x0009 3C00	0x0009 3FFF	128 x 16	0x0108 2780	0x0108 27FF
	Sector 80	1K x 16	0x0009 4000	0x0009 43FF	128 x 16	0x0108 2800	0x0108 287F
	Sector 81	1K x 16	0x0009 4400	0x0009 47FF	128 x 16	0x0108 2880	0x0108 28FF
	Sector 82	1K x 16	0x0009 4800	0x0009 4BFF	128 x 16	0x0108 2900	0x0108 297F
	Sector 83	1K x 16	0x0009 4C00	0x0009 4FFF	128 x 16	0x0108 2980	0x0108 29FF
	Sector 84	1K x 16	0x0009 5000	0x0009 53FF	128 x 16	0x0108 2A00	0x0108 2A7F
	Sector 85	1K x 16	0x0009 5400	0x0009 57FF	128 x 16	0x0108 2A80	0x0108 2AFF
	Sector 86	1K x 16	0x0009 5800	0x0009 5BFF	128 x 16	0x0108 2B00	0x0108 2B7F
	Sector 87	1K x 16	0x0009 5C00	0x0009 5FFF	128 x 16	0x0108 2B80	0x0108 2BFF
	Sector 88	1K x 16	0x0009 6000	0x0009 63FF	128 x 16	0x0108 2C00	0x0108 2C7F
	Sector 89	1K x 16	0x0009 6400	0x0009 67FF	128 x 16	0x0108 2C80	0x0108 2CFF
	Sector 90	1K x 16	0x0009 6800	0x0009 6BFF	128 x 16	0x0108 2D00	0x0108 2D7F
	Sector 91	1K x 16	0x0009 6C00	0x0009 6FFF	128 x 16	0x0108 2D80	0x0108 2DFF
	Sector 92	1K x 16	0x0009 7000	0x0009 73FF	128 x 16	0x0108 2E00	0x0108 2E7F
	Sector 93	1K x 16	0x0009 7400	0x0009 77FF	128 x 16	0x0108 2E80	0x0108 2EFF
	Sector 94	1K x 16	0x0009 7800	0x0009 7BFF	128 x 16	0x0108 2F00	0x0108 2F7F
	Sector 95	1K x 16	0x0009 7C00	0x0009 7FFF	128 x 16	0x0108 2F80	0x0108 2FFF

Table 7-2. Flash Memory Map (continued)

PART NUMBER	SECTOR	ADDRESS			ECC ADDRESS		
		SIZE	START	END	SIZE	START	END
F2800137	Sector 96	1K x 16	0x0009 8000	0x0009 83FF	128 x 16	0x0108 3000	0x0108 307F
	Sector 97	1K x 16	0x0009 8400	0x0009 87FF	128 x 16	0x0108 3080	0x0108 30FF
	Sector 98	1K x 16	0x0009 8800	0x0009 8BFF	128 x 16	0x0108 3100	0x0108 317F
	Sector 99	1K x 16	0x0009 8C00	0x0009 8FFF	128 x 16	0x0108 3180	0x0108 31FF
	Sector 100	1K x 16	0x0009 9000	0x0009 93FF	128 x 16	0x0108 3200	0x0108 327F
	Sector 101	1K x 16	0x0009 9400	0x0009 97FF	128 x 16	0x0108 3280	0x0108 32FF
	Sector 102	1K x 16	0x0009 9800	0x0009 9BFF	128 x 16	0x0108 3300	0x0108 337F
	Sector 103	1K x 16	0x0009 9C00	0x0009 9FFF	128 x 16	0x0108 3380	0x0108 33FF
	Sector 104	1K x 16	0x0009 A000	0x0009 A3FF	128 x 16	0x0108 3400	0x0108 347F
	Sector 105	1K x 16	0x0009 A400	0x0009 A7FF	128 x 16	0x0108 3480	0x0108 34FF
	Sector 106	1K x 16	0x0009 A800	0x0009 ABFF	128 x 16	0x0108 3500	0x0108 357F
	Sector 107	1K x 16	0x0009 AC00	0x0009 AFFF	128 x 16	0x0108 3580	0x0108 35FF
	Sector 108	1K x 16	0x0009 B000	0x0009 B3FF	128 x 16	0x0108 3600	0x0108 367F
	Sector 109	1K x 16	0x0009 B400	0x0009 B7FF	128 x 16	0x0108 3680	0x0108 36FF
	Sector 110	1K x 16	0x0009 B800	0x0009 BBFF	128 x 16	0x0108 3700	0x0108 377F
	Sector 111	1K x 16	0x0009 BC00	0x0009 BFFF	128 x 16	0x0108 3780	0x0108 37FF
	Sector 112	1K x 16	0x0009 C000	0x0009 C3FF	128 x 16	0x0108 3800	0x0108 387F
	Sector 113	1K x 16	0x0009 C400	0x0009 C7FF	128 x 16	0x0108 3880	0x0108 38FF
	Sector 114	1K x 16	0x0009 C800	0x0009 CBFF	128 x 16	0x0108 3900	0x0108 397F
	Sector 115	1K x 16	0x0009 CC00	0x0009 CFFF	128 x 16	0x0108 3980	0x0108 39FF
	Sector 116	1K x 16	0x0009 D000	0x0009 D3FF	128 x 16	0x0108 3A00	0x0108 3A7F
	Sector 117	1K x 16	0x0009 D400	0x0009 D7FF	128 x 16	0x0108 3A80	0x0108 3AFF
	Sector 118	1K x 16	0x0009 D800	0x0009 DBFF	128 x 16	0x0108 3B00	0x0108 3B7F
	Sector 119	1K x 16	0x0009 DC00	0x0009 DFFF	128 x 16	0x0108 3B80	0x0108 3BFF
	Sector 120	1K x 16	0x0009 E000	0x0009 E3FF	128 x 16	0x0108 3C00	0x0108 3C7F
	Sector 121	1K x 16	0x0009 E400	0x0009 E7FF	128 x 16	0x0108 3C80	0x0108 3CFF
	Sector 122	1K x 16	0x0009 E800	0x0009 EBFF	128 x 16	0x0108 3D00	0x0108 3D7F
	Sector 123	1K x 16	0x0009 EC00	0x0009 EFFF	128 x 16	0x0108 3D80	0x0108 3DFF
	Sector 124	1K x 16	0x0009 F000	0x0009 F3FF	128 x 16	0x0108 3E00	0x0108 3E7F
	Sector 125	1K x 16	0x0009 F400	0x0009 F7FF	128 x 16	0x0108 3E80	0x0108 3EFF
	Sector 126	1K x 16	0x0009 F800	0x0009 FBFF	128 x 16	0x0108 3F00	0x0108 3F7F
	Sector 127	1K x 16	0x0009 FC00	0x0009 FFFF	128 x 16	0x0108 3F80	0x0108 3FFF

7.3.3 Peripheral Registers Memory Map

Table 7-3. Peripheral Registers Memory Map

Bit Field Name		DriverLib Name	Base Address	Pipeline Protected
Instance	Structure			
Peripheral Frame 0 (PF0)				
-	-	M0_RAM_BASE	0x0000_0000	-
-	-	M1_RAM_BASE	0x0000_0400	-
AdcaResultRegs	ADC_RESULT_REGS	ADCARESULT_BASE	0x0000_0B00	-
AdccResultRegs	ADC_RESULT_REGS	ADCCRESULT_BASE	0x0000_0B40	-
CpuTimer0Regs	CPUTIMER_REGS	CPUTIMER0_BASE	0x0000_0C00	-
CpuTimer1Regs	CPUTIMER_REGS	CPUTIMER1_BASE	0x0000_0C08	-
CpuTimer2Regs	CPUTIMER_REGS	CPUTIMER2_BASE	0x0000_0C10	-
PieCtrlRegs	PIE_CTRL_REGS	PIECTRL_BASE	0x0000_0CE0	-
PieVectTable	PIE_VECT_TABLE	PIEVECTTABLE_BASE	0x0000_0D00	-
-	-	LS0_RAM_BASE	0x0000_8000	-

Table 7-3. Peripheral Registers Memory Map (continued)

Bit Field Name		DriverLib Name	Base Address	Pipeline Protected
Instance	Structure			
-	-	LS1_RAM_BASE	0x0000_A000	-
UidRegs	UID_REGS	UID_BASE	0x0007_1140	-
DcsmZ1OtpRegs	DCSM_Z1_OTP	DCSM_Z1OTP_BASE	0x0007_8000	-
DcsmZ2OtpRegs	DCSM_Z2_OTP	DCSM_Z2OTP_BASE	0x0007_8200	-
Peripheral Frame 1 (PF1)				
EPwm1Regs	EPWM_REGS	EPWM1_BASE	0x0000_4000	YES
EPwm2Regs	EPWM_REGS	EPWM2_BASE	0x0000_4100	YES
EPwm3Regs	EPWM_REGS	EPWM3_BASE	0x0000_4200	YES
EPwm4Regs	EPWM_REGS	EPWM4_BASE	0x0000_4300	YES
EPwm5Regs	EPWM_REGS	EPWM5_BASE	0x0000_4400	YES
EPwm6Regs	EPWM_REGS	EPWM6_BASE	0x0000_4500	YES
EPwm7Regs	EPWM_REGS	EPWM7_BASE	0x0000_4600	YES
EQep1Regs	EQEP_REGS	EQEP1_BASE	0x0000_5100	YES
ECap1Regs	ECAP_REGS	ECAP1_BASE	0x0000_5200	YES
ECap2Regs	ECAP_REGS	ECAP2_BASE	0x0000_5240	YES
Cmpss1Regs	CMPSS_REGS	CMPSS1_BASE	0x0000_5500	YES
CmpssLite2Regs	CMPSS_LITE_REGS	CMPSSLITE2_BASE	0x0000_5540	YES
CmpssLite3Regs	CMPSS_LITE_REGS	CMPSSLITE3_BASE	0x0000_5580	YES
CmpssLite4Regs	CMPSS_LITE_REGS	CMPSSLITE4_BASE	0x0000_55C0	YES
Peripheral Frame 2 (PF2)				
SpiaRegs	SPI_REGS	SPIA_BASE	0x0000_6100	YES
Peripheral Frame 3 (PF3)				
AdcaRegs	ADC_REGS	ADCA_BASE	0x0000_7400	YES
AdccRegs	ADC_REGS	ADCC_BASE	0x0000_7500	YES
Peripheral Frame 4 (PF4)				
InputXbarRegs	INPUT_XBAR_REGS	INPUTXBAR_BASE	0x0000_7900	YES
XbarRegs	XBAR_REGS	XBAR_BASE	0x0000_7920	YES
SyncSocRegs	SYNC_SOC_REGS	SYNCSOC_BASE	0x0000_7940	YES
EPwmXbarRegs	EPWM_XBAR_REGS	EPWMXBAR_BASE	0x0000_7A00	YES
OutputXbarRegs	OUTPUT_XBAR_REGS	OUTPUTXBAR_BASE	0x0000_7A80	YES
GpioCtrlRegs	GPIO_CTRL_REGS	GPIOCTRL_BASE	0x0000_7C00	YES
GpioDataRegs	GPIO_DATA_REGS	GPIODATA_BASE	0x0000_7F00	YES
GpioDataReadRegs	GPIO_DATA_READ_REGS	GPIODATAREAD_BASE	0x0000_7F80	YES
DevCfgRegs	DEV_CFG_REGS	DEVCFG_BASE	0x0005_D000	YES
ClkCfgRegs	CLK_CFG_REGS	CLKCFG_BASE	0x0005_D200	YES
CpuSysRegs	CPU_SYS_REGS	CPUSYS_BASE	0x0005_D300	YES
SysStatusRegs	SYS_STATUS_REGS	SYSSTAT_BASE	0x0005_D400	YES
AnalogSubsysRegs	ANALOG_SUBSYS_REGS	ANALOGSUBSYS_BASE	0x0005_D700	YES
Peripheral Frame 6 (PF6)				
Epg1Regs	EPG_REGS	EPG1_BASE	0x0005_EC00	YES
Epg1MuxRegs	EPG_MUX_REGS	EPG1MUX_BASE	0x0005_ECD0	YES
DcsmZ1Regs	DCSM_Z1_REGS	DCSM_Z1_BASE	0x0005_F000	YES
DcsmZ2Regs	DCSM_Z2_REGS	DCSM_Z2_BASE	0x0005_F080	YES
DcsmCommonRegs	DCSM_COMMON_REGS	DCSMCOMMON_BASE	0x0005_F0C0	YES
MemCfgRegs	MEM_CFG_REGS	MEMCFG_BASE	0x0005_F400	YES
AccessProtectionRegs	ACCESS_PROTECTION_REGS	ACCESSPROTECTION_BASE	0x0005_F500	YES
MemoryErrorRegs	MEMORY_ERROR_REGS	MEMORYERROR_BASE	0x0005_F540	YES
TestErrorRegs	TEST_ERROR_REGS	TESTERROR_BASE	0x0005_F590	YES
Flash0CtrlRegs	FLASH_CTRL_REGS	FLASH0CTRL_BASE	0x0005_F800	YES

Table 7-3. Peripheral Registers Memory Map (continued)

Bit Field Name		DriverLib Name	Base Address	Pipeline Protected
Instance	Structure			
Flash0EccRegs	FLASH_ECC_REGS	FLASH0ECC_BASE	0x0005_FB00	YES
Peripheral Frame 7 (PF7)				
CanaRegs	CAN_REGS	CANA_BASE	0x0004_8000	YES
-	-	CANA_MSG_RAM_BASE	0x0004_9000	YES
MpostRegs	MPOST_REGS	MPOST_BASE	0x0005_E200	YES
Dcc0Regs	DCC_REGS	DCC0_BASE	0x0005_E700	YES
Peripheral Frame 9 (PF9)				
WdRegs	WD_REGS	WD_BASE	0x0000_7000	YES
NmiIntruptRegs	NMI_INTRUPT_REGS	NMI_BASE	0x0000_7060	YES
XintRegs	XINT_REGS	XINT_BASE	0x0000_7070	YES
SciaRegs	SCI_REGS	SCIA_BASE	0x0000_7200	YES
ScibRegs	SCI_REGS	SCIB_BASE	0x0000_7210	YES
ScicRegs	SCI_REGS	SCIC_BASE	0x0000_7220	YES
I2caRegs	I2C_REGS	I2CA_BASE	0x0000_7300	YES
I2cbRegs	I2C_REGS	I2CB_BASE	0x0000_7340	YES

7.4 Identification

Table 7-4 lists the Device Identification Registers. Additional information on these device identification registers can be found in the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual*.

Table 7-4. Device Identification Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION	
			Bits	*Options*
PARTIDL	0x0005 D008	2	14-13 RESERVED	RESERVED
			10-8 PIN_COUNT	2 = 64 pin (QFP) 3 = 80 pin (QFP) 4 = 48 pin (QFP) 5 = 32 pin (QFN) 7 = 48 pin (QFN) 8 = 64 pin (QFP, with VREGENZ)
			7-6 QUAL	0 = Engineering sample (TMX) 1 = Pilot production (TMP) 2 = Fully qualified (TMS)
PARTIDH	0x0005 D00A	2	Device part identification number	
			TMS320F2800137	0x06FF 0500
			TMS320F2800135 (non-VPM packages)	0x06FD 0500
			TMS320F2800133	0x06FB 0500
			TMS320F2800132	0x06FA 0500
			TMS320F2800135VPM	0x06F9 0500
REVID	0x0005 D00C	2	Silicon revision number	
			Revision 0	0x0000 0001
			Revision A	0x0000 0002
			Revision B	0x0000 0003
			Revision C	0x0000 0004
UID_UNIQUE0	0x0007 114A	2	Unique identification number. This number is different on each individual device with the same PARTIDH. This unique number can be used as a serial number in the application. This number is present only on TMS devices.	
UID_UNIQUE1	0x0007 114C	2	Unique identification number. This number is different on each individual device with the same PARTIDH. This unique number can be used as a serial number in the application. This number is present only on TMS devices.	

7.5 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the *TMS320C28x CPU and Instruction Set Reference Guide*.

7.5.1 Floating-Point Unit (FPU)

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating-point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the RB, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

For more information on the C28x Floating Point Unit (FPU), see the *TMS320C28x Extended Instruction Sets Technical Reference Manual*.

7.5.2 Trigonometric Math Unit (TMU)

The trigonometric math unit (TMU) extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in Table 7-5.

Table 7-5. TMU Supported Instructions

Instructions	C Equivalent Operation	Pipeline Cycles
MPY2PIF32 RaH,RbH	a = b * 2pi	2/3
DIV2PIF32 RaH,RbH	a = b / 2pi	2/3
DIVF32 RaH,RbH,RcH	a = b/c	5
SQRTF32 RaH,RbH	a = sqrt(b)	5
SINPUF32 RaH,RbH	a = sin(b*2pi)	4
COSPUF32 RaH,RbH	a = cos(b*2pi)	4
ATANPUF32 RaH,RbH	a = atan(b)/2pi	4
QUADF32 RaH,RbH,RcH,RdH	Operation to assist in calculating ATANPU2	5

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations.

For more information, see the *TMS320C28x Extended Instruction Sets Technical Reference Manual*.

7.6 Device Boot Modes

This section explains the default boot modes, as well as all the available boot modes supported on this device. The boot ROM uses the boot mode select, general-purpose input/output (GPIO) pins to determine the boot mode configuration.

Table 7-6 shows the boot mode options available for selection by the default boot mode select pins. Users have the option to program the device to customize the boot modes selectable in the boot-up table as well as the boot mode select pin GPIOs used.

All the peripheral boot modes that are supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, CANA, and so forth). Whenever these boot modes are referred to in this chapter, such as SCI boot, it is actually referring to the first module instance, which means the SCI boot on the SCIA port. The same applies to the other peripheral boots.

See the Reset (XRSn) Switching Characteristics table and the Reset Timing Diagrams for $t_{boot\text{-}flash}$, the boot ROM execution time to first instruction fetch in flash.

Table 7-6. Device Default Boot Modes

BOOT MODE	GPIO24 (DEFAULT BOOT MODE SELECT PIN 1)	GPIO32 (DEFAULT BOOT MODE SELECT PIN 0)
Parallel IO	0	0
SCI / Wait Boot(1)	0	1
CAN	1	0
Flash	1	1

(1) SCI boot mode can be used as a wait boot mode as long as SCI continues to wait for an 'A' or 'a' during the SCI autobaud lock process.

Table 7-7 lists the possible boot modes supported on the device. The default boot mode pins are GPIO24 (boot mode pin 1) and GPIO32 (boot mode pin 0). Users may choose to have weak pullups for boot mode pins if they use a peripheral on these pins as well, so the pullups can be overdriven. On this device, customers can change the factory default boot mode pins by programming user-configurable Dual Code Security Module (DCSM) OTP locations.

Table 7-7. All Available Boot Modes

BOOT MODE NUMBER	BOOT MODE
0	Parallel
1	SCI / Wait
2	CAN
3	Flash
4	Wait
5	RAM
6	SPI
7	I2C
10	Secure Flash

Note

All the peripheral boot modes supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, CANA, and so forth). Whenever these boot modes are referred to in this section, such as SCI boot, it is actually referring to the first module instance, meaning SCI boot on the SCIA port. The same applies to the other peripheral boots.

7.6.1 Device Boot Configurations

This section details what boot configurations are available and how to configure them. This device supports from 0 boot mode select pins up to 3 boot mode select pins as well as from 1 configured boot mode up to 8 configured boot modes.

To change and configure the device from the default settings to custom settings for your application, use the following process:

1. Determine all the various ways you want application to be able to boot. (For example: Primary boot option of Flash boot for your main application, secondary boot option of CAN boot for firmware updates, tertiary boot option of SCI boot for debugging, etc)
2. Based on the number of boot modes needed, determine how many boot mode select pins (BMSPs) are required to select between your selected boot modes. (For example: 2 BMSPs are required to select between 3 boot mode options)
3. Assign the required BMSPs to a physical GPIO pin. (For example, BMSP0 to GPIO10, BMSP1 to GPIO51, and BMSP2 left as default which is disabled). Refer to Section 7.6.1.1 for all the details on performing these configurations.
4. Assign the determined boot mode definitions to indexes in your custom boot table that correlate to the decoded value of the BMSPs. For example, BOOTDEF0=Boot to Flash, BOOTDEF1=CAN Boot, BOOTDEF2=SCI Boot; all other BOOTDEFx are left as default/nothing). Refer to Section 7.6.1.2 for all the details on setting up and configuring the custom boot mode table.

Additionally, the Boot Mode Example Use Cases section of the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual* provides some example use cases on how to configure the BMSPs and custom boot tables.

Note

The CAN boot mode turns on the XTAL. Be sure an XTAL is installed in the application before using CAN boot mode.

7.6.1.1 Configuring Boot Mode Pins

This section explains how the boot mode select pins can be customized by the user, by programming the BOOTPIN-CONFIG location (refer to Table 7-8) in the user-configurable dual-zone security module (DCSM) OTP. The location in the DCSM OTP is Z1-OTP-BOOTPIN-CONFIG or Z2-OTP-BOOTPIN-CONFIG. When debugging, EMU-BOOTPIN-CONFIG is the emulation equivalent of Z1-OTP-BOOTPIN-CONFIG/Z2-OTP-BOOTPIN-CONFIG, and can be programmed to experiment with different boot modes without writing to OTP. The device can be programmed to use 0, 1, 2, or 3 boot mode select pins as needed.

Note

When using Z2-OTP-BOOTPIN-CONFIG, the configurations programmed in this location will take priority over the configurations in Z1-OTP-BOOTPIN-CONFIG. It is recommended to use Z1-OTP-BOOTPIN-CONFIG first and then if OTP configurations need to be altered, switch to using Z2-OTP-BOOTPIN-CONFIG.

Table 7-8. BOOTPIN-CONFIG Bit Fields

BIT	NAME	DESCRIPTION
31:24	Key	Write 0x5A to these 8-bits to indicate the bits in this register are valid
23:16	Boot Mode Select Pin 2 (BMSP2)	Refer to BMSP0 description except for BMSP2
15:8	Boot Mode Select Pin 1 (BMSP1)	Refer to BMSP0 description except for BMSP1
7:0	Boot Mode Select Pin 0 (BMSP0)	Set to the GPIO pin to be used during boot (up to 255): - 0x0 = GPIO0 - 0x01 = GPIO1 - and so on Writing 0xFF disables BMSP0 and this pin is no longer used to select the boot mode.

Note

GPIO 224 to 253 are analog pins, but digital inputs are possible on these pins provided the software writes to the GPIOHAMSEL register bits.

The following GPIOs **cannot** be used as a BMSP. If selected for a particular BMSP, the boot ROM will automatically select the factory default GPIOs for BMSP0 and BMSP1. Factory default for BMSP2 is 0xFF, which disables the BMSP.

- GPIO 14 and GPIO 15 (Not available on any package)
- GPIO 25 to GPIO 27 (Not available on any package)
- GPIO 30, GPIO 31, GPIO 34, and GPIO 38 (Not available on any package)
- GPIO 42 to GPIO 58 (Not available on any package)
- GPIO 62 to GPIO 223 (Not available on any package)

Table 7-9. Standalone Boot Mode Select Pin Decoding

BOOTPIN_CONFIG KEY	BMSP0	BMSP1	BMSP2	REALIZED BOOT MODE
!= 0x5A	Don't Care	Don't Care	Don't Care	Boot as defined by the factory default BMSPs
= 0x5A	0xFF	0xFF	0xFF	Boot as defined in the boot table for boot mode 0 (All BMSPs disabled)
	Valid GPIO	0xFF	0xFF	Boot as defined by the value of BMSP0 (BMSP1 and BMSP2 disabled)
	0xFF	Valid GPIO	0xFF	Boot as defined by the value of BMSP1 (BMSP0 and BMSP2 disabled)
	0xFF	0xFF	Valid GPIO	Boot as defined by the value of BMSP2 (BMSP0 and BMSP1 disabled)
	Valid GPIO	Valid GPIO	0xFF	Boot as defined by the values of BMSP0 and BMSP1 (BMSP2 disabled)
	Valid GPIO	0xFF	Valid GPIO	Boot as defined by the values of BMSP0 and BMSP2 (BMSP1 disabled)
	0xFF	Valid GPIO	Valid GPIO	Boot as defined by the values of BMSP1 and BMSP2 (BMSP0 disabled)
	Valid GPIO	Valid GPIO	Valid GPIO	Boot as defined by the values of BMSP0, BMSP1, and BMSP2
	Invalid GPIO	Valid GPIO	Valid GPIO	BMSP0 is reset to the factory default BMSP0 GPIO Boot as defined by the values of BMSP0, BMSP1, and BMSP2
	Valid GPIO	Invalid GPIO	Valid GPIO	BMSP1 is reset to the factory default BMSP1 GPIO Boot as defined by the values of BMSP0, BMSP1, and BMSP2
	Valid GPIO	Valid GPIO	Invalid GPIO	BMSP2 is reset to the factory default state, which is disabled Boot as defined by the values of BMSP0 and BMSP1

Note

When decoding the boot mode, BMSP0 is the least-significant-bit and BMSP2 is the most-significant-bit of the boot table index value. It is recommended when disabling BMSPs to start with disabling BMSP2. For example, in an instance when only using BMSP2 (BMSP1 and BMSP0 are disabled), then only the boot table indexes of 0 and 4 will be selectable. In the instance when using only BMSP0, then the selectable boot table indexes are 0 and 1.

7.6.1.2 Configuring Boot Mode Table Options

This section explains how to configure the boot definition table, BOOTDEF, for the device and the associated boot options. The 64-bit location is located in user-configurable DCSM OTP in the Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations. When debugging, EMU-BOOTDEF-LOW and EMU-BOOTDEF-HIGH are the emulation equivalents of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH, and can be programmed to experiment with different boot mode options without writing to OTP. The range of customization to the boot definition table depends on how many boot mode select pins (BMSP) are being used. For example, 0 BMSPs equals to 1 table entry, 1 BMSP equals to 2 table entries, 2 BMSPs equals to 4 table entries, and 3 BMSPs equals to 8 table entries. Refer to the *TMS320F280013x Real-Time Microcontrollers Technical Reference Manual* for examples on how to set up the BOOTPIN_CONFIG and BOOTDEF values.

Note

The locations Z2-OTP-BOOTDEF-LOW and Z2-OTP-BOOTDEF-HIGH will be used instead of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations when Z2-OTP-BOOTPIN-CONFIG is configured. Refer to Section 7.6.1.1 for more details on BOOTPIN_CONFIG usage.

Table 7-10. BOOTDEF Bit Fields

BOOTDEF NAME	BYTE POSITION	NAME	DESCRIPTION
BOOT_DEF0	7:0	BOOT_DEF0 Mode/Options	Set the boot mode for index 0 of the boot table. Different boot modes and their options can include, for example, a boot mode that uses different GPIOs for a specific bootloader or a different flash entry point address. Any unsupported boot mode will cause the device to either go to wait boot or boot to flash. Refer to *GPIO Assignments* for valid BOOTDEF values to set in the table.
BOOT_DEF1	15:8	BOOT_DEF1 Mode/Options	Refer to BOOT_DEF0 description
BOOT_DEF2	23:16	BOOT_DEF2 Mode/Options	
BOOT_DEF3	31:24	BOOT_DEF3 Mode/Options	
BOOT_DEF4	39:32	BOOT_DEF4 Mode/Options	
BOOT_DEF5	47:40	BOOT_DEF5 Mode/Options	
BOOT_DEF6	55:48	BOOT_DEF6 Mode/Options	
BOOT_DEF7	63:56	BOOT_DEF7 Mode/Options	

7.6.2 GPIO Assignments

This section details the GPIOs and boot option values used for boot mode set in the BOOT_DEF memory location located at Z1-OTP-BOOTDEF-LOW/ Z2-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH/ Z2-OTP-BOOTDEF-HIGH. Refer to Configuring Boot Mode Table Options on how to configure BOOT_DEF. When selecting a boot mode option, make sure to verify that the necessary pins are available in the pin mux options for the specific device package being used.

Table 7-11. SCI Boot Options

OPTION	BOOTDEF VALUE	SCITXDA GPIO	SCIRXDA GPIO
0 (default)	0x01	GPIO29	GPIO28
1	0x21	GPIO1	GPIO0
2	0x41	GPIO8	GPIO9
3	0x61	GPIO7	GPIO3
4	0x81	GPIO16	GPIO3

Table 7-12. CAN Boot Options

OPTION	BOOTDEF VALUE	CANTXA GPIO	CANRXA GPIO
0 (default)	0x02	GPIO4	GPIO5
1	0x22	GPIO32	GPIO33
2	0x42	GPIO2	GPIO3
3	0x62	GPIO13	GPIO12

Note

F280013x and F280015x CANTXA GPIO Option 0 (default) selections are different. All other CAN boot option GPIO selections are the same. Please refer to respective device data sheet for details.

Table 7-13. I2C Boot Options

OPTION	BOOTDEF VALUE	SDAA GPIO	SCLA GPIO
0	0x07	GPIO0	GPIO1
1	0x27	GPIO32	GPIO33
2	0x47	GPIO5	GPIO4

Table 7-14. RAM Boot Options

OPTION	BOOTDEF VALUE	RAM ENTRY POINT (ADDRESS)
0	0x05	0x0000 0000

Table 7-15. Flash Boot Options

OPTION	BOOTDEF VALUE	FLASH ENTRY POINT (ADDRESS)	FLASH SECTOR
0 (default)	0x03	0x0008 0000	Bank0 Sector 0
1	0x23	0x0008 8000	Bank 0 Sector 32
2	0x43	0x0008 FFF0	Bank 0 End of Sector 63
3	0x63	0x0009 0000	Bank 0 Sector 64
4	0x83	0x0009 8000	Bank 0 Sector 96
6	0xA3	0x0009 FFF0	Bank 0 End of Sector 127

Table 7-16. Secure Flash Boot Options

OPTION	BOOTDEF VALUE	FLASH ENTRY POINT (ADDRESS)	FLASH SECTOR
0 (default)	0x0A	0x0008 0000	Bank0 Sector 0

Table 7-16. Secure Flash Boot Options (continued)

OPTION	BOOTDEF VALUE	FLASH ENTRY POINT (ADDRESS)	FLASH SECTOR
1	0x2A	0x0008 8000	Bank 0 Sector 32
2	0x4A	0x0008 FFF0	Bank 0 End of Sector 63
3	0x6A	0x0009 0000	Bank 0 Sector 64
4	0x8A	0x0009 8000	Bank 0 Sector 96

Table 7-17. Wait Boot Options

OPTION	BOOTDEF VALUE	WATCHDOG
0	0x04	Enabled
1	0x24	Disabled

Table 7-18. SPI Boot Options

OPTION	BOOTDEF VALUE	SPISIMOA	SPISOMIA	SPICLKA	SPISTEA
0	0x06	GPIO7	GPIO1	GPIO3	GPIO5
1	0x26	GPIO16	GPIO1	GPIO3	GPIO0
2	0x46	GPIO8	GPIO10	GPIO9	GPIO11
3	0x66	GPIO16	GPIO13	GPIO12	GPIO29

Table 7-19. Parallel Boot Options

OPTION	BOOTDEF VALUE	D0-D7 GPIO	28x(DSP) CONTROL GPIO	HOST CONTROL GPIO
0 (default)	0x00	D0 - GPIO0	GPIO224	GPIO242
		D1 - GPIO1		
		D2 - GPIO3		
		D3 - GPIO4		
		D4 - GPIO5		
		D5 - GPIO7		
		D6 - GPIO28		
		D7 - GPIO29		
1	0x20	D0 - GPIO0	GPIO12	GPIO13
		D1 - GPIO1		
		D2 - GPIO2		
		D3 - GPIO3		
		D4 - GPIO4		
		D5 - GPIO5		
		D6 - GPIO6		
		D7 - GPIO7		
2	0x40	D0 - GPIO0	GPIO16	GPIO29
		D1 - GPIO1		
		D2 - GPIO2		
		D3 - GPIO3		
		D4 - GPIO4		
		D5 - GPIO5		
		D6 - GPIO6		
		D7 - GPIO7		

7.7 Security

Security features are enforced by the Dual Code Security Module (DCSM). The primary layer of defense is securing the boundary of the chip, which should always be enabled. Additionally, the Dual Zone Security feature is available to support code partitioning.

7.7.1 Securing the Boundary of the Chip

The following two features, along with authentication in the firmware update code, should be used to help to prevent unauthorized code from running on the device.

7.7.1.1 JTAGLOCK

Enabling the JTAGLOCK feature in the USER OTP disables JTAG access (for example, debug probe) to resources on the device.

7.7.1.2 Zero-pin Boot

Enabling the Zero-pin Boot option along with Flash Boot in the USER OTP blocks all pin-based external bootloader options (for example, SCI, CAN, Parallel).

7.7.2 Dual-Zone Security

The dual-zone security mechanism offers protection for two zones: Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both zones is identical. Each zone has its own dedicated secure resource (OTP memory and secure ROM) and allocated secure resource (LSx RAM and flash sectors).

7.7.3 Disclaimer

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

7.8 Watchdog

The watchdog module is the same as the one on previous TMS320C2000™ microcontrollers, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backward-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 7-2 shows the various functional blocks within the watchdog module.

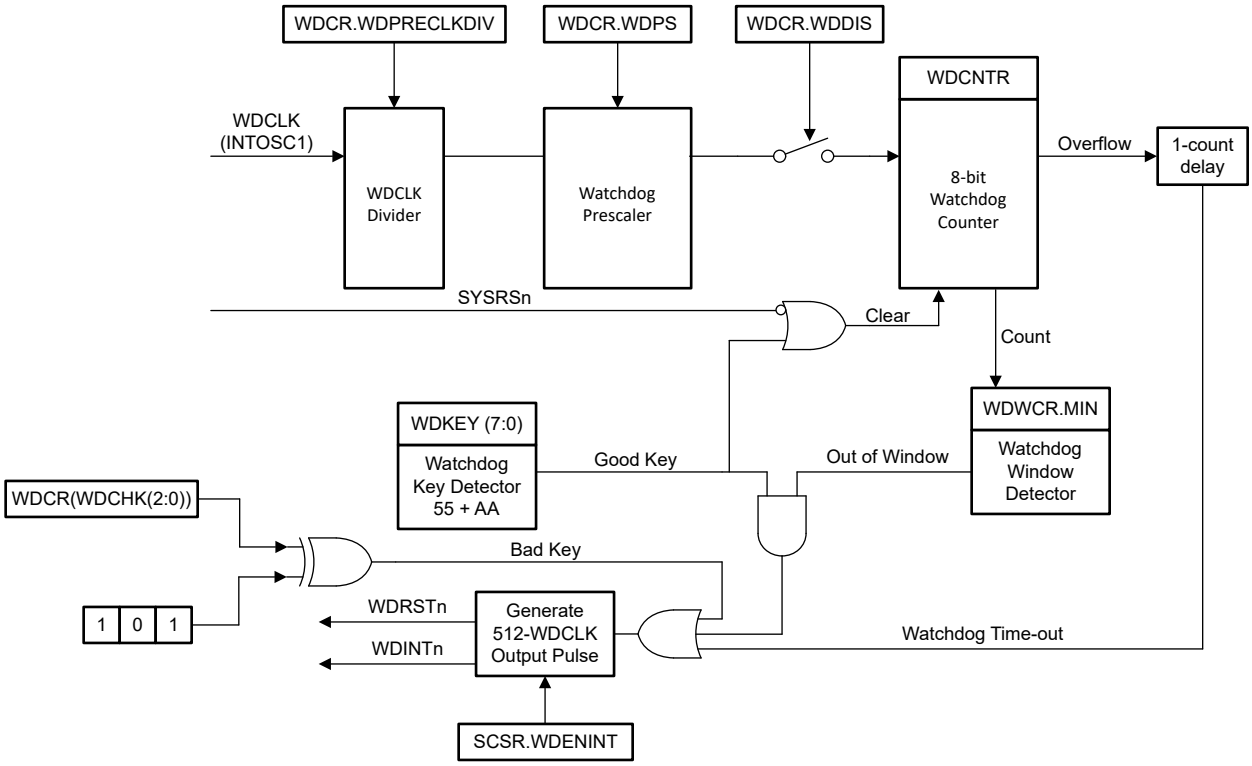


Figure 7-2. Windowed Watchdog

7.9 C28x Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for TI-RTOS. It is connected to INT14 of the CPU. If TI-RTOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLK (default)
- Internal oscillator 1 (INTOSC1)
- Internal oscillator 2 (INTOSC2)
- X1 (XTAL)

7.10 Dual-Clock Comparator (DCC)

The DCC module is used for evaluating and monitoring the clock input based on a second clock, which can be a more accurate and reliable version. This instrumentation is used to detect faults in clock source or clock structures, thereby enhancing the system's safety metrics.

7.10.1 Features

The DCC has the following features:

- Allows the application to ensure that a fixed ratio is maintained between frequencies of two clock signals.
- Supports the definition of a programmable tolerance window in terms of the number of reference clock cycles.
- Supports continuous monitoring without requiring application intervention.
- Supports a single-sequence mode for spot measurements.
- Allows the selection of a clock source for each of the counters, resulting in several specific use cases.

7.10.2 Mapping of DCCx Clock Source Inputs

Table 7-20. DCCx Clock Source0 Table

DCCxCLKSRC0[3:0]	CLOCK NAME
0x0	XTAL/X1
0x1	INTOSC1
0x2	INTOSC2
0x4	TCK
0x5	CPU1.SYSCLK
0x8	AUXCLKIN
0xC	INPUT XBAR (Output16 of input-xbar)
others	Reserved

Table 7-21. DCCx Clock Source1 Table

DCCxCLKSRC1[4:0]	CLOCK NAME
0x0	PLLRAWCLK
0x2	INTOSC1
0x3	INTOSC2
0x6	CPU1.SYSCLK
0x9	Input XBAR (Output15 of the input-xbar)
0xA	AUXCLKIN
0xB	EPWMCLK
0xC	LSPCLK
0xD	ADCCLK
0xE	WDCLK
0xF	CAN0BITCLK
others	Reserved

8 Applications, Implementation, and Layout

8.1 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

The *Hardware Design Guide for F2800x C2000™ Real-Time MCU Series Application Note* is an essential guide for hardware developers using C2000 devices, and helps to streamline the design process while mitigating the potential for faulty designs. Key topics discussed include: power requirements; general-purpose input/output (GPIO) connections; analog inputs and ADC; clocking generation and requirements; and JTAG debugging among many others.

8.2 Key Device Features

Table 8-1. Key Device Features

MODULE	FEATURE	SYSTEM BENEFIT
PROCESSING		
Real-time control CPUs	Up to 120 MIPS C28x: 120 MIPS Flash: Up to 256KB RAM : Up to 36KB 32-bit Floating-Point Unit (FPU32) Trigonometric Math Unit (TMU)	TI's 32-bit C28x DSP core provides 120 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. **FPU32:** Native hardware support for IEEE-754 single-precision floating-point operations **TMU:** Accelerators used to speed up execution of trigonometric and arithmetic operations for faster computation (such as PLL and DQ transform) optimized for control applications. TMU helps in achieving faster control loops, resulting in higher efficiency and better component sizing. Special instructions to support nonlinear PID control algorithms
SENSING		
Analog-to-Digital Converter (ADC) (12-bit)	Up to 2 ADC modules 4 MSPS Up to 21 channels	ADC provides precise and concurrent sampling of all three-phase currents and DC bus with zero jitter. ADC post-processing – On-chip hardware reduces ADC ISR complexity and shortens current loop cycles More ADCs help in multiphase applications. Provide better effective MSPS (oversampling) and typical ENOB for better control-loop performance.

Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
Comparator Subsystem (CMPSS)	**CMPSS** 1 windowed comparator Dual 12-bit DACs DAC ramp generation Low DAC output on external pin Digital filters 60-ns detection to trip time Slope compensation	**System protection without false alarms:** Comparator Subsystem (CMPSS) modules are useful for applications such as peak-current mode control, switched-mode power, power factor correction, and voltage trip monitoring. PWM trip-triggering and removal of unwanted noise are easy with blanking window and filtering features provided with the analog comparator subsystems. Provides better control accuracy. No need for further CPU configuration to control the PWM with the Comparator and 12-bit DAC (CMPSS) and 9.5-bit effective reference DAC for CMPSS_LITE. Enables protection and control using the same pin.
	CMPSS_LITE 3 windowed comparators Dual 9.5-bit effective reference DACs Digital filters 40-ns detection to trip time Slope compensation	
Enhanced Quadrature Encoder Pulse (eQEP)	1 eQEP module	Used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine used in a high-performance motion and position-control system. Also can be used in other applications to count input pulses from an external device (such as a sensor).
Enhanced Capture (eCAP)	2 eCAP modules Measures elapsed time between events (up to 4 time-stamped events). Connects to any GPIO through the input X-BAR. When not used in capture mode, the eCAP module can be configured as a single-channel PWM output (APWM).	**Applications for eCAP include:** Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors) Elapsed time measurements between position sensor pulses Period and duty cycle measurements of pulse train signals Decoding current or voltage amplitude derived from duty-cycle encoded current/voltage sensors

Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
ACTUATION		
Enhanced Pulse Width Modulation (ePWM)	Up to 14 ePWM channels Ability to generate high-side/low-side PWMs with deadband Supports Valley switching (ability to switch PWM output at valley point) and features like blanking window	Flexible PWM waveform generation with best power topology coverage. Shadowed deadband and shadowed action qualifier enable adaptive PWM generation and protection for improved control accuracy and reduced power loss. Enables improvement in Power Factor (PF) and Total Harmonic Distortion (THD), which is especially relevant in Power Factor Correction (PFC) applications. Improves light load efficiency.
	One-shot and global reload feature	Critical for variable frequency and multiphase DC-DC applications and helps in attaining high-frequency control loops (>2 MHz). Enables control of interleaved LLC topologies at high frequencies
	Independent PWM action on a Cycle-by-Cycle (CBC) trip event and an One-Shot Trip (OST) event	Provides cycle-by-cycle protection and complete shutoff of PWM under fault condition. Helps implement multiphase PFC or DC-DC control.
	Load on SYNC (support for shadow-to-active load on a SYNC event)	Enables variable-frequency applications (allows LLC control in power conversion).
	Ability to shut down the PWMs without software intervention (no ISR latency)	Fast protection under fault condition
	Delayed Trip Functionality	Helps implement the deadband with Peak Current Mode Control (PCMC) Phase-Shifted Full Bride (PSFB) DC-DC easily without occupying much CPU resources (even on trigger events based on comparator, trip, or sync-in events).
	Deadband Generator (DB) submodule	Prevents simultaneous ON conditions of High and Low side gates by adding programmable delay to rising (RED) and falling (FED) PWM signal edges.
	Flexible PWM Phase Relationships and Timer Synchronization	Each ePWM module can be synchronized with other ePWM modules or other peripherals. Keeps PWM edges perfectly in synchronization with each other or with certain events. Supports flexible ADC scheduling with specific sampling window in synchronization with power device switching.
High-Resolution Pulse Width Modulation (HRPWM)	2 channels with high-resolution capability (150 ps) Provides 150-ps steps for duty cycle, period, deadband and phase offsets for 99% greater precision	Beneficial for accurate control and enables better-performance high-frequency power conversion. Achieves cleaner waveforms and avoids oscillations/limit cycle at output.
CONNECTIVITY		
Serial Peripheral Interface (SPI)	1 high-speed SPI port	Supports 30 MHz
Serial Communication Interface (SCI)	3 SCI (UART) modules	Interfaces with controllers
Controller Area Network (CAN)	1 CAN module	Provides compatibility with classic CAN modules
Inter-Integrated Circuit (I2C)	2 I2C modules	Interfaces with external EEPROMs, sensors, or controllers

Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
OTHER SYSTEM FEATURES		
Security enhancers	Dual-zone Code Security Module (DCSM) Watchdog Write Protection on Register Missing Clock Detection Logic (MCD) Error Correction Code (ECC) and parity Dual-Clock Comparator (DCC)	**DCSM:** Prevents duplication and reverse-engineering of proprietary code **Watchdog:** Generates reset if CPU gets stuck into endless loop of execution **Write Protection on Registers:** LOCK protection on system configuration registers Protection against spurious CPU writes **MCD:** Automatic clock failure detection **ECC and parity:** Single-bit error correction and double-bit error detection **DCC:** Used to detect faults in clock source
Crossbars (XBARs)	Provides flexibility to connect device inputs, outputs, and internal resources in a variety of configurations. • Input X-BAR • Output X-BAR • ePWM X-BAR	**Enhances hardware design versatility:** **Input X-BAR:** Routes signals from any GPIO to multiple IP blocks within the chip **Output XBAR:** Routes internal signals onto designated GPIO pins **ePWM X-BAR:** Routes internal signals from various IP blocks to EPWM

8.3 Application Information

8.3.1 Typical Applications

The *Typical Applications* section details some applications of this device. For a more extensive list of applications, see the Section 2 of this data sheet.

8.3.1.1 Air-conditioner Outdoor Unit

Air-conditioner outdoor unit design considerations include maximizing power efficiency; minimizing acoustics; and cost. Variable-speed air-conditioners enable continuous temperature regulation and are more efficient than fixed-speed air-conditioners. The air-conditioner's outdoor unit (ODU) consists of a power factor correction (PFC) stage, compressor motor drive, and fan motor drive. A sensorless Field-Oriented Control (FOC)-based Permanent Magnet Synchronous Motor (PMSM) drive is used in the ODU compressor and fan motors to control motor speed and torque by varying the input frequency and voltage of the motors. PFC ensures that the current waveform follows the voltage waveform, improving the line-side power factor, and regulates the output DC voltage to a constant value, regardless of any changes in load or input conditions.

8.3.1.1.1 System Block Diagram

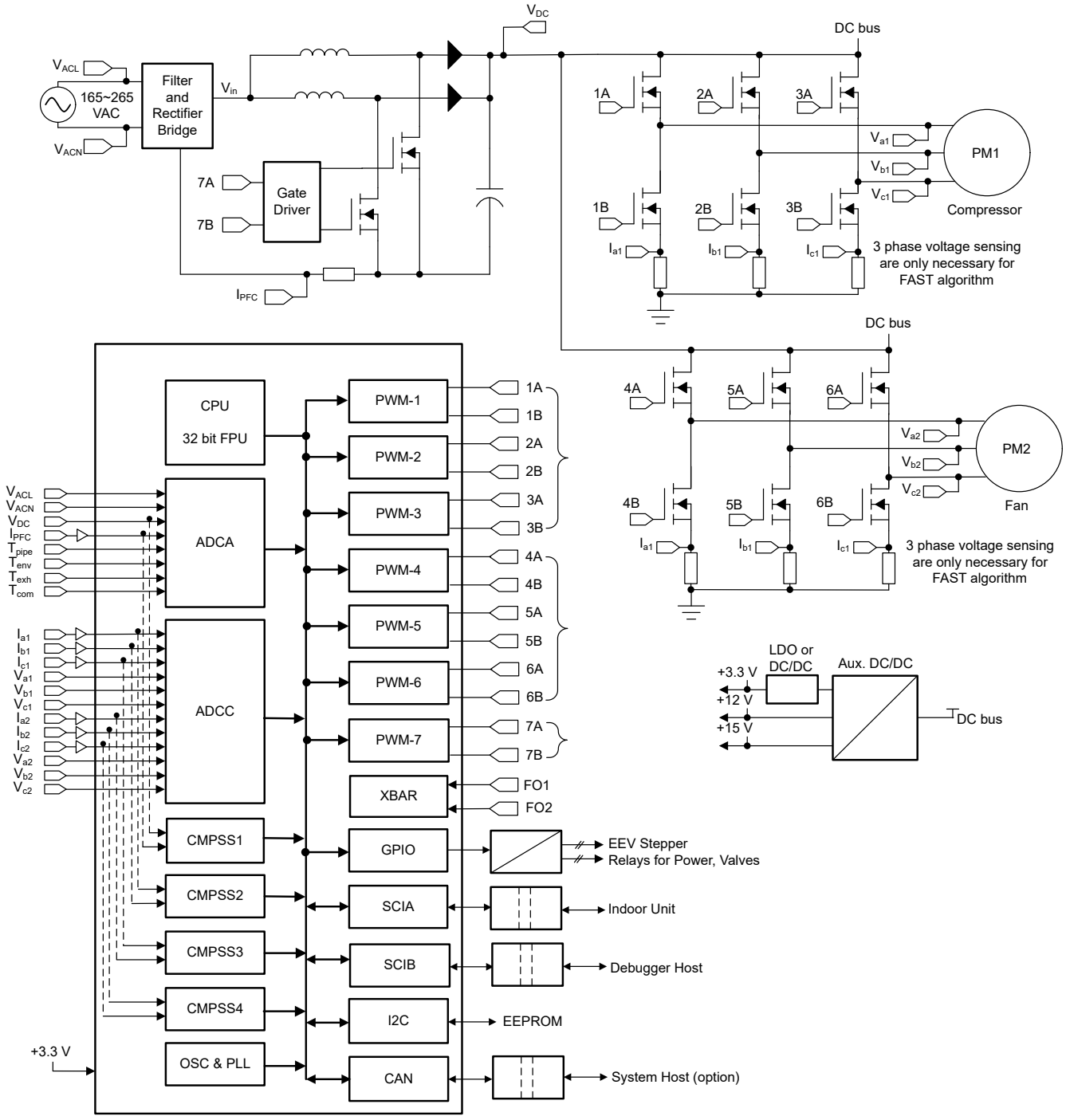


Figure 8-1. Typical Variable-Frequency Air-Conditioner with Dual-Motor Control Using Three-Shunt Plus Interleave PFC

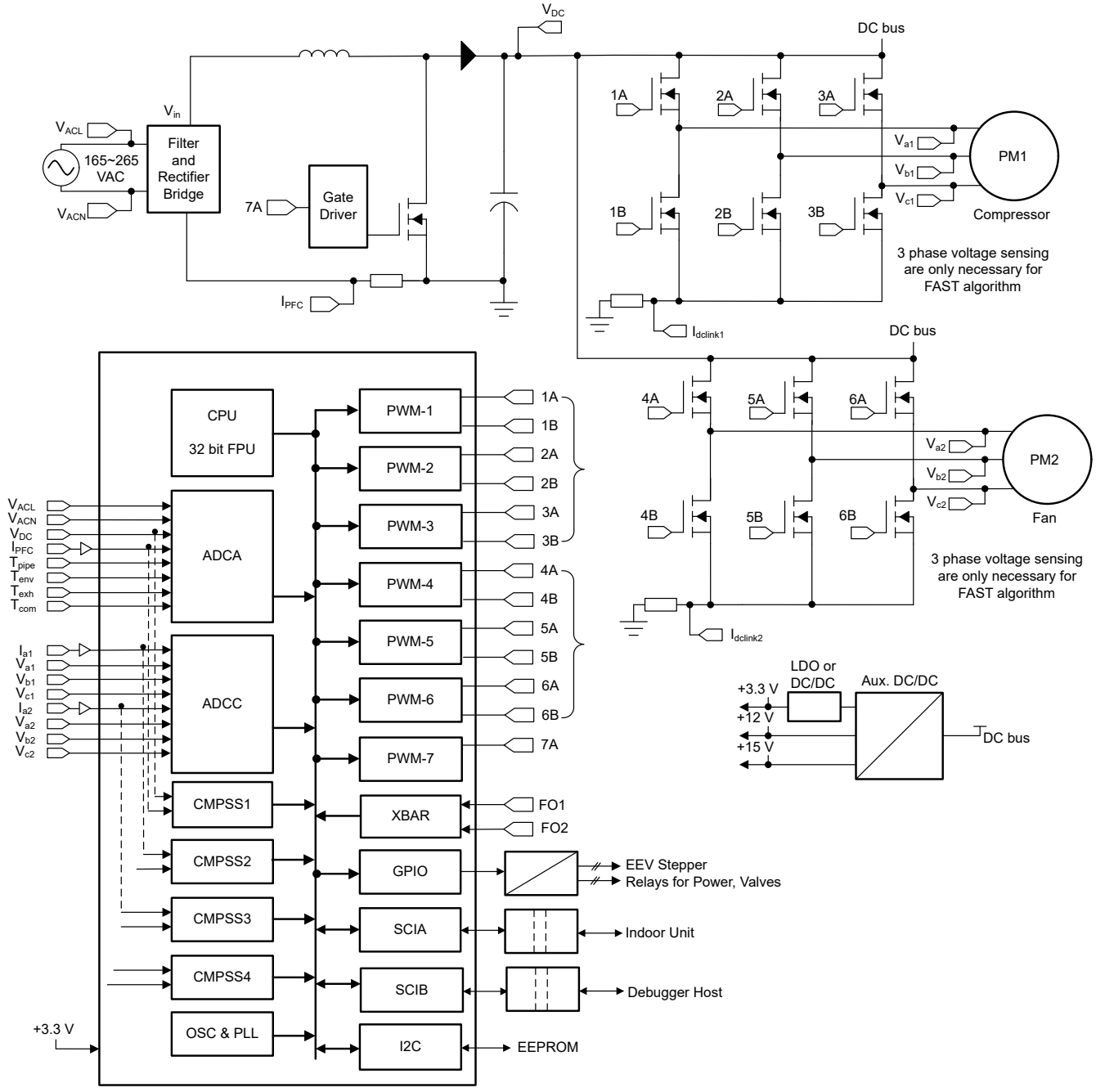


Figure 8-2. Typical Variable-Frequency Air-Conditioner with Dual-Motor Control Using Single Shunt Plus Single-Phase PFC

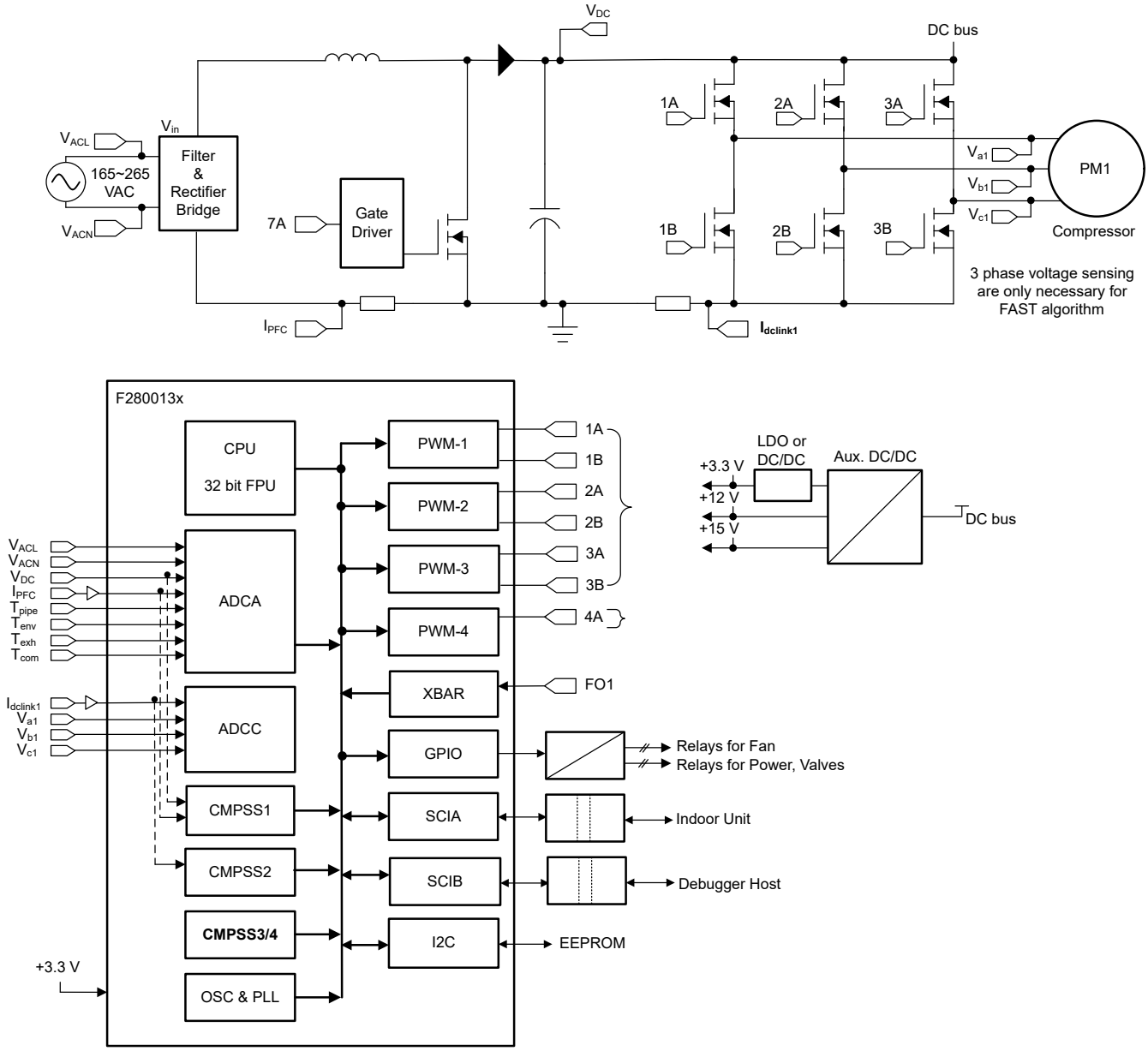


Figure 8-3. Typical Variable-Frequency Air-Conditioner with Single-Motor Control Using Single Shunt Plus Single-Phase PFC

8.3.1.1.2 Air Conditioner Outdoor Unit Resources

Reference Designs and Associated Training Videos

TIDM-02010: Dual motor control with digital interleaved PFC for HVAC reference design

The TIDM-02010 reference design is a 1.5-kW dual-motor drive and power factor correction (PFC) control reference design for a variable-frequency air-conditioner outdoor unit controller in HVAC applications. This reference design illustrates a method to implement sensorless 3-phase PMSM vector control for compressor and fan motor drive, and digital interleaved boost PFC for meeting new efficiency standards with a single C2000™ microcontroller. The hardware and software available with this reference design are tested and ready to use to help accelerate development time to market. The reference design includes hardware design files and software codes.

Variable speed air conditioner (HVAC) reference design demo (Video)
This video introduces dual-motor control with interleaved PFC for HVAC application design using a single C2000 MCU. The test results achieved on this reference design are also presented as part of this presentation.

8.3.1.2 Washer and Dryer

Modern washer and dryer systems require powerful motor control with high energy efficiency; low noise and vibration; and full system protection. Furthermore, the motor drive control needs to support variable spin speeds with variable loads to improve washing and drying performance; and to decrease water consumption. C2000 MCUs are powerful real-time controllers that are capable of meeting these needs with sensorless field-oriented control (FOC), allowing for maximum efficiency, maximum motor power, minimum torque ripple, reduction of audible noise, and utilization of the maximum motor torque that is required at motor acceleration during the washer or dryer drum start-up with heavy load. The different washer or dryer types using dual motors or single motor with a single-chip architecture as shown in Figure 8-4, Figure 8-5, and Figure 8-6.

8.3.1.2.1 System Block Diagram

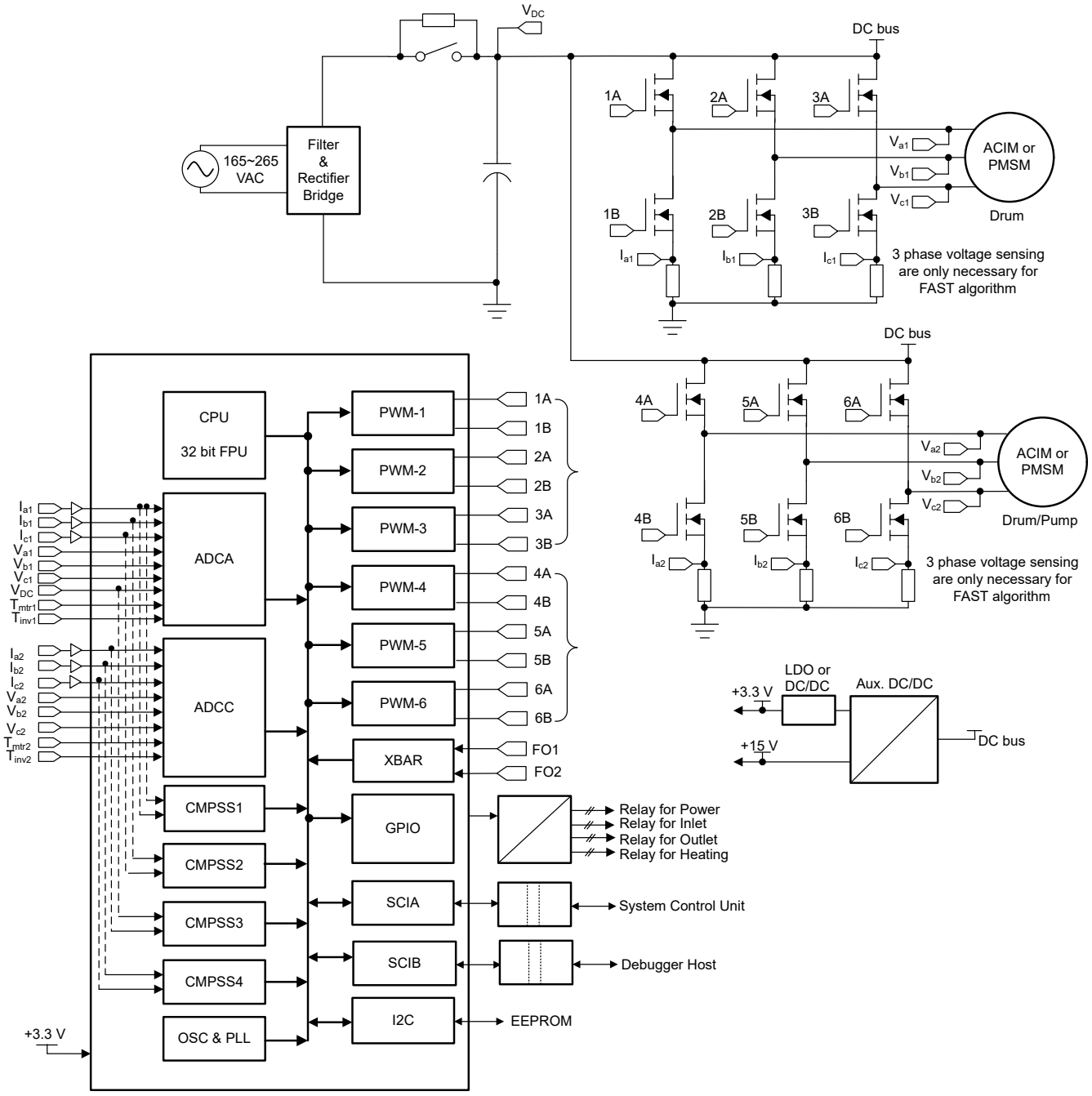


Figure 8-4. Typical Washer and Dryer with Dual-Motor Control Using Three-Shunt Current Sensing

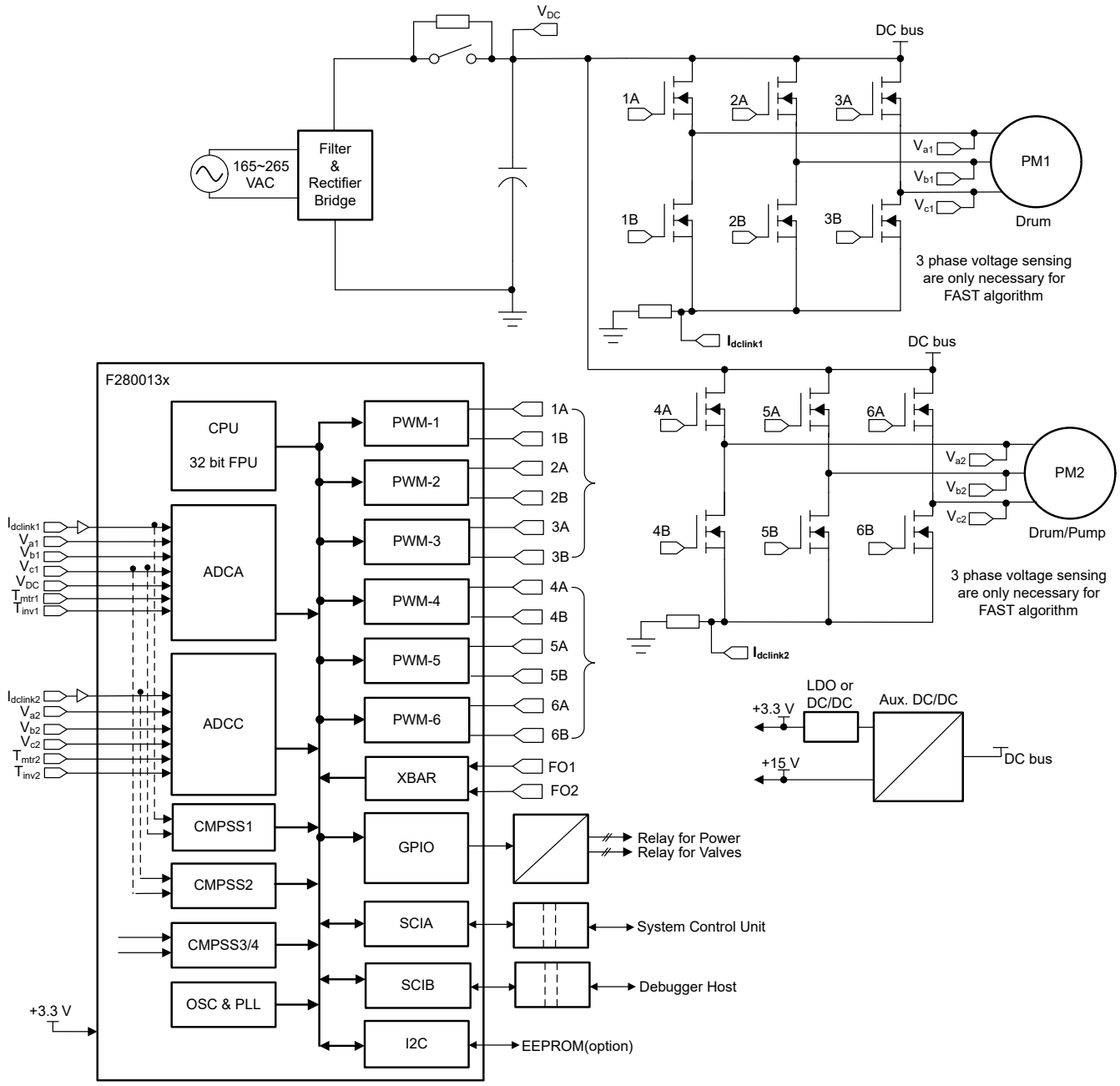


Figure 8-5. Typical Washer and Dryer with Dual-Motor Control Using Single-Shunt Current Sensing

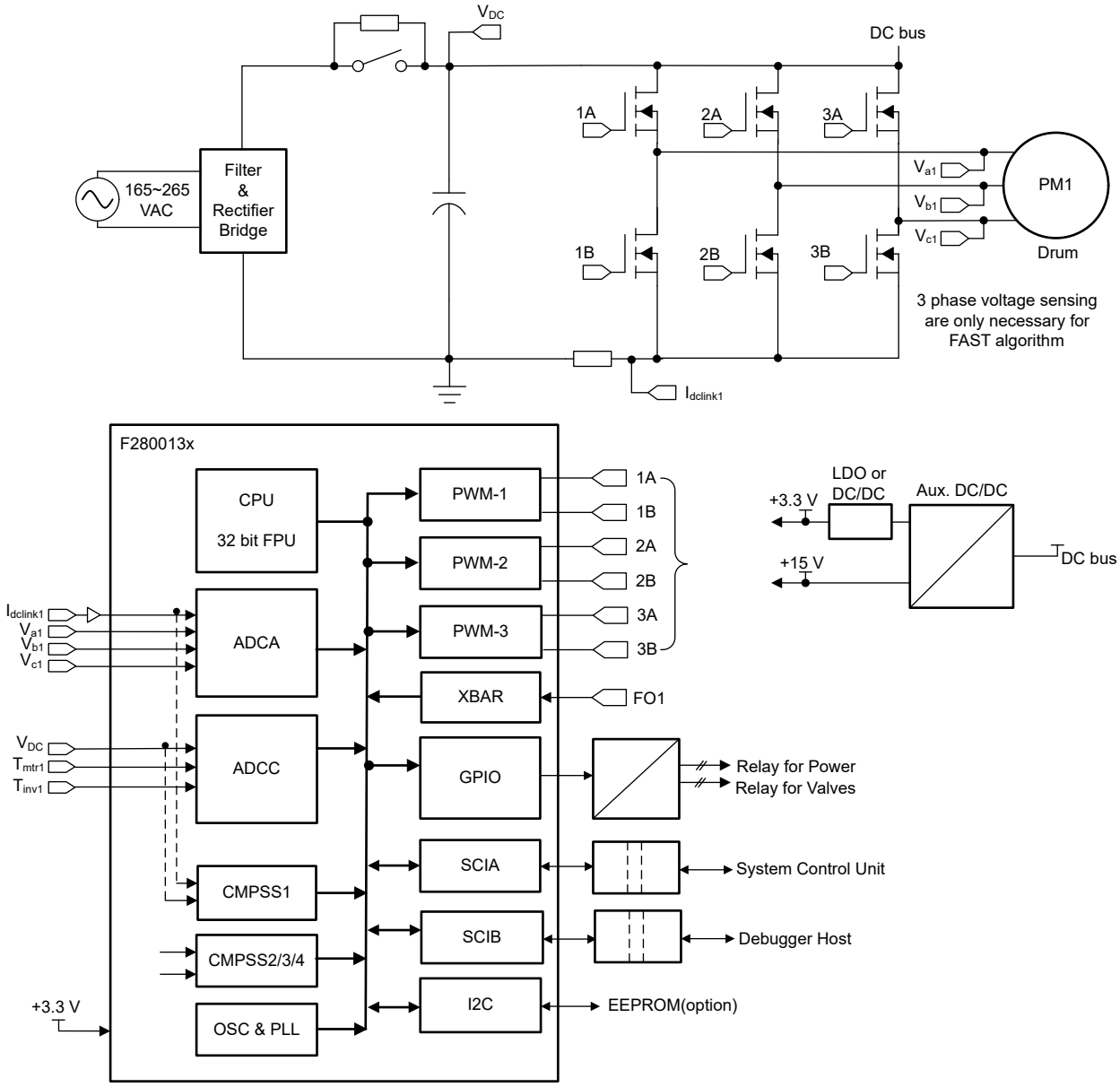


Figure 8-6. Typical Washer and Dryer with One-Motor Control Using Single-Shunt Current Sensing

8.3.1.2.2 Washer and Dryer Resources

Reference Designs and Associated Training Videos

TIDM-02010: Dual motor control with digital interleaved PFC for HVAC reference design

The TIDM-02010 reference design is a 1.5-kW dual-motor drive and power factor correction (PFC) control reference design for a variable-frequency air-conditioner outdoor unit controller in HVAC applications. This reference design illustrates a method to implement sensorless 3-phase PMSM vector control for compressor and fan motor drive, and digital interleaved boost PFC for meeting new efficiency standards with a single C2000™ microcontroller. The hardware and software available with this reference design are tested and ready to use to help accelerate development time to market. The reference design includes hardware design files and software codes.

Universal Motor Control Project and Lab User's Guide
The Universal Motor Control Lab provides an example for motor drive control using a C2000 MCU. This lab is a single project with build examples for different sensorless (FAST™, eSMO, InstaSPIN™-BLDC) and sensored (Incremental Encoder, Hall) motor control techniques (FOC, Trapezoidal). This lab includes system features and debug interfaces that can be used across a variety of three-phase inverter motor evaluation kits or on a customer's own board for washer, dryer, or refrigerator applications. The example codes of this lab are included in the Motor Control Software Development Kit (SDK). The MotorControl SDK (MC SDK) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based motor control system development time targeted for various three-phase motor control applications.

Variable speed air conditioner (HVAC) reference design demo (Video)
This video introduces dual-motor control with interleaved PFC for HVAC application design using a single C2000 MCU. The test results achieved on this reference design are also presented as part of this presentation.

8.3.1.3 Robotic Lawn Mower

Robotic lawn mower systems have multiple low-voltage battery-powered motors that need to be controlled precisely for drivetrain, cutting, and auxiliary functions. Motor efficiency is important to extend use time and precision operation allows for autonomous operation when required. C2000 MCUs are powerful real-time controllers that are capable of meeting these needs with sensorless or sensor-based field-oriented control (FOC), allowing for maximum efficiency, maximum motor power, minimum torque ripple, reduction of audible noise, and utilization of the maximum motor torque that is required during start-up with heavy load. C2000 devices can be used for multiaxis drivetrain control, cutting blades, and auxiliary functions like lifts, pumps, or blowers.

8.3.1.3.1 System Block Diagram

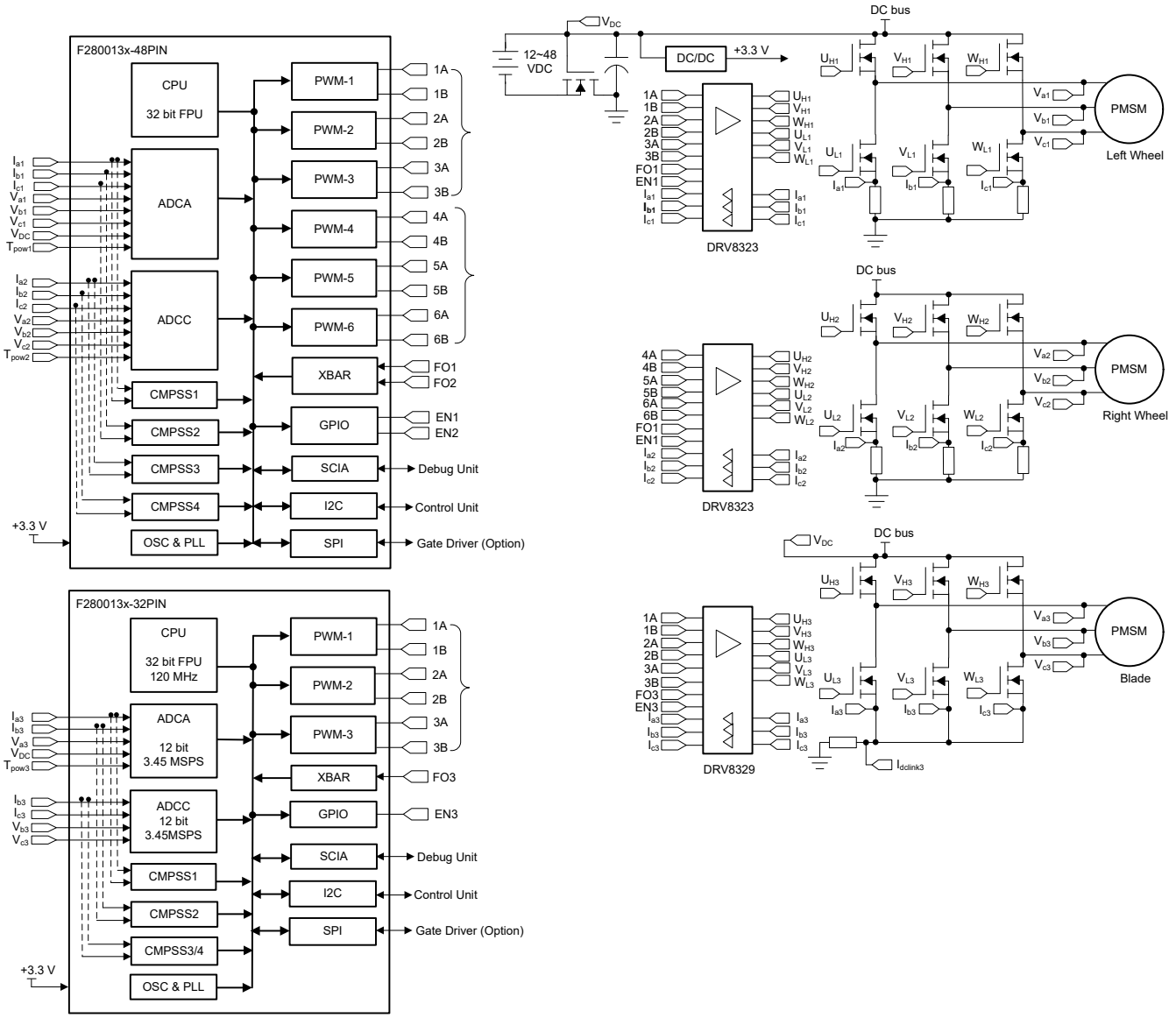


Figure 8-7. Dual-Chip Solution for Robotic Lawn Mower

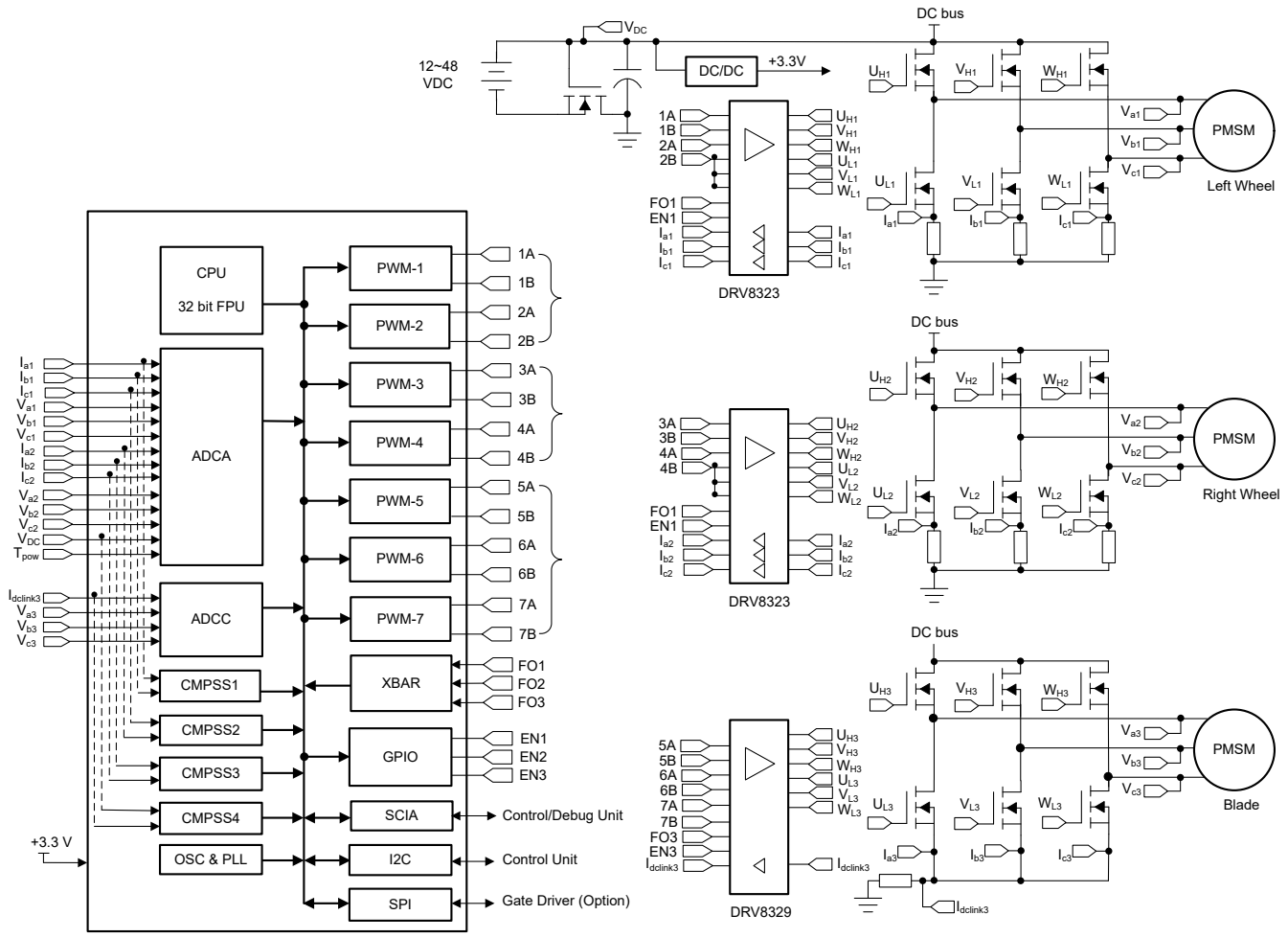


Figure 8-8. Single-Chip Solution for Robotic Lawn Mower

8.3.1.3.2 Robotic Lawn Mower Resources

Reference Designs and Associated Training Videos

Dual-Axis Motor Control Using FCL and SFRA On a Single C2000™ MCU Application Report
This design guide helps to evaluate the fast current loop (FCL) algorithm for high-bandwidth inner loop current control of dual-axis PM servo drives based on a single C2000 MCUs using TI's LaunchPad kit and inverter BoosterPack kit. The examples codes of this reference design is included in Motor Control Software Development Kit.

Quick Response Control of PMSM Using Fast Current Loop Application Report
This reference helps to evaluate fast current loop (FCL) for high bandwidth current loop control of PM servo drives and its frequency response analysis using C2000 MCUs. The examples codes of this reference design is included in Motor Control Software Development Kit.

Universal Motor Control Project and Lab User's Guide
The Universal Motor Control Lab provides an example for motor drive control using a C2000 MCU. This lab is a single project with build examples for different sensorless (FAST™, eSMO, InstaSPIN™-BLDC) and sensored (Incremental Encoder, Hall) motor control techniques (FOC, Trapezoidal). This lab includes system features and debug interfaces that can be used across a variety of three-phase inverter motor evaluation kits or on a customer's own board for washer, dryer, or refrigerator applications. The example codes of this lab are included in the Motor Control Software Development Kit (SDK). The MotorControl SDK (MC SDK) is a cohesive set of

software infrastructure, tools, and documentation designed to minimize C2000 MCU-based motor control system development time targeted for various three-phase motor control applications.

8.3.1.4 Merchant Telecom Rectifiers

Merchant telecom rectifier consists of a power factor correction (PFC) stage and a DC-DC converter stage. The Totem pole PFC is widely used as the PFC stage. For the DC-DC stage, LLC and phase-shifted full bridge (PSFB) are the two most popular topologies. Single-chip and two-chip architecture can be used in merchant telecom rectifier, as shown in Figure 8-9 and Figure 8-10.

The PFC stage draws sine-wave current from the AC mains in phase with the AC voltage, and maintains a steady DC bus voltage (VDC, typically +400 V) across its output. This output voltage is applied to the input of DC-DC stage, which converts it to an isolated low-output voltage Vout (usually 48 V).

8.3.1.4.1 System Block Diagram

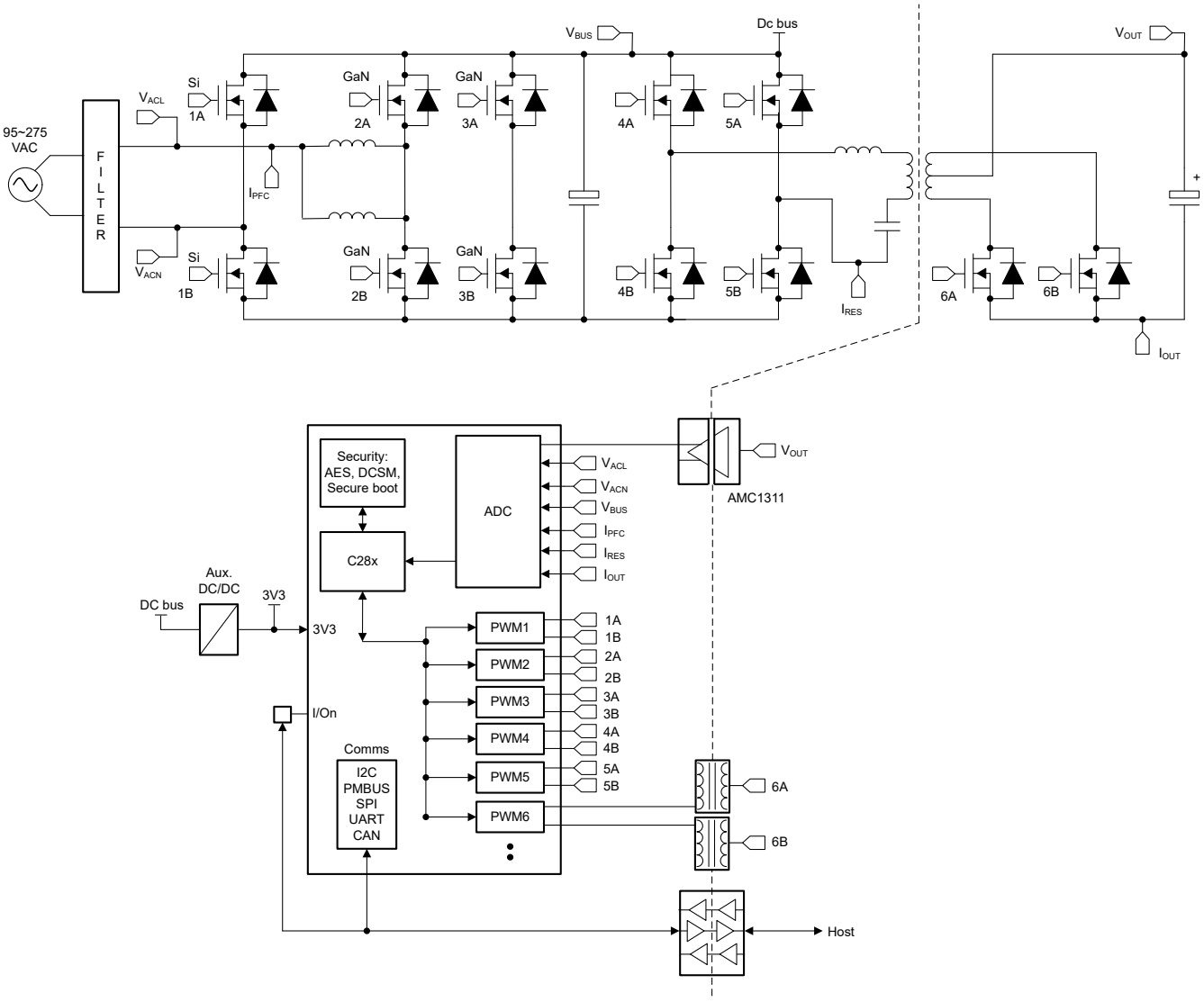


Figure 8-9. Merchant Telecom Rectifier Single-chip Architecture

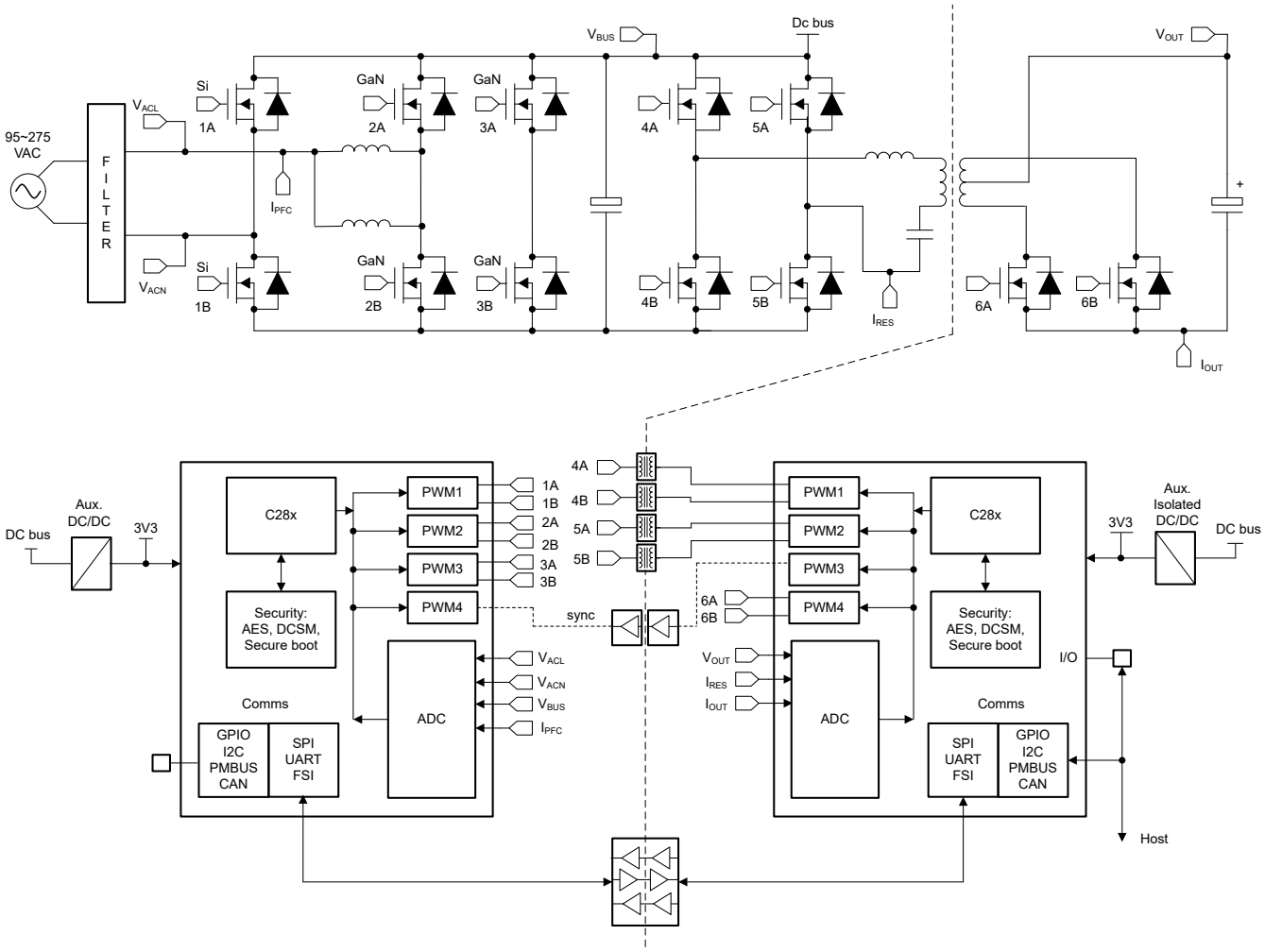


Figure 8-10. Merchant Telecom Rectifier Dual-chip Architecture

8.3.1.4.2 Merchant Telecom Rectifiers Resources

Reference Designs and Associated Training Videos

1-kW reference design with CCM totem pole PFC and current-mode LLC realized by C2000™ and GaN
This reference design demonstrates a hybrid hysteresis control (HHC) method, a kind of current-mode control method on half-bridge LLC stage with a C2000™ F28004x microcontroller. The hardware is based on TIDA-010062, which is 1-kW, 80-Plus titanium, GaN CCM totem pole bridgeless PFC and half-bridge LLC reference design. A separate sensing card is added for hybrid hysteresis control, which recreates the voltage on the resonant capacitor. This HHC LLC stage shows better transient response and ease-of-control loop design compared with the single-loop voltage-mode control method (VMC).

PMP41081 1-kW, 12-V HHC LLC reference design using C2000™ real-time microcontroller
This reference design is a 1-kW, 400-V to 12-V half-bridge resonant DC/DC platform used to evaluate the load transient performance of hybrid-hysteretic control (HHC) with a C2000™ microcontroller.

3-kW phase-shifted full bridge with active clamp reference design with > 270-W/in3 power density
This reference design is a GaN-based 3-kW phase-shifted full bridge (PSFB) targeting maximum power density. The design has an active clamp to minimize voltage stress on the secondary synchronous rectifier MOSFETs enabling use of lower voltage-rating MOSFETs with better figure-of-merit (FoM). PMP23126 uses our 30mΩ GaN on the primary side and silicon MOSFETs on the secondary side. The LMG3522 top-side cooled GaN with

integrated driver and protection enables higher efficiency by maintaining ZVS over a wider range of operation compared to Si MOSFET. The PSFB operates at 100 kHz and achieves a peak efficiency of 97.74%.

PMP41017 3kW two-phase interleaved half-bridge LLC reference design with GaN and C2000™ MCU
This reference design is a 3-kW, two-phase, interleaved half-bridge inductor-inductor-capacitor (LLC) using the LMG3422 and C2000™ devices.

Digitally Controlled High Efficiency and High Power Density PFC Circuits - Part 2 (Video)
This presentation will introduce two bridgeless PFC designs using C2000 MCU. TI high voltage GaN is used to implement a 3.3kW interleaved CCM totem-pole PFC and a 1.6kW interleaved TRM totem-pole PFC designs. Detailed design considerations are provided to minimize switching loss, current crossover distortion, input current THD and improve efficiency and PF.

TIDA-010203 High efficiency PFC stage using GaN and C2000™ Real-time control MCUs (Video)
GaN power FETs and C2000™ MCUs enable a totem-pole Power Factor Correction (PFC) topology, eliminating bridge rectifier power losses.

TIDA-010062 1-kW, 80 Plus titanium, GaN CCM totem pole bridgeless PFC and half-bridge LLC reference design
This reference design is a digitally controlled, compact 1-kW AC/DC power supply design for server power supply unit (PSU) and telecom rectifier applications. The highly efficient design supports two main power stages, including a front-end continuous conduction mode (CCM) totem-pole bridgeless power factor correction (PFC) stage. The PFC stage features an LMG341x GaN FET with integrated driver to provide enhanced efficiency across a wide load range and meet 80-plus titanium requirements. The design also supports a half-bridge LLC isolated DC/DC stage to achieve a +12-V DC output at 1-kW. Two control cards use C2000™ Entry-Performance MCUs to control both power stages.

TIDA-010203 4-kW single-phase totem pole PFC reference design with C2000 and GaN
This reference design is a 4-kW CCM totem-pole PFC with a F280049/F280025 control card and an LMG342x EVM board. This design demonstrates a robust PFC solution, which avoids isolated current sense by putting the controller's ground in the middle of a MOSFET leg. Benefitting from non-isolation, AC current sense can be implemented by high-speed amplifier OPA607, helping to realize reliable overcurrent protection. In this design, efficiency, thermal image, AC drop, lighting surge, and EMI CE are fully validated. With completed test data, this reference design shows the maturity of totem-pole PFC with C2000 and GaN, and is a good study platform for high-efficiency products' PFC stage design.

TIDM-1001 Two Phase Interleaved LLC Resonant Converter Reference Design Using C2000™ MCUs
Resonant converters are popular DC-DC converters frequently used in server, telecom, automotive, industrial, and other power supply applications. Their high performance (efficiency, power density, etc.), improving requirements of the various industry standards, and the ever-increasing power density goals have made these converters a good choice for medium- to high-power applications. This design implements a digitally controlled 500-W two-phase interleaved LLC resonant converter. The system is controlled by a single C2000™ microcontroller (MCU), TMS320F280025C, which also generates PWM waveforms for all power electronic switching devices under all operating modes. This design implements a novel current-sharing technique to accurately achieve current-balancing between phases.

TIDM-1007 Interleaved CCM Totem Pole PFC Reference Design (Video)
This video covers the hardware aspects, the control aspects, and the software design that are required to control a totem-pole PFC using a C2000 microcontroller. The test results achieved on this reference design are also presented as part of this presentation.

Variable-frequency, ZVS, 5-kW, GaN-based, two-phase totem-pole PFC reference design
This reference design is a high-density and high-efficiency 5-kW totem-pole power factor correction (PFC) design. The design uses a two-phase totem-pole PFC operating with variable frequency and zero voltage switching (ZVS). The control uses a new topology and improved triangular current mode (iTCM) to achieve both small size and high efficiency. The design uses a high performance processing core inside a TMS320F280049C microcontroller to maintain efficiency over a wide operating range. The PFC operates with variable frequency

between 100 kHz and 800 kHz. A peak system efficiency of 99% was achieved with an open-frame power density of 120 W/in3.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Getting Started and Next Steps

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

9.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS**320F2800137). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX and TMDX) through fully qualified production devices and tools (TMS and TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

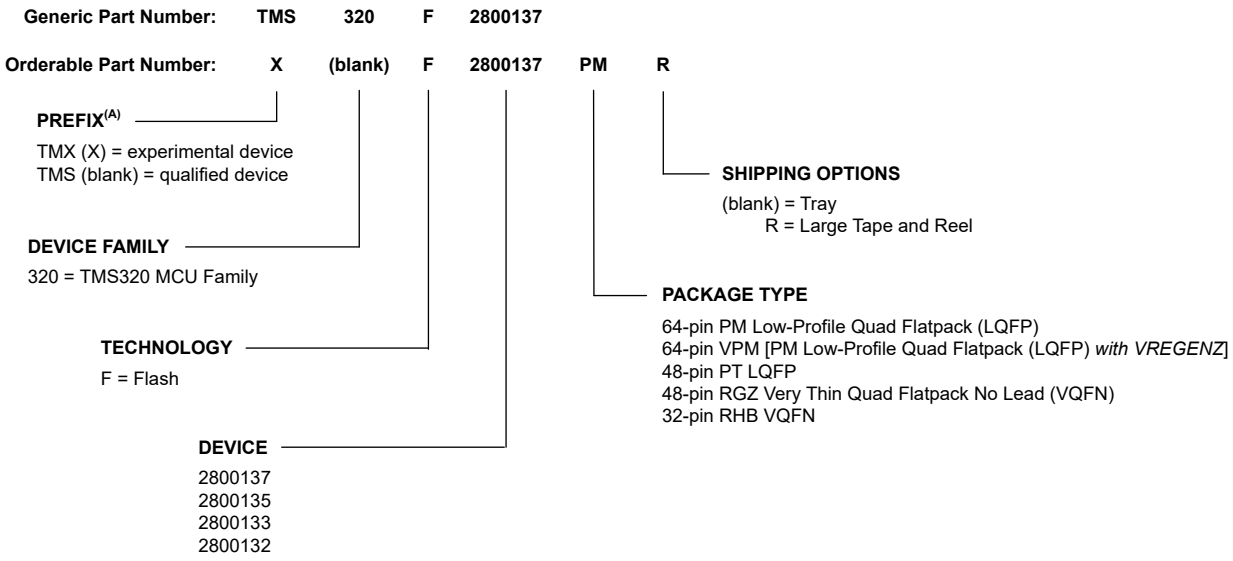
"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PM).

For orderable part numbers of TMS320F280013x devices in the PM, PT, RGZ, and RHB package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

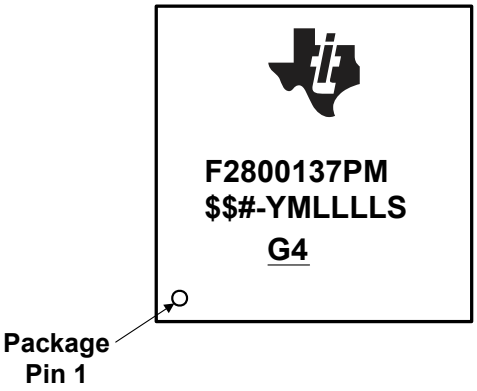


A. Prefix X is used in orderable part numbers.

Figure 9-1. Device Nomenclature

9.3 Markings

Figure 9-2, Figure 9-3, Figure 9-4, and Figure 9-5 show the package symbolization. Table 9-1 lists the silicon revision codes.

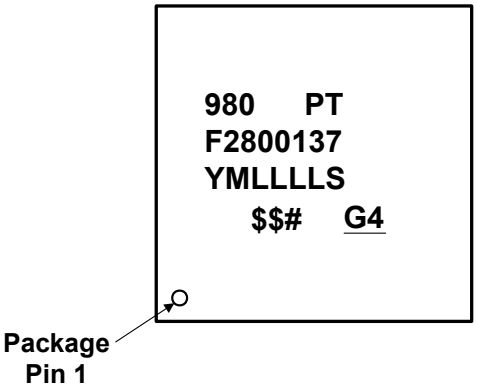


YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
 # = Silicon Revision Code

G4 = ECAT

Figure 9-2. Package Symbolization for PM Package



YMLLLLS = Lot Trace Code

980 = TI EIA Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
 # = Silicon Revision Code

G4 = ECAT

Figure 9-3. Package Symbolization for PT Package

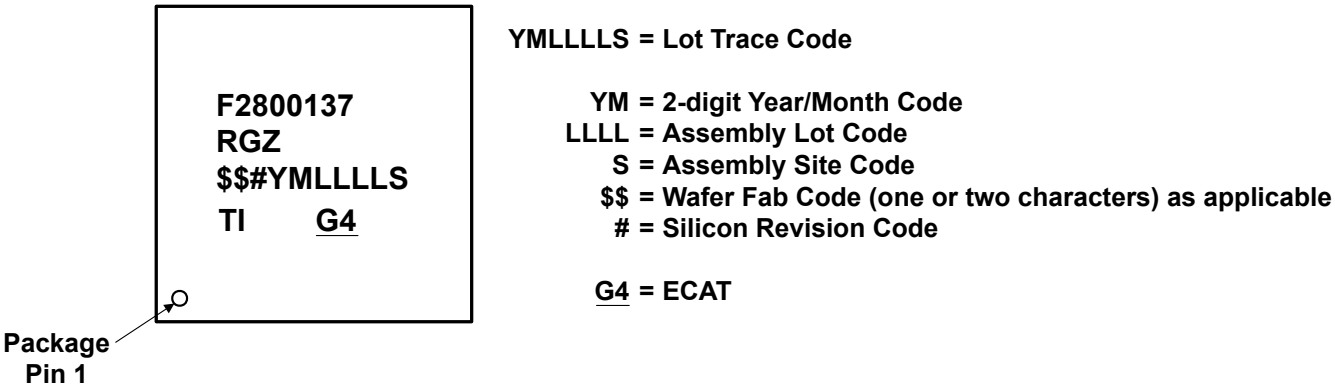


Figure 9-4. Package Symbolization for RGZ Package

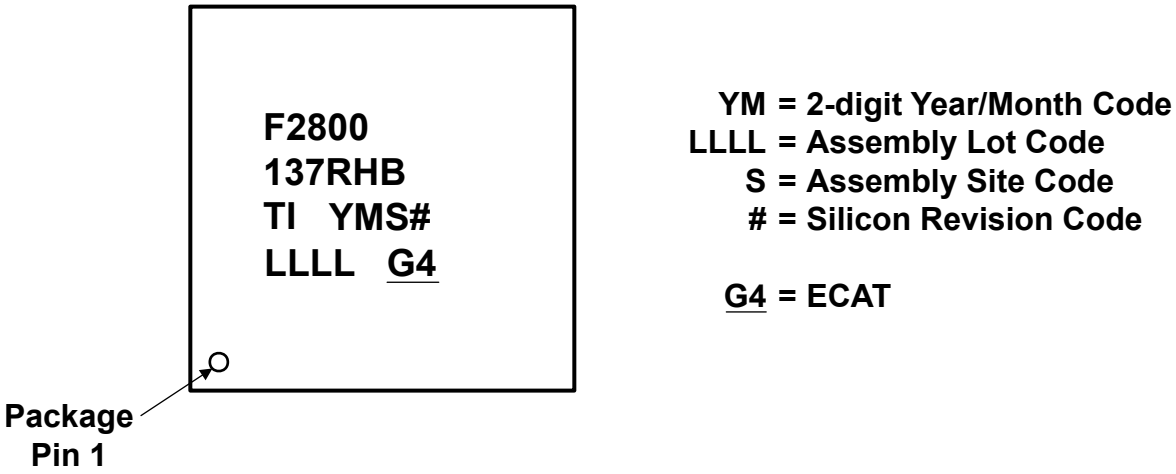


Figure 9-5. Package Symbolization for RHB Package

Table 9-1. Revision Identification

SILICON REVISION CODE	SILICON REVISION	REVID(1) Address: 0x5D00C	COMMENTS
Blank	0	0x0000 0001	This silicon revision is available as TMX.
A	A	0x0000 0002	This silicon revision is available as TMX.
B	B	0x0000 0003	This silicon revision is available as TMS. Revisions B and C are functionally equivalent.
C	C	0x0000 0004	This silicon revision is available as TMS. Revisions B and C are functionally equivalent.

(1) Silicon Revision ID

9.4 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions follow. To view all available tools and software for C2000™ real-time control MCUs, visit the C2000 real-time control MCUs – Design & development page as well as the C2000 software page.

Development Tools

F2800137 controlCARD
The F2800137 controlCARD is an HSEC180 controlCARD-based evaluation and development tool for the C2000™ F280013x series of microcontroller products. controlCARDs are ideal to use for initial evaluation and system prototyping. controlCARDs are complete board-level modules that utilize one of two standard form factors (100-pin DIMM or 180-pin HSEC) to provide a low-profile single-board controller solution. For first evaluation controlCARDs are typically purchased bundled with a baseboard or bundled in an application kit.

LAUNCHXL-F2800137
LAUNCHXL-F2800137 is a low-cost development board for the TI C2000™ Real-Time Controllers F280013x series. Ideal for initial evaluation and prototyping, it provides a standardized and easy-to-use platform to develop your next application. This extended version LaunchPad™ development kit offers extra pins for evaluation and supports the connection of two BoosterPack™ plug-in modules.

TI Resource Explorer
To enhance your experience, be sure to check out the TI Resource Explorer to browse examples, libraries, and documentation for your applications.

Software Tools

C2000Ware for C2000 MCUs
C2000Ware for C2000™ MCUs is a cohesive set of software and documentation created to minimize development time. It includes device-specific drivers, libraries, and peripheral examples.

Digital Power SDK
Digital Power SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based digital power system development time targeted for various AC-DC, DC-DC and DC-AC power supply applications. The software includes firmware that runs on C2000 digital power evaluation modules (EVMs) and TI reference designs, which are targeted for solar, telecom, server, electric vehicle chargers and industrial power delivery applications. Digital Power SDK provides all the needed resources at every stage of development and evaluation in a digital power applications.

Motor Control SDK
Motor Control SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI designs (TIDs), which are targeted for industrial drive and other motor control, Motor Control SDK provides all the needed resources at every stage of development and evaluation for high-performance motor control applications.

Code Composer Studio™ (CCS) Integrated Development Environment (IDE) for C2000 microcontrollers
Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking the user through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SysConfig System configuration tool SysConfig is a comprehensive collection of graphical utilities for configuring pins, peripherals, radios, subsystems, and other components. SysConfig helps you manage, expose and resolve conflicts visually so that you have more time to create differentiated applications. The tool's output includes C header and code files that can be used with software development kit (SDK) examples or used to configure custom software. The SysConfig tool automatically selects the pinmux settings that satisfy the entered requirements. The SysConfig tool is delivered integrated in CCS, as a standalone installer, or can be used via the dev.ti.com cloud tools portal. For more information about the SysConfig system configuration tool, visit the System configuration tool page.

C2000 Third-party search tool TI has partnered with multiple companies to offer a wide range of solutions and services for TI C2000 devices. These companies can accelerate your path to production using C2000 devices. Download this search tool to quickly browse third-party details and find the right third-party to meet your needs.

UniFlash Standalone Flash Tool
UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

Models

Various models are available for download from the product Design & development pages. These models include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the Design tools & simulation section of the Design & development page for each device.

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the C2000™ real-time control MCUs – Support & training site. Additionally, the C2000 Academy course provides new users with a way to ramp quickly with C2000 devices and their many features. This is a great entry point for users getting started with C2000, and is available at the C2000 Academy resource explorer page.

9.5 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral follows.

Errata

TMS320F280013x Real-Time MCUs Silicon Errata describes known advisories on silicon and provides workarounds.

Technical Reference Manual

TMS320F280013x Real-Time Microcontrollers Technical Reference Manual details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the F280013x real-time microcontrollers.

CPU User's Guides

TMS320C28x CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

TMS320C28x Extended Instruction Sets Technical Reference Manual describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

Peripheral Guides

C2000 Real-Time Control Peripherals Reference Guide describes the peripheral reference guides of the 28x DSPs.

Tools Guides

TMS320C28x Assembly Language Tools v22.6.0.LTS User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

TMS320C28x Optimizing C/C++ Compiler v22.6.0.LTS User's Guide describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

Application Reports

The SMT & packaging application notes website lists documentation on TI's surface mount technology (SMT) and application notes on a variety of packaging-related topics.

Semiconductor Packing Methodology describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

Calculating Useful Lifetimes of Embedded Processors provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

An Introduction to IBIS (I/O Buffer Information Specification) Modeling discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures, and future trends.

Serial Flash Programming of C2000™ Microcontrollers discusses using a flash kernel and ROM loaders for serial programming a device.

The Essential Guide for Developing With C2000™ Real-Time Microcontrollers provides a deeper look into the components that differentiate the C2000 Microcontroller Unit (MCU) as it pertains to Real-Time Control Systems.

9.6 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.7 Trademarks

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All trademarks are the property of their respective owners.

9.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.9 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from March 14, 2023 to November 2, 2023 (from Revision A (March 2023) to Revision B (November 2023)) **Page**

- **Global:** Information on the TMS320F2800133 device is now Production Data....1
- *Features* section: Changed Security features under "On-chip memory" feature....1
- *Package Information* table: Added table....2
- *Device Information* table: Deleted TMS320F2800135V row. Added EXTERNAL VOLTAGE REGULATOR column. Added "64 VPM" to PACKAGE OPTIONS column of TMS320F2800135 row....2
- *Device Comparison* table: Deleted "F2800135V" column. 64 VPM package clarified as only package available within "F2800135" column for "External VREG Support Using VREGENZ" row....6
- *Device Comparison* table: Changed "Code security for on-chip flash and RAM" to "Security: JTAGLOCK, Zero-pin boot, Dual-zone security"....6
- *Pin Attributes* table: Changed DESCRIPTION of TDO....8
- *Pin Diagrams* section: Changed figure title from "64-Pin PM Low-Profile Quad Flatpack *with VREGENZ* on F2800135V (Top View)" to "64-Pin PM Low-Profile Quad Flatpack *with VREGENZ* (Top View)"....8
- *Digital Signals* table: Changed DESCRIPTION of TDO....24
- *Digital Inputs and Outputs on ADC Pins (AGPIOs)* section: Changed section....32
- *GPIO and ADC Allocation* table: Changed "F2800135V" to "64 VPM."....38
- *Electrical Characteristics* table: Changed $R_{PULLDOWN}$ MIN, TYP, and MAX values. Changed MIN value from 27 kΩ to 22.66 kΩ. Changed TYP value from 31 kΩ to 31.49 kΩ. Changed MAX value from 37 kΩ to 61.55 kΩ....40
- *Electrical Characteristics* table: Changed R_{PULLUP} MIN, TYP, and MAX values. Changed MIN value from 26 kΩ to 19.89 kΩ. Changed TYP value from 30 kΩ to 29.45 kΩ. Changed MAX value from 38 kΩ to 53.63 kΩ....40
- *ESD Ratings* table: Deleted F2800135V....40
- *Current Consumption Graphs* section: Added section....47
- *External Supervisor Usage* section: Changed VDD Monitoring paragraph....53
- *Delay Blocks* section: Changed section....54
- *VREGENZ* section: Changed section....54
- *VDDIO Decoupling* section: Changed section....54
- *VDD Decoupling* section: Changed section....55
- *Supply Pins Ganging* section: Changed section....55
- *Signal Pins Power Sequence* section: Changed section....55
- *Supply Sequencing Summary and Effects of Violations* section: Changed section....58
- *Recommended Operating Conditions Applicability to the PMM* section: Added section....58
- *System PLL* figure: Changed figure....65
- *Internal Clock Frequencies* table: Changed MIN $t_{c(SYSCLK)}$ from 10 ns to 8.33 ns. Changed MIN $t_{c(LSPCLK)}$ from 10 ns to 8.33 ns....68
- *INTOSC Characteristics* table: Updated table....77
- *RAM Specifications* section: Added section....81
- *ROM Specifications* section: Added section....82
- *ADC Operating Conditions* table: Changed "Sample rate" row. Changed "Sample window duration (set by ACQPS and PERx.SYSCLK)" row....105
- *ADC Performance Per Pin* section: Added section....108
- *ADC Timings in 12-bit Mode* table: Deleted footnote that references the "ADC: DMA Read of State Result" advisory in the *TMS320F280013x Real-Time MCUs Silicon Errata*....112
- *Temperature Sensor Characteristics* table: Updated T_{acc}, Temperature Accuracy....114
- *Comparator Subsystem (CMPSS)* section: Changed first paragraph....115
- *Block Diagrams* section: Added "Each reference 12-bit DAC can be configured to drive a reference voltage into the negative input of the respective comparator" paragraph. Added "Reference DAC Block Diagram" figure....116
- *Buffered Output from CMPx_DACL Electrical Characteristics* table: Deleted reference to "11-bit effective (monotonic response)" footnote from DNL (Differential Non Linearity)....119

- *CMPSS DAC Dynamic Error* section: Added section.....122
- *I2C Electrical Data and Timing* section: Added "A pullup resistor must be chosen to meet the I2C standard timings ..." paragraph to **Note**.....140
- *I2C Timing Requirements* table: Added footnotes.....140
- *Flash Memory Map* table: Deleted F2800135V from PART NUMBER column.....155
- *Security* section: Changed *Dual Code Security Module* section to *Security* section.....170
- *Air Conditioner Outdoor Unit Resources* section: Changed *Reference Designs and Associated Training Videos* section.....180
- *Washer and Dryer Resources* section: Changed *Reference Designs and Associated Training Videos* section.....184
- *Robotic Lawn Mower Resources* section: Changed *Reference Designs and Associated Training Videos* section.....187
- *Merchant Telecom Rectifier Single-chip Architecture* figure: Corrected EPWM labels of lower FETs.....188
- *Merchant Telecom Rectifier Dual-chip Architecture* figure: Corrected EPWM labels of lower FETs.....188
- *Device Nomenclature* figure: Deleted "2800135V" from **DEVICE**. Added "64-pin VPM [PM Low-Profile Quad Flatpack (LQFP) *with VREGENZ*]" to **PACKAGE TYPE**.....192

11 Mechanical, Packaging, and Orderable Information

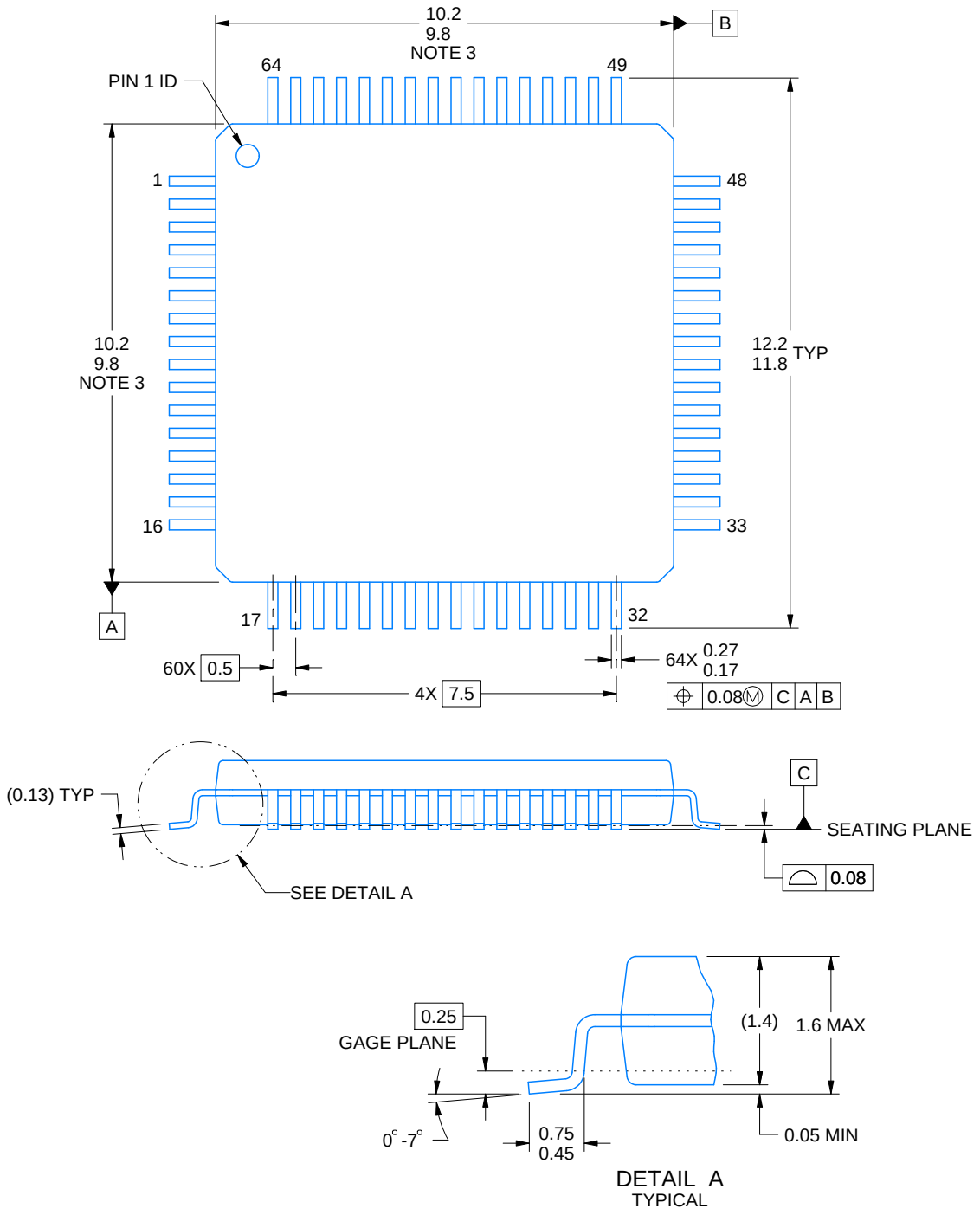
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

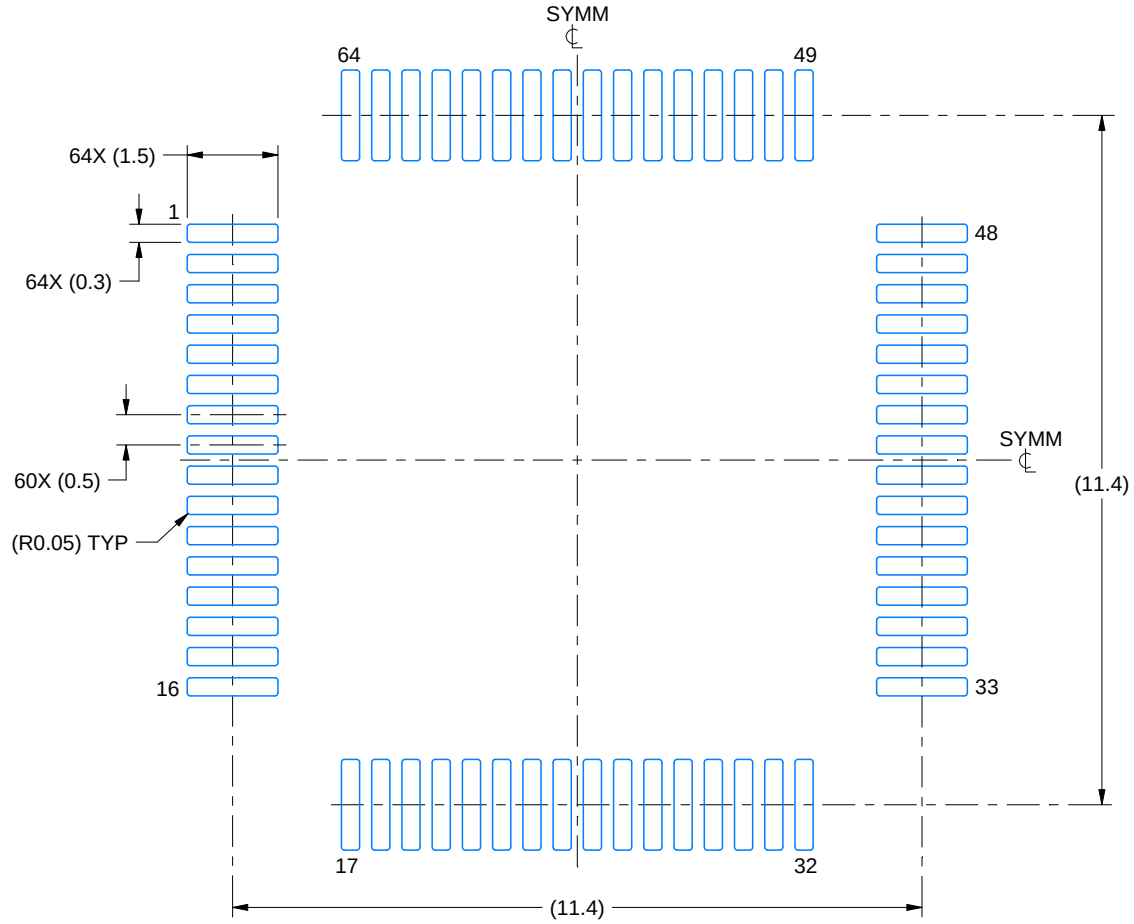
PLASTIC QUAD FLATPACK



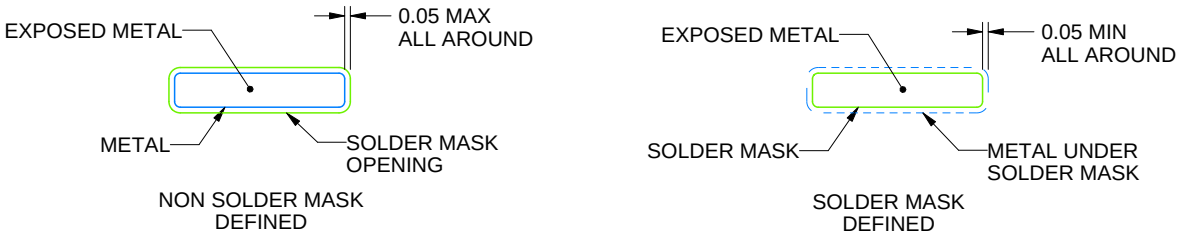
4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

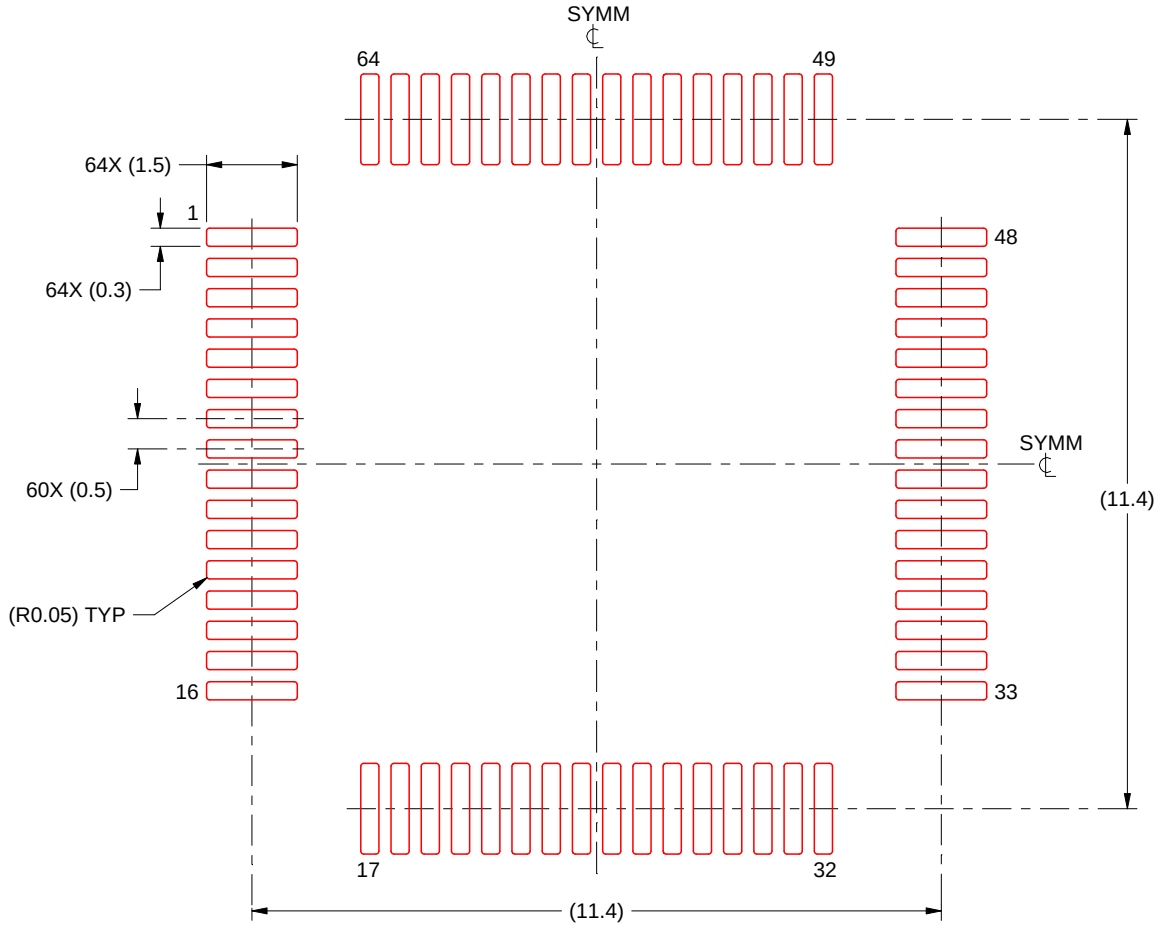


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

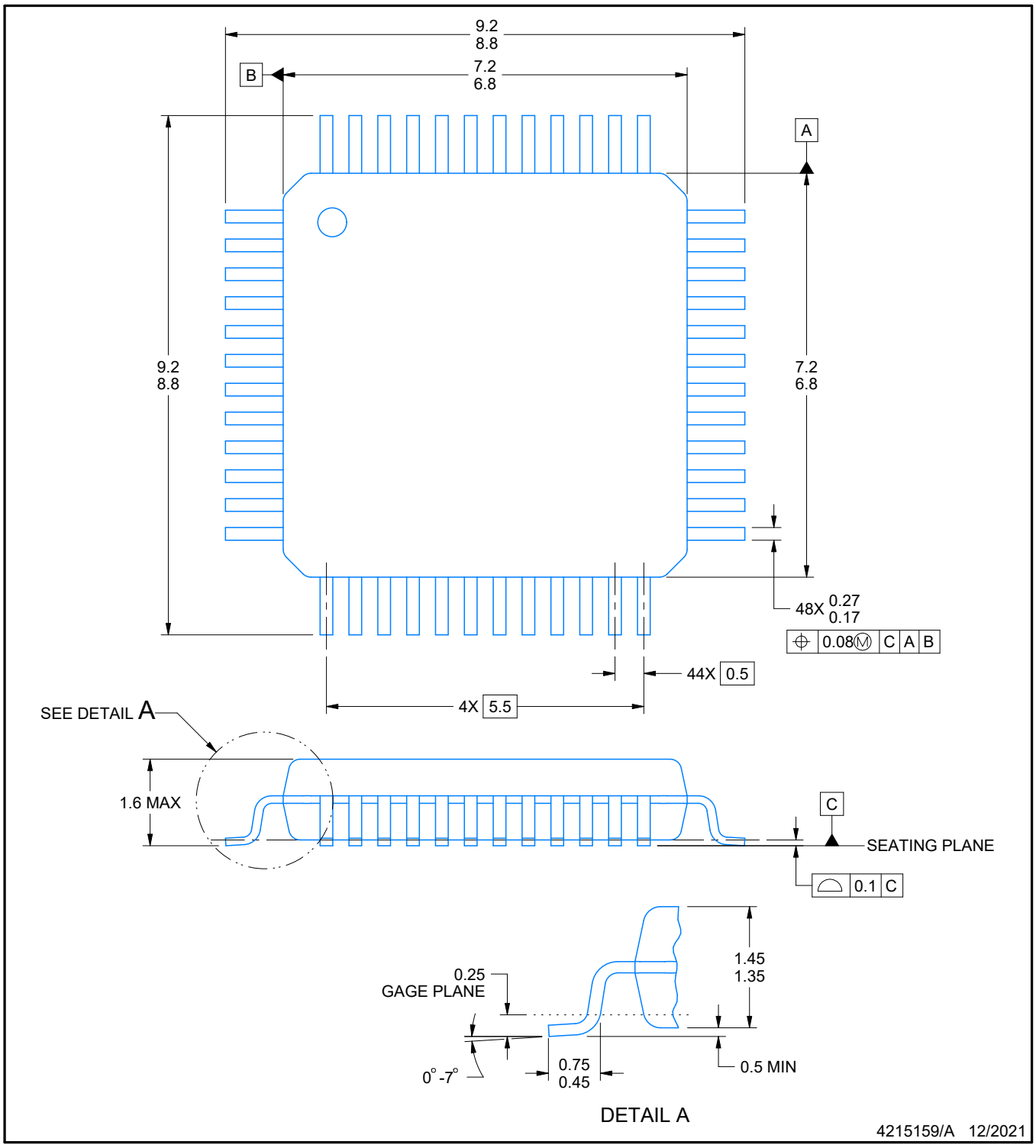
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PT0048A

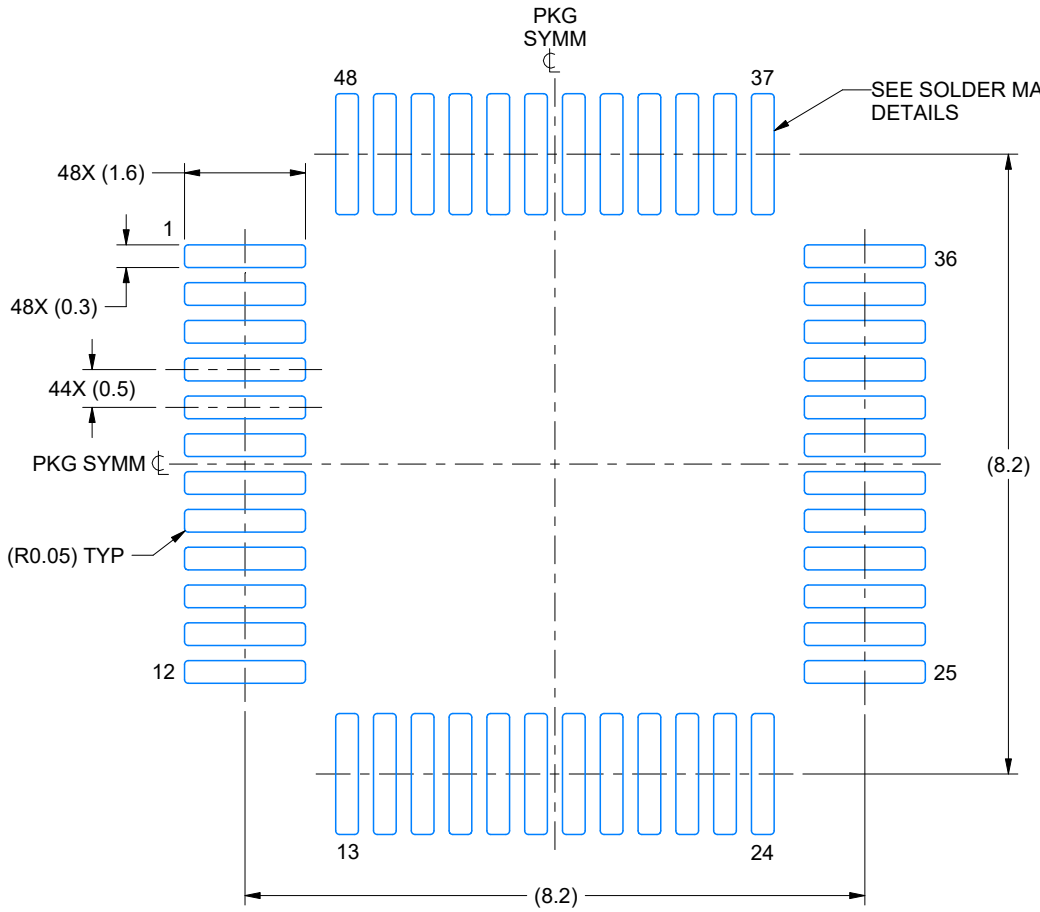
LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK

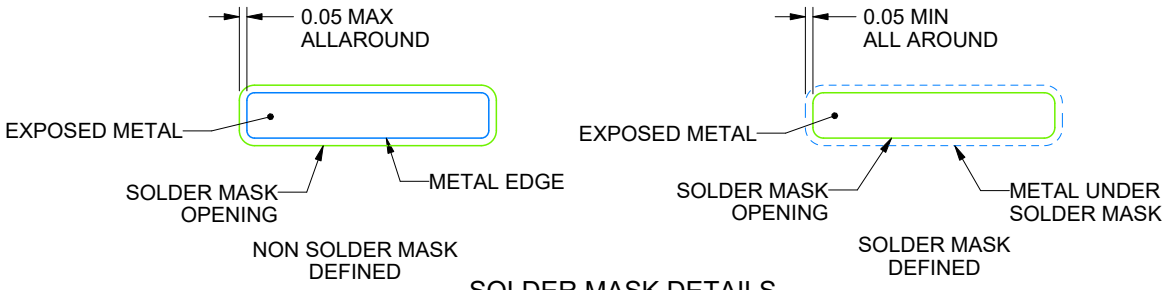


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000

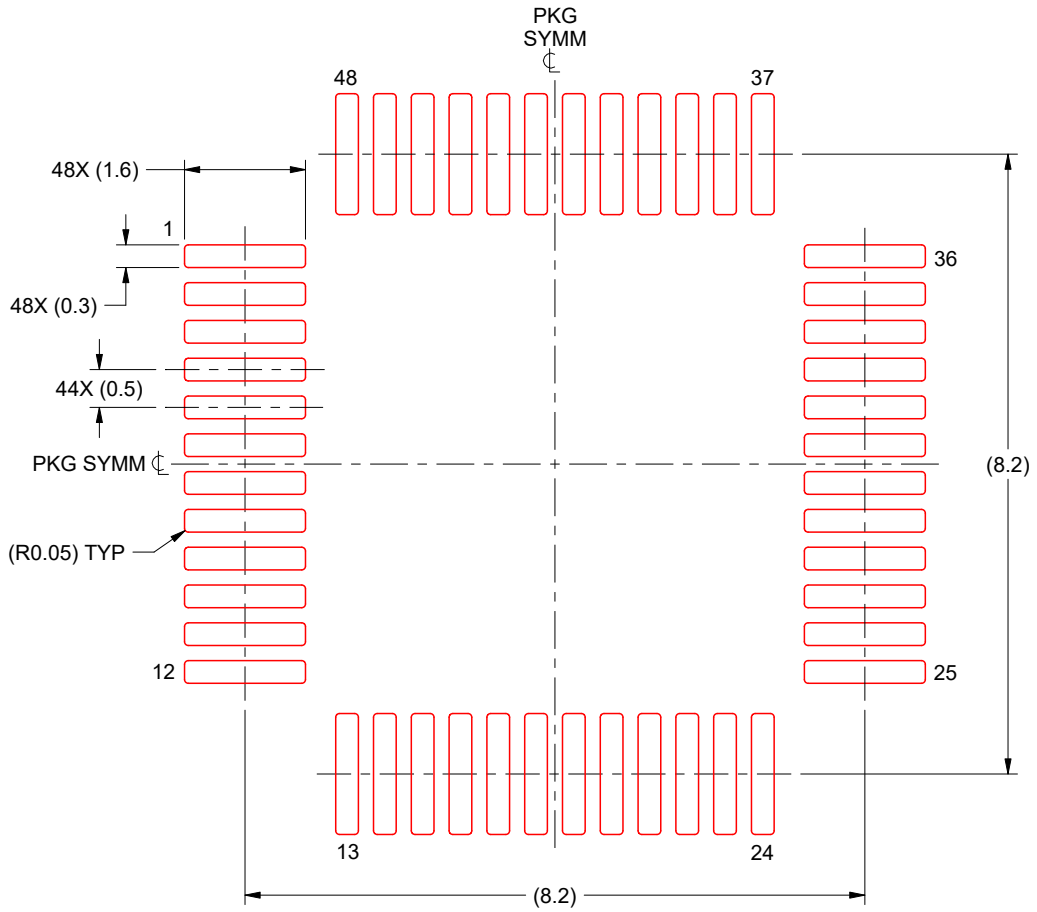


SOLDER MASK DETAILS

4215159/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/A 12/2021

NOTES: (continued)

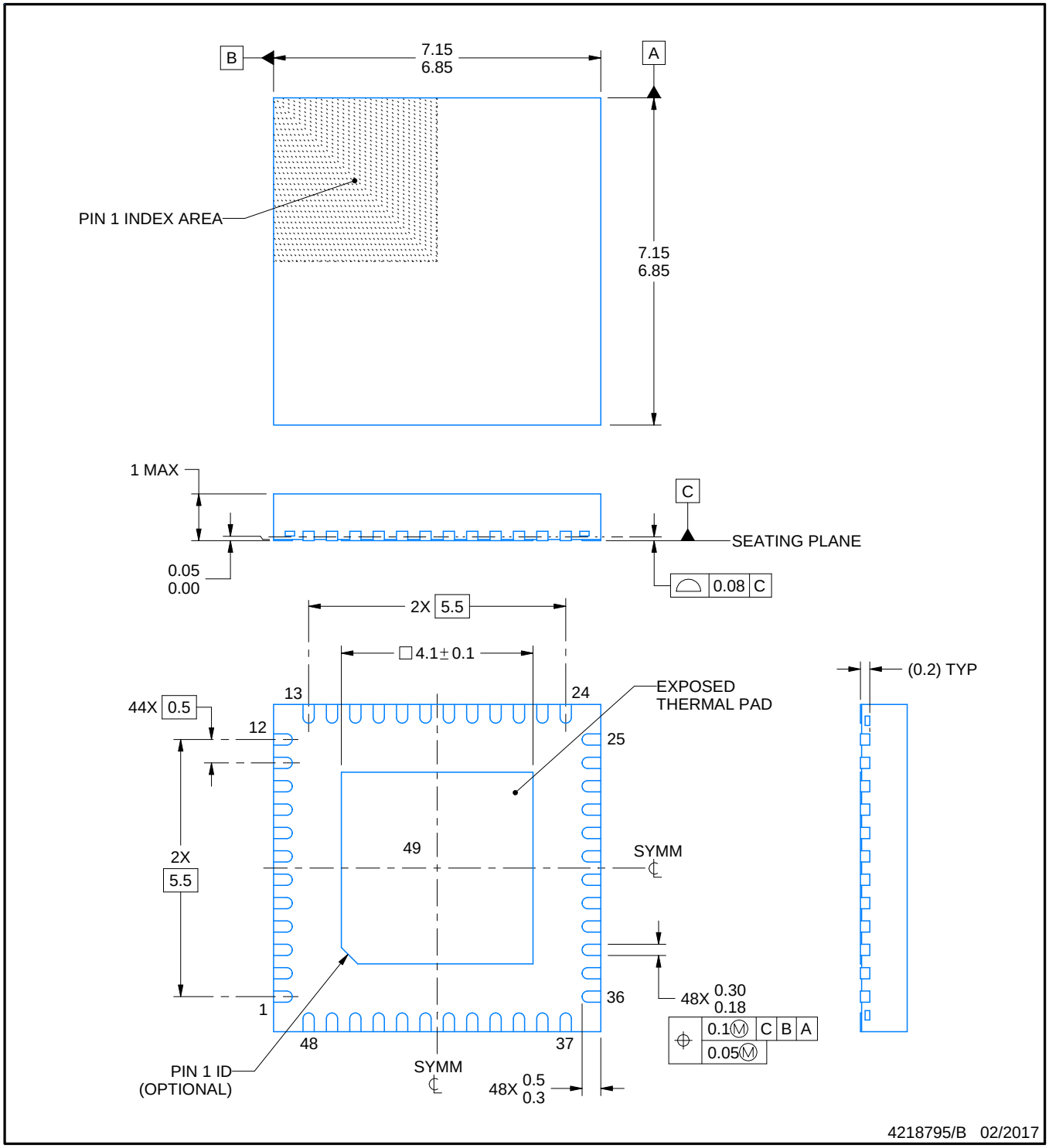
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

RGZ0048B

PACKAGE OUTLINE

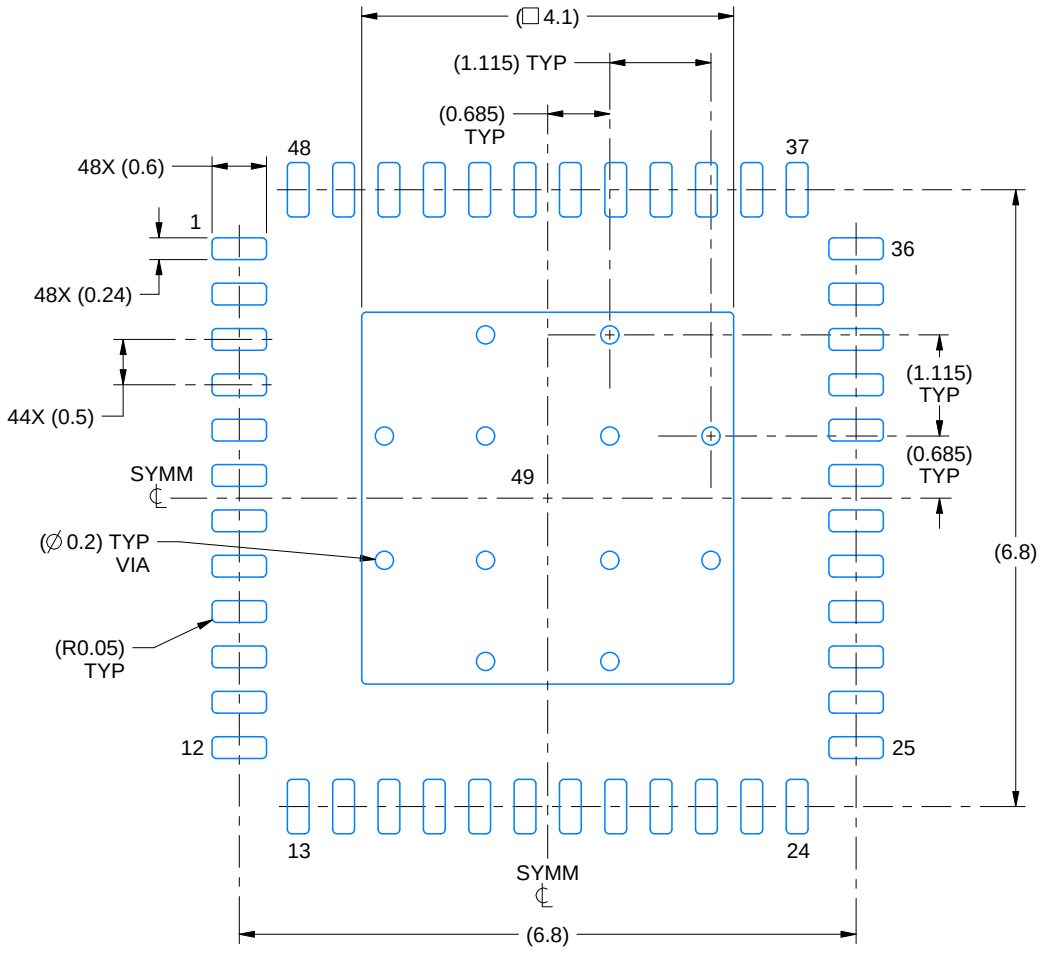
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

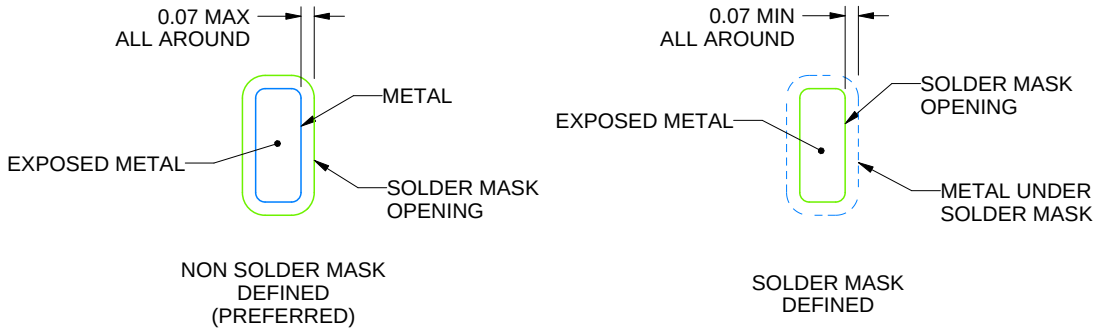


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

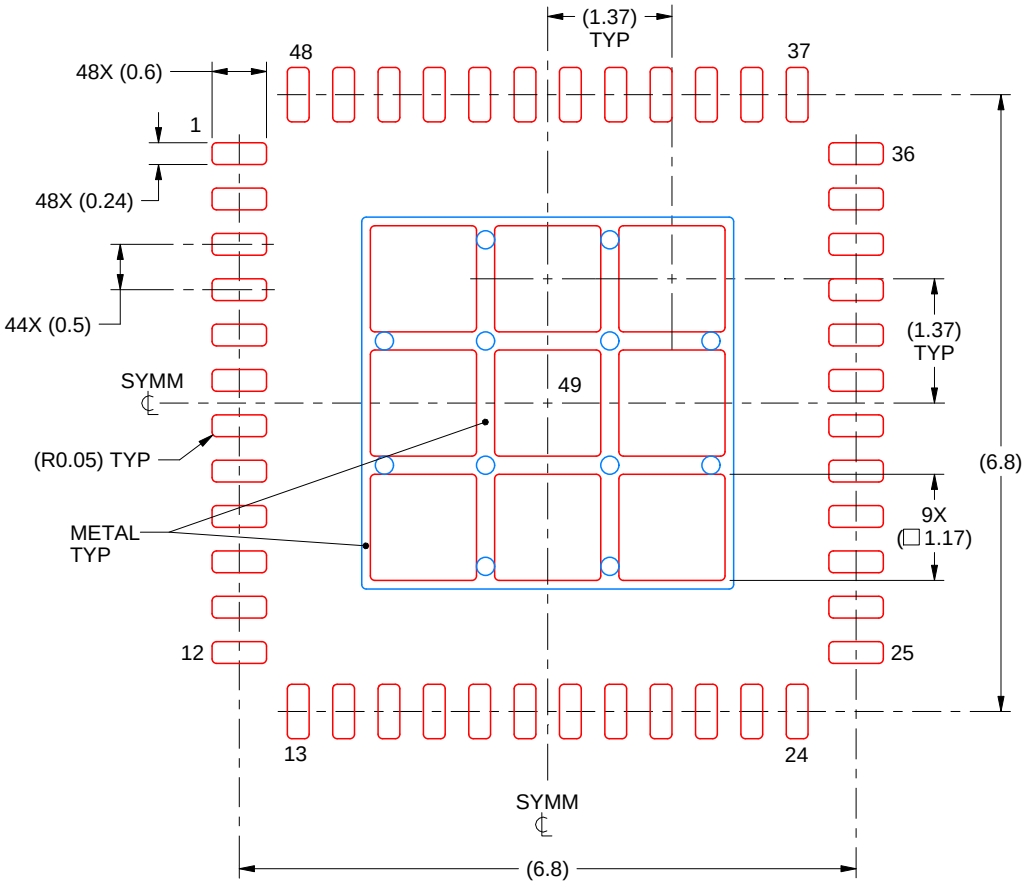


SOLDER MASK DETAILS

4218795/B 02/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

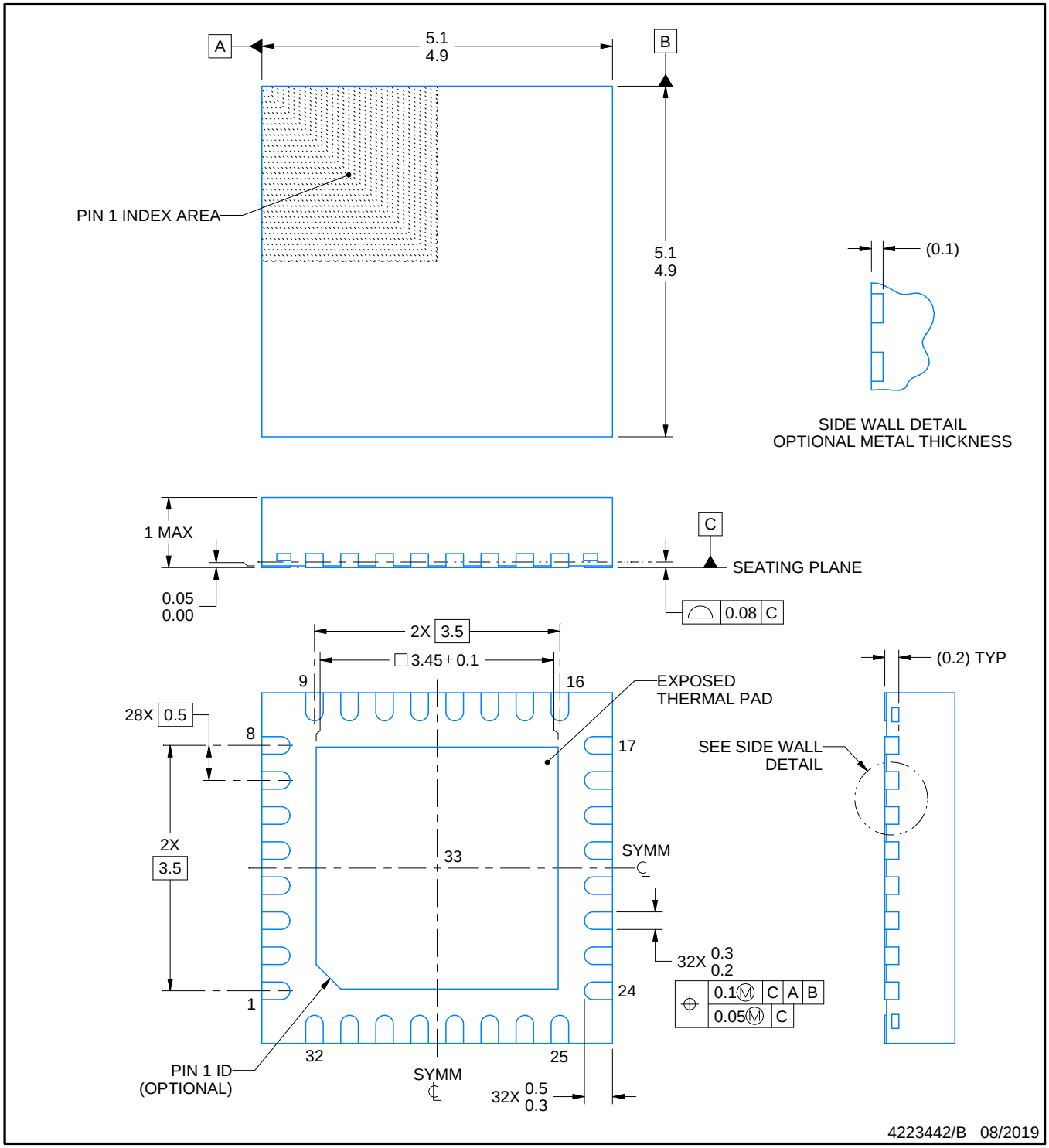
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RHB0032E

PACKAGE OUTLINE

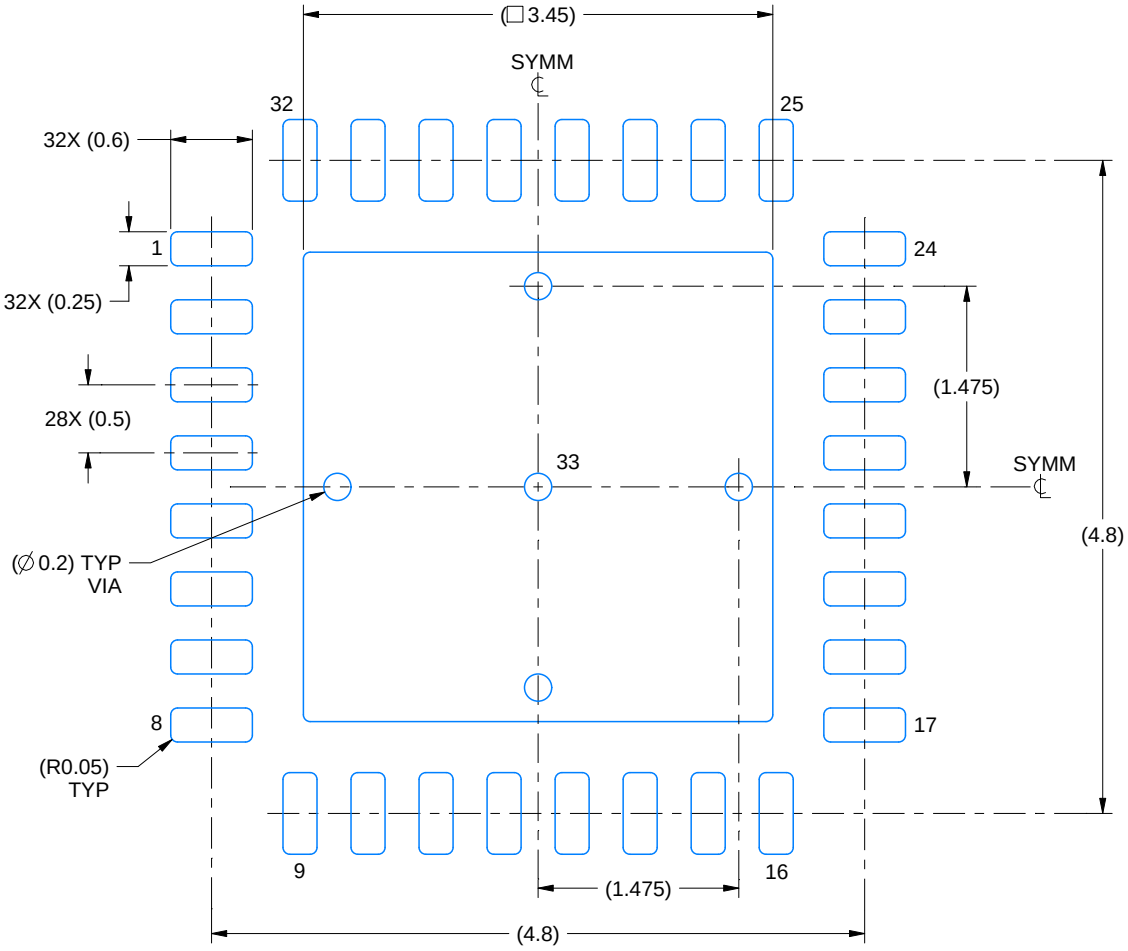
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

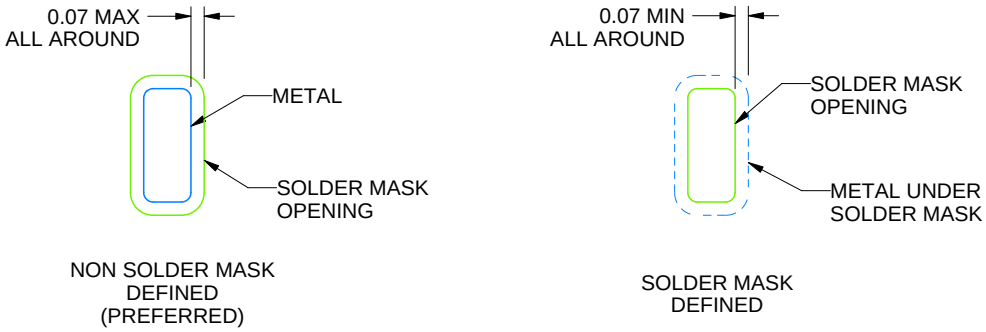


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

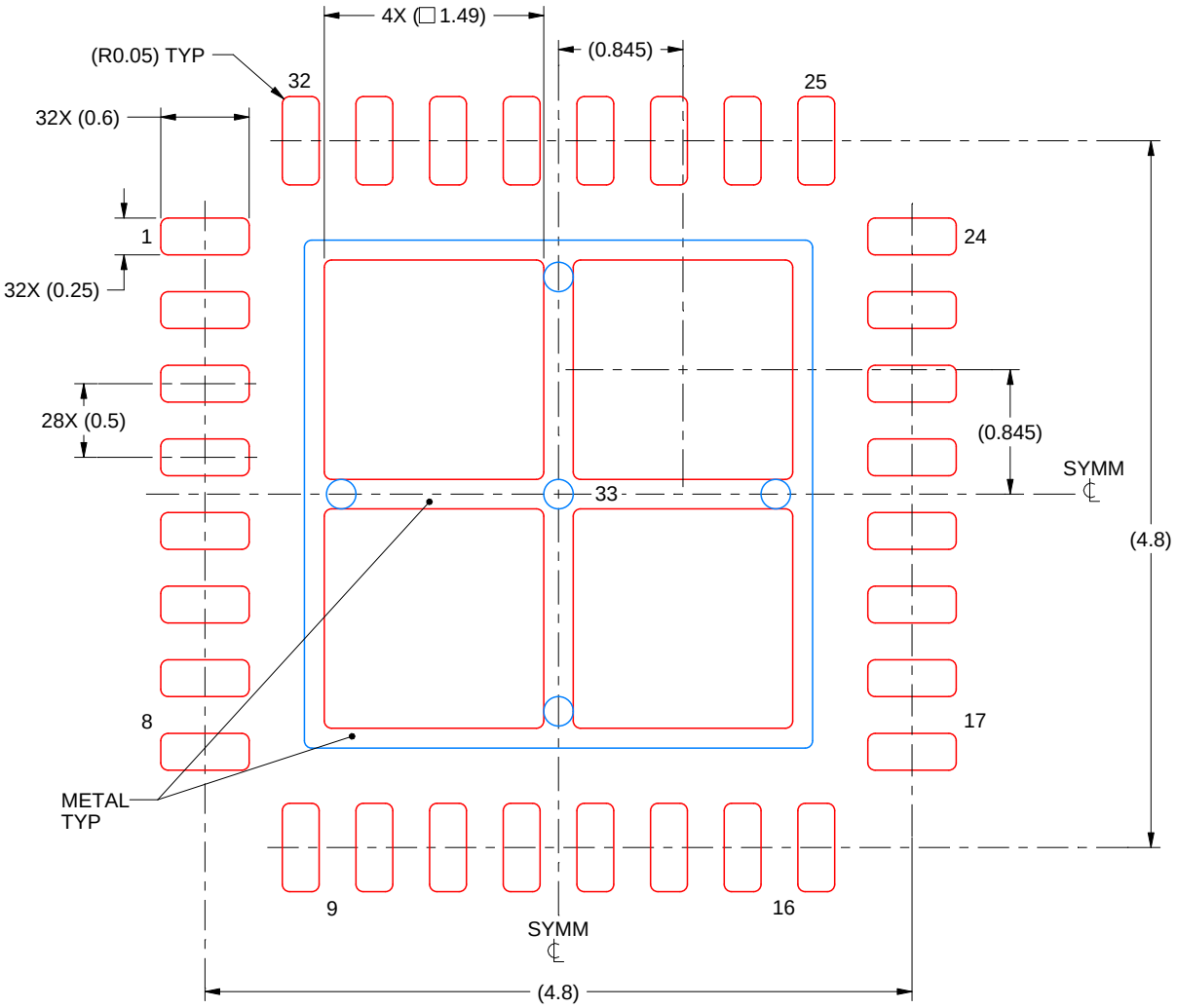


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
F2800132PTR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800132 PT	Samples
F2800132RGZR	ACTIVE	VQFN	RGZ	48	4000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800132 RGZ	Samples
F2800132RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	F2800 132RHB	Samples
F2800133PMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800133PM	Samples
F2800133PTR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800133 PT	Samples
F2800133RGZR	ACTIVE	VQFN	RGZ	48	4000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800133 RGZ	Samples
F2800133RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	F2800 133RHB	Samples
F2800135PMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800135PM	Samples
F2800135PTR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800135 PT	Samples
F2800135RGZR	ACTIVE	VQFN	RGZ	48	4000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800135 RGZ	Samples
F2800135RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	F2800 135RHB	Samples
F2800135VPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800135VPM	Samples
F2800137PM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800137PM	Samples
F2800137PMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800137PM	Samples
F2800137PT	ACTIVE	LQFP	PT	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800137 PT	Samples
F2800137PTR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800137 PT	Samples
F2800137RGZR	ACTIVE	VQFN	RGZ	48	4000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F2800137 RGZ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
F2800137RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	F2800 137RHB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

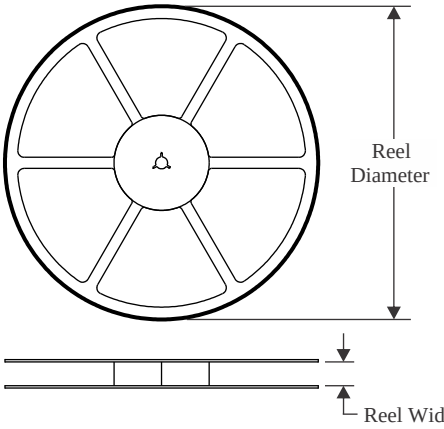
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

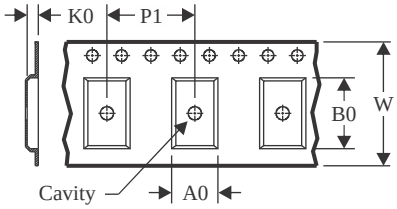
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

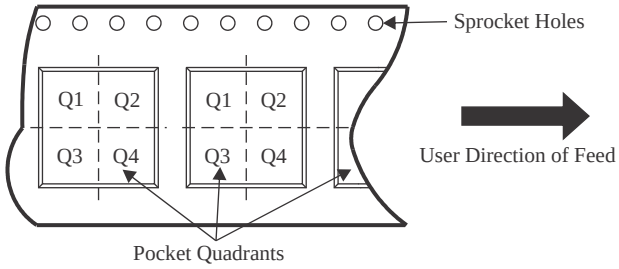


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

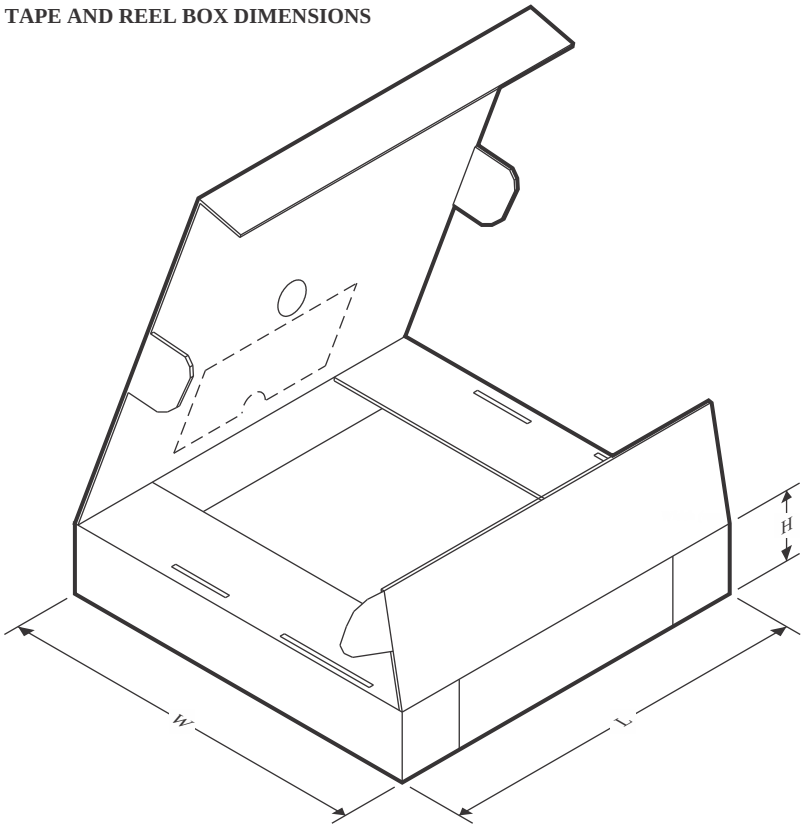
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
F2800132PTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F2800132RGZR	VQFN	RGZ	48	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
F2800132RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
F2800133PMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
F2800133PTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F2800133RGZR	VQFN	RGZ	48	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
F2800133RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
F2800135PMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
F2800135PTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F2800135RGZR	VQFN	RGZ	48	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
F2800135RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
F2800135VPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
F2800137PMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
F2800137PTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2
F2800137RGZR	VQFN	RGZ	48	4000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
F2800137RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

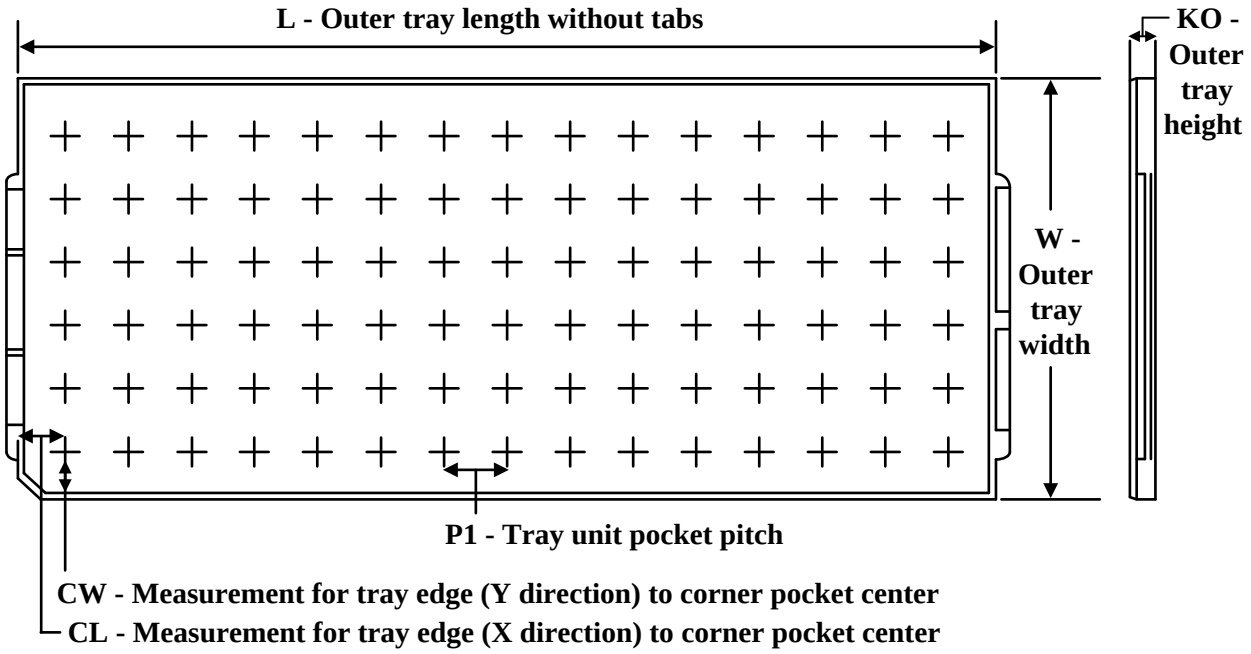
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
F2800132PTR	LQFP	PT	48	1000	336.6	336.6	31.8
F2800132RGZR	VQFN	RGZ	48	4000	367.0	367.0	35.0
F2800132RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
F2800133PMR	LQFP	PM	64	1000	336.6	336.6	41.3
F2800133PTR	LQFP	PT	48	1000	336.6	336.6	31.8
F2800133RGZR	VQFN	RGZ	48	4000	367.0	367.0	35.0
F2800133RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
F2800135PMR	LQFP	PM	64	1000	336.6	336.6	41.3
F2800135PTR	LQFP	PT	48	1000	336.6	336.6	31.8
F2800135RGZR	VQFN	RGZ	48	4000	367.0	367.0	35.0
F2800135RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
F2800135VPMR	LQFP	PM	64	1000	336.6	336.6	41.3
F2800137PMR	LQFP	PM	64	1000	336.6	336.6	41.3
F2800137PTR	LQFP	PT	48	1000	336.6	336.6	31.8
F2800137RGZR	VQFN	RGZ	48	4000	367.0	367.0	35.0
F2800137RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
F2800137PM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
F2800137PT	PT	LQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

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