

TMS320F280015x Real-Time Microcontrollers

1 Features

- 32-bit lockstep dual-TMS320C28x core at 120 MHz
 - IEEE 754 Floating-Point Unit (FPU)
 - Trigonometric Math Unit (TMU)
 - CRC Engine and Instructions (VCRC)
- On-chip memory
 - 256KB (128KW) of single bank flash (ECC-protected)
 - 36KB (18KW) of RAM (ECC/Parity-protected)
 - Security
 - JTAGLOCK
 - Zero-pin boot
 - Dual-zone security
- Clock and system control
 - Two internal 10-MHz oscillators
 - Crystal oscillator or external clock input
 - Windowed watchdog timer module
 - Missing clock detection circuitry
 - Dual-clock Comparator (DCC)
- 1.2-V core, 3.3-V I/O design
 - Internal VREG for 1.2-V generation
 - Brownout reset (BOR) circuit
- System peripherals
 - 52 individually programmable multiplexed General-Purpose Input/Output (GPIO) pins (11 shared with Analog)
 - 10 digital inputs on analog pins
 - Enhanced Peripheral Interrupt Expansion (ePIE)
 - Multiple low-power mode (LPM) support
 - Unique Identification (UID) number
- Communications peripherals
 - One Power-Management Bus (PMBus) interface
 - Two Inter-integrated Circuit (I2C) interfaces
 - One Controller Area Network (CAN/DCAN) bus port
 - One Controller Area Network with Flexible Data-Rate (CAN FD/MCAN) bus port
 - One Serial Peripheral Interface (SPI) ports
 - Three UART-compatible Serial Communication Interface (SCI)
 - One UART-compatible Local Interconnect Network (LIN) interfaces
- Analog system
 - Two 4-MSPS, 12-bit Analog-to-Digital Converters (ADCs)
 - Up to 21 external channels (11 shared with GPIO)
 - Four integrated Post-Processing Blocks (PPB) per ADC
 - One windowed comparator (CMPSS) with 12-bit reference Digital-to-Analog Converters (DACs)
 - Digital glitch filters
 - COMPDACOUT (11 bit)
 - Three windowed comparators (CMPSS_LITE) with 9.5-bit effective reference DACs
- Enhanced control peripherals
 - 14 ePWM channels with four channels that have high-resolution capability (150-ps resolution)
 - Integrated dead-band support
 - Integrated hardware trip zones (TZs)
 - Three Enhanced Capture (eCAP) modules
 - Two Enhanced Quadrature Encoder Pulse (eQEP) modules with support for CW/CCW operation modes
 - Embedded Pattern Generator (EPG)
- CMAC Keys (128-bits) for SW AES
- Diagnostic features
 - Memory Power On Self Test (MPOST)
- **Functional Safety-Compliant**
 - Developed for functional safety applications
 - Documentation available to aid ISO 26262 and IEC 61508 system design
 - **Systematic capability up to ASIL D and SIL 3**
 - **Hardware integrity up to ASIL B and SIL 2**
- Safety-related certification
 - **ISO 26262 certified up to ASIL B by TÜV SÜD**
 - **IEC 61508 certified up to SIL 2 by TÜV SÜD**
- Package options:
 - 80-pin Low-profile Quad Flatpack (LQFP) [PN suffix]
 - 64-pin LQFP [PM suffix]
 - 48-pin PowerPAD™ Thermally Enhanced Thin Quad Flatpack (HTQFP) [PHP suffix]
 - 32-pin Very Thin Quad Flatpack No-Lead (VQFN) [RHB suffix]
- Ambient Temperature (T_A) (see *Device Information* table and [Device Comparison](#)):
 - F280015xS, F280015xQ parts: –40°C to 125°C
 - F280015xE parts: –40°C to 150°C



2 Applications

- Automotive
 - ADAS
 - Radar ECU
 - Mechanically scanning LIDAR
 - Body electronics & lighting
 - Door module
 - Trunk module
 - Window module
 - Body control module (BCM)
 - HVAC compressor module
 - HVAC control module
 - Interior heater module
 - Headlight
 - Seat comfort module
 - Seat position and fold module
 - Steering wheel control
 - DC/AC inverter
 - Mid power DC/DC converter
- Hybrid, Electric, Powertrain Systems
 - Battery management system (BMS)
 - DC/DC converter
 - Inverter & motor control
 - On-board (OBC) & wireless charger
 - Vehicle control unit (VCU)
 - Virtual engine sound system (VESS)
- Engine fan
- eTurbo/charger
- Pump
- Automatic transmission
- Electric power steering (EPS)
- Infotainment and cluster
 - Head-up display
 - Telematics control unit
 - Automotive head unit
 - Aftermarket audio amplifier
 - Automotive active noise cancellation
 - Automotive external amplifier
- Industrial
 - Motor drives
 - AC drive control module
 - AC drive power stage module
 - Servo drive control module
 - Servo drive power stage module
 - Factory automation & control
 - Mobile robot motor control
 - Telecom & server power
 - Merchant DC/DC
 - Merchant network & server PSU
 - Merchant telecom rectifiers
 - UPS
 - Three phase UPS
 - Single phase online UPS

3 Description

The TMS320F280015x (F280015x) is a member of the cost-optimized C2000 real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics.

These include such [applications](#) as:

- HVAC compressor module
- Headlight
- DC/DC converter
- Inverter & motor control
- On-board (OBC) & wireless charger
- Pump
- Industrial motor drives
- Motor control
- Digital power
- Sensing and signal processing

TMS320F280015x has dual 32-bit C28x CPUs in Lockstep, enabling the device to achieve ASIL B functional safety device rating without much SW overhead. The [real-time control subsystem](#) is based on TI's 32-bit C28x DSP core, which provides 120 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the [Trigonometric Math Unit \(TMU\)](#) and [VCRC \(Cyclical Redundancy Check\) extended instruction sets](#), speeding up common algorithms key to real-time control systems.

The F280015x supports up to 256KB (128KW) of flash memory. Up to 36KB (18KW) of on-chip SRAM is also available to supplement the flash memory.

High-performance analog blocks are integrated on the F280015x real-time microcontroller (MCU) and are closely coupled with the processing and PWM units to provide optimal real-time signal chain performance. Fourteen PWM channels enable control of various power stages from a 3-phase inverter to power-factor correction and other advanced multilevel power topologies.

Interfacing is supported through various industry-standard communication ports (such as PMBUS, SPI, SCI, LIN, I2C, CAN and CAN FD) and offers [multiple pin-muxing options](#) for optimal signal placement.

Want to learn more about features that make C2000™ MCUs the right choice for your real-time control system? Check out [The Essential Guide for Developing With C2000™ Real-Time Microcontrollers](#) and visit the [C2000 real-time microcontrollers](#) page.

The [Getting Started With C2000™ Real-Time Control Microcontrollers \(MCUs\) Getting Started Guide](#) covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the [TMDSCNCD2800157](#) evaluation board and download [C2000Ware](#).

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ | BODY SIZE (NOM) |
|-------------------|------------------------|-----------------------------|-----------------|
| TMS320F2800157-Q1 | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| | PHP (HTQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| | RHB (VQFN, 32) | 5 mm × 5 mm | 5 mm × 5 mm |
| TMS320F2800157 | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| | PHP (HTQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| TMS320F2800156-Q1 | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| | PHP (HTQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| | RHB (VQFN, 32) | 5 mm × 5 mm | 5 mm × 5 mm |
| TMS320F2800155-Q1 | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| | PHP (HTQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| | RHB (VQFN, 32) | 5 mm × 5 mm | 5 mm × 5 mm |
| TMS320F2800155 | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| | PHP (HTQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| TMS320F2800154-Q1 | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| | PHP (HTQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| | RHB (VQFN, 32) | 5 mm × 5 mm | 5 mm × 5 mm |
| TMS320F2800153-Q1 | PHP (HTQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| | RHB (VQFN, 32) | 5 mm × 5 mm | 5 mm × 5 mm |
| TMS320F2800152-Q1 | PHP (HTQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| | RHB (VQFN, 32) | 5 mm × 5 mm | 5 mm × 5 mm |

(1) For more information, see [Mechanical, Packaging, and Orderable Information](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

| PART NUMBER ⁽¹⁾ | CODE ⁽²⁾ | PACKAGE OPTIONS | AEC-Q100 | FREQUENCY (MHz) | CMPSS (12-bit DAC) | HRPWM Channels | FLASH SIZE | Free-Air Temperature | |
|----------------------------------|---------------------|------------------------|----------|-----------------|--------------------|----------------|------------|----------------------|----------------|
| TMS320F2800157 | S | 80PN | – | 120 | 1 | 4 | 256KB | –40°C to 125°C | |
| TMS320F2800155 | | 64PM 48PHP | | | | | 128KB | | |
| TMS320F2800157-Q1 | Q | 80PN | Grade 1 | 120 | 1 | 4 | 256KB | | |
| TMS320F2800155-Q1 | | 64PM 48PHP 32RHB | | | | | 128KB | | |
| TMS320F2800156-Q1 | | 48PHP 32RHB | | 256KB | | | | | |
| TMS320F2800154-Q1 | | | | 100 | – | – | 128KB | | |
| TMS320F2800153-Q1 | | | | 120 | 1 | 4 | 64KB | | |
| TMS320F2800152-Q1 | | | | 100 | – | – | 64KB | | |
| TMS320F2800157-Q1 ⁽³⁾ | E | 48PHP | Grade 0 | 120 | 1 | 4 | 256KB | | –40°C to 150°C |
| TMS320F2800156-Q1 ⁽³⁾ | | | | 100 | – | – | 256KB | | |

- (1) For more information on these devices, see the [Device Comparison](#) table.
(2) **S**: Non-automotive parts
Q: Automotive **Grade 1** parts
E: Automotive **Grade 0** parts
(3) Preview information (not Production Data).

3.1 Functional Block Diagram

The [Functional Block Diagram](#) shows the CPU system and associated peripherals.

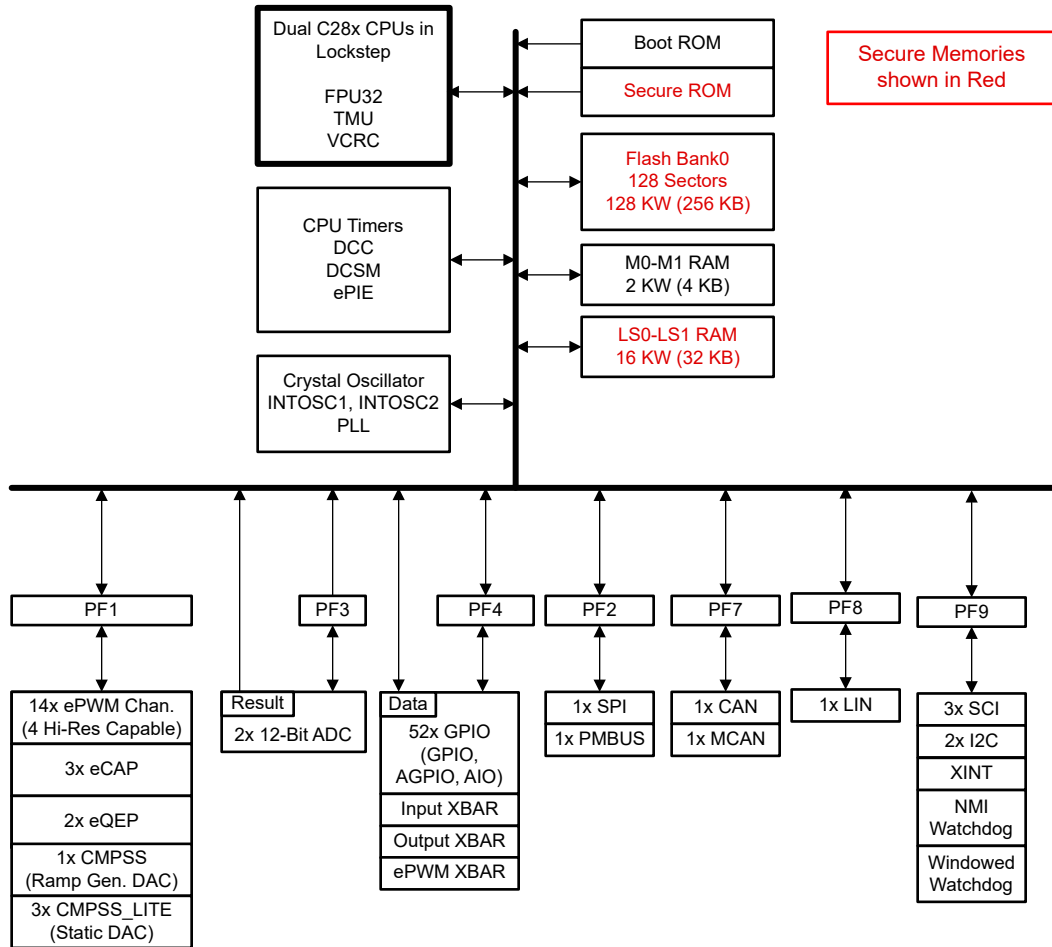


Figure 3-1. Functional Block Diagram

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4 Device Comparison

Table 4-1 lists the features of the TMS320F280015x devices.

Table 4-1. Device Comparison

| FEATURE ⁽¹⁾ | | F2800157- F2800157- Q1 ⁽²⁾ | F2800155- F2800155- Q1 | F2800153- Q1 | F2800156- Q1 ⁽²⁾ | F2800154- Q1 | F2800152- Q1 |
|-------------------------------------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|-----------------|--------------------------------|-----------------|-----------------|
| PROCESSOR AND ACCELERATORS | | | | | | | |
| C28x (dual-core, lockstep) | Frequency (MHz) | 120 | | | 100 | | |
| | FPU32 - Type 0 | Yes | | | | | |
| | TMU – Type 0 | Yes | | | | | |
| | VCRC | Yes | | | | | |
| MEMORY | | | | | | | |
| Flash | | 256KB (128KW) | 128KB (64KW) | 64KB (32KW) | 256KB (128KW) | 128KB (64KW) | 64KB (32KW) |
| RAM | | 36KB (18KW) | | | | | |
| Security: JTAGLOCK, Zero-pin boot, Dual-zone security | | Yes | | | | | |
| SYSTEM | | | | | | | |
| 32-bit CPU timers | | 3 | | | | | |
| Watchdog-timer | | 1 | | | | | |
| Dual Clock Compare (DCC) | | 1 | | | | | |
| External Interrupts | | 5 | | | | | |
| Embedded Pattern Generator (EPG) | | 1 | | | | | |
| Nonmaskable Interrupt Watchdog (NMIWD) timers | | 1 | | | | | |
| Crystal oscillator/External clock input | | 1 | | | | | |
| INTOSC with ExtR accuracy ⁽⁶⁾ | | +/- 1% | | | | | |
| Internal oscillator accuracy (2 INTOSC) | | See the <i>Internal Oscillators</i> section | | | | | |
| GPIO | 80-pin QFP PN | 52 (11 shared with analog and 4 shared with TDI, TDO, X1, X2) | | | | | |
| | 64-pin QFP PM | 37 (11 shared with analog and 4 shared with TDI, TDO, X1, X2) | | | | | |
| | 48-pin QFP PHP | 27 (9 shared with analog and 4 shared with TDI, TDO, X1, X2) | | | | | |
| | 32-pin QFN RHB | 18 (5 shared with analog and 4 shared with TDI, TDO, X1, X2) | | | | | |
| | Additional GPIO | 4 (When cJTAG is used, TDI and TDO can be GPIO. When INTOSC is used as clock source, X1 and X2 can be GPIO.) Note: These 4 GPIOs are included in the counts above. | | | | | |
| AIO (digital input shared with analog) | 80-pin QFP PN | 10 | | | | | |
| | 64-pin QFP PM | 10 | | | | | |
| | 48-pin QFP PHP | 9 | | | | | |
| | 32-pin QFN RHB | 6 | | | | | |
| ANALOG PERIPHERALS | | | | | | | |
| ADC 12-bit | Number of ADCs | 2 | | | | | |
| ADC Conversion-time(ns) ⁽³⁾ / MSPS | 80-pin QFP PN | 250 ns / 4.00 MSPS | | | 290 ns / 3.45 MSPS | | |
| | 64-pin QFP PM | | | | | | |
| | 48-pin QFP PHP | | | | | | |
| | 32-pin QFN RHB | | | | | | |

Table 4-1. Device Comparison (continued)

| FEATURE ⁽¹⁾ | | F2800157 F2800157- Q1 ⁽²⁾ | F2800155 F2800155- Q1 | F2800153- Q1 | F2800156- Q1 ⁽²⁾ | F2800154- Q1 | F2800152- Q1 |
|------------------------------------------------|---------------------------------------------------------------------------------------------------------------|--------------------------------------------|-----------------------------|-----------------|--------------------------------|-----------------|-----------------|
| ADC channels (single-ended) | 80-pin QFP PN | 21 (11 shared with GPIO) | | | | | |
| | 64-pin QFP PM | 21 (11 shared with GPIO) | | | | | |
| | 48-pin QFP PHP | 18 (9 shared with GPIO) | | | | | |
| | 32-pin QFN RHB | 11 (5 shared with GPIO) | | | | | |
| Temperature sensor | | 1 | | | | | |
| Comparator Subsystem | CMPSS (each includes two comparators and two dynamic DACs with incrementing and decrementing ramp generators) | 1 | | | - | | |
| | CMPSS_LITE (each includes two comparators and two static DACs) | 3 | | | | | |
| | CMPx_DACL output | 1 | | | - | | |
| CONTROL PERIPHERALS⁽⁴⁾ | | | | | | | |
| eCAP modules – Type 2 | | 3 | | | | | |
| ePWM/HRPWM – Type 4 | Total channels | 14 | | | | | |
| | Channels with high-resolution capability | 4 (ePWM1, ePWM2) | | | - | | |
| eQEP modules – Type 2 | | 2 | | | | | |
| COMMUNICATION PERIPHERALS⁽⁴⁾ | | | | | | | |
| PMBus – Type 0 | | 1 | | | | | |
| CAN – Type 0 | | 1 | | | | | |
| CAN FD (MCAN) – Type 2 | | 1 | | | | | |
| I2C – Type 1 | | 2 | | | | | |
| SCI – Type 0 (UART-Compatible) | | 3 | | | | | |
| LIN – Type 1 (UART-Compatible) | | 1 | | | | | |
| SPI – Type 2 | | 1 | | | | | |

Table 4-1. Device Comparison (continued)

| FEATURE ⁽¹⁾ | | F2800157 F2800157- Q1 ⁽²⁾ | F2800155 F2800155- Q1 | F2800153- Q1 | F2800156- Q1 ⁽²⁾ | F2800154- Q1 | F2800152- Q1 |
|--------------------------------------------------------|----------------------------------------|--------------------------------------------|--------------------------------|--------------------------------------------|--------------------------------|-----------------|-----------------|
| PACKAGE, TEMPERATURE, AND QUALIFICATION OPTIONS | | | | | | | |
| F280015xS parts | Junction temperature (T _J) | -40°C to 140°C | | | - | | |
| | Free-Air temperature (T _A) | -40°C to 125°C | | | - | | |
| | Package options | 80PN, 64PM, 48PHP | | | - | | |
| | AEC-Q100 qualification ⁽⁵⁾ | - | | | | | |
| F280015xQ parts | Junction temperature (T _J) | -40°C to 140°C | | | | | |
| | Free-Air temperature (T _A) | -40°C to 125°C | | | | | |
| | Package options | 80PN, 64PM, 48PHP, 32RHB ⁽⁷⁾ | 48PHP, 32RHB ⁽⁷⁾ | 80PN, 64PM, 48PHP, 32RHB ⁽⁷⁾ | 48PHP, 32RHB ⁽⁷⁾ | | |
| | AEC-Q100 qualification ⁽⁵⁾ | Grade 1 | | | | | |
| F280015xE parts | Junction temperature (T _J) | -40°C to 155°C | - | - | -40°C to 155°C | - | - |
| | Free-Air temperature (T _A) | -40°C to 150°C | - | - | -40°C to 150°C | - | - |
| | Package options | 48PHP | - | - | 48PHP | - | - |
| | AEC-Q100 qualification ⁽⁵⁾ | Grade 0 | - | - | Grade 0 | - | - |

- (1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module.
- (2) Information on the TMS320F2800157-Q1 (**Grade 1**) and TMS320F2800156-Q1 (**Grade 1**) devices is Production Data. Information on the TMS320F2800157-Q1 (**Grade 0**) and TMS320F2800156-Q1 (**Grade 0**) devices is preview information only (not Production Data).
- (3) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.
- (4) For devices that are available in more than one package, the peripheral count listed in the smaller package is reduced because the smaller package has less device pins available. The number of peripherals internally present on the device is not reduced compared to the largest package offered within a part number. See [Section 5](#) to identify which peripheral instances are accessible on pins in the smaller package.
- (5) Q1 refers to AEC-Q100 qualification for automotive applications.
- (6) See the *Internal Oscillators* section for INTOSC accuracy values
- (7) 32 RHB is Functional Safety Quality-Managed

4.1 Related Products

[TMS320F2803x Real-Time Microcontrollers](#)

The F2803x series increases the pin-count and memory size options. The F2803x series also introduces the parallel control law accelerator (CLA) option.

[TMS320F2807x Real-Time Microcontrollers](#)

The F2807x series offers the most performance, largest pin counts, flash memory sizes, and peripheral options. The F2807x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

[TMS320F28004x Real-Time Microcontrollers](#)

The F28004x series is a reduced version of the F2807x series with the latest generational enhancements.

[TMS320F2838x Real-Time Microcontrollers](#)

The F2838x series offers more performance, larger pin counts, flash memory sizes, peripheral and wide variety of connectivity options. The F2838x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

[TMS320F28002x Real-Time Microcontrollers](#)

The F28002x series is a reduced version of the F28004x series with the latest generational enhancements.

[TMS320F28003x Real-Time Microcontrollers](#)

The F28003x series builds upon the F28002x series offering higher frequency, more memory, and more peripheral options. CAN FD and security features are introduced from F2838x series.

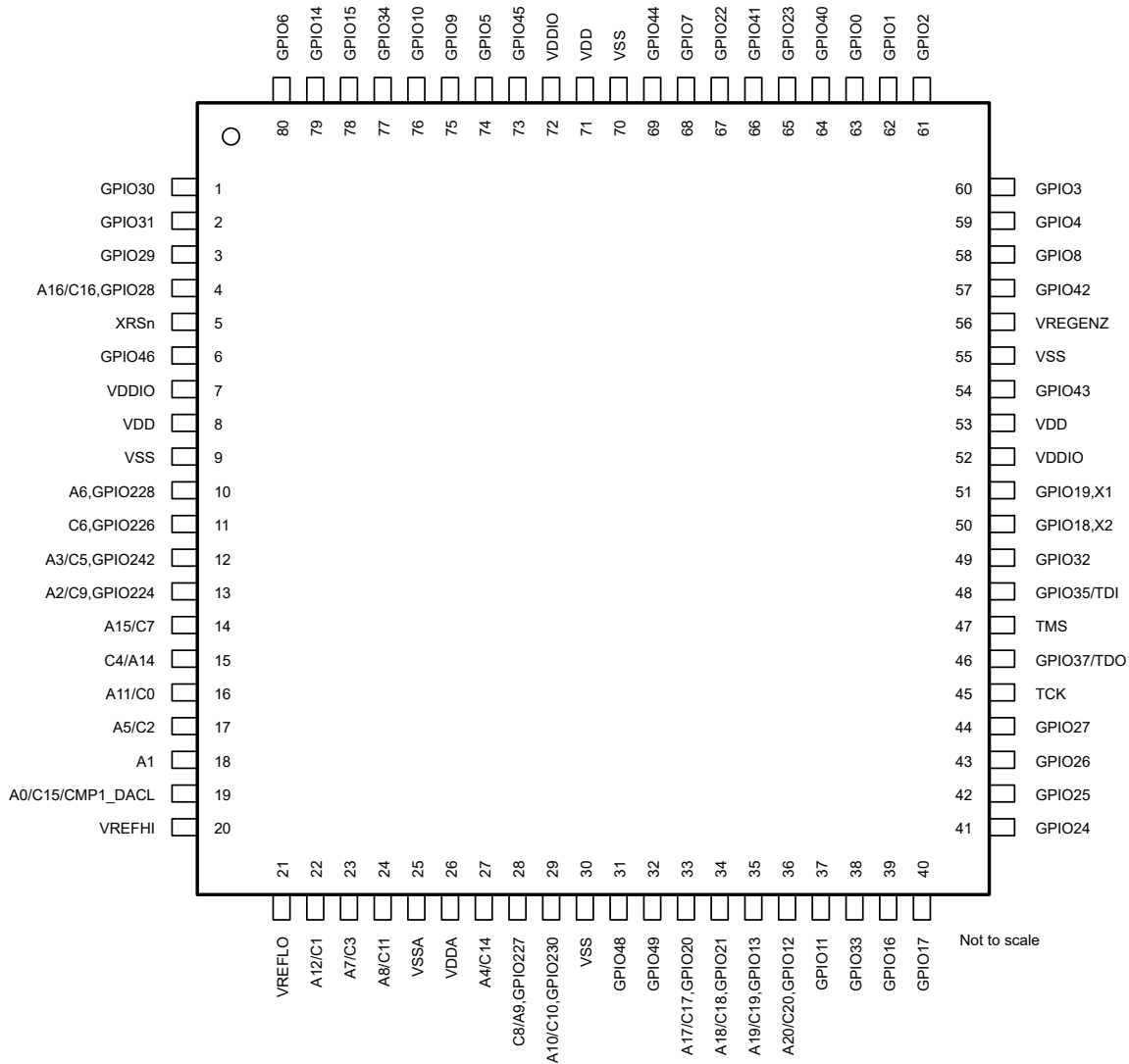
[TMS320F280013x Real-Time Microcontrollers](#)

The F280013x is a similar class of device as F280015x, catered towards industrial applications.

5 Pin Configuration and Functions

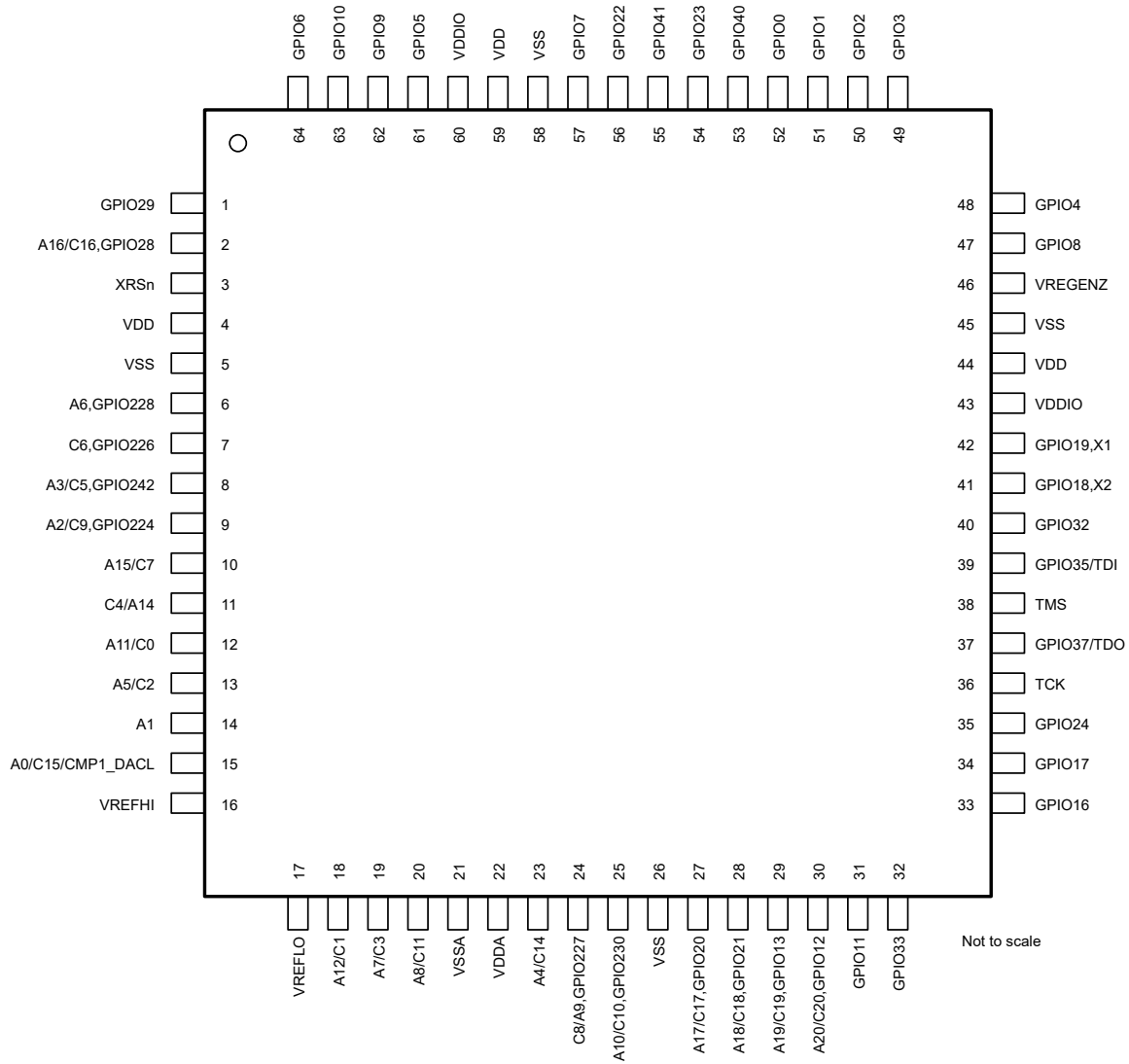
5.1 Pin Diagrams

Figure 5-1 shows the pin assignments on the 80-pin PN low-profile quad flatpack (LQFP). Figure 5-2 shows the pin assignments on the 64-pin PM LQFP. Figure 5-3 shows the pin assignments on the 48-pin PHP PowerPAD™ thermally enhanced thin quad flatpack (HTQFP). Figure 5-4 shows the pin assignments on the 32-pin RHB very thin quad flatpack no lead (VQFN).



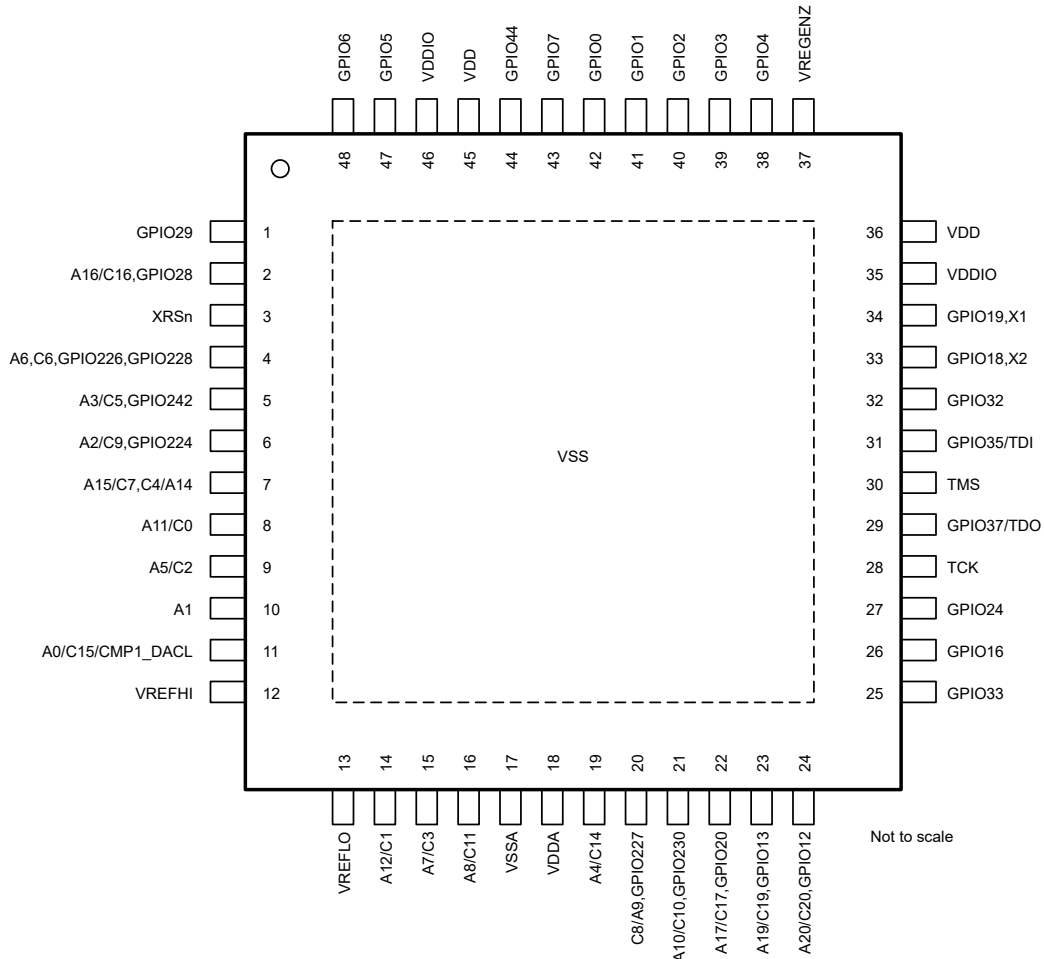
A. Only the GPIO function is shown on GPIO terminals. See Section 5.2 for the complete, muxed signal name.

Figure 5-1. 80-Pin PN Low-Profile Quad Flatpack (Top View)



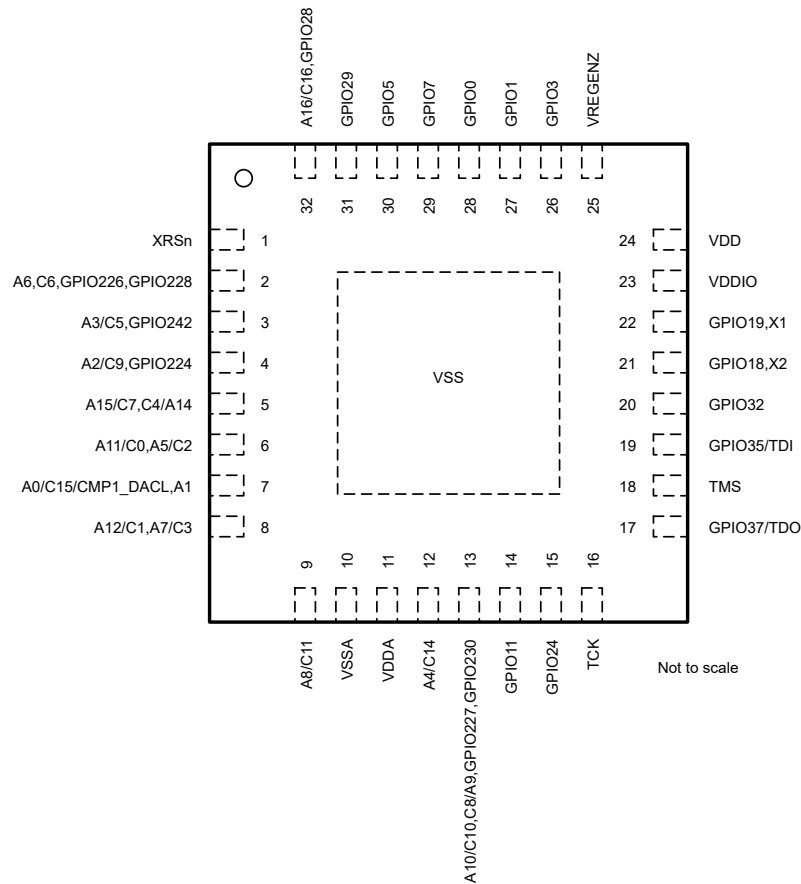
A. Only the GPIO function is shown on GPIO terminals. See [Section 5.2](#) for the complete, muxed signal name.

Figure 5-2. 64-Pin PM Low-Profile Quad Flatpack (Top View)



A. Only the GPIO function is shown on GPIO terminals. See [Section 5.2](#) for the complete, muxed signal name.

Figure 5-3. 48-Pin PHP PowerPAD™ Thermally Enhanced Thin Quad Flatpack (Top View)



A. Only the GPIO function is shown on GPIO terminals. See [Section 5.2](#) for the complete, muxed signal name.

Figure 5-4. 32-Pin RHB Very Thin Quad Flatpack No Lead (Top View)

5.2 Pin Attributes

Table 5-1. Pin Attributes

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|---------------------------------------------------------------------------------------------|--------------|-------|-------|--------|--------|----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ANALOG | | | | | | | |
| A0 C15 CMP1_DACL CMP3_HP2 CMP3_LP2 AIO231 | 0, 4, 8, 12 | 19 | 15 | 11 | 7 | I | ADC-A Input 0 ADC-C Input 15 CMPSS-1 Low DAC Output CMPSS-3 High Comparator Positive Input 2 CMPSS-3 Low Comparator Positive Input 2 Analog Pin Used For Digital Input 231 |
| A1 CMP1_HP4 CMP1_LP4 AIO232 | 0, 4, 8, 12 | 18 | 14 | 10 | 7 | I | ADC-A Input 1 CMPSS-1 High Comparator Positive Input 4 CMPSS-1 Low Comparator Positive Input 4 Analog Pin Used For Digital Input 232 |
| A2 C9 CMP1_HP0 CMP1_LP0 GPIO224 | | 13 | 9 | 6 | 4 | I I/O | ADC-A Input 2 ADC-C Input 9 CMPSS-1 High Comparator Positive Input 0 CMPSS-1 Low Comparator Positive Input 0 General-Purpose Input Output 224 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A3 C5 CMP3_HN0 CMP3_HP3 CMP3_LN0 CMP3_LP3 GPIO242 | | 12 | 8 | 5 | 3 | I I/O | ADC-A Input 3 ADC-C Input 5 CMPSS-3 High Comparator Negative Input 0 CMPSS-3 High Comparator Positive Input 3 CMPSS-3 Low Comparator Negative Input 0 CMPSS-3 Low Comparator Positive Input 3 General-Purpose Input Output 242 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A4 C14 CMP2_HP0 CMP2_LP0 CMP4_HN0 CMP4_HP3 CMP4_LN0 CMP4_LP3 AIO225 | 0, 4, 8, 12 | 27 | 23 | 19 | 12 | I I | ADC-A Input 4 ADC-C Input 14 CMPSS-2 High Comparator Positive Input 0 CMPSS-2 Low Comparator Positive Input 0 CMPSS-4 High Comparator Negative Input 0 CMPSS-4 High Comparator Positive Input 3 CMPSS-4 Low Comparator Negative Input 0 CMPSS-4 Low Comparator Positive Input 3 Analog Pin Used For Digital Input 225 |
| A5 C2 CMP3_HN1 CMP3_HP1 CMP3_LN1 CMP3_LP1 AIO244 | 0, 4, 8, 12 | 17 | 13 | 9 | 6 | I I | ADC-A Input 5 ADC-C Input 2 CMPSS-3 High Comparator Negative Input 1 CMPSS-3 High Comparator Positive Input 1 CMPSS-3 Low Comparator Negative Input 1 CMPSS-3 Low Comparator Positive Input 1 Analog Pin Used For Digital Input 244 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|---------------------------------------------------------------------------------------------|--------------|-------|-------|--------|--------|-------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A6 CMP1_HP2 CMP1_LP2 GPIO228 | | 10 | 6 | 4 | 2 | I I I I/O | ADC-A Input 6 CMPSS-1 High Comparator Positive Input 2 CMPSS-1 Low Comparator Positive Input 2 General-Purpose Input Output 228 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A7 C3 CMP4_HN1 CMP4_HP1 CMP4_LN1 CMP4_LP1 AIO245 | 0, 4, 8, 12 | 23 | 19 | 15 | 8 | I I I I I I I | ADC-A Input 7 ADC-C Input 3 CMPSS-4 High Comparator Negative Input 1 CMPSS-4 High Comparator Positive Input 1 CMPSS-4 Low Comparator Negative Input 1 CMPSS-4 Low Comparator Positive Input 1 Analog Pin Used For Digital Input 245 |
| A8 C11 CMP2_HP4 CMP2_LP4 CMP4_HP4 CMP4_LP4 AIO241 | 0, 4, 8, 12 | 24 | 20 | 16 | 9 | I I I I I I I | ADC-A Input 8 ADC-C Input 11 CMPSS-2 High Comparator Positive Input 4 CMPSS-2 Low Comparator Positive Input 4 CMPSS-4 High Comparator Positive Input 4 CMPSS-4 Low Comparator Positive Input 4 Analog Pin Used For Digital Input 241 |
| A10 C10 CMP2_HN0 CMP2_HP3 CMP2_LN0 CMP2_LP3 GPIO230 | | 29 | 25 | 21 | 13 | I I I I I I I/O | ADC-A Input 10 ADC-C Input 10 CMPSS-2 High Comparator Negative Input 0 CMPSS-2 High Comparator Positive Input 3 CMPSS-2 Low Comparator Negative Input 0 CMPSS-2 Low Comparator Positive Input 3 General-Purpose Input Output 230 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A11 C0 CMP1_HN1 CMP1_HP1 CMP1_LN1 CMP1_LP1 AIO237 | 0, 4, 8, 12 | 16 | 12 | 8 | 6 | I I I I I I I | ADC-A Input 11 ADC-C Input 0 CMPSS-1 High Comparator Negative Input 1 CMPSS-1 High Comparator Positive Input 1 CMPSS-1 Low Comparator Negative Input 1 CMPSS-1 Low Comparator Positive Input 1 Analog Pin Used For Digital Input 237 |
| A12 C1 CMP2_HN1 CMP2_HP1 CMP2_LN1 CMP2_LP1 CMP4_HP2 CMP4_LP2 AIO238 | 0, 4, 8, 12 | 22 | 18 | 14 | 8 | I I I I I I I I I | ADC-A Input 12 ADC-C Input 1 CMPSS-2 High Comparator Negative Input 1 CMPSS-2 High Comparator Positive Input 1 CMPSS-2 Low Comparator Negative Input 1 CMPSS-2 Low Comparator Positive Input 1 CMPSS-4 High Comparator Positive Input 2 CMPSS-4 Low Comparator Positive Input 2 Analog Pin Used For Digital Input 238 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|---------------------------------------------------------------------|--------------|-------|-------|--------|--------|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A15 C7 CMP1_HN0 CMP1_HP3 CMP1_LN0 CMP1_LP3 AIO233 | 0, 4, 8, 12 | 14 | 10 | 7 | 5 | I I I I I I I | ADC-A Input 15 ADC-C Input 7 CMPSS-1 High Comparator Negative Input 0 CMPSS-1 High Comparator Positive Input 3 CMPSS-1 Low Comparator Negative Input 0 CMPSS-1 Low Comparator Positive Input 3 Analog Pin Used For Digital Input 233 |
| A16 C16 GPIO28 | | 4 | 2 | 2 | 32 | I I I/O | ADC-A Input 16 ADC-C Input 16 General-Purpose Input Output 28 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A17 C17 GPIO20 | | 33 | 27 | 22 | | I I I/O | ADC-A Input 17 ADC-C Input 17 General-Purpose Input Output 20 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A18 C18 GPIO21 | | 34 | 28 | | | I I I/O | ADC-A Input 18 ADC-C Input 18 General-Purpose Input Output 21 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A19 C19 GPIO13 | | 35 | 29 | 23 | | I I I/O | ADC-A Input 19 ADC-C Input 19 General-Purpose Input Output 13 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A20 C20 GPIO12 | | 36 | 30 | 24 | | I I I/O | ADC-A Input 20 ADC-C Input 20 General-Purpose Input Output 12 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A14 C4 CMP3_HP4 CMP3_LP4 AIO239 | 0, 4, 8, 12 | 15 | 11 | 7 | 5 | I I I I I | ADC-A Input 14 ADC-C Input 4 CMPSS-3 High Comparator Positive Input 4 CMPSS-3 Low Comparator Positive Input 4 Analog Pin Used For Digital Input 239 |
| C6 CMP3_HP0 CMP3_LP0 GPIO226 | | 11 | 7 | 4 | 2 | I I I I/O | ADC-C Input 6 CMPSS-3 High Comparator Positive Input 0 CMPSS-3 Low Comparator Positive Input 0 General-Purpose Input Output 226 This pin also has digital mux functions which are described in the GPIO section of this table. |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|--------------|--------------|-------|-------|--------|--------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A9 | | | | | | I | ADC-A Input 9 |
| C8 | | | | | | I | ADC-C Input 8 |
| CMP2_HP2 | | | | | | I | CMPSS-2 High Comparator Positive Input 2 |
| CMP2_LP2 | | | | | | I | CMPSS-2 Low Comparator Positive Input 2 |
| CMP4_HP0 | | 28 | 24 | 20 | 13 | I | CMPSS-4 High Comparator Positive Input 0 |
| CMP4_LP0 | | | | | | I | CMPSS-4 Low Comparator Positive Input 0 |
| GPIO227 | | | | | | I/O | General-Purpose Input Output 227 This pin also has digital mux functions which are described in the GPIO section of this table. |
| VREFHI | | 20 | 16 | 12 | | I | ADC High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2- μ F capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. On the 32 QFN package, VREFHI is internally tied to VDDA. |
| VREFLO | | 21 | 17 | 13 | | I | ADC Low Reference |
| GPIO | | | | | | | |
| GPIO0 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 0 |
| EPWM1_A | 1 | | | | | O | ePWM-1 Output A |
| CANA_RX | 2 | | | | | I | CAN-A Receive |
| OUTPUTXBAR7 | 3 | | | | | O | Output X-BAR Output 7 |
| SCIA_RX | 5 | 63 | 52 | 42 | 28 | I | SCI-A Receive Data |
| I2CA_SDA | 6 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| SPIA_STE | 7 | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| MCAN_RX | 10 | | | | | I | CAN/CAN FD Receive |
| EQEP1_INDEX | 13 | | | | | I/O | eQEP-1 Index |
| EPWM3_A | 15 | | | | | O | ePWM-3 Output A |
| GPIO1 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 1 |
| EPWM1_B | 1 | | | | | O | ePWM-1 Output B |
| SCIA_TX | 5 | | | | | O | SCI-A Transmit Data |
| I2CA_SCL | 6 | 62 | 51 | 41 | 27 | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SPIA_SOMI | 7 | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| EQEP1_STROBE | 9 | | | | | I/O | eQEP-1 Strobe |
| MCAN_TX | 10 | | | | | O | CAN/CAN FD Transmit |
| EPWM3_B | 15 | | | | | O | ePWM-3 Output B |
| GPIO2 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 2 |
| EPWM2_A | 1 | | | | | O | ePWM-2 Output A |
| OUTPUTXBAR1 | 5 | | | | | O | Output X-BAR Output 1 |
| PMBUSA_SDA | 6 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SPIA_SIMO | 7 | 61 | 50 | 40 | | I/O | SPI-A Slave In, Master Out (SIMO) |
| SCIA_TX | 9 | | | | | O | SCI-A Transmit Data |
| I2CB_SDA | 11 | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| CANA_TX | 14 | | | | | O | CAN-A Transmit |
| EPWM4_A | 15 | | | | | O | ePWM-4 Output A |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|--------------|--------------|-------|-------|--------|--------|----------|----------------------------------------|
| GPIO3 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 3 |
| EPWM2_B | 1 | | | | | O | ePWM-2 Output B |
| OUTPUTXBAR2 | 2, 5 | | | | | O | Output X-BAR Output 2 |
| PMBUSA_SCL | 6 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SPIA_CLK | 7 | 60 | 49 | 39 | 26 | I/O | SPI-A Clock |
| SCIA_RX | 9 | | | | | I | SCI-A Receive Data |
| I2CB_SCL | 11 | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| CANA_RX | 14 | | | | | I | CAN-A Receive |
| EPWM4_B | 15 | | | | | O | ePWM-4 Output B |
| GPIO4 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 4 |
| EPWM3_A | 1 | | | | | O | ePWM-3 Output A |
| I2CA_SCL | 2 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| MCAN_TX | 3 | | | | | O | CAN/CAN FD Transmit |
| OUTPUTXBAR3 | 5 | 59 | 48 | 38 | | O | Output X-BAR Output 3 |
| CANA_TX | 6 | | | | | O | CAN-A Transmit |
| EQEP2_STROBE | 9 | | | | | I/O | eQEP-2 Strobe |
| SPIA_SOMI | 14 | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| EPWM1_A | 15 | | | | | O | ePWM-1 Output A |
| GPIO5 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 5 |
| EPWM3_B | 1 | | | | | O | ePWM-3 Output B |
| I2CA_SDA | 2 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| OUTPUTXBAR3 | 3 | | | | | O | Output X-BAR Output 3 |
| MCAN_RX | 5 | 74 | 61 | 47 | 30 | I | CAN/CAN FD Receive |
| CANA_RX | 6 | | | | | I | CAN-A Receive |
| SPIA_STE | 7 | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| SCIA_RX | 11 | | | | | I | SCI-A Receive Data |
| EPWM1_B | 15 | | | | | O | ePWM-1 Output B |
| GPIO6 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 6 |
| EPWM4_A | 1 | | | | | O | ePWM-4 Output A |
| OUTPUTXBAR4 | 2 | | | | | O | Output X-BAR Output 4 |
| SYNCOUT | 3 | 80 | 64 | 48 | | O | External ePWM Synchronization Pulse |
| EQEP1_A | 5 | | | | | I | eQEP-1 Input A |
| EPWM2_A | 15 | | | | | O | ePWM-2 Output A |
| GPIO7 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 7 |
| EPWM4_B | 1 | | | | | O | ePWM-4 Output B |
| EPWM2_A | 2 | | | | | O | ePWM-2 Output A |
| OUTPUTXBAR5 | 3 | | | | | O | Output X-BAR Output 5 |
| EQEP1_B | 5 | 68 | 57 | 43 | 29 | I | eQEP-1 Input B |
| SPIA_SIMO | 7 | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| SCIA_TX | 11 | | | | | O | SCI-A Transmit Data |
| CANA_TX | 14 | | | | | O | CAN-A Transmit |
| EPWM2_B | 15 | | | | | O | ePWM-2 Output B |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|--------------|--------------|-------|-------|--------|--------|----------|-----------------------------------------------------------------------------------------------------------------------------|
| GPIO8 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 8 |
| EPWM5_A | 1 | | | | | O | ePWM-5 Output A |
| ADCSOAO | 3 | | | | | O | ADC Start of Conversion A for External ADC |
| EQEP1_STROBE | 5 | 58 | 47 | | | I/O | eQEP-1 Strobe |
| SCIA_TX | 6 | | | | | O | SCI-A Transmit Data |
| SPIA_SIMO | 7 | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| I2CA_SCL | 9 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| GPIO9 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 9 |
| EPWM5_B | 1 | | | | | O | ePWM-5 Output B |
| SCIB_TX | 2 | | | | | O | SCI-B Transmit Data |
| OUTPUTXBAR6 | 3 | | | | | O | Output X-BAR Output 6 |
| EQEP1_INDEX | 5 | 75 | 62 | | | I/O | eQEP-1 Index |
| SCIA_RX | 6 | | | | | I | SCI-A Receive Data |
| SPIA_CLK | 7 | | | | | I/O | SPI-A Clock |
| I2CB_SCL | 14 | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| GPIO10 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 10 |
| EPWM6_A | 1 | | | | | O | ePWM-6 Output A |
| ADCSOCBO | 3 | | | | | O | ADC Start of Conversion B for External ADC |
| EQEP1_A | 5 | 76 | 63 | | | I | eQEP-1 Input A |
| SCIB_TX | 6 | | | | | O | SCI-B Transmit Data |
| SPIA_SOMI | 7 | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| I2CA_SDA | 9 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| GPIO11 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 11 |
| EPWM6_B | 1 | | | | | O | ePWM-6 Output B |
| CANA_RX | 2 | | | | | I | CAN-A Receive |
| OUTPUTXBAR7 | 3 | | | | | O | Output X-BAR Output 7 |
| EQEP1_B | 5 | 37 | 31 | | 14 | I | eQEP-1 Input B |
| SCIB_RX | 6 | | | | | I | SCI-B Receive Data |
| SPIA_STE | 7 | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| EQEP2_A | 11 | | | | | I | eQEP-2 Input A |
| SPIA_SIMO | 13 | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| GPIO12 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 12 This pin also has analog functions which are described in the ANALOG section of this table. |
| EPWM7_A | 1 | | | | | O | ePWM-7 Output A |
| MCAN_RX | 3 | | | | | I | CAN/CAN FD Receive |
| EQEP1_STROBE | 5 | 36 | 30 | 24 | | I/O | eQEP-1 Strobe |
| SCIB_TX | 6 | | | | | O | SCI-B Transmit Data |
| PMBUSA_CTL | 7 | | | | | I/O | PMBus-A Control Signal - Slave Input/Master Output |
| SPIA_CLK | 11 | | | | | I/O | SPI-A Clock |
| CANA_RX | 13 | | | | | I | CAN-A Receive |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|--------------|--------------|-------|-------|--------|--------|----------|-----------------------------------------------------------------------------------------------------------------------------|
| GPIO13 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 13 This pin also has analog functions which are described in the ANALOG section of this table. |
| EPWM7_B | 1 | | | | | O | ePWM-7 Output B |
| MCAN_TX | 3 | | | | | O | CAN/CAN FD Transmit |
| EQEP1_INDEX | 5 | 35 | 29 | 23 | | I/O | eQEP-1 Index |
| SCIB_RX | 6 | | | | | I | SCI-B Receive Data |
| PMBUSA_ALERT | 7 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| SPIA_SOMI | 11 | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| CANA_TX | 13 | | | | | O | CAN-A Transmit |
| GPIO14 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 14 |
| SCIB_TX | 2 | | | | | O | SCI-B Transmit Data |
| I2CB_SDA | 5 | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| OUTPUTXBAR3 | 6 | 79 | | | | O | Output X-BAR Output 3 |
| PMBUSA_SDA | 7 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| EQEP2_A | 10 | | | | | I | eQEP-2 Input A |
| EPWM3_A | 13 | | | | | O | ePWM-3 Output A |
| GPIO15 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 15 |
| SCIB_RX | 2 | | | | | I | SCI-B Receive Data |
| I2CB_SCL | 5 | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| OUTPUTXBAR4 | 6 | 78 | | | | O | Output X-BAR Output 4 |
| PMBUSA_SCL | 7 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| EQEP2_B | 10 | | | | | I | eQEP-2 Input B |
| EPWM3_B | 13 | | | | | O | ePWM-3 Output B |
| GPIO16 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 16 |
| SPIA_SIMO | 1 | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| OUTPUTXBAR7 | 3 | | | | | O | Output X-BAR Output 7 |
| EPWM5_A | 5 | | | | | O | ePWM-5 Output A |
| SCIA_TX | 6 | | | | | O | SCI-A Transmit Data |
| EQEP1_STROBE | 9 | 39 | 33 | 26 | | I/O | eQEP-1 Strobe |
| PMBUSA_SCL | 10 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| XCLKOUT | 11 | | | | | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. |
| EQEP2_B | 13 | | | | | I | eQEP-2 Input B |
| GPIO17 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 17 |
| SPIA_SOMI | 1 | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| OUTPUTXBAR8 | 3 | | | | | O | Output X-BAR Output 8 |
| EPWM5_B | 5 | | | | | O | ePWM-5 Output B |
| SCIA_RX | 6 | 40 | 34 | | | I | SCI-A Receive Data |
| EQEP1_INDEX | 9 | | | | | I/O | eQEP-1 Index |
| PMBUSA_SDA | 10 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| CANA_TX | 11 | | | | | O | CAN-A Transmit |
| EPWM6_A | 14 | | | | | O | ePWM-6 Output A |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|--------------|--------------|-------|-------|--------|--------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO18 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 18 |
| SPIA_CLK | 1 | | | | | I/O | SPI-A Clock |
| SCIB_TX | 2 | | | | | O | SCI-B Transmit Data |
| CANA_RX | 3 | | | | | I | CAN-A Receive |
| EPWM6_A | 5 | | | | | O | ePWM-6 Output A |
| I2CA_SCL | 6 | 50 | 41 | 33 | 21 | I/OD | I2C-A Open-Drain Bidirectional Clock |
| EQEP2_A | 9 | | | | | I | eQEP-2 Input A |
| PMBUSA_CTL | 10 | | | | | I/O | PMBus-A Control Signal - Slave Input/Master Output |
| XCLKOUT | 11 | | | | | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. |
| X2 | ALT | | | | | I/O | Crystal oscillator output. |
| GPIO19 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 19 |
| SPIA_STE | 1 | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| SCIB_RX | 2 | | | | | I | SCI-B Receive Data |
| CANA_TX | 3 | | | | | O | CAN-A Transmit |
| EPWM6_B | 5 | | | | | O | ePWM-6 Output B |
| I2CA_SDA | 6 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| EQEP2_B | 9 | | | | | I | eQEP-2 Input B |
| PMBUSA_ALERT | 10 | 51 | 42 | 34 | 22 | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| X1 | ALT | | | | | I/O | Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock. |
| ExtR | ALT2 | | | | | I | External resistor for internal oscillator. This can be used for greater clock accuracy. |
| GPIO20 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 20 This pin also has analog functions which are described in the ANALOG section of this table. |
| EQEP1_A | 1 | | | | | I | eQEP-1 Input A |
| CANA_TX | 3 | 33 | 27 | 22 | | O | CAN-A Transmit |
| SPIA_SIMO | 6 | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| MCAN_TX | 9 | | | | | O | CAN/CAN FD Transmit |
| I2CA_SCL | 11 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SCIC_TX | 15 | | | | | O | SCI-C Transmit Data |
| GPIO21 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 21 This pin also has analog functions which are described in the ANALOG section of this table. |
| EQEP1_B | 1 | | | | | I | eQEP-1 Input B |
| CANA_RX | 3 | 34 | 28 | | | I | CAN-A Receive |
| SPIA_SOMI | 6 | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| MCAN_RX | 9 | | | | | I | CAN/CAN FD Receive |
| I2CA_SDA | 11 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| SCIC_RX | 15 | | | | | I | SCI-C Receive Data |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|--------------|--------------|-------|-------|--------|--------|----------|-----------------------------------------------------------------|
| GPIO22 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 22 |
| EQEP1_STROBE | 1 | | | | | I/O | eQEP-1 Strobe |
| SCIB_TX | 3 | 67 | 56 | | | O | SCI-B Transmit Data |
| LINA_TX | 9 | | | | | O | LIN-A Transmit |
| EPWM4_A | 14 | | | | | O | ePWM-4 Output A |
| GPIO23 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 23 |
| EQEP1_INDEX | 1 | | | | | I/O | eQEP-1 Index |
| SCIB_RX | 3 | 65 | 54 | | | I | SCI-B Receive Data |
| LINA_RX | 9 | | | | | I | LIN-A Receive |
| EPWM4_B | 14 | | | | | O | ePWM-4 Output B |
| GPIO24 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 24 |
| OUTPUTXBAR1 | 1 | | | | | O | Output X-BAR Output 1 |
| EQEP2_A | 2 | | | | | I | eQEP-2 Input A |
| SPIA_STE | 3 | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| EPWM4_A | 5 | 41 | 35 | 27 | 15 | O | ePWM-4 Output A |
| SPIA_SIMO | 6 | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| PMBUSA_SCL | 10 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SCIA_TX | 11 | | | | | O | SCI-A Transmit Data |
| ERRORSTS | 13 | | | | | O | Error Status Output. This signal requires an external pulldown. |
| GPIO25 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 25 |
| OUTPUTXBAR2 | 1 | | | | | O | Output X-BAR Output 2 |
| EQEP2_B | 2 | 42 | | | | I | eQEP-2 Input B |
| EQEP1_A | 5 | | | | | I | eQEP-1 Input A |
| PMBUSA_SDA | 10 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SCIA_RX | 11 | | | | | I | SCI-A Receive Data |
| GPIO26 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 26 |
| OUTPUTXBAR3 | 1, 5 | | | | | O | Output X-BAR Output 3 |
| EQEP2_INDEX | 2 | 43 | | | | I/O | eQEP-2 Index |
| PMBUSA_CTL | 10 | | | | | I/O | PMBus-A Control Signal - Slave Input/Master Output |
| I2CA_SDA | 11 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| GPIO27 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 27 |
| OUTPUTXBAR4 | 1, 5 | | | | | O | Output X-BAR Output 4 |
| EQEP2_STROBE | 2 | 44 | | | | I/O | eQEP-2 Strobe |
| PMBUSA_ALERT | 10 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| I2CA_SCL | 11 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|--------------|--------------|-------|-------|--------|--------|----------|-----------------------------------------------------------------------------------------------------------------------------|
| GPIO28 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 28 This pin also has analog functions which are described in the ANALOG section of this table. |
| SCIA_RX | 1 | | | | | I | SCI-A Receive Data |
| EPWM7_A | 3 | | | | | O | ePWM-7 Output A |
| OUTPUTXBAR5 | 5 | | | | | O | Output X-BAR Output 5 |
| EQEP1_A | 6 | 4 | 2 | 2 | 32 | I | eQEP-1 Input A |
| EQEP2_STROBE | 9 | | | | | I/O | eQEP-2 Strobe |
| LINA_TX | 10 | | | | | O | LIN-A Transmit |
| SPIA_CLK | 11 | | | | | I/O | SPI-A Clock |
| ERRORSTS | 13 | | | | | O | Error Status Output. This signal requires an external pulldown. |
| I2CB_SDA | 14 | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| GPIO29 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 29 |
| SCIA_TX | 1 | | | | | O | SCI-A Transmit Data |
| EPWM7_B | 3 | | | | | O | ePWM-7 Output B |
| OUTPUTXBAR6 | 5 | | | | | O | Output X-BAR Output 6 |
| EQEP1_B | 6 | | | | | I | eQEP-1 Input B |
| EQEP2_INDEX | 9 | 3 | 1 | 1 | 31 | I/O | eQEP-2 Index |
| LINA_RX | 10 | | | | | I | LIN-A Receive |
| SPIA_STE | 11 | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| ERRORSTS | 13 | | | | | O | Error Status Output. This signal requires an external pulldown. |
| I2CB_SCL | 14 | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| GPIO30 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 30 |
| CANA_RX | 1 | | | | | I | CAN-A Receive |
| OUTPUTXBAR7 | 5 | | | | | O | Output X-BAR Output 7 |
| EQEP1_STROBE | 6 | 1 | | | | I/O | eQEP-1 Strobe |
| MCAN_RX | 10 | | | | | I | CAN/CAN FD Receive |
| EPWM1_A | 11 | | | | | O | ePWM-1 Output A |
| GPIO31 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 31 |
| CANA_TX | 1 | | | | | O | CAN-A Transmit |
| OUTPUTXBAR8 | 5 | | | | | O | Output X-BAR Output 8 |
| EQEP1_INDEX | 6 | 2 | | | | I/O | eQEP-1 Index |
| MCAN_TX | 10 | | | | | O | CAN/CAN FD Transmit |
| EPWM1_B | 11 | | | | | O | ePWM-1 Output B |
| GPIO32 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 32 |
| I2CA_SDA | 1 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| EQEP1_INDEX | 2 | | | | | I/O | eQEP-1 Index |
| SPIA_CLK | 3 | | | | | I/O | SPI-A Clock |
| EPWM4_B | 5 | 49 | 40 | 32 | 20 | O | ePWM-4 Output B |
| LINA_TX | 6 | | | | | O | LIN-A Transmit |
| CANA_TX | 10 | | | | | O | CAN-A Transmit |
| PMBUSA_SDA | 11 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| ADCSOCBO | 13 | | | | | O | ADC Start of Conversion B for External ADC |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|--------------|--------------|-------|-------|--------|--------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO33 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 33 |
| I2CA_SCL | 1 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| OUTPUTXBAR4 | 5 | | | | | O | Output X-BAR Output 4 |
| LINA_RX | 6 | 38 | 32 | 25 | | I | LIN-A Receive |
| CANA_RX | 10 | | | | | I | CAN-A Receive |
| EQEP2_B | 11 | | | | | I | eQEP-2 Input B |
| ADCSOAO | 13 | | | | | O | ADC Start of Conversion A for External ADC |
| GPIO34 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 34 |
| OUTPUTXBAR1 | 1 | | | | | O | Output X-BAR Output 1 |
| PMBUSA_SDA | 6 | 77 | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| I2CB_SDA | 14 | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| GPIO35 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 35 |
| SCIA_RX | 1 | | | | | I | SCI-A Receive Data |
| SPIA_SOMI | 2 | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| I2CA_SDA | 3 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| CANA_RX | 5 | | | | | I | CAN-A Receive |
| PMBUSA_SCL | 6 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| LINA_RX | 7 | | | | | I | LIN-A Receive |
| EQEP1_A | 9 | 48 | 39 | 31 | 19 | I | eQEP-1 Input A |
| PMBUSA_CTL | 10 | | | | | I/O | PMBus-A Control Signal - Slave Input/Master Output |
| EPWM5_B | 11 | | | | | O | ePWM-5 Output B |
| TDI | 15 | | | | | I | JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input. |
| GPIO37 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 37 |
| OUTPUTXBAR2 | 1 | | | | | O | Output X-BAR Output 2 |
| SPIA_STE | 2 | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| I2CA_SCL | 3 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SCIA_TX | 5 | | | | | O | SCI-A Transmit Data |
| CANA_TX | 6 | | | | | O | CAN-A Transmit |
| LINA_TX | 7 | | | | | O | LIN-A Transmit |
| EQEP1_B | 9 | | | | | I | eQEP-1 Input B |
| PMBUSA_ALERT | 10 | 46 | 37 | 29 | 17 | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| EPWM5_A | 11 | | | | | O | ePWM-5 Output A |
| TDO | 15 | | | | | O | JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|--------------|--------------|-------|-------|--------|--------|----------|----------------------------------------------------|
| GPIO39 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 39 |
| MCAN_RX | 6 | | | | | I | CAN/CAN FD Receive |
| EQEP2_INDEX | 9 | | | | | I/O | eQEP-2 Index |
| SYNCOUT | 13 | | | | | O | External ePWM Synchronization Pulse |
| EQEP1_INDEX | 14 | | | | | I/O | eQEP-1 Index |
| GPIO40 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 40 |
| EPWM2_B | 5 | | | | | O | ePWM-2 Output B |
| PMBUSA_SDA | 6 | 64 | 53 | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SCIB_TX | 9 | | | | | O | SCI-B Transmit Data |
| EQEP1_A | 10 | | | | | I | eQEP-1 Input A |
| GPIO41 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 41 |
| EPWM7_A | 1 | | | | | O | ePWM-7 Output A |
| EPWM2_A | 5 | | | | | O | ePWM-2 Output A |
| PMBUSA_SCL | 6 | 66 | 55 | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SCIB_RX | 9 | | | | | I | SCI-B Receive Data |
| EQEP1_B | 10 | | | | | I | eQEP-1 Input B |
| GPIO42 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 42 |
| LINA_RX | 2 | | | | | I | LIN-A Receive |
| OUTPUTXBAR5 | 3 | | | | | O | Output X-BAR Output 5 |
| PMBUSA_CTL | 5 | 57 | | | | I/O | PMBus-A Control Signal - Slave Input/Master Output |
| I2CA_SDA | 6 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| SCIC_RX | 7 | | | | | I | SCI-C Receive Data |
| EQEP1_STROBE | 10 | | | | | I/O | eQEP-1 Strobe |
| GPIO43 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 43 |
| OUTPUTXBAR6 | 3 | | | | | O | Output X-BAR Output 6 |
| PMBUSA_ALERT | 5, 9 | 54 | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| I2CA_SCL | 6 | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SCIC_TX | 7 | | | | | O | SCI-C Transmit Data |
| EQEP1_INDEX | 10 | | | | | I/O | eQEP-1 Index |
| GPIO44 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 44 |
| OUTPUTXBAR7 | 3 | | | | | O | Output X-BAR Output 7 |
| EQEP1_A | 5 | 69 | | 44 | | I | eQEP-1 Input A |
| PMBUSA_SDA | 6 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| PMBUSA_CTL | 9 | | | | | I/O | PMBus-A Control Signal - Slave Input/Master Output |
| GPIO45 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 45 |
| OUTPUTXBAR8 | 3 | 73 | | | | O | Output X-BAR Output 8 |
| PMBUSA_ALERT | 9 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| GPIO46 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 46 |
| LINA_TX | 3 | 6 | | | | O | LIN-A Transmit |
| MCAN_TX | 5 | | | | | O | CAN/CAN FD Transmit |
| PMBUSA_SDA | 9 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|--------------|--------------|-------|-------|--------|--------|----------|------------------------------------------------------------------------------------------------------------------------------|
| GPIO48 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 48 |
| OUTPUTXBAR3 | 1 | | | | | O | Output X-BAR Output 3 |
| CANA_TX | 3 | 31 | | | | O | CAN-A Transmit |
| MCAN_TX | 5 | | | | | O | CAN/CAN FD Transmit |
| SCIA_TX | 6 | | | | | O | SCI-A Transmit Data |
| PMBUSA_SDA | 9 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| GPIO49 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 49 |
| OUTPUTXBAR4 | 1 | | | | | O | Output X-BAR Output 4 |
| CANA_RX | 3 | 32 | | | | I | CAN-A Receive |
| MCAN_RX | 5 | | | | | I | CAN/CAN FD Receive |
| SCIA_RX | 6 | | | | | I | SCI-A Receive Data |
| LINA_RX | 9 | | | | | I | LIN-A Receive |
| GPIO224 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 224 This pin also has analog functions which are described in the ANALOG section of this table. |
| OUTPUTXBAR3 | 5 | | | | | O | Output X-BAR Output 3 |
| SPIA_SIMO | 6 | 13 | 9 | 6 | 4 | I/O | SPI-A Slave In, Master Out (SIMO) |
| EPWM1_A | 9 | | | | | O | ePWM-1 Output A |
| CANA_TX | 10 | | | | | O | CAN-A Transmit |
| EQEP1_A | 11 | | | | | I | eQEP-1 Input A |
| SCIC_TX | 14 | | | | | O | SCI-C Transmit Data |
| GPIO226 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 226 This pin also has analog functions which are described in the ANALOG section of this table. |
| LINA_RX | 3 | | | | | I | LIN-A Receive |
| EPWM6_A | 5 | 11 | 7 | 4 | 2 | O | ePWM-6 Output A |
| SPIA_CLK | 6 | | | | | I/O | SPI-A Clock |
| EPWM1_B | 9 | | | | | O | ePWM-1 Output B |
| EQEP1_STROBE | 11 | | | | | I/O | eQEP-1 Strobe |
| SCIC_RX | 14 | | | | | I | SCI-C Receive Data |
| GPIO227 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 227 This pin also has analog functions which are described in the ANALOG section of this table. |
| I2CB_SCL | 1 | 28 | 24 | 20 | 13 | I/OD | I2C-B Open-Drain Bidirectional Clock |
| EPWM3_A | 3 | | | | | O | ePWM-3 Output A |
| OUTPUTXBAR1 | 5 | | | | | O | Output X-BAR Output 1 |
| EPWM2_B | 6 | | | | | O | ePWM-2 Output B |
| GPIO228 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 228 This pin also has analog functions which are described in the ANALOG section of this table. |
| ADCSOCAO | 3 | | | | | O | ADC Start of Conversion A for External ADC |
| CANA_TX | 5 | 10 | 6 | 4 | 2 | O | CAN-A Transmit |
| SPIA_SOMI | 6 | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| EPWM2_B | 9 | | | | | O | ePWM-2 Output B |
| EQEP1_B | 11 | | | | | I | eQEP-1 Input B |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|------------------------------|--------------|-----------|-----------|--------|--------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO230 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 230 This pin also has analog functions which are described in the ANALOG section of this table. |
| I2CB_SDA | 1 | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| EPWM3_B | 3 | 29 | 25 | 21 | 13 | O | ePWM-3 Output B |
| CANA_RX | 5 | | | | | I | CAN-A Receive |
| EPWM2_A | 6 | | | | | O | ePWM-2 Output A |
| I2CA_SDA | 7 | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| PMBUSA_SCL | 9 | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| GPIO242 | 0, 4, 8, 12 | | | | | I/O | General-Purpose Input Output 242 This pin also has analog functions which are described in the ANALOG section of this table. |
| OUTPUTXBAR2 | 5 | | | | | O | Output X-BAR Output 2 |
| SPIA_STE | 6 | 12 | 8 | 5 | 3 | I/O | SPI-A Slave Transmit Enable (STE) |
| EPWM4_A | 9 | | | | | O | ePWM-4 Output A |
| CANA_RX | 10 | | | | | I | CAN-A Receive |
| EQEP1_INDEX | 11 | | | | | I/O | eQEP-1 Index |
| TEST, JTAG, AND RESET | | | | | | | |
| TCK | | 45 | 36 | 28 | 16 | I | JTAG test clock with internal pullup. |
| TMS | | 47 | 38 | 30 | 18 | I/O | JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation. |
| XRSn | | 5 | 3 | 3 | 1 | I/OD | Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device. |
| POWER AND GROUND | | | | | | | |
| VDD | | 8, 53, 71 | 4, 44, 59 | 36, 45 | 24 | | 1.2-V Digital Logic Power Pins. See the Power Management Module (PMM) section for usage details. |
| VDDA | | 26 | 22 | 18 | 11 | | 3.3-V Analog Power Pins. Place a minimum 2.2-μF decoupling capacitor on each pin. On the 32 QFN package, VREFHI is internally tied to VDDA. See the Power Management Module (PMM) section for usage details. |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 80 PN | 64 PM | 48 PHP | 32 RHB | PIN TYPE | DESCRIPTION |
|-------------|--------------|---------------|---------------|--------|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------|
| VDDIO | | 7, 52, 72 | 43, 60 | 35, 46 | 23 | | 3.3-V Digital I/O Power Pins. See the Power Management Module (PMM) section for usage details. |
| VREGENZ | | 56 | 46 | 37 | 25 | I | Internal voltage regulator enable with internal pulldown. Tie low to VSS to enable internal VREG. Tie high to VDDIO to use an external supply. |
| VSS | | 9, 30, 55, 70 | 5, 26, 45, 58 | PAD | PAD | | Digital Ground. For QFN packages, the ground pad on the bottom of the package must be soldered to the ground plane of the PCB. |
| VSSA | | 25 | 21 | 17 | 10 | | Analog Ground |

5.3 Signal Descriptions

5.3.1 Analog Signals

Table 5-2. Analog Signals

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 80 PN | 64 PM | 48 PHP | 32 RHB |
|-------------|----------|---------------------------------------|-------|-------|--------|--------|
| A0 | I | ADC-A Input 0 | 19 | 15 | 11 | 7 |
| A1 | I | ADC-A Input 1 | 18 | 14 | 10 | 7 |
| A2 | I | ADC-A Input 2 | 13 | 9 | 6 | 4 |
| A3 | I | ADC-A Input 3 | 12 | 8 | 5 | 3 |
| A4 | I | ADC-A Input 4 | 27 | 23 | 19 | 12 |
| A5 | I | ADC-A Input 5 | 17 | 13 | 9 | 6 |
| A6 | I | ADC-A Input 6 | 10 | 6 | 4 | 2 |
| A7 | I | ADC-A Input 7 | 23 | 19 | 15 | 8 |
| A8 | I | ADC-A Input 8 | 24 | 20 | 16 | 9 |
| A9 | I | ADC-A Input 9 | 28 | 24 | 20 | 13 |
| A10 | I | ADC-A Input 10 | 29 | 25 | 21 | 13 |
| A11 | I | ADC-A Input 11 | 16 | 12 | 8 | 6 |
| A12 | I | ADC-A Input 12 | 22 | 18 | 14 | 8 |
| A14 | I | ADC-A Input 14 | 15 | 11 | 7 | 5 |
| A15 | I | ADC-A Input 15 | 14 | 10 | 7 | 5 |
| A16 | I | ADC-A Input 16 | 4 | 2 | 2 | 32 |
| A17 | I | ADC-A Input 17 | 33 | 27 | 22 | |
| A18 | I | ADC-A Input 18 | 34 | 28 | | |
| A19 | I | ADC-A Input 19 | 35 | 29 | 23 | |
| A20 | I | ADC-A Input 20 | 36 | 30 | 24 | |
| AIO225 | I | Analog Pin Used For Digital Input 225 | 27 | 23 | 19 | 12 |
| AIO231 | I | Analog Pin Used For Digital Input 231 | 19 | 15 | 11 | 7 |
| AIO232 | I | Analog Pin Used For Digital Input 232 | 18 | 14 | 10 | 7 |
| AIO233 | I | Analog Pin Used For Digital Input 233 | 14 | 10 | 7 | 5 |
| AIO237 | I | Analog Pin Used For Digital Input 237 | 16 | 12 | 8 | 6 |
| AIO238 | I | Analog Pin Used For Digital Input 238 | 22 | 18 | 14 | 8 |
| AIO239 | I | Analog Pin Used For Digital Input 239 | 15 | 11 | 7 | 5 |
| AIO241 | I | Analog Pin Used For Digital Input 241 | 24 | 20 | 16 | 9 |
| AIO244 | I | Analog Pin Used For Digital Input 244 | 17 | 13 | 9 | 6 |
| AIO245 | I | Analog Pin Used For Digital Input 245 | 23 | 19 | 15 | 8 |
| C0 | I | ADC-C Input 0 | 16 | 12 | 8 | 6 |
| C1 | I | ADC-C Input 1 | 22 | 18 | 14 | 8 |
| C2 | I | ADC-C Input 2 | 17 | 13 | 9 | 6 |
| C3 | I | ADC-C Input 3 | 23 | 19 | 15 | 8 |
| C4 | I | ADC-C Input 4 | 15 | 11 | 7 | 5 |
| C5 | I | ADC-C Input 5 | 12 | 8 | 5 | 3 |
| C6 | I | ADC-C Input 6 | 11 | 7 | 4 | 2 |
| C7 | I | ADC-C Input 7 | 14 | 10 | 7 | 5 |
| C8 | I | ADC-C Input 8 | 28 | 24 | 20 | 13 |
| C9 | I | ADC-C Input 9 | 13 | 9 | 6 | 4 |
| C10 | I | ADC-C Input 10 | 29 | 25 | 21 | 13 |
| C11 | I | ADC-C Input 11 | 24 | 20 | 16 | 9 |

Table 5-2. Analog Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 80 PN | 64 PM | 48 PHP | 32 RHB |
|-------------|----------|------------------------------------------|-------|-------|--------|--------|
| C14 | I | ADC-C Input 14 | 27 | 23 | 19 | 12 |
| C15 | I | ADC-C Input 15 | 19 | 15 | 11 | 7 |
| C16 | I | ADC-C Input 16 | 4 | 2 | 2 | 32 |
| C17 | I | ADC-C Input 17 | 33 | 27 | 22 | |
| C18 | I | ADC-C Input 18 | 34 | 28 | | |
| C19 | I | ADC-C Input 19 | 35 | 29 | 23 | |
| C20 | I | ADC-C Input 20 | 36 | 30 | 24 | |
| CMP1_DACL | I | CMPSS-1 Low DAC Output | 19 | 15 | 11 | 7 |
| CMP1_HN0 | I | CMPSS-1 High Comparator Negative Input 0 | 14 | 10 | 7 | 5 |
| CMP1_HN1 | I | CMPSS-1 High Comparator Negative Input 1 | 16 | 12 | 8 | 6 |
| CMP1_HP0 | I | CMPSS-1 High Comparator Positive Input 0 | 13 | 9 | 6 | 4 |
| CMP1_HP1 | I | CMPSS-1 High Comparator Positive Input 1 | 16 | 12 | 8 | 6 |
| CMP1_HP2 | I | CMPSS-1 High Comparator Positive Input 2 | 10 | 6 | 4 | 2 |
| CMP1_HP3 | I | CMPSS-1 High Comparator Positive Input 3 | 14 | 10 | 7 | 5 |
| CMP1_HP4 | I | CMPSS-1 High Comparator Positive Input 4 | 18 | 14 | 10 | 7 |
| CMP1_LN0 | I | CMPSS-1 Low Comparator Negative Input 0 | 14 | 10 | 7 | 5 |
| CMP1_LN1 | I | CMPSS-1 Low Comparator Negative Input 1 | 16 | 12 | 8 | 6 |
| CMP1_LP0 | I | CMPSS-1 Low Comparator Positive Input 0 | 13 | 9 | 6 | 4 |
| CMP1_LP1 | I | CMPSS-1 Low Comparator Positive Input 1 | 16 | 12 | 8 | 6 |
| CMP1_LP2 | I | CMPSS-1 Low Comparator Positive Input 2 | 10 | 6 | 4 | 2 |
| CMP1_LP3 | I | CMPSS-1 Low Comparator Positive Input 3 | 14 | 10 | 7 | 5 |
| CMP1_LP4 | I | CMPSS-1 Low Comparator Positive Input 4 | 18 | 14 | 10 | 7 |
| CMP2_HN0 | I | CMPSS-2 High Comparator Negative Input 0 | 29 | 25 | 21 | 13 |
| CMP2_HN1 | I | CMPSS-2 High Comparator Negative Input 1 | 22 | 18 | 14 | 8 |
| CMP2_HP0 | I | CMPSS-2 High Comparator Positive Input 0 | 27 | 23 | 19 | 12 |
| CMP2_HP1 | I | CMPSS-2 High Comparator Positive Input 1 | 22 | 18 | 14 | 8 |
| CMP2_HP2 | I | CMPSS-2 High Comparator Positive Input 2 | 28 | 24 | 20 | 13 |
| CMP2_HP3 | I | CMPSS-2 High Comparator Positive Input 3 | 29 | 25 | 21 | 13 |
| CMP2_HP4 | I | CMPSS-2 High Comparator Positive Input 4 | 24 | 20 | 16 | 9 |

Table 5-2. Analog Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 80 PN | 64 PM | 48 PHP | 32 RHB |
|-------------|----------|------------------------------------------|-------|-------|--------|--------|
| CMP2_LN0 | I | CMPSS-2 Low Comparator Negative Input 0 | 29 | 25 | 21 | 13 |
| CMP2_LN1 | I | CMPSS-2 Low Comparator Negative Input 1 | 22 | 18 | 14 | 8 |
| CMP2_LP0 | I | CMPSS-2 Low Comparator Positive Input 0 | 27 | 23 | 19 | 12 |
| CMP2_LP1 | I | CMPSS-2 Low Comparator Positive Input 1 | 22 | 18 | 14 | 8 |
| CMP2_LP2 | I | CMPSS-2 Low Comparator Positive Input 2 | 28 | 24 | 20 | 13 |
| CMP2_LP3 | I | CMPSS-2 Low Comparator Positive Input 3 | 29 | 25 | 21 | 13 |
| CMP2_LP4 | I | CMPSS-2 Low Comparator Positive Input 4 | 24 | 20 | 16 | 9 |
| CMP3_HN0 | I | CMPSS-3 High Comparator Negative Input 0 | 12 | 8 | 5 | 3 |
| CMP3_HN1 | I | CMPSS-3 High Comparator Negative Input 1 | 17 | 13 | 9 | 6 |
| CMP3_HP0 | I | CMPSS-3 High Comparator Positive Input 0 | 11 | 7 | 4 | 2 |
| CMP3_HP1 | I | CMPSS-3 High Comparator Positive Input 1 | 17 | 13 | 9 | 6 |
| CMP3_HP2 | I | CMPSS-3 High Comparator Positive Input 2 | 19 | 15 | 11 | 7 |
| CMP3_HP3 | I | CMPSS-3 High Comparator Positive Input 3 | 12 | 8 | 5 | 3 |
| CMP3_HP4 | I | CMPSS-3 High Comparator Positive Input 4 | 15 | 11 | 7 | 5 |
| CMP3_LN0 | I | CMPSS-3 Low Comparator Negative Input 0 | 12 | 8 | 5 | 3 |
| CMP3_LN1 | I | CMPSS-3 Low Comparator Negative Input 1 | 17 | 13 | 9 | 6 |
| CMP3_LP0 | I | CMPSS-3 Low Comparator Positive Input 0 | 11 | 7 | 4 | 2 |
| CMP3_LP1 | I | CMPSS-3 Low Comparator Positive Input 1 | 17 | 13 | 9 | 6 |
| CMP3_LP2 | I | CMPSS-3 Low Comparator Positive Input 2 | 19 | 15 | 11 | 7 |
| CMP3_LP3 | I | CMPSS-3 Low Comparator Positive Input 3 | 12 | 8 | 5 | 3 |
| CMP3_LP4 | I | CMPSS-3 Low Comparator Positive Input 4 | 15 | 11 | 7 | 5 |
| CMP4_HN0 | I | CMPSS-4 High Comparator Negative Input 0 | 27 | 23 | 19 | 12 |
| CMP4_HN1 | I | CMPSS-4 High Comparator Negative Input 1 | 23 | 19 | 15 | 8 |
| CMP4_HP0 | I | CMPSS-4 High Comparator Positive Input 0 | 28 | 24 | 20 | 13 |
| CMP4_HP1 | I | CMPSS-4 High Comparator Positive Input 1 | 23 | 19 | 15 | 8 |
| CMP4_HP2 | I | CMPSS-4 High Comparator Positive Input 2 | 22 | 18 | 14 | 8 |

Table 5-2. Analog Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 80 PN | 64 PM | 48 PHP | 32 RHB |
|-------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|--------|--------|
| CMP4_HP3 | I | CMPSS-4 High Comparator Positive Input 3 | 27 | 23 | 19 | 12 |
| CMP4_HP4 | I | CMPSS-4 High Comparator Positive Input 4 | 24 | 20 | 16 | 9 |
| CMP4_LN0 | I | CMPSS-4 Low Comparator Negative Input 0 | 27 | 23 | 19 | 12 |
| CMP4_LN1 | I | CMPSS-4 Low Comparator Negative Input 1 | 23 | 19 | 15 | 8 |
| CMP4_LP0 | I | CMPSS-4 Low Comparator Positive Input 0 | 28 | 24 | 20 | 13 |
| CMP4_LP1 | I | CMPSS-4 Low Comparator Positive Input 1 | 23 | 19 | 15 | 8 |
| CMP4_LP2 | I | CMPSS-4 Low Comparator Positive Input 2 | 22 | 18 | 14 | 8 |
| CMP4_LP3 | I | CMPSS-4 Low Comparator Positive Input 3 | 27 | 23 | 19 | 12 |
| CMP4_LP4 | I | CMPSS-4 Low Comparator Positive Input 4 | 24 | 20 | 16 | 9 |
| VREFHI | I | ADC High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2- μ F capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. On the 32 QFN package, VREFHI is internally tied to VDDA. | 20 | 16 | 12 | |
| VREFLO | I | ADC Low Reference | 21 | 17 | 13 | |

5.3.2 Digital Signals

Table 5-3. Digital Signals

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 80 PN | 64 PM | 48 PHP | 32 RHB |
|--------------|----------|-----------------------------------------------------------------------------------------|---------------------------------------------------|---------------------------------------------------|-------------------------------------------|--------------------------------------|-------------------------------|
| ADCSOCAO | O | ADC Start of Conversion A for External ADC | 8, 33, 228 | 10, 38, 58 | 6, 32, 47 | 4, 25 | 2 |
| ADCSOCBO | O | ADC Start of Conversion B for External ADC | 10, 32 | 49, 76 | 40, 63 | 32 | 20 |
| CANA_RX | I | CAN-A Receive | 0, 3, 5, 11, 12, 18, 21, 30, 33, 35, 49, 230, 242 | 1, 12, 29, 32, 34, 36, 37, 38, 48, 50, 60, 63, 74 | 8, 25, 28, 30, 31, 32, 39, 41, 49, 52, 61 | 5, 21, 24, 25, 31, 33, 39, 42, 47 | 3, 13, 14, 19, 21, 26, 28, 30 |
| CANA_TX | O | CAN-A Transmit | 2, 4, 7, 13, 17, 19, 20, 31, 32, 37, 48, 224, 228 | 2, 10, 13, 31, 33, 35, 40, 46, 49, 51, 59, 61, 68 | 6, 9, 27, 29, 34, 37, 40, 42, 48, 50, 57 | 4, 6, 22, 23, 29, 32, 34, 38, 40, 43 | 2, 4, 17, 20, 22, 29 |
| EPWM1_A | O | ePWM-1 Output A | 0, 4, 30, 224 | 1, 13, 59, 63 | 9, 48, 52 | 6, 38, 42 | 4, 28 |
| EPWM1_B | O | ePWM-1 Output B | 1, 5, 31, 226 | 2, 11, 62, 74 | 7, 51, 61 | 4, 41, 47 | 2, 27, 30 |
| EPWM2_A | O | ePWM-2 Output A | 2, 6, 7, 41, 230 | 29, 61, 66, 68, 80 | 25, 50, 55, 57, 64 | 21, 40, 43, 48 | 13, 29 |
| EPWM2_B | O | ePWM-2 Output B | 3, 7, 40, 227, 228 | 10, 28, 60, 64, 68 | 6, 24, 49, 53, 57 | 4, 20, 39, 43 | 2, 13, 26, 29 |
| EPWM3_A | O | ePWM-3 Output A | 0, 4, 14, 227 | 28, 59, 63, 79 | 24, 48, 52 | 20, 38, 42 | 13, 28 |
| EPWM3_B | O | ePWM-3 Output B | 1, 5, 15, 230 | 29, 62, 74, 78 | 25, 51, 61 | 21, 41, 47 | 13, 27, 30 |
| EPWM4_A | O | ePWM-4 Output A | 2, 6, 22, 24, 242 | 12, 41, 61, 67, 80 | 8, 35, 50, 56, 64 | 5, 27, 40, 48 | 3, 15 |
| EPWM4_B | O | ePWM-4 Output B | 3, 7, 23, 32 | 49, 60, 65, 68 | 40, 49, 54, 57 | 32, 39, 43 | 20, 26, 29 |
| EPWM5_A | O | ePWM-5 Output A | 8, 16, 37 | 39, 46, 58 | 33, 37, 47 | 26, 29 | 17 |
| EPWM5_B | O | ePWM-5 Output B | 9, 17, 35 | 40, 48, 75 | 34, 39, 62 | 31 | 19 |
| EPWM6_A | O | ePWM-6 Output A | 10, 17, 18, 226 | 11, 40, 50, 76 | 7, 34, 41, 63 | 4, 33 | 2, 21 |
| EPWM6_B | O | ePWM-6 Output B | 11, 19 | 37, 51 | 31, 42 | 34 | 14, 22 |
| EPWM7_A | O | ePWM-7 Output A | 12, 28, 41 | 4, 36, 66 | 2, 30, 55 | 2, 24 | 32 |
| EPWM7_B | O | ePWM-7 Output B | 13, 29 | 3, 35 | 1, 29 | 1, 23 | 31 |
| EQEP1_A | I | eQEP-1 Input A | 6, 10, 20, 25, 28, 35, 40, 44, 224 | 4, 13, 33, 42, 48, 64, 69, 76, 80 | 2, 9, 27, 39, 53, 63, 64 | 2, 6, 22, 31, 44, 48 | 4, 19, 32 |
| EQEP1_B | I | eQEP-1 Input B | 7, 11, 21, 29, 37, 41, 228 | 3, 10, 34, 37, 46, 66, 68 | 1, 6, 28, 31, 37, 55, 57 | 1, 4, 29, 43 | 2, 14, 17, 29, 31 |
| EQEP1_INDEX | I/O | eQEP-1 Index | 0, 9, 13, 17, 23, 31, 32, 39, 43, 242 | 2, 12, 35, 40, 49, 54, 63, 65, 75 | 8, 29, 34, 40, 52, 54, 62 | 5, 23, 32, 42 | 3, 20, 28 |
| EQEP1_STROBE | I/O | eQEP-1 Strobe | 1, 8, 12, 16, 22, 30, 42, 226 | 1, 11, 36, 39, 57, 58, 62, 67 | 7, 30, 33, 47, 51, 56 | 4, 24, 26, 41 | 2, 27 |
| EQEP2_A | I | eQEP-2 Input A | 11, 14, 18, 24 | 37, 41, 50, 79 | 31, 35, 41 | 27, 33 | 14, 15, 21 |
| EQEP2_B | I | eQEP-2 Input B | 15, 16, 19, 25, 33 | 38, 39, 42, 51, 78 | 32, 33, 42 | 25, 26, 34 | 22 |
| EQEP2_INDEX | I/O | eQEP-2 Index | 26, 29, 39 | 3, 43 | 1 | 1 | 31 |
| EQEP2_STROBE | I/O | eQEP-2 Strobe | 4, 27, 28 | 4, 44, 59 | 2, 48 | 2, 38 | 32 |
| ERRORSTS | O | Error Status Output. This signal requires an external pulldown. | 24, 28, 29 | 3, 4, 41 | 1, 2, 35 | 1, 2, 27 | 15, 31, 32 |
| ExtR | I | External resistor for internal oscillator. This can be used for greater clock accuracy. | 19 | 51 | 42 | 34 | 22 |
| GPIO0 | I/O | General-Purpose Input Output 0 | 0 | 63 | 52 | 42 | 28 |
| GPIO1 | I/O | General-Purpose Input Output 1 | 1 | 62 | 51 | 41 | 27 |
| GPIO2 | I/O | General-Purpose Input Output 2 | 2 | 61 | 50 | 40 | |
| GPIO3 | I/O | General-Purpose Input Output 3 | 3 | 60 | 49 | 39 | 26 |
| GPIO4 | I/O | General-Purpose Input Output 4 | 4 | 59 | 48 | 38 | |
| GPIO5 | I/O | General-Purpose Input Output 5 | 5 | 74 | 61 | 47 | 30 |
| GPIO6 | I/O | General-Purpose Input Output 6 | 6 | 80 | 64 | 48 | |
| GPIO7 | I/O | General-Purpose Input Output 7 | 7 | 68 | 57 | 43 | 29 |
| GPIO8 | I/O | General-Purpose Input Output 8 | 8 | 58 | 47 | | |
| GPIO9 | I/O | General-Purpose Input Output 9 | 9 | 75 | 62 | | |
| GPIO10 | I/O | General-Purpose Input Output 10 | 10 | 76 | 63 | | |
| GPIO11 | I/O | General-Purpose Input Output 11 | 11 | 37 | 31 | | 14 |
| GPIO12 | I/O | General-Purpose Input Output 12 | 12 | 36 | 30 | 24 | |
| GPIO13 | I/O | General-Purpose Input Output 13 | 13 | 35 | 29 | 23 | |
| GPIO14 | I/O | General-Purpose Input Output 14 | 14 | 79 | | | |
| GPIO15 | I/O | General-Purpose Input Output 15 | 15 | 78 | | | |
| GPIO16 | I/O | General-Purpose Input Output 16 | 16 | 39 | 33 | 26 | |
| GPIO17 | I/O | General-Purpose Input Output 17 | 17 | 40 | 34 | | |

Table 5-3. Digital Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 80 PN | 64 PM | 48 PHP | 32 RHB |
|-------------|----------|--------------------------------------|---------------------------------------|----------------------------------------|--------------------------------|------------------------|------------------------|
| GPIO18 | I/O | General-Purpose Input Output 18 | 18 | 50 | 41 | 33 | 21 |
| GPIO19 | I/O | General-Purpose Input Output 19 | 19 | 51 | 42 | 34 | 22 |
| GPIO20 | I/O | General-Purpose Input Output 20 | 20 | 33 | 27 | 22 | |
| GPIO21 | I/O | General-Purpose Input Output 21 | 21 | 34 | 28 | | |
| GPIO22 | I/O | General-Purpose Input Output 22 | 22 | 67 | 56 | | |
| GPIO23 | I/O | General-Purpose Input Output 23 | 23 | 65 | 54 | | |
| GPIO24 | I/O | General-Purpose Input Output 24 | 24 | 41 | 35 | 27 | 15 |
| GPIO25 | I/O | General-Purpose Input Output 25 | 25 | 42 | | | |
| GPIO26 | I/O | General-Purpose Input Output 26 | 26 | 43 | | | |
| GPIO27 | I/O | General-Purpose Input Output 27 | 27 | 44 | | | |
| GPIO28 | I/O | General-Purpose Input Output 28 | 28 | 4 | 2 | 2 | 32 |
| GPIO29 | I/O | General-Purpose Input Output 29 | 29 | 3 | 1 | 1 | 31 |
| GPIO30 | I/O | General-Purpose Input Output 30 | 30 | 1 | | | |
| GPIO31 | I/O | General-Purpose Input Output 31 | 31 | 2 | | | |
| GPIO32 | I/O | General-Purpose Input Output 32 | 32 | 49 | 40 | 32 | 20 |
| GPIO33 | I/O | General-Purpose Input Output 33 | 33 | 38 | 32 | 25 | |
| GPIO34 | I/O | General-Purpose Input Output 34 | 34 | 77 | | | |
| GPIO35 | I/O | General-Purpose Input Output 35 | 35 | 48 | 39 | 31 | 19 |
| GPIO37 | I/O | General-Purpose Input Output 37 | 37 | 46 | 37 | 29 | 17 |
| GPIO39 | I/O | General-Purpose Input Output 39 | 39 | | | | |
| GPIO40 | I/O | General-Purpose Input Output 40 | 40 | 64 | 53 | | |
| GPIO41 | I/O | General-Purpose Input Output 41 | 41 | 66 | 55 | | |
| GPIO42 | I/O | General-Purpose Input Output 42 | 42 | 57 | | | |
| GPIO43 | I/O | General-Purpose Input Output 43 | 43 | 54 | | | |
| GPIO44 | I/O | General-Purpose Input Output 44 | 44 | 69 | | 44 | |
| GPIO45 | I/O | General-Purpose Input Output 45 | 45 | 73 | | | |
| GPIO46 | I/O | General-Purpose Input Output 46 | 46 | 6 | | | |
| GPIO48 | I/O | General-Purpose Input Output 48 | 48 | 31 | | | |
| GPIO49 | I/O | General-Purpose Input Output 49 | 49 | 32 | | | |
| GPIO224 | I/O | General-Purpose Input Output 224 | 224 | 13 | 9 | 6 | 4 |
| GPIO226 | I/O | General-Purpose Input Output 226 | 226 | 11 | 7 | 4 | 2 |
| GPIO227 | I/O | General-Purpose Input Output 227 | 227 | 28 | 24 | 20 | 13 |
| GPIO228 | I/O | General-Purpose Input Output 228 | 228 | 10 | 6 | 4 | 2 |
| GPIO230 | I/O | General-Purpose Input Output 230 | 230 | 29 | 25 | 21 | 13 |
| GPIO242 | I/O | General-Purpose Input Output 242 | 242 | 12 | 8 | 5 | 3 |
| I2CA_SCL | I/OD | I2C-A Open-Drain Bidirectional Clock | 1, 4, 8, 18, 20, 27, 33, 37, 43 | 33, 38, 44, 46, 50, 54, 58, 59, 62 | 27, 32, 37, 41, 47, 48, 51 | 22, 25, 29, 33, 38, 41 | 17, 21, 27 |
| I2CA_SDA | I/OD | I2C-A Open-Drain Bidirectional Data | 0, 5, 10, 19, 21, 26, 32, 35, 42, 230 | 29, 34, 43, 48, 49, 51, 57, 63, 74, 76 | 25, 28, 39, 40, 42, 52, 61, 63 | 21, 31, 32, 34, 42, 47 | 13, 19, 20, 22, 28, 30 |
| I2CB_SCL | I/OD | I2C-B Open-Drain Bidirectional Clock | 3, 9, 15, 29, 227 | 3, 28, 60, 75, 78 | 1, 24, 49, 62 | 1, 20, 39 | 13, 26, 31 |
| I2CB_SDA | I/OD | I2C-B Open-Drain Bidirectional Data | 2, 14, 28, 34, 230 | 4, 29, 61, 77, 79 | 2, 25, 50 | 2, 21, 40 | 13, 32 |
| LINA_RX | I | LIN-A Receive | 23, 29, 33, 35, 42, 49, 226 | 3, 11, 32, 38, 48, 57, 65 | 1, 7, 32, 39, 54 | 1, 4, 25, 31 | 2, 19, 31 |
| LINA_TX | O | LIN-A Transmit | 22, 28, 32, 37, 46 | 4, 6, 46, 49, 67 | 2, 37, 40, 56 | 2, 29, 32 | 17, 20, 32 |
| MCAN_RX | I | CAN/CAN FD Receive | 0, 5, 12, 21, 30, 39, 49 | 1, 32, 34, 36, 63, 74 | 28, 30, 52, 61 | 24, 42, 47 | 28, 30 |
| MCAN_TX | O | CAN/CAN FD Transmit | 1, 4, 13, 20, 31, 46, 48 | 2, 6, 31, 33, 35, 59, 62 | 27, 29, 48, 51 | 22, 23, 38, 41 | 27 |
| OUTPUTXBAR1 | O | Output X-BAR Output 1 | 2, 24, 34, 227 | 28, 41, 61, 77 | 24, 35, 50 | 20, 27, 40 | 13, 15 |
| OUTPUTXBAR2 | O | Output X-BAR Output 2 | 3, 25, 37, 242 | 12, 42, 46, 60 | 8, 37, 49 | 5, 29, 39 | 3, 17, 26 |
| OUTPUTXBAR3 | O | Output X-BAR Output 3 | 4, 5, 14, 26, 48, 224 | 13, 31, 43, 59, 74, 79 | 9, 48, 61 | 6, 38, 47 | 4, 30 |
| OUTPUTXBAR4 | O | Output X-BAR Output 4 | 6, 15, 27, 33, 49 | 32, 38, 44, 78, 80 | 32, 64 | 25, 48 | |
| OUTPUTXBAR5 | O | Output X-BAR Output 5 | 7, 28, 42 | 4, 57, 68 | 2, 57 | 2, 43 | 29, 32 |
| OUTPUTXBAR6 | O | Output X-BAR Output 6 | 9, 29, 43 | 3, 54, 75 | 1, 62 | 1 | 31 |
| OUTPUTXBAR7 | O | Output X-BAR Output 7 | 0, 11, 16, 30, 44 | 1, 37, 39, 63, 69 | 31, 33, 52 | 26, 42, 44 | 14, 28 |
| OUTPUTXBAR8 | O | Output X-BAR Output 8 | 17, 31, 45 | 2, 40, 73 | 34 | | |

Table 5-3. Digital Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 80 PN | 64 PM | 48 PHP | 32 RHB |
|--------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------|---------------------------------------|-------------------------------|---------------------------|-------------------------------|
| PMBUSA_ALERT | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal | 13, 19, 27, 37, 43, 45 | 35, 44, 46, 51, 54, 73 | 29, 37, 42 | 23, 29, 34 | 17, 22 |
| PMBUSA_CTL | I/O | PMBus-A Control Signal - Slave Input/Master Output | 12, 18, 26, 35, 42, 44 | 36, 43, 48, 50, 57, 69 | 30, 39, 41 | 24, 31, 33, 44 | 19, 21 |
| PMBUSA_SCL | I/OD | PMBus-A Open-Drain Bidirectional Clock | 3, 15, 16, 24, 35, 41, 230 | 29, 39, 41, 48, 60, 66, 78 | 25, 33, 35, 39, 49, 55 | 21, 26, 27, 31, 39 | 13, 15, 19, 26 |
| PMBUSA_SDA | I/OD | PMBus-A Open-Drain Bidirectional Data | 2, 14, 17, 25, 32, 34, 40, 44, 46, 48 | 6, 31, 40, 42, 49, 61, 64, 69, 77, 79 | 34, 40, 50, 53 | 32, 40, 44 | 20 |
| SCIA_RX | I | SCI-A Receive Data | 0, 3, 5, 9, 17, 25, 28, 35, 49 | 4, 32, 40, 42, 48, 60, 63, 74, 75 | 2, 34, 39, 49, 52, 61, 62 | 2, 31, 39, 42, 47 | 19, 26, 28, 30, 32 |
| SCIA_TX | O | SCI-A Transmit Data | 1, 2, 7, 8, 16, 24, 29, 37, 48 | 3, 31, 39, 41, 46, 58, 61, 62, 68 | 1, 33, 35, 37, 47, 50, 51, 57 | 1, 26, 27, 29, 40, 41, 43 | 15, 17, 27, 29, 31 |
| SCIB_RX | I | SCI-B Receive Data | 11, 13, 15, 19, 23, 41 | 35, 37, 51, 65, 66, 78 | 29, 31, 42, 54, 55 | 23, 34 | 14, 22 |
| SCIB_TX | O | SCI-B Transmit Data | 9, 10, 12, 14, 18, 22, 40 | 36, 50, 64, 67, 75, 76, 79 | 30, 41, 53, 56, 62, 63 | 24, 33 | 21 |
| SCIC_RX | I | SCI-C Receive Data | 21, 42, 226 | 11, 34, 57 | 7, 28 | 4 | 2 |
| SCIC_TX | O | SCI-C Transmit Data | 20, 43, 224 | 13, 33, 54 | 9, 27 | 6, 22 | 4 |
| SPIA_CLK | I/O | SPI-A Clock | 3, 9, 12, 18, 28, 32, 226 | 4, 11, 36, 49, 50, 60, 75 | 2, 7, 30, 40, 41, 49, 62 | 2, 4, 24, 32, 33, 39 | 2, 20, 21, 26, 32 |
| SPIA_SIMO | I/O | SPI-A Slave In, Master Out (SIMO) | 2, 7, 8, 11, 16, 20, 24, 224 | 13, 33, 37, 39, 41, 58, 61, 68 | 9, 27, 31, 33, 35, 47, 50, 57 | 6, 22, 26, 27, 40, 43 | 4, 14, 15, 29 |
| SPIA_SOMI | I/O | SPI-A Slave Out, Master In (SOMI) | 1, 4, 10, 13, 17, 21, 35, 228 | 10, 34, 35, 40, 48, 59, 62, 76 | 6, 28, 29, 34, 39, 48, 51, 63 | 4, 23, 31, 38, 41 | 2, 19, 27 |
| SPIA_STE | I/O | SPI-A Slave Transmit Enable (STE) | 0, 5, 11, 19, 24, 29, 37, 242 | 3, 12, 37, 41, 46, 51, 63, 74 | 1, 8, 31, 35, 37, 42, 52, 61 | 1, 5, 27, 29, 34, 42, 47 | 3, 14, 15, 17, 22, 28, 30, 31 |
| SYNCOUT | O | External ePWM Synchronization Pulse | 6, 39 | 80 | 64 | 48 | |
| TDI | I | JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input. | 35 | 48 | 39 | 31 | 19 |
| TDO | O | JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. | 37 | 46 | 37 | 29 | 17 |
| X1 | I/O | Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock. | 19 | 51 | 42 | 34 | 22 |
| X2 | I/O | Crystal oscillator output. | 18 | 50 | 41 | 33 | 21 |
| XCLKOUT | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. | 16, 18 | 39, 50 | 33, 41 | 26, 33 | 21 |

5.3.3 Power and Ground

Table 5-4. Power and Ground

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 80 PN | 64 PM | 48 PHP | 32 RHB |
|-------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------------|--------|--------|
| VDD | | 1.2-V Digital Logic Power Pins. See the Power Management Module (PMM) section for usage details. | 8, 53, 71 | 4, 44, 59 | 36, 45 | 24 |
| VDDA | | 3.3-V Analog Power Pins. Place a minimum 2.2- μ F decoupling capacitor on each pin. On the 32 QFN package, VREFHI is internally tied to VDDA. See the Power Management Module (PMM) section for usage details. | 26 | 22 | 18 | 11 |
| VDDIO | | 3.3-V Digital I/O Power Pins. See the Power Management Module (PMM) section for usage details. | 7, 52, 72 | 43, 60 | 35, 46 | 23 |
| VREGENZ | I | Internal voltage regulator enable with internal pulldown. Tie low to VSS to enable internal VREG. Tie high to VDDIO to use an external supply. | 56 | 46 | 37 | 25 |
| VSS | | Digital Ground. For QFN packages, the ground pad on the bottom of the package must be soldered to the ground plane of the PCB. | 9, 30, 55, 70 | 5, 26, 45, 58 | PAD | PAD |
| VSSA | | Analog Ground | 25 | 21 | 17 | 10 |

5.3.4 Test, JTAG, and Reset

Table 5-5. Test, JTAG, and Reset

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 80 PN | 64 PM | 48 PHP | 32 RHB |
|-------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|--------|--------|
| TCK | I | JTAG test clock with internal pullup. | 45 | 36 | 28 | 16 |
| TMS | I/O | JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation. | 47 | 38 | 30 | 18 |
| XRSn | I/OD | Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device. | 5 | 3 | 3 | 1 |

5.4 Pin Multiplexing

5.4.1 GPIO Muxed Pins

Section 5.4.1.1 lists the GPIO muxed pins.

5.4.1.1 GPIO Muxed Pins

Table 5-6. GPIO Muxed Pins

| 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 9 | 10 | 11 | 13 | 14 | 15 | ALT |
|-------------|--------------|--------------|-------------|--------------|--------------|--------------|--------------|--------------|------------|-------------|-----------|---------|-----|
| GPIO0 | EPWM1_A | CANA_RX | OUTPUTXBAR7 | SCIA_RX | I2CA_SDA | SPIA_STE | | MCAN_RX | | EQEP1_INDEX | | EPWM3_A | |
| GPIO1 | EPWM1_B | | | SCIA_TX | I2CA_SCL | SPIA_SOMI | EQEP1_STROBE | MCAN_TX | | | | EPWM3_B | |
| GPIO2 | EPWM2_A | | | OUTPUTXBAR1 | PMBUSA_SDA | SPIA_SIMO | SCIA_TX | | I2CB_SDA | | CANA_TX | EPWM4_A | |
| GPIO3 | EPWM2_B | OUTPUTXBAR2 | | OUTPUTXBAR2 | PMBUSA_SCL | SPIA_CLK | SCIA_RX | | I2CB_SCL | | CANA_RX | EPWM4_B | |
| GPIO4 | EPWM3_A | I2CA_SCL | MCAN_TX | OUTPUTXBAR3 | CANA_TX | | EQEP2_STROBE | | | | SPIA_SOMI | EPWM1_A | |
| GPIO5 | EPWM3_B | I2CA_SDA | OUTPUTXBAR3 | MCAN_RX | CANA_RX | SPIA_STE | | | SCIA_RX | | | EPWM1_B | |
| GPIO6 | EPWM4_A | OUTPUTXBAR4 | SYNCOUT | EQEP1_A | | | | | | | | EPWM2_A | |
| GPIO7 | EPWM4_B | EPWM2_A | OUTPUTXBAR5 | EQEP1_B | | SPIA_SIMO | | | SCIA_TX | | CANA_TX | EPWM2_B | |
| GPIO8 | EPWM5_A | | ADCSOAO | EQEP1_STROBE | SCIA_TX | SPIA_SIMO | I2CA_SCL | | | | | | |
| GPIO9 | EPWM5_B | SCIB_TX | OUTPUTXBAR6 | EQEP1_INDEX | SCIA_RX | SPIA_CLK | | | | | I2CB_SCL | | |
| GPIO10 | EPWM6_A | | ADCSOCBO | EQEP1_A | SCIB_TX | SPIA_SOMI | I2CA_SDA | | | | | | |
| GPIO11 | EPWM6_B | CANA_RX | OUTPUTXBAR7 | EQEP1_B | SCIB_RX | SPIA_STE | | | EQEP2_A | SPIA_SIMO | | | |
| GPIO12 | EPWM7_A | | MCAN_RX | EQEP1_STROBE | SCIB_TX | PMBUSA_CTL | | | SPIA_CLK | CANA_RX | | | |
| GPIO13 | EPWM7_B | | MCAN_TX | EQEP1_INDEX | SCIB_RX | PMBUSA_ALERT | | | SPIA_SOMI | CANA_TX | | | |
| GPIO14 | | SCIB_TX | | I2CB_SDA | OUTPUTXBAR3 | PMBUSA_SDA | | EQEP2_A | | EPWM3_A | | | |
| GPIO15 | | SCIB_RX | | I2CB_SCL | OUTPUTXBAR4 | PMBUSA_SCL | | EQEP2_B | | EPWM3_B | | | |
| GPIO16 | SPIA_SIMO | | OUTPUTXBAR7 | EPWM5_A | SCIA_TX | | EQEP1_STROBE | PMBUSA_SCL | XCLKOUT | EQEP2_B | | | |
| GPIO17 | SPIA_SOMI | | OUTPUTXBAR8 | EPWM5_B | SCIA_RX | | EQEP1_INDEX | PMBUSA_SDA | CANA_TX | | EPWM6_A | | |
| GPIO18 | SPIA_CLK | SCIB_TX | CANA_RX | EPWM6_A | I2CA_SCL | | EQEP2_A | PMBUSA_CTL | XCLKOUT | | | | X2 |
| GPIO19 | SPIA_STE | SCIB_RX | CANA_TX | EPWM6_B | I2CA_SDA | | EQEP2_B | PMBUSA_ALERT | | | | | X1 |
| GPIO20 | EQEP1_A | | CANA_TX | | SPIA_SIMO | | MCAN_TX | | I2CA_SCL | | | SCIC_TX | |
| GPIO21 | EQEP1_B | | CANA_RX | | SPIA_SOMI | | MCAN_RX | | I2CA_SDA | | | SCIC_RX | |
| GPIO22 | EQEP1_STROBE | | SCIB_TX | | | | LINA_TX | | | | EPWM4_A | | |
| GPIO23 | EQEP1_INDEX | | SCIB_RX | | | | LINA_RX | | | | EPWM4_B | | |
| GPIO24 | OUTPUTXBAR1 | EQEP2_A | SPIA_STE | EPWM4_A | SPIA_SIMO | | | PMBUSA_SCL | SCIA_TX | ERRORSTS | | | |
| GPIO25 | OUTPUTXBAR2 | EQEP2_B | | EQEP1_A | | | | PMBUSA_SDA | SCIA_RX | | | | |
| GPIO26 | OUTPUTXBAR3 | EQEP2_INDEX | | OUTPUTXBAR3 | | | | PMBUSA_CTL | I2CA_SDA | | | | |
| GPIO27 | OUTPUTXBAR4 | EQEP2_STROBE | | OUTPUTXBAR4 | | | | PMBUSA_ALERT | I2CA_SCL | | | | |
| GPIO28 | SCIA_RX | | EPWM7_A | OUTPUTXBAR5 | EQEP1_A | | EQEP2_STROBE | LINA_TX | SPIA_CLK | ERRORSTS | I2CB_SDA | | |
| GPIO29 | SCIA_TX | | EPWM7_B | OUTPUTXBAR6 | EQEP1_B | | EQEP2_INDEX | LINA_RX | SPIA_STE | ERRORSTS | I2CB_SCL | | |
| GPIO30 | CANA_RX | | | OUTPUTXBAR7 | EQEP1_STROBE | | | MCAN_RX | EPWM1_A | | | | |
| GPIO31 | CANA_TX | | | OUTPUTXBAR8 | EQEP1_INDEX | | | MCAN_TX | EPWM1_B | | | | |
| GPIO32 | I2CA_SDA | EQEP1_INDEX | SPIA_CLK | EPWM4_B | LINA_TX | | | CANA_TX | PMBUSA_SDA | ADCSOCBO | | | |
| GPIO33 | I2CA_SCL | | | OUTPUTXBAR4 | LINA_RX | | | CANA_RX | EQEP2_B | ADCSOAO | | | |
| GPIO34 | OUTPUTXBAR1 | | | | PMBUSA_SDA | | | | | | I2CB_SDA | | |
| GPIO35 | SCIA_RX | SPIA_SOMI | I2CA_SDA | CANA_RX | PMBUSA_SCL | LINA_RX | EQEP1_A | PMBUSA_CTL | EPWM5_B | | | TDI | |
| GPIO37 | OUTPUTXBAR2 | SPIA_STE | I2CA_SCL | SCIA_TX | CANA_TX | LINA_TX | EQEP1_B | PMBUSA_ALERT | EPWM5_A | | | TDO | |

Table 5-6. GPIO Muxed Pins (continued)

| 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 9 | 10 | 11 | 13 | 14 | 15 | ALT |
|-------------|-------------|---------|-------------|--------------|------------|----------|--------------|--------------|--------------|---------|-------------|----|-----|
| GPIO39 | | | | | MCAN_RX | | EQEP2_INDEX | | | SYNCOUT | EQEP1_INDEX | | |
| GPIO40 | | | | EPWM2_B | PMBUSA_SDA | | SCIB_TX | EQEP1_A | | | | | |
| GPIO41 | EPWM7_A | | | EPWM2_A | PMBUSA_SCL | | SCIB_RX | EQEP1_B | | | | | |
| GPIO42 | | LINA_RX | OUTPUTXBAR5 | PMBUSA_CTL | I2CA_SDA | SCIC_RX | | EQEP1_STROBE | | | | | |
| GPIO43 | | | OUTPUTXBAR6 | PMBUSA_ALERT | I2CA_SCL | SCIC_TX | PMBUSA_ALERT | EQEP1_INDEX | | | | | |
| GPIO44 | | | OUTPUTXBAR7 | EQEP1_A | PMBUSA_SDA | | PMBUSA_CTL | | | | | | |
| GPIO45 | | | OUTPUTXBAR8 | | | | PMBUSA_ALERT | | | | | | |
| GPIO46 | | | LINA_TX | MCAN_TX | | | PMBUSA_SDA | | | | | | |
| GPIO48 | OUTPUTXBAR3 | | CANA_TX | MCAN_TX | SCIA_TX | | PMBUSA_SDA | | | | | | |
| GPIO49 | OUTPUTXBAR4 | | CANA_RX | MCAN_RX | SCIA_RX | | LINA_RX | | | | | | |
| GPIO224 | | | | OUTPUTXBAR3 | SPIA_SIMO | | EPWM1_A | CANA_TX | EQEP1_A | | SCIC_TX | | |
| GPIO226 | | | LINA_RX | EPWM6_A | SPIA_CLK | | EPWM1_B | | EQEP1_STROBE | | SCIC_RX | | |
| GPIO227 | I2CB_SCL | | EPWM3_A | OUTPUTXBAR1 | EPWM2_B | | | | | | | | |
| GPIO228 | | | ADCSOAO | CANA_TX | SPIA_SOMI | | EPWM2_B | | EQEP1_B | | | | |
| GPIO230 | I2CB_SDA | | EPWM3_B | CANA_RX | EPWM2_A | I2CA_SDA | PMBUSA_SCL | | | | | | |
| GPIO242 | | | | OUTPUTXBAR2 | SPIA_STE | | EPWM4_A | CANA_RX | EQEP1_INDEX | | | | |
| AIO225 | | | | | | | | | | | | | |
| AIO231 | | | | | | | | | | | | | |
| AIO232 | | | | | | | | | | | | | |
| AIO233 | | | | | | | | | | | | | |
| AIO237 | | | | | | | | | | | | | |
| AIO238 | | | | | | | | | | | | | |
| AIO239 | | | | | | | | | | | | | |
| AIO241 | | | | | | | | | | | | | |
| AIO244 | | | | | | | | | | | | | |
| AIO245 | | | | | | | | | | | | | |

5.4.2 Digital Inputs on ADC Pins (AIOs)

GPIOs on port H are multiplexed with analog pins. These are also referred to as AIOs. These pins can only function in input mode. By default, these pins will function as analog pins and the GPIOs are in a high-Z state. The GPHAMSEL register is used to configure these pins for digital or analog operation.

Note

If digital signals with sharp edges (high dv/dt) are connected to the AIOs, cross-talk can occur with adjacent analog signals. The user should therefore limit the edge rate of signals connected to AIOs if adjacent channels are being used for analog functions.

5.4.3 Digital Inputs and Outputs on ADC Pins (AGPIOs)

Some GPIOs are multiplexed with analog pins and have digital input and output functionality. These are also referred to as AGPIOs. Unlike AIOs, AGPIOs have full input and output capability.

By default, the AGPIOs are not connected and must be configured. [Table 5-7](#) shows how to configure the AGPIOs. To enable the analog functionality, set the register AGPIOTRLx from analog subsystem. To enable the digital functionality, set the register GPxAMSEL from the *General-Purpose Input/Output (GPIO)* chapter.

Table 5-7. AGPIO Configuration

| AGPIOTRLx.GPIOy (Default = 0) | GPxAMSEL.GPIOy (Default = 1) | Pin Connected To: | |
|----------------------------------|---------------------------------|-------------------|------------------|
| | | ADC | GPIOy |
| 0 | 0 | - | Yes |
| 0 | 1 | - ⁽¹⁾ | - ⁽¹⁾ |
| 1 | 0 | - | Yes |
| 1 | 1 | Yes | - |

(1) By default there are no signals connected to AGPIO pins. One of the other rows in the table must be chosen for pin functionality.

Note

If digital signals with sharp edges (high dv/dt) are connected to the AGPIOs, cross-talk can occur with adjacent analog signals. The user must therefore limit the edge rate of signals connected to AGPIOs, if adjacent channels are being used for analog functions.

5.4.4 GPIO Input X-BAR

The Input X-BAR is used to route signals from a GPIO to many different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts (see [Figure 5-5](#)). [Table 5-8](#) lists the input X-BAR destinations. For details on configuring the Input X-BAR, see the Crossbar (X-BAR) chapter of the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#).

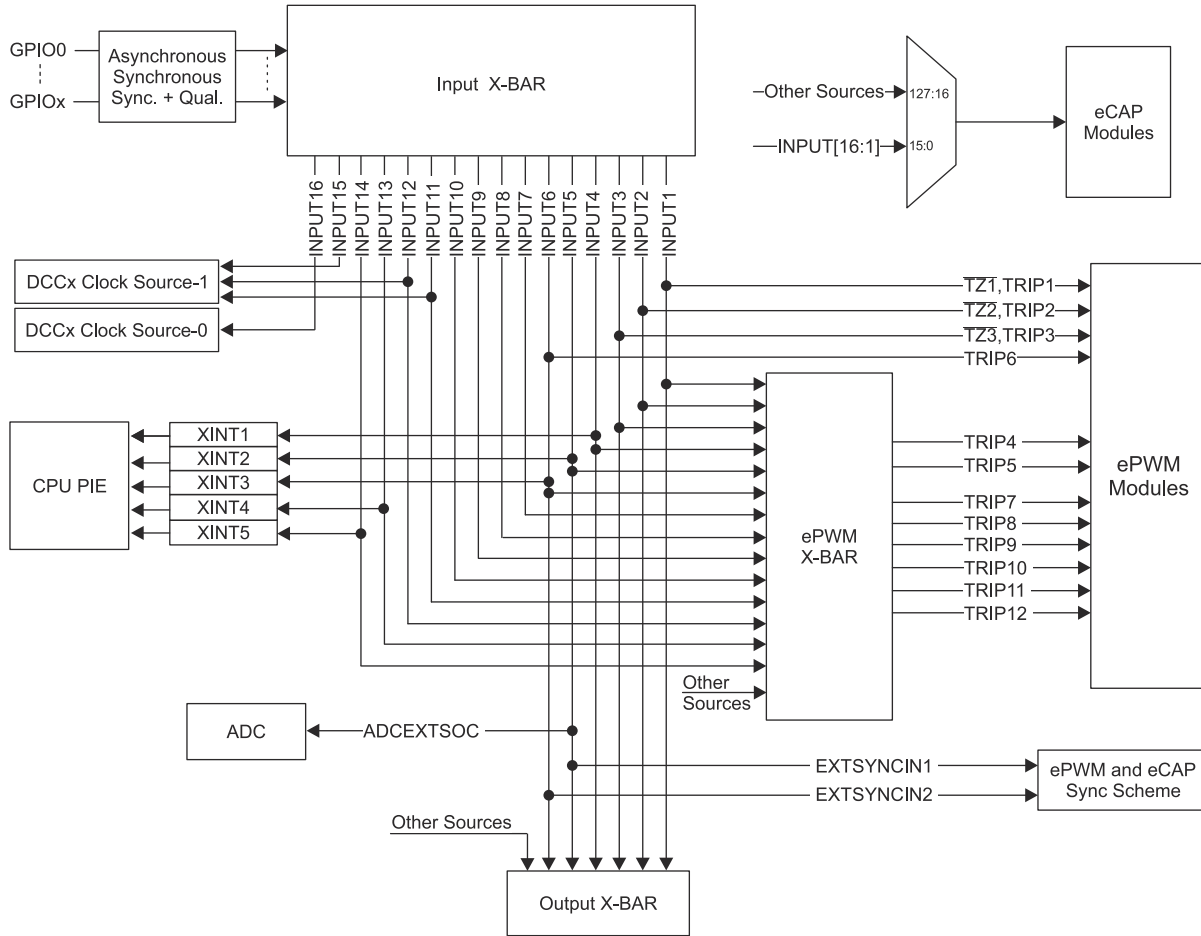


Figure 5-5. Input X-BAR

Table 5-8. Input X-BAR Destinations

| INPUT | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|----------------------------|---------------|---------------|---------------|-------|----------------|----------------|-----|-----|-----|-----|----------|----------|-------------|-------------|-------------|-------------|
| ECAP | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| EPWM X-BAR | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | | |
| OUTPUT X-BAR | Yes | Yes | Yes | Yes | Yes | Yes | | | | | | | | | | |
| CPU XINT | | | | XINT1 | XINT2 | XINT3 | | | | | | | XINT4 | XINT5 | | |
| EPWM TRIP | TZ1, TRIP1 | TZ2, TRIP2 | TZ3, TRIP3 | | | TRIP6 | | | | | | | | | | |
| ADC START OF CONVERSION | | | | | ADCEXT TSOC | | | | | | | | | | | |
| EPWM / ECAP SYNC | | | | | EXTSY NCIN1 | EXTSY NCIN2 | | | | | | | | | | |
| DCCx | | | | | | | | | | | CLK 1 | CLK 1 | | | CLK1 | CLK0 |
| EPG | | | | | | | | | | | | | EPG1 IN1 | EPG1 IN2 | EPG1 IN3 | EPG1 IN4 |

5.4.5 GPIO Output X-BAR and ePWM X-BAR

The Output X-BAR has eight outputs that can be selected on the GPIO mux as OUTPUTXBARx. The ePWM X-BAR has eight outputs that are connected to the TRIPx inputs of the ePWM. The sources for the Output X-BAR and ePWM X-BAR are shown in Figure 5-6.

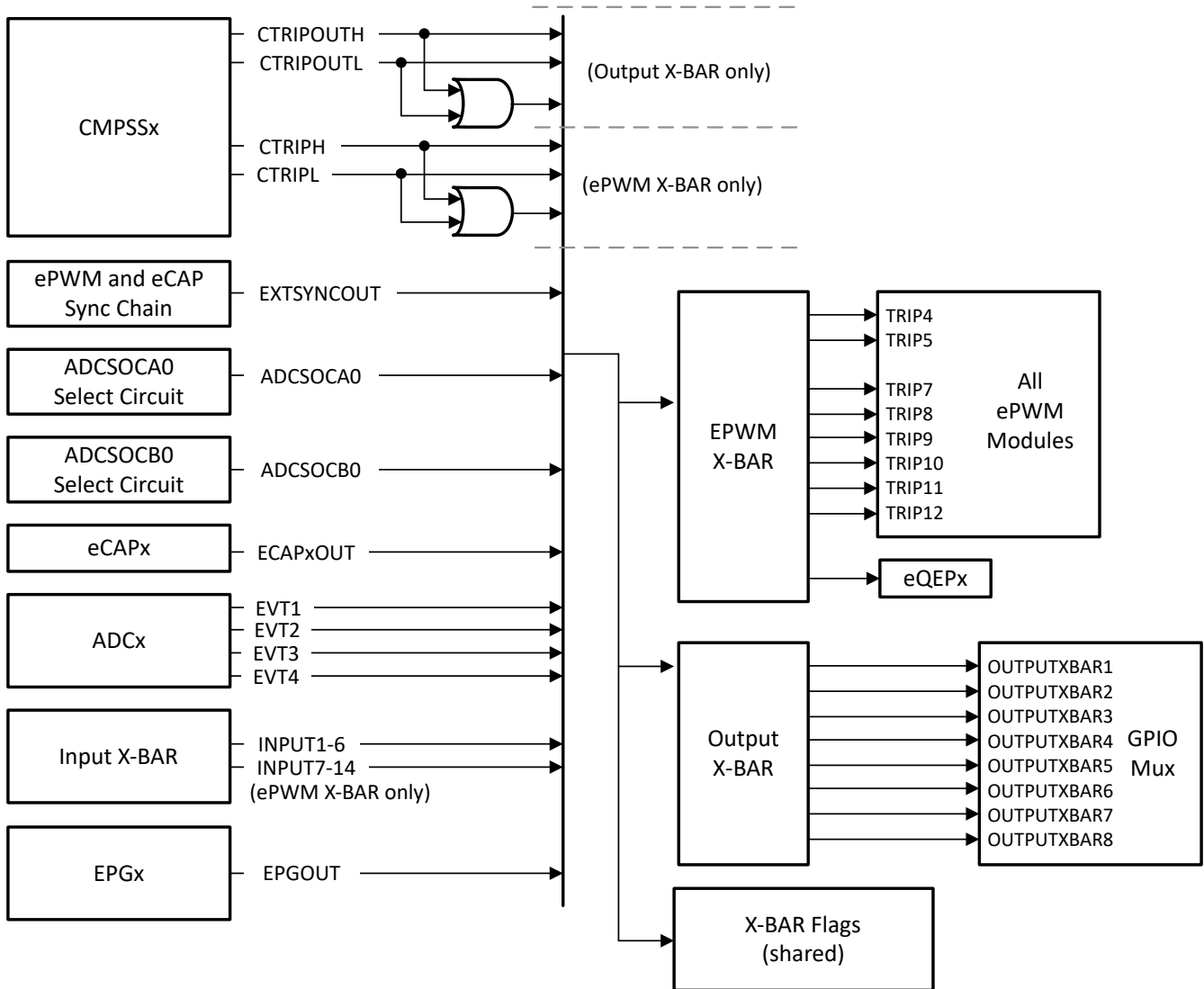


Figure 5-6. Output X-BAR and ePWM X-BAR Sources

5.5 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. [Table 5-9](#) lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. To avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in [Table 5-9](#) with pullups and pulldowns are always on and cannot be disabled.

Table 5-9. Pins With Internal Pullup and Pulldown

| PIN | RESET (XRSn = 0) | DEVICE BOOT | APPLICATION |
|-----------------------------|-------------------------------|--------------------------------|---------------------|
| GPIOx | Pullup disabled | Pullup disabled ⁽¹⁾ | Application defined |
| GPIO35/TDI | Pullup disabled | | Application defined |
| GPIO37/TDO | Pullup disabled | | Application defined |
| TCK | Pullup active | | |
| TMS | Pullup active | | |
| XRSn | Pullup active | | |
| Other pins (including AIOs) | No pullup or pulldown present | | |

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

5.6 Connections for Unused Pins

For applications that do not need to use all functions of the device, [Table 5-10](#) lists acceptable conditioning for any unused pins. When multiple options are listed in [Table 5-10](#), any option is acceptable. Pins not listed in [Table 5-10](#) must be connected according to [Section 5](#).

Table 5-10. Connections for Unused Pins

| SIGNAL NAME | ACCEPTABLE PRACTICE |
|--------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ANALOG | |
| VREFHI | Tie to VDDA (applies only if ADC is not used in the application) |
| VREFLO | Tie to VSSA |
| Analog input pins | <ul style="list-style-type: none"> No Connect Tie to VSSA Tie to VSSA through resistor |
| Analog input pins (shared with GPIO) | <ul style="list-style-type: none"> No Connect Tie to VSSA through resistor |
| DIGITAL | |
| GPIOx | <ul style="list-style-type: none"> No connection (input mode with internal pullup enabled) No connection (output mode with internal pullup disabled) Pullup or pulldown resistor (any value resistor, input mode, and with internal pullup disabled) |
| GPIO35/TDI | When TDI mux option is selected (default), the GPIO is in Input mode. <ul style="list-style-type: none"> Internal pullup enabled External pullup resistor |
| GPIO37/TDO | When TDO mux option is selected (default), the GPIO is in Output mode only during JTAG activity; otherwise, it is in a tri-state condition. The pin must be biased to avoid extra current on the input buffer. <ul style="list-style-type: none"> Internal pullup enabled External pullup resistor |
| TCK | <ul style="list-style-type: none"> No Connect Pullup resistor |
| TMS | Pullup resistor |

Table 5-10. Connections for Unused Pins (continued)

| SIGNAL NAME | ACCEPTABLE PRACTICE |
|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO19/X1 | Turn XTAL off and: <ul style="list-style-type: none"> • Input mode with internal pullup enabled • Input mode with external pullup or pulldown resistor • Output mode with internal pullup disabled |
| GPIO18/X2 | Turn XTAL off and: <ul style="list-style-type: none"> • Input mode with internal pullup enabled • Input mode with external pullup or pulldown resistor • Output mode with internal pullup disabled |
| POWER AND GROUND | |
| VDD | All VDD pins must be connected per Section 5.3 . Pins should not be used to bias any external circuits. |
| VDDA | If a dedicated analog supply is not used, tie to VDDIO. |
| VDDIO | All VDDIO pins must be connected per Section 5.3 . |
| VSS | All VSS pins must be connected to board ground. |
| VSSA | If an analog ground is not used, tie to VSS. |

6 Specifications

6.1 Absolute Maximum Ratings

over recommended operating conditions (unless otherwise noted)^{(1) (2)}

| | | MIN | MAX | UNIT |
|------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|------|-----|------|
| Supply voltage | VDD with respect to VSS | -0.3 | 1.5 | V |
| | VDDIO with respect to VSS | -0.3 | 4.6 | |
| | VDDA with respect to VSSA | -0.3 | 4.6 | |
| Input voltage | V _{IN} (3.3 V) | -0.3 | 4.6 | V |
| Output voltage | V _O | -0.3 | 4.6 | V |
| Input clamp current | Digital/analog input (per pin), I _{IK} (V _{IN} < VSS/VSSA or V _{IN} > VDDIO/VDDA) ⁽⁴⁾ | -20 | 20 | mA |
| | Total for all inputs, I _{IKTOTAL} (V _{IN} < VSS/VSSA or V _{IN} > VDDIO/VDDA) | -20 | 20 | |
| Output current | Digital output (per pin), I _{OUT} | -20 | 20 | mA |
| Operating junction temperature | T _J | -40 | 155 | °C |
| Storage temperature ⁽³⁾ | T _{stg} | -65 | 150 | °C |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to VSS, unless otherwise noted.
- (3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the [Semiconductor and IC Package Thermal Metrics Application Report](#).
- (4) Continuous clamp current per pin is ±2 mA. Do not operate in this condition continuously as V_{DDIO}/V_{DDA} voltage may internally rise and impact other electrical specifications.

6.2 ESD Ratings – Commercial

| | | | VALUE | UNIT | |
|------------------------------------------|-------------------------------|-----------------------------------------------------------------------|-------------------------------------------------------------|------|------|
| F2800157, F2800155 in 80-pin PN package | | | | | |
| V _(ESD) | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All pins | | ±500 |
| | | | Corner pins on 80-pin PN: 1, 20, 21, 40, 41, 60, 61, 80 | | ±750 |
| F2800157, F2800155 in 64-pin PM package | | | | | |
| V _(ESD) | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All pins | | ±500 |
| | | | Corner pins on 64-pin PM: 1, 16, 17, 32, 33, 48, 49, 64 | | ±750 |
| F2800157, F2800155 in 48-pin PHP package | | | | | |
| V _(ESD) | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All pins | | ±500 |
| | | | Corner pins on 48-pin PHP: 1, 12, 13, 24, 25, 36, 37, 48 | | ±750 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings – Automotive

| | | | VALUE | UNIT | |
|------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|---------------------------------------------------------|-------------------------------------------------------------|-------|---|
| F2800157-Q1, F2800156-Q1, F2800155-Q1, F2800154-Q1 in 80-pin PN package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 80-pin PN: 1, 20, 21, 40, 41, 60, 61, 80 | ±750 | |
| F2800157-Q1, F2800156-Q1, F2800155-Q1, F2800154-Q1 in 64-pin PM package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 64-pin PM: 1, 16, 17, 32, 33, 48, 49, 64 | ±750 | |
| F2800157-Q1 (Grade 1 and Grade 0), F2800156-Q1 (Grade 1 and Grade 0), F2800155-Q1, F2800154-Q1, F2800153-Q1, F2800152-Q1 in 48-pin PHP package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 48-pin PHP: 1, 12, 13, 24, 25, 36, 37, 48 | ±750 | |
| F2800157-Q1, F2800156-Q1, F2800155-Q1, F2800154-Q1, F2800153-Q1, F2800152-Q1 in 32-pin RHB package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 32-pin RHB: 1, 8, 9, 16, 17, 24, 25, 32 | ±750 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|-----------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------|-----|-------------|------|
| Device supply voltage, VDDIO and VDDA | Internal BOR enabled ⁽³⁾ | V _{BOR-VDDIO} (MAX) + V _{BOR-GB} ⁽²⁾ | 3.3 | 3.63 | V |
| | Internal BOR disabled | | 2.8 | 3.63 | |
| Device supply voltage, VDD | | 1.14 | 1.2 | 1.32 | V |
| Device ground, VSS | | | 0 | | V |
| Analog ground, VSSA | | | 0 | | V |
| SR _{SUPPLY} | Supply ramp rate of VDDIO, VDD, VDDA with respect to VSS. ⁽⁴⁾ | | | | |
| V _{IN} | Digital input voltage | VSS – 0.3 | | VDDIO + 0.3 | V |
| | Analog input voltage | VSSA – 0.3 | | VDDA + 0.3 | V |
| Junction temperature, T _J ⁽¹⁾ | F280015xS, F280015xQ parts | –40 | | 140 | °C |
| | F280015xE parts | –40 | | 155 | °C |
| Free-Air temperature, T _A | F280015xS, F280015xQ parts | –40 | | 125 | °C |
| | F280015xE parts | –40 | | 150 | °C |

- (1) Operation above T_J = 105°C for extended duration will reduce the lifetime of the device. See [Calculating Useful Lifetimes of Embedded Processors](#) for more information.
- (2) See the *Power Management Module (PMM) section*.
- (3) Internal BOR is enabled by default.
- (4) See the *Power Management Module Operating Conditions table*.

6.5 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations. [Section 6.5.1](#) and [Section 6.5.2](#) list the system current consumption values.

6.5.1 System Current Consumption - VREG Enable - Internal Supply

Over recommended operating conditions (unless otherwise noted)

TYP : V_{nom} , Temperatures shown are T_j

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|-----------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|------|-------|------|
| OPERATING MODE | | | | | | |
| I_{DDIO} | VDDIO current consumption during operational usage | This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency. This | 30 °C | 52 | | mA |
| | | | 85 °C | | 59.3 | mA |
| | | | 125 °C | | 71.22 | mA |
| | | | 143 °C ⁽³⁾ | | 77.1 | mA |
| | | | 155 °C ^{(4) (5)} | | 44.1 | mA |
| I_{DDA} | VDDA current consumption during operational usage | includes Core supply current with Internal Vreg Enabled. - CPU is running from RAM - Flash is powered up - X1/X2 crystal is powered up - PLL is enabled, SYSCLK=Max Device frequency - Analog modules are powered up - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 1.6 | | mA |
| | | | 85 °C | | 2 | mA |
| | | | 125 °C | | 2.5 | mA |
| | | | 143 °C ⁽³⁾ | | 2.5 | mA |
| | | | 155 °C ^{(4) (5)} | | 2.6 | mA |
| IDLE MODE | | | | | | |
| I_{DDIO} | VDDIO current consumption while device is in Idle mode | - CPU is in IDLE mode - Flash is powered down - PLL is Enabled, SYSCLK=Max Device Frequency, CPUCLK is gated - X1/X2 crystal is powered up | 30 °C | 19.3 | | mA |
| | | | 85 °C | | 24 | mA |
| | | | 125 °C | | 37.22 | mA |
| | | | 134 °C ⁽³⁾ | | 39.8 | mA |
| | | | 155 °C ⁽⁴⁾ | | 45.1 | mA |
| I_{DDA} | VDDA current consumption while device is in Idle mode | - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 0.01 | | mA |
| | | | 85 °C | | 0.1 | mA |
| | | | 125 °C | | 0.1 | mA |
| | | | 134 °C ⁽³⁾ | | 0.1 | mA |
| | | | 155 °C ⁽⁴⁾ | | 0.1 | mA |
| STANDBY MODE (PLL Enabled) | | | | | | |
| I_{DDIO} | VDDIO current consumption while device is in Standby mode | - CPU is in STANDBY mode - Flash is powered down - PLL is Enabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down | 30 °C | 7.6 | | mA |
| | | | 85 °C | | 11.8 | mA |
| | | | 125 °C | | 23.82 | mA |
| | | | 131 °C ⁽³⁾ | | 25.5 | mA |
| | | | 154 °C ⁽⁴⁾ | | 31.8 | mA |
| I_{DDA} | VDDA current consumption while device is in Standby mode | - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 0.01 | | mA |
| | | | 85 °C | | 0.1 | mA |
| | | | 125 °C | | 0.1 | mA |
| | | | 131 °C ⁽³⁾ | | 0.1 | mA |
| | | | 154 °C ⁽⁴⁾ | | 0.1 | mA |

6.5.1 System Current Consumption - VREG Enable - Internal Supply (continued)

Over recommended operating conditions (unless otherwise noted)

TYP : V_{nom} , Temperatures shown are T_J

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------------------------|---------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----|-------------------|-------------------|------|
| STANDBY MODE (PLL Disabled) | | | | | | | |
| I_{DDIO} | VDDIO current consumption while device is in Standby mode | <ul style="list-style-type: none"> - CPU is in STANDBY mode - Flash is powered down - PLL is Disabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down | 30 °C | | 5.8 | | mA |
| | | | 85 °C | | | 10 | mA |
| | | | 125 °C | | | 22.92 | mA |
| | | | 131 °C ⁽³⁾ | | | 24.5 | mA |
| | | | 154 °C ⁽⁴⁾ | | | 29.7 | mA |
| I_{DDA} | VDDA current consumption while device is in Standby mode | <ul style="list-style-type: none"> - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | | 0.01 | | mA |
| | | | 85 °C | | | 0.1 | mA |
| | | | 125 °C | | | 0.1 | mA |
| | | | 131 °C ⁽³⁾ | | | 0.1 | mA |
| | | | 154 °C ⁽⁴⁾ | | | 0.1 | mA |
| HALT MODE | | | | | | | |
| I_{DDIO} | VDDIO current consumption while device is in Halt mode | <ul style="list-style-type: none"> - CPU is in HALT mode - Flash is powered down - PLL is Disabled, SYSCLK and CPUCLK are gated - X1/X2 crystal is powered down | 30 °C | | 5.3 | | mA |
| | | | 85 °C | | | 9.5 | mA |
| | | | 125 °C | | | 22.52 | mA |
| | | | 131 °C ⁽³⁾ | | | 24.1 | mA |
| | | | 154 °C ⁽⁴⁾ | | | 29.2 | mA |
| I_{DDA} | VDDA current consumption while device is in Halt mode | <ul style="list-style-type: none"> - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | | 0.01 | | mA |
| | | | 85 °C | | | 0.1 | mA |
| | | | 125 °C | | | 0.1 | mA |
| | | | 131 °C ⁽³⁾ | | | 0.1 | mA |
| | | | 154 °C ⁽⁴⁾ | | | 0.1 | mA |
| FLASH ERASE/PROGRAM | | | | | | | |
| I_{DDIO} | VDDIO current consumption during Erase/Program cycle ⁽¹⁾ | <ul style="list-style-type: none"> - CPU is running from RAM - Flash going through continuous Program/Erase operation - PLL is enabled, SYSCLK=Max Device frequency. - Peripheral clocks are turned OFF. - X1/X2 crystal is powered up - Analog is powered down - Outputs are static without DC Load - Inputs are static high or low | | | 65 ⁽⁶⁾ | 90 ⁽⁶⁾ | mA |
| I_{DDA} | VDDA current consumption during Erase/Program cycle | | | | 0.1 | 2.6 | mA |

6.5.1 System Current Consumption - VREG Enable - Internal Supply (continued)

Over recommended operating conditions (unless otherwise noted)

TYP : V_{nom} , Temperatures shown are T_J

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|----------------------------------------------------------------|-----------------------|-----|------|-----|------|
| RESET MODE | | | | | | |
| I_{DDIO} | VDDIO current consumption while reset is active ⁽²⁾ | 30 °C | | 7 | | mA |
| | | 85 °C | | 10.7 | | mA |
| | | 125 °C | | 17 | | mA |
| | | 129 °C ⁽³⁾ | | 17.8 | | mA |
| | | 153 °C ⁽⁴⁾ | | 24.3 | | mA |
| I_{DDA} | VDDA current consumption while reset is active ⁽²⁾ | 30 °C | | 0.01 | | mA |
| | | 85 °C | | 0.01 | | mA |
| | | 125 °C | | 0.01 | | mA |
| | | 129 °C ⁽³⁾ | | 0.01 | | mA |
| | | 153 °C ⁽⁴⁾ | | 0.01 | | mA |

- (1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.
- (2) This is the current consumption while reset is active (that is, XRSn is low).
- (3) Temperature shown is T_J that occurs when T_A is 125 °C (AEC-Q100 Grade 1) at the given current. T_J rises above T_A to due to device self-heating from current consumption. This T_J is applicable for all packages. See *Thermal Resistance Characteristics* sections for each package for values used in calculating self-heating due to current consumption.
- (4) Temperature shown is T_J that occurs when T_A is 150 °C (AEC-Q100 Grade 0) at the given current. T_J rises above T_A to due to device self-heating from current consumption. This T_J is applicable for 48PHP package. See *Thermal Resistance Characteristics* sections for each package for values used in calculating self-heating due to current consumption.
- (5) Device SYSCLK frequency reduced to 60 MHz to avoid exceeding T_J MAX specification of device. See *Thermal Design Considerations for AEC-Q100 Grade 0* section for more details.
- (6) Continuous ERASE/PROGRAM pulses will exceed T_J MAX and must be avoided. Programming and erasing a single sector will not cause a thermal rise above T_J MAX and can be done at all temperatures. The current provided is the peak ERASE/PROGRAM pulse current. Device power consumption must not exceed approximately 169 mW (continuous) when using AEC-Q100 Grade 0 temperature ranges. Otherwise, T_J MAX specification will be exceeded. To avoid exceeding T_J MAX, the average flash current consumed can be reduced by increasing the time between ERASE/PROGRAM flash pulses. This reduces the overall self-heating of the device by giving the device time to cool down to ambient temperatures after any temperature rise that occurs during the ERASE/PROGRAM pulse.

6.5.2 System Current Consumption - VREG Disable - External Supply

Over recommended operating conditions (unless otherwise noted)

TYP : V_{nom} , Temperatures shown are T_J

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|------|-------|------|
| OPERATING MODE | | | | | | |
| I_{DD} | VDD current consumption during operational usage | This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency. This includes Core supply current with Internal Vreg Enabled. - CPU is running from RAM - Flash is powered up - X1/X2 crystal is powered up - PLL is enabled, SYSCLK=Max Device frequency | 30 °C | 50 | | mA |
| | | | 85 °C | | 58.8 | mA |
| | | | 125 °C | | 72.82 | mA |
| | | | 134 °C ⁽³⁾ | | 74.9 | mA |
| | | | 155 °C ⁽⁴⁾ | | 77.48 | mA |
| I_{DDIO} | VDDIO current consumption during operational usage | includes Core supply current with Internal Vreg Enabled. - CPU is running from RAM - Flash is powered up - X1/X2 crystal is powered up - PLL is enabled, SYSCLK=Max Device frequency | 30 °C | 9.75 | | mA |
| | | | 85 °C | | 8.14 | mA |
| | | | 125 °C | | 8.12 | mA |
| | | | 134 °C ⁽³⁾ | | 8.2 | mA |
| | | | 155 °C ⁽⁴⁾ | | 8.34 | mA |
| I_{DDA} | VDDA current consumption during operational usage | - Analog modules are powered up - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 1.6 | | mA |
| | | | 85 °C | | 2 | mA |
| | | | 125 °C | | 2.3 | mA |
| | | | 134 °C ⁽³⁾ | | 2.4 | mA |
| | | | 155 °C ⁽⁴⁾ | | 2.5 | mA |
| IDLE MODE | | | | | | |
| I_{DD} | VDD current consumption while device is in Idle mode | - CPU is in IDLE mode - Flash is powered down - PLL is Enabled, SYSCLK=Max Device Frequency, CPUCLK is gated | 30 °C | 16.6 | | mA |
| | | | 85 °C | | 28.1 | mA |
| | | | 125 °C | | 41.02 | mA |
| | | | 130 °C ⁽³⁾ | | 42.0 | mA |
| | | | 153 °C ⁽⁴⁾ | | 43.8 | mA |
| I_{DDIO} | VDDIO current consumption while device is in Idle mode | - X1/X2 crystal is powered up - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 4 | | mA |
| | | | 85 °C | | 4 | mA |
| | | | 125 °C | | 4.5 | mA |
| | | | 130 °C ⁽³⁾ | | 4.6 | mA |
| | | | 153 °C ⁽⁴⁾ | | 5 | mA |
| I_{DDA} | VDDA current consumption while device is in Idle mode | | 30 °C | 0.01 | | mA |
| | | | 85 °C | | 0.1 | mA |
| | | | 125 °C | | 0.1 | mA |
| | | | 130 °C ⁽³⁾ | | 0.1 | mA |
| | | | 153 °C ⁽⁴⁾ | | 0.1 | mA |

6.5.2 System Current Consumption - VREG Disable - External Supply (continued)

Over recommended operating conditions (unless otherwise noted)

TYP : V_{nom} , Temperatures shown are T_J

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|-----------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|------|-------|------|
| STANDBY MODE (PLL Enabled) | | | | | | |
| I_{DD} | VDD current consumption while device is in Standby mode | - CPU is in STANDBY mode - Flash is powered down | 30 °C | 3.9 | | mA |
| | | | 85 °C | | 11.2 | mA |
| | | | 125 °C | | 28.02 | mA |
| | | | 129 °C ⁽³⁾ | | 29.0 | mA |
| | | | 152 °C ⁽⁴⁾ | | 30.9 | mA |
| I_{DDIO} | VDDIO current consumption while device is in Standby mode | - PLL is Enabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load | 30 °C | 6.8 | | mA |
| | | | 85 °C | | 5.11 | mA |
| | | | 125 °C | | 5 | mA |
| | | | 129 °C ⁽³⁾ | | 5 | mA |
| | | | 152 °C ⁽⁴⁾ | | 5.06 | mA |
| I_{DDA} | VDDA current consumption while device is in Standby mode | - Inputs are static high or low | 30 °C | 0.01 | | mA |
| | | | 85 °C | | 0.1 | mA |
| | | | 125 °C | | 0.1 | mA |
| | | | 129 °C ⁽³⁾ | | 0.1 | mA |
| | | | 152 °C ⁽⁴⁾ | | 0.1 | mA |
| STANDBY MODE (PLL Disabled) | | | | | | |
| I_{DD} | VDD current consumption while device is in Standby mode | - CPU is in STANDBY mode - Flash is powered down | 30 °C | 2.8 | | mA |
| | | | 85 °C | | 10 | mA |
| | | | 125 °C | | 26.82 | mA |
| | | | 129 °C ⁽³⁾ | | 27.7 | mA |
| | | | 152 °C ⁽⁴⁾ | | 29.64 | mA |
| I_{DDIO} | VDDIO current consumption while device is in Standby mode | - PLL is Disabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load | 30 °C | 6.25 | | mA |
| | | | 85 °C | | 4.36 | mA |
| | | | 125 °C | | 4.22 | mA |
| | | | 129 °C ⁽³⁾ | | 4.23 | mA |
| | | | 152 °C ⁽⁴⁾ | | 4.27 | mA |
| I_{DDA} | VDDA current consumption while device is in Standby mode | - Inputs are static high or low | 30 °C | 0.01 | | mA |
| | | | 85 °C | | 0.1 | mA |
| | | | 125 °C | | 0.1 | mA |
| | | | 129 °C ⁽³⁾ | | 0.1 | mA |
| | | | 152 °C ⁽⁴⁾ | | 0.1 | mA |

6.5.2 System Current Consumption - VREG Disable - External Supply (continued)

Over recommended operating conditions (unless otherwise noted)

TYP : V_{nom} , Temperatures shown are T_J

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|---------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|------|-------|------|
| HALT MODE | | | | | | |
| I_{DD} | VDD current consumption while device is in Halt mode | <ul style="list-style-type: none"> - CPU is in HALT mode - Flash is powered down - PLL is Disabled, SYSCLK and CPUCLK are gated - X1/X2 crystal is powered down | 30 °C | 2.3 | | mA |
| | | | 85 °C | | 9.6 | mA |
| | | | 125 °C | | 26.32 | mA |
| | | | 129 °C ⁽³⁾ | | 27.2 | mA |
| | | | 152 °C ⁽⁴⁾ | | 29.14 | mA |
| I_{DDIO} | VDDIO current consumption while device is in Halt mode | <ul style="list-style-type: none"> - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 6.20 | | mA |
| | | | 85 °C | | 4.36 | mA |
| | | | 125 °C | | 4.23 | mA |
| | | | 129 °C ⁽³⁾ | | 4.24 | mA |
| | | | 152 °C ⁽⁴⁾ | | 4.27 | mA |
| I_{DDA} | VDDA current consumption while device is in Halt mode | <ul style="list-style-type: none"> - Inputs are static high or low | 30 °C | 0.01 | | mA |
| | | | 85 °C | | 0.1 | mA |
| | | | 125 °C | | 0.1 | mA |
| | | | 129 °C ⁽³⁾ | | 0.1 | mA |
| | | | 152 °C ⁽⁴⁾ | | 0.1 | mA |
| FLASH ERASE/PROGRAM | | | | | | |
| I_{DD} | VDD current consumption during Erase/Program cycle ⁽¹⁾ | <ul style="list-style-type: none"> - CPU is running from RAM - Flash going through continuous Program/Erase operation - PLL is enabled, SYSCLK=Max Device frequency. - Peripheral clocks are turned OFF. - X1/X2 crystal is powered up - Analog is powered down - Outputs are static without DC Load - Inputs are static high or low | | 58 | 70 | mA |
| I_{DDIO} | VDDIO current consumption during Erase/Program cycle ⁽¹⁾ | | | 11 | 20 | mA |
| I_{DDA} | VDDA current consumption during Erase/Program cycle | | | 0.1 | 2.5 | mA |

6.5.2 System Current Consumption - VREG Disable - External Supply (continued)

Over recommended operating conditions (unless otherwise noted)

TYP : V_{nom} , Temperatures shown are T_J

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|----------------------------------------------------------------|-----------------------|-----|------|-----|------|
| RESET MODE | | | | | | |
| I_{DD} | VDD current consumption while reset is active ⁽²⁾ | 30 °C | | 2.2 | | mA |
| | | 85 °C | | 4.2 | | mA |
| | | 125 °C | | 8.7 | | mA |
| | | 127 °C ⁽³⁾ | | 9 | | mA |
| | | 152 °C ⁽⁴⁾ | | 14 | | mA |
| I_{DDIO} | VDDIO current consumption while reset is active ⁽²⁾ | 30 °C | | 5 | | mA |
| | | 85 °C | | 5 | | mA |
| | | 125 °C | | 5 | | mA |
| | | 127 °C ⁽³⁾ | | 5 | | mA |
| | | 152 °C ⁽⁴⁾ | | 5 | | mA |
| I_{DDA} | VDDA current consumption while reset is active ⁽²⁾ | 30 °C | | 0.01 | | mA |
| | | 85 °C | | 0.01 | | mA |
| | | 125 °C | | 0.01 | | mA |
| | | 127 °C ⁽³⁾ | | 0.01 | | mA |
| | | 152 °C ⁽⁴⁾ | | 0.01 | | mA |

- (1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.
- (2) This is the current consumption while reset is active (that is, XRSn is low).
- (3) Temperature shown is T_J that occurs when T_A is 125 °C (AEC-Q100 Grade 1) at the given current. T_J rises above T_A to due to device self-heating from current consumption. This T_J is applicable for all packages. See *Thermal Resistance Characteristics* sections for each package for values used in calculating self-heating due to current consumption.
- (4) Temperature shown is T_J that occurs when T_A is 150 °C (AEC-Q100 Grade 0) at the given current. T_J rises above T_A to due to device self-heating from current consumption. This T_J is applicable for 48PHP package. See *Thermal Resistance Characteristics* sections for each package for values used in calculating self-heating due to current consumption.

6.5.3 Operating Mode Test Description

Section 6.5.1, Section 6.5.2, and the Section 6.5.5.1 list the current consumption values for the operational mode of the device. The operational mode provides an estimation of what an application might encounter. The test condition for these measurements has the following properties:

- Code is executing from RAM.
- FLASH is read and kept in active state.
- No external components are driven by I/O pins.
- All peripherals have clocks enabled.
- All CPUs are actively executing code.
- All analog peripherals are powered up. ADCs and DACs are periodically converting.

6.5.4 Current Consumption Graphs

The below graphs show a typical representation of the relationship between frequency, temperature, supply, and current consumption on the device. Actual results vary based on the system implementation and conditions.

Figure 6-1 shows the typical operating current profile across frequency. Figure 6-2 shows the typical operating current profile across temperature and operating mode for internal supply, with data based on the *System Current Consumption - VREG Enable - Internal Supply* table (30 °C data is taken at VNOM with higher temperature data points taken at VMAX). Figure 6-3 shows the typical operating current profile across temperature and operating mode for external supply, with data based on the *System Current Consumption - VREG Enable - External Supply* table (30 °C data is taken at VNOM with higher temperature data points taken at VMAX).

CAUTION

Figure 6-2 includes operating mode current data above 125 °C. Not all current and temperature combinations illustrated in the graph are possible. To minimize the risk of damage to equipment, operating current must be limited below certain levels to avoid exceeding T_J MAX device specifications as outlined in Section 6.12.

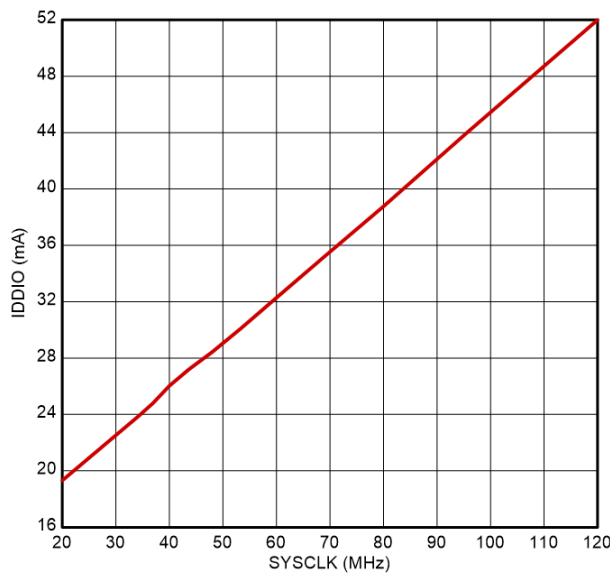


Figure 6-1. Operating Current Versus Frequency

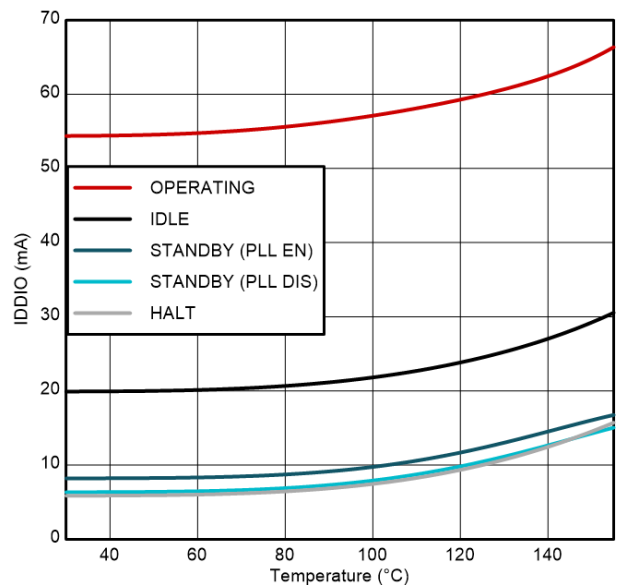


Figure 6-2. Current Versus Temperature - Internal Supply

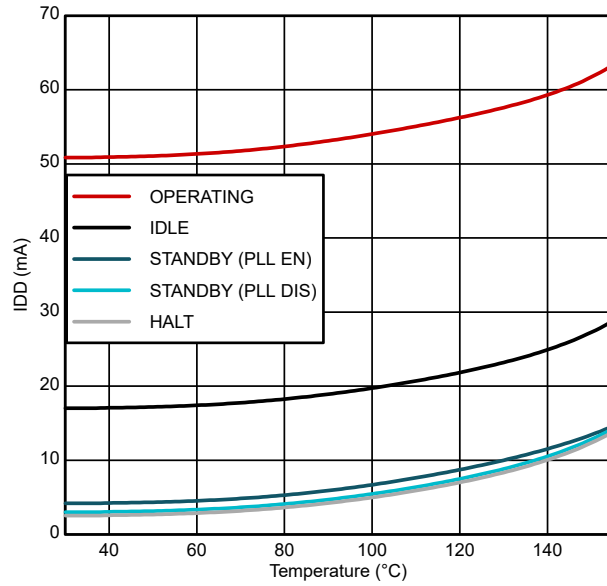


Figure 6-3. Current Versus Temperature - External Supply

6.5.5 Reducing Current Consumption

The F280015x devices provide some methods to reduce the device current consumption:

- One of the two low-power modes—IDLE or STANDBY—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- Each peripheral has an individual clock-enable bit (PCLKCRx). Reduced current consumption may be achieved by turning off the clock to any peripheral that is not used in a given application. [Section 6.5.5.1](#) lists the typical current reduction that may be achieved by disabling the clocks using the PCLKCRx register.
- To realize the lowest VDDA current consumption in an LPM, see the Analog-to-Digital Converter (ADC) chapter of the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#) to ensure each module is powered down as well.

6.5.5.1 Typical Current Reduction per Disabled Peripheral

For peripherals with multiple instances, the current quoted is for all modules combined.

| PERIPHERAL | I _{DDIO} CURRENT REDUCTION (mA) |
|---------------------------|------------------------------------------|
| ADC ⁽¹⁾ | 0.62 |
| CMPSS_LITE ⁽¹⁾ | 0.26 |
| CMPSS ⁽¹⁾ | 0.42 |
| CPU TIMER | 0.08 |
| MCAN (CAN FD) | 1.24 |
| DCAN | 1.32 |
| DCC | 0.06 |
| eCAP | 0.06 |
| EPG | 0.28 |
| ePWM | 0.88 |
| HRPWM | 0.94 |
| eQEP | 0.1 |
| LIN | 0.34 |
| SCI | 0.18 |
| I2C | 0.3 |
| PMBUS | 0.24 |
| SPI | 0.12 |

(1) This current represents the current drawn by the digital portion of the each module.

6.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|-------------------------------|------------------------------------------------------|---------------------------------------------------|---------------------------------------------------------------|-------|-------|-------|----|----|
| Digital and Analog IO | | | | | | | | |
| V _{OH} | High-level output voltage | I _{OH} = I _{OH} MIN | VDDIO * 0.8 | | | V | | |
| | | I _{OH} = -100 μA | VDDIO - 0.2 | | | | | |
| V _{OL} | Low-level output voltage | I _{OL} = I _{OL} MAX | | | 0.4 | V | | |
| | | I _{OL} = 100 μA | | | 0.2 | | | |
| I _{OH} | High-level output source current for all output pins | | -4 | | | mA | | |
| I _{OL} | Low-level output sink current for all output pins | | | | 4 | mA | | |
| R _{OH} | High-level output impedance for all output pins | | VOH=VDDSD-0.4V | | 50 | 65 | 96 | Ω |
| R _{OL} | Low-level output impedance for all output pins | | VOL=0.4V | | 48 | 60 | 84 | Ω |
| V _{IH} | High-level input voltage | | | | 2.0 | | | V |
| V _{IL} | Low-level input voltage | | | | | 0.8 | | V |
| V _{HYSTERESIS} | Input hysteresis (AIO) | | | | 125 | | | mV |
| | Input hysteresis (GPIO) | | | | 125 | | | |
| I _{PULLDOWN} | Input current | Pins with pulldown | VDDIO = 3.3 V V _{IN} = VDDIO | | | 120 | | μA |
| I _{PULLUP} | Input current | Digital inputs with pullup enabled ⁽¹⁾ | VDDIO = 3.3 V V _{IN} = 0 V | | | 160 | | μA |
| R _{PULLDOWN} | Weak pulldown resistance | | | 22.66 | 31.49 | 61.55 | | kΩ |
| R _{PULLUP} | Weak pullup resistance | | | 19.89 | 29.45 | 53.63 | | kΩ |
| I _{LEAK} | Pin leakage | Digital inputs | Pullups and outputs disabled 0 V ≤ V _{IN} ≤ VDDIO | | | 0.1 | | μA |
| | | Analog pins | Analog drivers disabled 0 V ≤ V _{IN} ≤ VDDA | | | 0.1 | | |
| C _I | Input capacitance | Digital inputs | | | | 2 | | pF |
| | | Analog pins ⁽²⁾ | | | | | | |
| VREG and BOR | | | | | | | | |
| VREG, POR, BOR ⁽³⁾ | | | | | | | | |

(1) See the *Pins With Internal Pullup and Pulldown* table for a list of pins with a pullup or pulldown.

(2) The analog pins are specified separately; see the Per-Channel Parasitic Capacitance tables that are in the ADC Input Model section

(3) See the *Power Management Module (PMM)* section.

6.7 Thermal Resistance Characteristics for PN Package

| | | °C/W ⁽¹⁾ |
|------------------------------|---------------------------------------------|---------------------|
| R θ_{JC} | Junction-to-case thermal resistance, top | 17.7 |
| | Junction-to-case thermal resistance, bottom | N/A |
| R θ_{JB} | Junction-to-board thermal resistance | 36.5 |
| R θ_{JA} (High k PCB) | Junction-to-free air thermal resistance | 56.7 |
| Psi $_{JT}$ | Junction-to-package top | 0.8 |
| Psi $_{JB}$ | Junction-to-board | 36 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.8 Thermal Resistance Characteristics for PM Package

| | | °C/W ⁽¹⁾ |
|------------------------------|---------------------------------------------|---------------------|
| R θ_{JC} | Junction-to-case thermal resistance, top | 20.3 |
| | Junction-to-case thermal resistance, bottom | N/A |
| R θ_{JB} | Junction-to-board thermal resistance | 36.4 |
| R θ_{JA} (High k PCB) | Junction-to-free air thermal resistance | 59.8 |
| Psi $_{JT}$ | Junction-to-package top | 0.9 |
| Psi $_{JB}$ | Junction-to-board | 36 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.9 Thermal Resistance Characteristics for PHP Package

| | | °C/W ⁽¹⁾ |
|------------------------------|---------------------------------------------|---------------------|
| R θ_{JC} | Junction-to-case thermal resistance, top | 17.1 |
| | Junction-to-case thermal resistance, bottom | 2.2 |
| R θ_{JB} | Junction-to-board thermal resistance | 12.3 |
| R θ_{JA} (High k PCB) | Junction-to-free air thermal resistance | 29.5 |
| Psi $_{JT}$ | Junction-to-package top | 0.2 |
| Psi $_{JB}$ | Junction-to-board | 12.3 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.10 Thermal Resistance Characteristics for RHB Package

| | | °C/W ⁽¹⁾ |
|------------------------------|---------------------------------------------|---------------------|
| R θ_{JC} | Junction-to-case thermal resistance, top | 20.7 |
| | Junction-to-case thermal resistance, bottom | 2.3 |
| R θ_{JB} | Junction-to-board thermal resistance | 11.3 |
| R θ_{JA} (High k PCB) | Junction-to-free air thermal resistance | 31.2 |
| Psi $_{JT}$ | Junction-to-package top | 0.2 |
| Psi $_{JB}$ | Junction-to-board | 11.2 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.11 Thermal Design Considerations

Based on the end application design and operational profile, the I $_{DD}$ and I $_{DDIO}$ currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T $_A$) varies with the end application and product design. The critical factor that affects reliability and functionality is T $_J$, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T $_J$ within the specified limits. T $_{case}$ should be measured to estimate the operating junction temperature T $_J$. T $_{case}$ is normally measured at the center of the package top-side surface. The thermal application report [Semiconductor and IC Package Thermal Metrics](#) helps to understand the thermal metrics and definitions.

6.12 Thermal Design Considerations for AEC-Q100 Grade 0

Note

This section only applies to internal supply (VREG enabled) mode. External supply (VREG disabled) mode requires none of the considerations in this section.

F280015xE parts are AEC-Q100 Grade 0 qualified. To maintain both ambient T $_A$ (150°C) and junction T $_J$ (155°C) temperature requirements, the device frequency, excessive IO current, and flash erase/program pulse frequency must be limited. This is only required for internal supply mode (VREG enabled). The tables below summarize an example of how the T $_A$ and T $_J$ requirements can be met for different ambient temperature ranges of the Grade 0 device.

Table 6-1. Operating Mode Power Example

| SUPPLY | VOLTAGE (V) | T $_A$ 125°C | | T $_A$ 150°C ⁽³⁾ | |
|----------------------|-------------|-----------------------------|------------|-----------------------------|------------|
| | | CURRENT ⁽¹⁾ (mA) | POWER (mW) | CURRENT ⁽¹⁾ (mA) | POWER (mW) |
| IDDIO ⁽²⁾ | 3.63 | 77.1 | 280 | 45.3 | 164 |
| IDDA | 3.63 | 2.6 | 9 | 1.4 | 5 |
| TOTAL | | – | 289 | – | 169 |

- (1) Refer to the *System Current Consumption - VREG Enable - Internal Supply* table for details.
- (2) VDDIO power is dependent on system activity and loads, the values listed in that table assume no DC loads on IO buffers and typical IO switching activity.
- (3) Frequency limited to 60 MHz to reduce current consumption. Current and power values represent the estimated maximum allowable values based on the thermal characteristics outlined in *Thermal Resistance Characteristics for PHP Package*.

Table 6-2. AEC-Q100 Grade 0 Thermal Management - VREG Enable

| T _A | USE CASE | | | T _J | T _J REQUIREMENT |
|----------------|---------------------------------------------|--------|-------------------------------------------------------|----------------|----------------------------|
| | SYSCCLK FREQUENCY f _(SYSCCLK) | POWER | T _A -to-T _J RISE ⁽¹⁾ | | |
| 125°C | 120 MHz | 289 mW | 18°C | 143°C | <155°C |
| 150°C | 60 MHz | 160 mW | 5°C | 155°C | |

(1) T_A-to-T_J rise in this example is calculated using RΘ_{JA} from the *Thermal Resistance Characteristics for PHP Package* table.

6.12.1 Simple Frequency Reduction

The simplest system approach to meet the T_A and T_J requirements is to always run SYSCCLK at f_(SYSCCLK_TA_GRADE0) MAX (60 MHz) in a Grade 0 application.

6.12.2 Dynamic Frequency Reduction

An alternate implementation is to dynamically change the f_(SYSCCLK) frequency depending on the system temperature. An external temperature sensor can be used to measure T_A, or the internal temperature sensor can be used to measure T_J. Before the temperature passes the maximum allowed T_A (145°C) or T_J (155°C), the application code can reduce the f_(SYSCCLK) frequency as noted above. Some system considerations for this approach:

1. Temperature sensors (internal or external) have an accuracy specification which must be considered when selecting a temperature threshold for transitioning.
2. Temperature threshold hysteresis must be used to avoid rapid cycling between frequency ranges.
3. Control loops and peripherals like ePWM must be adjusted for the new f_(SYSCCLK) frequency if the control loop operates in the higher temperature range.
4. Communications peripherals dependent on specific baud rates must be adjusted to the new f_(SYSCCLK) frequency.
5. Time based counters like the Watchdog timer or delay software delay functions must be adjusted.

There are other clock-related dependencies that affect the required updates when changing frequencies. The *Clocking System* diagram and ClockTree Tool in [C2000™ SysConfig](#) can assist with determining which dependencies must be updated.

6.12.3 Flash Considerations

The FLASH ERASE/PROGRAM current when using internal supply (VREG enabled) can cause self-heating above the T_J MAX specification of the device. To avoid this, the average flash program/erase current can be reduced by increasing the time between flash ERASE/PROGRAM pulses. This reduces the overall self-heating of the device by giving time to cool down to ambient temperatures after any temperature rise that occurs during the ERASE/PROGRAM pulse.

6.13 System

6.13.1 Power Management Module (PMM)

6.13.1.1 Introduction

The Power Management Module (PMM) handles all the power management functions required for device operation.

6.13.1.2 Overview

The block diagram of the PMM is shown in Figure 6-4. As can be seen, the PMM comprises of various subcomponents, which are described in the subsequent sections.

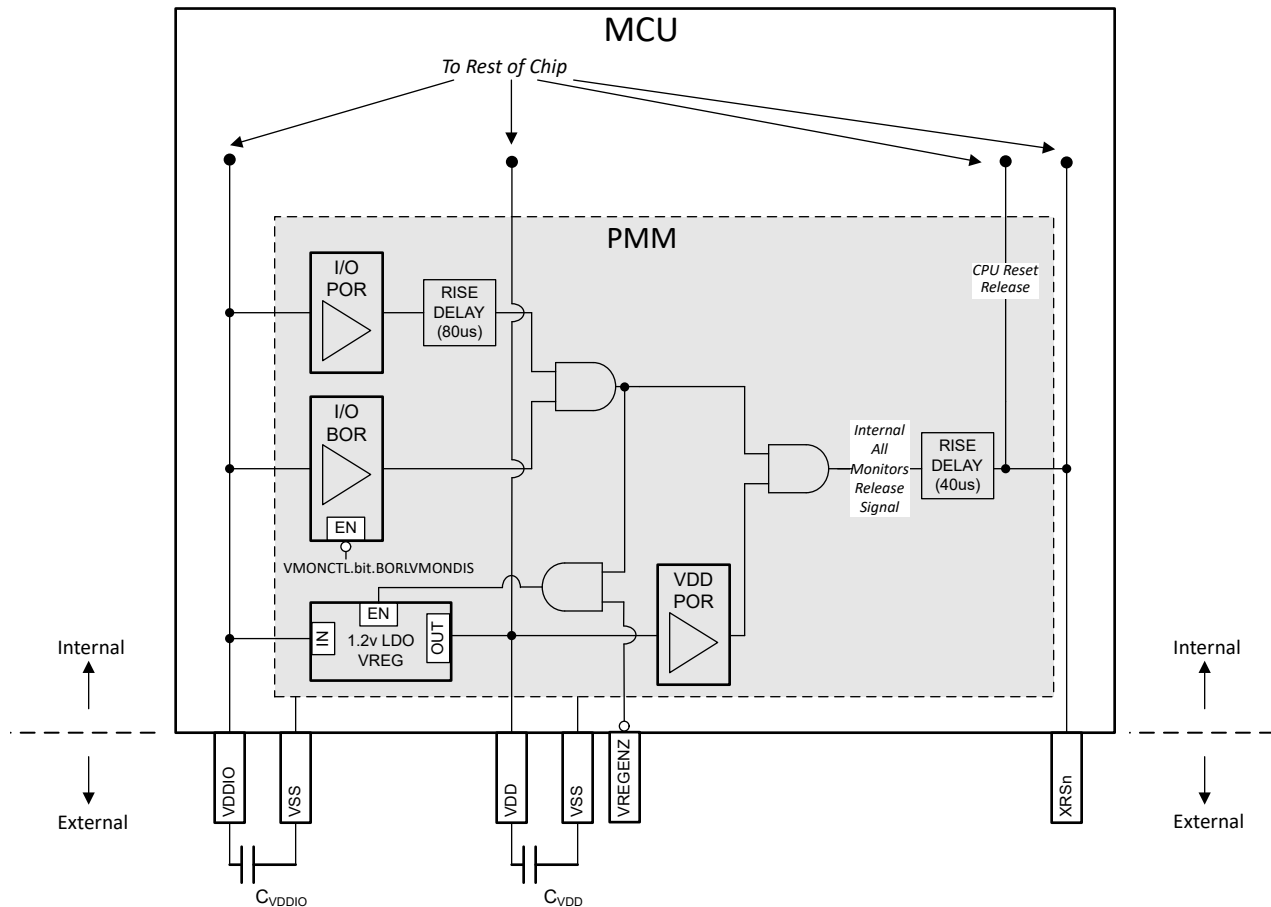


Figure 6-4. PMM Block Diagram

6.13.1.2.1 Power Rail Monitors

The PMM has voltage monitors on the supply rails that release the XRSn signal high once the voltages cross the set threshold during power up. They also function to trip the XRSn signal low if any of the voltages drop below the programmed levels. The various voltage monitors are described in subsequent sections.

Note

Not all the voltage monitors are supported for device operation in an application after boot up. In the case where a voltage monitor is not supported, an external supervisor is recommended if the device needs supply voltage monitoring while the application is running.

The three voltage monitors (I/O POR, I/O BOR, VDD POR) all have to release their respective outputs before the device begins operation (that is, XRSn goes high). However, if any of the voltage monitors trips, XRSn is driven low. The I/Os are held in high impedance when any of the voltage monitors trip.

6.13.1.2.1.1 I/O POR (Power-On Reset) Monitor

The I/O POR monitor supervises the VDDIO rail. During power up, this is the first monitor to release (that is, first to untrip) on VDDIO.

6.13.1.2.1.2 I/O BOR (Brown-Out Reset) Monitor

The I/O BOR monitor also supervises the VDDIO rail. During power up, this is the second monitor to release (that is, second to untrip) on VDDIO. This monitor has a tighter tolerance compared to the I/O POR.

Any drop in voltage below the recommended operating voltages will trip the I/O BOR and reset the device but this can be disabled by setting VMONCTL.bit.BORLVMONDIS to 1. The I/O BOR can only be disabled after the device has fully booted up. If the I/O BOR is disabled, the I/O POR will reset the device for voltage drops.

Note

The level at which the I/O POR trips is well below the minimum recommended voltage for VDDIO, and therefore should not be used for device supervision.

Figure 6-5 shows the operating region of the I/O BOR.

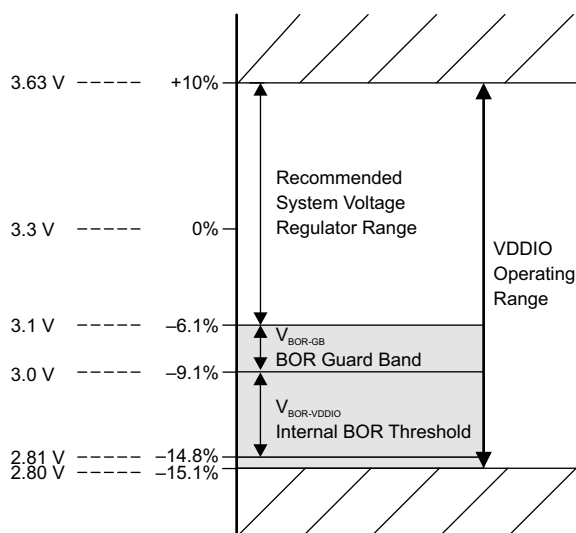


Figure 6-5. I/O BOR Operating Region

6.13.1.2.1.3 VDD POR (Power-On Reset) Monitor

The VDD POR monitor supervises the VDD rail. During power up, this monitor releases (that is, untrips) once the voltage crosses the programmed trip level on VDD.

Note

VDD POR is programmed at a level below the minimum recommended voltage for VDD, and therefore it should not be relied upon for VDD supervision if that is required in the application.

6.13.1.2.2 External Supervisor Usage

VDDIO Monitoring: The I/O BOR is supported for application use, so an external supervisor is not required to monitor the I/O rail.

VDD Monitoring:

- VDD supplied from the internal VREG: The VDD supply is derived from the VDDIO supply. The VREG is designed in such a way that a valid VDDIO supply(monitored by the IO BOR) implies a valid VDD supply.
- VDD supplied from an external supply: The VDD POR is not supported for application use. If VDD monitoring is required by the application, an external supervisor can be used to monitor the VDD rail.

Note

The use of an external supervisor with the internal VREG is not supported.If VDD monitoring is required by the application, a package with a VREGENZ pin must be used to power VDD externally.

6.13.1.2.3 Delay Blocks

The delay blocks in the path of the voltage monitors work together to delay the release time between the voltage monitors and XRSn. These delays are designed to make sure that the voltages are stable when XRSn releases in external VREG mode. The delay blocks are only active during power up (that is, when VDDIO and VDD are ramping up).

The delay blocks contribute to the minimum slew rates specified in [Power Management Module Electrical Data and Timing](#) for the power rails.

Note

The delay numbers specified in the block diagram are typical numbers.

6.13.1.2.4 Internal 1.2-V LDO Voltage Regulator (VREG)

The internal VREG is supplied by the VDDIO rail and can generate the 1.2 V required to power the VDD pins. It is enabled by tying the VREGENZ pin low. Although the internal VREG eliminates the need to use an external supply for VDD, decoupling capacitors are still required on the VDD pins for VREG stability and transients. See the *VDD Decoupling* section for details.

6.13.1.2.5 VREGENZ

The VREGENZ (VREG disable) pin controls the state of the internal VREG. To enable the internal VREG, connect the VREGENZ pin to a logic low voltage. For applications supplying VDD externally (external VREG), disable the internal VREG by tying the VREGENZ pin high.

Note

Not all device packages have VREGENZ pinned out. For packages without VREGENZ, external VREG mode is not supported.

6.13.1.3 External Components

6.13.1.3.1 Decoupling Capacitors

VDDIO and VDD require decoupling capacitors for correct operation. The requirements are outlined in subsequent sections.

6.13.1.3.1.1 VDDIO Decoupling

Place a minimum amount of decoupling capacitance on VDDIO. See the C_{VDDIO} parameter in [Power Management Module Electrical Data and Timing](#). The actual amount of decoupling capacitance to use is a requirement of the power supply driving VDDIO. Either of the configurations outlined below is acceptable:

- **Configuration 1:** Place a decoupling capacitor on each VDDIO pin per the C_{VDDIO} parameter.
- **Configuration 2:** Install a single decoupling capacitor that is the equivalent of $C_{VDDIO} * VDDIO$ pins.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.13.1.3.1.2 VDD Decoupling

Place a minimum amount of decoupling capacitance on VDD. See the C_{VDD} TOTAL parameter in [Power Management Module Electrical Data and Timing](#).

In external VREG mode, the actual amount of decoupling capacitance to use is a requirement of the power supply driving VDD.

Either of the configurations outlined below is acceptable:

- **Configuration 1:** Divide C_{VDD} TOTAL across the VDD pins.
- **Configuration 2:** Install a single decoupling capacitor with value of C_{VDD} TOTAL.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.13.1.4 Power Sequencing

6.13.1.4.1 Supply Pins Ganging

Connecting all 3.3-V rails together and supplying from a single source are strongly recommended. This list includes:

- VDDIO
- VDDA

In addition, connect all power pins to avoid leaving any unconnected.

In external VREG mode, the VDD pins should be tied together and supplied from a single source.

In internal VREG mode, tying the VDD pins together is optional as long as each VDD pin has a capacitor connected to pin. See the *VDD Decoupling* section for VDD decoupling configurations.

The analog modules on the device have fairly high PSRR; therefore, in most cases, noise on VDDA will have to exceed the recommended operating conditions of the supply rails before the analog modules see performance degradation. Therefore, supplying VDDA separately typically offers minimal benefits. Nevertheless, for the purposes of noise improvement, placing a pi filter between VDDIO and VDDA is acceptable.

Note

All the supply pins per rail are tied together internally. For example, all VDDIO pins are tied together internally, all VDD pins are tied together internally, and so forth.

6.13.1.4.2 Signal Pins Power Sequence

Before powering the device, do not apply voltage larger than 0.3 V above VDDIO or 0.3 V below VSS to any digital pin and 0.3 V above VDDA or 0.3 V below VSSA to any analog pin (including VREFHI). Simply, the signal pins should only be driven after XRSn goes high, provided all the 3.3-V rails are tied together. This sequencing is still required even if VDDIO and VDDA are not tied together.

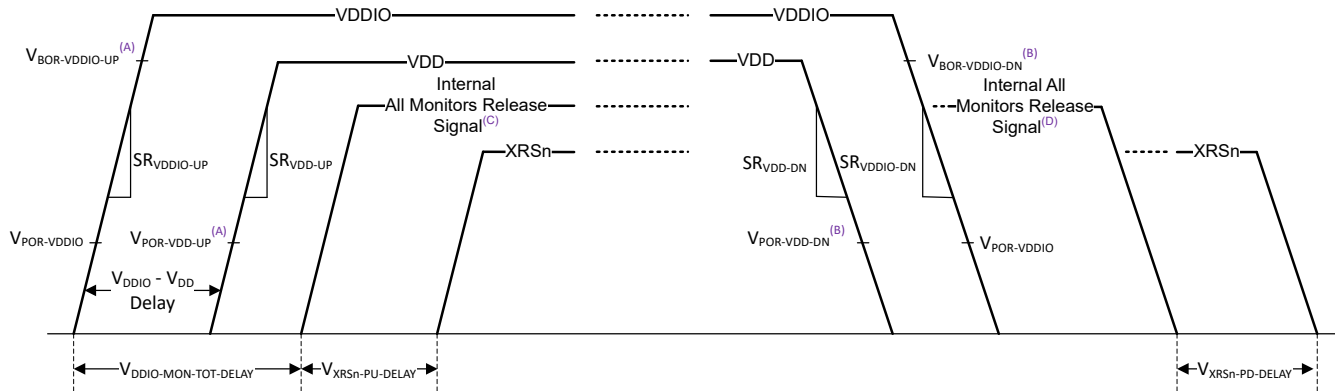
CAUTION

If the above sequence is violated, device malfunction and possibly damage can occur as current will flow through unintended parasitic paths in the device.

6.13.1.4.3 Supply Pins Power Sequence

6.13.1.4.3.1 External VREG/VDD Mode Sequence

Figure 6-6 depicts the power sequencing requirements for external VREG mode. The values for all the parameters indicated can be found in [Power Management Module Electrical Data and Timing](#).



- A. This trip point is the trip point before XRSn releases. See the Power Management Module Characteristics table.
- B. This trip point is the trip point after XRSn releases. See the Power Management Module Characteristics table.
- C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the PMM Block Diagram.
- D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the PMM Block Diagram.

Figure 6-6. External VREG Power Up Sequence

For Power Up:

1. VDDIO (that is, the 3.3-V rail) should come up first with the minimum slew rate specified.
2. VDD (that is, the 1.2-V rail) should come up next with the minimum slew rate specified.
3. The time delta between the VDDIO rail coming up and when the VDD rail can come up is also specified.
4. After the times specified by $V_{DDIO-MON-TOT-DELAY}$ and $V_{XRSN-PD-DELAY}$, XRSn will be released and the device starts the boot-up sequence.
5. The I/O BOR monitor has different release points during power up and power down.
6. During power up, both VDDIO and VDD rails have to be up before XRSn releases.

For Power Down:

1. There is no requirement between VDDIO and VDD on which should power down first; however, there is a minimum slew rate specification.
2. The I/O BOR monitor has different release points during power up and power down.
3. Any of the POR or BOR monitors that trips during power down will cause XRSn to go low after $V_{XRSN-PD-DELAY}$.

Note

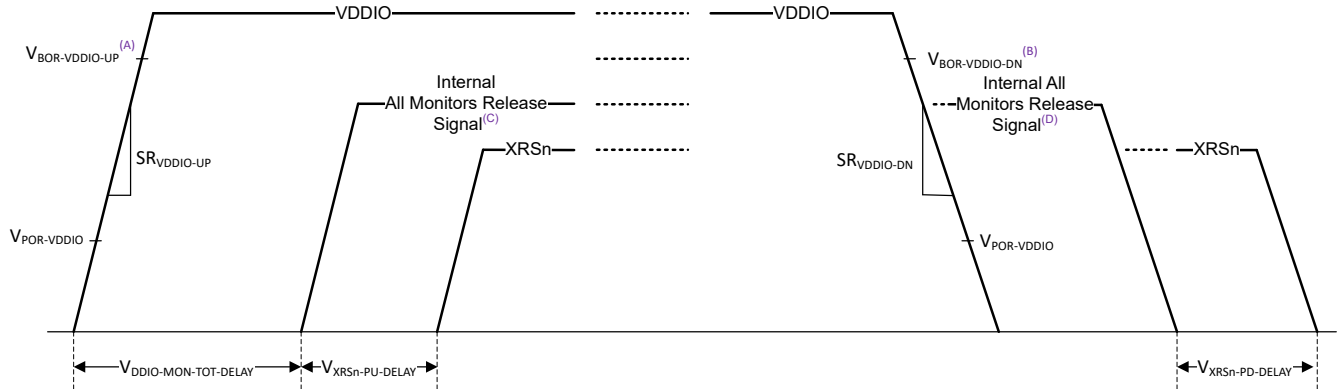
The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.13.1.4.3.2 Internal VREG/VDD Mode Sequence

Figure 6-7 depicts the power sequencing requirements for internal VREG mode. The values for all the parameters indicated can be found in [Power Management Module Electrical Data and Timing](#).



- A. This trip point is the trip point before XRSn releases. See the Power Management Module Characteristics table.
- B. This trip point is the trip point after XRSn releases. See the Power Management Module Characteristics table.
- C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the PMM Block Diagram.
- D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the PMM Block Diagram.

Figure 6-7. Internal VREG Power Up Sequence

• **For Power Up:**

1. VDDIO (that is, the 3.3-V rail) should come up with the minimum slew rate specified.
2. The Internal VREG powers up after the I/O monitors (I/O POR and I/O BOR) are released.
3. After the times specified by $V_{DDIO-MON-TOT-DELAY}$ and $V_{XRSn-PU-DELAY}$, XRSn will be released and the device starts the boot-up sequence.
4. The I/O BOR monitor has different release points during power up and power down.

• **For Power Down:**

1. The only requirement on VDDIO during power down is the slew rate.
2. The I/O BOR monitor has different release points during power up and power down.
3. The I/O BOR tripping will cause XRSn to go low after $V_{XRSn-PD-DELAY}$ and also power down the Internal VREG.

Note

The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.13.1.4.3.3 Supply Sequencing Summary and Effects of Violations

The acceptable power-up sequence for the rails is summarized below. "Power up" here means the rail in question has reached the minimum recommended operating voltage.

CAUTION
Non-acceptable sequences leads to reliability concerns and possibly damage.

For simplicity, connecting all 3.3-V rails together and following the descriptions in [Supply Pins Power Sequence](#) is recommended.

Table 6-3. External VREG Sequence Summary

| CASE | RAILS POWER-UP ORDER | | | ACCEPTABLE |
|------|----------------------|------|-----|------------|
| | VDDIO | VDDA | VDD | |
| A | 1 | 2 | 3 | Yes |
| B | 1 | 3 | 2 | Yes |
| C | 2 | 1 | 3 | - |
| D | 2 | 3 | 1 | - |
| E | 3 | 2 | 1 | - |
| F | 3 | 1 | 2 | - |
| G | 1 | 1 | 2 | Yes |
| H | 2 | 2 | 1 | - |

Table 6-4. Internal VREG Sequence Summary

| CASE | RAILS POWER-UP ORDER | | ACCEPTABLE |
|------|----------------------|------|------------|
| | VDDIO | VDDA | |
| A | 1 | 2 | Yes |
| B | 2 | 1 | - |
| C | 1 | 1 | Yes |

Note

The analog modules on the device should only be powered after VDDA has reached the minimum recommended operating voltage.

6.13.1.4.3.4 Supply Slew Rate

VDDIO has a minimum slew rate requirement. If the minimum slew rate is not met, XRSn might toggle a few times until VDDIO crosses the I/O BOR region.

Note

The toggling on XRSn has no adverse effect on the device as boot only starts once XRSn is steadily high. However if XRSn from the device is used to gate the reset signal of other ICs, then the slew rate requirement should be met to prevent this toggling.

VDD has a minimum slew rate requirement in external VREG mode. If the minimum slew rate is not met, the VDD POR may release before the VDD operational minimum voltage is met and the device may not start in a properly reset state.

6.13.1.5 Recommended Operating Conditions Applicability to the PMM

As noted in the *Recommended Operating Conditions* table, the voltage (V_{IN}) of all pins on the device should be kept above $VSS - 0.3$ V. Negative voltages below this value will inject current into the device, which could cause abnormal operation. Specific care should be taken for pins near the PMM. A negative voltage on these pins can cause the POR or BOR blocks to unexpectedly assert XRSn or disable the internal VREG (see the *PMM Block Diagram*). Pins near the PMM on this device are shown in the *Pins Near PMM* table below.

Table 6-5. Pins Near PMM

| PIN NAME | PIN NUMBER | | | |
|----------|------------|-------|--------|--------|
| | 80 PN | 64 PM | 48 PHP | 32 RHB |
| GPIO42 | 57 | – | – | – |
| GPIO8 | 58 | 47 | – | – |
| GPIO4 | 59 | 48 | 38 | – |
| GPIO3 | 60 | 49 | 39 | 26 |
| GPIO2 | 61 | 50 | 40 | – |

Table 6-5. Pins Near PMM (continued)

| PIN NAME | PIN NUMBER | | | |
|----------|------------|-------|--------|--------|
| | 80 PN | 64 PM | 48 PHP | 32 RHB |
| GPIO1 | 62 | 51 | 41 | 27 |
| GPIO0 | 63 | 52 | 42 | 28 |

Methods to avoid negative noise on pins include (in order of importance):

1. Reduce or eliminate noise at the source.
2. Avoid coupling between noise sources on these pins.
3. Filters near the device pin to isolate any noise.

6.13.1.6 Power Management Module Electrical Data and Timing

6.13.1.6.1 Power Management Module Operating Conditions

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------------|----------------------------------------------|-----------------|-----|-----|-----|-------|
| General | | | | | | |
| C_{VDDIO} (1) (2) | VDDIO Capacitance Per Pin ⁽⁷⁾ | | 0.1 | | | uF |
| C_{VDDA} (1) (2) | VDDA Capacitance Per Pin ⁽⁷⁾ | | 2.2 | | | uF |
| SR_{VDD33} (3) | Supply Ramp Rate of 3.3V Rails (VDDIO, VDDA) | | 20 | | 100 | mV/us |
| $V_{BOR-VDDIO-GB}$ (5) | VDDIO Brown Out Reset Voltage Guard Band | | | 0.1 | | V |
| External VREG | | | | | | |
| C_{VDD} TOTAL (1) (4) | Total VDD Capacitance ⁽⁷⁾ | | | 10 | | uF |
| SR_{VDD12} (3) | Supply Ramp Rate of 1.2V Rail (VDD) | | 10 | | 100 | mV/us |
| $V_{DDIO} - V_{DD}$ Delay ⁽⁶⁾ | Ramp Delay Between VDDIO and VDD | | 0 | | | us |
| Internal VREG | | | | | | |
| C_{VDD} TOTAL (1) (4) | Total VDD Capacitance ⁽⁷⁾ | | | 10 | | uF |

- (1) A bulk capacitor should also be used. The exact value of the decoupling capacitance depends on the system voltage regulation solution that is supplying these pins.
- (2) It is recommended to tie the 3.3V rails (VDDIO, VDDA) together and supply them from a single source.
- (3) See the *Supply Slew Rate* section. Supply ramp rate faster than the maximum can trigger the on-chip ESD protection.
- (4) See the *Power Management Module (PMM)* section on possible configurations for the total decoupling capacitance.
- (5) TI recommends $V_{BOR-VDDIO-GB}$ to avoid BOR-VDDIO resets due to normal supply noise or load-transient events on the 3.3-V VDDIO system regulator. Good system regulator design and decoupling capacitance (following the system regulator specifications) are important to prevent activation of the BOR-VDDIO during normal device operation. The value of $V_{BOR-VDDIO-GB}$ is a system-level design consideration; the voltage listed here is typical for many applications.
- (6) Delay between when the 3.3-V rail ramps up and when the 1.2-V rail ramps up. See the *VREG Sequence Summary* table for the allowable supply ramp sequences.
- (7) Max capacitor tolerance should be 20%.

6.13.1.6.2 Power Management Module Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|--------------------------------------------|-------------------------------|-------|-----|-------|------|
| V_{VREG} | Internal Voltage Regulator Output | | 1.152 | 1.2 | 1.248 | V |
| $V_{VREG-PU}$ | Internal Voltage Regulator Power Up Time | | | | 350 | us |
| $V_{VREG-INRUSH}$ (5) | Internal Voltage Regulator Inrush Current | | | 650 | | mA |
| $V_{POR-VDDIO}$ | VDDIO Power on Reset Voltage | Before and After XRSn Release | | 2.3 | | V |
| $V_{BOR-VDDIO-UP}$ (1) | VDDIO Brown Out Reset Voltage on Ramp Up | Before XRSn Release | | 2.7 | | V |
| $V_{BOR-VDDIO-DOWN}$ (1) | VDDIO Brown Out Reset Voltage on Ramp Down | After XRSn Release | 2.81 | | 3.0 | V |
| $V_{POR-VDD-UP}$ (2) | VDD Power on Reset Voltage on Ramp-Up | Before XRSn Release | | 1 | | V |
| $V_{POR-VDD-DOWN}$ (2) | VDD Power on Reset Voltage on Ramp-Down | After XRSn Release | | 1 | | V |

6.13.1.6.2 Power Management Module Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|------------------------------------------------------------------|---------------------------------|-----|-----|-----|------|
| $V_{XRSn-PU-DELAY}$ ⁽³⁾ | XRSn Release Delay after Supplies are Ramped Up During Power-Up | | | 40 | | us |
| $V_{XRSn-PD-DELAY}$ ⁽⁴⁾ | XRSn Trip Delay after Supplies are Ramped Down During Power-Down | | | 2 | | us |
| $V_{DDIO-MON-TOT-DELAY}$ | Total Delays in Path of VDDIO Monitors (POR, BOR) | | | 80 | | us |
| $V_{XRSn-MON-RELEASE-DELAY}$ | XRSn Release Delay after a VDD POR Event | Supplies Within Operating Range | | 40 | | us |
| | XRSn Release Delay after a VDDIO BOR Event | | | 40 | | us |
| | XRSn Release Delay after a VDDIO POR Event | | | 120 | | us |

- (1) See the *Supply Voltages* figure.
- (2) $V_{POR-VDD}$ is significantly below the recommended operating conditions. If monitoring of VDD is needed, an external supervisor is required.
- (3) Supplies are considered fully ramped up after they cross the minimum recommended operating conditions for the respective rail. All POR and BOR monitors need to be released before this delay takes effect. RC network delay will add to this.
- (4) On power down, any of the POR or BOR monitors that trips will immediately trip XRSn. This delay is the time between any of the POR, BOR monitors tripping and XRSn going low. It is variable and depends on the ramp down rate of the supply. RC network delay will add to this.
- (5) This is the transient current drawn on the VDDIO rail when the internal VREG turns on. Due to this, there might be some voltage drops on the VDDIO rail when the VREG turns on which could cause the VREG to ramp up in steps. There is no detriment to the device from this but the effect can be reduced if desired by using sufficient decoupling capacitors on VDDIO or picking an LDO/DC-DC that can supply this transient current.

6.13.2 Reset Timing

XRSn is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR) and brown-out reset (BOR) monitors. During power up, the monitor circuits keep the XRSn pin low. For more details, see the *Power Management Module (PMM)* section. A watchdog or NMI watchdog reset will also drive the pin low. An external open-drain circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between XRSn and VDDIO. A capacitor should be placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Figure 6-8 shows the recommended reset circuit.

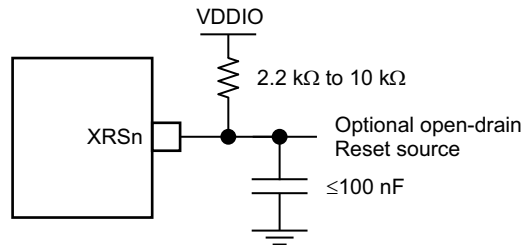


Figure 6-8. Reset Circuit

6.13.2.1 Reset Sources

The Reset Signals table summarizes the various reset signals and their effect on the device.

Table 6-6. Reset Signals

| Reset Source | CPU Core Reset (C28x, FPU, TMU) | Peripherals Reset | JTAG / Debug Logic Reset | IOs | XRS Output |
|------------------------|---------------------------------|-------------------|--------------------------|------|------------|
| POR | Yes | Yes | Yes | Hi-Z | Yes |
| BOR | Yes | Yes | Yes | Hi-Z | Yes |
| XRS Pin | Yes | Yes | No | Hi-Z | - |
| WDRS | Yes | Yes | No | Hi-Z | Yes |
| NMIWDRS | Yes | Yes | No | Hi-Z | Yes |
| SYSRS (Debugger Reset) | Yes | Yes | No | Hi-Z | No |
| SCCRESET | Yes | Yes | No | Hi-Z | No |
| SIMRESET. XRS | Yes | Yes | No | Hi-Z | Yes |
| SIMRESET. CPU1RS | Yes | Yes | No | Hi-Z | No |

The parameter $t_{h(\text{boot-mode})}$ must account for a reset initiated from any of these sources.

See the Resets section of the System Control chapter in the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#).

CAUTION

Some reset sources are internally driven by the device. Some of these sources will drive XRSn low, use this to disable any other devices driving the boot pins. The SCCRESET and debugger reset sources do not drive XRSn; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP.

6.13.2.2 Reset Electrical Data and Timing

6.13.2.2.1 Reset - XRSn - Timing Requirements

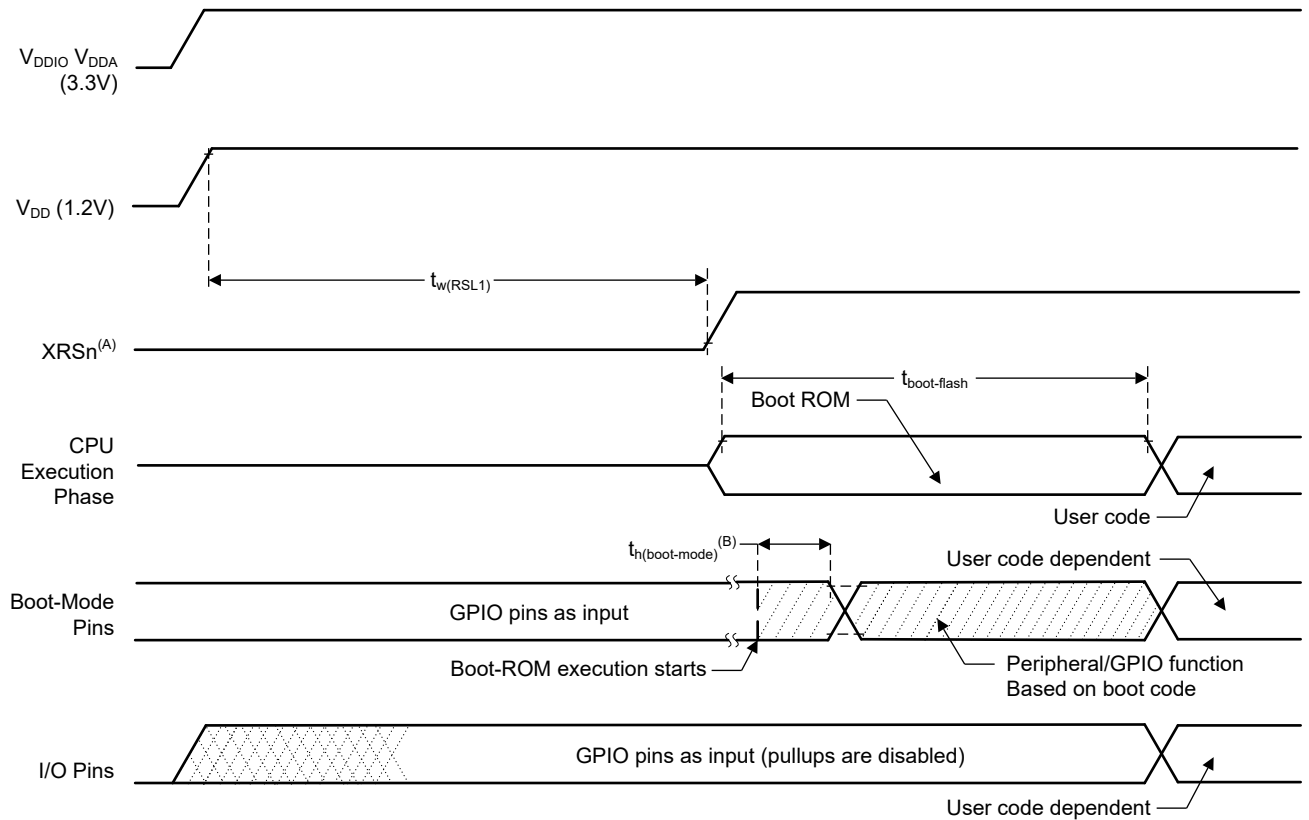
| | | MIN | MAX | UNIT |
|---------------------------|----------------------------------------|-----|-----|---------------|
| $t_{h(\text{boot-mode})}$ | Hold time for boot-mode pins | 1.5 | | ms |
| $t_{w(\text{RSL2})}$ | Pulse duration, XRSn low on warm reset | 3.2 | | μs |

6.13.2.2.2 Reset - XRSn - Switching Characteristics

over recommended operating conditions (unless otherwise noted)

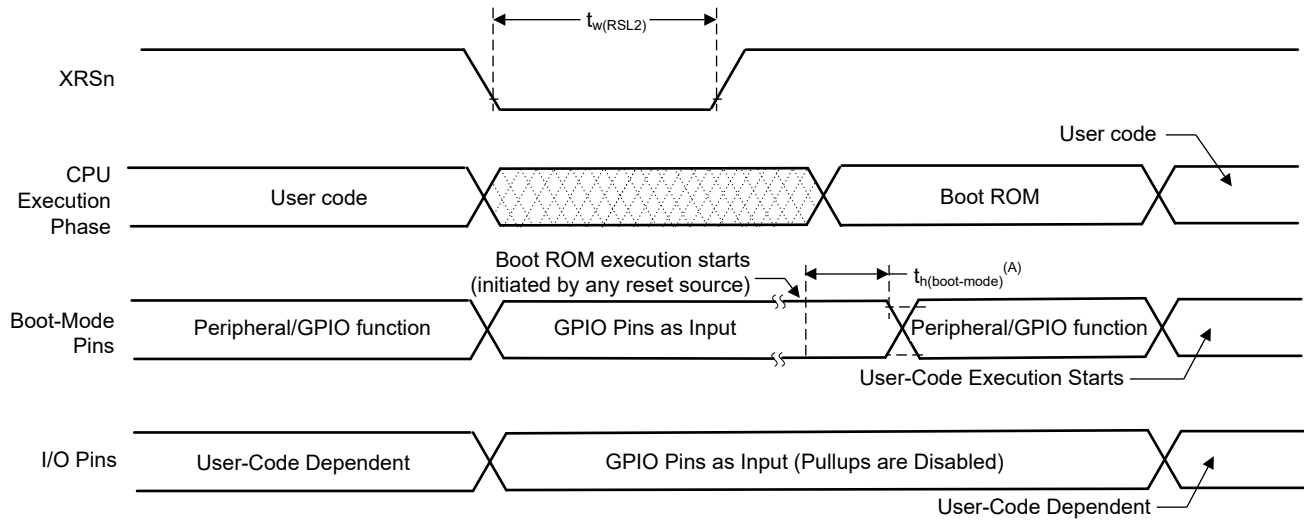
| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------------|---------------------------------------------------------------------|-----|----------------------------|-----|---------------|
| $t_{w(\text{RSL1})}$ | Pulse duration, XRSn driven low by device after supplies are stable | | 100 | | μs |
| $t_{w(\text{WDRS})}$ | Pulse duration, reset pulse generated by watchdog | | $512t_{c(\text{OSCCCLK})}$ | | cycles |
| $t_{\text{boot-flash}}$ | Boot-ROM execution time to first instruction fetch in flash | | | 1.2 | ms |

6.13.2.2.3 Reset Timing Diagrams



- The XRSn pin can be driven externally by a supervisor or an external pullup resistor, see the Pin Attributes table. On-chip monitors will hold this pin low until the supplies are in a valid range.
- After reset from any source (see the Reset Sources section), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-9. Power-on Reset



- A. After reset from any source (see the Reset Sources section), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-10. Warm Reset

6.13.3 Clock Specifications

6.13.3.1 Clock Sources

Table 6-7. Possible Reference Clock Sources

| CLOCK SOURCE | DESCRIPTION |
|------------------------|-------------------------------------------------------------------------------------------------------------------|
| INTOSC1 | Internal oscillator 1. 10-MHz internal oscillator. |
| INTOSC2 ⁽¹⁾ | Internal oscillator 2. 10-MHz internal oscillator. |
| X1 (XTAL) | External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin. |

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for the PLL (OSCCLK).

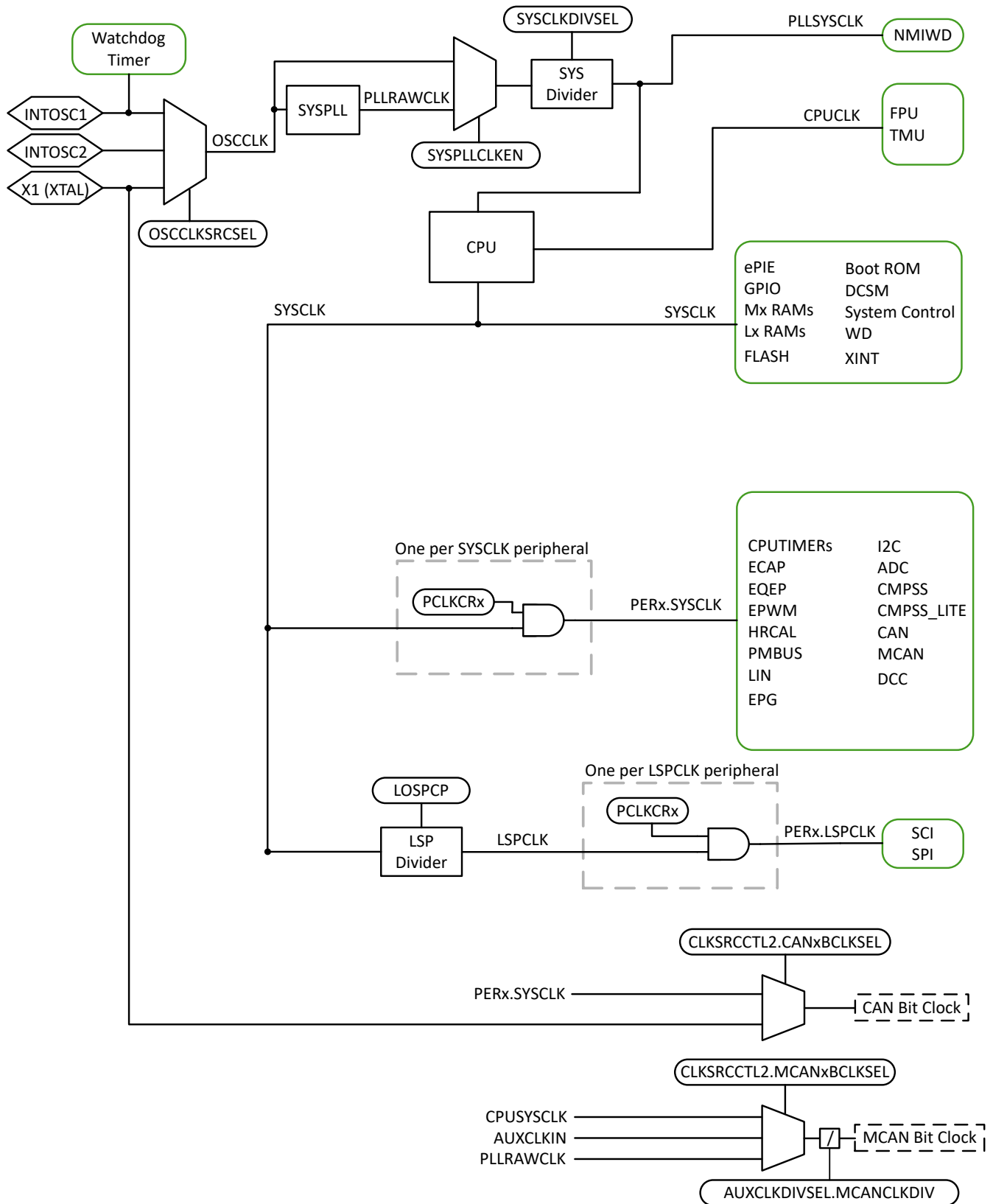


Figure 6-11. Clocking System

SYSPLL

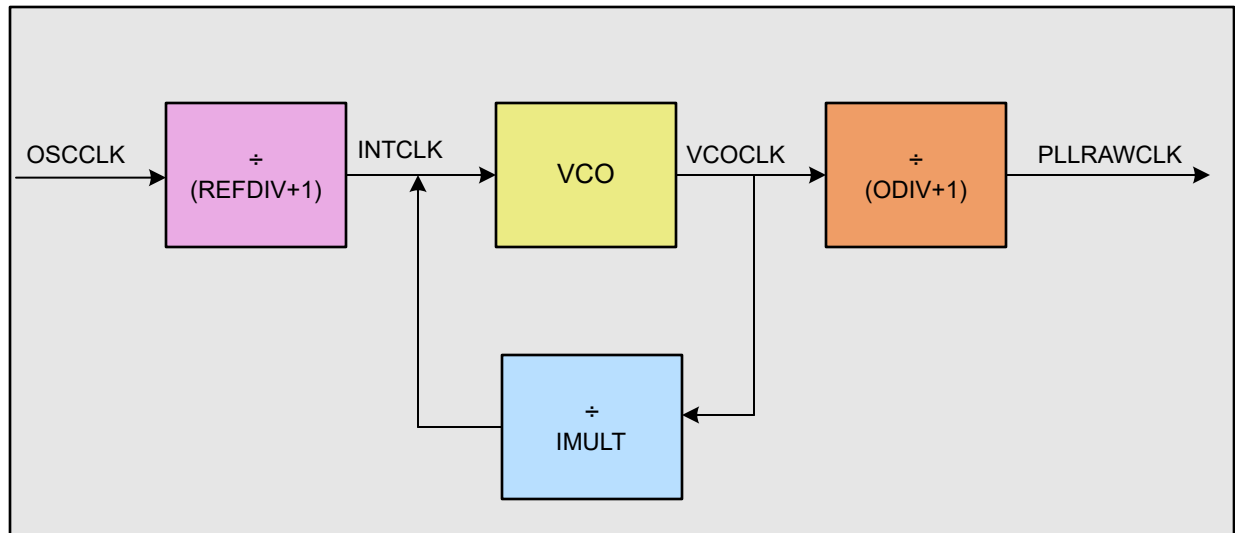


Figure 6-12. System PLL

In the *System PLL* figure,

$$f_{PLLRAWCLK} = \frac{f_{OSCCLK}}{(REFDIV + 1)} \times \frac{IMULT}{(ODIV + 1)} \quad (1)$$

6.13.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

6.13.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

6.13.3.2.1.1 Input Clock Frequency

| | | MIN | MAX | UNIT |
|--------------|------------------------------------------------------|-----|-----|------|
| $f_{(XTAL)}$ | Frequency, X1/X2, from external crystal or resonator | 10 | 20 | MHz |
| $f_{(X1)}$ | Frequency, X1, from external oscillator | 10 | 25 | MHz |

6.13.3.2.1.2 XTAL Oscillator Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------|--------------------------------|-------------|-----|-------------|------|
| X1 V_{IL} | Valid low-level input voltage | -0.3 | | 0.3 * VDDIO | V |
| X1 V_{IH} | Valid high-level input voltage | 0.7 * VDDIO | | VDDIO + 0.3 | V |

6.13.3.2.1.3 X1 Input Level Characteristics When Using an External Clock Source - Not a Crystal

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|-------------|-----------------------------------------|-------------|-------------|------|
| X1 V_{IL} | Valid low-level input voltage (Buffer) | -0.3 | 0.3 * VDDIO | V |
| X1 V_{IH} | Valid high-level input voltage (Buffer) | 0.7 * VDDIO | VDDIO + 0.3 | V |

6.13.3.2.1.4 X1 Timing Requirements

| | | MIN | MAX | UNIT |
|--------------|--------------------------------------------------------|-----|---------|------|
| $t_{f(X1)}$ | Fall time, X1 | | 6 | ns |
| $t_{r(X1)}$ | Rise time, X1 | | 6 | ns |
| $t_{w(X1L)}$ | Pulse duration, X1 low as a percentage of $t_{c(X1)}$ | | 45% 55% | |
| $t_{w(X1H)}$ | Pulse duration, X1 high as a percentage of $t_{c(X1)}$ | | 45% 55% | |

6.13.3.2.1.5 AUXCLKIN Timing Requirements

| | | MIN | MAX | UNIT |
|---------------|---------------------------------------------------------------|-----|---------|------|
| $t_{f(AUXI)}$ | Fall time, AUXCLKIN | | 6 | ns |
| $t_{r(AUXI)}$ | Rise time, AUXCLKIN | | 6 | ns |
| $t_{w(AUXL)}$ | Pulse duration, AUXCLKIN low as a percentage of $t_{c(XCI)}$ | | 45% 55% | |
| $t_{w(AUXH)}$ | Pulse duration, AUXCLKIN high as a percentage of $t_{c(XCI)}$ | | 45% 55% | |

6.13.3.2.1.6 APLL Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT |
|----------------------------------|-----|-----|--------------------------------------------------|------|
| PLL Lock time | | | | |
| SYS PLL Lock Time ⁽¹⁾ | | | $5\mu s + (1024 * (REFDIV + 1) * t_{c(OSCCLK)})$ | us |

- (1) The PLL lock time here defines the typical time that takes for the PLL to lock once PLL is enabled (SYSPLLCTL1[PLLENA]=1). Additional time to verify the PLL clock using Dual Clock Comparator (DCC) is not accounted here. TI recommends using the latest example software from C2000Ware for initializing the PLLs. For the system PLL, see InitSysPll() or SysCtl_setClock().

6.13.3.2.1.7 XCLKOUT Switching Characteristics - PLL Bypassed or Enabled

over recommended operating conditions (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|--------------------------|--------------------|-----|-----|------|
| $t_{f(XCO)}$ | Fall time, XCLKOUT | | 6 | ns |
| $t_{r(XCO)}$ | Rise time, XCLKOUT | | 6 | ns |

6.13.3.2.1.7 XCLKOUT Switching Characteristics - PLL Bypassed or Enabled (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|--------------------------|------------------------------|---------------|---------------|------|
| $t_{w(XCOL)}$ | Pulse duration, XCLKOUT low | $H - 2^{(2)}$ | $H + 2^{(2)}$ | ns |
| $t_{w(XCOH)}$ | Pulse duration, XCLKOUT high | $H - 2^{(2)}$ | $H + 2^{(2)}$ | ns |
| $f_{(XCO)}$ | Frequency, XCLKOUT | | 50 | MHz |

(1) A load of 6 pF is assumed for these parameters.

(2) $H = 0.5t_{c(XCO)}$

6.13.3.2.1.8 Internal Clock Frequencies

| | | MIN | NOM | MAX | UNIT |
|------------------------------|------------------------------------------------------------------------------------------|------|----------------------|-----|------|
| $f_{(SYSCLK)}$ | Frequency, device (system) clock | 2 | | 120 | MHz |
| $f_{(SYSCLK_TA_GRADE_0)}$ | Frequency, device (system) clock at AEC-Q100 Grade 0 free-air temperature ⁽²⁾ | 2 | | 60 | MHz |
| $t_{c(SYSCLK)}$ | Period, device (system) clock | 8.33 | | 500 | ns |
| $f_{(INTCLK)}$ | Frequency, system PLL going into VCO (after REFDIV) | 2 | | 20 | MHz |
| $f_{(VCOCLK)}$ | Frequency, system PLL VCO (before ODIV) | 220 | | 600 | MHz |
| $f_{(PLLRAWCLK)}$ | Frequency, system PLL output (before SYSCLK divider) | 6 | | 240 | MHz |
| $f_{(PLL)}$ | Frequency, PLLSYSCLK | 2 | | 120 | MHz |
| $f_{(PLL_LIMP)}$ | Frequency, PLL Limp Frequency ⁽¹⁾ | | $45/(ODIV+1)$ | | MHz |
| $f_{(LSP)}$ | Frequency, LSPCLK | 2 | | 120 | MHz |
| $t_{c(LSPCLK)}$ | Period, LSPCLK | 8.33 | | 500 | ns |
| $f_{(OSCCLK)}$ | Frequency, OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1) | | See respective clock | | MHz |
| $f_{(EPWM)}$ | Frequency, EPWMCLK | | | 120 | MHz |
| $f_{(HRPWM)}$ | Frequency, HRPWMCLK | 60 | | 120 | MHz |

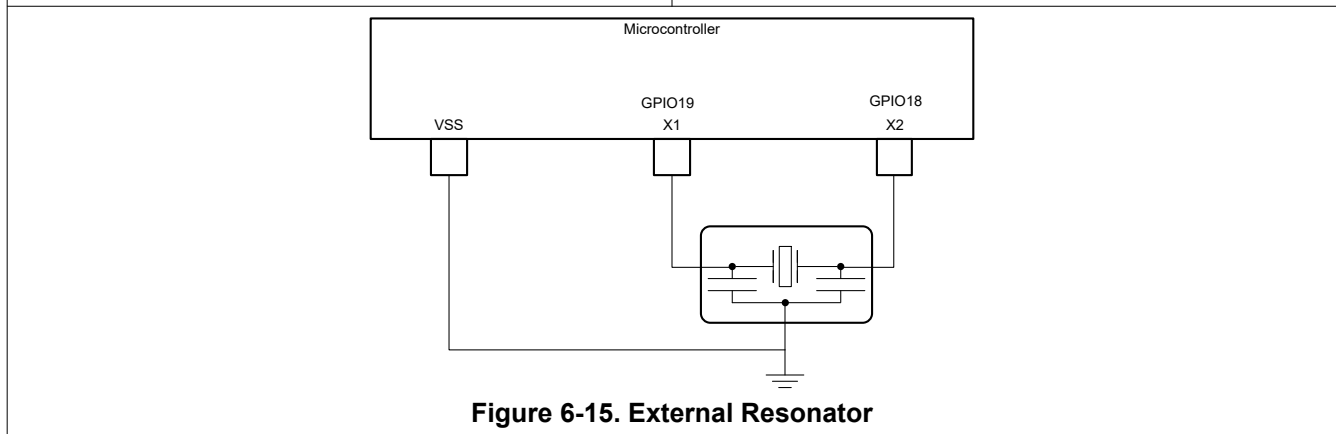
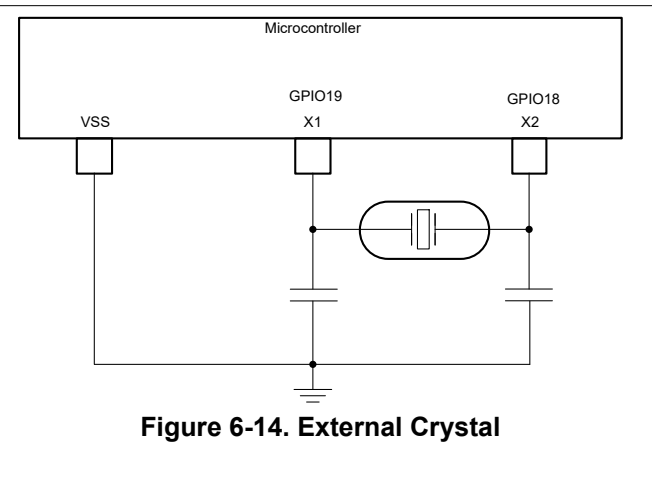
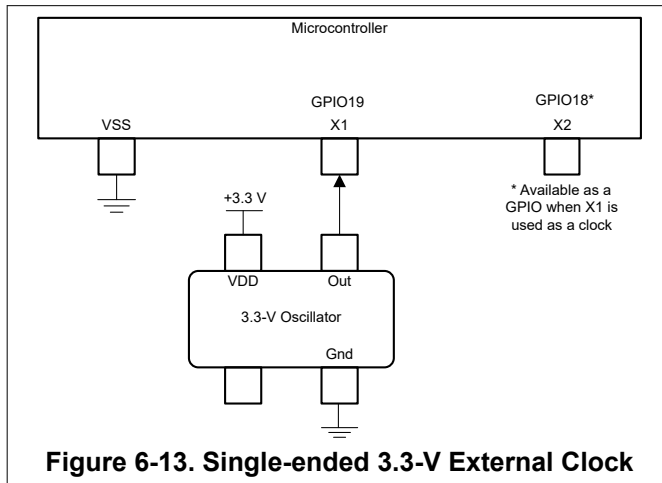
(1) PLL output frequency when OSCCLK is dead (Loss of OSCCLK causes PLL to Limp).

(2) For more details regarding changing device frequency for thermal management, see *Thermal Design Considerations for AEC-Q100 Grade 0* section.

6.13.3.3 Input Clocks and PLLs

In addition to the internal 0-pin oscillators, three types of external clock sources are supported:

- A single-ended 3.3-V external clock. The clock signal should be connected to X1, as shown in [Figure 6-13](#), with the XTALCR.SE bit set to 1.
- An external crystal. The crystal should be connected across X1 and X2 with its load capacitors connected to VSS as shown in [Figure 6-14](#).
- An external resonator. The resonator should be connected across X1 and X2 with its ground connected to VSS as shown in [Figure 6-15](#).



6.13.3.4 XTAL Oscillator

6.13.3.4.1 Introduction

The crystal oscillator in this device is an embedded electrical oscillator that, when paired with a compatible quartz crystal (or a ceramic resonator), can generate the system clock required by the device.

6.13.3.4.2 Overview

The following sections describe the components of the electrical oscillator and crystal.

6.13.3.4.2.1 Electrical Oscillator

The electrical oscillator in this device is a Pierce oscillator. It is a positive feedback inverter circuit that requires a tuning circuit in order to oscillate. When this oscillator is paired with a compatible crystal, a tank circuit is formed. This tank circuit oscillates at the fundamental frequency of the crystal. On this device, the oscillator is designed to operate in parallel resonance mode due to the shunt capacitor (C0) and required load capacitors (CL). [Figure 6-16](#) illustrates the components of the electrical oscillator and the tank circuit.

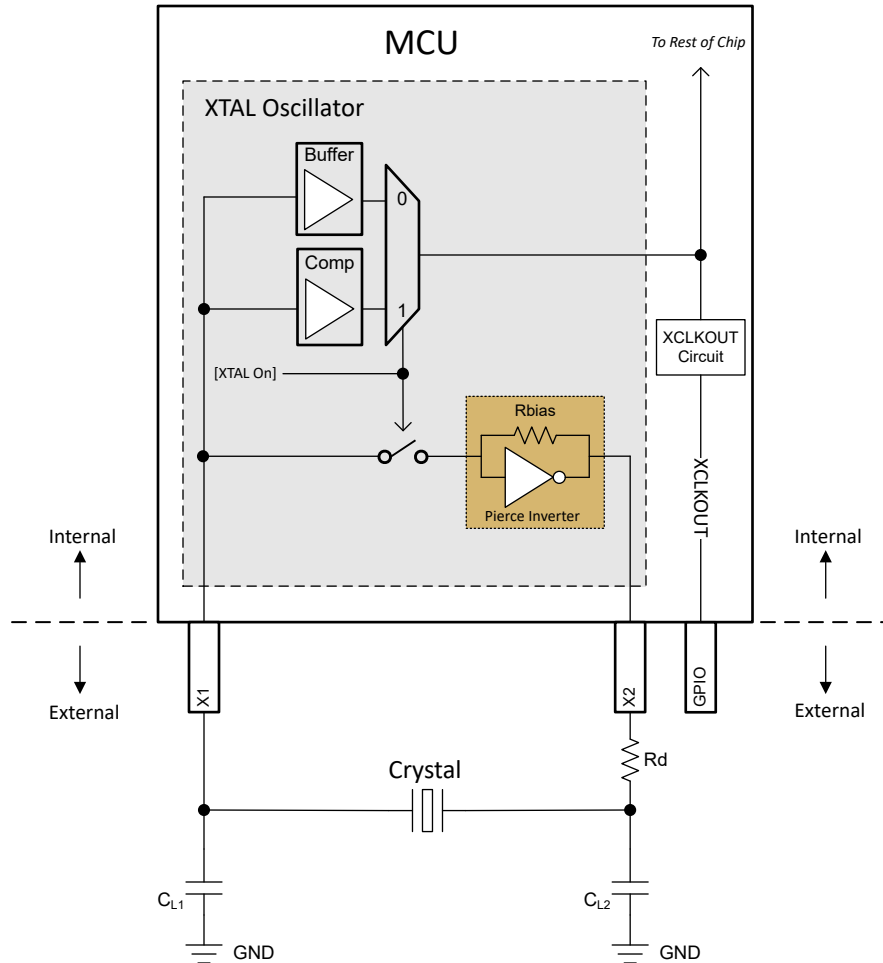


Figure 6-16. Electrical Oscillator Block Diagram

6.13.3.4.2.1.1 Modes of Operation

The electrical oscillator in this device has two modes of operation: crystal mode and single-ended mode.

6.13.3.4.2.1.1.1 Crystal Mode of Operation

In the crystal mode of operation, a quartz crystal with load capacitors has to be connected to X1 and X2.

This mode of operation is engaged when $[XTAL\ On] = 1$, which is achieved by setting $XTALCR.OSCOFF = 0$ and $XTALCR.SE = 0$. There is an internal bias resistor for the feedback loop so an external one should not be used. Adding an external bias resistor will create a parallel resistance with the internal R_{bias} , moving the bias point of operation and possibly leading to clipped waveforms, out-of-specification duty cycle, and reduction in the effective negative resistance.

In this mode of operation, the resultant clock on X1 is passed through a comparator (Comp) to the rest of the chip. The clock on X1 needs to meet the V_{IH} and V_{IL} of the comparator. See the *XTAL Oscillator Characteristics* table for the V_{IH} and V_{IL} requirements of the comparator.

6.13.3.4.2.1.1.2 Single-Ended Mode of Operation

In the single-ended mode of operation, a clock signal is connected to X1 with X2 left unconnected. A quartz crystal should not be used in this mode.

This mode is enabled when $[XTAL\ On] = 0$, which can be achieved by setting $XTALCR.OSCOFF = 1$ and $XTALCR.SE = 1$.

In this mode of operation, the clock on X1 is passed through a buffer (Buffer) to the rest of the chip. See the *X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)* table for the input requirements of the buffer.

6.13.3.4.2.1.2 XTAL Output on XCLKOUT

The output of the electrical oscillator that is fed to the rest of the chip can be brought out on XCLKOUT for observation by configuring the CLKSRCCTL3.XCLKOUTSEL and XCLKOUTDIVSEL.XCLKOUTDIV registers. See the GPIO Muxed Pins table for a list of GPIOs that XCLKOUT comes out on.

6.13.3.4.2.2 Quartz Crystal

Electrically, a quartz crystal can be represented by an LCR (Inductor-Capacitor-Resistor) circuit. However, unlike an LCR circuit, crystals have very high Q due to the low motional resistance and are also very underdamped. Components of the crystal are shown in Figure 6-17 and explained below.

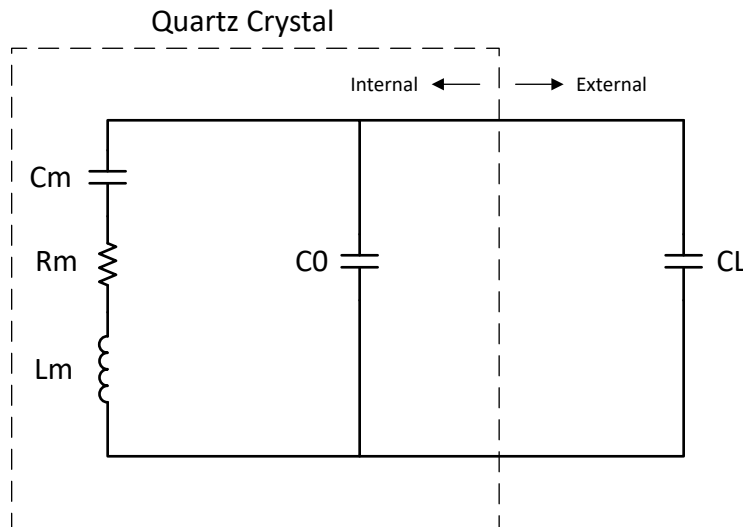


Figure 6-17. Crystal Electrical Representation

Cm (Motional capacitance): Denotes the elasticity of the crystal.

Rm (Motional resistance): Denotes the resistive losses within the crystal. This is not the ESR of the crystal but can be approximated as such depending on the values of the other crystal components.

Lm (Motional inductance): Denotes the vibrating mass of the crystal.

C0 (Shunt capacitance): The capacitance formed from the two crystal electrodes and stray package capacitance.

CL (Load capacitance): This is the effective capacitance seen by the crystal at its electrodes. It is external to the crystal. The frequency ppm specified in the crystal data sheet is usually tied to the CL parameter.

Note that most crystal manufacturers specify CL as the effective capacitance seen at the crystal pins, while some crystal manufacturers specify CL as the capacitance on just one of the crystal pins. Check with the crystal manufacturer for how the CL is specified in order to use the correct values in calculations.

From Figure 6-16, CL1 and CL2 are in series; so, to find the equivalent total capacitance seen by the crystal, the capacitance series formula has to be applied which simply evaluates to $[CL1]/2$ if $CL1 = CL2$.

It is recommended that a stray PCB capacitance be added to this value. 3 pF to 5 pF are reasonable estimates, but the actual value will depend on the PCB in question.

Note that the load capacitance is a requirement of both the electrical oscillator and crystal. The value chosen has to satisfy both the electrical oscillator and the crystal.

The effect of CL on the crystal is frequency-pulling. If the effective load capacitance is lower than the target, the crystal frequency will increase and vice versa. However, the effect of frequency-pulling is usually very minimal and typically results in less than 10-ppm variation from the nominal frequency.

6.13.3.4.2.3 GPIO Modes of Operation

On this device, X1 and X2 can be used as GPIO19 and GPIO18, respectively, depending on the operating mode of the XTAL. Refer to the External Oscillator (XTAL) section of the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#).

6.13.3.4.3 Functional Operation

6.13.3.4.3.1 ESR – Effective Series Resistance

Effective Series Resistance is the resistive load the crystal presents to the electrical oscillator at resonance. The higher the ESR, the lower the Q, and less likely the crystal will start up or maintain oscillation. The relationship between ESR and the crystal components is indicated below.

$$ESR = R_m * \left(1 + \frac{C_0}{CL}\right)^2 \quad (2)$$

Note that ESR is not the same as motional resistance of the crystal, but can be approximated as such if the effective load capacitance is much greater than the shunt capacitance.

6.13.3.4.3.2 Rneg – Negative Resistance

Negative resistance is the impedance presented by the electrical oscillator to the crystal. It is the amount of energy the electrical oscillator must supply to the crystal to overcome the losses incurred during oscillation. Rneg depicts a circuit that provides rather than consume energy and can also be viewed as the overall gain of the circuit.

The generally accepted practice is to have Rneg > 3x ESR to 5x ESR to ensure the crystal starts up under all conditions. Note that it takes slightly more energy to start up the crystal than it does to sustain oscillation; therefore, if it can be ensured that the negative resistance requirement is met at start-up, then oscillation sustenance will not be an issue.

[Figure 6-18](#) and [Figure 6-19](#) show the variation between negative resistance and the crystal components for this device. As can be seen from the graphs, the crystal shunt capacitance (C0) and effective load capacitance (CL) greatly influence the negative resistance of the electrical oscillator. Note that these are typical graphs; so, refer to [Table 6-8](#) for minimum and maximum values for design considerations.

6.13.3.4.3.3 Start-up Time

Start-up time is an important consideration when selecting the components of the crystal circuit. As mentioned in the [Rneg – Negative Resistance](#) section, for reliable start-up across all conditions, it is recommended that the Rneg > 3x ESR to 5x ESR of the crystal.

Crystal ESR and the dampening resistor (Rd) greatly affect the start-up time. The higher the two values, the longer the crystal takes to start up. Longer start-up times are usually a sign that the crystal and components are not a correct match.

Refer to [Crystal Oscillator Specifications](#) for the typical start-up times. Note that the numbers specified here are typical numbers provided for guidance only. Actual start-up time depends heavily on the crystal in question and the external components.

6.13.3.4.3.3.1 X1/X2 Precondition

On this device, the GPIO19/18 alternate functionality on X1/X2 can be used to speed up the start-up time of the crystal if needed. This functionality is achieved by preconditioning the load capacitors CL1 and CL2 to a known state before the XTAL is turned on. See the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#) for details.

6.13.3.4.3.4 DL – Drive Level

Drive level refers to how much power is provided by the electrical oscillator and dissipated by the crystal. The maximum drive level specified in the crystal manufacturer's data sheet is usually the maximum the crystal can dissipate without damage or significant reduction in operating life. On the other hand, the drive level specified by the electrical oscillator is the maximum power it can provide. The actual power provided by the electrical oscillator is not necessarily the maximum power and depends on the crystal and board components.

For cases where the actual drive level from the electrical oscillator exceeds the maximum drive level specification of the crystal, a dampening resistor (R_d) should be installed to limit the current and reduce the power dissipated by the crystal. Note that R_d reduces the circuit gain; and therefore, the actual value to use should be evaluated to make sure all other conditions for start-up and sustained oscillation are met.

6.13.3.4.4 How to Choose a Crystal

Using [Crystal Oscillator Specifications](#) as a reference:

1. Pick a crystal frequency (for example, 20 MHz).
2. Check that the ESR of the crystal $\leq 50 \Omega$ per specifications for 20 MHz.
3. Check that the load capacitance requirement of the crystal manufacturer is within 6 pF and 12 pF per specifications for 20 MHz.
 - As mentioned, CL1 and CL2 are in series; so, provided $CL1 = CL2$, effective load capacitance $CL = [CL1]/2$.
 - Adding board parasitics to this results in $CL = [CL1]/2 + C_{stray}$
4. Check that the maximum drive level of the crystal ≥ 1 mW. If this requirement is not met, a dampening resistor R_d can be used. Refer to [DL – Drive Level](#) on other points to consider when using R_d .

6.13.3.4.5 Testing

It is recommended that the user have the crystal manufacturer completely characterize the crystal with their board to ensure the crystal always starts up and maintains oscillation.

Below is a brief overview of some measurements that can be performed:

Due to how sensitive the crystal circuit is to capacitance, it is recommended that scope probes not be connected to X1 and X2. If scope probes must be used to monitor X1/X2, an active probe with less than 1-pF input capacitance should be used.

Frequency

1. Bring out the XTAL on XCLKOUT.
2. Measure this frequency as the crystal frequency.

Negative Resistance

1. Bring out the XTAL on XCLKOUT.
2. Place a potentiometer in series with the crystal between the load capacitors.
3. Increase the resistance of the potentiometer until the clock on XCLKOUT stops.
4. This resistance plus the crystal's actual ESR is the negative resistance of the electrical oscillator.

Start-Up Time

1. Turn off the XTAL.
2. Bring out the XTAL on XCLKOUT.
3. Turn on the XTAL and measure how long it takes the clock on XCLKOUT to stay within 45% and 55% duty cycle.

6.13.3.4.6 Common Problems and Debug Tips

Crystal Fails to Start Up

- Go through the [How to Choose a Crystal](#) section and make sure there are no violations.

Crystal Takes a Long Time to Start Up

- If a dampening resistor Rd is installed, it is too high.
- If no dampening resistor is installed, either the crystal ESR is too high or the overall circuit gain is too low due to high load capacitance.

6.13.3.4.7 Crystal Oscillator Specifications

6.13.3.4.7.1 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|------------|---------------------------------------------------|-----|-----|-----|------|
| Start-up time ⁽¹⁾ | f = 10 MHz | ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF | | 4 | | ms |
| | f = 20 MHz | ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF | | 2 | | ms |
| Crystal drive level (DL) | | | | | 1 | mW |

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

6.13.3.4.7.2 Crystal Equivalent Series Resistance (ESR) Requirements

For the [Crystal Equivalent Series Resistance \(ESR\) Requirements](#) table:

- Crystal shunt capacitance (C0) should be less than or equal to 7 pF.
- ESR = Negative Resistance/3

Table 6-8. Crystal Equivalent Series Resistance (ESR) Requirements

| CRYSTAL FREQUENCY (MHz) | MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF) | MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF) |
|-------------------------|----------------------------------------|----------------------------------------|
| 10 | 55 | 110 |
| 12 | 50 | 95 |
| 14 | 50 | 90 |
| 16 | 45 | 75 |
| 18 | 45 | 65 |
| 20 | 45 | 50 |

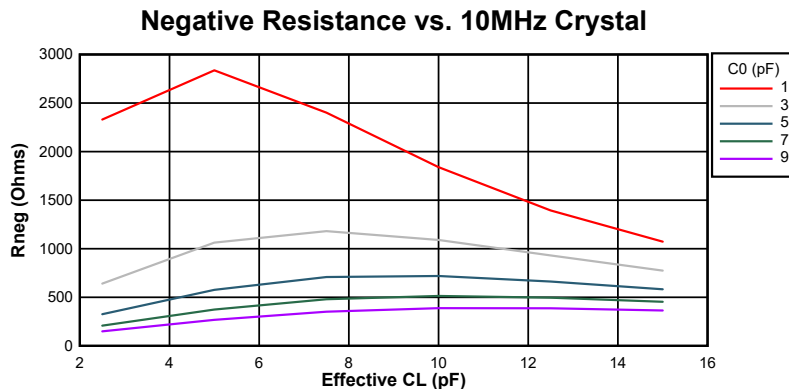


Figure 6-18. Negative Resistance Variation at 10 MHz

Negative Resistance vs. 20MHz Crystal

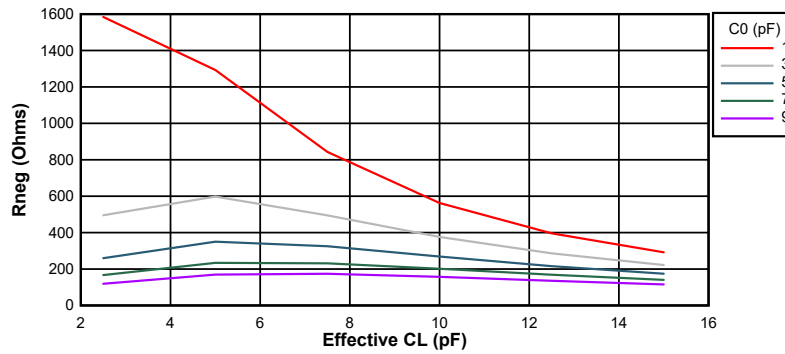


Figure 6-19. Negative Resistance Variation at 20 MHz

6.13.3.4.7.3 Crystal Oscillator Parameters

| | | MIN | MAX | UNIT |
|----------|---------------------------|-----|-----|------|
| CL1, CL2 | Load capacitance | 12 | 24 | pF |
| C0 | Crystal shunt capacitance | | 7 | pF |

6.13.3.4.7.4 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|------------|---------------------------------------------------|-----|-----|-----|------|
| Start-up time ⁽¹⁾ | f = 10 MHz | ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF | | 4 | | ms |
| | f = 20 MHz | ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF | | 2 | | ms |
| Crystal drive level (DL) | | | | | 1 | mW |

- (1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

6.13.3.5 Internal Oscillators

To reduce production board costs and application development time, all F280015x devices contain two independent internal oscillators, referred to as INTOSC1 and INTOSC2. By default, INTOSC2 is set as the source for the system reference clock (OSCCLK) and INTOSC1 is set as the backup clock source.

Applications requiring tighter **SCI baud rate matching** can use the SCI baud tuning example (baud_tune_via_uart) available in C2000Ware.

6.13.3.5.1 INTOSC Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | PART | PACKAGE SUFFIX | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|-----------------------------------------|-----------------------|-----------------|-------------------|-----|-------------|------|
| f _{INTOSC} | F2800157, F2800155 | PN (non-Q1) | -40°C to 125°C | 9.82 (-1.8%) | 10 | 10.1 (1.0%) | MHz |
| | | | -30°C to 90°C | 9.86 (-1.4%) | 10 | 10.1 (1.0%) | |
| | | | -10°C to 85°C | 9.9 (-1.0%) | 10 | 10.1 (1.0%) | |
| | F280015xQ, F280015xE parts | RHB, PHP, PM, PN (Q1) | -40°C to 125°C | 9.7 (-3.0%) | 10 | 10.3 (3.0%) | |
| | F280015xE parts | PHP | -40°C to 150°C | | 10 | | |
| f _{INTOSC-STABILITY} | Frequency stability at room temperature | All | All | 30°C, Nominal VDD | | ±0.1 | % |
| t _{INTOSC-ST} | Start-up and settling time | All | All | | | 20 | µs |

(1) INTOSC frequency may shift due to the thermal and mechanical stress of solder reflow. A post-reflow bake can restore the unit to its original data sheet performance.

6.13.3.5.2 INTOSC2 with External Precision Resistor – ExtR

To achieve better accuracy, an external precision resistor can be used with INTOSC2.

The external components required are:

- 100-kΩ precision resistor between ExtR pin and VSS
- 10-nF capacitor for noise filtering
- 20-µF VDDIO capacitance minimum for low noise supply and load transients

Figure 6-20 shows an example illustration of these required external components.

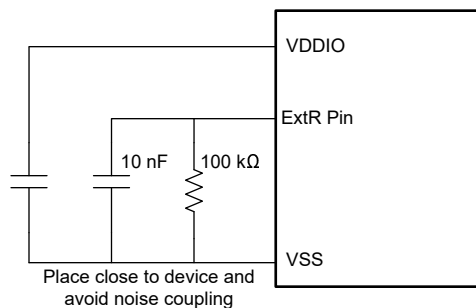


Figure 6-20. ExtR Example Schematic

In ExtR mode, the oscillator frequency error is directly proportional to the accuracy of the ExtR resistor.

The quality of the VDDIO supply directly affects the ExtR INTOSC performance. VDDIO capacitance values and circuit design must be decided with care to provide the cleanest supply possible to avoid jitter, noise, and other performance issues.

Placing a resistor on the ExtR pin prevents the pin from being used as a GPIO or X1.

Table 6-9 provides the ExtR specification values.

Table 6-9. ExtR Specifications

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------------------|-------------------------------------|------|-----|-------|------|
| f _{INTOSC2-ExtR-ERR-PERC} | Ideal 0% error 100 kΩ ExtR resistor | -0.7 | 0 | +0.7 | % |
| f _{INTOSC2-ExtR} | Ideal 0% error 100 kΩ ExtR resistor | 9.93 | 10 | 10.07 | MHz |
| f _{ExtR-SETTLING} | Switch to ExtR Mode | | 1 | | ms |
| ExtR Resistance, R _{ExtR} | | | 100 | | kΩ |
| ExtR Decoupling Capacitance, C _{ExtR} | | | 10 | | nF |
| VDDIO Decoupling Capacitance, C _{VDDIO} | | 20 | | | μF |

Table 6-10 provides an example calculation for determining the total error of INTOSC2 given the parameters of a resistor.

Table 6-10. Sample Total Error Calculation

| PARAMETER | VALUE | UNIT |
|---------------------------------------|----------------------------------------------------------------------------------------------------------------|--------|
| INTOSC2 Ideal Frequency Variation | 0.70 | % |
| ExtR Resistor Tolerance | R _{TOLERANCE} | % |
| ExtR Resistor Temperature Coefficient | R _{TEMPCO} | ppm/°C |
| Operating Temperature | T _{OPERATING_POINT} | °C |
| ExtR Data Sheet Ambient Temperature | T _{AMBIENT} | °C |
| Total Frequency Error | $[(0.70/100) + (R_{TOLERANCE}/100) + ((R_{TEMPCO}/1E6) * \text{abs}(T_{OPERATING_POINT} - T_{AMBIENT}))]*100$ | % |

Table 6-11 provides example values using the above calculation.

Table 6-11. Total Error Example Values

| PARAMETER | VALUE | UNIT |
|---------------------------------------|--------------------------------------------------------------------|--------|
| INTOSC2 Ideal Frequency Variation | 0.70 | % |
| ExtR Resistor Tolerance | 0.10 | % |
| ExtR Resistor Temperature Coefficient | 25 | ppm/°C |
| Operating Temperature | 90 | °C |
| ExtR Data Sheet Ambient Temperature | 25 | °C |
| Total Frequency Error Calculation | $((0.70/100) + (0.10/100) + ((25/1E6) * \text{abs}(90-25))) * 100$ | % |
| Total Frequency Error Calculation | 0.96 | % |

For best performance, use the following board layout guidelines:

- Route ExtR trace as short as possible
- Route ExtR to the nearest VSS pin
- Place ExtR (R_{ExtR}) and C_{ExtR} on the same side as the C2000 device, with routing on the same layer only
- Any adjacent GPIO pin (GPIO18, X2 for example) can be routed using the opposite side and in a different layer so as to reduce adjacent GPIO coupling
- VSS connection must be tied both to VSS plane and directly to C2000 device VSS pin
- VSS guard trace is recommended around the ExtR trace as shown in [Figure 6-21](#)
- Fill VSS or VDDIO plane in layer below ExtR and C_{ExtR} to avoid routing signal traces in adjacent layer

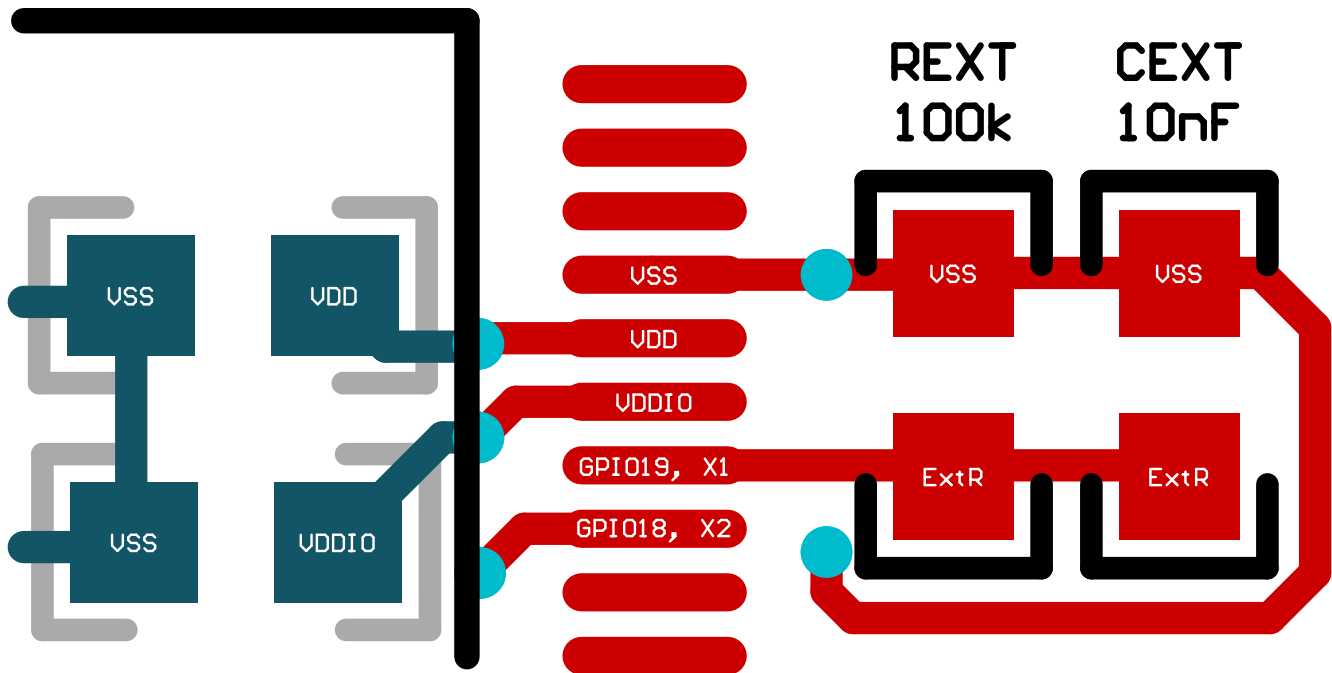


Figure 6-21. ExtR PCB Layout Example

6.13.4 Flash Parameters

Table 6-12 lists the minimum required Flash wait states with different clock sources and frequencies. Wait state is the value set in register FRDCNTL[RWAIT].

Table 6-12. Minimum Required Flash Wait States with Different Clock Sources and Frequencies

| CPUCLK (MHz) | Wait States (FRDCNTL[RWAIT] ⁽¹⁾) |
|-------------------|----------------------------------------------|
| 80 < CPUCLK ≤ 120 | 2 |
| 0 < CPUCLK ≤ 80 | 1 |

(1) Minimum required FRDCNTL[RWAIT] is 1, RWAIT=0 is not supported.

The F280015x devices have an improved 128-bit prefetch buffer that provides high flash code execution efficiency across wait states. Figure 6-22 and Figure 6-23 illustrate typical efficiency across wait-state settings compared to previous-generation devices with a 64-bit prefetch buffer. Wait-state execution efficiency with a prefetch buffer will depend on how many branches are present in application software. Two examples of linear code and if-then-else code are provided.

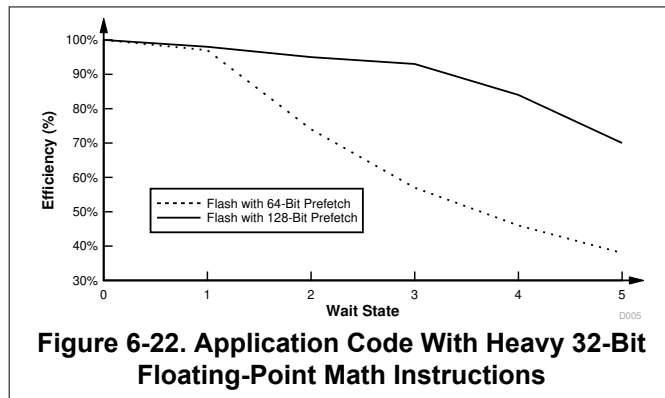


Figure 6-22. Application Code With Heavy 32-Bit Floating-Point Math Instructions

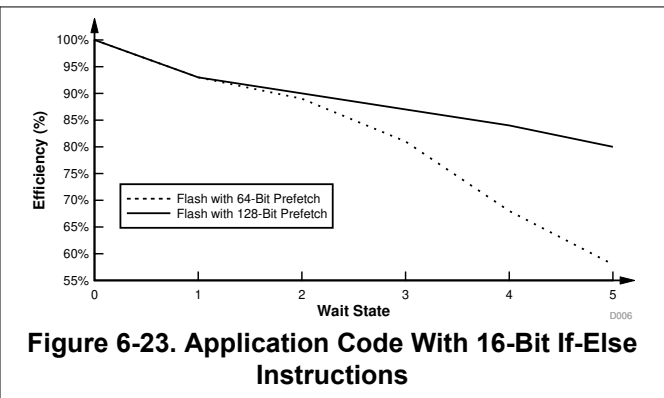


Figure 6-23. Application Code With 16-Bit If-Else Instructions

Note

The Main Array flash programming must be aligned to 64-bit address boundaries and each 64-bit word may only be programmed once per write/erase cycle.

6.13.4.1 Flash Parameters

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------------------------|-----------------------------|-----|------|--------|--------|
| Program Time ⁽¹⁾ | 128 data bits + 16 ECC bits | | 62.5 | 625 | μs |
| | 2KB (Sector) | | 8 | 80 | μs |
| Erase Time ^{(2) (3)} at < 25 cycles | 2KB (Sector) | | 15 | 55 | ms |
| | 64KB | | 17 | 61 | ms |
| | 128KB | | 18 | 66 | ms |
| | 256KB | | 21 | 78 | ms |
| Erase Time ^{(2) (3)} at 1000 cycles | 2KB (Sector) | | 25 | 130 | ms |
| | 64KB | | 28 | 143 | ms |
| | 128KB | | 30 | 157 | ms |
| | 256KB | | 35 | 183 | ms |
| Erase Time ^{(2) (3)} at 2000 cycles | 2KB (Sector) | | 30 | 221 | ms |
| | 64KB | | 33 | 243 | ms |
| | 128KB | | 36 | 265 | ms |
| | 256KB | | 42 | 310 | ms |
| Erase Time ^{(2) (3)} at 20K cycles | 2KB (Sector) | | 120 | 1003 | ms |
| | 64KB | | 132 | 1102 | ms |
| | 128KB | | 145 | 1205 | ms |
| | 256KB | | 169 | 1410 | ms |
| N _{wec} Write/Erase Cycles per Bank ⁽⁴⁾ | | | | 100000 | cycles |
| t _{retention} Data retention duration at T _J = 85°C | | 20 | | | years |

- (1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
- Code that uses flash API to program the flash
 - Flash API itself
 - Flash data to be programmed
- In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the JTAG debug probe used. Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does. Erase time includes Erase verify by the CPU and does not involve any data transfer.
- (2) Erase time includes Erase verify by the CPU.
- (3) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.
- (4) The combined total of bank and sector write/erase cycles is limited to this number.

6.13.5 RAM Specifications

Table 6-13. RAM Parameters

| RAM TYPE | SIZE EACH | FETCH TIME (CYCLES) | READ TIME (CYCLES) | STORE TIME (CYCLES) | SUPPORTED BUS WIDTHS (BITS) | HOST ACCESS LIST | WAIT STATES | BURST ACCESS SUPPORT |
|----------|-----------|---------------------|--------------------|---------------------|-----------------------------|------------------|-------------|----------------------|
| LS RAM | 32KB | 2 | 2 | 1 | 16/32 | C28x | 0 | No |
| M0 | 2KB | | | | | | | |
| M1 | | | | | | | | |

6.13.6 ROM Specifications

Table 6-14. ROM Parameters

| RAM TYPE | SIZE EACH | FETCH TIME (CYCLES) | READ TIME (CYCLES) | STORE TIME (CYCLES) | SUPPORTED BUS WIDTHS (BITS) | HOST ACCESS LIST | WAIT STATES | BURST ACCESS SUPPORT |
|-----------------------|-----------|---------------------|--------------------|---------------------|-----------------------------|------------------|-------------|----------------------|
| Boot ROM + Secure ROM | 96KB | 2 | 2 | 1 | 16/32 | C28x | 0 | No |

6.13.7 Emulation/JTAG

The JTAG (IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture) port has four dedicated pins: TMS, TDI, TDO, and TCK. The cJTAG (IEEE Standard 1149.7-2009 for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture) port is a compact JTAG interface requiring only two pins (TMS and TCK), which allows other device functionality to be muxed to the traditional GPIO35 (TDI) and GPIO37 (TDO) pins.

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most JTAG debug probe operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22- Ω resistors should be placed in series on each JTAG signal.

The PD (Power Detect) pin of the JTAG debug probe header should be connected to the board's 3.3-V supply. Header GND pins should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output pin back to the RTCK input pin of the header (to sense clock continuity by the JTAG debug probe). This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 k Ω to 4.7 k Ω (depending on the drive strength of the debugger ports). Typically, a 2.2-k Ω value is used.

Header pin $\overline{\text{RESET}}$ is an open-drain output from the JTAG debug probe header that enables board components to be reset through JTAG debug probe commands (available only through the 20-pin header). [Figure 6-24](#) shows how the 14-pin JTAG header connects to the MCU's JTAG port signals. [Figure 6-25](#) shows how to connect to the 20-pin JTAG header. The 20-pin JTAG header pins EMU2, EMU3, and EMU4 are not used and should be grounded.

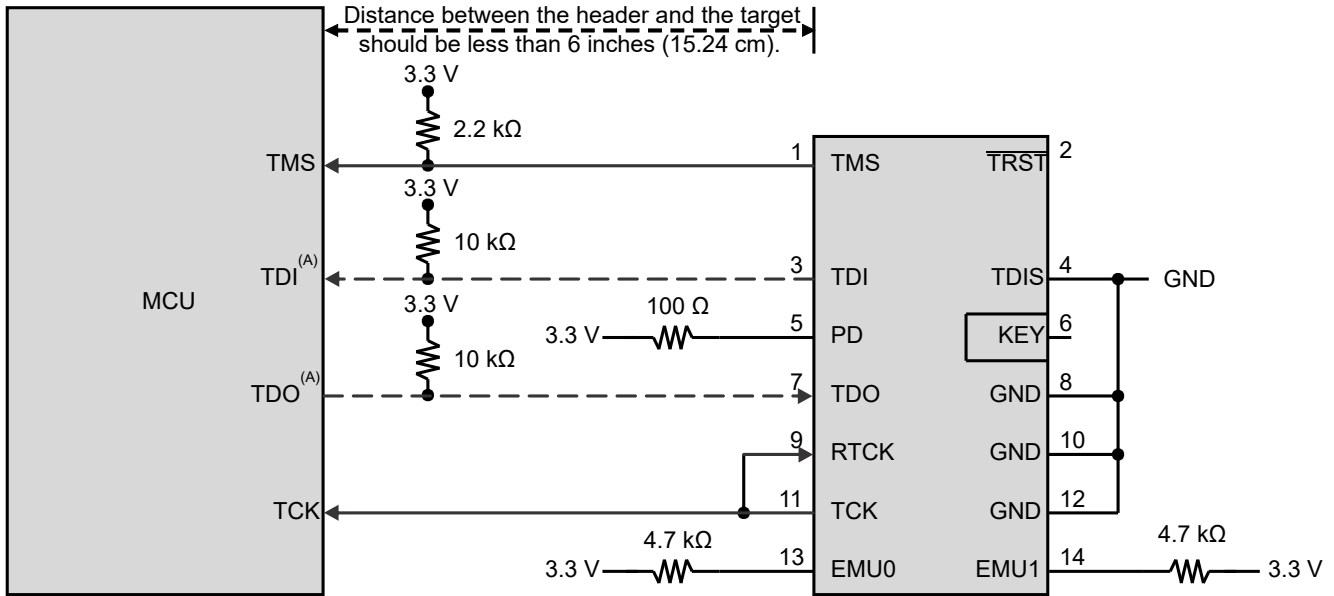
For more information about hardware breakpoints and watchpoints, see [Hardware Breakpoints and Watchpoints in CCS for C2000 devices](#).

For more information about JTAG emulation, see the [XDS Target Connection Guide](#).

Note

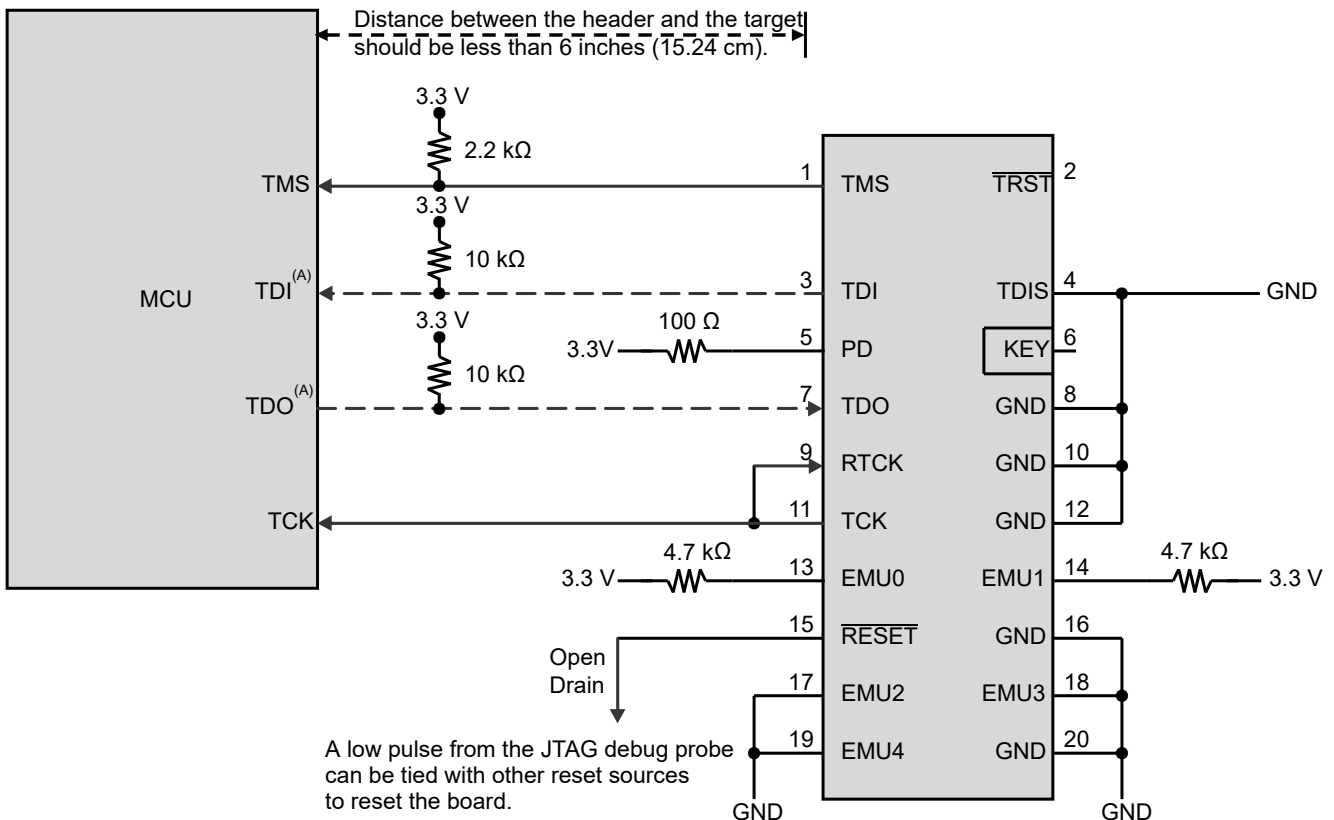
JTAG Test Data Input (TDI) is the default mux selection for the pin. The internal pullup is disabled by default. If this pin is used as JTAG TDI, the internal pullup should be enabled or an external pullup added on the board to avoid a floating input. In the cJTAG option, this pin can be used as GPIO.

JTAG Test Data Output (TDO) is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating. The internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. In the cJTAG option, this pin can be used as GPIO.



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-24. Connecting to the 14-Pin JTAG Header



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-25. Connecting to the 20-Pin JTAG Header

6.13.7.1 JTAG Electrical Data and Timing

6.13.7.1.1 JTAG Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|---------------------------|------------------------------------------|-------|-----|------|
| 1 | $t_c(\text{TCK})$ | Cycle time, TCK | 66.66 | | ns |
| 1a | $t_w(\text{TCKH})$ | Pulse duration, TCK high (40% of t_c) | 26.66 | | ns |
| 1b | $t_w(\text{TCKL})$ | Pulse duration, TCK low (40% of t_c) | 26.66 | | ns |
| 3 | $t_{su}(\text{TDI-TCKH})$ | Input setup time, TDI valid to TCK high | 7 | | ns |
| | $t_{su}(\text{TMS-TCKH})$ | Input setup time, TMS valid to TCK high | 7 | | |
| 4 | $t_h(\text{TCKH-TDI})$ | Input hold time, TDI valid from TCK high | 7 | | ns |
| | $t_h(\text{TCKH-TMS})$ | Input hold time, TMS valid from TCK high | 7 | | |

6.13.7.1.2 JTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|-----|------------------------|----------------------------------|-----|-----|------|
| 2 | $t_d(\text{TCKL-TDO})$ | Delay time, TCK low to TDO valid | 6 | 20 | ns |

6.13.7.1.3 JTAG Timing Diagram

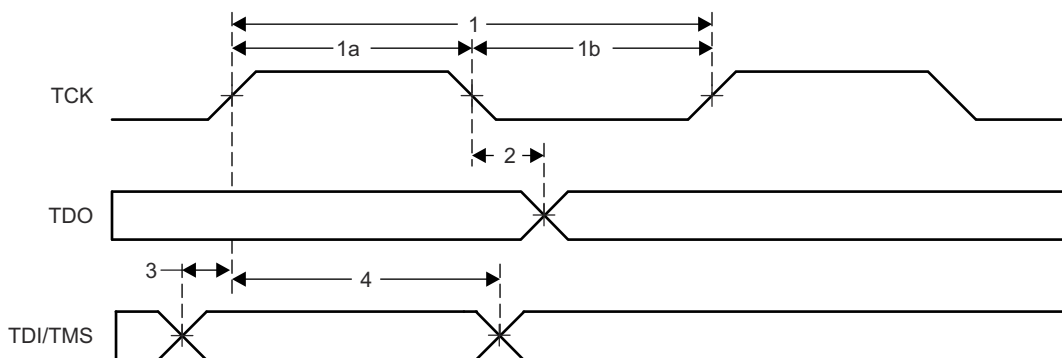


Figure 6-26. JTAG Timing

6.13.7.2 cJTAG Electrical Data and Timing

6.13.7.2.1 cJTAG Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|--------------------|------------------------------------------|-----|-----|------|
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 100 | | ns |
| 1a | $t_{w(TCKH)}$ | Pulse duration, TCK high (40% of t_c) | 40 | | ns |
| 1b | $t_{w(TCKL)}$ | Pulse duration, TCK low (40% of t_c) | 40 | | ns |
| 3 | $t_{su(TMS-TCKH)}$ | Input setup time, TMS valid to TCK high | 7 | | ns |
| | $t_{su(TMS-TCKL)}$ | Input setup time, TMS valid to TCK low | 7 | | ns |
| 4 | $t_h(TCKH-TMS)$ | Input hold time, TMS valid from TCK high | 2 | | ns |
| | $t_h(TCKL-TMS)$ | Input hold time, TMS valid from TCK low | 2 | | ns |

6.13.7.2.2 cJTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|---------------------|-------------------------------------|-----|------|
| 2 | $t_d(TCKL-TMS)$ | Delay time, TCK low to TMS valid | 20 | ns |
| 5 | $t_{dis}(TCKH-TMS)$ | Delay time, TCK high to TMS disable | 20 | ns |

6.13.7.2.3 cJTAG Timing Diagram

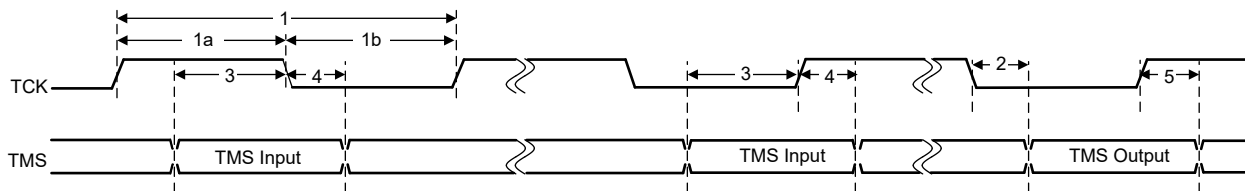


Figure 6-27. cJTAG Timing

6.13.8 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

The GPIO module contains an Output X-BAR which allows an assortment of internal signals to be routed to a GPIO in the GPIO mux positions denoted as OUTPUTXBARx. The GPIO module also contains an Input X-BAR which is used to route signals from any GPIO input to different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts. For more details, see the X-BAR chapter in the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#).

6.13.8.1 GPIO – Output Timing

6.13.8.1.1 General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | MIN | MAX | UNIT |
|--------------|---------------------------------------|-----------|-----|------------------|------|
| $t_{r(GPO)}$ | Rise time, GPIO switching low to high | All GPIOs | | 6 ⁽¹⁾ | ns |
| $t_{f(GPO)}$ | Fall time, GPIO switching high to low | All GPIOs | | 6 ⁽¹⁾ | ns |
| f_{GPO} | Toggling frequency, GPIO pins | | | 50 | MHz |

(1) Rise time and fall time vary with load. These values assume a 6-pF load.

6.13.8.1.2 General-Purpose Output Timing Diagram

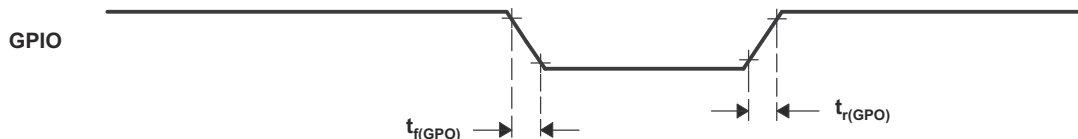


Figure 6-28. General-Purpose Output Timing

6.13.8.2 GPIO – Input Timing

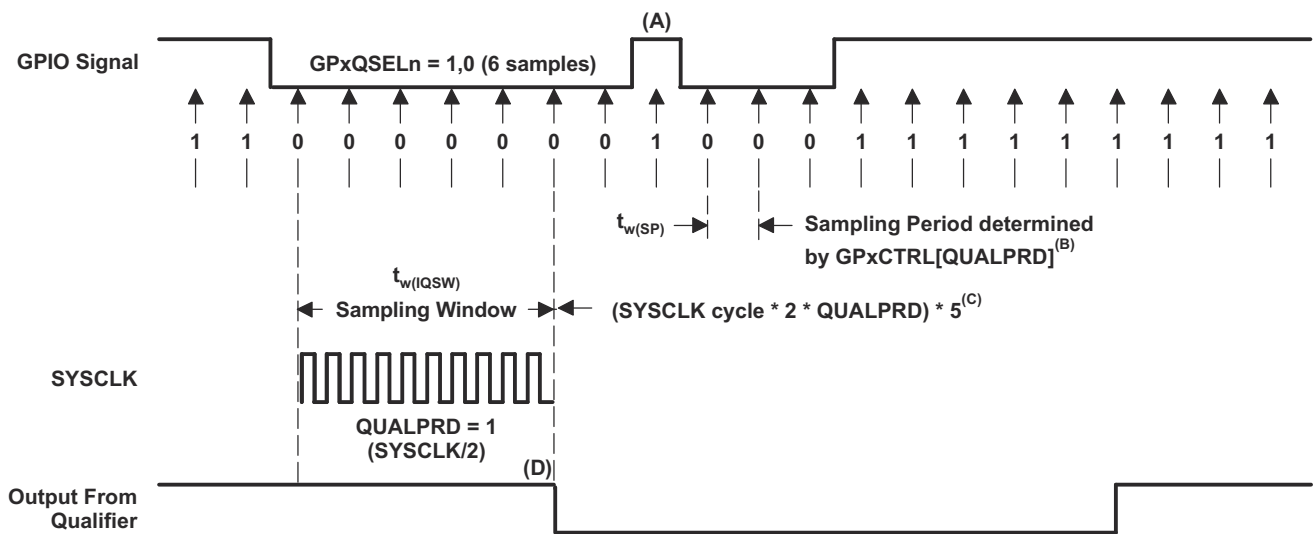
6.13.8.2.1 General-Purpose Input Timing Requirements

| | | | MIN | MAX | UNIT |
|--------------------|---------------------------------|----------------------|-----|--------------------------------------------|--------|
| $t_{w(SP)}$ | Sampling period | QUALPRD = 0 | | $1t_{c(SYSCLK)}$ | cycles |
| | | QUALPRD \neq 0 | | $2t_{c(SYSCLK)} * QUALPRD$ | cycles |
| $t_{w(IQSW)}$ | Input qualifier sampling window | | | $t_{w(SP)} * (n^{(1)} - 1)$ | cycles |
| $t_{w(GPI)}^{(2)}$ | Pulse duration, GPIO low/high | Synchronous mode | | $2t_{c(SYSCLK)}$ | cycles |
| | | With input qualifier | | $t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$ | cycles |

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.

(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.

6.13.8.2.2 Sampling Mode



- A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCCLK cycle. For any other value "n", the qualification sampling period is 2n SYSCCLK cycles (that is, at every 2n SYSCCLK cycles, the GPIO pin will be sampled).
- B. The qualification period selected through the GPxCTRL register applies to groups of eight GPIO pins.
- C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
- D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCCLK cycles or greater. In other words, the inputs should be stable for $(5 * QUALPRD * 2)$ SYSCCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, a 13-SYSCCLK-wide pulse ensures reliable recognition.

Figure 6-29. Sampling Mode

6.13.8.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

Sampling frequency = $\text{SYSCLK} / (2 \times \text{QUALPRD})$, if $\text{QUALPRD} \neq 0$

Sampling frequency = SYSCLK , if $\text{QUALPRD} = 0$

Sampling period = $\text{SYSCLK cycle} \times 2 \times \text{QUALPRD}$, if $\text{QUALPRD} \neq 0$

In the previous equations, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle , if $\text{QUALPRD} = 0$

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = $(\text{SYSCLK cycle} \times 2 \times \text{QUALPRD}) \times 2$, if $\text{QUALPRD} \neq 0$

Sampling window width = $(\text{SYSCLK cycle}) \times 2$, if $\text{QUALPRD} = 0$

Case 2:

Qualification using 6 samples

Sampling window width = $(\text{SYSCLK cycle} \times 2 \times \text{QUALPRD}) \times 5$, if $\text{QUALPRD} \neq 0$

Sampling window width = $(\text{SYSCLK cycle}) \times 5$, if $\text{QUALPRD} = 0$

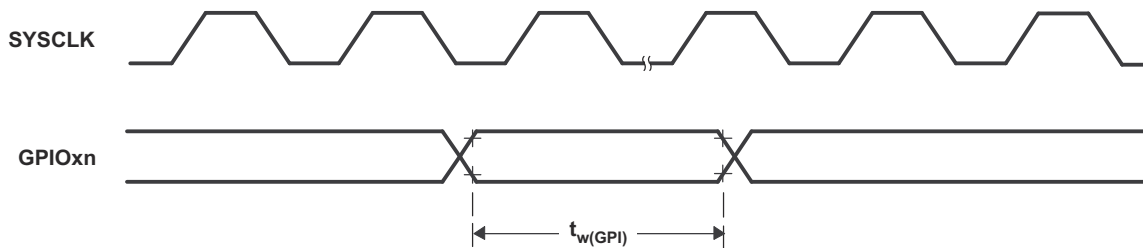


Figure 6-30. General-Purpose Input Timing

6.13.9 Interrupts

The C28x CPU has fourteen peripheral interrupt lines. Two of them (INT13 and INT14) are connected directly to CPU timers 1 and 2, respectively. The remaining twelve are connected to peripheral interrupt signals through the enhanced Peripheral Interrupt Expansion (ePIE) module. The ePIE multiplexes up to sixteen peripheral interrupts into each CPU interrupt line. It also expands the vector table to allow each interrupt to have its own ISR. This allows the CPU to support a large number of peripherals.

An interrupt path is divided into three stages—the peripheral, the ePIE, and the CPU. Each stage has its own enable and flag registers. This system allows the CPU to handle one interrupt while others are pending, implement and prioritize nested interrupts in software, and disable interrupts during certain critical tasks.

Figure 6-31 shows the interrupt architecture for this device.

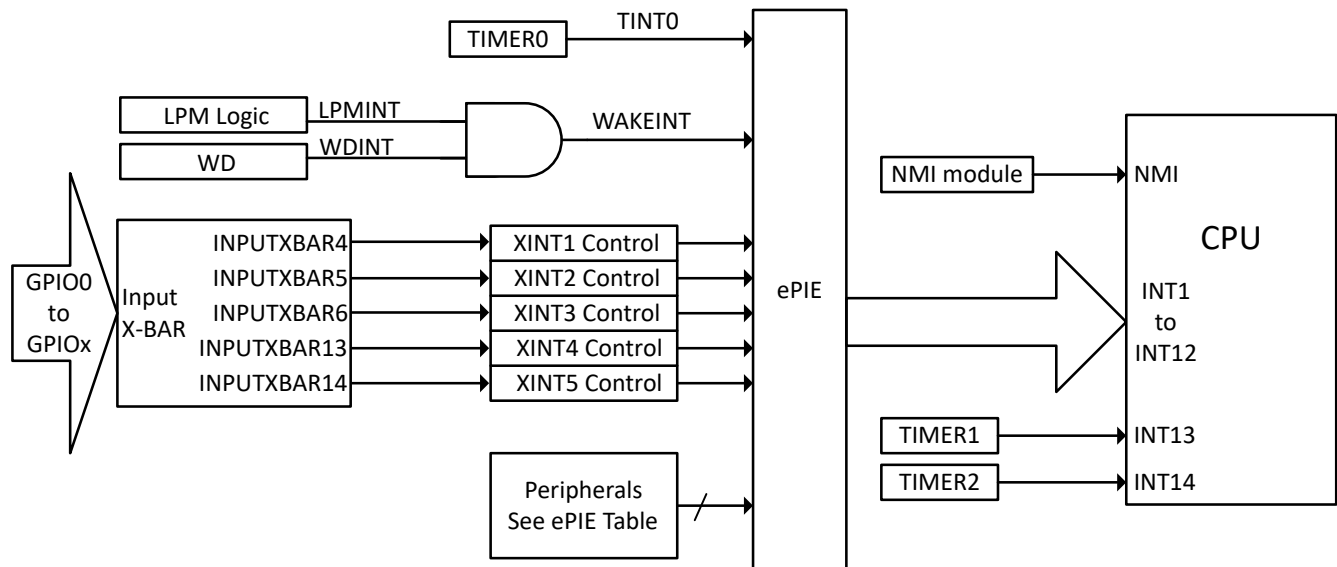


Figure 6-31. Device Interrupt Architecture

6.13.9.1 External Interrupt (XINT) Electrical Data and Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.13.9.1.1 External Interrupt Timing Requirements

| | | | MIN | MAX | UNIT |
|--------------|------------------------------------|----------------|--------------------------------------------|-----|--------|
| $t_{w(INT)}$ | Pulse duration, INT input low/high | Synchronous | $2t_{c(SYSCLK)}$ | | cycles |
| | | With qualifier | $t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$ | | cycles |

6.13.9.1.2 External Interrupt Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|--------------|-------------------------------------------------------------------|---------------------------------|---------------------------------------------|--------|
| $t_{d(INT)}$ | Delay time, INT low/high to interrupt-vector fetch ⁽¹⁾ | $t_{w(IQSW)} + 14t_{c(SYSCLK)}$ | $t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCLK)}$ | cycles |

(1) This assumes that the ISR is in a single-cycle memory.

6.13.9.1.3 External Interrupt Timing

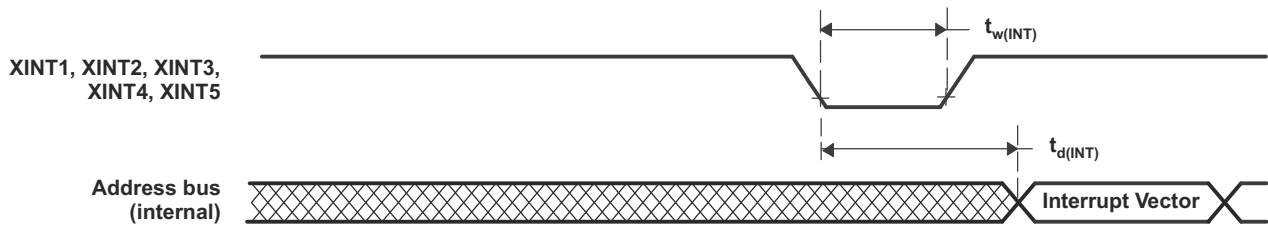


Figure 6-32. External Interrupt Timing

6.13.10 Low-Power Modes

This device has HALT, IDLE and STANDBY as clock-gating low-power modes.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the Low-Power Modes section of the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#).

6.13.10.1 Clock-Gating Low-Power Modes

IDLE and HALT modes on this device are similar to those on other C28x devices. [Table 6-15](#) describes the effect on the system when any of the clock-gating low-power modes are entered.

Table 6-15. Effect of Clock-Gating Low-Power Modes on the Device

| MODULES/ CLOCK DOMAIN | IDLE | STANDBY | HALT |
|-------------------------------------------|---------|---------|----------------------------------------------------|
| SYSCLK | Active | Gated | Gated |
| CPUCLK | Gated | Gated | Gated |
| Clock to modules connected to PERx.SYSCLK | Active | Gated | Gated |
| WDCLK | Active | Active | Gated if CLKSRCCTL1.WDHALTI = 0 |
| PLL | Powered | Powered | Software must power down PLL before entering HALT. |
| INTOSC1 | Powered | Powered | Powered down if CLKSRCCTL1.WDHALTI = 0 |
| INTOSC2 | Powered | Powered | Powered down if CLKSRCCTL1.WDHALTI = 0 |
| Flash ⁽¹⁾ | Powered | Powered | Powered |
| XTAL ⁽²⁾ | Powered | Powered | Powered |

- (1) The Flash module is not powered down by hardware in any LPM. It may be powered down using software if required by the application. For more information, see the Flash and OTP Memory section of the System Control chapter in the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#).
- (2) The XTAL is not powered down by hardware in any LPM. It may be powered down by software setting the XTALCR.OSCOFF bit to 1. This can be done at any time during the application if the XTAL is not required.

6.13.10.2 Low-Power Mode Wake-up Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.13.10.2.1 IDLE Mode Timing Requirements

| | | | MIN | MAX | UNIT |
|---------------|-----------------------------------------|-------------------------|--------------------------------|-----|--------|
| $t_{w(WAKE)}$ | Pulse duration, external wake-up signal | Without input qualifier | $2t_{c(SYSCLK)}$ | | cycles |
| | | With input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |

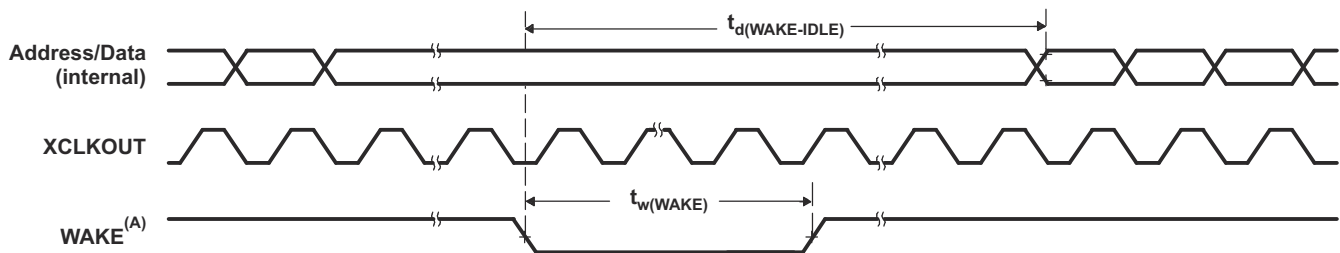
6.13.10.2.2 IDLE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|-----------------------------------------------------------------------------|---------------------------|-------------------------|---------------------------------|--------|
| $t_{d(WAKE-IDLE)}$ | Delay time, external wake signal to program execution resume ⁽¹⁾ | From Flash (active state) | | $40t_{c(SYSCLK)}$ | cycles |
| | | | Without input qualifier | $40t_{c(SYSCLK)}$ | |
| $t_{d(WAKE-IDLE)}$ | Delay time, external wake signal to program execution resume ⁽¹⁾ | From RAM | | $25t_{c(SYSCLK)}$ | cycles |
| | | | Without input qualifier | $25t_{c(SYSCLK)}$ | |
| | | | With input qualifier | $25t_{c(SYSCLK)} + t_{w(WAKE)}$ | |

- (1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.

6.13.10.2.3 IDLE Entry and Exit Timing Diagram



- A. WAKE can be any enabled interrupt, \overline{WDINT} or $XRSn$. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

Figure 6-33. IDLE Entry and Exit Timing Diagram

6.13.10.2.4 STANDBY Mode Timing Requirements

| | | | MIN | MAX | UNIT |
|-------------------|-----------------------------------------|---------------------------------------------------------------|-----------------------------------|-----|--------|
| $t_{w(WAKE-INT)}$ | Pulse duration, external wake-up signal | QUALSTDBY = 0 $2t_{c(OSCCLK)}$ | $3t_{c(OSCCLK)}$ | | cycles |
| | | QUALSTDBY > 0 $(2 + QUALSTDBY)t_{c(OSCCLK)}$ ⁽¹⁾ | $(2 + QUALSTDBY) * t_{c(OSCCLK)}$ | | |

(1) QUALSTDBY is a 6-bit field in the LPMCR register.

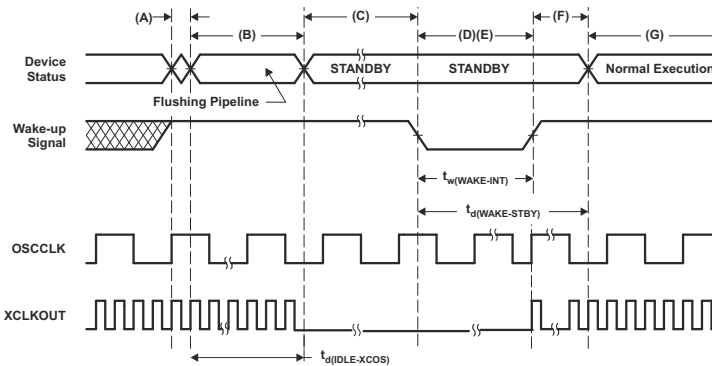
6.13.10.2.5 STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|-----------------------------------------------------------------------------|---------------------------------------------------|---------------------------------------------------|--------|
| $t_{d(IDLE-XCOS)}$ | Delay time, IDLE instruction executed to XCLKOUT stop | | $16t_{c(INTOSC1)}$ | cycles |
| $t_{d(WAKE-STBY)}$ | Delay time, external wake signal to program execution resume ⁽¹⁾ | Wake up from flash (Flash module in active state) | $175t_{c(SYSCLK)} + t_{w(WAKE-INT)}$ | cycles |
| $t_{d(WAKE-STBY)}$ | Delay time, external wake signal to program execution resume ⁽¹⁾ | Wake up from RAM | $3t_{c(OSC)} + 15t_{c(SYSCLK)} + t_{w(WAKE-INT)}$ | cycles |

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.

6.13.10.2.6 STANDBY Entry and Exit Timing Diagram



- A. IDLE instruction is executed to put the device into STANDBY mode.
- B. The LPM block responds to the STANDBY signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
- C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
- D. The external wake-up signal is driven active.
- E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
- F. After a latency period, the STANDBY mode is exited.
- G. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 6-34. STANDBY Entry and Exit Timing Diagram

6.13.10.2.7 HALT Mode Timing Requirements

| | | MIN | MAX | UNIT |
|---------------------------|-----------------------------------------------------------------------|--------------------------------------------|-----|--------|
| $t_{w(\text{WAKE-GPIO})}$ | Pulse duration, GPIO wake-up signal ⁽¹⁾ | $t_{\text{oscst}} + 2t_{c(\text{OSCCLK})}$ | | cycles |
| $t_{w(\text{WAKE-XRS})}$ | Pulse duration, $\overline{\text{XRS}}$ wake-up signal ⁽¹⁾ | $t_{\text{oscst}} + 8t_{c(\text{OSCCLK})}$ | | cycles |

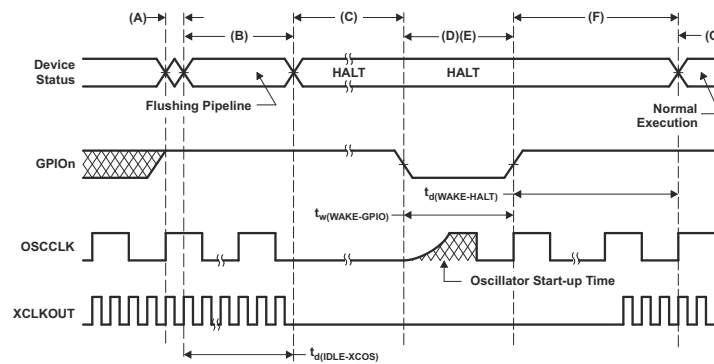
- (1) For applications using X1/X2 for OSCCLK, the user must characterize their specific oscillator start-up time as it is dependent on circuit/layout external to the device. See *Crystal Oscillator (XTAL)* section for more information. For applications using INTOSC1 or INTOSC2 for OSCCLK, see the Internal Oscillators section for t_{oscst} . Oscillator start-up time does not apply to applications using a single-ended crystal on the X1 pin, as it is powered externally to the device.

6.13.10.2.8 HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---------------------------|-----------------------------------------------------------------------|-----|---------------------------|--------|
| $t_{d(\text{IDLE-XCOS})}$ | Delay time, IDLE instruction executed to XCLKOUT stop | | $16t_{c(\text{INTOSC1})}$ | cycles |
| $t_{d(\text{WAKE-HALT})}$ | Delay time, external wake signal end to CPU1 program execution resume | | | cycles |
| | Wake up from Flash - Flash module in active state | | $75t_{c(\text{OSCCLK})}$ | |
| | Wake up from RAM | | $75t_{c(\text{OSCCLK})}$ | |

6.13.10.2.9 HALT Entry and Exit Timing Diagram



- A. IDLE instruction is executed to put the device into HALT mode.
- B. The LPM block responds to the HALT signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
- C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes very little power. It is possible to keep the internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT MODE. This is done by writing 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
- D. When the GPIOin pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wake-up procedure, care should be taken to maintain a low noise environment before entering and during HALT mode.
- E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
- F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after some latency. The HALT mode is now exited.
- G. Normal operation resumes.
- H. The user must relock the PLL upon HALT wakeup to ensure a stable PLL lock.

Figure 6-35. HALT Entry and Exit Timing Diagram

6.14 Analog Peripherals

The analog subsystem module is described in this section.

The analog modules on this device include the Analog-to-Digital Converter (ADC), Temperature Sensor, Comparator Subsystem (CMPSS), and Lite Comparator Subsystem variant (CMPSS_LITE).

The analog subsystem has the following features:

- Flexible voltage references
 - The ADCs are referenced to VREFHI and VSSA pins
 - VREFHI pin voltage can be driven in externally or can be generated by an internal bandgap voltage reference
 - The internal voltage reference range can be selected to be 0 V to 3.3 V or 0 V to 2.5 V
 - The comparator DACs are referenced to VDDA and VSSA
- Flexible pin usage
 - Comparator subsystem inputs and digital inputs (AIOs)/outputs (AGPIOs) are multiplexed with ADC inputs
 - Low comparator DAC (CMPx_DACL) can optionally be brought out to a multiplexed ADC pin for external use (exclusive with use of CMPSS compare functions and only available on some CMPSS instances)
 - Internal connection to V_{REFLO} on all ADCs for offset self-calibration

Figure 6-36 shows the Analog Subsystem Block Diagram for all packages. Figure 6-37 shows the analog group connections. Section 6.14.1 lists the analog pins and internal connections. Section 6.14.2 lists descriptions of analog signals.

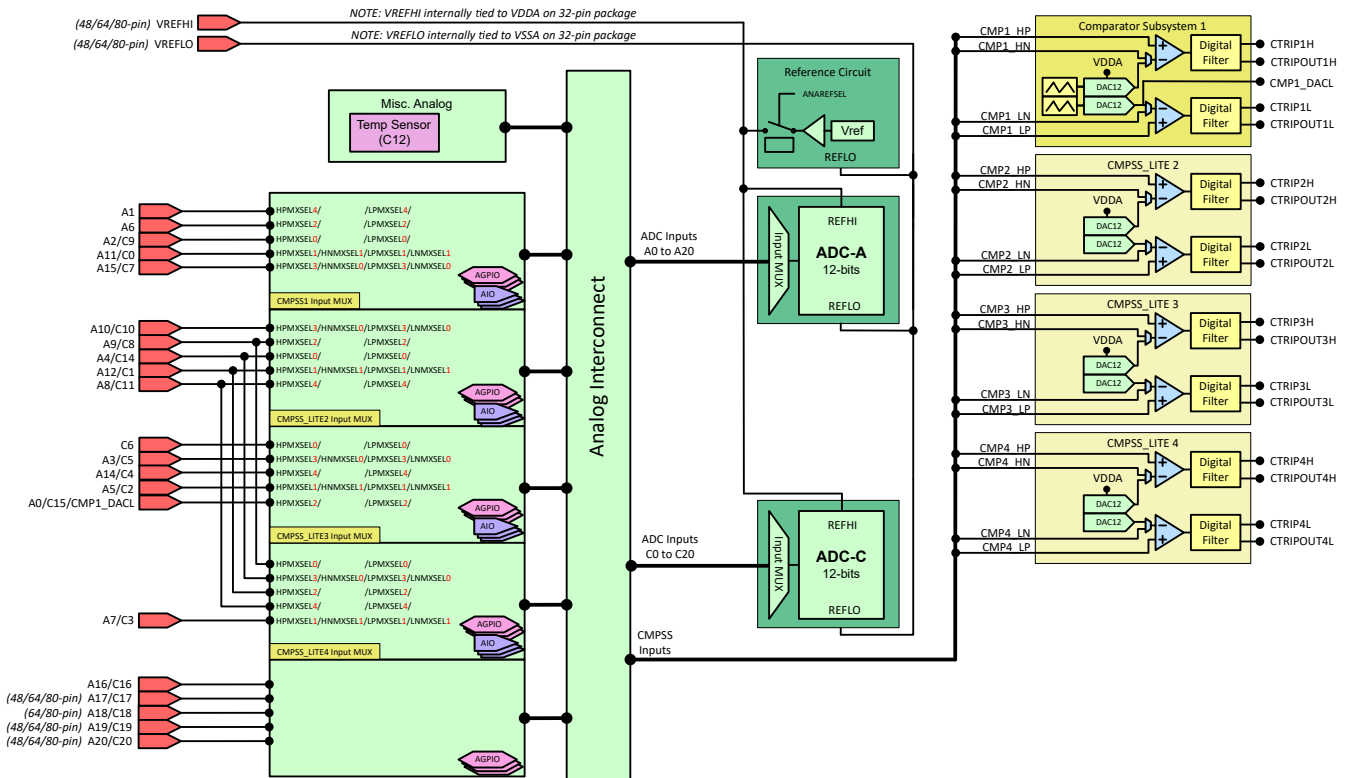
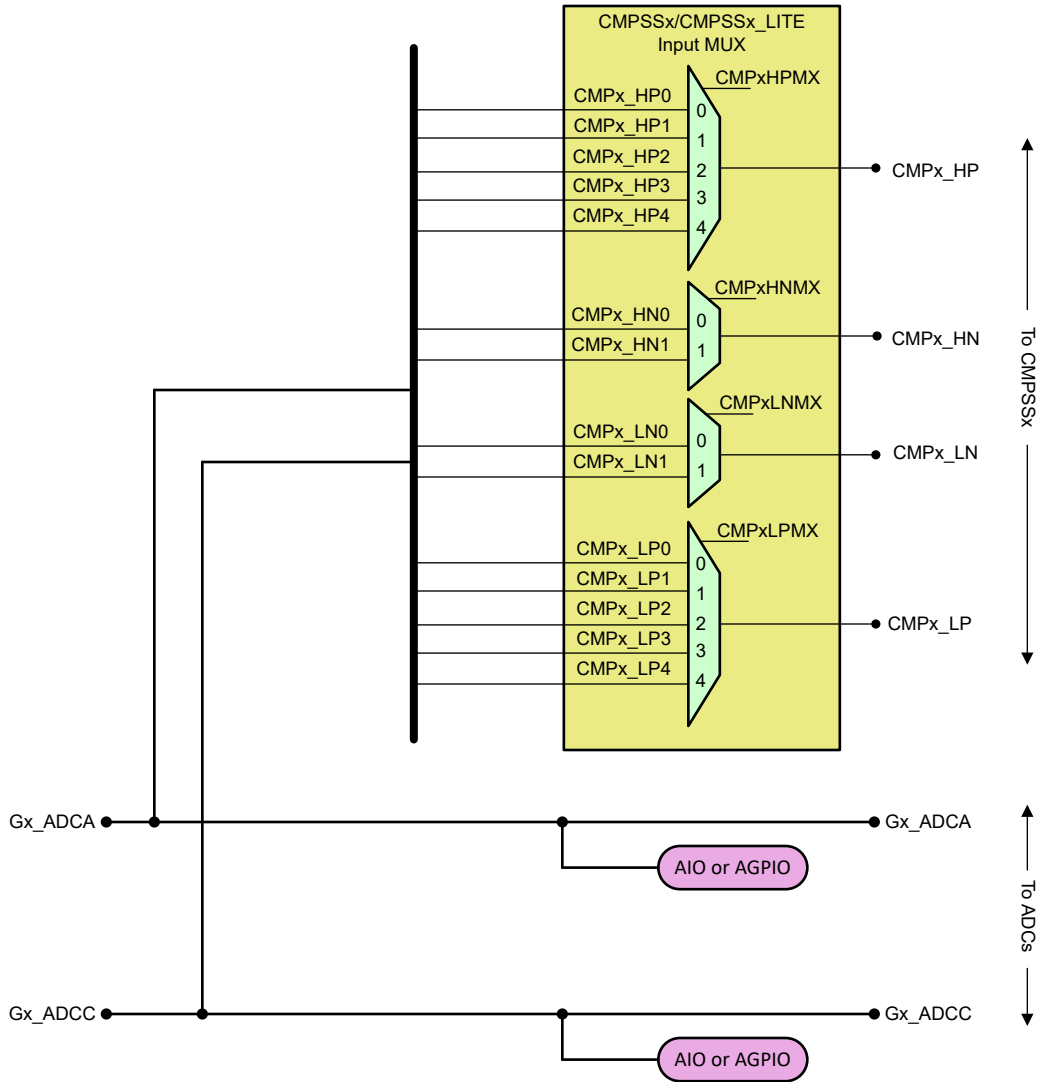


Figure 6-36. Analog Subsystem Block Diagram



Note: AIOs support digital input mode only.

Figure 6-37. Analog Group Connections

6.14.1 Analog Pins and Internal Connections

Table 6-16. Analog Pins and Internal Connections

| Pin Name | Pins/Package | | | | ADC | | DAC | Comparator Subsystem (Mux) | | | | AIO Input/ GPIO |
|----------------------------------|--------------|--------|------------------|-------------------|-----|-----|-----------|--------------------------------------|------------------|--------------------------------------|------------------|------------------------|
| | 80 QFP | 64 QFP | 48 QFP | 32 QFN | A | C | | High Positive | High Negative | Low Positive | Low Negative | |
| VREFHI | 20 | 16 | 12 | .(4) | | | | | | | | |
| VREFLO | 21 | 17 | 13 | .(4) | A13 | C13 | | | | | | |
| Analog Group 1 | | | | | | | | CMP1 | | | | |
| A6 | 10 | 6 | 4 ⁽¹⁾ | 2 ⁽¹⁾ | A6 | - | | CMP1 (HPMXSEL=2) | | CMP1 (LPMXSEL=2) | | GPIO228 ⁽³⁾ |
| A2/C9 | 13 | 9 | 6 | 4 | A2 | C9 | | CMP1 (HPMXSEL=0) | | CMP1 (LPMXSEL=0) | | GPIO224 ⁽³⁾ |
| A15/C7 | 14 | 10 | 7 ⁽¹⁾ | 5 ⁽¹⁾ | A15 | C7 | | CMP1 (HPMXSEL=3) | CMP1 (HNMXSEL=0) | CMP1 (LPMXSEL=3) | CMP1 (LNMXSEL=0) | AIO233 |
| A11/C0 | 16 | 12 | 8 | 6 ⁽¹⁾ | A11 | C0 | | CMP1 (HPMXSEL=1) | CMP1 (HNMXSEL=1) | CMP1 (LPMXSEL=1) | CMP1 (LNMXSEL=1) | AIO237 |
| A1 | 18 | 14 | 10 | 7 ⁽¹⁾ | A1 | - | | CMP1 (HPMXSEL=4) | | CMP1 (LPMXSEL=4) | | AIO232 |
| Analog Group 2 | | | | | | | | CMP2 | | | | |
| A10/C10 | 29 | 25 | 21 | 13 ⁽¹⁾ | A10 | C10 | | CMP2 (HPMXSEL=3) | CMP2 (HNMXSEL=0) | CMP2 (LPMXSEL=3) | CMP2 (LNMXSEL=0) | GPIO230 ⁽³⁾ |
| Analog Group 3 | | | | | | | | CMP3 | | | | |
| C6 | 11 | 7 | 4 ⁽¹⁾ | 2 ⁽¹⁾ | - | C6 | | CMP3 (HPMXSEL=0) | | CMP3 (LPMXSEL=0) | | GPIO226 ⁽³⁾ |
| A3/C5 | 12 | 8 | 5 | 3 | A3 | C5 | | CMP3 (HPMXSEL=3) | CMP3 (HNMXSEL=0) | CMP3 (LPMXSEL=3) | CMP3 (LNMXSEL=0) | GPIO242 ⁽³⁾ |
| A14/C4 | 15 | 11 | 7 ⁽¹⁾ | 5 ⁽¹⁾ | A14 | C4 | | CMP3 (HPMXSEL=4) | | CMP3 (LPMXSEL=4) | | AIO239 |
| A5/C2 | 17 | 13 | 9 | 6 ⁽¹⁾ | A5 | C2 | | CMP3 (HPMXSEL=1) | CMP3 (HNMXSEL=1) | CMP3 (LPMXSEL=1) | CMP3 (LNMXSEL=1) | AIO244 |
| A0/C15/CMP1_DACL | 19 | 15 | 11 | 7 ⁽¹⁾ | A0 | C15 | CMP1_DACL | CMP3 (HPMXSEL=2) | | CMP3 (LPMXSEL=2) | | AIO231 |
| Analog Group 4 | | | | | | | | CMP4 | | | | |
| A7/C3 | 23 | 19 | 15 | 8 ⁽¹⁾ | A7 | C3 | | CMP4 (HPMXSEL=1) | CMP4 (HNMXSEL=1) | CMP4 (LPMXSEL=1) | CMP4 (LNMXSEL=1) | AIO245 |
| Combined Analog Group 2/4 | | | | | | | | CMP2/4 | | | | |
| A12/C1 | 22 | 18 | 14 | 8 ⁽¹⁾ | A12 | C1 | | CMP2 (HPMXSEL=1) CMP4 (HPMXSEL=2) | CMP2 (HNMXSEL=1) | CMP2 (LPMXSEL=1) CMP4 (LPMXSEL=2) | CMP2 (LNMXSEL=1) | AIO238 |
| A8/C11 | 24 | 20 | 16 | 9 | A8 | C11 | | CMP2 (HPMXSEL=4) CMP4 (HPMXSEL=4) | | CMP2 (LPMXSEL=4) CMP4 (LPMXSEL=4) | | AIO241 |
| A4/C14 | 27 | 23 | 19 | 12 | A4 | C14 | | CMP2 (HPMXSEL=0) CMP4 (HPMXSEL=3) | CMP4 (HNMXSEL=0) | CMP2 (LPMXSEL=0) CMP4 (LPMXSEL=3) | CMP4 (LNMXSEL=0) | AIO225 |
| A9/C8 | 28 | 24 | 20 | 13 ⁽¹⁾ | A9 | C8 | | CMP2 (HPMXSEL=2) CMP4 (HPMXSEL=0) | | CMP2 (LPMXSEL=2) CMP4 (LPMXSEL=0) | | GPIO227 ⁽³⁾ |
| Other Analog | | | | | | | | | | | | |
| TempSensor ⁽²⁾ | - | - | - | - | - | C12 | | CMP2 (HPMXSEL=5) | | | | |
| A16/C16 | 4 | 2 | 2 | 32 | A16 | C16 | | | | | | GPIO28 ⁽³⁾ |
| A17/C17 | 33 | 27 | 22 | - | A17 | C17 | | | | | | GPIO20 ⁽³⁾ |
| A18/C18 | 34 | 28 | - | - | A18 | C18 | | | | | | GPIO21 ⁽³⁾ |
| A19/C19 | 35 | 29 | 23 | - | A19 | C19 | | | | | | GPIO13 ⁽³⁾ |

Table 6-16. Analog Pins and Internal Connections (continued)

| Pin Name | Pins/Package | | | | ADC | | DAC | Comparator Subsystem (Mux) | | | | AIO Input/ GPIO |
|----------|--------------|--------|--------|--------|-----|-----|-----|----------------------------|---------------|--------------|--------------|-----------------------|
| | 80 QFP | 64 QFP | 48 QFP | 32 QFN | A | C | | High Positive | High Negative | Low Positive | Low Negative | |
| A20/C20 | 36 | 30 | 24 | - | A20 | C20 | | | | | | GPIO12 ⁽³⁾ |

- (1) Signal is bonded together with another signal as a single pin on this package.
- (2) Internal connection only; does not come to a device pin.
- (3) The GPIOs on these analog pins support full digital input and output functionality and are referred to as AGPIOs. By default, the AGPIOs are unconnected; that is, the analog and digital functions are both disabled. For configuration details, see the *Digital Inputs and Outputs on ADC Pins (AGPIOs)* section.
- (4) On 32 RHB package, VREFHI is internally connected to VDDA and VREFLO is internally connected to VSSA.

6.14.2 Analog Signal Descriptions

Table 6-17. Analog Signal Descriptions

| Signal Name | Description |
|-------------|-------------------------------------------------------------------------|
| AIOx | Digital input on ADC pin |
| Ax | ADC A Input |
| Cx | ADC C Input |
| CMPx_HNy | Comparator subsystem high comparator negative input |
| CMPx_HPy | Comparator subsystem high comparator positive input |
| CMPx_LNy | Comparator subsystem low comparator negative input |
| CMPx_LPy | Comparator subsystem low comparator positive input |
| CMPx_DACL | DAC output from the lower CMPSS DAC (can be brought to an external pin) |
| TempSensor | Internal temperature sensor |

6.14.3 Analog-to-Digital Converter (ADC)

The ADC module described here is a successive approximation (SAR) style ADC with resolution of 12 bits. This section refers to the analog circuits of the converter as the “core,” and includes the channel-select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The digital circuits of the converter are referred to as the “wrapper” and include logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module consists of a single sample-and-hold (S/H) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is start-of-conversion (SOC)-based (see the SOC Principle of Operation section of the Analog-to-Digital Converter (ADC) chapter in the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#)).

Each ADC has the following features:

- Resolution of 12 bits
- Ratiometric external reference set by VREFHI/VREFLO
- Selectable internal reference of 2.5 V or 3.3 V
- Single-ended signal mode
- Input multiplexer with up to 21 channels
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
 - Software immediate start
 - All ePWMs: ADCSOC A or B
 - GPIO XINT2
 - CPU Timers 0/1/2
 - ADCINT1/2
- Four flexible PIE interrupts
- Burst-mode triggering option
- Four post-processing blocks, each with:
 - Saturating offset calibration
 - Error from setpoint calculation
 - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
 - Trigger-to-sample delay capture

Note

Not every channel can be pinned out from all ADCs. See the Pin Configuration and Functions section to determine which channels are available.

The block diagram for the ADC core and ADC wrapper are shown in Figure 6-38.

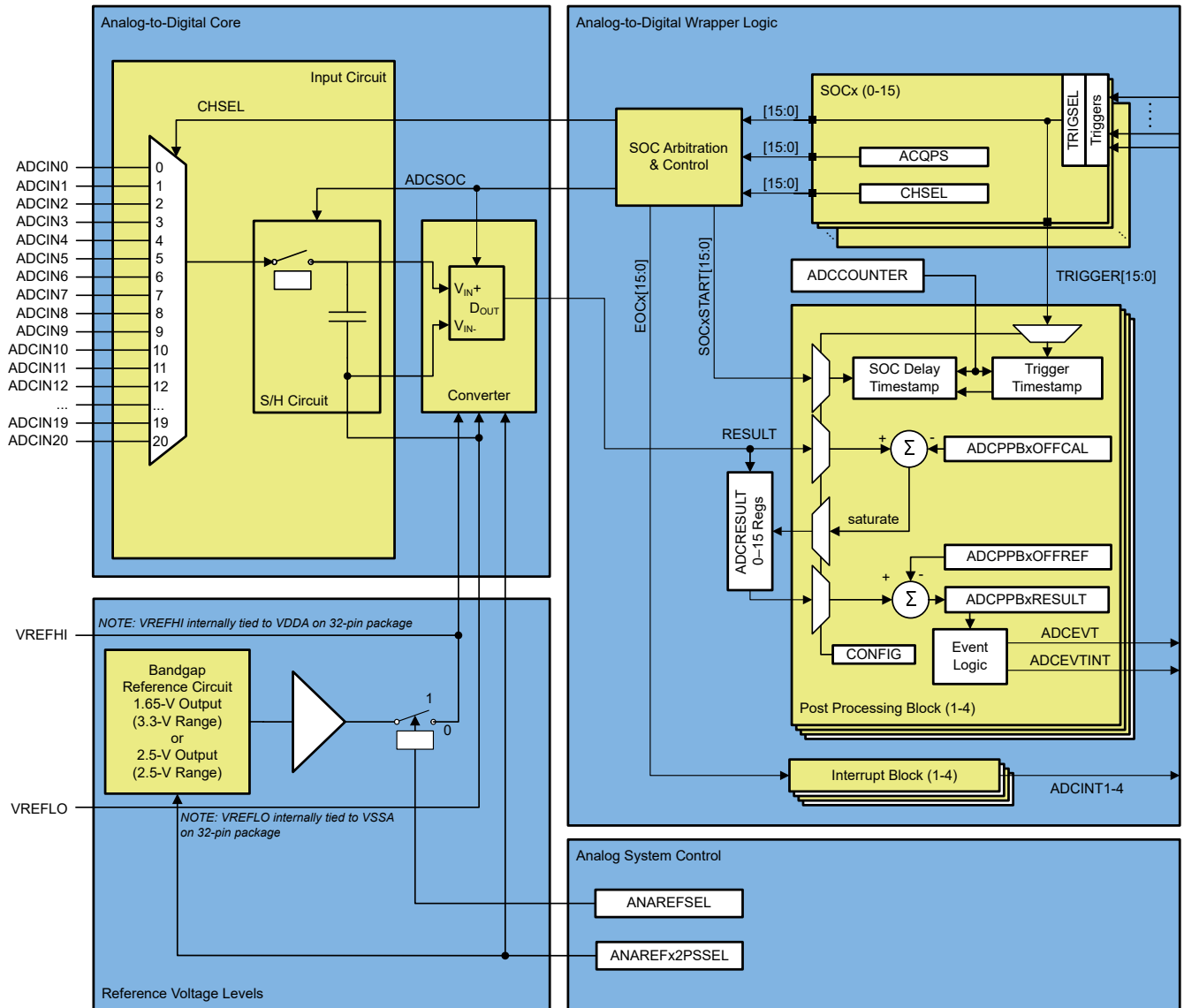


Figure 6-38. ADC Module Block Diagram

6.14.3.1 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are globally controlled per ADC module. Table 6-18 summarizes the basic ADC options and their level of configurability.

Table 6-18. ADC Options and Configuration Levels

| OPTIONS | CONFIGURABILITY |
|-----------------------------|--------------------------------------------------|
| Clock | Per module ⁽¹⁾ |
| Resolution | Not configurable (12-bit resolution only) |
| Signal mode | Not configurable (single-ended signal mode only) |
| Reference voltage source | Either external or internal for all modules |
| Trigger source | Per SOC ⁽¹⁾ |
| Converted channel | Per SOC |
| Acquisition window duration | Per SOC ⁽¹⁾ |
| EOC location | Per module |
| Burst mode | Per module ⁽¹⁾ |

(1) Writing these values differently to different ADC modules could cause the ADCs to operate asynchronously. For guidance on when the ADCs are operating synchronously or asynchronously, see the Ensuring Synchronous Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F280015x Real-Time Microcontrollers Technical Reference Manual*.

6.14.3.1.1 Signal Mode

The ADC supports single-ended signaling. The input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO.

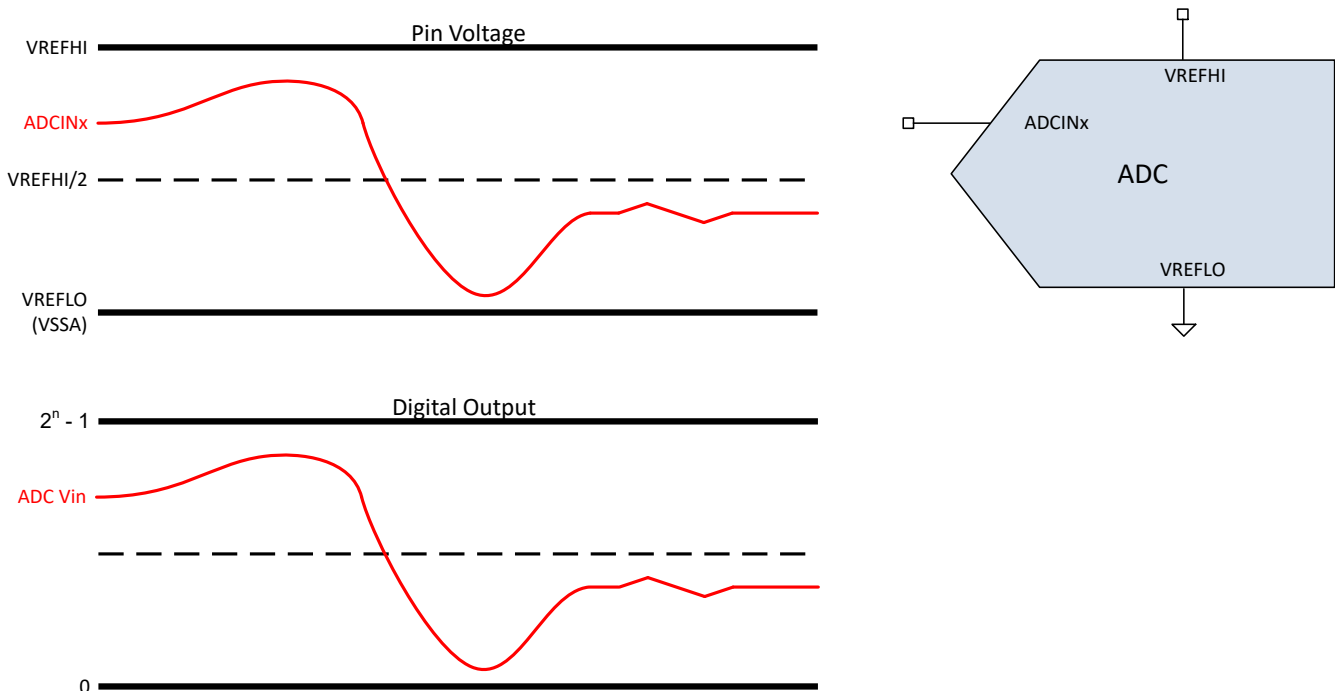


Figure 6-39. Single-ended Signaling Mode

6.14.3.2 ADC Electrical Data and Timing

Note

The ADC inputs should be kept below $V_{DDA} + 0.3$ V. If an ADC input goes above this level, ADC disturbances to other channels may occur by two mechanisms:

- ADC input overvoltage will overdrive the CMPSS mux, disturbing all other channels which share a common CMPSS mux. This disturbance will be continuous regardless of if the overvoltage input is sampled by the ADC
- When the ADC samples the overvoltage ADC input, VREFHI will be pulled up to a higher level. This will disturb subsequent ADC conversions on any channel until the V_{REF} stabilizes

Note

The VREFHI pin must be kept below $V_{DDA} + 0.3$ V to ensure proper functional operation. If the VREFHI pin exceeds this level, a blocking circuit may activate, and the internal value of VREFHI may float to 0 V internally, giving improper ADC conversion.

6.14.3.2.1 ADC Operating Conditions

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------------------------------------------|-------------------------------------------------|-------------|------------|--------------------------|------|
| ADCCLK (derived from PERx.SYSCLK) | F2800157, F2800155, F2800153 | 5 | | 60 | MHz |
| | F2800156, F2800154, F2800152 | 5 | | 50 | |
| Sample rate | 120-MHz SYSCLK F2800157, F2800155, F2800153 | | | 4 | MSPS |
| | 100-MHz SYSCLK F2800156, F2800154, F2800152 | | | 3.45 | |
| Sample window duration (set by ACQPS and PERx.SYSCLK) ⁽¹⁾ | With 50 Ω or less R_s , Pin with AIO | 75 | | | ns |
| | With 50 Ω or less R_s , Pin with AGPIO | 90 | | | |
| VREFHI | External Reference | 2.4 | 2.5 or 3.0 | V_{DDA} | V |
| VREFHI ⁽²⁾ | Internal Reference = 3.3V Range | | 1.65 | | V |
| | Internal Reference = 2.5V Range | | 2.5 | | V |
| VREFHI | Package = 32QFN | V_{DDA} | V_{DDA} | V_{DDA} | V |
| VREFLO | | V_{SSA} | | V_{SSA} | V |
| VREFHI - VREFLO | | 2.4 | | V_{DDA} | V |
| Conversion range | Internal Reference = 3.3 V Range | 0 | | 3.3 | V |
| | Internal Reference = 2.5 V Range | 0 | | 2.5 | |
| | External Reference | V_{REFLO} | | V_{REFHI} | |
| | Package = 32QFN | 0 | | V_{DDA} ⁽³⁾ | |

- (1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
- (2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.
- (3) On 32QFN package, VREFHI is internally tied to V_{DDA} and VREFLO is internally tied to V_{SSA} . Internal reference mode is not supported on 32QFN package.

6.14.3.2.2 ADC Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------------------|------------------------------------------------------------------------------|------|---------------|------|---------|
| General | | | | | |
| ADCCLK Conversion Cycles | 120-MHz SYSCLK | 10.1 | | 11 | ADCCLKs |
| Power Up Time | External Reference mode | | | 500 | μs |
| | Internal Reference mode | | | 5000 | μs |
| | Internal Reference mode, when switching between 2.5-V range and 3.3-V range. | | | 5000 | μs |
| VREFHI input current ⁽¹⁾ | | | 130 | | μA |
| Internal Reference Capacitor Value ⁽²⁾ | | 2.2 | | | μF |
| External Reference Capacitor Value ⁽²⁾ | | 2.2 | | | μF |
| DC Characteristics | | | | | |
| Gain Error | Internal reference | -45 | | 45 | LSB |
| | External reference | -5 | ±3 | 5 | |
| Offset Error | | -5 | ±2 | 5 | LSB |
| Channel-to-Channel Gain Error ⁽⁴⁾ | | | 2 | | LSB |
| Channel-to-Channel Offset Error ⁽⁴⁾ | | | 2 | | LSB |
| ADC-to-ADC Gain Error ⁽⁵⁾ | Identical VREFHI and VREFLO for all ADCs | | 4 | | LSB |
| ADC-to-ADC Offset Error ⁽⁵⁾ | Identical VREFHI and VREFLO for all ADCs | | 2 | | LSB |
| DNL Error | | >-1 | ±0.5 | 1 | LSB |
| INL Error | | -2 | ±1.0 | 2 | LSB |
| ADC-to-ADC Isolation | VREFHI = 2.5 V, synchronous ADCs | -1 | | 1 | LSBs |
| AC Characteristics | | | | | |
| SNR ⁽³⁾ | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 | | 68.8 | | dB |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC | | 60.1 | | |
| THD ⁽³⁾ | VREFHI = 2.5 V, fin = 100 kHz | | -80.6 | | dB |
| SFDR ⁽³⁾ | VREFHI = 2.5 V, fin = 100 kHz | | 79.2 | | dB |
| SINAD ⁽³⁾ | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 | | 68.5 | | dB |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC | | 60.0 | | |
| ENOB ⁽³⁾ | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC | | 11.0 | | bits |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs | | 11.0 | | |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs | | Not Supported | | |

6.14.3.2.2 ADC Characteristics (continued)

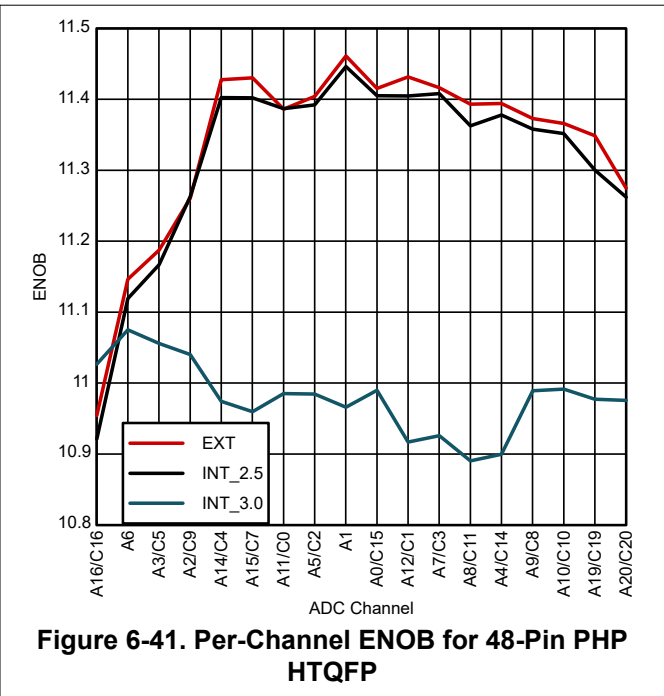
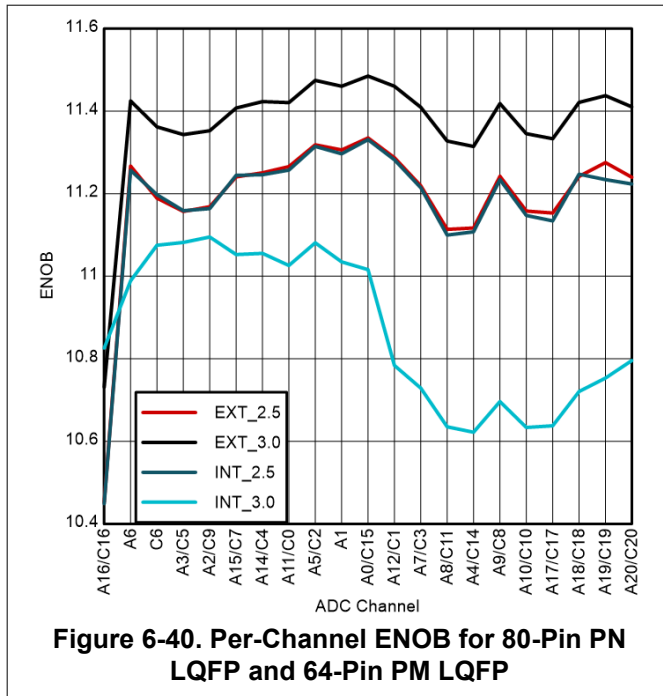
over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-----------------------------------------------------|-----|-----|-----|------|
| PSRR | VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz | | 60 | | dB |
| | VDD = 1.2-V DC + 100 mV DC up to Sine at 300 kHz | | 57 | | |
| | VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz | | 60 | | |
| | VDDA = 3.3-V DC + 200 mV Sine at 900 kHz | | 57 | | |

- (1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
- (2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
- (3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
- (4) Variation across all channels belonging to the same ADC module.
- (5) Worst case variation compared to other ADC modules.

6.14.3.2.3 ADC Performance Per Pin

ADC performance of each pin is affected by adjacent pins. The following plots provide details on how these pins differ in performance.



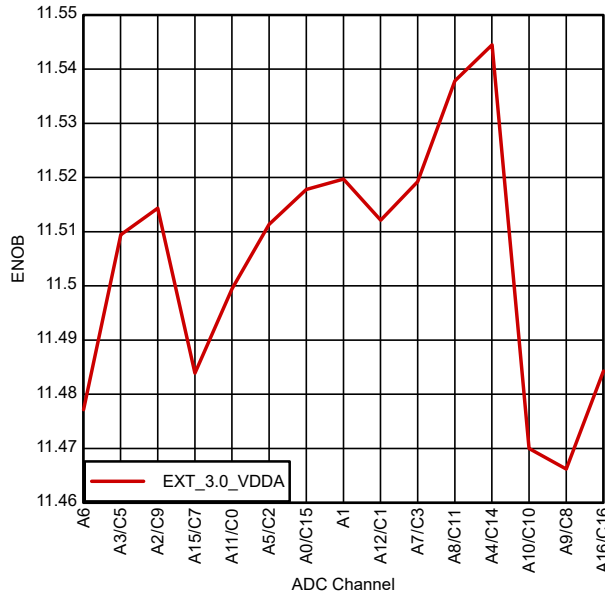


Figure 6-42. Per-Channel ENOB for 32-Pin RHB VQFN

6.14.3.2.4 ADC Input Model

The ADC input characteristics are given by Table 6-19 and Figure 6-43.

Table 6-19. Input Model Parameters

| | DESCRIPTION | REFERENCE MODE | VALUE |
|----------|-----------------------------|----------------------------------------------|--------------------------------------------------------|
| C_p | Parasitic input capacitance | All | See Table 6-20, Table 6-21, Table 6-22, and Table 6-23 |
| R_{on} | Sampling switch resistance | External Reference, 2.5-V Internal Reference | 500 Ω |
| | | 3.3-V Internal Reference | 860 Ω |
| C_h | Sampling capacitor | External Reference, 2.5-V Internal Reference | 12.5 pF |
| | | 3.3-V Internal Reference | 7.5 pF |
| R_s | Nominal source impedance | All | 50 Ω |

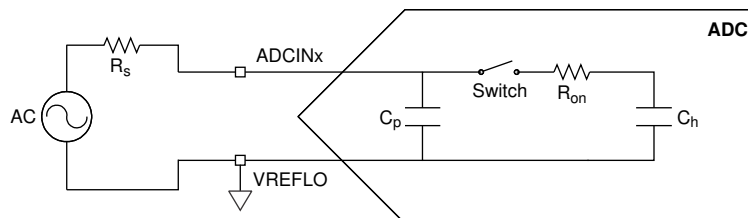


Figure 6-43. Input Model

This input model should be used with actual signal source impedance to determine the acquisition window duration. For more information, see the Choosing an Acquisition Window Duration section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F280015x Real-Time Microcontrollers Technical Reference Manual*. For recommendations on improving ADC input circuits, see the *ADC Input Circuit Evaluation for C2000 MCUs* Application Report.

Table 6-20. Per-Channel Parasitic Capacitance for 80-Pin PN LQFP

| ADC CHANNEL | C _p (pF) | |
|------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0/C15/CMP1_DACL | 7.7 | 10.2 |
| A1 | 1.6 | 4.1 |
| A2/C9 | 1.5 | 4 |
| A3/C5 | 1.8 | 4.3 |
| A4/C14 | 2.4 | 4.9 |
| A5/C2 | 2 | 4.5 |
| A6 | 1.4 | 3.9 |
| A7/C3 | 1.9 | 4.4 |
| A8/C11 | 2.2 | 4.7 |
| A9/C8 | 2.3 | 4.8 |
| A10/C10 | 2 | 4.5 |
| A11/C0 | 2.4 | 4.9 |
| A12/C1 | 3.2 | 5.7 |
| A14/C4/ADCINCAL | 2.4 | 4.9 |
| A15/C7 | 3 | 5.5 |
| A16/C16 | 2.4 | 4.9 |
| A17/C17 | 2.7 | 5.2 |
| A18/C18 | 2.7 | 5.2 |
| A19/C19 | 2.7 | 5.2 |
| A20/C20 | 2.7 | 5.2 |
| C6 | 1.7 | 4.2 |

Table 6-21. Per-Channel Parasitic Capacitance for 64-Pin PM LQFP

| ADC CHANNEL | C _p (pF) | |
|------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0/C15/CMP1_DACL | 7.7 | 10.2 |
| A1 | 1.6 | 4.1 |
| A2/C9 | 1.5 | 4 |
| A3/C5 | 1.8 | 4.3 |
| A4/C14 | 2.4 | 4.9 |
| A5/C2 | 2 | 4.5 |
| A6 | 1.4 | 3.9 |
| A7/C3 | 1.9 | 4.4 |
| A8/C11 | 2.2 | 4.7 |
| A9/C8 | 2.3 | 4.8 |
| A10/C10 | 2 | 4.5 |
| A11/C0 | 2.4 | 4.9 |
| A12/C1 | 3.2 | 5.7 |
| A14/C4/ADCINCAL | 2.4 | 4.9 |
| A15/C7 | 3 | 5.5 |
| A16/C16 | 2.4 | 4.9 |
| A17/C17 | 2.7 | 5.2 |
| A18/C18 | 2.7 | 5.2 |
| A19/C19 | 2.7 | 5.2 |
| A20/C20 | 2.7 | 5.2 |

Table 6-21. Per-Channel Parasitic Capacitance for 64-Pin PM LQFP (continued)

| ADC CHANNEL | C _p (pF) | |
|-------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| C6 | 1.7 | 4.2 |

Table 6-22. Per-Channel Parasitic Capacitance for 48-Pin PHP HTQFP

| ADC CHANNEL | C _p (pF) | |
|------------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0/C15/CMP1_DACL | 7.7 | 10.2 |
| A1 | 1.6 | 4.1 |
| A2/C9 | 1.5 | 4 |
| A3/C5 | 1.8 | 4.3 |
| A4/C14 | 2.4 | 4.9 |
| A5/C2 | 2 | 4.5 |
| A6/C6 | 3.1 | 8.1 |
| A7/C3 | 1.9 | 4.4 |
| A8/C11 | 2.2 | 4.7 |
| A9/C8 | 2.3 | 4.8 |
| A10/C10 | 2 | 4.5 |
| A11/C0 | 2.4 | 4.9 |
| A12/C1 | 3.2 | 5.7 |
| A14/A15/C4/C7/ADCINCAL | 5.4 | 10.4 |
| A16/C16 | 2.4 | 4.9 |
| A17/C17 | 2.7 | 5.2 |
| A19/C19 | 2.7 | 5.2 |
| A20/C20 | 2.7 | 5.2 |

Table 6-23. Per-Channel Parasitic Capacitance for 32-Pin RHB VQFN

| ADC CHANNEL | C _p (pF) | |
|------------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0/A1/C15/CMP1_DACL | 9.3 | 14.3 |
| A2/C9 | 1.5 | 4 |
| A3/C5 | 1.8 | 4.3 |
| A4/C14 | 2.4 | 4.9 |
| A5/C2/A11/C0 | 4.4 | 9.4 |
| A6/C6 | 3.1 | 8.1 |
| A7/C3/A12/C1 | 5.1 | 10.1 |
| A8/C11 | 2.2 | 4.7 |
| A9/C8/A10/C10 | 4.3 | 9.3 |
| A14/A15/C4/C7/ADCINCAL | 5.4 | 10.4 |
| A16/C16 | 2.4 | 4.9 |

6.14.3.2.5 ADC Timing Diagrams

Figure 6-44 shows the ADC conversion timings for two SOC0s given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOC0s are converting or pending when the trigger occurs.
- The round-robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the PIE module).

Table 6-24 lists the descriptions of the ADC timing parameters. Table 6-25 lists the ADC timings.

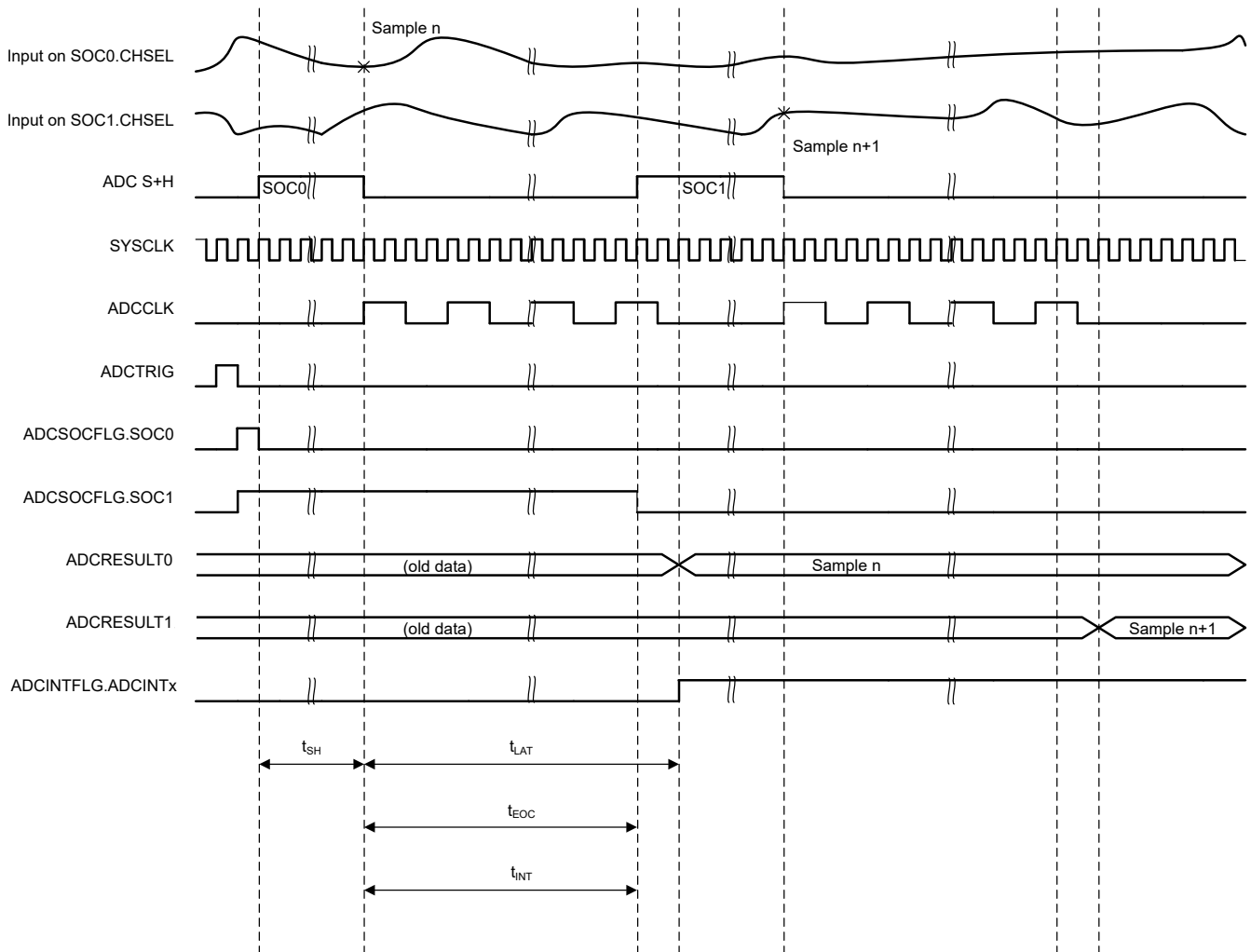


Figure 6-44. ADC Timings

Table 6-24. ADC Timing Parameter Descriptions

| PARAMETER | DESCRIPTION |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| t_{SH} | The duration of the S+H window. At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by $(ACQPS + 1)$ SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} is not necessarily the same for different SOC0s. Note: The value on the S+H capacitor is captured approximately 5 ns before the end of the S+H window regardless of device clock settings. |
| t_{LAT} | The time from the end of the S+H window until the ADC results latch in the ADCRESULTx register. If the ADCRESULTx register is read before this time, the previous conversion results are returned. |

Table 6-24. ADC Timing Parameter Descriptions (continued)

| PARAMETER | DESCRIPTION |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| t_{EOC} | The time from the end of the S+H window until the S+H window for the next ADC conversion can begin. The subsequent sample can start before the conversion results are latched. |
| t_{INT} | <p>The time from the end of the S+H window until an ADCINT flag is set (if configured).</p> <p>If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} coincides with the end of conversion (EOC) signal.</p> <p>If the INTPULSEPOS bit is 0, t_{INT} coincides with the end of the S+H window. If t_{INT} triggers a read of the ADC result register (by triggering an ISR that reads the result), care must be taken to make sure the read occurs after the results latch (otherwise, the previous results are read).</p> <p>If the INTPULSEPOS bit is 0, and the OFFSET field in the ADCINTCYCLE register is not 0, then there is a delay of OFFSET SYSCLK cycles before the ADCINT flag is set. This delay can be used to enter the ISR exactly when the sample is ready.</p> |

Table 6-25. ADC Timings in 12-bit Mode

| ADCCLK Prescale | | SYSCLK Cycles | | | |
|----------------------|----------------|---------------|-----------|-------------------------------------|---------------------|
| ADCCTL2. PRESCALE | Prescale Ratio | t_{EOC} | t_{LAT} | t_{INT} (Early) ⁽¹⁾ | t_{INT} (Late) |
| 0 | 1 | 11 | 13 | 0 | 11 |
| 2 | 2 | 21 | 23 | 0 | 21 |
| 4 | 3 | 31 | 34 | 0 | 31 |
| 6 | 4 | 41 | 44 | 0 | 41 |
| 8 | 5 | 51 | 55 | 0 | 51 |
| 10 | 6 | 61 | 65 | 0 | 61 |
| 12 | 7 | 71 | 76 | 0 | 71 |
| 14 | 8 | 81 | 86 | 0 | 81 |

- (1) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

6.14.4 Temperature Sensor

6.14.4.1 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time in the Temperature Sensor Characteristics table.

6.14.4.1.1 Temperature Sensor Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|----------------------------------------------------------------|-------------------------------------|-----|-----|-----|------|
| T _{acc} | Temperature Accuracy | Internal reference (-40°C to 30°C) | -15 | ±2 | 15 | °C |
| | | Internal reference (30°C to 85°C) | -9 | ±2 | 7 | °C |
| | | Internal reference (85°C to 125°C) | -5 | ±2 | 8 | °C |
| | | Internal reference (125°C to 140°C) | -6 | ±2 | 12 | °C |
| | | Internal reference (140°C to 155°C) | -16 | ±2 | 16 | °C |
| | | External reference (-40°C to 30°C) | -8 | ±2 | 10 | °C |
| | | External reference (30°C to 140°C) | -5 | ±2 | 8 | °C |
| | | External reference (140°C to 155°C) | -5 | ±2 | 8 | °C |
| t _{startup} | Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor) | | | 500 | | µs |
| t _{acq} | ADC acquisition time | | | 450 | | ns |

6.14.5 Comparator Subsystem (CMPSS)

The Comparator Subsystem (CMPSS) consists of analog comparators and supporting circuits that are useful for power applications such as peak current mode control, switched-mode power supply, power factor correction, voltage trip monitoring, and so forth.

This device contains two variants of the CMPSS module: CMPSS and CMPSS_LITE. These modules share a common architecture, but some features are supported only by the full CMPSS variant and not the CMPSS_LITE variant.

The comparator subsystem is built around a number of modules. Each subsystem contains two comparators, two reference 12-bit DACs (CMPSS_LITE instances are 9.5-bit effective reference DACs), and two digital filters. The subsystem also includes two ramp generators (full CMPSS modules only; not supported by CMPSS_LITE instances). Comparators are denoted "H" or "L" within each module where "H" and "L" represent high and low, respectively. Each comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator is driven from an external pin (see the *Analog Subsystem* chapter of the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#) for mux options available to the CMPSS). The negative input can be driven by an external pin or by the programmable reference 12-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required. Two ramp generator circuits are optionally available to control the reference 12-bit DAC values for the high and low comparator in the subsystem (full CMPSS modules only; not supported by CMPSS_LITE instances).

Each CMPSS includes:

- Two analog comparators
- Two programmable reference 12-bit DACs (9.5-bit effective DACs on CMPSS_LITE instances)
- Dual ramp generators (full CMPSS only; not available on CMPSS_LITE instances)
- Two digital filters with max filter clock prescale of 2^{24}
- Ability to synchronize submodules with EPWMSYNCPER
- Ability to extend clear signal with EPWMBLANK
- Ability to synchronize output with SYSCLK
- Ability to latch output
- Ability to invert output
- Option to use hysteresis on the input
- Option for negative input of comparator to be driven by an external signal or by the reference DAC
- Option to use the low comparator DAC output, CMPx_DACL, on an external pin (select instances only, mutually exclusive with use of compare functionality)
- External connection to CMPSS filters
- Wake-up from standby and halt LPM (Low Power Modes) triggered by CMPSS trip outputs

6.14.5.1 CMPSS Module Variants

This device contains two different variants of the CMPSS module: CMPSS (full module) and the CMPSS_LITE (reduced functionality and performance). The differences in features between the two variants are summarized in [Table 6-26](#).

Table 6-26. CMPSS and CMPSS_LITE Feature Comparison

| FEATURE | CMPSS | CMPSS_LITE |
|--------------------------------|------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|
| High and low comparators | Yes | Yes |
| Dual 12-bit reference DACs | Yes | Yes (9.5-bit effective) |
| DAC ramp generation | Yes | No |
| Low DAC output on external pin | Yes (Some instances) | No |
| Digital filters | Yes | Yes |
| Performance | Full performance (see the CMPSS Comparator Electrical Characteristics table) | Some reduced performance (see the CMPSS_LITE Comparator Electrical Characteristics table) |

6.14.5.2 CMPx_DACL

Some CMPSS module instances have support for DAC output buffered to a pin. This CMPx_DACL output from the CMPSS module uses the low-side DAC of the CMPSS module specified. When using DAC output from a CMPSS instance, all other CMPSS module features for that instance are unavailable.

For CMPx_DACL instances available for a particular device, please see the DAC column of the *Analog Pins and Internal Connections* table.

See the *Buffered Output from CMPx_DACL Electrical Characteristics* section for DAC output capabilities.

6.14.5.3 CMPSS Connectivity Diagram

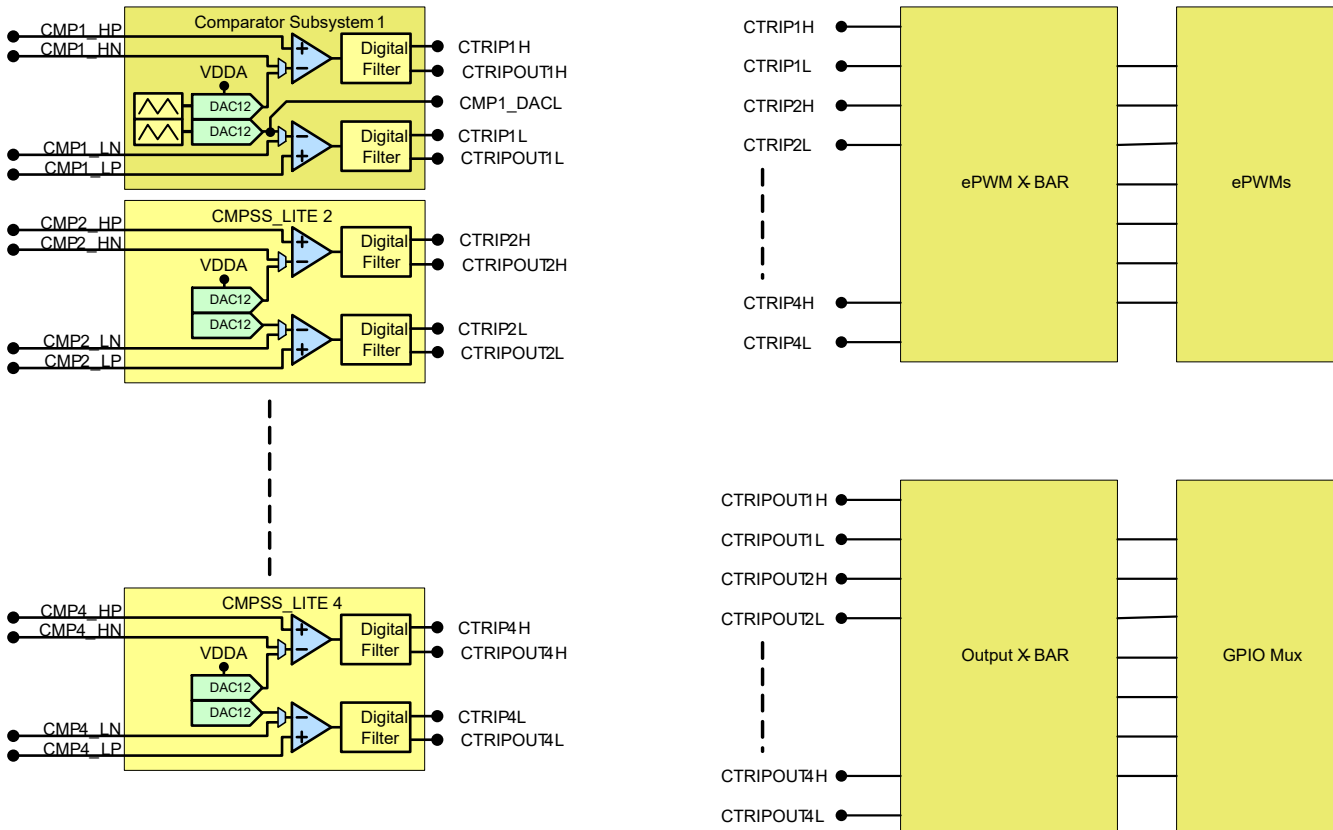


Figure 6-45. CMPSS Connectivity

6.14.5.4 Block Diagrams

The block diagram for the CMPSS is shown in Figure 6-46. The block diagram for the CMPSS_LITE is shown in Figure 6-47.

- CTRIPx(x= "H" or "L") signals are connected to the ePWM X-BAR for ePWM trip response. See the *Enhanced Pulse Width Modulator (ePWM)* chapter of the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#) for more details on the ePWM X-BAR mux configuration.
- CTRIPxOUTx(x= "H" or "L") signals are connected to the Output X-BAR for external signaling. See the *General-Purpose Input/Output (GPIO)* chapter of the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#) for more details on the Output X-BAR mux configuration.

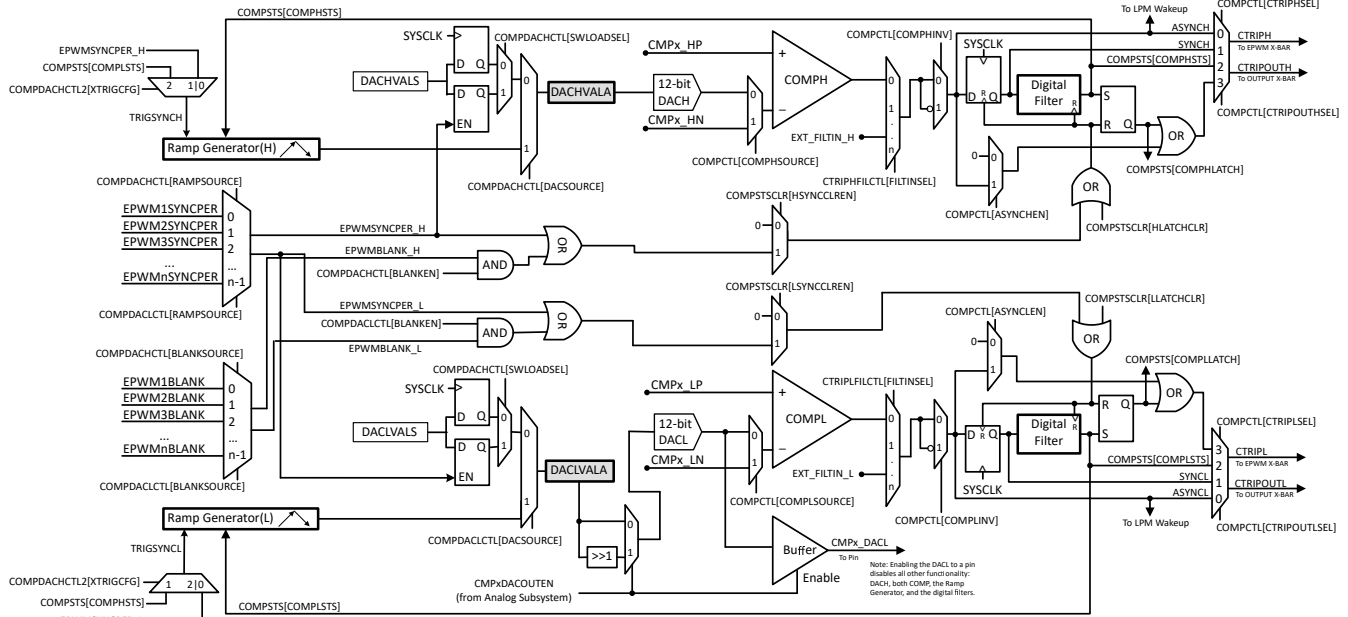


Figure 6-46. CMPSS Module Block Diagram

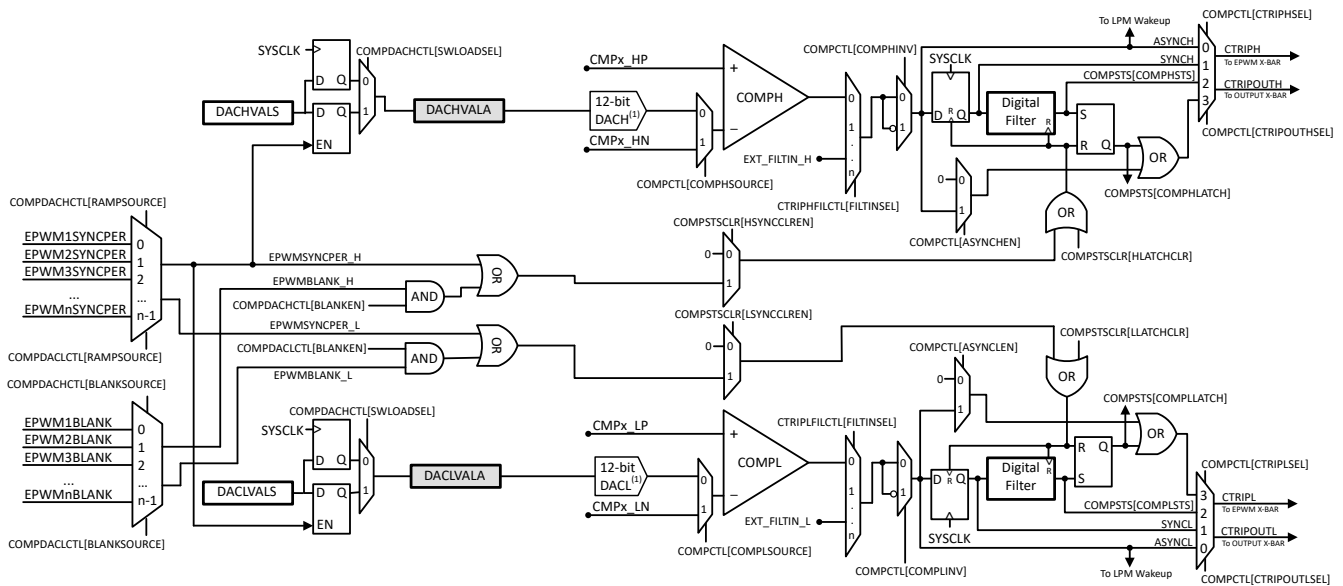


Figure 6-47. CMPSS_LITE Module Block Diagram

Each reference 12-bit DAC can be configured to drive a reference voltage into the negative input of the respective comparator. Some CMPSS instances also allow the low DAC output to be routed to a pin to act as an external DAC. In this case, all other CMPSS module functionality is not useable, including the high DAC, both comparators, ramp generation, and the digital filters. The reference 12-bit DAC is illustrated in [Figure 6-48](#).

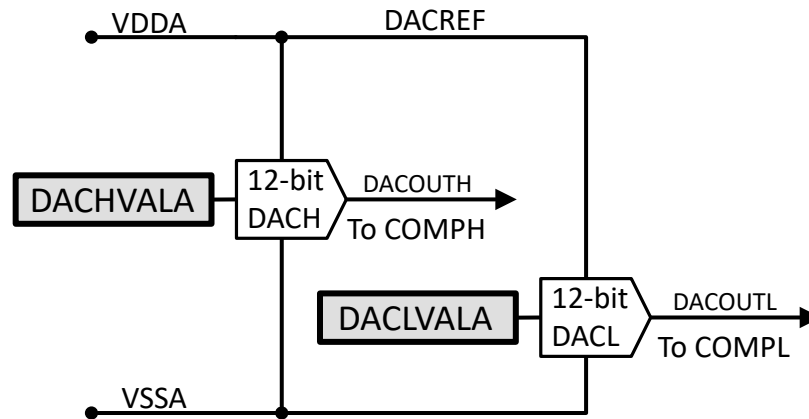


Figure 6-48. Reference DAC Block Diagram

6.14.5.5 CMPSS Electrical Data and Timing

6.14.5.5.1 CMPSS Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------------------------------------------------------------|------------------------------|----------------------------------------------|-----|-----|------|------|
| TPU | Power-up time | | | | 500 | μs |
| Comparator input (CMPINxx) range | | | 0 | | VDDA | V |
| Input referred offset error | | Low common mode, inverting input set to 50mV | -20 | | 20 | mV |
| Hysteresis ⁽¹⁾ | 1x | | 4 | 12 | 20 | LSB |
| | 2x | | 17 | 24 | 33 | |
| | 3x | | 25 | 36 | 50 | |
| | 4x | | 30 | 48 | 67 | |
| Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR) | | Step response | | 21 | 60 | ns |
| | | Ramp response (1.65V/μs) | | 26 | | |
| | | Ramp response (8.25mV/μs) | | 30 | | |
| PSRR | Power Supply Rejection Ratio | Up to 250 kHz | | 46 | | dB |
| CMRR | Common Mode Rejection Ratio | | 40 | | | dB |

(1) The CMPSS DAC is used as the reference to determine how much hysteresis to apply. Therefore, hysteresis will scale with the CMPSS DAC reference voltage. Hysteresis is available for all comparator input source configurations.

6.14.5.5.2 CMPSS_LITE Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------------------------------------------------------------|------------------------------|------------------------------------------------------|-----|-----|------|------|
| TPU | Power-up time | Bandgap Not Enabled | | | 500 | μs |
| Comparator input (CMPINxx) range | | | 0 | | VDDA | V |
| Input referred offset error | | Via AIO/AGPIO, Input common mode = 5% to 95% of VDDA | -20 | | 20 | mV |
| Hysteresis ⁽¹⁾ | 1x | | 2 | 10 | 19 | mV |
| | 2x | | 8 | 20 | 34 | |
| | 3x | | 15 | 30 | 51 | |
| | 4x | | 20 | 41 | 70 | |
| | 5x | | 26 | 52 | 88 | |
| | 6x | | 32 | 64 | 109 | |
| | 7x | | 38 | 77 | 131 | |
| Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR) | | Step response | | 21 | 40 | ns |
| | | Ramp response (1.65V/μs) | | 26 | | |
| | | Ramp response (8.25mV/μs) | | 30 | | |
| PSRR | Power Supply Rejection Ratio | Up to 250 kHz | | 46 | | dB |
| CMRR | Common Mode Rejection Ratio | | 40 | | | dB |

(1) Hysteresis is available for all comparator input source configurations.

CMPSS Comparator Input Referred Offset and Hysteresis

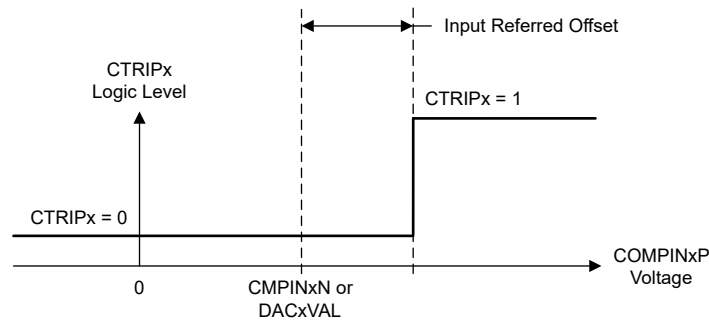


Figure 6-49. CMPSS Comparator Input Referred Offset

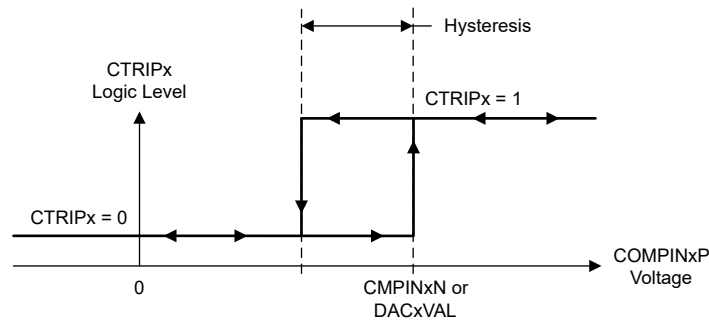


Figure 6-50. CMPSS Comparator Hysteresis

6.14.5.5.3 CMPSS DAC Static Electrical Characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------------|----------------------------------------------------------------------------------------|------|-----|------|----------|
| CMPSS DAC output range | Internal reference | 0 | | VDDA | V |
| Static offset error ⁽¹⁾ | | -25 | | 25 | mV |
| Static gain error ⁽¹⁾ | | -2 | | 2 | % of FSR |
| Static DNL | Endpoint corrected | >-1 | | 4 | LSB |
| Static INL | Endpoint corrected | -16 | | 16 | LSB |
| Settling time | Settling to 1LSB after full-scale output change | | | 1 | μs |
| Resolution | | | 12 | | bits |
| CMPSS DAC output disturbance ⁽²⁾ | Error induced by comparator trip or CMPSS DAC code change within the same CMPSS module | -100 | | 100 | LSB |
| CMPSS DAC disturbance time ⁽²⁾ | | | | 200 | ns |

(1) Includes comparator input referred errors.

(2) Disturbance error may be present on the CMPSS DAC output for a certain amount of time after a comparator trip.

6.14.5.5.4 CMPSS_LITE DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|-------------------------------------------------|------|-----|------|--------------|
| CMPSS DAC output range | | 0 | | VDDA | V |
| Static offset error ⁽¹⁾ | | -25 | | 25 | mV |
| Static gain error ⁽¹⁾ | | -0.5 | | 0.5 | % of FSR |
| Static DNL | Endpoint corrected | -5 | | 5 | LSB (12-bit) |
| Static INL | Endpoint corrected | -7 | | 7 | LSB (12-bit) |
| Static TUE (Total Unadjusted Error) | | | 35 | | mV |
| Settling time | Settling to 1LSB after full-scale output change | | 1 | | μs |

6.14.5.5.4 CMPSS_LITE DAC Static Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|-----------------|-----|-----|-----|------|
| Resolution ⁽²⁾ | | | 12 | | bits |

- (1) Includes comparator input referred errors.
- (2) 9.5-bit effective resolution for monotonic response

6.14.5.5.5 CMPSS Illustrative Graphs

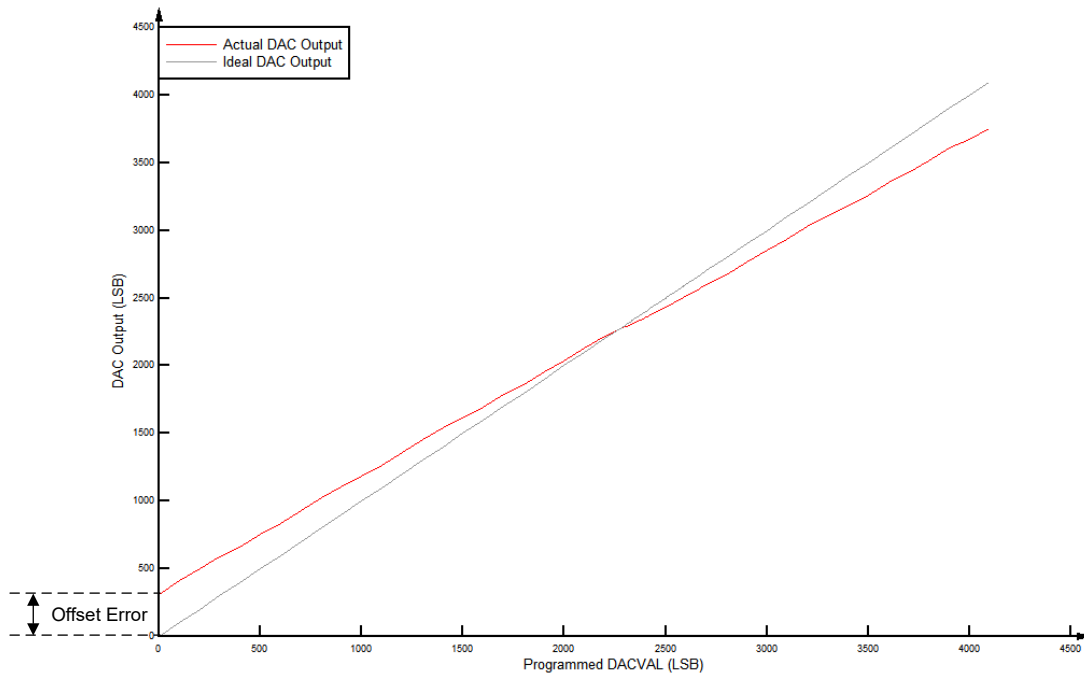


Figure 6-51. CMPSS DAC Static Offset

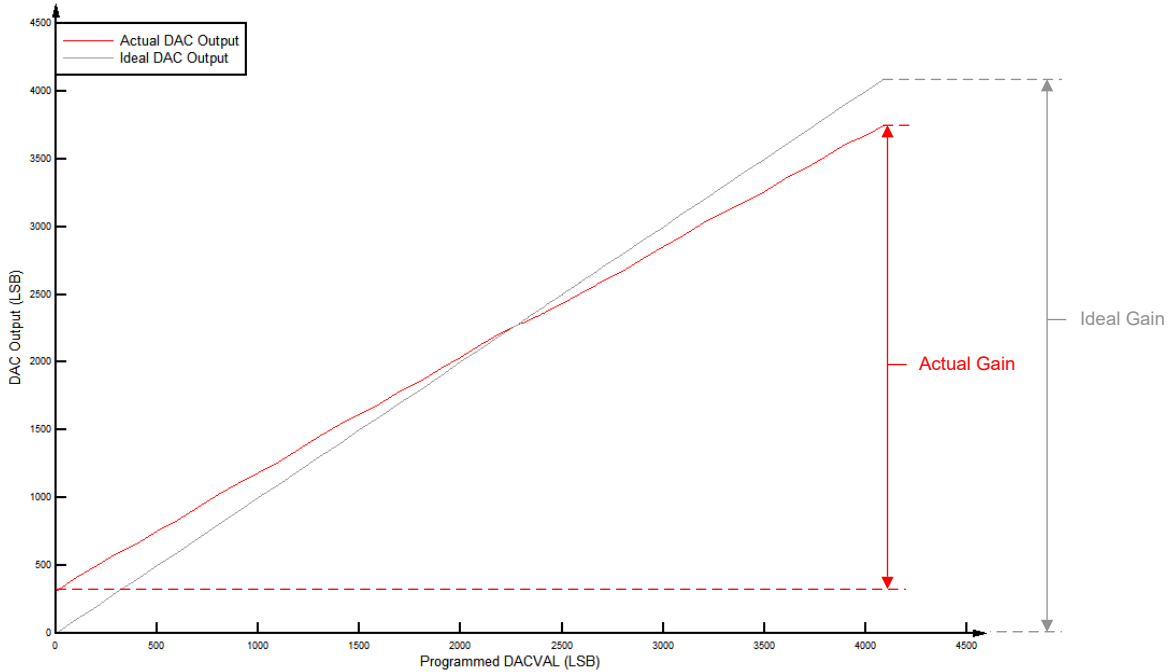


Figure 6-52. CMPSS DAC Static Gain

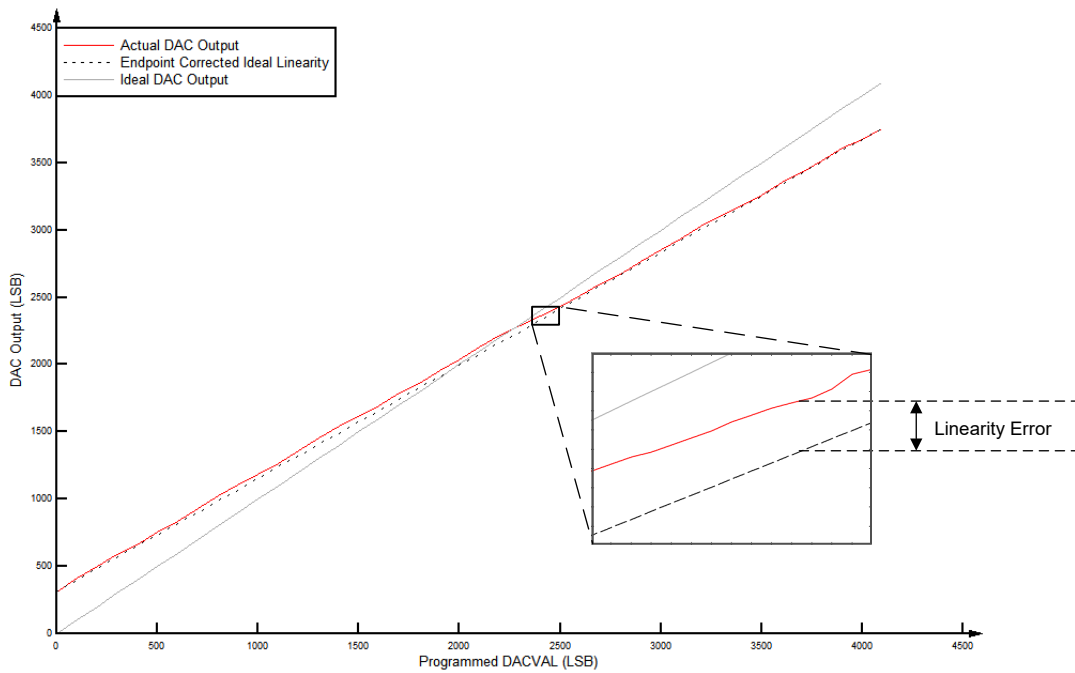


Figure 6-53. CMPSS DAC Static Linearity

6.14.5.5.6 CMPSS DAC Dynamic Error

When using the ramp generator to control the internal DAC, the step size can vary based on the application need. Since the step size of the DAC is less than a full scale transition, the settling time is improved from the electrical specification listed in the *CMPSS DAC Static Electrical Characteristics* table. The equation below and [Figure 6-54](#) can give guidance on the expected voltage error from ideal based on different RAMPxSTEPVALA values.

$$DYNAMICERROR = (m \times RAMPxSTEPVALA) + b \quad (3)$$

Table 6-27. DAC Max Dynamic Error Terms

| EQUATION PARAMETER | MIN (LSB) | MAX (LSB) |
|--------------------|-----------|-----------|
| m | 0.10 | 0.18 |
| b | 3.7 | 5.6 |

Note

Above error terms are based on the max SYSCLK of the target device. If operating below the max SYSCLK then the "m" error term should be scaled accordingly.

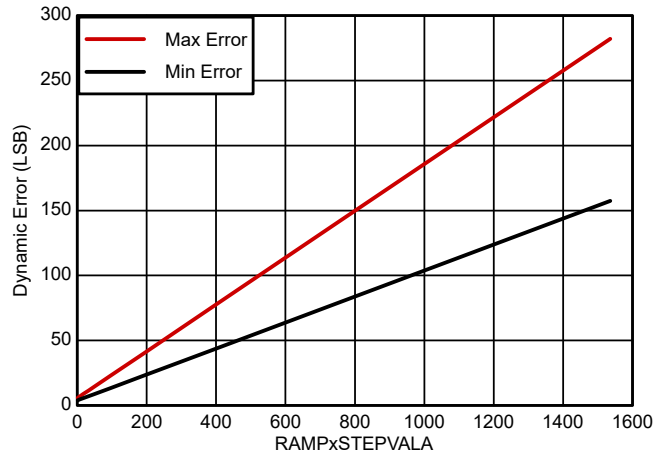


Figure 6-54. CMPSS DAC Dynamic Error

6.14.5.5.7 Buffered Output from CMPx_DACL Operating Conditions

over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|-------------------------------------------|-----------------------|-----|------------|------------|------|
| R _L | Resistive Load ⁽²⁾ | | 5 | | | kΩ |
| C _L | Capacitive Load | | | | 100 | pF |
| V _{OUT} | Valid Output Voltage Range ⁽³⁾ | R _L = 5 kΩ | 0.3 | | VDDA – 0.3 | V |
| | | R _L = 1 kΩ | 0.6 | | VDDA – 0.6 | V |
| Reference Voltage ⁽⁴⁾ | | VREFHI | 2.4 | 2.5 or 3.0 | VDDA | V |

- (1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
- (2) DAC can drive a minimum resistive load of 1 kΩ, but the output range will be limited.
- (3) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
- (4) For best PSRR performance, VREFHI should be less than VDDA.

6.14.5.5.8 Buffered Output from CMPx_DACL Electrical Characteristics

over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------------|------------------------------------------------|-----|-----|-----|------|
| General | | | | | |
| Resolution ⁽⁴⁾ | | | 12 | | bits |
| Load Regulation | | -1 | | 1 | mV/V |
| Glitch Energy | | | 1.5 | | V-ns |
| Voltage Output Settling Time Full-Scale | Settling to 2 LSBs after 0.3V-to-3V transition | | | 2 | μs |

6.14.5.5.8 Buffered Output from CMPx_DACL Electrical Characteristics (continued)

 over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------------|---------------------------------------------|---------------------------------------------------|------|-------|-----|--------------|
| Voltage Output Settling Time 1/4 th Full-Scale | | Settling to 2 LSBs after 0.3V-to-0.75V transition | | | 1.6 | μs |
| Voltage Output Slew Rate | | Slew rate from 0.3V-to-3V transition | 2.8 | | 4.5 | V/μs |
| Load Transient Settling Time | | 5-kΩ Load | | | 328 | ns |
| TPU | Power Up Time | Bandgap Not Enabled | | | 500 | μs |
| DC Characteristics | | | | | | |
| Offset | Offset Error | | -100 | | 100 | mV |
| Gain | Gain Error ⁽²⁾ | | -1.5 | | 1.5 | % of FSR |
| DNL | Differential Non Linearity | Endpoint corrected | -2 | | 2 | LSB (12-bit) |
| INL | Integral Non Linearity | Endpoint corrected | -7 | | 7 | LSB (12-bit) |
| AC Characteristics | | | | | | |
| Output Noise | | Integrated noise from 100 Hz to 100 kHz | | 600 | | μVrms |
| | | Noise density at 10 kHz | | 800 | | nVrms/√Hz |
| SNR | Signal to Noise Ratio | 1 kHz, 200 KSPS | | 64 | | dB |
| THD | Total Harmonic Distortion | 1 kHz, 200 KSPS | | -64.2 | | dB |
| SFDR | Spurious Free Dynamic Range | 1 kHz, 200 KSPS | | 66 | | dB |
| SINAD | Signal to Noise and Distortion Ratio | 1 kHz, 200 KSPS | | 61.7 | | dB |
| PSRR | Power Supply Rejection Ratio ⁽³⁾ | DC | | 70 | | dB |
| | | 100 kHz | | 30 | | dB |

(1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.

(2) Gain error is calculated for linear output range.

(3) VREFHI = 3.2 V, VDDA = 3.3 V DC + 100 mV Sine.

(4) 11-bit effective (monotonic response).

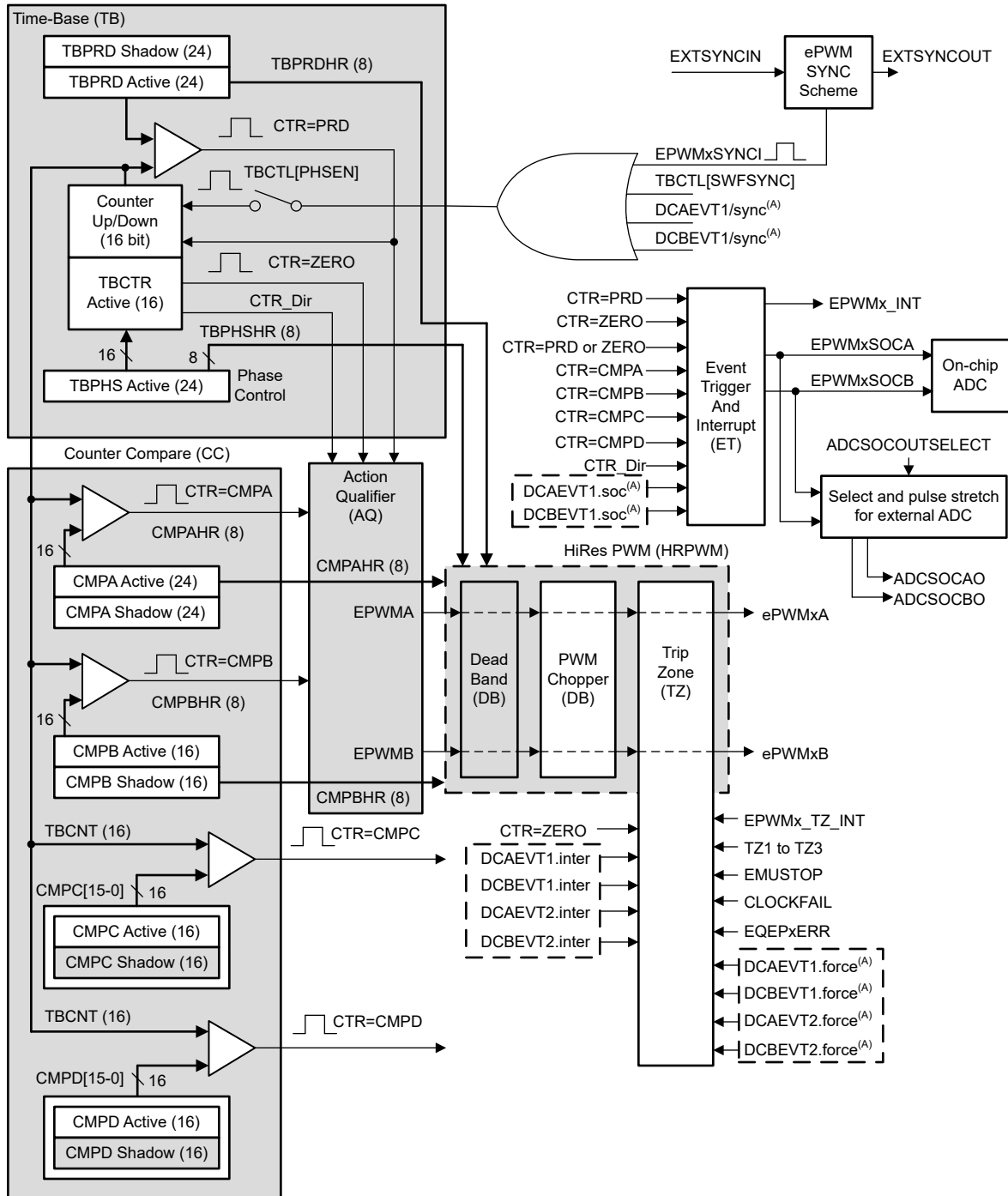
6.15 Control Peripherals

6.15.1 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules.

[Figure 6-55](#) shows the ePWM module. [Figure 6-56](#) shows the ePWM trip input connectivity.



A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

Figure 6-55. ePWM Submodules and Critical Internal Signal Interconnects

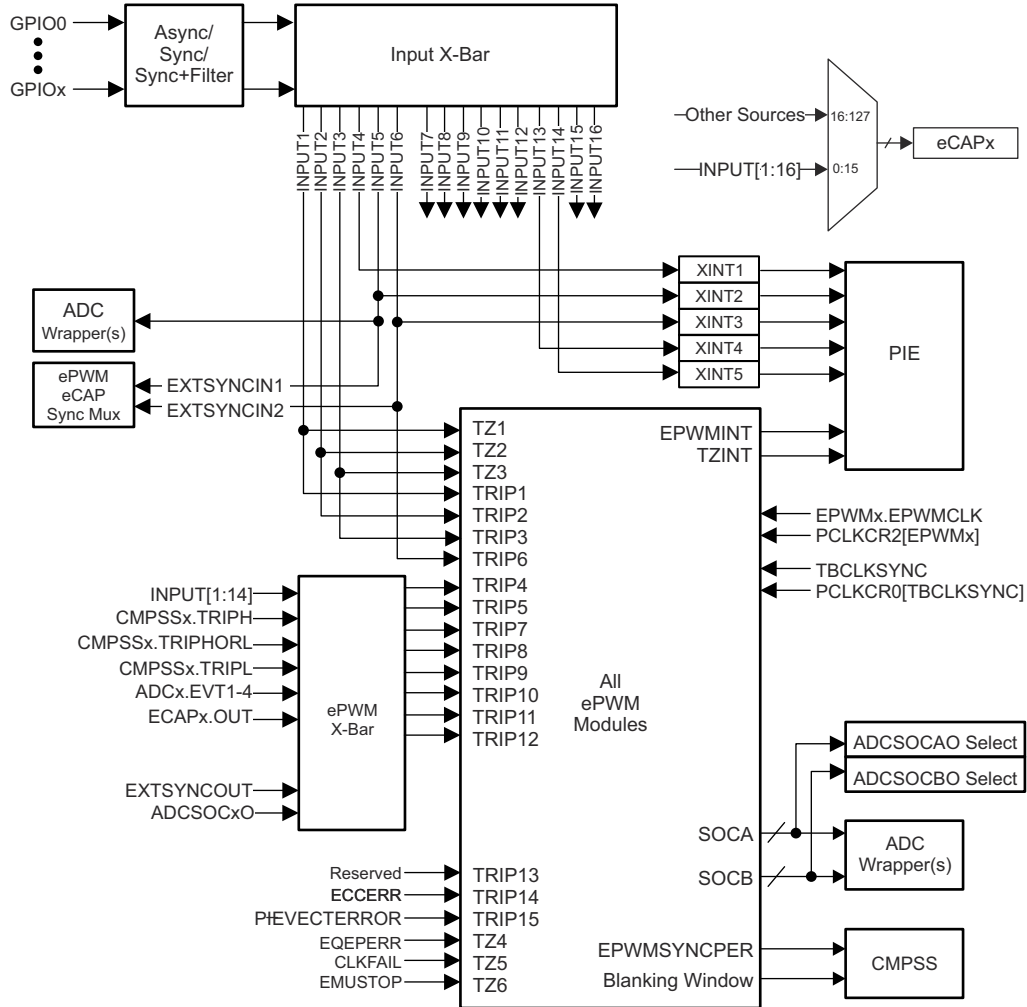


Figure 6-56. ePWM Trip Input Connectivity

6.15.1.1 Control Peripherals Synchronization

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules. Figure 6-57 shows the synchronization scheme.

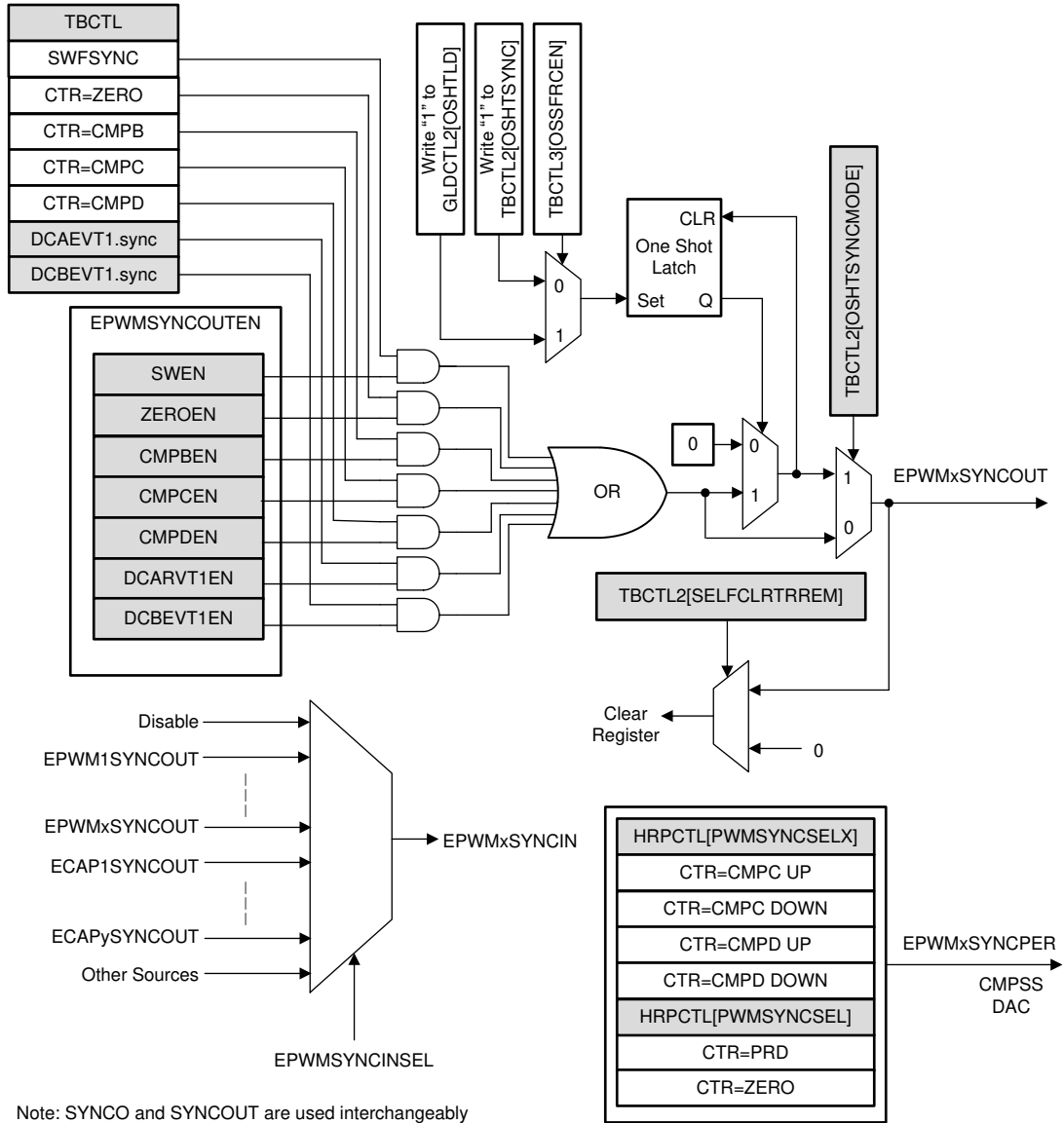


Figure 6-57. Synchronization Chain Architecture

6.15.1.2 ePWM Electrical Data and Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.15.1.2.1 ePWM Timing Requirements

| | | | MIN | MAX | UNIT |
|------------------------|------------------------|----------------------|-----------------------------------------------|-----|--------|
| $t_{w(\text{SYNCIN})}$ | Sync input pulse width | Asynchronous | $2t_{c(\text{EPWMCLK})}$ | | cycles |
| | | Synchronous | $2t_{c(\text{EPWMCLK})}$ | | |
| | | With input qualifier | $1t_{c(\text{EPWMCLK})} + t_{w(\text{IQSW})}$ | | |

6.15.1.2.2 ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|-----|--------|
| $t_{w(\text{PWM})}$ | Pulse duration, PWMx output high/low | 20 | | ns |
| $t_{w(\text{SYNCOUT})}$ | Sync output pulse width | $8t_{c(\text{SYSCLK})}$ | | cycles |
| $t_{d(\text{TZ-PWM})}$ | Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z | | 25 | ns |

(1) 20-pF load on pin.

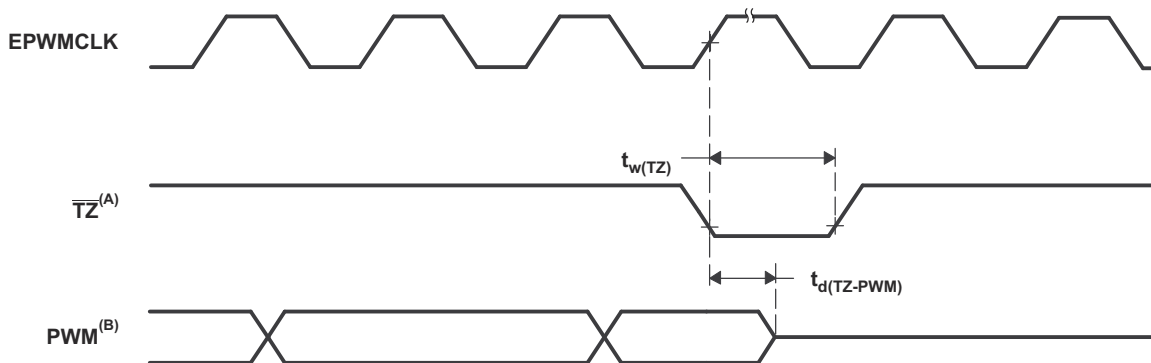
6.15.1.2.3 Trip-Zone Input Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.15.1.2.3.1 Trip-Zone Input Timing Requirements

| | | | MIN | MAX | UNIT |
|--------------------|---------------------------------------------------|----------------------|-----------------------------------------------|-----|--------|
| $t_{w(\text{TZ})}$ | Pulse duration, $\overline{\text{TZx}}$ input low | Asynchronous | $1t_{c(\text{EPWMCLK})}$ | | cycles |
| | | Synchronous | $2t_{c(\text{EPWMCLK})}$ | | cycles |
| | | With input qualifier | $1t_{c(\text{EPWMCLK})} + t_{w(\text{IQSW})}$ | | cycles |

6.15.1.2.3.2 PWM Hi-Z Characteristics Timing Diagram



A. TZ: TZ1, TZ2, TZ3, TRIP1–TRIP12

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after TZ is taken high depends on the PWM recovery software.

Figure 6-58. PWM Hi-Z Characteristics

6.15.2 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period and deadband registers of the ePWM module.

6.15.2.1 HRPWM Electrical Data and Timing

6.15.2.1.1 High-Resolution PWM Characteristics

| PARAMETER | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------|-----|-----|-----|------|
| Micro Edge Positioning (MEP) step size ⁽¹⁾ | | 150 | 310 | ps |

- (1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD}. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage. Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

6.15.3 External ADC Start-of-Conversion Electrical Data and Timing

6.15.3.1 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | MIN | MAX | UNIT |
|------------------------------------------------------------|-------------------|-----|--------|
| $t_{w(ADCSOCL)}$ Pulse duration, $\overline{ADCSOCxO}$ low | $32t_{c(SYSCLK)}$ | | cycles |

6.15.3.2 $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing Diagram

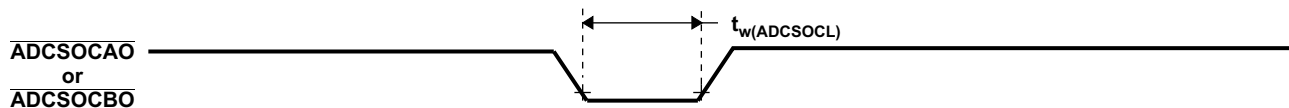


Figure 6-59. $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing

6.15.4 Enhanced Capture (eCAP)

The features of the eCAP module include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed by way of Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module features described in this chapter include:

- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single-shot capture of up to four event time-stamps
- Continuous mode capture of time stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output

The capture functionality of the Type 1 eCAP is enhanced from the Type 0 eCAP with the following added features:

- Event filter reset bit
 - Writing a 1 to ECCTL2[CTRFILTRESET] clears the event filter, the modulo counter, and any pending interrupts flags. Resetting the bit is useful for initialization and debug.
- Modulo counter status bits
 - The modulo counter (ECCTL2 [MODCNRSTS]) indicates which capture register is loaded next. In the Type 0 eCAP, to know the current state of the modulo counter was not possible
- Input multiplexer
 - ECCTL0 [INPUTSEL] selects one of 128 input signals, which are detailed in the Configuring Device Pins for the eCAP section of the Enhanced Capture (eCAP) chapter in the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#).
- EALLOW protection
 - EALLOW protection was added to critical registers. To maintain software compatibility with Type-0, configure DEV_CFG_REGS.ECAPTYPE to make these registers unprotected.

The capture functionality of the Type 2 eCAP is enhanced from the Type 1 eCAP with the following added features:

- Added ECAPxSYNCINSEL register
 - ECAPxSYNCINSEL register is added for each eCAP to select an external SYNCIN. Every eCAP can have a separate SYNCIN signal.

6.15.4.1 eCAP Block Diagram

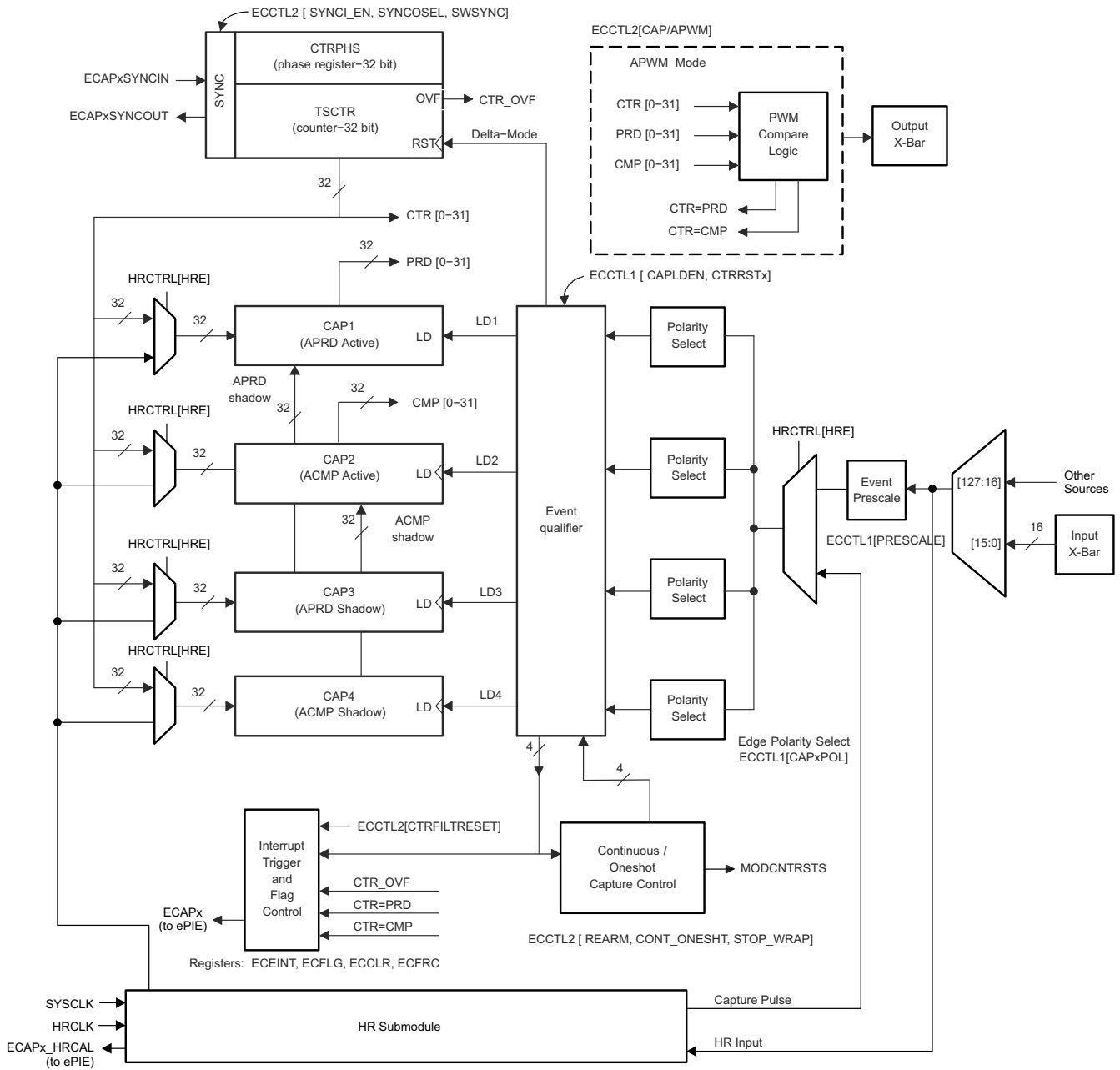


Figure 6-60. eCAP Block Diagram

6.15.4.2 eCAP Synchronization

The eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from EPWM, eCAP, or X-Bar. The SYNC signal is defined by the selection in the ECAPxSYNCINSEL[SEL] bit for ECAPx as shown in Figure 6-61.

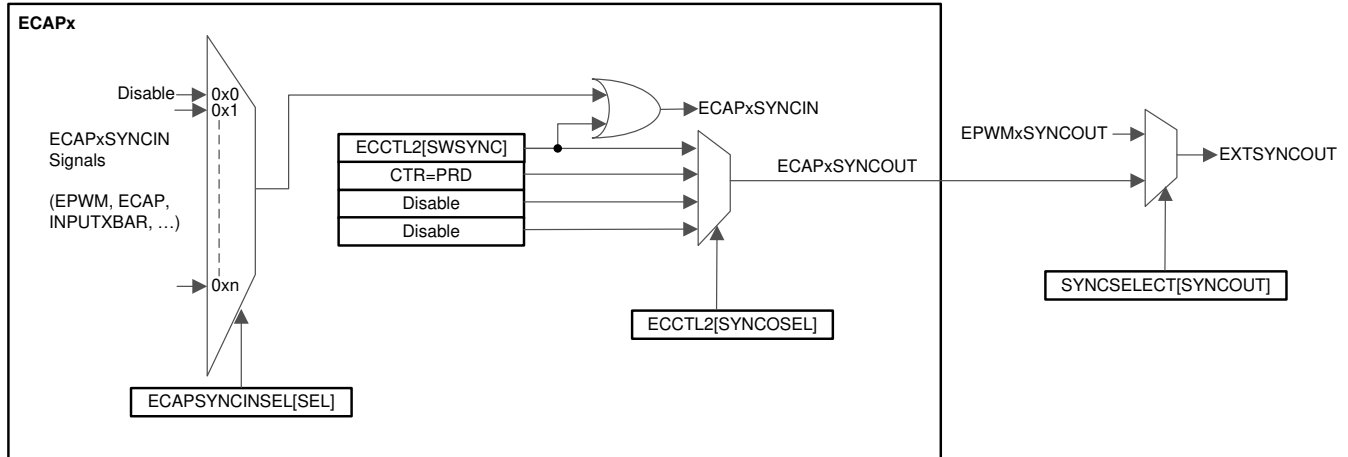


Figure 6-61. eCAP Synchronization Scheme

6.15.4.3 eCAP Electrical Data and Timing

6.15.4.3.1 eCAP Timing Requirements

| | | | MIN | NOM | MAX | UNIT |
|--------------|---------------------------|----------------------|--------------------------------|-----|-----|------|
| $t_{w(CAP)}$ | Capture input pulse width | Asynchronous | $2t_{c(SYSCLK)}$ | | ns | |
| | | Synchronous | $2t_{c(SYSCLK)}$ | | | |
| | | With input qualifier | $1t_{c(SYSCLK)} + t_{w_IQSW}$ | | | |

6.15.4.3.2 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------|---------------------------------------|-----|-----|-----|------|
| $t_{w(APWM)}$ | Pulse duration, APWMx output high/low | 20 | | | ns |

6.15.5 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module on this device is Type-2. The eQEP interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position control systems.

The eQEP peripheral contains the following major functional units (see Figure 6-62):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)
- Quadrature Mode Adapter (QMA)

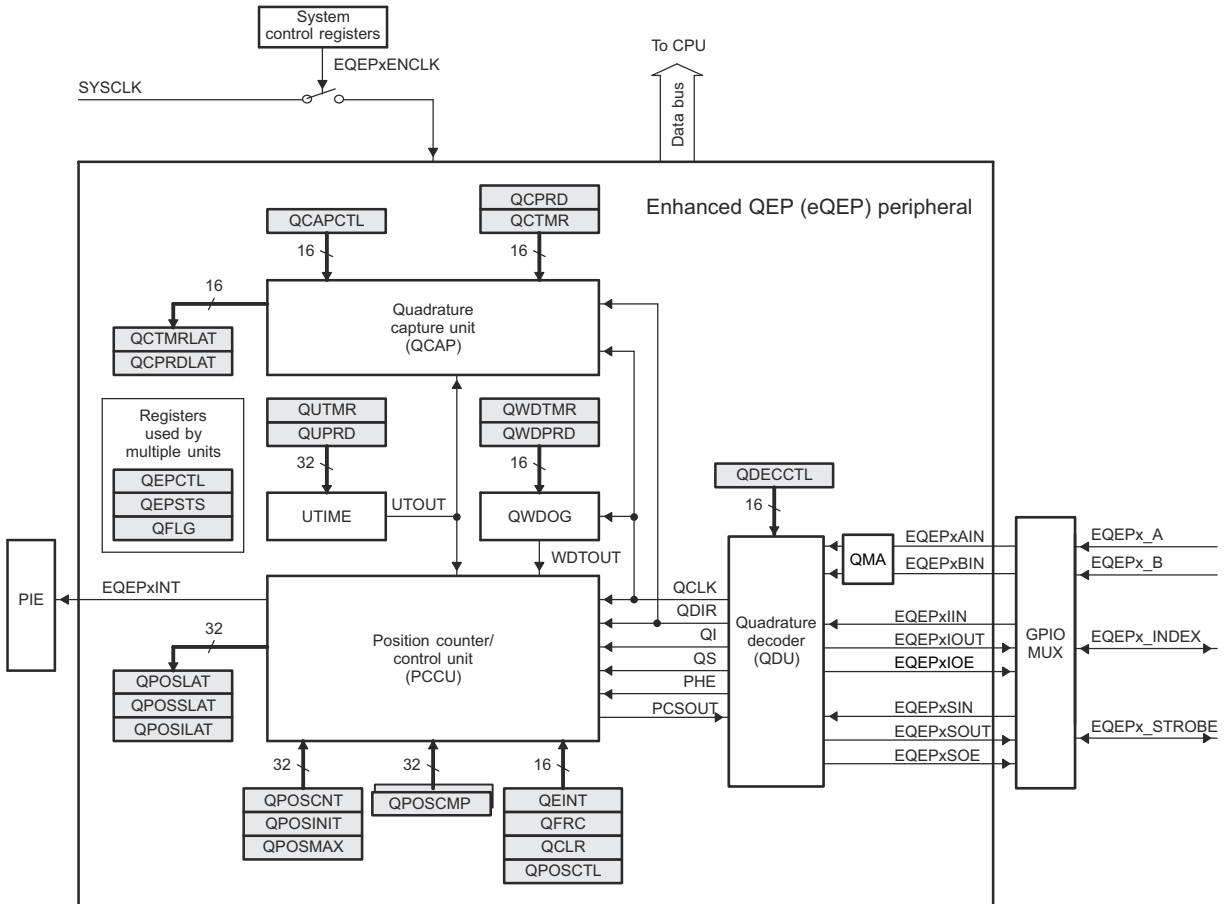


Figure 6-62. eQEP Block Diagram

6.15.5.1 eQEP Electrical Data and Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.15.5.1.1 eQEP Timing Requirements

| | | | MIN | MAX | UNIT |
|-----------------|---------------------------|----------------------------------|-----------------------------------|-----|--------|
| $t_{w(QEPP)}$ | QEP input period | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$ | | |
| $t_{w(INDEXH)}$ | QEP Index Input High time | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |
| $t_{w(INDEXL)}$ | QEP Index Input Low time | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |
| $t_{w(STROBH)}$ | QEP Strobe High time | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |
| $t_{w(STROBL)}$ | QEP Strobe Input Low time | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |

(1) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.

6.15.5.1.2 eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|------------------------|------------------------------------------------------------|------------------|-----|--------|
| $t_{d(CNTR)_{xin}}$ | Delay time, external clock to counter increment | $5t_{c(SYSCLK)}$ | | cycles |
| $t_{d(PCS-OUT)_{QEP}}$ | Delay time, QEP input edge to position compare sync output | $7t_{c(SYSCLK)}$ | | cycles |

6.16 Communications Peripherals

6.16.1 Controller Area Network (CAN)

Note

The CAN module uses the IP known as *DCAN*. This document uses the names *CAN* and *DCAN* interchangeably to reference this peripheral.

The CAN module implements the following features:

- Complies with ISO11898-1 (Bosch® CAN protocol specification 2.0 A and B)
- Bit rates up to 1 Mbps
- Multiple clock sources
- 32 message objects (mailboxes), each with the following properties:
 - Configurable as receive or transmit
 - Configurable with standard (11-bit) or extended (29-bit) identifier
 - Supports programmable identifier receive mask
 - Supports data and remote frames
 - Holds 0 to 8 bytes of data
 - Parity-checked configuration and data RAM
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loopback modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after bus-off state by a programmable 32-bit timer
- Two interrupt lines

Note

For a CAN bit clock of 100 MHz, the smallest bit rate possible is 3.90625Kbps.

Note

The accuracy of the on-chip oscillator is in the INTOSC Characteristics table. Depending on parameters such as the CAN bit timing settings, bit rate, bus length, and propagation delay, the accuracy of this oscillator may not meet the requirements of the CAN protocol. In this situation, an external clock source must be used.

Figure 6-63 shows the CAN block diagram.

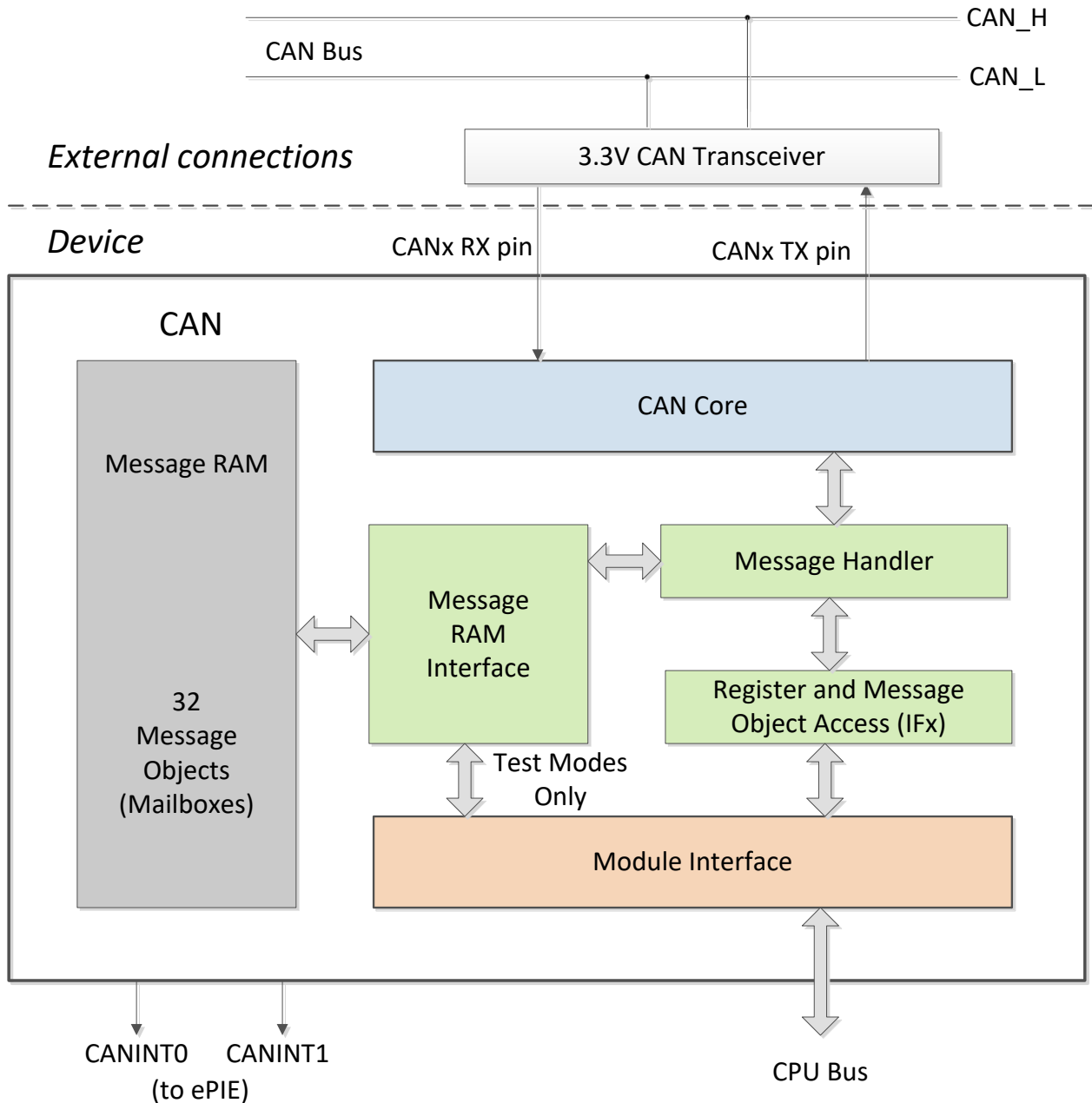


Figure 6-63. CAN Block Diagram

6.16.2 Modular Controller Area Network (MCAN)

The Controller Area Network (CAN) is a serial communications protocol that efficiently supports distributed real-time control with a high level of reliability. CAN has high immunity to electrical interference and the ability to detect various type of errors. In CAN, many short messages are broadcast to the entire network, which provides data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with flexible data-rate) protocols. The CAN FD feature allows higher throughput and increased payload per data frame. Classic CAN and CAN FD devices may coexist on the same network without any conflict provided that partial network transceivers, which can detect and ignore CAN FD without generating bus errors, are used by the classic CAN devices. The MCAN module is compliant to ISO 11898-1:2015.

Note

The availability of the CAN FD feature is dependent on the device's part number. Refer to the device data sheet for more information.

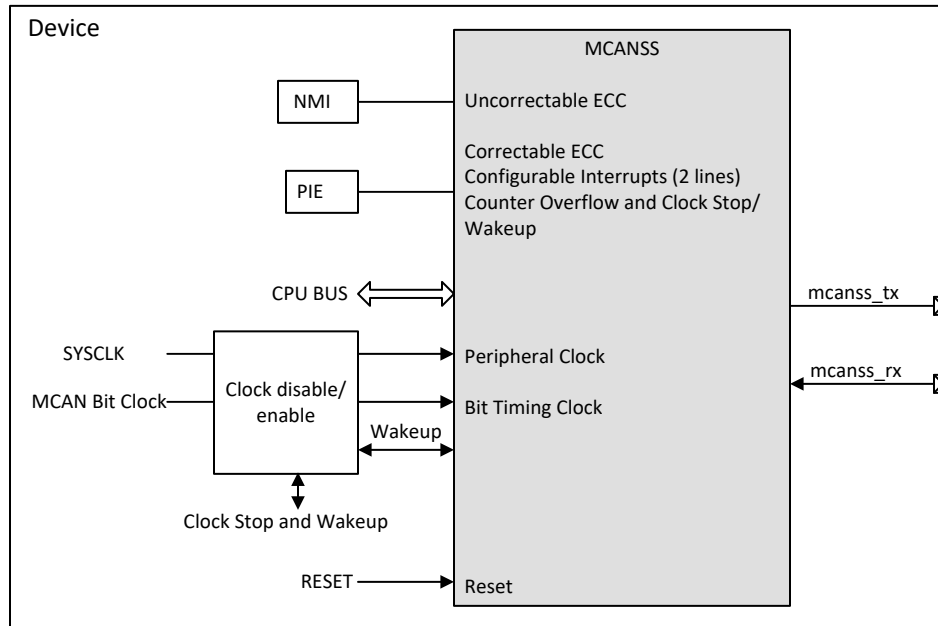


Figure 6-64. MCAN Module Overview

The MCAN module implements the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- AUTOSAR and SAE J1939 support
- Flexible Message RAM allocation (maximum configuration below is for a device with 4352 32-bit word message RAM)
 - Up to 32 dedicated transmit buffers
 - Configurable transmit FIFO, up to 32 elements
 - Configurable transmit queue, up to 32 elements
 - Configurable transmit Event FIFO, up to 32 elements
 - Up to 64 dedicated receive buffers
 - Two configurable receive FIFOs, up to 64 elements each
 - Up to 128 filter elements
- Loop-back mode for self-test
- Maskable interrupt (two configurable interrupt lines, correctable ECC, counter overflow and clock stop/wakeup)
- Non-maskable interrupt (uncorrectable ECC)
- Two clock domains (CAN clock/host clock)
- ECC check for Message RAM
- Clock stop and wake-up support
- Timestamp counter

Non-supported features:

- Host bus firewall
- Clock calibration
- Debug over CAN

6.16.3 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the NXP Semiconductors I²C-bus specification (version 2.1):
 - Support for 8-bit format transfers
 - 7-bit and 10-bit addressing modes
 - General call
 - START byte mode
 - Support for multiple master-transmitters and slave-receivers
 - Support for multiple slave-transmitters and master-receivers
 - Combined master transmit/receive and receive/transmit mode
 - Data transfer rate from 10Kbps up to 400Kbps (Fast-mode)
- Supports voltage thresholds compatible to:
 - SMBus 2.0 and below
 - PMBus 1.2 and below
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- Supports two ePIE interrupts
 - I2Cx interrupt – Any of the below conditions can be configured to generate an I2Cx interrupt:
 - Transmit Ready
 - Receive Ready
 - Register-Access Ready
 - No-Acknowledgment
 - Arbitration-Lost
 - Stop Condition Detected
 - Addressed-as-Slave
 - I2Cx_FIFO interrupts:
 - Transmit FIFO interrupt
 - Receive FIFO interrupt
- Module enable and disable capability
- Free data format mode

Figure 6-65 shows how the I2C peripheral module interfaces within the device.

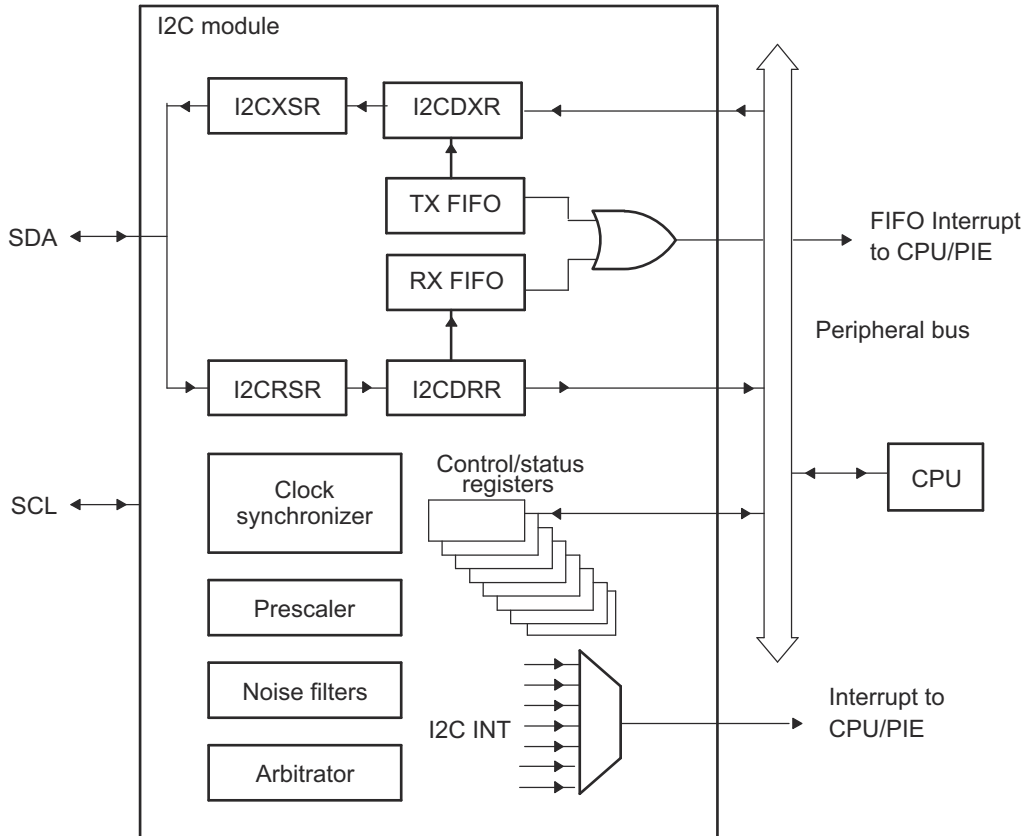


Figure 6-65. I2C Peripheral Module Interfaces

6.16.3.1 I2C Electrical Data and Timing

Note

To meet all of the I2C protocol timing specifications, the I2C module clock must be configured in the range from 7 MHz to 12 MHz.

A pullup resistor must be chosen to meet the I2C standard timings. In most circumstances, 2.2 kΩ of total bus resistance to VDDIO is sufficient. For evaluating pullup resistor values for a particular design, see the [I2C Bus Pullup Resistor Calculation](#) Application Report.

6.16.3.1.1 I2C Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|----------------------|------------------------|------------------------------------------------------------|--------------------|---------------------|------|
| Standard mode | | | | | |
| T0 | f_{mod} | I2C module frequency | 7 | 12 | MHz |
| T1 | $t_{h(SDA-SCL)START}$ | Hold time, START condition, SCL fall delay after SDA fall | 4.0 | | μs |
| T2 | $t_{su(SCL-SDA)START}$ | Setup time, Repeated START, SCL rise before SDA fall delay | 4.0 | | μs |
| T3 | $t_{h(SCL-DAT)}$ | Hold time, data after SCL fall | 0 | | μs |
| T4 | $t_{su(DAT-SCL)}$ | Setup time, data before SCL rise | 250 ⁽²⁾ | | ns |
| T5 | $t_r(SDA)$ | Rise time, SDA | | 1000 ⁽¹⁾ | ns |
| T6 | $t_r(SCL)$ | Rise time, SCL | | 1000 ⁽¹⁾ | ns |
| T7 | $t_f(SDA)$ | Fall time, SDA | | 300 | ns |
| T8 | $t_f(SCL)$ | Fall time, SCL | | 300 | ns |
| T9 | $t_{su(SCL-SDA)STOP}$ | Setup time, STOP condition, SCL rise before SDA rise delay | 4.0 | | μs |
| T10 | $t_w(SP)$ | Pulse duration of spikes that will be suppressed by filter | 0 | 50 | ns |
| T11 | C_b | capacitance load on each bus line | | 400 | pF |
| Fast mode | | | | | |
| T0 | f_{mod} | I2C module frequency | 7 | 12 | MHz |
| T1 | $t_{h(SDA-SCL)START}$ | Hold time, START condition, SCL fall delay after SDA fall | 0.6 | | μs |
| T2 | $t_{su(SCL-SDA)START}$ | Setup time, Repeated START, SCL rise before SDA fall delay | 0.6 | | μs |
| T3 | $t_{h(SCL-DAT)}$ | Hold time, data after SCL fall | 0 | | μs |
| T4 | $t_{su(DAT-SCL)}$ | Setup time, data before SCL rise | 100 | | ns |
| T5 | $t_r(SDA)$ | Rise time, SDA | 20 | 300 | ns |
| T6 | $t_r(SCL)$ | Rise time, SCL | 20 | 300 | ns |
| T7 | $t_f(SDA)$ | Fall time, SDA | 11.4 | 300 | ns |
| T8 | $t_f(SCL)$ | Fall time, SCL | 11.4 | 300 | ns |
| T9 | $t_{su(SCL-SDA)STOP}$ | Setup time, STOP condition, SCL rise before SDA rise delay | 0.6 | | μs |
| T10 | $t_w(SP)$ | Pulse duration of spikes that will be suppressed by filter | 0 | 50 | ns |
| T11 | C_b | capacitance load on each bus line | | 400 | pF |

(1) In order to minimize the rise time, TI recommends using a strong pullup on both the SDA and SCL bus lines on the order of 2.2-kΩ net pullup resistance. It is also recommended that the value of the pullup resistance used on both SCL and SDA pins be matched.

(2) The C2000 I2C is a Fast-mode device. There is a limitation when using the I2C as a target transmitter with a standard mode host. For more information, see the [TMS320F280015x Real-Time MCUs Silicon Errata](#).

6.16.3.1.2 I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT | |
|----------------------|------------------|-------------------------------------------------|-----------------------------------|------|---------|---------|
| Standard mode | | | | | | |
| S1 | f_{SCL} | SCL clock frequency | 0 | 100 | kHz | |
| S2 | T_{SCL} | SCL clock period | 10 | | μs | |
| S3 | $t_{w(SCLL)}$ | Pulse duration, SCL clock low | 4.7 | | μs | |
| S4 | $t_{w(SCLH)}$ | Pulse duration, SCL clock high | 4.0 | | μs | |
| S5 | t_{BUF} | Bus free time between STOP and START conditions | 4.7 | | μs | |
| S6 | $t_{v(SCL-DAT)}$ | Valid time, data after SCL fall | | 3.45 | μs | |
| S7 | $t_{v(SCL-ACK)}$ | Valid time, Acknowledge after SCL fall | | 3.45 | μs | |
| S8 | I_I | Input current on pins | $0.1 V_{bus} < V_i < 0.9 V_{bus}$ | -10 | 10 | μA |
| Fast mode | | | | | | |
| S1 | f_{SCL} | SCL clock frequency | 0 | 400 | kHz | |
| S2 | T_{SCL} | SCL clock period | 2.5 | | μs | |
| S3 | $t_{w(SCLL)}$ | Pulse duration, SCL clock low | 1.3 | | μs | |
| S4 | $t_{w(SCLH)}$ | Pulse duration, SCL clock high | 0.6 | | μs | |
| S5 | t_{BUF} | Bus free time between STOP and START conditions | 1.3 | | μs | |
| S6 | $t_{v(SCL-DAT)}$ | Valid time, data after SCL fall | | 0.9 | μs | |
| S7 | $t_{v(SCL-ACK)}$ | Valid time, Acknowledge after SCL fall | | 0.9 | μs | |
| S8 | I_I | Input current on pins | $0.1 V_{bus} < V_i < 0.9 V_{bus}$ | -10 | 10 | μA |

6.16.3.1.3 I2C Timing Diagram

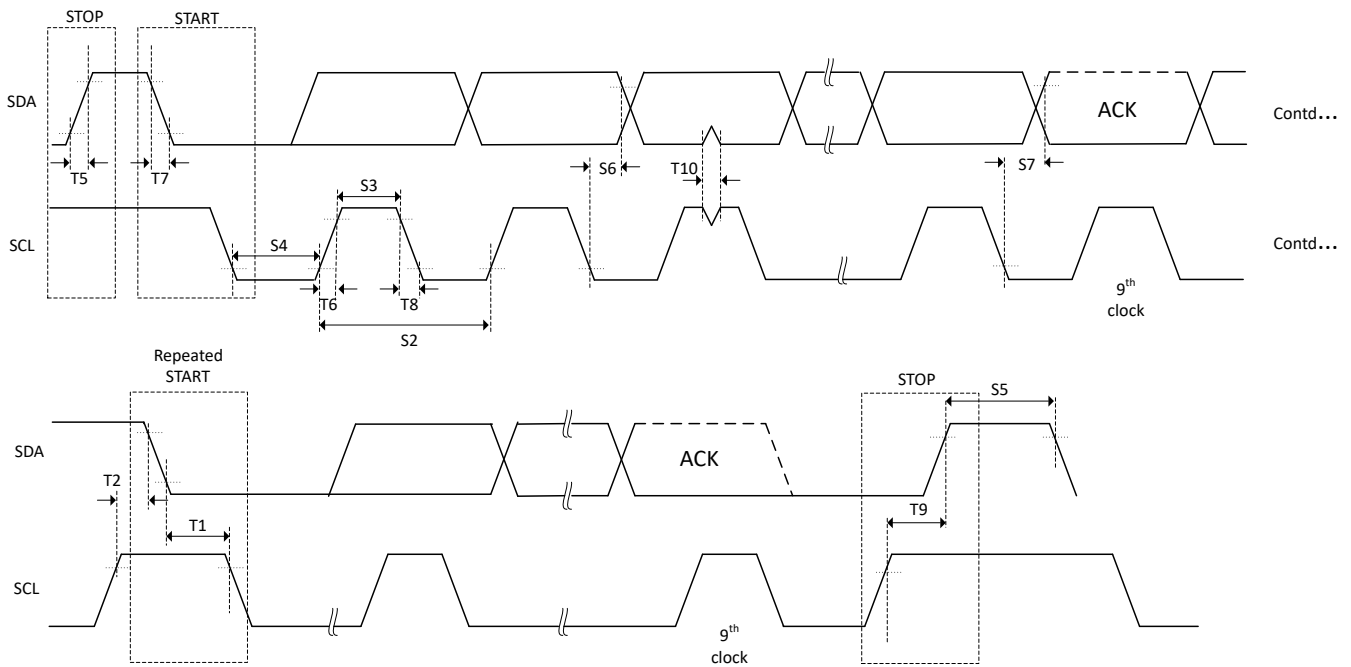


Figure 6-66. I2C Timing Diagram

6.16.4 Power Management Bus (PMBus) Interface

The PMBus module has the following features:

- Compliance with the SMI Forum PMBus Specification (Part I v1.0 and Part II v1.1)
- Supports voltage thresholds compatible to:
 - PMBus 1.2 and below
 - SMBus 2.0 and below
- Support for master and slave modes
- Support for I2C mode
- Support for two speeds:
 - Standard Mode: Up to 100 kHz
 - Fast Mode: 400 kHz
- Packet error checking
- CONTROL and ALERT signals
- Clock high and low time-outs
- Four-byte transmit and receive buffers
- One maskable interrupt, which can be generated by several conditions:
 - Receive data ready
 - Transmit buffer empty
 - Slave address received
 - End of message
 - ALERT input asserted
 - Clock low time-out
 - Clock high time-out
 - Bus free

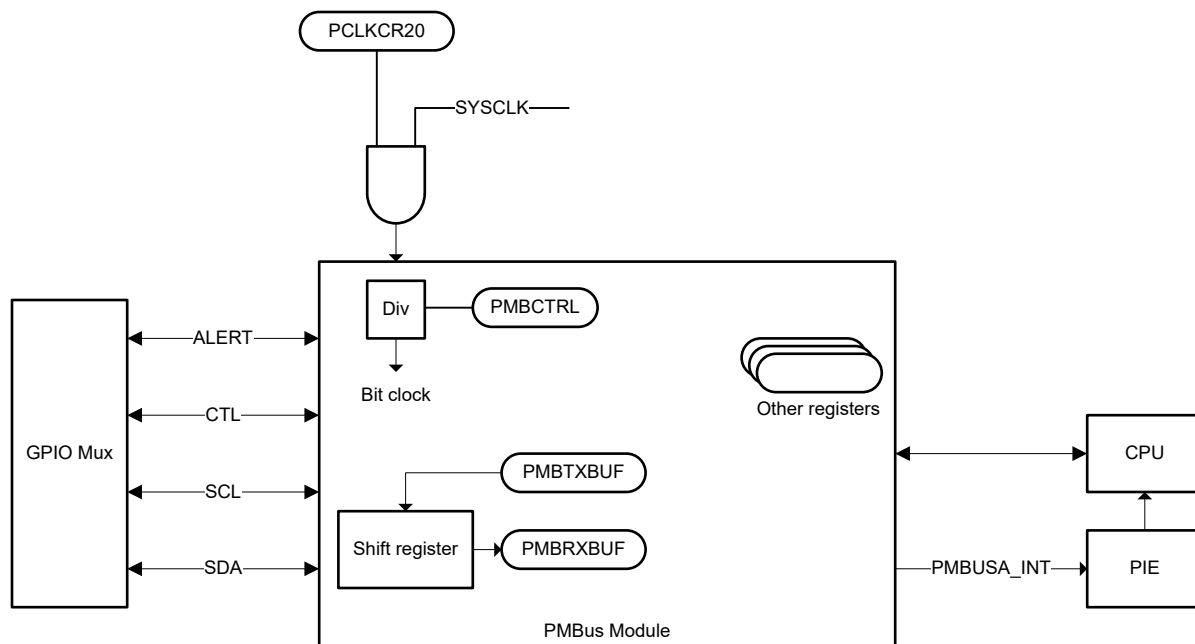


Figure 6-67. PMBus Block Diagram

6.16.4.1 PMBus Electrical Data and Timing

6.16.4.1.1 PMBus Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|-------------------------------------------------------------------|--------------------------------------------------------------|-----|-------|-----|------|
| V _{IL} | Valid low-level input voltage | | | | 0.8 | V |
| V _{IH} | Valid high-level input voltage | | 2.1 | VDDIO | | V |
| V _{OL} | Low-level output voltage | At I _{pullup} = 4 mA | | | 0.4 | V |
| I _{OL} | Low-level output current | V _{OL} ≤ 0.4 V | 4 | | | mA |
| t _{SP} | Pulse width of spikes that must be suppressed by the input filter | | 0 | | 50 | ns |
| I _i | Input leakage current on each pin | 0.1 V _{bus} < V _i < 0.9 V _{bus} | -10 | | 10 | μA |
| C _i | Capacitance on each pin | | | | 10 | pF |

6.16.4.1.2 PMBus Fast Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---------------------------------------------------------|--------------------|-----|-----|-----|------|
| f _{SCL} | SCL clock frequency | | 10 | | 400 | kHz |
| t _{BUF} | Bus free time between STOP and START conditions | | 1.3 | | | μs |
| t _{HD;STA} | START condition hold time -- SDA fall to SCL fall delay | | 0.6 | | | μs |
| t _{SU;STA} | Repeated START setup time -- SCL rise to SDA fall delay | | 0.6 | | | μs |
| t _{SU;STO} | STOP condition setup time -- SCL rise to SDA rise delay | | 0.6 | | | μs |
| t _{HD;DAT} | Data hold time after SCL fall | | 300 | | | ns |
| t _{SU;DAT} | Data setup time before SCL rise | | 100 | | | ns |
| t _{Timeout} | Clock low time-out | | 25 | | 35 | ms |
| t _{LOW} | Low period of the SCL clock | | 1.3 | | | μs |
| t _{HIGH} | High period of the SCL clock | | 0.6 | | 50 | μs |
| t _{LOW;SEXT} | Cumulative clock low extend time (slave device) | From START to STOP | | | 25 | ms |
| t _{LOW;MEXT} | Cumulative clock low extend time (master device) | Within each byte | | | 10 | ms |
| t _r | Rise time of SDA and SCL | 5% to 95% | 20 | | 300 | ns |
| t _f | Fall time of SDA and SCL | 95% to 5% | 20 | | 300 | ns |

6.16.4.1.3 PMBus Standard Mode Switching Characteristics
over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---------------------------------------------------------|--------------------|-----|-----|------|------|
| f _{SCL} | SCL clock frequency | | 10 | | 100 | kHz |
| t _{BUF} | Bus free time between STOP and START conditions | | 4.7 | | | μs |
| t _{HD;STA} | START condition hold time -- SDA fall to SCL fall delay | | 4 | | | μs |
| t _{SU;STA} | Repeated START setup time -- SCL rise to SDA fall delay | | 4.7 | | | μs |
| t _{SU;STO} | STOP condition setup time -- SCL rise to SDA rise delay | | 4 | | | μs |
| t _{HD;DAT} | Data hold time after SCL fall | | 300 | | | ns |
| t _{SU;DAT} | Data setup time before SCL rise | | 250 | | | ns |
| t _{Timeout} | Clock low time-out | | 25 | | 35 | ms |
| t _{LOW} | Low period of the SCL clock | | 4.7 | | | μs |
| t _{HIGH} | High period of the SCL clock | | 4 | | 50 | μs |
| t _{LOW;SEXT} | Cumulative clock low extend time (slave device) | From START to STOP | | | 25 | ms |
| t _{LOW;MEXT} | Cumulative clock low extend time (master device) | Within each byte | | | 10 | ms |
| t _r | Rise time of SDA and SCL | | | | 1000 | ns |
| t _f | Fall time of SDA and SCL | | | | 300 | ns |

6.16.5 Serial Communications Interface (SCI)

The SCI is a 2-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register.

Features of the SCI module include:

- Two external pins:
 - SCITXD: SCI transmit-output pin
 - SCIRXD: SCI receive-input pin
 - Baud rate programmable to 64K different rates
- Data-word format
 - 1 start bit
 - Data-word length programmable from 1 to 8 bits
 - Optional even/odd/no parity bit
 - 1 or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
 - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
 - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

Note

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

Figure 6-68 shows the SCI block diagram.

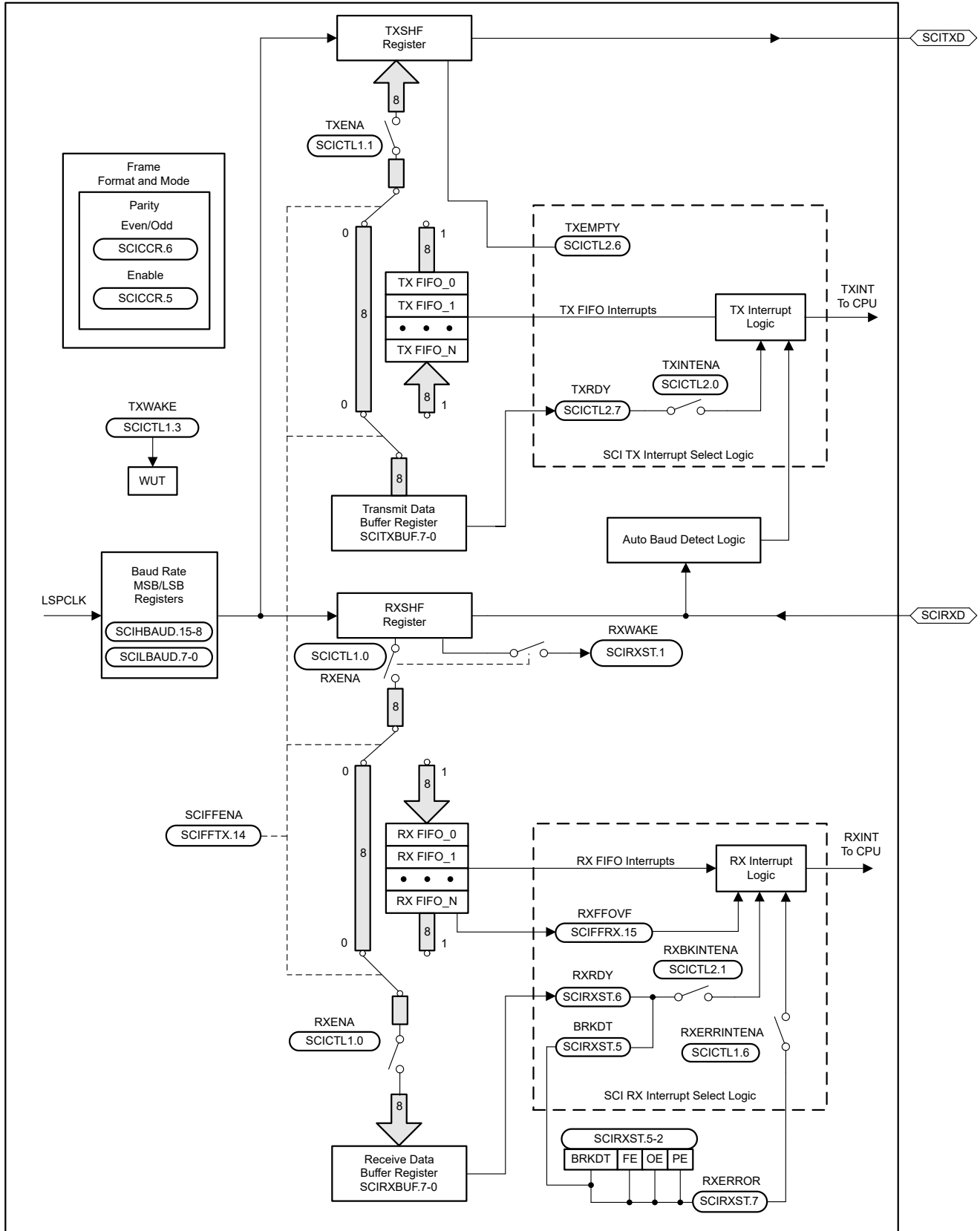


Figure 6-68. SCI Block Diagram

6.16.6 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input and output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the MCU controller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and analog-to-digital converters (ADCs). Multidevice communications are supported by the master or slave operation of the SPI. The port supports a 16-level, receive and transmit FIFO for reducing CPU servicing overhead.

The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- SPISTĒ: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: Master and Slave
- Baud rate: 125 different programmable rates. The maximum baud rate that can be employed is limited by the maximum speed of the I/O buffers used on the SPI pins.
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
 - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
 - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithm
- 16-level transmit/receive FIFO
- High-speed mode
- Delayed transmit control
- 3-wire SPI mode
- SPISTĒ inversion for digital audio interface receive mode on devices with two SPI modules

Figure 6-69 shows the SPI CPU interfaces.

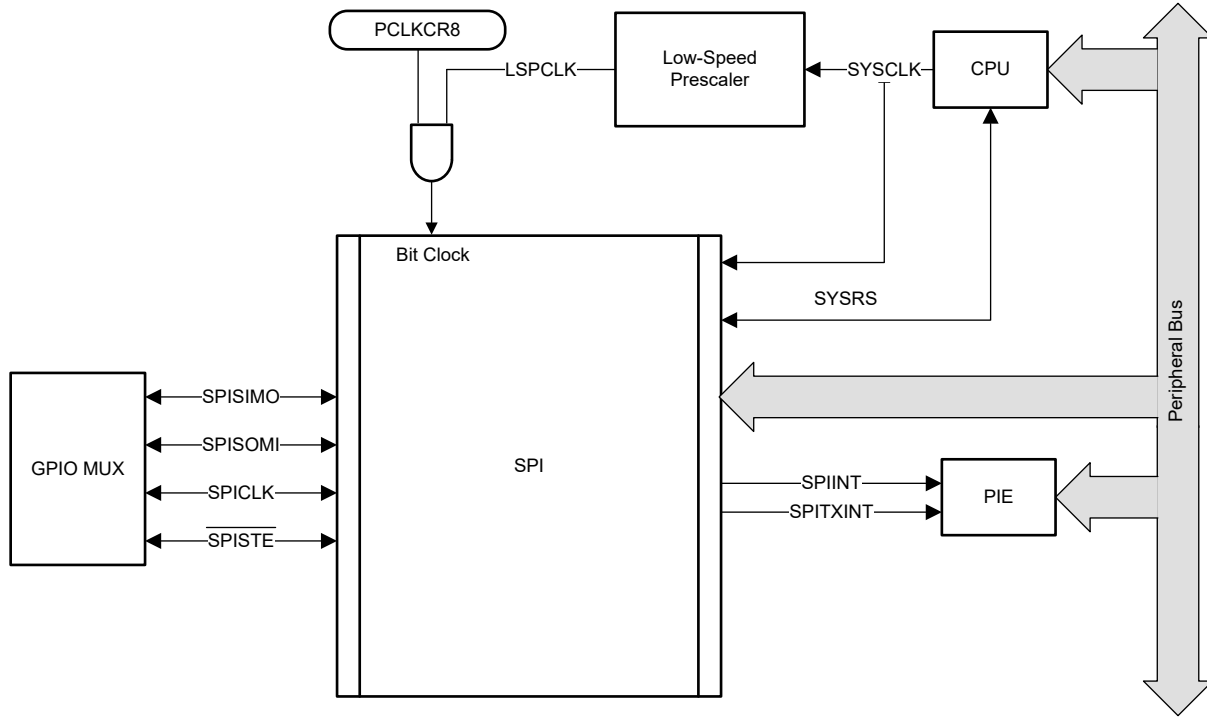


Figure 6-69. SPI CPU Interface

6.16.6.1 SPI Master Mode Timings

The following section contains the SPI Master Mode Timings. For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#).

Note

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPISIMO, and SPISOMI.

6.16.6.1.1 SPI Master Mode Timing Requirements

| NO. | | | (BRR + 1) ⁽¹⁾ | MIN | MAX | UNIT |
|------------------------|-----------------|-----------------------------------------|--------------------------|-----|-----|------|
| High-Speed Mode | | | | | | |
| 8 | $t_{su(SOMI)M}$ | Setup time, SPISOMI valid before SPICLK | Even, Odd | 1 | | ns |
| 9 | $t_{h(SOMI)M}$ | Hold time, SPISOMI valid after SPICLK | Even, Odd | 6.5 | | ns |
| Normal Mode | | | | | | |
| 8 | $t_{su(SOMI)M}$ | Setup time, SPISOMI valid before SPICLK | Even, Odd | 15 | | ns |
| 9 | $t_{h(SOMI)M}$ | Hold time, SPISOMI valid after SPICLK | Even, Odd | 0 | | ns |

- (1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

6.16.6.1.2 SPI Master Mode Switching Characteristics - Clock Phase 0

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER ^{(1) (2)} | | (BRR + 1) ⁽³⁾ | MIN | MAX | UNIT |
|------------------------|------------------------------|----------------------------------------------------|--------------------------|-----------------------------------------|-----------------------------------------|------|
| General | | | | | | |
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ | $128t_{c(LSPCLK)}$ | ns |
| | | | Odd | $5t_{c(LSPCLK)}$ | $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPC1)M}$ | Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$ | |
| 3 | $t_{w(SPC2)M}$ | Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$ | |
| 23 | $t_{d(SPC)M}$ | Delay time, \overline{SPISTE} active to SPICLK | Even | $1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$ | $1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$ | ns |
| | | | Odd | $1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} - 3$ | $1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} + 3$ | |
| 24 | $t_{v(STE)M}$ | Valid time, SPICLK to \overline{SPISTE} inactive | Even | $0.5t_{c(SPC)M} - 3$ | $0.5t_{c(SPC)M} + 3$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$ | |
| High-Speed Mode | | | | | | |
| 4 | $t_{d(SIMO)M}$ | Delay time, SPICLK to SPISIMO valid | Even, Odd | | 1 | ns |
| 5 | $t_{v(SIMO)M}$ | Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |
| Normal Mode | | | | | | |
| 4 | $t_{d(SIMO)M}$ | Delay time, SPICLK to SPISIMO valid | Even, Odd | | 2 | ns |
| 5 | $t_{v(SIMO)M}$ | Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |

(1) 10-pF load on pin for High-Speed Mode.

(2) 20-pF load on pin for Normal Mode.

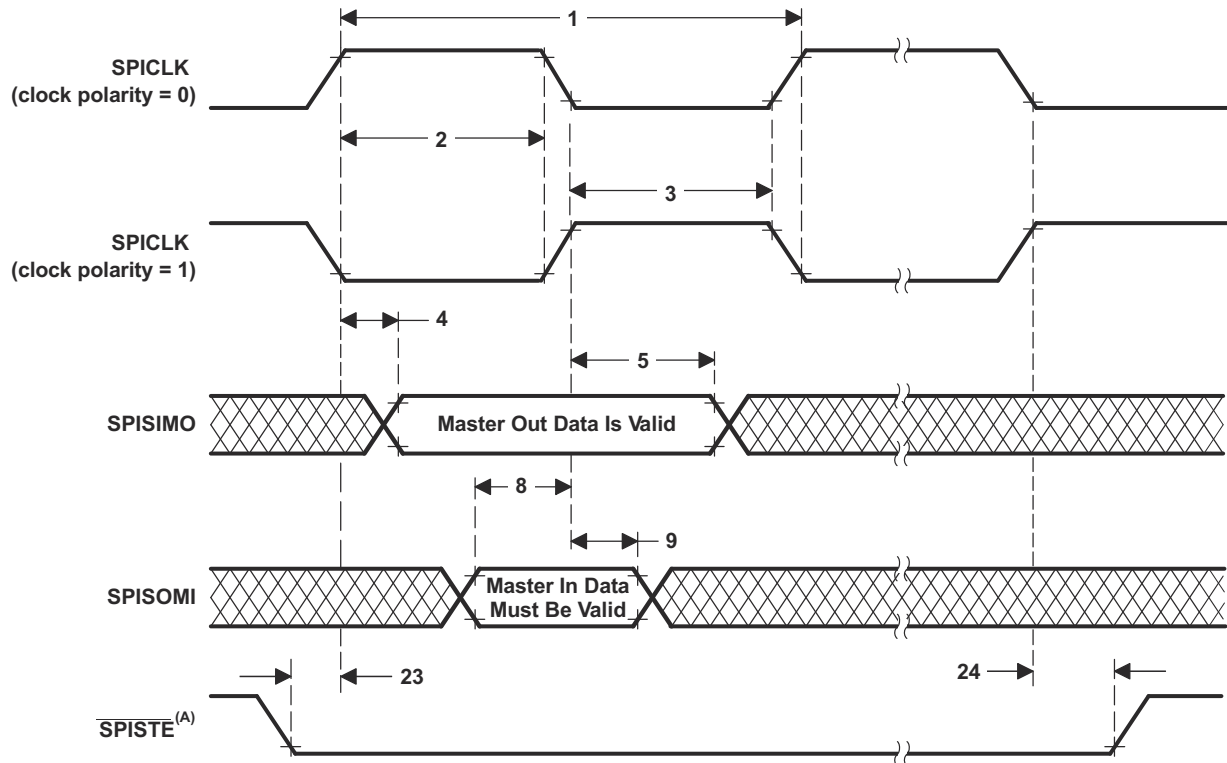
(3) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

6.16.6.1.3 SPI Master Mode Switching Characteristics - Clock Phase 1
over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER ^{(1) (2)} | | (BRR + 1) | MIN | MAX | UNIT |
|------------------------|------------------------------|---------------------------------------------------|-----------|-----------------------------------------|-----------------------------------------|------|
| General | | | | | | |
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ | $128t_{c(LSPCLK)}$ | ns |
| | | | Odd | $5t_{c(LSPCLK)}$ | $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPCH)M}$ | Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$ | |
| 3 | $t_{w(SPC2)M}$ | Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$ | |
| 23 | $t_{d(SPC)M}$ | Delay time, \overline{SPISTE} valid to SPICLK | Even, Odd | $2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$ | $2t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$ | ns |
| 24 | $t_{d(STE)M}$ | Delay time, SPICLK to \overline{SPISTE} invalid | Even | -3 | 3 | ns |
| | | | Odd | -3 | 3 | |
| High-Speed Mode | | | | | | |
| 4 | $t_{d(SIMO)M}$ | Delay time, SPISIMO valid to SPICLK | Even | $0.5t_{c(SPC)M} - 2$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 2$ | | |
| 5 | $t_{v(SIMO)M}$ | Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |
| Normal Mode | | | | | | |
| 4 | $t_{d(SIMO)M}$ | Delay time, SPISIMO valid to SPICLK | Even | $0.5t_{c(SPC)M} - 2$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 2$ | | |
| 5 | $t_{v(SIMO)M}$ | Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |

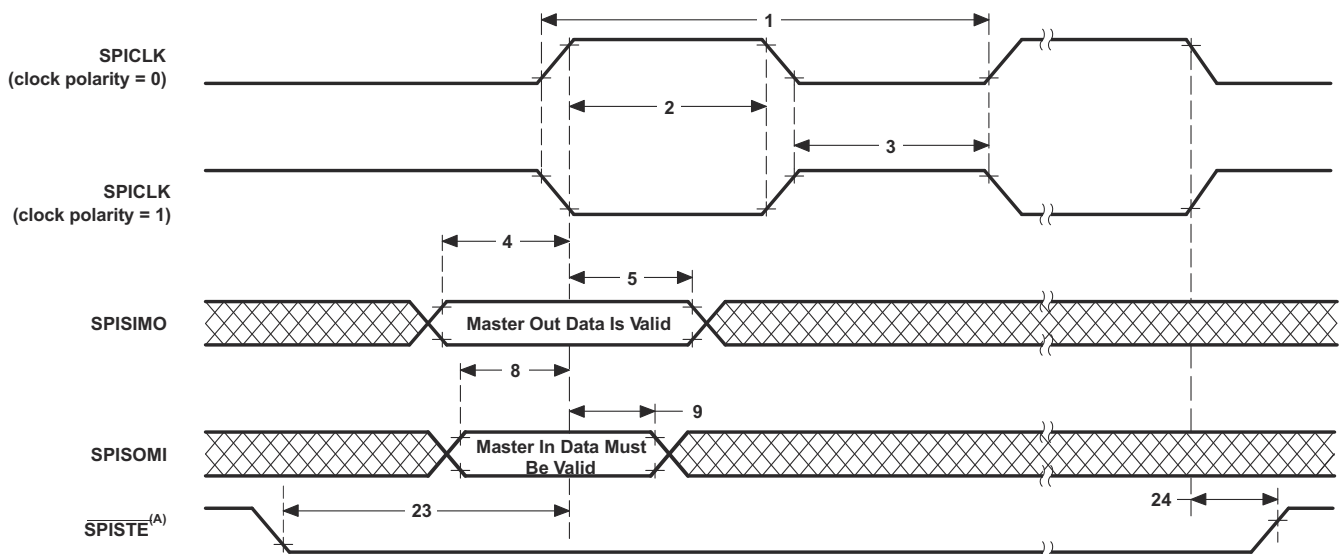
- (1) 10-pF load on pin for High-Speed Mode.
(2) 20-pF load on pin for Normal Mode.

6.16.6.1.4 SPI Master Mode Timing Diagrams



A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-70. SPI Master Mode External Timing (Clock Phase = 0)



A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-71. SPI Master Mode External Timing (Clock Phase = 1)

6.16.6.2 SPI Slave Mode Timings

The following section contains the SPI Slave Mode Timings. For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#).

6.16.6.2.1 SPI Slave Mode Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|-----------------|-----------------------------------------------------------------------|-----------------------|-----|------|
| 12 | $t_{c(SPC)S}$ | Cycle time, SPICLK | $4t_{c(SYSCLK)}$ | | ns |
| 13 | $t_{w(SPC1)S}$ | Pulse duration, SPICLK, first pulse | $2t_{c(SYSCLK)} - 1$ | | ns |
| 14 | $t_{w(SPC2)S}$ | Pulse duration, SPICLK, second pulse | $2t_{c(SYSCLK)} - 1$ | | ns |
| 19 | $t_{su(SIMO)S}$ | Setup time, SPISIMO valid before SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 20 | $t_{h(SIMO)S}$ | Hold time, SPISIMO valid after SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 25 | $t_{su(STE)S}$ | Setup time, \overline{SPISTE} valid before SPICLK (Clock Phase = 0) | $2t_{c(SYSCLK)} + 15$ | | ns |
| | | Setup time, \overline{SPISTE} valid before SPICLK (Clock Phase = 1) | $2t_{c(SYSCLK)} + 15$ | | ns |
| 26 | $t_{h(STE)S}$ | Hold time, \overline{SPISTE} invalid after SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |

6.16.6.2.2 SPI Slave Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|-----|--------------------------|----------------------------------------|-----|------|------|
| 15 | $t_{d(SOMI)S}$ | Delay time, SPICLK to SPISOMI valid | | 12.5 | ns |
| 16 | $t_{v(SOMI)S}$ | Valid time, SPISOMI valid after SPICLK | 0 | | ns |

(1) 20-pF load on pin.

6.16.6.2.3 SPI Slave Mode Timing Diagrams

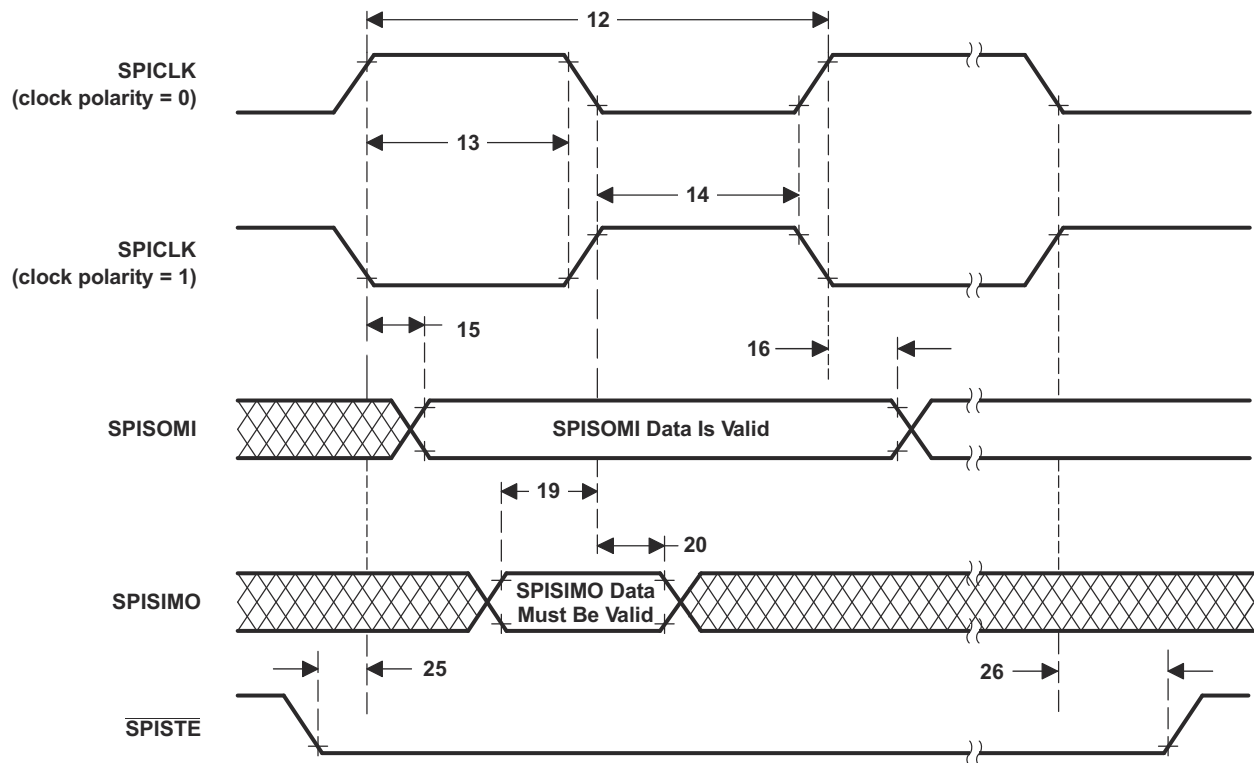


Figure 6-72. SPI Slave Mode External Timing (Clock Phase = 0)

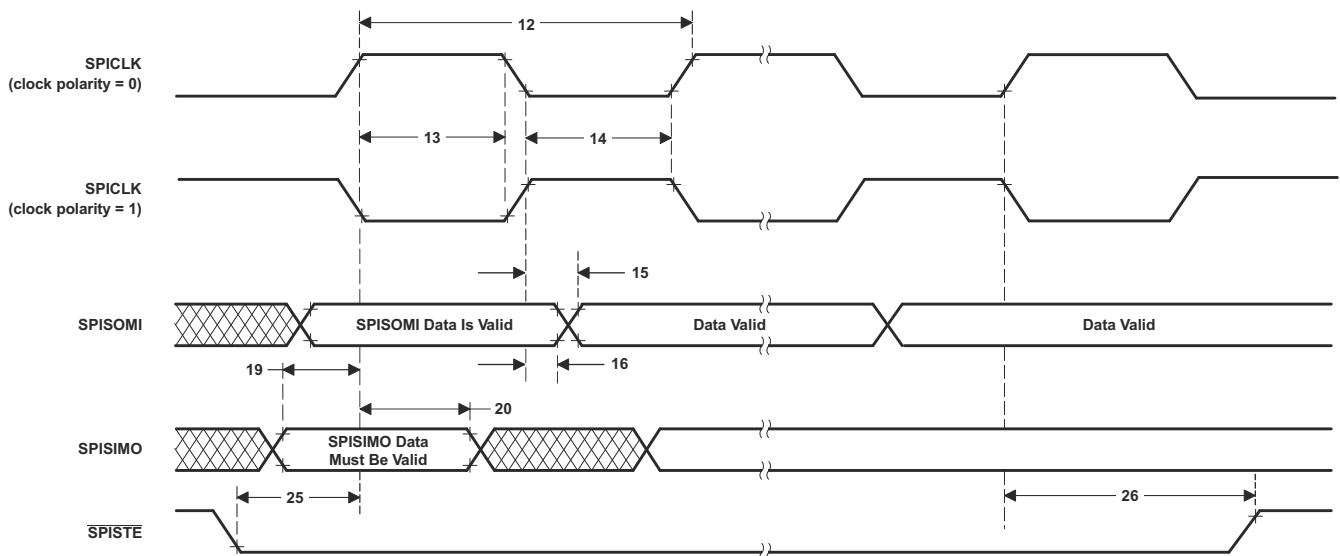


Figure 6-73. SPI Slave Mode External Timing (Clock Phase = 1)

6.16.7 Local Interconnect Network (LIN)

This device contains one Local Interconnect Network (LIN) module. The LIN module adheres to the LIN 2.1 standard as defined by the *LIN Specification Package Revision 2.1*. The LIN is a low-cost serial interface designed for applications where the CAN protocol may be too expensive to implement, such as small subnetworks for cabin comfort functions like interior lighting or window control in an automotive application.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-master and multiple-slave with a message identification for multicast transmission between any network nodes.

The LIN module can be programmed to work either as an SCI or as a LIN as the core of the module is an SCI. The hardware features of the SCI are augmented to achieve LIN compatibility. The SCI module is a universal asynchronous receiver-transmitter (UART) that implements the standard non-return-to-zero format.

Though the registers are common for LIN and SCI, the register descriptions have notes to identify the register/bit usage in different modes. Because of this, code written for this module cannot be directly ported to the stand-alone SCI module and vice versa.

The LIN module has the following features:

- Compatibility with LIN 1.3, 2.0 and 2.1 protocols
- Configurable baud rate up to 20 kbps (as per LIN 2.1 protocol)
- Two external pins: LINRX and LINTX
- Multibuffered receive and transmit units
- Identification masks for message filtering
- Automatic master header generation
 - Programmable synchronization break field
 - Synchronization field
 - Identifier field
- Slave automatic synchronization
 - Synchronization break detection
 - Optional baud rate update
 - Synchronization validation
- 2³¹ programmable transmission rates with 7 fractional bits
- Wakeup on LINRX dominant level from transceiver
- Automatic wake-up support
 - Wakeup signal generation
 - Expiration times on wakeup signals
- Automatic bus idle detection
- Error detection
 - Bit error
 - Bus error
 - No-response error
 - Checksum error
 - Synchronization field error
 - Parity error
- Two interrupt lines with priority encoding for:
 - Receive
 - Transmit
 - ID, error, and status
- Support for LIN 2.0 checksum
- Enhanced synchronizer finite state machine (FSM) support for frame processing
- Enhanced handling of extended frames
- Enhanced baud rate generator
- Update wakeup/go to sleep

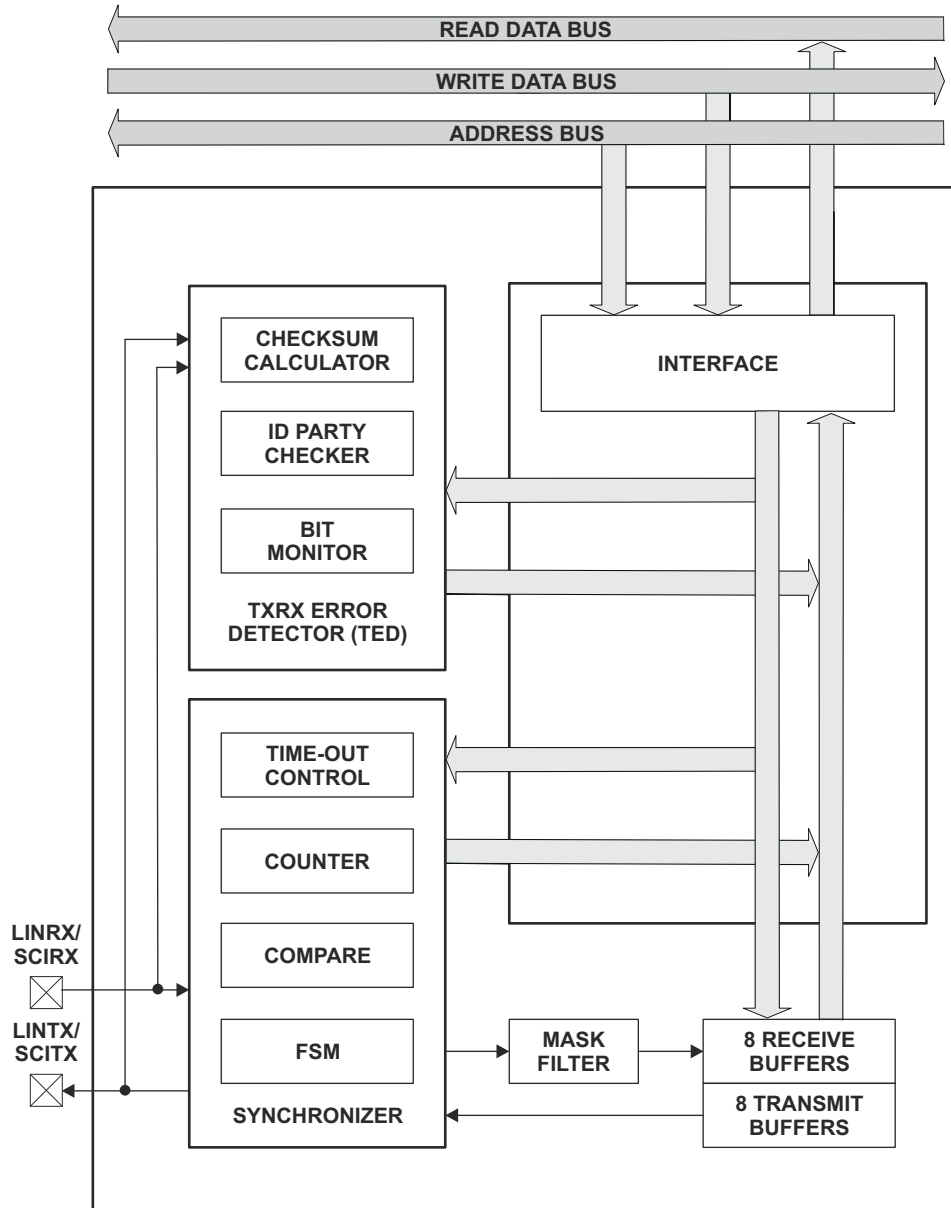


Figure 6-74. LIN Block Diagram

7 Detailed Description

7.1 Overview

The TMS320F280015x (F280015x) is a member of the cost-optimized C2000 real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics.

These include such [applications](#) as:

- [HVAC compressor module](#)
- [Headlight](#)
- [DC/DC converter](#)
- [Inverter & motor control](#)
- [On-board \(OBC\) & wireless charger](#)
- [Pump](#)
- [Industrial motor drives](#)
- [Motor control](#)
- [Digital power](#)
- [Sensing and signal processing](#)

TMS320F280015x has dual 32-bit C28x CPUs in Lockstep, enabling the device to achieve ASIL B functional safety device rating without much SW overhead. The [real-time control subsystem](#) is based on TI's 32-bit C28x DSP core, which provides 120 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the [Trigonometric Math Unit \(TMU\)](#) and [VCRC \(Cyclical Redundancy Check\) extended instruction sets](#), speeding up common algorithms key to real-time control systems.

The F280015x supports up to 256KB (128KW) of flash memory. Up to 36KB (18KW) of on-chip SRAM is also available to supplement the flash memory.

High-performance analog blocks are integrated on the F280015x real-time microcontroller (MCU) and are closely coupled with the processing and PWM units to provide optimal real-time signal chain performance. Fourteen PWM channels enable control of various power stages from a 3-phase inverter to power-factor correction and other advanced multilevel power topologies.

Interfacing is supported through various industry-standard communication ports (such as PMBUS, SPI, SCI, LIN, I2C, CAN and CAN FD) and offers [multiple pin-muxing options](#) for optimal signal placement.

Want to learn more about features that make C2000™ MCUs the right choice for your real-time control system? Check out [The Essential Guide for Developing With C2000™ Real-Time Microcontrollers](#) and visit the [C2000 real-time microcontrollers](#) page.

The [Getting Started With C2000™ Real-Time Control Microcontrollers \(MCUs\) Getting Started Guide](#) covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the [TMDSCNCD2800157](#) evaluation board and download [C2000Ware](#).

7.2 Functional Block Diagram

The [Functional Block Diagram](#) shows the CPU system and associated peripherals.

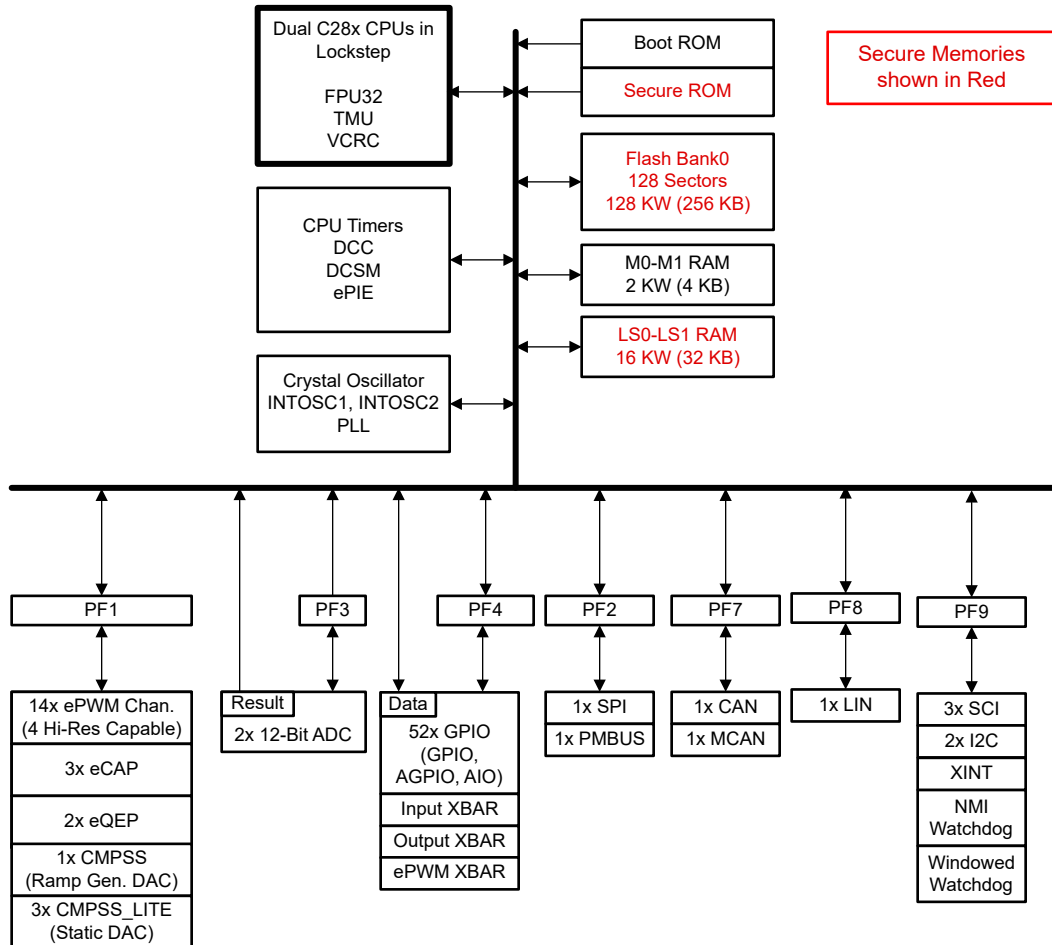


Figure 7-1. Functional Block Diagram

7.3 Memory

7.3.1 Memory Map

The Memory Map table describes the memory map. See the Memory Controller Module section of the System Control chapter in the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#).

Table 7-1. Memory Map

| MEMORY | SIZE | START ADDRESS | END ADDRESS | ECC/ PARITY | ACCESS PROTECTION | SECURITY |
|-------------------------------------------|-----------|---------------|-------------|-------------|-------------------|------------------|
| M0 RAM | 1K x 16 | 0x0000 0000 | 0x0000 03FF | ECC | Yes | - |
| M1 RAM | 1K x 16 | 0x0000 0400 | 0x0000 07FF | ECC | Yes | - |
| PieVectTable | 256 x 16 | 0x0000 0D00 | 0x0000 0DFF | - | - | - |
| LS0 RAM | 8K x 16 | 0x0000 8000 | 0x0000 9FFF | Parity | Yes | Yes |
| LS1 RAM | 8K x 16 | 0x0000 A000 | 0x0000 BFFF | Parity | Yes | Yes |
| TI OTP ¹ | 1.5K x 16 | 0x0007 1000 | 0x0007 15FF | ECC | - | Yes ² |
| User OTP | 1K x 16 | 0x0007 8000 | 0x0007 83FF | ECC | - | Yes ² |
| Flash | 128K x 16 | 0x0008 0000 | 0x0009 FFFF | ECC | - | Yes |
| Secure ROM | 7K x 16 | 0x003F 4000 | 0x003F 5BFF | Parity | - | Yes |
| CPU STL ROM | 9K x 16 | 0x003F 5C00 | 0x003F 7FFF | Parity | - | - |
| Boot ROM | 32K x 16 | 0x003F 8000 | 0x003F FFFF | Parity | - | - |
| Pie Vector Fetch Error (part of Boot ROM) | 1 x 16 | 0x003F FFBE | 0x003F FFBF | Parity | - | - |
| Default Vectors (part of Boot ROM) | 64 x 16 | 0x003F FFC0 | 0x003F FFFF | Parity | - | - |

(1) TI OTP is for TI internal use only.

(2) Only a subset is secure.

7.3.1.1 Dedicated RAM (Mx RAM)

This device has two dedicated RAM blocks: M0 and M1. M0 and M1 memories are small blocks of memory which are tightly coupled with the CPU. Only the CPU has access to these memories. No other masters have access to these memories.

All dedicated RAMs have the ECC feature.

7.3.1.2 Local Shared RAM (LSx RAM)

Local shared RAMs (LSx RAMs) are secure memories and have Parity. These memories are dedicated to the CPU.

7.3.2 Flash Memory Map

On the F280015x devices, one flash bank (256KB [128KW]) is available. Code to program the flash should be executed out of RAM, there should not be any kind of access to the flash bank when an erase or program operation is in progress.

Table 7-2. Flash Memory Map

| PART NUMBER | SECTOR | ADDRESS | | | ECC ADDRESS | | |
|-----------------------|-----------------------------------|-----------|-------------|-------------|-------------|-------------|-------------|
| | | SIZE | START | END | SIZE | START | END |
| OTP Sectors | | | | | | | |
| ALL | TI OTP Bank 0 (Unsecure) | 1520 x 16 | 0x0007 1000 | 0x0007 15EF | 128 x 16 | 0x0107 0200 | 0x0107 02BD |
| | TI OTP Bank 0 (Secure) | 16 x 16 | 0x0007 15F0 | 0x0007 15FF | 128 x 16 | 0x0107 02BE | 0x0107 02BF |
| | User configurable DCSM OTP Bank 0 | 1K x 16 | 0x0007 8000 | 0x0007 83FF | 128 x 16 | 0x0107 1000 | 0x0107 107F |
| Bank 0 Sectors | | | | | | | |
| ALL | Sector 0 | 1K x 16 | 0x0008 0000 | 0x0008 03FF | 128 x 16 | 0x0108 0000 | 0x0108 007F |
| | Sector 1 | 1K x 16 | 0x0008 0400 | 0x0008 07FF | 128 x 16 | 0x0108 0080 | 0x0108 00FF |
| | Sector 2 | 1K x 16 | 0x0008 0800 | 0x0008 0BFF | 128 x 16 | 0x0108 0100 | 0x0108 017F |
| | Sector 3 | 1K x 16 | 0x0008 0C00 | 0x0008 0FFF | 128 x 16 | 0x0108 0180 | 0x0108 01FF |
| | Sector 4 | 1K x 16 | 0x0008 1000 | 0x0008 13FF | 128 x 16 | 0x0108 0200 | 0x0108 027F |
| | Sector 5 | 1K x 16 | 0x0008 1400 | 0x0008 17FF | 128 x 16 | 0x0108 0280 | 0x0108 02FF |
| | Sector 6 | 1K x 16 | 0x0008 1800 | 0x0008 1BFF | 128 x 16 | 0x0108 0300 | 0x0108 037F |
| | Sector 7 | 1K x 16 | 0x0008 1C00 | 0x0008 1FFF | 128 x 16 | 0x0108 0380 | 0x0108 03FF |
| | Sector 8 | 1K x 16 | 0x0008 2000 | 0x0008 23FF | 128 x 16 | 0x0108 0400 | 0x0108 047F |
| | Sector 9 | 1K x 16 | 0x0008 2400 | 0x0008 27FF | 128 x 16 | 0x0108 0480 | 0x0108 04FF |
| | Sector 10 | 1K x 16 | 0x0008 2800 | 0x0008 2BFF | 128 x 16 | 0x0108 0500 | 0x0108 057F |
| | Sector 11 | 1K x 16 | 0x0008 2C00 | 0x0008 2FFF | 128 x 16 | 0x0108 0580 | 0x0108 05FF |
| | Sector 12 | 1K x 16 | 0x0008 3000 | 0x0008 33FF | 128 x 16 | 0x0108 0600 | 0x0108 067F |
| | Sector 13 | 1K x 16 | 0x0008 3400 | 0x0008 37FF | 128 x 16 | 0x0108 0680 | 0x0108 06FF |
| | Sector 14 | 1K x 16 | 0x0008 3800 | 0x0008 3BFF | 128 x 16 | 0x0108 0700 | 0x0108 077F |
| | Sector 15 | 1K x 16 | 0x0008 3C00 | 0x0008 3FFF | 128 x 16 | 0x0108 0780 | 0x0108 07FF |
| | Sector 16 | 1K x 16 | 0x0008 4000 | 0x0008 43FF | 128 x 16 | 0x0108 0800 | 0x0108 087F |
| | Sector 17 | 1K x 16 | 0x0008 4400 | 0x0008 47FF | 128 x 16 | 0x0108 0880 | 0x0108 08FF |
| | Sector 18 | 1K x 16 | 0x0008 4800 | 0x0008 4BFF | 128 x 16 | 0x0108 0900 | 0x0108 097F |
| | Sector 19 | 1K x 16 | 0x0008 4C00 | 0x0008 4FFF | 128 x 16 | 0x0108 0980 | 0x0108 09FF |
| | Sector 20 | 1K x 16 | 0x0008 5000 | 0x0008 53FF | 128 x 16 | 0x0108 0A00 | 0x0108 0A7F |
| | Sector 21 | 1K x 16 | 0x0008 5400 | 0x0008 57FF | 128 x 16 | 0x0108 0A80 | 0x0108 0AFF |
| | Sector 22 | 1K x 16 | 0x0008 5800 | 0x0008 5BFF | 128 x 16 | 0x0108 0B00 | 0x0108 0B7F |
| | Sector 23 | 1K x 16 | 0x0008 5C00 | 0x0008 5FFF | 128 x 16 | 0x0108 0B80 | 0x0108 0BFF |
| | Sector 24 | 1K x 16 | 0x0008 6000 | 0x0008 63FF | 128 x 16 | 0x0108 0C00 | 0x0108 0C7F |
| | Sector 25 | 1K x 16 | 0x0008 6400 | 0x0008 67FF | 128 x 16 | 0x0108 0C80 | 0x0108 0CFF |
| | Sector 26 | 1K x 16 | 0x0008 6800 | 0x0008 6BFF | 128 x 16 | 0x0108 0D00 | 0x0108 0D7F |
| | Sector 27 | 1K x 16 | 0x0008 6C00 | 0x0008 6FFF | 128 x 16 | 0x0108 0D80 | 0x0108 0DFF |
| | Sector 28 | 1K x 16 | 0x0008 7000 | 0x0008 73FF | 128 x 16 | 0x0108 0E00 | 0x0108 0E7F |
| | Sector 29 | 1K x 16 | 0x0008 7400 | 0x0008 77FF | 128 x 16 | 0x0108 0E80 | 0x0108 0EFF |
| | Sector 30 | 1K x 16 | 0x0008 7800 | 0x0008 7BFF | 128 x 16 | 0x0108 0F00 | 0x0108 0F7F |
| | Sector 31 | 1K x 16 | 0x0008 7C00 | 0x0008 7FFF | 128 x 16 | 0x0108 0F80 | 0x0108 0FFF |

Table 7-2. Flash Memory Map (continued)

| PART NUMBER | SECTOR | ADDRESS | | | ECC ADDRESS | | |
|---------------------------------------------------------------------------------------|-----------|---------|-------------|-------------|-------------|-------------|-------------|
| | | SIZE | START | END | SIZE | START | END |
| F2800157-Q1, F2800157, F2800156-Q1, F2800155-Q1, F2800155, F2800154-Q1 | Sector 32 | 1K x 16 | 0x0008 8000 | 0x0008 83FF | 128 x 16 | 0x0108 1000 | 0x0108 107F |
| | Sector 33 | 1K x 16 | 0x0008 8400 | 0x0008 87FF | 128 x 16 | 0x0108 1080 | 0x0108 10FF |
| | Sector 34 | 1K x 16 | 0x0008 8800 | 0x0008 8BFF | 128 x 16 | 0x0108 1100 | 0x0108 117F |
| | Sector 35 | 1K x 16 | 0x0008 8C00 | 0x0008 8FFF | 128 x 16 | 0x0108 1180 | 0x0108 11FF |
| | Sector 36 | 1K x 16 | 0x0008 9000 | 0x0008 93FF | 128 x 16 | 0x0108 1200 | 0x0108 127F |
| | Sector 37 | 1K x 16 | 0x0008 9400 | 0x0008 97FF | 128 x 16 | 0x0108 1280 | 0x0108 12FF |
| | Sector 38 | 1K x 16 | 0x0008 9800 | 0x0008 9BFF | 128 x 16 | 0x0108 1300 | 0x0108 137F |
| | Sector 39 | 1K x 16 | 0x0008 9C00 | 0x0008 9FFF | 128 x 16 | 0x0108 1380 | 0x0108 13FF |
| | Sector 40 | 1K x 16 | 0x0008 A000 | 0x0008 A3FF | 128 x 16 | 0x0108 1400 | 0x0108 147F |
| | Sector 41 | 1K x 16 | 0x0008 A400 | 0x0008 A7FF | 128 x 16 | 0x0108 1480 | 0x0108 14FF |
| | Sector 42 | 1K x 16 | 0x0008 A800 | 0x0008 ABFF | 128 x 16 | 0x0108 1500 | 0x0108 157F |
| | Sector 43 | 1K x 16 | 0x0008 AC00 | 0x0008 AFFF | 128 x 16 | 0x0108 1580 | 0x0108 15FF |
| | Sector 44 | 1K x 16 | 0x0008 B000 | 0x0008 B3FF | 128 x 16 | 0x0108 1600 | 0x0108 167F |
| | Sector 45 | 1K x 16 | 0x0008 B400 | 0x0008 B7FF | 128 x 16 | 0x0108 1680 | 0x0108 16FF |
| | Sector 46 | 1K x 16 | 0x0008 B800 | 0x0008 BBFF | 128 x 16 | 0x0108 1700 | 0x0108 177F |
| | Sector 47 | 1K x 16 | 0x0008 BC00 | 0x0008 BFFF | 128 x 16 | 0x0108 1780 | 0x0108 17FF |
| | Sector 48 | 1K x 16 | 0x0008 C000 | 0x0008 C3FF | 128 x 16 | 0x0108 1800 | 0x0108 187F |
| | Sector 49 | 1K x 16 | 0x0008 C400 | 0x0008 C7FF | 128 x 16 | 0x0108 1880 | 0x0108 18FF |
| | Sector 50 | 1K x 16 | 0x0008 C800 | 0x0008 CBFF | 128 x 16 | 0x0108 1900 | 0x0108 197F |
| | Sector 51 | 1K x 16 | 0x0008 CC00 | 0x0008 CFFF | 128 x 16 | 0x0108 1980 | 0x0108 19FF |
| | Sector 52 | 1K x 16 | 0x0008 D000 | 0x0008 D3FF | 128 x 16 | 0x0108 1A00 | 0x0108 1A7F |
| | Sector 53 | 1K x 16 | 0x0008 D400 | 0x0008 D7FF | 128 x 16 | 0x0108 1A80 | 0x0108 1AFF |
| | Sector 54 | 1K x 16 | 0x0008 D800 | 0x0008 DBFF | 128 x 16 | 0x0108 1B00 | 0x0108 1B7F |
| | Sector 55 | 1K x 16 | 0x0008 DC00 | 0x0008 DFFF | 128 x 16 | 0x0108 1B80 | 0x0108 1BFF |
| | Sector 56 | 1K x 16 | 0x0008 E000 | 0x0008 E3FF | 128 x 16 | 0x0108 1C00 | 0x0108 1C7F |
| | Sector 57 | 1K x 16 | 0x0008 E400 | 0x0008 E7FF | 128 x 16 | 0x0108 1C80 | 0x0108 1CFF |
| | Sector 58 | 1K x 16 | 0x0008 E800 | 0x0008 EBFF | 128 x 16 | 0x0108 1D00 | 0x0108 1D7F |
| | Sector 59 | 1K x 16 | 0x0008 EC00 | 0x0008 EFFF | 128 x 16 | 0x0108 1D80 | 0x0108 1DFF |
| | Sector 60 | 1K x 16 | 0x0008 F000 | 0x0008 F3FF | 128 x 16 | 0x0108 1E00 | 0x0108 1E7F |
| | Sector 61 | 1K x 16 | 0x0008 F400 | 0x0008 F7FF | 128 x 16 | 0x0108 1E80 | 0x0108 1EFF |
| | Sector 62 | 1K x 16 | 0x0008 F800 | 0x0008 FBFF | 128 x 16 | 0x0108 1F00 | 0x0108 1F7F |
| | Sector 63 | 1K x 16 | 0x0008 FC00 | 0x0008 FFFF | 128 x 16 | 0x0108 1F80 | 0x0108 1FFF |

Table 7-2. Flash Memory Map (continued)

| PART NUMBER | SECTOR | ADDRESS | | | ECC ADDRESS | | |
|------------------------------------------|-----------|---------|-------------|-------------|-------------|-------------|-------------|
| | | SIZE | START | END | SIZE | START | END |
| F2800157-Q1, F2800157, F2800156-Q1 | Sector 64 | 1K x 16 | 0x0009 0000 | 0x0009 03FF | 128 x 16 | 0x0108 2000 | 0x0108 207F |
| | Sector 65 | 1K x 16 | 0x0009 0400 | 0x0009 07FF | 128 x 16 | 0x0108 2080 | 0x0108 20FF |
| | Sector 66 | 1K x 16 | 0x0009 0800 | 0x0009 0BFF | 128 x 16 | 0x0108 2100 | 0x0108 217F |
| | Sector 67 | 1K x 16 | 0x0009 0C00 | 0x0009 0FFF | 128 x 16 | 0x0108 2180 | 0x0108 21FF |
| | Sector 68 | 1K x 16 | 0x0009 1000 | 0x0009 13FF | 128 x 16 | 0x0108 2200 | 0x0108 227F |
| | Sector 69 | 1K x 16 | 0x0009 1400 | 0x0009 17FF | 128 x 16 | 0x0108 2280 | 0x0108 22FF |
| | Sector 70 | 1K x 16 | 0x0009 1800 | 0x0009 1BFF | 128 x 16 | 0x0108 2300 | 0x0108 237F |
| | Sector 71 | 1K x 16 | 0x0009 1C00 | 0x0009 1FFF | 128 x 16 | 0x0108 2380 | 0x0108 23FF |
| | Sector 72 | 1K x 16 | 0x0009 2000 | 0x0009 23FF | 128 x 16 | 0x0108 2400 | 0x0108 247F |
| | Sector 73 | 1K x 16 | 0x0009 2400 | 0x0009 27FF | 128 x 16 | 0x0108 2480 | 0x0108 24FF |
| | Sector 74 | 1K x 16 | 0x0009 2800 | 0x0009 2BFF | 128 x 16 | 0x0108 2500 | 0x0108 257F |
| | Sector 75 | 1K x 16 | 0x0009 2C00 | 0x0009 2FFF | 128 x 16 | 0x0108 2580 | 0x0108 25FF |
| | Sector 76 | 1K x 16 | 0x0009 3000 | 0x0009 33FF | 128 x 16 | 0x0108 2600 | 0x0108 267F |
| | Sector 77 | 1K x 16 | 0x0009 3400 | 0x0009 37FF | 128 x 16 | 0x0108 2680 | 0x0108 26FF |
| | Sector 78 | 1K x 16 | 0x0009 3800 | 0x0009 3BFF | 128 x 16 | 0x0108 2700 | 0x0108 277F |
| | Sector 79 | 1K x 16 | 0x0009 3C00 | 0x0009 3FFF | 128 x 16 | 0x0108 2780 | 0x0108 27FF |
| | Sector 80 | 1K x 16 | 0x0009 4000 | 0x0009 43FF | 128 x 16 | 0x0108 2800 | 0x0108 287F |
| | Sector 81 | 1K x 16 | 0x0009 4400 | 0x0009 47FF | 128 x 16 | 0x0108 2880 | 0x0108 28FF |
| | Sector 82 | 1K x 16 | 0x0009 4800 | 0x0009 4BFF | 128 x 16 | 0x0108 2900 | 0x0108 297F |
| | Sector 83 | 1K x 16 | 0x0009 4C00 | 0x0009 4FFF | 128 x 16 | 0x0108 2980 | 0x0108 29FF |
| | Sector 84 | 1K x 16 | 0x0009 5000 | 0x0009 53FF | 128 x 16 | 0x0108 2A00 | 0x0108 2A7F |
| | Sector 85 | 1K x 16 | 0x0009 5400 | 0x0009 57FF | 128 x 16 | 0x0108 2A80 | 0x0108 2AFF |
| | Sector 86 | 1K x 16 | 0x0009 5800 | 0x0009 5BFF | 128 x 16 | 0x0108 2B00 | 0x0108 2B7F |
| | Sector 87 | 1K x 16 | 0x0009 5C00 | 0x0009 5FFF | 128 x 16 | 0x0108 2B80 | 0x0108 2BFF |
| | Sector 88 | 1K x 16 | 0x0009 6000 | 0x0009 63FF | 128 x 16 | 0x0108 2C00 | 0x0108 2C7F |
| | Sector 89 | 1K x 16 | 0x0009 6400 | 0x0009 67FF | 128 x 16 | 0x0108 2C80 | 0x0108 2CFF |
| | Sector 90 | 1K x 16 | 0x0009 6800 | 0x0009 6BFF | 128 x 16 | 0x0108 2D00 | 0x0108 2D7F |
| | Sector 91 | 1K x 16 | 0x0009 6C00 | 0x0009 6FFF | 128 x 16 | 0x0108 2D80 | 0x0108 2DFF |
| | Sector 92 | 1K x 16 | 0x0009 7000 | 0x0009 73FF | 128 x 16 | 0x0108 2E00 | 0x0108 2E7F |
| | Sector 93 | 1K x 16 | 0x0009 7400 | 0x0009 77FF | 128 x 16 | 0x0108 2E80 | 0x0108 2EFF |
| | Sector 94 | 1K x 16 | 0x0009 7800 | 0x0009 7BFF | 128 x 16 | 0x0108 2F00 | 0x0108 2F7F |
| | Sector 95 | 1K x 16 | 0x0009 7C00 | 0x0009 7FFF | 128 x 16 | 0x0108 2F80 | 0x0108 2FFF |

Table 7-2. Flash Memory Map (continued)

| PART NUMBER | SECTOR | ADDRESS | | | ECC ADDRESS | | |
|------------------------------------------|------------|-------------|-------------|-------------|-------------|-------------|-------------|
| | | SIZE | START | END | SIZE | START | END |
| F2800157-Q1, F2800157, F2800156-Q1 | Sector 96 | 1K x 16 | 0x0009 8000 | 0x0009 83FF | 128 x 16 | 0x0108 3000 | 0x0108 307F |
| | Sector 97 | 1K x 16 | 0x0009 8400 | 0x0009 87FF | 128 x 16 | 0x0108 3080 | 0x0108 30FF |
| | Sector 98 | 1K x 16 | 0x0009 8800 | 0x0009 8BFF | 128 x 16 | 0x0108 3100 | 0x0108 317F |
| | Sector 99 | 1K x 16 | 0x0009 8C00 | 0x0009 8FFF | 128 x 16 | 0x0108 3180 | 0x0108 31FF |
| | Sector 100 | 1K x 16 | 0x0009 9000 | 0x0009 93FF | 128 x 16 | 0x0108 3200 | 0x0108 327F |
| | Sector 101 | 1K x 16 | 0x0009 9400 | 0x0009 97FF | 128 x 16 | 0x0108 3280 | 0x0108 32FF |
| | Sector 102 | 1K x 16 | 0x0009 9800 | 0x0009 9BFF | 128 x 16 | 0x0108 3300 | 0x0108 337F |
| | Sector 103 | 1K x 16 | 0x0009 9C00 | 0x0009 9FFF | 128 x 16 | 0x0108 3380 | 0x0108 33FF |
| | Sector 104 | 1K x 16 | 0x0009 A000 | 0x0009 A3FF | 128 x 16 | 0x0108 3400 | 0x0108 347F |
| | Sector 105 | 1K x 16 | 0x0009 A400 | 0x0009 A7FF | 128 x 16 | 0x0108 3480 | 0x0108 34FF |
| | Sector 106 | 1K x 16 | 0x0009 A800 | 0x0009 ABFF | 128 x 16 | 0x0108 3500 | 0x0108 357F |
| | Sector 107 | 1K x 16 | 0x0009 AC00 | 0x0009 AFFF | 128 x 16 | 0x0108 3580 | 0x0108 35FF |
| | Sector 108 | 1K x 16 | 0x0009 B000 | 0x0009 B3FF | 128 x 16 | 0x0108 3600 | 0x0108 367F |
| | Sector 109 | 1K x 16 | 0x0009 B400 | 0x0009 B7FF | 128 x 16 | 0x0108 3680 | 0x0108 36FF |
| | Sector 110 | 1K x 16 | 0x0009 B800 | 0x0009 BBFF | 128 x 16 | 0x0108 3700 | 0x0108 377F |
| | Sector 111 | 1K x 16 | 0x0009 BC00 | 0x0009 BFFF | 128 x 16 | 0x0108 3780 | 0x0108 37FF |
| | Sector 112 | 1K x 16 | 0x0009 C000 | 0x0009 C3FF | 128 x 16 | 0x0108 3800 | 0x0108 387F |
| | Sector 113 | 1K x 16 | 0x0009 C400 | 0x0009 C7FF | 128 x 16 | 0x0108 3880 | 0x0108 38FF |
| | Sector 114 | 1K x 16 | 0x0009 C800 | 0x0009 CBFF | 128 x 16 | 0x0108 3900 | 0x0108 397F |
| | Sector 115 | 1K x 16 | 0x0009 CC00 | 0x0009 CFFF | 128 x 16 | 0x0108 3980 | 0x0108 39FF |
| | Sector 116 | 1K x 16 | 0x0009 D000 | 0x0009 D3FF | 128 x 16 | 0x0108 3A00 | 0x0108 3A7F |
| | Sector 117 | 1K x 16 | 0x0009 D400 | 0x0009 D7FF | 128 x 16 | 0x0108 3A80 | 0x0108 3AFF |
| | Sector 118 | 1K x 16 | 0x0009 D800 | 0x0009 DBFF | 128 x 16 | 0x0108 3B00 | 0x0108 3B7F |
| | Sector 119 | 1K x 16 | 0x0009 DC00 | 0x0009 DFFF | 128 x 16 | 0x0108 3B80 | 0x0108 3BFF |
| | Sector 120 | 1K x 16 | 0x0009 E000 | 0x0009 E3FF | 128 x 16 | 0x0108 3C00 | 0x0108 3C7F |
| | Sector 121 | 1K x 16 | 0x0009 E400 | 0x0009 E7FF | 128 x 16 | 0x0108 3C80 | 0x0108 3CFF |
| | Sector 122 | 1K x 16 | 0x0009 E800 | 0x0009 EBFF | 128 x 16 | 0x0108 3D00 | 0x0108 3D7F |
| Sector 123 | 1K x 16 | 0x0009 EC00 | 0x0009 EFFF | 128 x 16 | 0x0108 3D80 | 0x0108 3DFF | |
| Sector 124 | 1K x 16 | 0x0009 F000 | 0x0009 F3FF | 128 x 16 | 0x0108 3E00 | 0x0108 3E7F | |
| Sector 125 | 1K x 16 | 0x0009 F400 | 0x0009 F7FF | 128 x 16 | 0x0108 3E80 | 0x0108 3EFF | |
| Sector 126 | 1K x 16 | 0x0009 F800 | 0x0009 FBFF | 128 x 16 | 0x0108 3F00 | 0x0108 3F7F | |
| Sector 127 | 1K x 16 | 0x0009 FC00 | 0x0009 FFFF | 128 x 16 | 0x0108 3F80 | 0x0108 3FFF | |

7.3.3 Peripheral Registers Memory Map

Table 7-3. Peripheral Registers Memory Map

| Bit Field Name | | DriverLib Name | Base Address | Pipeline Protected |
|---------------------------------|---------------------|-------------------|--------------|--------------------|
| Instance | Structure | | | |
| Peripheral Frame 0 (PF0) | | | | |
| - | - | M0_RAM_BASE | 0x0000_0000 | - |
| - | - | M1_RAM_BASE | 0x0000_0400 | - |
| AdcaResultRegs | ADC_RESULT_REGS | ADCARESULT_BASE | 0x0000_0B00 | - |
| AdccResultRegs | ADC_RESULT_REGS | ADCCRESULT_BASE | 0x0000_0B40 | - |
| CpuTimer0Regs | CPUTIMER_REGS | CPUTIMER0_BASE | 0x0000_0C00 | - |
| CpuTimer1Regs | CPUTIMER_REGS | CPUTIMER1_BASE | 0x0000_0C08 | - |
| CpuTimer2Regs | CPUTIMER_REGS | CPUTIMER2_BASE | 0x0000_0C10 | - |
| PieCtrlRegs | PIE_CTRL_REGS | PIECTRL_BASE | 0x0000_0CE0 | - |
| PieVectTable | PIE_VECT_TABLE | PIEVECTTABLE_BASE | 0x0000_0D00 | - |
| - | - | LS0_RAM_BASE | 0x0000_8000 | - |
| - | - | LS1_RAM_BASE | 0x0000_A000 | - |
| UidRegs | UID_REGS | UID_BASE | 0x0007_1140 | - |
| DcsmZ1OtpRegs | DCSM_Z1_OTP | DCSM_Z1OTP_BASE | 0x0007_8000 | - |
| DcsmZ2OtpRegs | DCSM_Z2_OTP | DCSM_Z2OTP_BASE | 0x0007_8200 | - |
| Peripheral Frame 1 (PF1) | | | | |
| EPwm1Regs | EPWM_REGS | EPWM1_BASE | 0x0000_4000 | YES |
| EPwm2Regs | EPWM_REGS | EPWM2_BASE | 0x0000_4100 | YES |
| EPwm3Regs | EPWM_REGS | EPWM3_BASE | 0x0000_4200 | YES |
| EPwm4Regs | EPWM_REGS | EPWM4_BASE | 0x0000_4300 | YES |
| EPwm5Regs | EPWM_REGS | EPWM5_BASE | 0x0000_4400 | YES |
| EPwm6Regs | EPWM_REGS | EPWM6_BASE | 0x0000_4500 | YES |
| EPwm7Regs | EPWM_REGS | EPWM7_BASE | 0x0000_4600 | YES |
| EQep1Regs | EQEP_REGS | EQEP1_BASE | 0x0000_5100 | YES |
| EQep2Regs | EQEP_REGS | EQEP2_BASE | 0x0000_5140 | YES |
| ECap1Regs | ECAP_REGS | ECAP1_BASE | 0x0000_5200 | YES |
| ECap2Regs | ECAP_REGS | ECAP2_BASE | 0x0000_5240 | YES |
| ECap3Regs | ECAP_REGS | ECAP3_BASE | 0x0000_5280 | YES |
| Cmpss1Regs | CMPSS_REGS | CMPSS1_BASE | 0x0000_5500 | YES |
| CmpssLite2Regs | CMPSS_LITE_REGS | CMPSSLITE2_BASE | 0x0000_5540 | YES |
| CmpssLite3Regs | CMPSS_LITE_REGS | CMPSSLITE3_BASE | 0x0000_5580 | YES |
| CmpssLite4Regs | CMPSS_LITE_REGS | CMPSSLITE4_BASE | 0x0000_55C0 | YES |
| Peripheral Frame 2 (PF2) | | | | |
| SpiaRegs | SPI_REGS | SPIA_BASE | 0x0000_6100 | YES |
| PmbusaRegs | PMBUS_REGS | PMBUSA_BASE | 0x0000_6400 | YES |
| Peripheral Frame 3 (PF3) | | | | |
| AdcaRegs | ADC_REGS | ADCA_BASE | 0x0000_7400 | YES |
| AdccRegs | ADC_REGS | ADCC_BASE | 0x0000_7500 | YES |
| Peripheral Frame 4 (PF4) | | | | |
| InputXbarRegs | INPUT_XBAR_REGS | INPUTXBAR_BASE | 0x0000_7900 | YES |
| XbarRegs | XBAR_REGS | XBAR_BASE | 0x0000_7920 | YES |
| SyncSocRegs | SYNC_SOC_REGS | SYNCSOC_BASE | 0x0000_7940 | YES |
| EPwmXbarRegs | EPWM_XBAR_REGS | EPWMXBAR_BASE | 0x0000_7A00 | YES |
| OutputXbarRegs | OUTPUT_XBAR_REGS | OUTPUTXBAR_BASE | 0x0000_7A80 | YES |
| GpioCtrlRegs | GPIO_CTRL_REGS | GPIOCTRL_BASE | 0x0000_7C00 | YES |
| GpioDataRegs | GPIO_DATA_REGS | GPIODATA_BASE | 0x0000_7F00 | YES |
| GpioDataReadRegs | GPIO_DATA_READ_REGS | GPIODATAREAD_BASE | 0x0000_7F80 | YES |

Table 7-3. Peripheral Registers Memory Map (continued)

| Bit Field Name | | DriverLib Name | Base Address | Pipeline Protected |
|---------------------------------|------------------------|-----------------------|--------------|--------------------|
| Instance | Structure | | | |
| DevCfgRegs | DEV_CFG_REGS | DEVCFG_BASE | 0x0005_D000 | YES |
| ClkCfgRegs | CLK_CFG_REGS | CLKCFG_BASE | 0x0005_D200 | YES |
| CpuSysRegs | CPU_SYS_REGS | CPUSYS_BASE | 0x0005_D300 | YES |
| SysStatusRegs | SYS_STATUS_REGS | SYSSTAT_BASE | 0x0005_D400 | YES |
| AnalogSubsysRegs | ANALOG_SUBSYS_REGS | ANALOGSUBSYS_BASE | 0x0005_D700 | YES |
| Peripheral Frame 6 (PF6) | | | | |
| Epg1Regs | EPG_REGS | EPG1_BASE | 0x0005_EC00 | YES |
| Epg1MuxRegs | EPG_MUX_REGS | EPG1MUX_BASE | 0x0005_ECD0 | YES |
| DcsmZ1Regs | DCSM_Z1_REGS | DCSM_Z1_BASE | 0x0005_F000 | YES |
| DcsmZ2Regs | DCSM_Z2_REGS | DCSM_Z2_BASE | 0x0005_F080 | YES |
| DcsmCommonRegs | DCSM_COMMON_REGS | DCSMCOMMON_BASE | 0x0005_F0C0 | YES |
| MemCfgRegs | MEM_CFG_REGS | MEMCFG_BASE | 0x0005_F400 | YES |
| AccessProtectionRegs | ACCESS_PROTECTION_REGS | ACCESSPROTECTION_BASE | 0x0005_F500 | YES |
| MemoryErrorRegs | MEMORY_ERROR_REGS | MEMORYERROR_BASE | 0x0005_F540 | YES |
| TestErrorRegs | TEST_ERROR_REGS | TESTERROR_BASE | 0x0005_F590 | YES |
| Flash0CtrlRegs | FLASH_CTRL_REGS | FLASH0CTRL_BASE | 0x0005_F800 | YES |
| Flash0EccRegs | FLASH_ECC_REGS | FLASH0ECC_BASE | 0x0005_FB00 | YES |
| Peripheral Frame 7 (PF7) | | | | |
| CanaRegs | CAN_REGS | CANA_BASE | 0x0004_8000 | YES |
| - | - | CANA_MSG_RAM_BASE | 0x0004_9000 | YES |
| LCMCPU1Regs | LCM_REGS | LCM_CPU1_BASE | 0x0004_C000 | YES |
| - | - | MCANA_DRIVER_BASE | 0x0005_8000 | YES |
| McanaSsRegs | MCANSS_REGS | MCANASS_BASE | 0x0005_C400 | YES |
| McanaRegs | MCAN_REGS | MCANA_BASE | 0x0005_C600 | YES |
| McanaErrorRegs | MCAN_ERROR_REGS | MCANA_ERROR_BASE | 0x0005_C800 | YES |
| MpostRegs | MPOST_REGS | MPOST_BASE | 0x0005_E200 | YES |
| Dcc0Regs | DCC_REGS | DCC0_BASE | 0x0005_E700 | YES |
| Peripheral Frame 8 (PF8) | | | | |
| LinaRegs | LIN_REGS | LINA_BASE | 0x0000_6A00 | YES |
| Peripheral Frame 9 (PF9) | | | | |
| WdRegs | WD_REGS | WD_BASE | 0x0000_7000 | YES |
| NmiIntruptRegs | NMI_INTRUPT_REGS | NMI_BASE | 0x0000_7060 | YES |
| XintRegs | XINT_REGS | XINT_BASE | 0x0000_7070 | YES |
| SciaRegs | SCI_REGS | SCIA_BASE | 0x0000_7200 | YES |
| ScibRegs | SCI_REGS | SCIB_BASE | 0x0000_7210 | YES |
| ScicRegs | SCI_REGS | SCIC_BASE | 0x0000_7220 | YES |
| I2caRegs | I2C_REGS | I2CA_BASE | 0x0000_7300 | YES |
| I2cbRegs | I2C_REGS | I2CB_BASE | 0x0000_7340 | YES |

7.4 Identification

Table 7-4 lists the Device Identification Registers. Additional information on these device identification registers can be found in the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#).

Table 7-4. Device Identification Registers

| NAME | ADDRESS | SIZE (x16) | DESCRIPTION | |
|-------------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|
| | | | Bits | Options |
| PARTIDL | 0x0005 D008 | 2 | 14-13 INSTASPIN | 1 = InstaSPIN-FOC 2 = NONE 3 = NONE |
| | | | 10-8 PIN_COUNT | 2 = 64 pin (QFP) 3 = 80 pin (QFP) 4 = 48 pin (QFP) 5 = 32 pin (QFN) 7 = 48 pin (QFN) 8 = 64 pin (QFP, with VREGENZ) |
| | | | 7-6 QUAL | 0 = Engineering sample (TMX) 1 = Pilot production (TMP) 2 = Fully qualified (TMS) |
| PARTIDH | 0x0005 D00A | 2 | Device part identification number TMS320F2800157 0x07FF 0500 TMS320F2800156 0x07FE 0500 TMS320F2800155 0x07FD 0500 TMS320F2800154 0x07FC 0500 TMS320F2800153 0x07FB 0500 TMS320F2800152 0x07FA 0500 | |
| REVID | 0x0005 D00C | 2 | Silicon revision number Revision 0 0x0000 0001 Revision A 0x0000 0002 Revision B 0x0000 0003 | |
| UID_UNIQUE0 | 0x0007 114A | 2 | Unique identification number. This number is different on each individual device with the same PARTIDH. This unique number can be used as a serial number in the application. This number is present only on TMS devices. | |
| UID_UNIQUE1 | 0x0007 114C | 2 | Unique identification number. This number is different on each individual device with the same PARTIDH. This unique number can be used as a serial number in the application. This number is present only on TMS devices. | |

7.5 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the [TMS320C28x CPU and Instruction Set Reference Guide](#).

7.5.1 Floating-Point Unit (FPU)

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating-point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the RB, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

For more information on the C28x Floating Point Unit (FPU), see the [TMS320C28x Extended Instruction Sets Technical Reference Manual](#).

7.5.2 Trigonometric Math Unit (TMU)

The trigonometric math unit (TMU) extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in [Table 7-5](#).

Table 7-5. TMU Supported Instructions

| Instructions | C Equivalent Operation | Pipeline Cycles |
|-------------------------|--------------------------------------------|-----------------|
| MPY2PIF32 RaH,RbH | $a = b * 2\pi$ | 2/3 |
| DIV2PIF32 RaH,RbH | $a = b / 2\pi$ | 2/3 |
| DIVF32 RaH,RbH,RcH | $a = b/c$ | 5 |
| SQRTF32 RaH,RbH | $a = \text{sqrt}(b)$ | 5 |
| SINPUF32 RaH,RbH | $a = \sin(b*2\pi)$ | 4 |
| COSPUF32 RaH,RbH | $a = \cos(b*2\pi)$ | 4 |
| ATANPUF32 RaH,RbH | $a = \text{atan}(b)/2\pi$ | 4 |
| QUADF32 RaH,RbH,RcH,RdH | Operation to assist in calculating ATANPU2 | 5 |

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations.

For more information, see the [TMS320C28x Extended Instruction Sets Technical Reference Manual](#).

7.5.3 VCRC Unit

Cyclic redundancy check (CRC) algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The C28x+VCRC can perform 8-bit, 16-bit, 24-bit,

and 32-bit CRCs. For example, the VCRC can compute the CRC for a block length of 10 bytes in 10 cycles. A CRC result register contains the current CRC, which is updated whenever a CRC instruction is executed.

The following are the CRC polynomials used by the CRC calculation logic of the VCRC:

- CRC8 polynomial = 0x07
- CRC16 polynomial 1 = 0x8005
- CRC16 polynomial 2 = 0x1021
- CRC24 polynomial = 0x5d6dcb
- CRC32 polynomial 1 = 0x04c11db7
- CRC32 polynomial 2 = 0x1edc6f41

This module can calculate CRCs for a byte of data in a single cycle. The CRC calculation for CRC8, CRC16, CRC24, and CRC32 is done byte-wise (instead of computing on a complete 16-bit or 32-bit data read by the C28x core) to match the byte-wise computation requirement mandated by various standards.

The VCRC Unit also allows the user to provide the size (1b-32b) and value of any polynomial to fit custom CRC requirements. The CRC execution time increases to three cycles when using a custom polynomial.

For more information on the Cyclic Redundancy Check (VCRC) instruction sets, see the [TMS320C28x Extended Instruction Sets Technical Reference Manual](#).

7.5.4 Lockstep Compare Module (LCM)

Hardware module integrity during run-time is a critical functional safety requirement. Hardware Redundancy implemented by the lockstep CPU architecture (two CPUs executing the same function and the output of the CPUs are continuously compared) is a proven method for achieving high diagnostic coverage for both permanent and transient faults. The Lockstep Comparator Module (LCM) is implemented to compare output from the C28x CPU to detect permanent and transient faults.

The LCM implements the following features:

- Pipelined architecture
- Redundant comparison
- Self-test capability
 - Match and mismatch test
 - Error forcing capability
- Temporal redundancy: The operation of the two modules is skewed by two cycles to address the issue of common cause failures like failure of clock, power, and so on. This makes sure of temporal redundancy.
- Spatial redundancy: Each module is physically separate and their outputs are compared. The physical separation provides spatial redundancy.
- Non-delayed functional output path to provide non-delayed CPU execution for the system (while still having temporal redundancy).
- Register protection of critical memory mapped registers of the module, using a parity scheme.

Figure 7-2 shows the LCM block diagram.

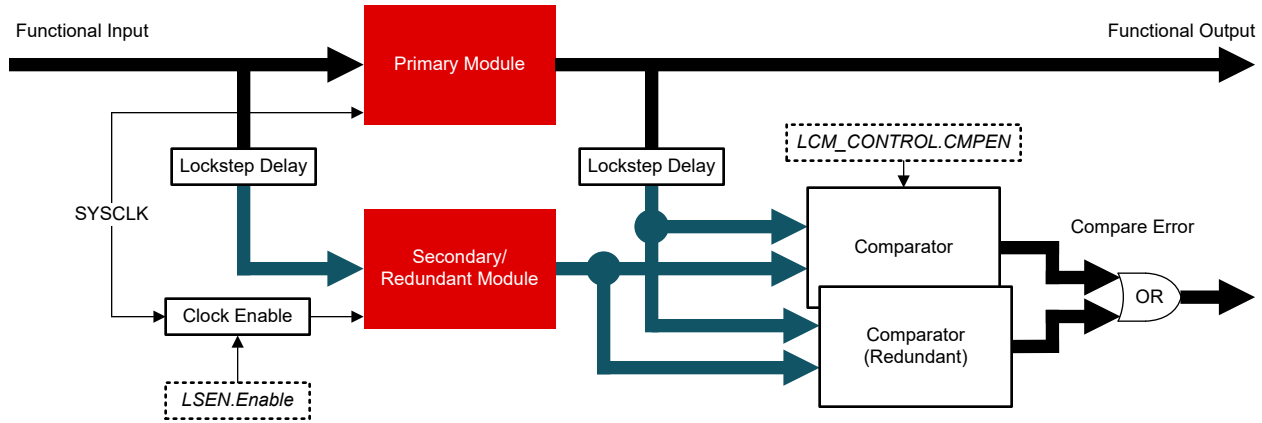


Figure 7-2. LCM Block Diagram

Note

The *Module* described in this block diagram can be either a CPU (for example, CPU1) or a peripheral (for example, DMA) depending on availability for the device.

7.6 Device Boot Modes

This section explains the default boot modes, as well as all the available boot modes supported on this device. The boot ROM uses the boot mode select, general-purpose input/output (GPIO) pins to determine the boot mode configuration.

Table 7-6 shows the boot mode options available for selection by the default boot mode select pins. Users have the option to program the device to customize the boot modes selectable in the boot-up table as well as the boot mode select pin GPIOs used.

All the peripheral boot modes that are supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, CANA, and so forth). Whenever these boot modes are referred to in this chapter, such as SCI boot, it is actually referring to the first module instance, which means the SCI boot on the SCIA port. The same applies to the other peripheral boots.

See the Reset (XRSn) Switching Characteristics table and the Reset Timing Diagrams for $t_{boot-flash}$, the boot ROM execution time to first instruction fetch in flash.

Table 7-6. Device Default Boot Modes

| BOOT MODE | GPIO24 (DEFAULT BOOT MODE SELECT PIN 1) | GPIO32 (DEFAULT BOOT MODE SELECT PIN 0) |
|--------------------------------|--------------------------------------------|--------------------------------------------|
| Parallel IO | 0 | 0 |
| SCI / Wait Boot ⁽¹⁾ | 0 | 1 |
| CAN | 1 | 0 |
| Flash | 1 | 1 |

(1) SCI boot mode can be used as a wait boot mode as long as SCI continues to wait for an 'A' or 'a' during the SCI autobaud lock process.

Table 7-7 lists the possible boot modes supported on the device. The default boot mode pins are GPIO24 (boot mode pin 1) and GPIO32 (boot mode pin 0). Users may choose to have weak pullups for boot mode pins if they use a peripheral on these pins as well, so the pullups can be overdriven. On this device, customers can change the factory default boot mode pins by programming user-configurable Dual Code Security Module (DCSM) OTP locations.

Table 7-7. All Available Boot Modes

| BOOT MODE NUMBER | BOOT MODE |
|------------------|--------------|
| 0 | Parallel |
| 1 | SCI / Wait |
| 2 | CAN |
| 3 | Flash |
| 4 | Wait |
| 5 | RAM |
| 6 | SPI |
| 7 | I2C |
| 8 | CAN FD |
| 10 | Secure Flash |

Note

All the peripheral boot modes supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, CANA, and so forth). Whenever these boot modes are referred to in this section, such as SCI boot, it is actually referring to the first module instance, meaning SCI boot on the SCIA port. The same applies to the other peripheral boots.

7.6.1 Device Boot Configurations

This section details what boot configurations are available and how to configure them. This device supports from 0 boot mode select pins up to 3 boot mode select pins as well as from 1 configured boot mode up to 8 configured boot modes.

To change and configure the device from the default settings to custom settings for your application, use the following process:

1. Determine all the various ways you want application to be able to boot. (For example: Primary boot option of Flash boot for your main application, secondary boot option of CAN boot for firmware updates, tertiary boot option of SCI boot for debugging, etc)
2. Based on the number of boot modes needed, determine how many boot mode select pins (BMSPs) are required to select between your selected boot modes. (For example: 2 BMSPs are required to select between 3 boot mode options)
3. Assign the required BMSPs to a physical GPIO pin. (For example, BMSP0 to GPIO10, BMSP1 to GPIO51, and BMSP2 left as default which is disabled). Refer to [Section 7.6.1.1](#) for all the details on performing these configurations.
4. Assign the determined boot mode definitions to indexes in your custom boot table that correlate to the decoded value of the BMSPs. For example, BOOTDEF0=Boot to Flash, BOOTDEF1=CAN Boot, BOOTDEF2=SCI Boot; all other BOOTDEFx are left as default/nothing). Refer to [Section 7.6.1.2](#) for all the details on setting up and configuring the custom boot mode table.

Additionally, the Boot Mode Example Use Cases section of the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#) provides some example use cases on how to configure the BMSPs and custom boot tables.

Note

The CAN boot mode turns on the XTAL. Be sure an XTAL is installed in the application before using CAN boot mode.

7.6.1.1 Configuring Boot Mode Pins

This section explains how the boot mode select pins can be customized by the user, by programming the BOOTPIN-CONFIG location (refer to [Table 7-8](#)) in the user-configurable dual-zone security module (DCSM) OTP. The location in the DCSM OTP is Z1-OTP-BOOTPIN-CONFIG or Z2-OTP-BOOTPIN-CONFIG. When debugging, EMU-BOOTPIN-CONFIG is the emulation equivalent of Z1-OTP-BOOTPIN-CONFIG/Z2-OTP-BOOTPIN-CONFIG, and can be programmed to experiment with different boot modes without writing to OTP. The device can be programmed to use 0, 1, 2, or 3 boot mode select pins as needed.

Note

When using Z2-OTP-BOOTPIN-CONFIG, the configurations programmed in this location will take priority over the configurations in Z1-OTP-BOOTPIN-CONFIG. It is recommended to use Z1-OTP-BOOTPIN-CONFIG first and then if OTP configurations need to be altered, switch to using Z2-OTP-BOOTPIN-CONFIG.

Table 7-8. BOOTPIN-CONFIG Bit Fields

| BIT | NAME | DESCRIPTION |
|-------|--------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | Key | Write 0x5A to these 8-bits to indicate the bits in this register are valid |
| 23:16 | Boot Mode Select Pin 2 (BMSP2) | Refer to BMSP0 description except for BMSP2 |
| 15:8 | Boot Mode Select Pin 1 (BMSP1) | Refer to BMSP0 description except for BMSP1 |
| 7:0 | Boot Mode Select Pin 0 (BMSP0) | Set to the GPIO pin to be used during boot (up to 255): - 0x0 = GPIO0 - 0x01 = GPIO1 - and so on Writing 0xFF disables BMSP0 and this pin is no longer used to select the boot mode. |

Note

GPIO 224 to 253 are analog pins, but digital inputs are possible on these pins provided the software writes to the GPIOHAMSEL register bits.

The following GPIOs **cannot** be used as a BMSP. If selected for a particular BMSP, the boot ROM will automatically select the factory default GPIOs for BMSP0 and BMSP1. Factory default for BMSP2 is 0xFF, which disables the BMSP.

- GPIO 36, 38, 39, 47, 50-223, 225, 229, 230-241, 243 (Not available on any package)

Table 7-9. Standalone Boot Mode Select Pin Decoding

| BOOTPIN_CONFIG KEY | BMSP0 | BMSP1 | BMSP2 | REALIZED BOOT MODE |
|--------------------|--------------|--------------|--------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|
| != 0x5A | Don't Care | Don't Care | Don't Care | Boot as defined by the factory default BMSPs |
| = 0x5A | 0xFF | 0xFF | 0xFF | Boot as defined in the boot table for boot mode 0 (All BMSPs disabled) |
| | Valid GPIO | 0xFF | 0xFF | Boot as defined by the value of BMSP0 (BMSP1 and BMSP2 disabled) |
| | 0xFF | Valid GPIO | 0xFF | Boot as defined by the value of BMSP1 (BMSP0 and BMSP2 disabled) |
| | 0xFF | 0xFF | Valid GPIO | Boot as defined by the value of BMSP2 (BMSP0 and BMSP1 disabled) |
| | Valid GPIO | Valid GPIO | 0xFF | Boot as defined by the values of BMSP0 and BMSP1 (BMSP2 disabled) |
| | Valid GPIO | 0xFF | Valid GPIO | Boot as defined by the values of BMSP0 and BMSP2 (BMSP1 disabled) |
| | 0xFF | Valid GPIO | Valid GPIO | Boot as defined by the values of BMSP1 and BMSP2 (BMSP0 disabled) |
| | Valid GPIO | Valid GPIO | Valid GPIO | Boot as defined by the values of BMSP0, BMSP1, and BMSP2 |
| | Invalid GPIO | Valid GPIO | Valid GPIO | BMSP0 is reset to the factory default BMSP0 GPIO Boot as defined by the values of BMSP0, BMSP1, and BMSP2 |
| | Valid GPIO | Invalid GPIO | Valid GPIO | BMSP1 is reset to the factory default BMSP1 GPIO Boot as defined by the values of BMSP0, BMSP1, and BMSP2 |
| Valid GPIO | Valid GPIO | Invalid GPIO | BMSP2 is reset to the factory default state, which is disabled Boot as defined by the values of BMSP0 and BMSP1 | |

Note

When decoding the boot mode, BMSP0 is the least-significant-bit and BMSP2 is the most-significant-bit of the boot table index value. It is recommended when disabling BMSPs to start with disabling BMSP2. For example, in an instance when only using BMSP2 (BMSP1 and BMSP0 are disabled), then only the boot table indexes of 0 and 4 will be selectable. In the instance when using only BMSP0, then the selectable boot table indexes are 0 and 1.

7.6.1.2 Configuring Boot Mode Table Options

This section explains how to configure the boot definition table, BOOTDEF, for the device and the associated boot options. The 64-bit location is located in user-configurable DCSM OTP in the Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations. When debugging, EMU-BOOTDEF-LOW and EMU-BOOTDEF-HIGH are the emulation equivalents of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH, and can be programmed to experiment with different boot mode options without writing to OTP. The range of customization to the boot definition table depends on how many boot mode select pins (BMSP) are being used. For example, 0 BMSPs equals to 1 table entry, 1 BMSP equals to 2 table entries, 2 BMSPs equals to 4 table entries, and 3 BMSPs equals to 8 table entries. Refer to the [TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#) for examples on how to set up the BOOTPIN_CONFIG and BOOTDEF values.

Note

The locations Z2-OTP-BOOTDEF-LOW and Z2-OTP-BOOTDEF-HIGH will be used instead of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations when Z2-OTP-BOOTPIN-CONFIG is configured. Refer to [Section 7.6.1.1](#) for more details on BOOTPIN_CONFIG usage.

Table 7-10. BOOTDEF Bit Fields

| BOOTDEF NAME | BYTE POSITION | NAME | DESCRIPTION |
|--------------|---------------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BOOT_DEF0 | 7:0 | BOOT_DEF0 Mode/Options | Set the boot mode for index 0 of the boot table. Different boot modes and their options can include, for example, a boot mode that uses different GPIOs for a specific bootloader or a different flash entry point address. Any unsupported boot mode will cause the device to either go to wait boot or boot to flash. Refer to GPIO Assignments for valid BOOTDEF values to set in the table. |
| BOOT_DEF1 | 15:8 | BOOT_DEF1 Mode/Options | Refer to BOOT_DEF0 description |
| BOOT_DEF2 | 23:16 | BOOT_DEF2 Mode/Options | |
| BOOT_DEF3 | 31:24 | BOOT_DEF3 Mode/Options | |
| BOOT_DEF4 | 39:32 | BOOT_DEF4 Mode/Options | |
| BOOT_DEF5 | 47:40 | BOOT_DEF5 Mode/Options | |
| BOOT_DEF6 | 55:48 | BOOT_DEF6 Mode/Options | |
| BOOT_DEF7 | 63:56 | BOOT_DEF7 Mode/Options | |

7.6.2 GPIO Assignments

This section details the GPIOs and boot option values used for boot mode set in the BOOT_DEF memory location located at Z1-OTP-BOOTDEF-LOW/ Z2-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH/ Z2-OTP-BOOTDEF-HIGH. Refer to [Configuring Boot Mode Table Options](#) on how to configure BOOT_DEF. When selecting a boot mode option, make sure to verify that the necessary pins are available in the pin mux options for the specific device package being used.

Table 7-11. SCI Boot Options

| OPTION | BOOTDEF VALUE | SCITXDA GPIO | SCIRXDA GPIO |
|-------------|---------------|--------------|--------------|
| 0 (default) | 0x01 | GPIO29 | GPIO28 |
| 1 | 0x21 | GPIO1 | GPIO0 |
| 2 | 0x41 | GPIO8 | GPIO9 |
| 3 | 0x61 | GPIO7 | GPIO3 |
| 4 | 0x81 | GPIO16 | GPIO3 |

Table 7-12. CAN Boot Options

| OPTION | BOOTDEF VALUE | CANTXA GPIO | CANRXA GPIO |
|-------------|---------------|-------------|-------------|
| 0 (default) | 0x02 | GPIO7 | GPIO5 |
| 1 | 0x22 | GPIO32 | GPIO33 |
| 2 | 0x42 | GPIO2 | GPIO3 |
| 3 | 0x62 | GPIO13 | GPIO12 |

Note

F280013x and F280015x CANTXA GPIO Option 0 (default) selections are different. All other CAN boot option GPIO selections are the same. Please refer to respective device data sheet for details.

Table 7-13. CAN FD Boot Options

| OPTION | BOOTDEF VALUE | MCANTXA GPIO | MCANRXA GPIO |
|---------------------|---------------|--------------|--------------|
| 0 (default) | 0x08 | GPIO4 | GPIO5 |
| 1 | 0x28 | GPIO1 | GPIO0 |
| 2 | 0x48 | GPIO13 | GPIO12 |
| 3 (DEBUG-Send Test) | 0x68 | GPIO4 | GPIO5 |
| 4 (DEBUG-Send Test) | 0x88 | GPIO1 | GPIO0 |
| 5 (DEBUG-Send Test) | 0xA8 | GPIO13 | GPIO12 |

Table 7-14. I2C Boot Options

| OPTION | BOOTDEF VALUE | SDAA GPIO | SCLA GPIO |
|--------|---------------|-----------|-----------|
| 0 | 0x07 | GPIO0 | GPIO1 |
| 1 | 0x27 | GPIO32 | GPIO33 |
| 2 | 0x47 | GPIO5 | GPIO4 |

Table 7-15. RAM Boot Options

| OPTION | BOOTDEF VALUE | RAM ENTRY POINT (ADDRESS) |
|--------|---------------|---------------------------|
| 0 | 0x05 | 0x0000 0000 |

Table 7-16. Flash Boot Options

| OPTION | BOOTDEF VALUE | FLASH ENTRY POINT (ADDRESS) | FLASH SECTOR |
|-------------|---------------|-----------------------------|------------------|
| 0 (default) | 0x03 | 0x0008 0000 | Bank0 Sector 0 |
| 1 | 0x23 | 0x0008 8000 | Bank 0 Sector 32 |

Table 7-16. Flash Boot Options (continued)

| OPTION | BOOTDEF VALUE | FLASH ENTRY POINT (ADDRESS) | FLASH SECTOR |
|--------|---------------|-----------------------------|--------------------------|
| 2 | 0x43 | 0x0008 FFF0 | Bank 0 End of Sector 63 |
| 3 | 0x63 | 0x0009 0000 | Bank 0 Sector 64 |
| 4 | 0x83 | 0x0009 8000 | Bank 0 Sector 96 |
| 6 | 0xA3 | 0x0009 FFF0 | Bank 0 End of Sector 127 |

Table 7-17. Secure Flash Boot Options

| OPTION | BOOTDEF VALUE | FLASH ENTRY POINT (ADDRESS) | FLASH SECTOR |
|-------------|---------------|-----------------------------|-------------------------|
| 0 (default) | 0x0A | 0x0008 0000 | Bank0 Sector 0 |
| 1 | 0x2A | 0x0008 8000 | Bank 0 Sector 32 |
| 2 | 0x4A | 0x0008 FFF0 | Bank 0 End of Sector 63 |
| 3 | 0x6A | 0x0009 0000 | Bank 0 Sector 64 |
| 4 | 0x8A | 0x0009 8000 | Bank 0 Sector 96 |

Table 7-18. Wait Boot Options

| OPTION | BOOTDEF VALUE | WATCHDOG |
|--------|---------------|----------|
| 0 | 0x04 | Enabled |
| 1 | 0x24 | Disabled |

Table 7-19. SPI Boot Options

| OPTION | BOOTDEF VALUE | SPISIMOA | SPISOMIA | SPICLKA | SPISTEA |
|--------|---------------|----------|----------|---------|---------|
| 0 | 0x06 | GPIO7 | GPIO1 | GPIO3 | GPIO5 |
| 1 | 0x26 | GPIO16 | GPIO1 | GPIO3 | GPIO0 |
| 2 | 0x46 | GPIO8 | GPIO10 | GPIO9 | GPIO11 |
| 3 | 0x66 | GPIO16 | GPIO13 | GPIO12 | GPIO29 |

Table 7-20. Parallel Boot Options

| OPTION | BOOTDEF VALUE | D0-D7 GPIO | 28x(DSP) CONTROL GPIO | HOST CONTROL GPIO |
|-------------|---------------|-------------|-----------------------|-------------------|
| 0 (default) | 0x00 | D0 - GPIO0 | GPIO224 | GPIO242 |
| | | D1 - GPIO1 | | |
| | | D2 - GPIO3 | | |
| | | D3 - GPIO4 | | |
| | | D4 - GPIO5 | | |
| | | D5 - GPIO7 | | |
| | | D6 - GPIO28 | | |
| | | D7 - GPIO29 | | |
| 1 | 0x20 | D0 - GPIO0 | GPIO12 | GPIO13 |
| | | D1 - GPIO1 | | |
| | | D2 - GPIO2 | | |
| | | D3 - GPIO3 | | |
| | | D4 - GPIO4 | | |
| | | D5 - GPIO5 | | |
| | | D6 - GPIO6 | | |
| | | D7 - GPIO7 | | |

Table 7-20. Parallel Boot Options (continued)

| OPTION | BOOTDEF VALUE | D0-D7 GPIO | 28x(DSP) CONTROL GPIO | HOST CONTROL GPIO |
|--------|---------------|------------|-----------------------|-------------------|
| 2 | 0x40 | D0 - GPIO0 | GPIO16 | GPIO29 |
| | | D1 - GPIO1 | | |
| | | D2 - GPIO2 | | |
| | | D3 - GPIO3 | | |
| | | D4 - GPIO4 | | |
| | | D5 - GPIO5 | | |
| | | D6 - GPIO6 | | |
| | | D7 - GPIO7 | | |

7.7 Security

Security features are enforced by the Dual Code Security Module (DCSM). The primary layer of defense is securing the boundary of the chip, which should always be enabled. Additionally, the Dual Zone Security feature is available to support code partitioning.

7.7.1 Securing the Boundary of the Chip

The following two features, along with authentication in the firmware update code, should be used to help to prevent unauthorized code from running on the device.

7.7.1.1 JTAGLOCK

Enabling the JTAGLOCK feature in the USER OTP disables JTAG access (for example, debug probe) to resources on the device.

7.7.1.2 Zero-pin Boot

Enabling the Zero-pin Boot option along with Flash Boot in the USER OTP blocks all pin-based external bootloader options (for example, SCI, CAN, Parallel).

7.7.2 Dual-Zone Security

The dual-zone security mechanism offers protection for two zones: Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both zones is identical. Each zone has its own dedicated secure resource (OTP memory and secure ROM) and allocated secure resource (LSx RAM and flash sectors).

7.7.3 Disclaimer

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

7.8 Watchdog

The watchdog module is the same as the one on previous TMS320C2000™ microcontrollers, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backward-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 7-3 shows the various functional blocks within the watchdog module.

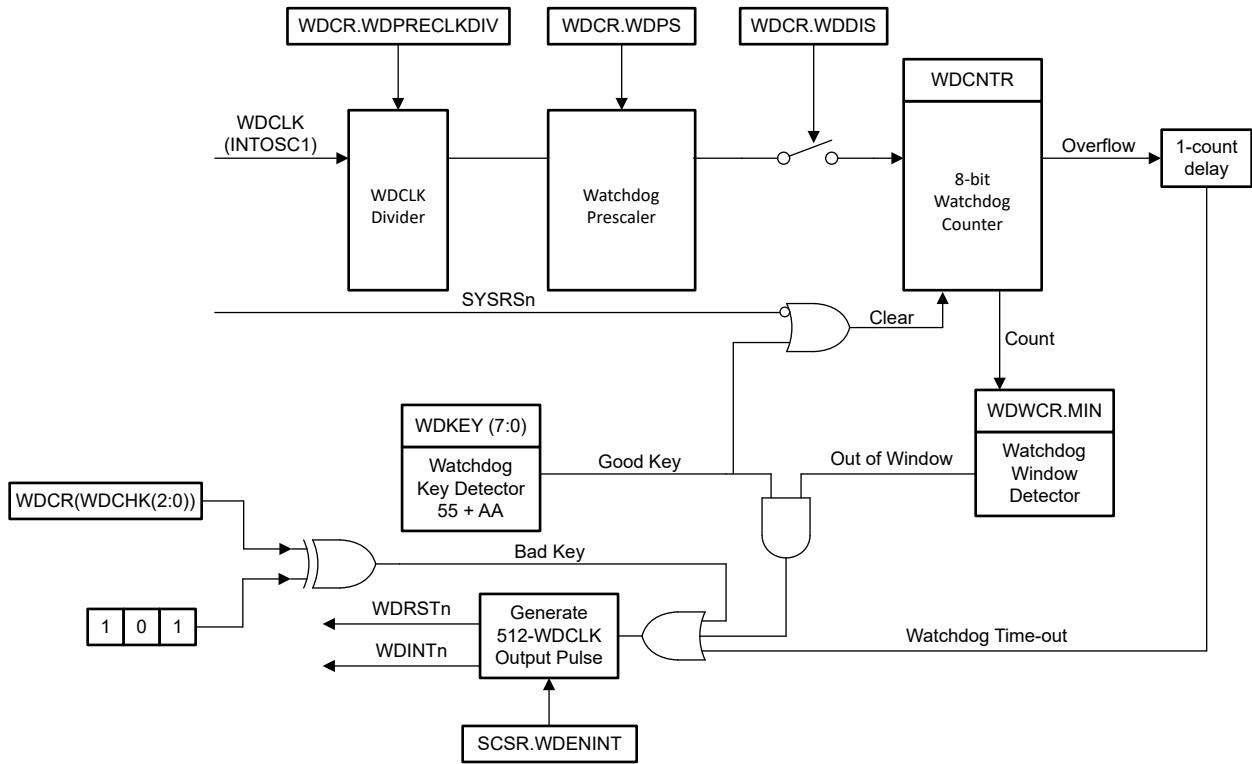


Figure 7-3. Windowed Watchdog

7.9 C28x Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presetable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for TI-RTOS. It is connected to INT14 of the CPU. If TI-RTOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLK (default)
- Internal oscillator 1 (INTOSC1)
- Internal oscillator 2 (INTOSC2)
- X1 (XTAL)

7.10 Dual-Clock Comparator (DCC)

The DCC module is used for evaluating and monitoring the clock input based on a second clock, which can be a more accurate and reliable version. This instrumentation is used to detect faults in clock source or clock structures, thereby enhancing the system's safety metrics.

7.10.1 Features

The DCC has the following features:

- Allows the application to ensure that a fixed ratio is maintained between frequencies of two clock signals.
- Supports the definition of a programmable tolerance window in terms of the number of reference clock cycles.
- Supports continuous monitoring without requiring application intervention.
- Supports a single-sequence mode for spot measurements.
- Allows the selection of a clock source for each of the counters, resulting in several specific use cases.

7.10.2 Mapping of DCCx Clock Source Inputs

Table 7-21. DCCx Clock Source0 Table

| DCCxCLKSRC0[3:0] | CLOCK NAME |
|------------------|-------------------------------------|
| 0x0 | XTAL/X1 |
| 0x1 | INTOSC1 |
| 0x2 | INTOSC2 |
| 0x4 | TCK |
| 0x5 | CPU1.SYSCLK |
| 0x8 | AUXCLKIN |
| 0xC | INPUT XBAR (Output16 of input-xbar) |
| others | Reserved |

Table 7-22. DCCx Clock Source¹ Table

| DCCxCLKSRC1[4:0] | CLOCK NAME |
|-------------------------|-----------------------------------------|
| 0x0 | PLLRAWCLK |
| 0x2 | INTOSC1 |
| 0x3 | INTOSC2 |
| 0x6 | CPU1.SYSCLK |
| 0x9 | Input XBAR (Output15 of the input-xbar) |
| 0xA | AUXCLKIN |
| 0xB | EPWMCLK |
| 0xC | LSPCLK |
| 0xD | ADCCLK |
| 0xE | WDCLK |
| 0xF | CAN0BITCLK |
| others | Reserved |

7.11 Functional Safety

Functional Safety-Compliant products are developed using an ISO 26262/IEC 61508-compliant hardware development process that is independently assessed and certified to meet ASIL D/SIL 3 systematic capability (see [certificate](#)). The TMS320F280015x has been certified to meet a component-level random hardware capability of ASIL B and SIL 2 (see [certificate](#)).

A functional safety manual that describes all of the hardware and software functional safety mechanisms is available. See the [Functional Safety Manual for TMS320F280015x](#).

A detailed, tunable, fault-injected, quantitative FMEDA that enables the calculation of random hardware metrics—as outlined in the International Organization for Standardization ISO 26262 and the International Electrotechnical Commission IEC 61508 for automotive and industrial applications, respectively—is also available. This tunable FMEDA must be requested; see the [C2000™ Safety Package for Automotive and Industrial Real-Time Microcontrollers User's Guide](#).

- A white paper outlining the value (or benefit) of a tunable FMEDA is available. See the [Functional Safety: A tunable FMEDA for C2000™ MCUs](#) publication.
- Part 1 and Part 2 of a five-part FMEDA tuning training are available from the [TI Video Library](#). Part 1 is [Basics of FMEDA and how it is useful in system level safety analysis](#). Part 2 is [Introduction to the C2000™ Tunable FMEDA](#). Parts 3, 4, and 5 are packaged with the tunable FMEDA, and must be requested.

Two diagnostic libraries designed for the F280015x series of devices are available to aid in the development of functionally safe systems—the C28x Self-Test Library (C28x_STL) and the Software Diagnostic Library (SDL). The C28x_STL provides software tests of the C28x CPU and has been independently assessed and certified. It is available upon request only, see the [C2000™ Safety Package for Automotive and Industrial Real-Time Microcontrollers User's Guide](#). The SDL is a set of reference software providing example implementations of several safety mechanisms described in the device safety manual, such as LCM self-tests, software tests of SRAMs, software tests of Missing Clock Detect functionality, clock integrity checks using CPU Timers, and several other key features. The SDL is provided as part of [C2000Ware](#).

C2000 real-time MCUs are also equipped with a TI release validation-based C28x and CLA Compiler Qualification Kit (CQKIT), which is available for free and may be requested at the [Safety compiler qualification kit](#) web page.

Additional details about how to develop functionally safe systems with C2000 real-time MCUs can be found in the following documents:

- [Automotive Functional Safety for C2000™ Real-Time Microcontrollers](#) summarizes the available functional safety products, documentation, software, and support available for aiding in the ISO 26262 certification process.
- [Industrial Functional Safety for C2000™ Real-Time Microcontrollers](#) summarizes the available functional safety products, documentation, software, and support available for aiding in the IEC 61508 certification process.
- [Error Detection in SRAM Application Report](#) provides technical information about the nature of the SRAM bit cell and bit array, as well as the sources of SRAM failures. It then presents methods for managing memory failures in electronic systems. This discussion is intended for electronic system developers or integrators who are interested in improving the robustness of the embedded SRAM.
- [C2000™ CPU Memory Built-In Self-Test](#) describes embedded memory validation using the C28x central processing unit (CPU) during an active control loop. It discusses system challenges to memory validation as well as the different solutions provided by C2000 devices and software. Finally, it presents the applicable Software Diagnostic Library features for memory testing.

8 Applications, Implementation, and Layout

8.1 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

The [Hardware Design Guide for F2800x C2000™ Real-Time MCU Series Application Note](#) is an essential guide for hardware developers using C2000 devices, and helps to streamline the design process while mitigating the potential for faulty designs. Key topics discussed include: power requirements; general-purpose input/output (GPIO) connections; analog inputs and ADC; clocking generation and requirements; and JTAG debugging among many others.

8.2 Key Device Features

Table 8-1. Key Device Features

| MODULE | FEATURE | SYSTEM BENEFIT |
|--------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PROCESSING | | |
| Real-time control CPUs | Up to 120 MIPS C28x: 120 MIPS Flash: Up to 256KB RAM : Up to 36KB 32-bit Floating-Point Unit (FPU32) Trigonometric Math Unit (TMU) CRC engine and instructions (VCRC) | TI's 32-bit lockstep dual-C28x core enables the device to achieve ASIL B functional safety device rating without much software overhead. Provides 120 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. FPU32: Native hardware support for IEEE-754 single-precision floating-point operations TMU: Accelerators used to speed up execution of trigonometric and arithmetic operations for faster computation (such as PLL and DQ transform) optimized for control applications. Helps in achieving faster control loops, resulting in higher efficiency and better component sizing. Special instructions to support nonlinear PID control algorithms VCRC: Provides a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. |
| SENSING | | |
| Analog-to-Digital Converter (ADC) (12-bit) | Up to 2 ADC modules 4 MSPS Up to 21 channels | ADC provides precise and concurrent sampling of all three-phase currents and DC bus with zero jitter. ADC post-processing – On-chip hardware reduces ADC ISR complexity and shortens current loop cycles. More ADCs help in multiphase applications. Provide better effective MSPS (oversampling) and typical ENOB for better control-loop performance. |

Table 8-1. Key Device Features (continued)

| MODULE | FEATURE | SYSTEM BENEFIT |
|------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Comparator Subsystem (CMPSS) | CMPSS 1 windowed comparator Dual 12-bit DACs DAC ramp generation Low DAC output on external pin Digital filters 60-ns detection to trip time Slope compensation | System protection without false alarms: Comparator Subsystem (CMPSS) modules are useful for applications such as peak-current mode control, switched-mode power, power factor correction, and voltage trip monitoring. PWM trip-triggering and removal of unwanted noise are easy with blanking window and filtering features provided with the analog comparator subsystems. |
| | CMPSS_LITE 3 windowed comparators Dual 9.5-bit effective reference DACs Digital filters 40-ns detection to trip time Slope compensation | Provides better control accuracy. No need for further CPU configuration to control the PWM with the comparator and 12-bit DAC (CMPSS) and 9.5-bit effective reference DAC for CMPSS_LITE. Enables protection and control using the same pin. |
| Enhanced Quadrature Encoder Pulse (eQEP) | 2 eQEP modules | Used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine used in a high-performance motion and position-control system. Also can be used in other applications to count input pulses from an external device (such as a sensor). |
| Enhanced Capture (eCAP) | 3 eCAP modules Measures elapsed time between events (up to 4 time-stamped events). Connects to any GPIO through the input X-BAR. When not used in capture mode, the eCAP module can be configured as a single-channel PWM output (APWM). | Applications for eCAP include: Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors) Elapsed time measurements between position sensor pulses Period and duty cycle measurements of pulse train signals Decoding current or voltage amplitude derived from duty-cycle encoded current/voltage sensors |

Table 8-1. Key Device Features (continued)

| MODULE | FEATURE | SYSTEM BENEFIT |
|------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ACTUATION | | |
| Enhanced Pulse Width Modulation (ePWM) | Up to 14 ePWM channels Ability to generate high-side/low-side PWMs with deadband Supports Valley switching (ability to switch PWM output at valley point) and features like blanking window | Flexible PWM waveform generation with best power topology coverage. Shadowed Dead band itself and shadowed action qualifier enable adaptive PWM generation and protection for improved control accuracy and reduced power loss. Enables improvement in Power Factor (PF) and Total Harmonic Distortion (THD), which is especially relevant in Power Factor Correction (PFC) applications. Improves light load efficiency. |
| | One-shot and global reload feature | Critical for variable-frequency and multiphase DC-DC applications and helps in attaining high-frequency control loops (>2 MHz). Enables control of interleaved LLC topologies at high frequencies |
| | Independent PWM action on a Cycle-by-Cycle (CBC) trip event and an One-Shot Trip (OST) trip event | Provides cycle-by-cycle protection and complete shutoff of PWM under fault condition. Helps implement multiphase PFC or DC-DC control. |
| | Load on SYNC (support for shadow-to-active load on a SYNC event) | Enables variable-frequency applications (allows LLC control in power conversion). |
| | Ability to shut down the PWMs without software intervention (no ISR latency) | Fast protection under fault condition |
| | Delayed Trip Functionality | Helps implement the deadband with Peak Current Mode Control (PCMC) Phase-Shifted Full Bridge (PSFB) DC-DC easily without occupying much CPU resources (even on trigger events based on comparator, trip, or sync-in events). |
| | Dead band Generator (DB) submodule | Prevents simultaneous ON conditions of High and Low side gates by adding programmable delay to rising (RED) and falling (FED) PWM signal edges. |
| | Flexible PWM Phase Relationships and Timer Synchronization | Each ePWM module can be synchronized with other ePWM modules or other peripherals. Keeps PWM edges perfectly in synchronization with certain events. Supports flexible ADC scheduling with specific sampling window in synchronization with power device switching. |
| High-Resolution Pulse Width Modulation (HRPWM) | 4 channels with high-resolution capability (150 ps) Provides 150-ps steps for duty cycle, period, Dead band, and phase offsets for 99% greater precision | Beneficial for accurate control and enables better-performance high-frequency power conversion. Achieves cleaner waveforms and avoids oscillations/limit cycle at output. |
| CONNECTIVITY | | |
| Serial Peripheral Interface (SPI) | 1 high-speed SPI port | Supports 30 MHz |
| Serial Communication Interface (SCI) | 3 SCI (UART) modules | Interfaces with controllers |
| Local Interconnect Network (LIN) | 1 LIN | Provides a low-cost solution where the bandwidth and fault tolerance of a Controller Area Network (CAN) are not required |
| Controller Area Network (CAN/DCAN) | 1 DCAN module | Provides compatibility with classic CAN modules |

Table 8-1. Key Device Features (continued)

| MODULE | FEATURE | SYSTEM BENEFIT |
|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Controller Area Network (CAN FD/MCAN) | 1 CAN FD/MCAN module | CAN FD (flexible data-rate) is an enhancement to the classic CAN protocol. CAN FD facilitates dynamic switching to higher bit rates (>1 Mbps) for the data segment and allows for up to 64 bytes compared to 8 bytes in classic CAN. This is done without having to change the physical layer. This results in a bandwidth gain over traditional CAN. Systems using CAN-FD benefit from faster in-the-field flash updates. |
| Inter-Integrated Circuit (I2C) | 2 I2C modules | Interfaces with external EEPROMs, sensors, or controllers |
| Power-Management Bus (PMBus) | 1 PMBus module Compliance with the SMI Forum PMBus Specification (Part I v1.0 and Part II v1.1) | Seamless HW-based host communication |
| OTHER SYSTEM FEATURES | | |
| Security enhancers | Dual-zone Code Security Module (DCSM) Watchdog Write Protection on Register Missing Clock Detection Logic (MCD) Error Correction Code (ECC) and parity Dual-Clock Comparator (DCC) | DCSM: Prevents duplication and reverse-engineering of proprietary code Watchdog: Generates reset if CPU gets stuck in endless loops of execution Write Protection on Registers: LOCK protection on system configuration registers Protection against spurious CPU writes MCD: Automatic clock failure detection ECC and parity: Single-bit error correction and double-bit error detection DCC: Used to detect faults in clock source |
| Crossbars (XBARs) | Provides flexibility to connect device inputs, outputs, and internal resources in a variety of configurations. • Input X-BAR • Output X-BAR • ePWM X-BAR | Enhances hardware design versatility: Input X-BAR: Routes signals from any GPIO to multiple IP blocks within the chip Output XBAR: Routes internal signals onto designated GPIO pins ePWM X-BAR: Routes internal signals from various IP blocks to EPWM |

8.3 Application Information

8.3.1 Typical Application

The *Typical Applications* section details *some* applications of this device. For a more extensive list of applications, see the *Applications* section of this data sheet.

8.3.1.1 On-Board Charger (OBC)

In the OBC and High-Voltage DC-DC charger (HV DCDC) markets, the modular-based design and the combo-box-based design are the two primary architectures adopted. The modular approach provides flexibility in manufacturing and after-service; and the combo-box approach seeks to integrate multiple functions into one enclosure for compactness. F280015x targets the modular-based control architecture and cost-sensitive solutions, which require limited controller performance (≤ 120 MIPS) with the element functional safety of ASIL B (D) for the controller.

An on-board charger consists of two power stages: PFC (AC-DC) power converter and a subsequent DC-DC power converter. Each power stage is controlled with a single MCU.

OBC-charging design requirements are as follows:

- High-performance and fast digital control loops enabling highly efficient power conversion and increased power density.

- Enabling precise control and fast shutdown in an overcurrent scenario by high bandwidth and fast response current sensing.
- Safely and efficiently controlling and protecting the power switch [insulated-gate bipolar transistor/silicon carbide (IGBT/SiC)].

8.3.1.1.1 System Block Diagram

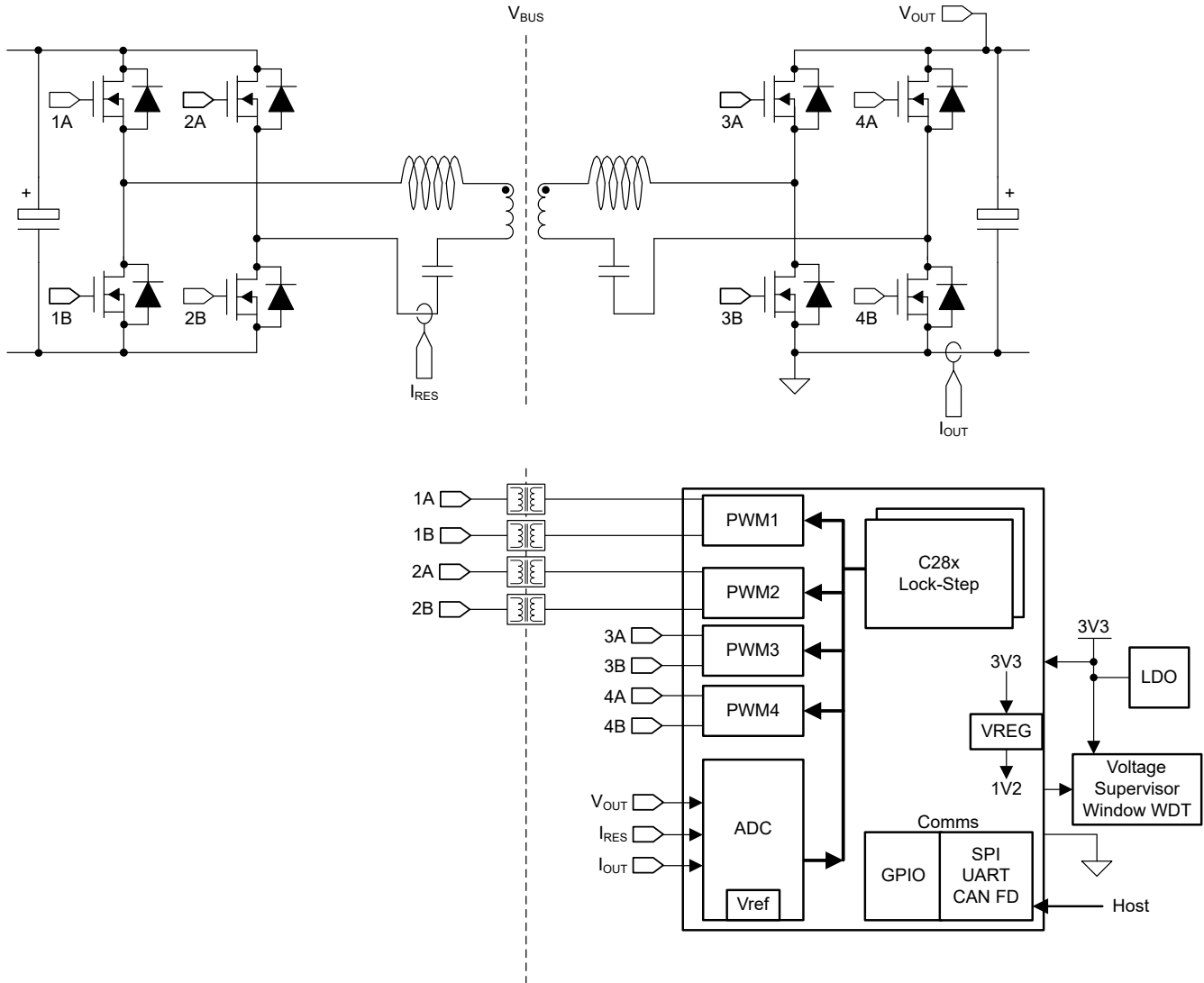


Figure 8-1. OBC - DC - DC

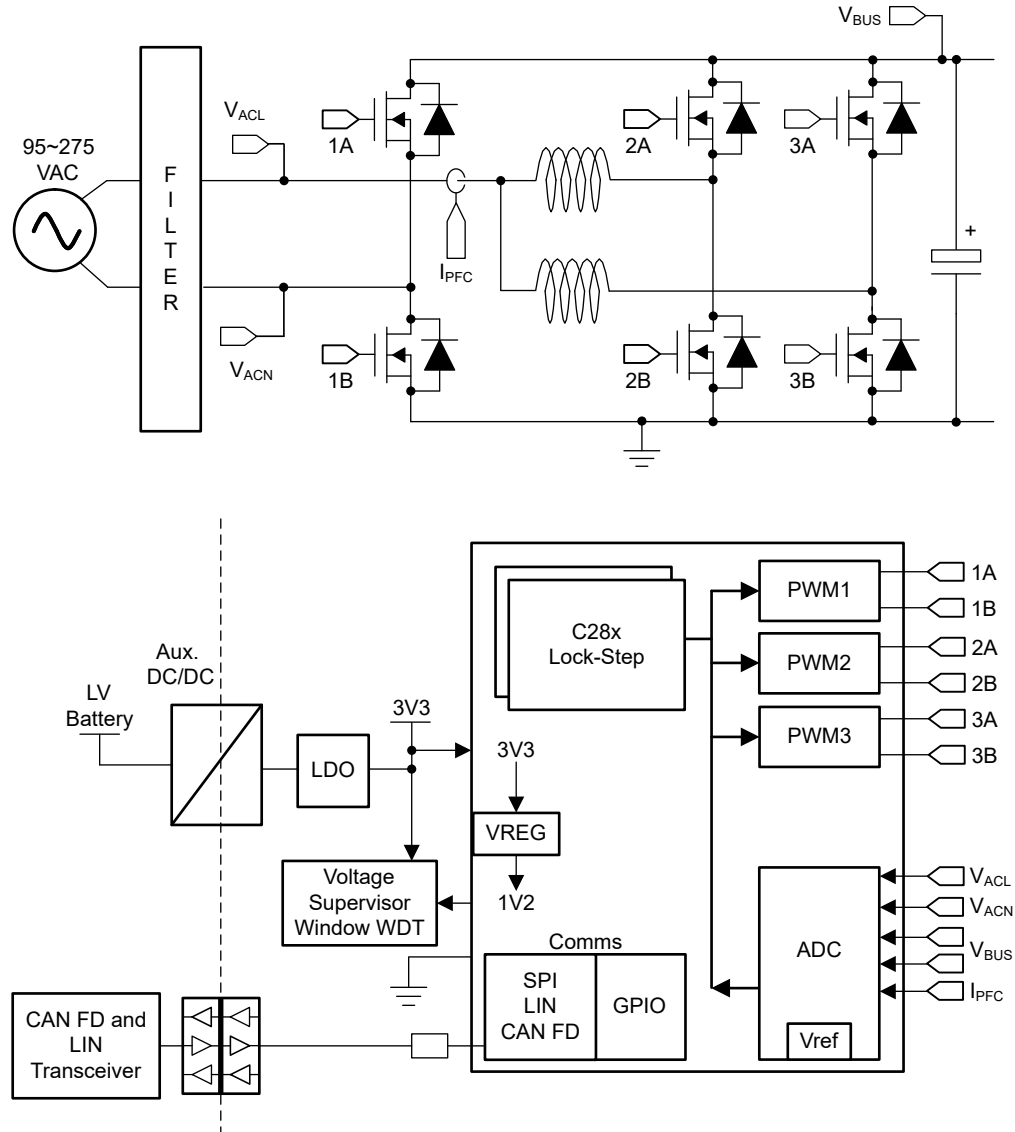


Figure 8-2. Single-Phase Totem Pole

8.3.1.1.2 OBC Resources

Reference Designs and Associated Training Videos

[C2000 Digital Power Training videos](#)

This power topology is capable of bidirectional power flow (PFC and grid-tied inverter) and uses GaN devices, which enables higher efficiency and reduction in size of the power supply. The hardware and software available with this reference design accelerates time to market.

[C2000™ MCUs - Electric vehicle \(EV\) training videos \(Video\)](#)

This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

[PMP22650 GaN-based, 6.6-kW, bidirectional, onboard charger reference design](#)

The PMP22650 reference design is a 6.6-kW, bidirectional, onboard charger. The design employs a two-phase totem pole PFC and a full-bridge CLLLC converter with synchronous rectification. The CLLLC utilizes both frequency and phase modulation to regulate the output across the required regulation range. The design uses a single processing core inside a TMS320F28388D microcontroller to control both the PFC and CLLLC.

Synchronous rectification is implemented via the same microcontroller with Rogowski coil current sensors. High density is achieved through the use of high-speed GaN switches (LMG3522). The PFC is operating at 120 kHz and the CLLLC runs with a variable frequency from 200 kHz to 800 kHz. A peak system efficiency of 96.5% was achieved with an open-frame power density of 3.8 kW/L. While the design calculations were done for a 6.6-kW output power, the design represents a suitable starting point for a 7.x-kW (for example, 7.2-kW to 7.4-kW) rated OBC operating from a 240-V input with a 32-A breaker.

[TIDUEG2C TIDM-02002 Bidirectional CLLLC resonant dual active bridge \(DAB\) reference design for HEV/EV onboard charger](#)

The CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

[TIDUEG3A TIDM-1022 Valley switching boost power factor correction \(PFC\) reference design](#)

This reference design illustrates a digital control method to significantly improve Boost Power Factor Correction (PFC) converter performance such as the efficiency and Total Harmonic Distortion (THD) under light load condition where efficiency and THD standards are difficult to meet. This is achieved using the integrated digital control feature of the C2000™ microcontroller (MCU). The design supports phase-shedding, valley-switching, valley-skipping, and Zero Voltage Switching (ZVS) for different load and instantaneous input voltage conditions. The software available with this reference design accelerates time to market.

8.3.1.2 Automotive Pump

Fluid or fuel control pumps are typically used in automotive engine management systems based on the type of powertrain required. Depending on the type of system and load, these actuators are in open loop or closed loop, complete with precise control.

All vehicles—internal combustion engine, electric, or hybrid (ICE/EV/HEV)—need various types of pumps (such as fuel pumps; coolant or water pumps; and oil pumps). Although the purpose of each pump is different, the function of the pump is the same: to move fluid, fuel, or oil from one place to another. In the example of a fuel pump, the pump transfers fuel from the fuel tank to the engine chamber for the engine to use. Depending on the function, pumps can be variable-speed pumps or fixed-speed pumps.

The vehicle's battery provides the current required to run the fuel pump. An electronic control unit (ECU) regulates the output pressure and volume of the gasoline, as well as meters the incoming fuel from the tank. The ECU assists the car in conserving fuel, resulting in improved economy and power.

8.3.1.2.1 System Block Diagram

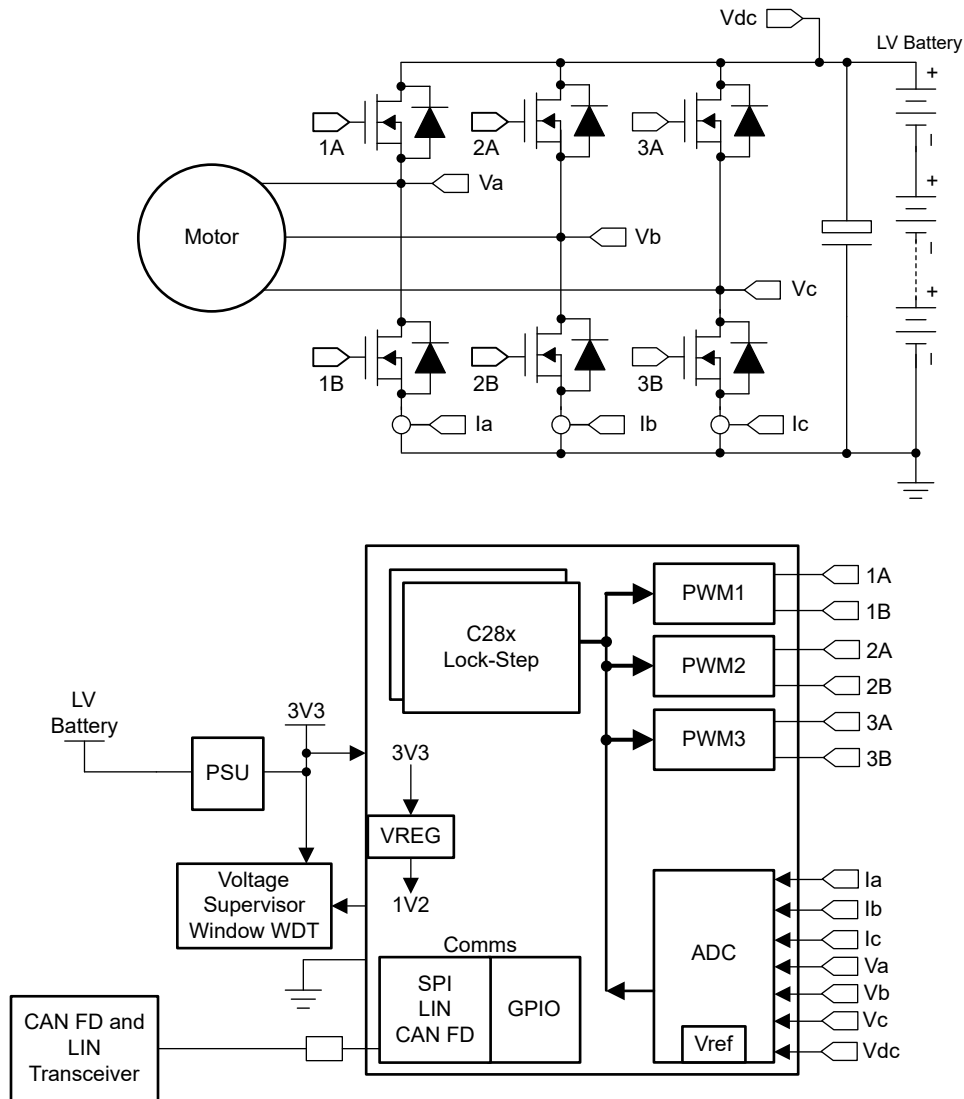


Figure 8-3. Automotive Pump

8.3.1.2.2 Automotive Pump Resources

Reference Designs and Associated Training Videos

[C2000™ MCUs - Electric vehicle \(EV\) training videos](#) (Video)

This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

[TIDA-00281 Automotive 48-V, 1-kW Motor Drive Reference Design](#)

TIDA-00281 is a 3-phase brushless DC (BLDC) motor drive designed to operate in 48-V automotive applications. The board is designed to drive motors in the 1-kW range and can handle currents up to 30 A. The design includes analog circuits working in conjunction with a C2000 LaunchPad™ Development Kit to spin a 3-phase BLDC motor without the need for position feedback from hall effect sensors or quadrature encoder.

8.3.1.3 Positive Temperature Coefficient (PTC) Heater

Heating up the cabin of electric vehicles can be challenging since, in contrast to vehicles with conventional combustion engines, the waste heat available is limited. Therefore, it is necessary to provide a high-voltage

cabin heater for Battery-powered Electric Vehicles (BEVs) and Hybrid Electric Vehicles (HEVs). As part of the heating, ventilation and air-conditioning (HVAC) system: a PTC cabin heater increases the temperature of the air stream coming from the blower.

In HEV/EVs, the sizing or the absence of a combustion engine requires the introduction of two additional components that play a key role in the HVAC system:

- A brushless DC (BLDC) motor is a type of DC motor that rotates the AC compressor, instead of the engine.
- A positive temperature coefficient (PTC) heater or alternatively, a heat pump, heats the coolant, rather than the engine.

Automotive interior heater module designs require:

- Minimized number of isolated components.
- Reduced electromagnetic interference (EMI) to optimize system performance.

8.3.1.3.1 System Block Diagram

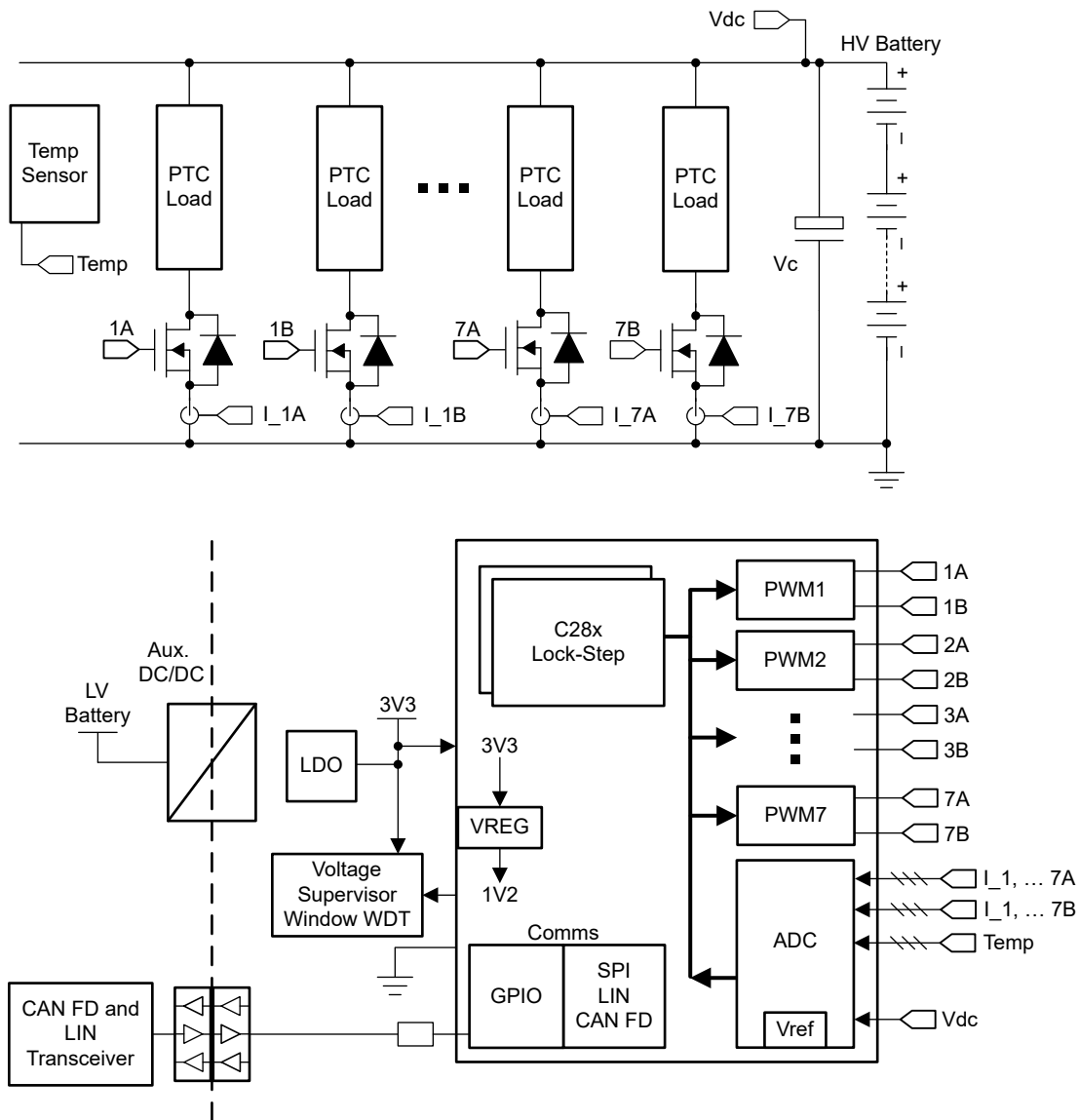


Figure 8-4. PTC

8.3.1.3.2 PTC Resources

Reference Designs and Associated Training Videos

[C2000™ MCUs - Electric vehicle \(EV\) training videos](#) (Video)

This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

[How to design heating and cooling systems for HEV/EVs](#)

In this white paper, we will describe the new heating and cooling control modules in 48-V, 400-V or 800-V HEVs and EVs. From there, you will learn about the unique subsystems in these modules with examples and system diagrams, and we will finish by reviewing functional solutions for these subsystems to help you start planning your implementation

[TIDA-01418 Automotive high voltage, high power motor driver reference design for HVAC compressor](#)

This brushless DC (BLDC) motor reference design controls an automotive HVAC (heating, ventilation, and air conditioning) compressor by using the UCC27712-Q1 high-side and low-side gate driver followed by discrete insulated-gate bipolar transistor (IGBT) half bridges. This reference design uses TI's InstaSPIN software with a three-phase motor control algorithm, which the designer can enable using special libraries in the read-only memory (ROM) of Piccolo microcontrollers (MCUs) and provides expert tools to designers of sensorless (velocity and torque) motor control applications.

8.3.1.4 Automotive HVAC Compressor

In a vehicle, the purpose of a conventional HVAC compressor is to cool the cabin. In hybrid and electric vehicles (HEVs and EVs), the compressor system not only cools the cabin but also the battery which powers the vehicle.

In HEV/EVs, the sizing or the absence of a combustion engine requires the introduction of two additional components that play a key role in the HVAC system:

- A brushless DC (BLDC) motor is a type of DC motor that rotates the AC compressor, instead of the engine.
- A positive temperature coefficient (PTC) heater or alternatively, a heat pump, heats the coolant, rather than the engine.

Automotive HVAC compressor module designs require:

- Minimized number of isolated components.
- Reduced EMI to optimize system performance.
- Comprehensive diagnostics for fault identification.
- High efficiency and sensorless torque control even at low speeds.

8.3.1.4.1 System Block Diagram

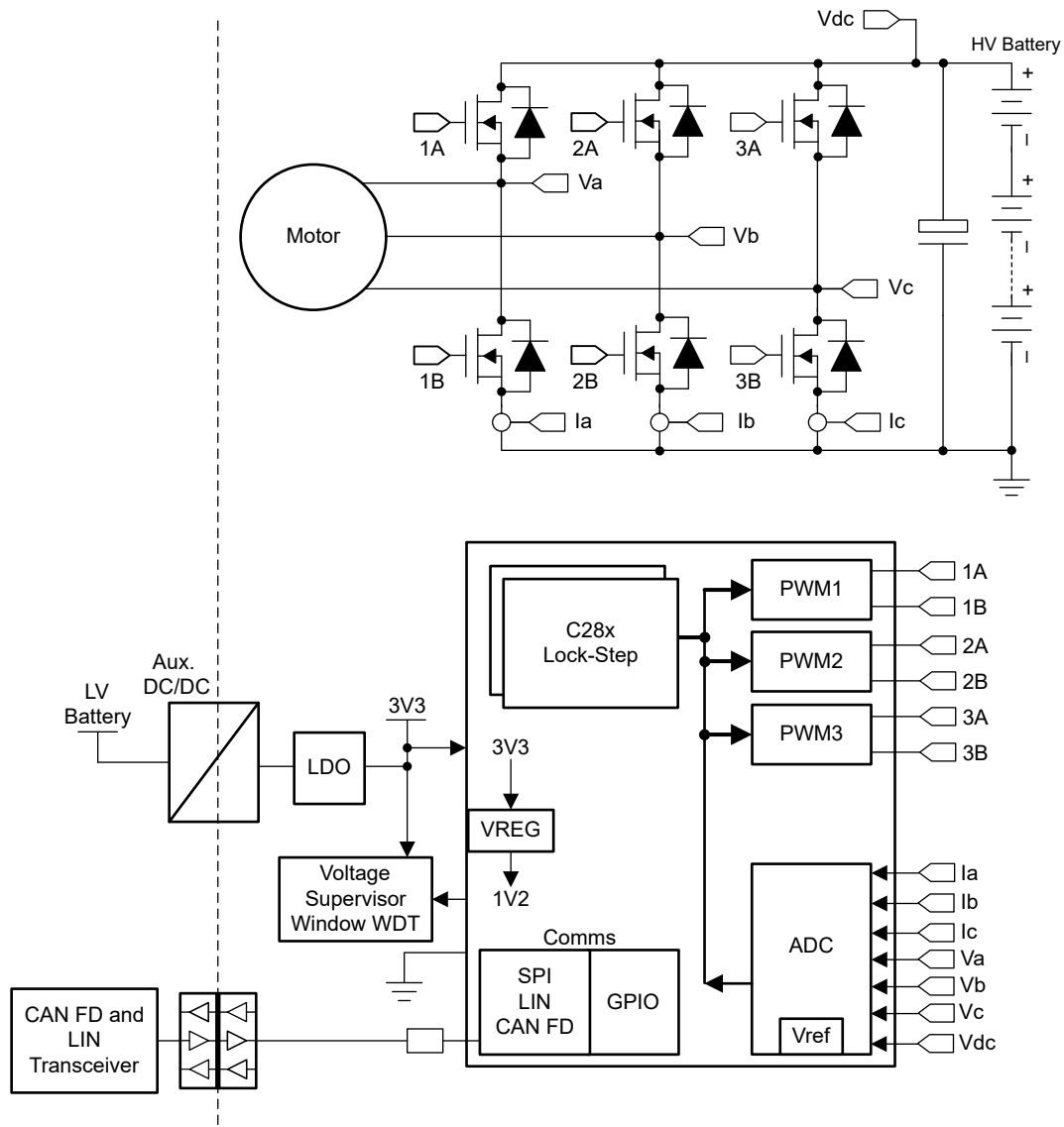


Figure 8-5. Automotive HVAC Compressor

8.3.1.4.2 Automotive HVAC Compressor Resources

Reference Designs and Associated Training Videos

[C2000™ MCUs - Electric vehicle \(EV\) training videos](#) (Video)

This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

[How to design heating and cooling systems for HEV/EVs](#)

In this white paper, we will describe the new heating and cooling control modules in 48-V, 400-V or 800-V HEVs and EVs. From there, you will learn about the unique subsystems in these modules with examples and system diagrams, and we will finish by reviewing functional solutions for these subsystems to help you start planning your implementation

Reliable real-time control in automotive HVAC compressor applications for HEVs and EVs

In this article, we focus on the design challenges of HVAC compressor subsystems within HEV and EV heating and cooling systems and discuss how real-time control can address those challenges.

8.3.1.5 Single-Phase Line-Interactive Uninterruptable Power Supply (UPS)

A line-interactive UPS maintains the DC/AC inverter in line and charges a battery under normal condition when AC power is available. When AC power is lost, the UPS generates AC power from the battery.

For this type of UPS, an AC power inverter is always connected to the output of the UPS. When the input AC power is normal, the inverter of the UPS is in reverse operation (AC/DC mode) and provides battery charging. Once the input power fails, the transfer switch opens and the power flows from the battery to the UPS output. This is indicated in the diagram below. The transfer switches S1 and S2 connect to the "Line_ON" position when AC power is available. When there is a power failure, S1 and S2 take the "Line_OFF" position.

Line-interactive UPS systems are a cheaper option than the online double-conversion technology and will protect a critical load from power failures, power sags, power surges, undervoltage and overvoltage. However, this type of UPS does not protect against electrical line noise, frequency variation, switching transient, and harmonic distortion.

8.3.1.5.1 System Block Diagram

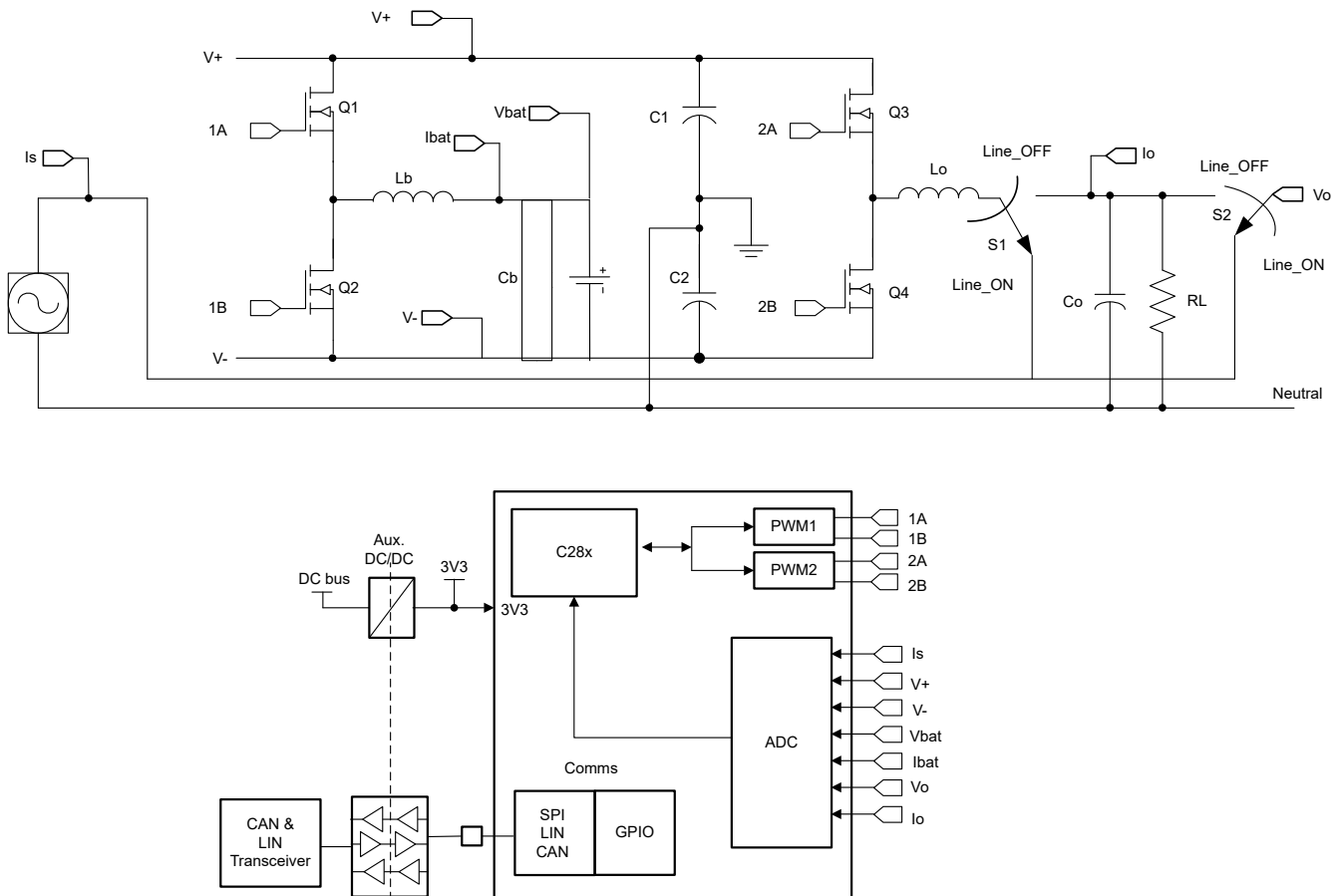


Figure 8-6. Single-Phase Line-Interactive UPS

8.3.1.5.2 Single-Phase Line-Interactive UPS Resources

Reference Designs and Associated Training Videos

[TIDM-02002 CLLLC resonant dual active bridge for HEV/EV onboard charger \(Video\)](#)

The CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

[PMP23069 3.6-kW single-phase totem-pole bridgeless PFC reference design with a > 180-W/in³ power density](#)

This reference design is a GaN-based 3.6-kW single-phase continuous conduction mode (CCM) totem-pole power factor correction (PFC) converter targeting maximum power density. The power stage is followed by a small boost converter, which helps to reduce the size of the bulk capacitor. The LMG3522 top-side cooled GaN with integrated driver and protection enables higher efficiency and reduces power supply size and complexity. The F28004x or F28002x C2000 controller is used for all the advanced controls that includes fast relay control; baby boost operation during AC dropout event; reverse-current-flow protection; and communication between the PFC and the housekeeping controller. The PFC operates at a switching frequency of 65 kHz and achieves peak efficiency of 98.7%.

[TIDUEG2C TIDM-02002 Bidirectional CLLLC resonant dual active bridge \(DAB\) reference design for HEV/EV onboard charger](#)

The CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

[TIDUAI7 TIDM-BIDIR-400-12: Bidirectional 400-V/12-V DC/DC Converter Reference Design](#)

The Bidirectional 400V-12V DC/DC Converter Reference Design is a microcontroller-based implementation of an isolated bidirectional DC-DC converter. A phase-shifted full-bridge (PSFB) with synchronous rectification controls power flow from a 400-V bus/battery to the 12-V battery in step-down mode, while a push-pull stage controls the reverse power flow from the low-voltage battery to the high-voltage bus/battery in boost mode. In this implementation, closed-loop control for both directions of power flow is implemented using a Texas Instruments TMS320F28035 32-bit microcontroller, which is placed on the LV side. This digital controller system can implement advanced control strategies to optimally control the power stage under different conditions and also provide system-level intelligence to make safe and seamless transitions between operation modes and PWM switching patterns.

[TIDM-1000 Vienna Rectifier-Based Three Phase Power Factor Correction Reference Design Using C2000 MCU](#)

The Vienna rectifier power topology is used in high-power, three-phase power factor correction applications such as off-board electric vehicle charging and telecom rectifiers. This design illustrates how to control a Vienna rectifier using a C2000 MCU.

8.3.1.6 AC Drive Power Stage Module

The AC drive power stage module is an electronic device that converts a fixed frequency and voltage to an adjustable frequency and AC voltage source. It controls the speed, torque and direction of an AC motor. The AC drive power stage module is widely used in industrial machinery for converting electrical power to mechanical power (for example, conveyors, elevators, cranes, fans, pumps, and compressors). AC drive power stage modules often require: precise current and voltage sense for speed and torque control in scalar voltage or frequency control or sensored-/sensorless-FOC operation, and robust overcurrent protection against short circuit and shoot.

8.3.1.6.1 System Block Diagram

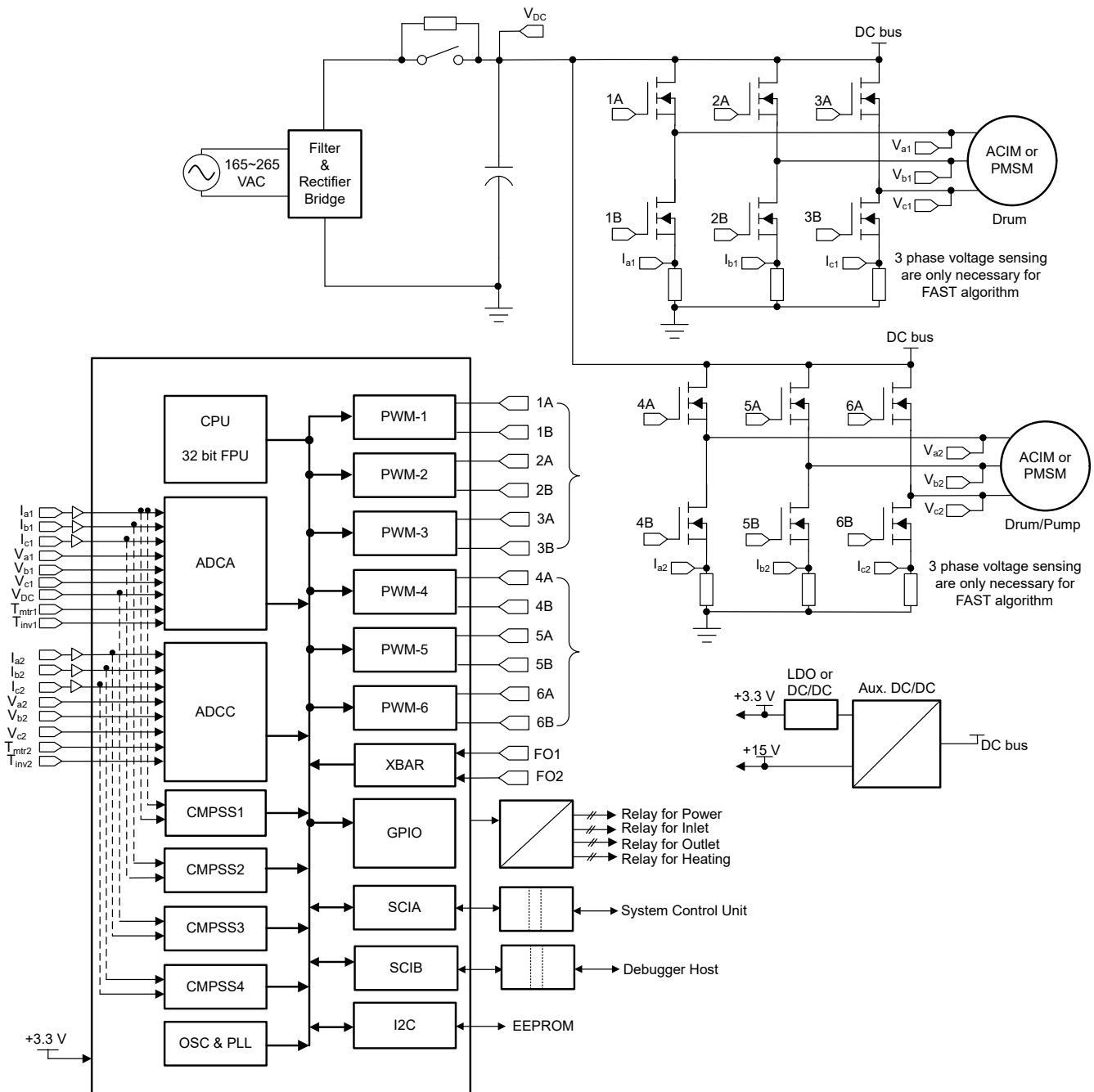


Figure 8-7. Typical Washer and Dryer with Dual-Motor Control Using Three-Shunt Current Sensing

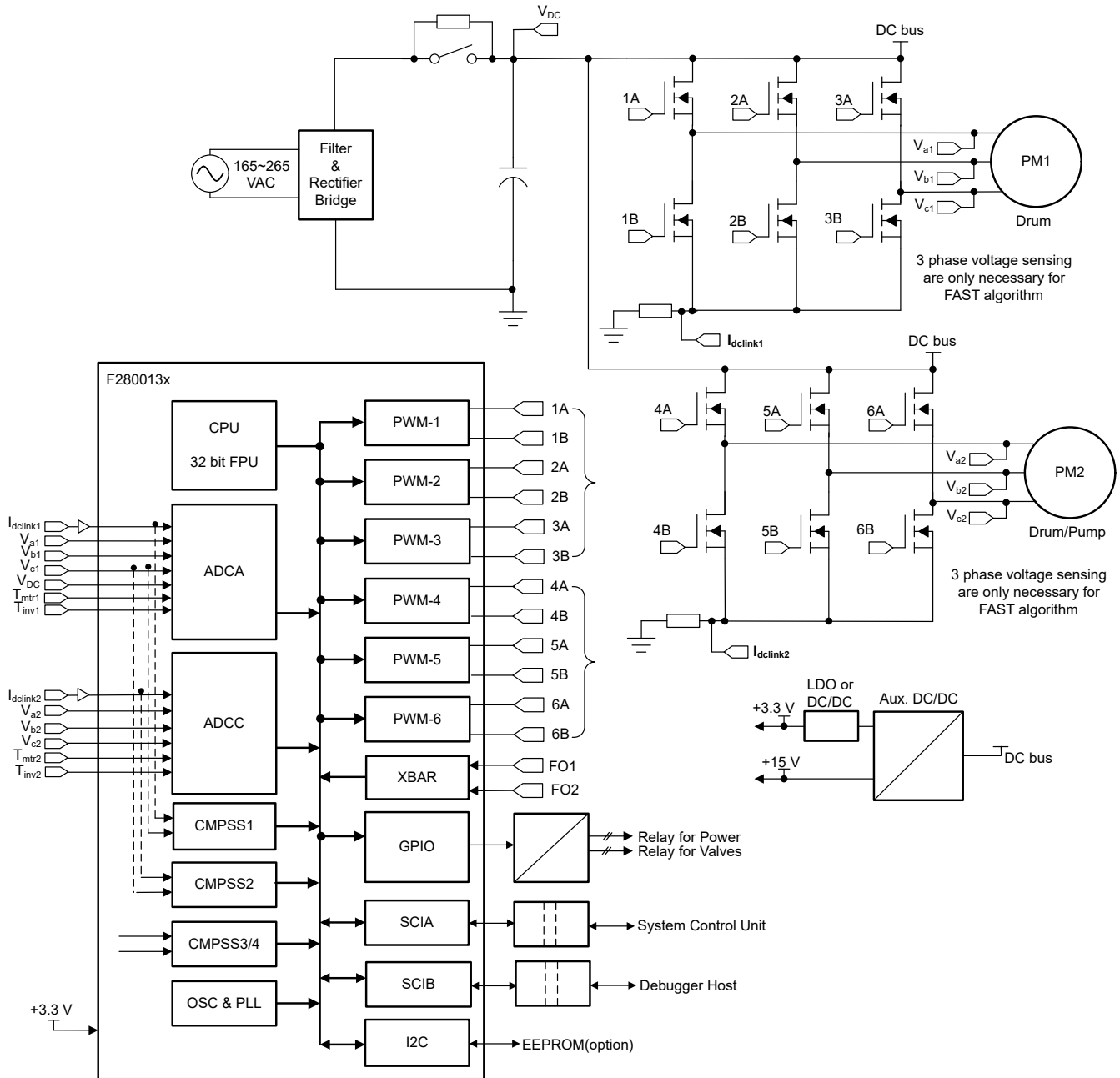


Figure 8-8. Typical Washer and Dryer with Dual-Motor Control Using Single-Shunt Current Sensing

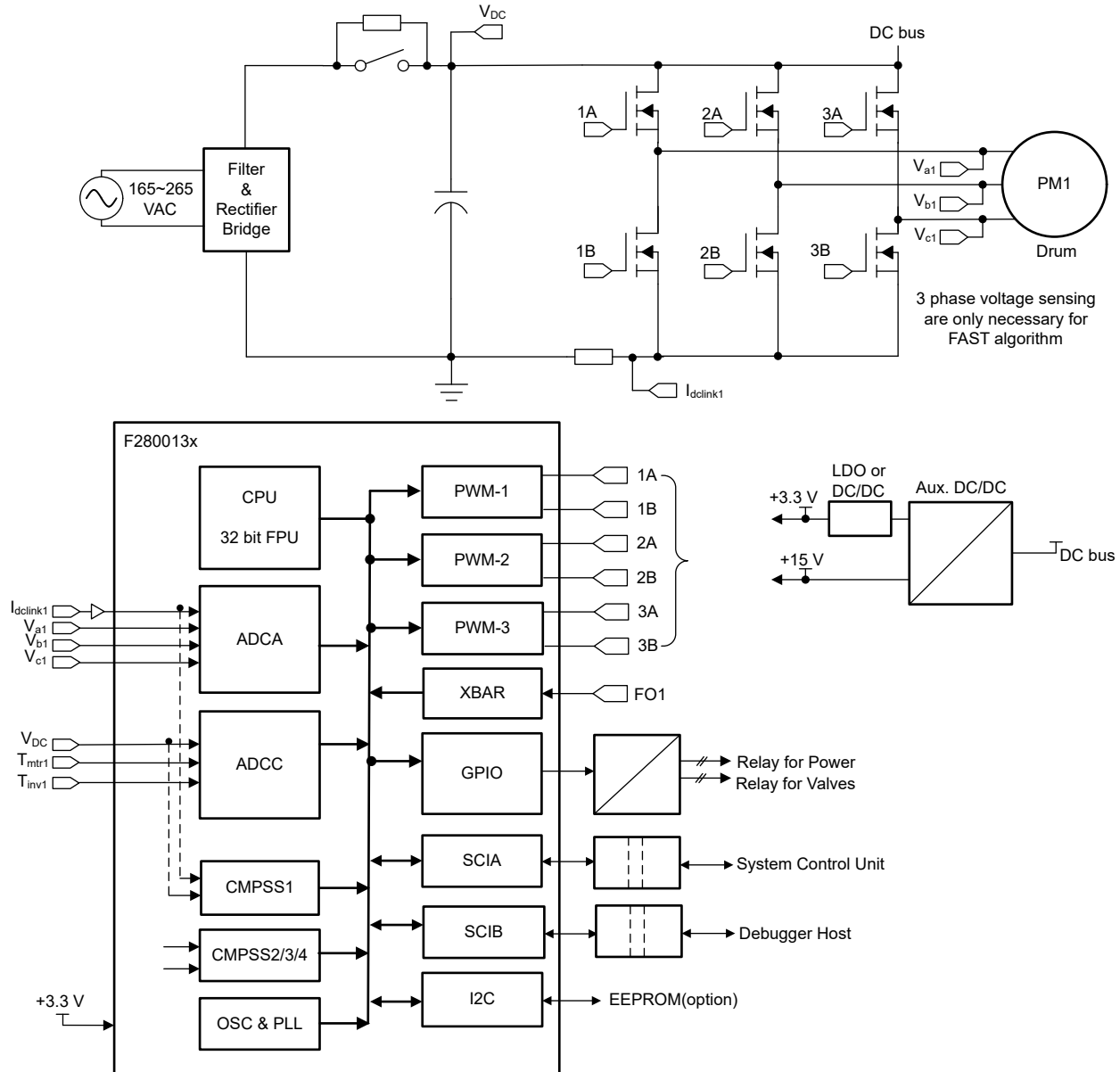


Figure 8-9. Typical Washer and Dryer with One-Motor Control Using Single-Shunt Current Sensing

8.3.1.6.2 AC Drive Power Stage Module Resources

Reference Designs and Associated Training Videos

[TIDM-02010: Dual motor control with digital interleaved PFC for HVAC reference design](#)

The TIDM-02010 reference design is a 1.5-kW dual-motor drive and power factor correction (PFC) control reference design for a variable-frequency air-conditioner outdoor unit controller in HVAC applications. This reference design illustrates a method to implement sensorless 3-phase PMSM vector control for compressor and fan motor drive, and digital interleaved boost PFC for meeting new efficiency standards with a single C2000™ microcontroller. The hardware and software available with this reference design are tested and ready to use to help accelerate development time to market. The reference design includes hardware design files and software codes.

[Universal Motor Control Project and Lab User's Guide](#)

The Universal Motor Control Lab provides an example for motor drive control using a C2000 MCU. This lab is a single project with build examples for different sensorless (FAST™, eSMO, InstaSPIN™-BLDC) and sensed (Incremental Encoder, Hall) motor control techniques (FOC, Trapezoidal). This lab includes system features and debug interfaces that can be used across a variety of three-phase inverter motor evaluation kits or on a customer's own board for washer, dryer, or refrigerator applications. The example codes of this lab are included in the [MotorControl Software Development Kit \(SDK\)](#). The MotorControl SDK (MC SDK) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based motor control system development time targeted for various three-phase motor control applications.

[Variable speed air conditioner \(HVAC\) reference design demo \(Video\)](#)

This video introduces dual-motor control with interleaved PFC for HVAC application design using a single C2000 MCU. The test results achieved on this reference design are also presented as part of this presentation.

8.3.1.7 Server or Telecom Power Supply Unit (PSU)

A server or telecom power supply unit (PSU) consists of a power factor correction (PFC) stage and a DC-DC converter stage. The Totem pole PFC is widely used as the PFC stage. For the DC-DC stage, LLC and phase-shifted full bridge (PSFB) are the two most popular topologies. Usually, current server PSU is based on a two-chip architecture, as shown in [Figure 8-10](#). Telecom PSU is more likely to have a single-chip architecture, as shown in [Figure 8-11](#).

The PFC stage draws sine-wave current from the AC mains in phase with the AC voltage, and maintains a steady DC bus voltage (VDC, typically +400 V) across its output. This output voltage is applied to the input of DC-DC stage, which converts it to an isolated low-output voltage V_{out} (12 V/48 V for server, 48 V for telecom).

8.3.1.7.1 System Block Diagram

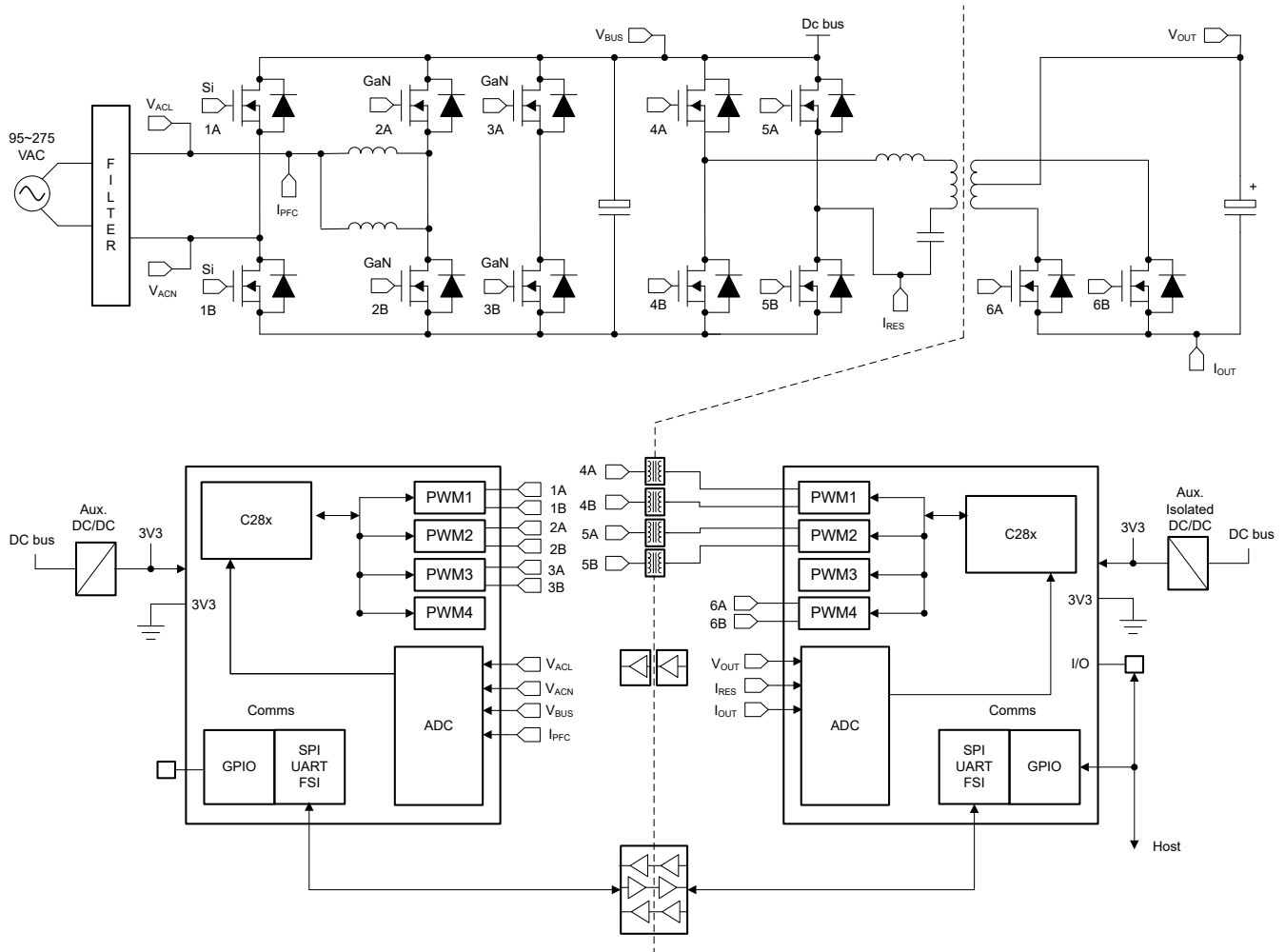


Figure 8-10. Typical Server PSU Architecture

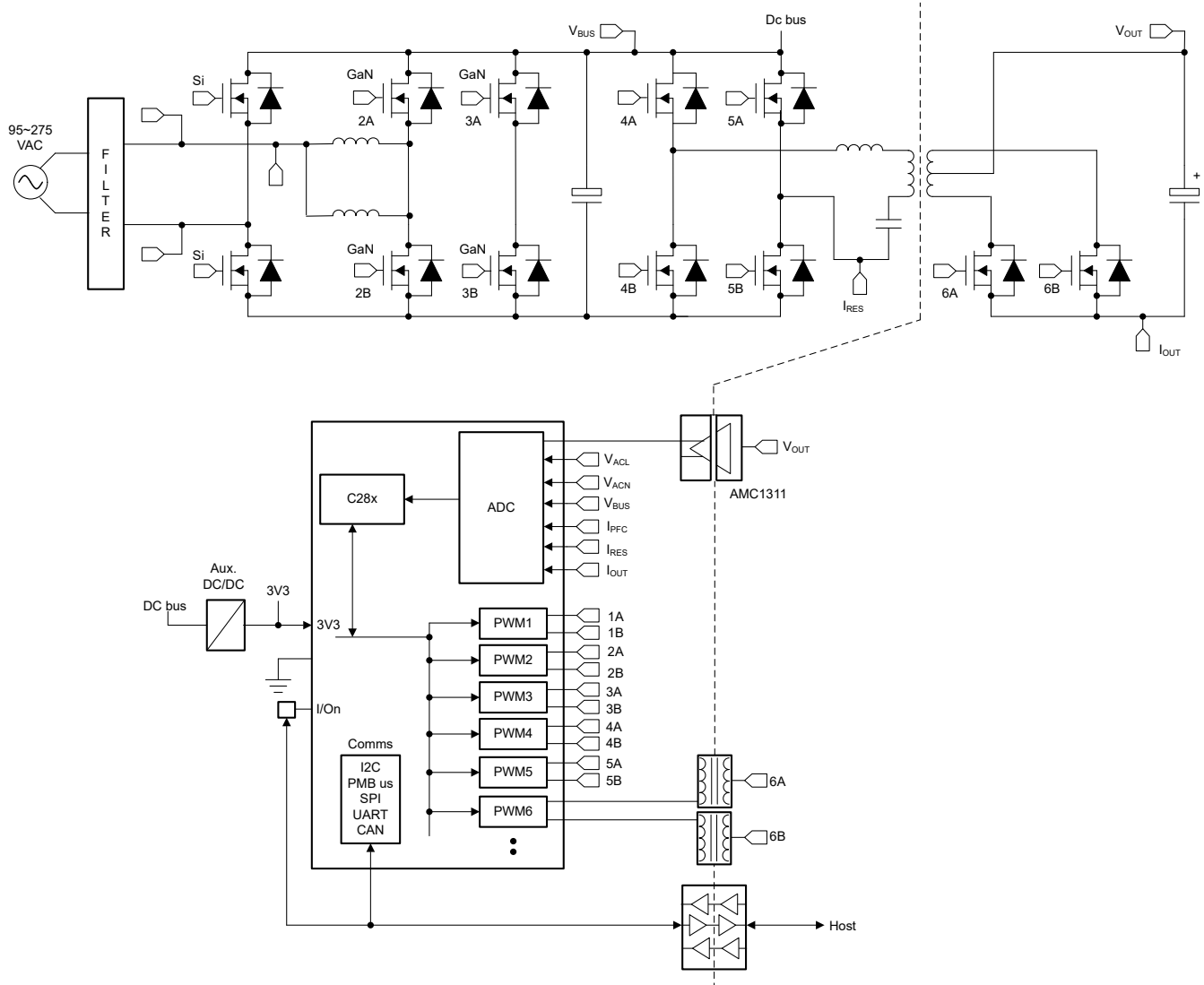


Figure 8-11. Typical Telecom PSU Architecture

8.3.1.7.2 Server or Telecom PSU Resources

Reference Designs and Associated Training Videos

[TIDM-1007 High efficiency GaN CCM totem pole bridgeless Power Factor Correction \(PFC\) reference design](#)

Interleaved Continuous Conduction Mode (CCM) Totem Pole (TTPL) Bridgeless Power Factor Correction (PFC) is an attractive power topology with the use of high band-gap GaN devices because of high efficiency and the reduced size of the power supply. This design illustrates a method to control this power stage using C2000 MCUs and the LMG3410 GaN FET module. Adaptive dead time and phase-shedding methods are implemented for improved efficiency. The Nonlinear Voltage Compensator is designed to reduce overshoot and undershoot during transients. A software phase-locked loop (SPLL) based scheme is chosen to drive the totem pole bridge accurately. The hardware and software available with this design help accelerate your time to market.

[TIDM-1007 Interleaved CCM Totem Pole PFC Reference Design \(Video\)](#)

This video covers the hardware aspects, the control aspects, and the software design that are required to control a totem-pole PFC using a C2000 microcontroller. The test results achieved on this reference design are also presented as part of this presentation.

[TIDA-010203 4-kW single-phase totem pole PFC reference design with C2000 and GaN](#)

This reference design is a 4-kW CCM totem-pole PFC with a F280049/F280025 control card and an LMG342x EVM board. This design demonstrates a robust PFC solution, which avoids isolated current sense by putting the controller's ground in the middle of a MOSFET leg. Benefitting from non-isolation, AC current sense can be implemented by high-speed amplifier OPA607, helping to realize reliable overcurrent protection. In this design, efficiency, thermal image, AC drop, lighting surge, and EMI CE are fully validated. With completed test data, this reference design shows the maturity of totem-pole PFC with C2000 and GaN, and is a good study platform for high-efficiency products' PFC stage design.

[High efficiency PFC stage using GaN and C2000™ Real-time control MCUs \(Video\)](#)

GaN power FETs and C2000™ MCUs enable a totem-pole Power Factor Correction (PFC) topology, eliminating bridge rectifier power losses.

[TIDM-02000 Peak current-mode controlled phase-shifted full-bridge reference design using C2000™ real-time MCU](#)

This design implements a digitally peak current mode-controlled (PCMC) phase-shifted full bridge (PSFB) DC-DC converter that converts a 400-V DC input to a regulated 12-V DC output. Novel PCMC waveform generation based on the type-4 PWM and internal slope compensation; and simple PCMC implementation are the highlights of this design. A TMS320F280049C MCU from the C2000 real-time microcontroller family is used.

[TIDA-010062 1-kW, 80 Plus titanium, GaN CCM totem pole bridgeless PFC and half-bridge LLC reference design](#)

This reference design is a digitally controlled, compact 1-kW AC/DC power supply design for server power supply unit (PSU) and telecom rectifier applications. The highly efficient design supports two main power stages, including a front-end continuous conduction mode (CCM) totem-pole bridgeless power factor correction (PFC) stage. The PFC stage features an LMG341x GaN FET with integrated driver to provide enhanced efficiency across a wide load range and meet 80-plus titanium requirements. The design also supports a half-bridge LLC isolated DC/DC stage to achieve a +12-V DC output at 1-kW. Two control cards use C2000™ [Entry-Performance MCUs](#) to control both power stages.

[TIDM-1001 Two Phase Interleaved LLC Resonant Converter Reference Design Using C2000™ MCUs](#)

Resonant converters are popular DC-DC converters frequently used in server, telecom, automotive, industrial, and other power supply applications. Their high performance (efficiency, power density, etc.), improving requirements of the various industry standards, and the ever-increasing power density goals have made these converters a good choice for medium- to high-power applications.

This design implements a digitally controlled 500-W two-phase interleaved LLC resonant converter. The system is controlled by a single C2000™ microcontroller (MCU), TMS320F280025C, which also generates PWM waveforms for all power electronic switching devices under all operating modes. This design implements a novel current-sharing technique to accurately achieve current-balancing between phases.

For more information, see [Merchant network & server PSU](#).

[Hardware Design Guide for F2800x C2000™ Real-Time MCU Series](#)

This is an essential guide for hardware developers using C2000 devices and helps streamline the design process while mitigating the potential for faulty designs. Key topics discussed include: power requirements; general-purpose input/output (GPIO) connections; analog inputs and ADC; clocking generation and requirements; and JTAG debugging, among many others.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Getting Started and Next Steps

The [Getting Started With C2000™ Real-Time Control Microcontrollers \(MCUs\) Getting Started Guide](#) covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

9.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS320F2800155**). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX and TMDX) through fully qualified production devices and tools (TMS and TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

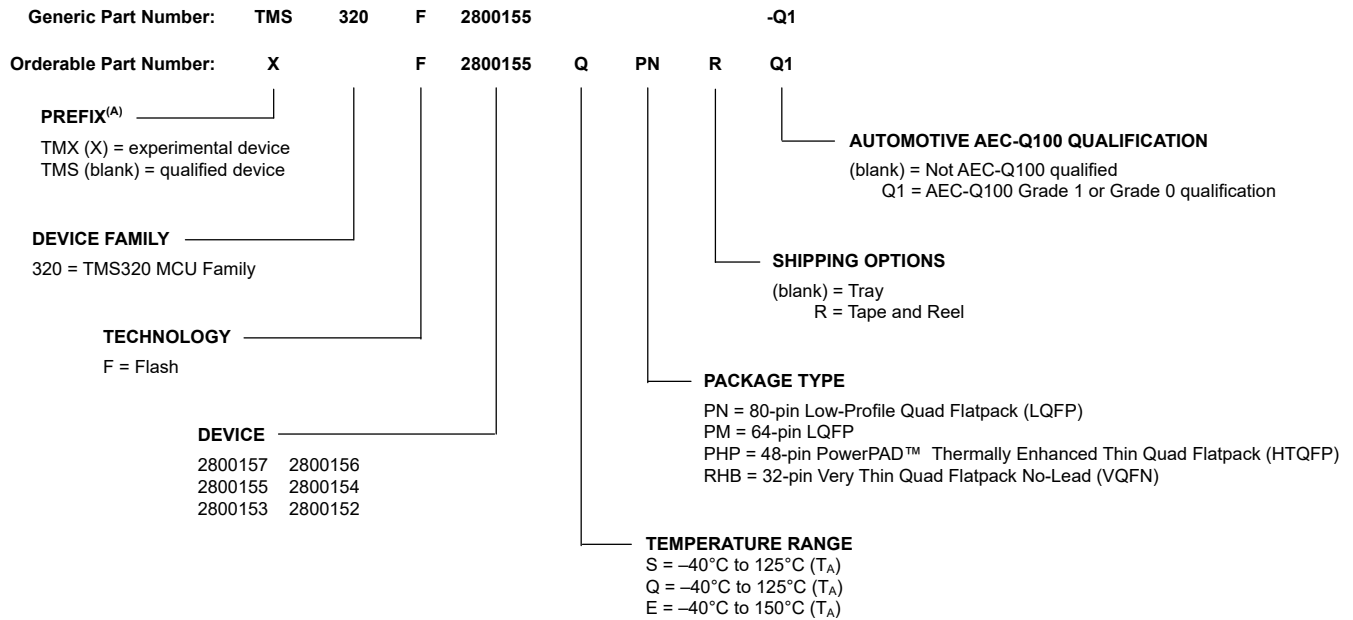
Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PN) and temperature range (for example, Q).

For orderable part numbers of TMS320F280015x devices in the PN, PM, PHP, and RHB package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the [TMS320F280015x Real-Time MCUs Silicon Errata](#).



A. Prefix X is used in orderable part numbers.

Figure 9-1. Device Nomenclature

9.3 Markings

Figure 9-2, Figure 9-3, Figure 9-4, Figure 9-5, Figure 9-6, Figure 9-7, Figure 9-8, and Figure 9-9 show the package symbolization. Table 9-1 lists the silicon revision codes.

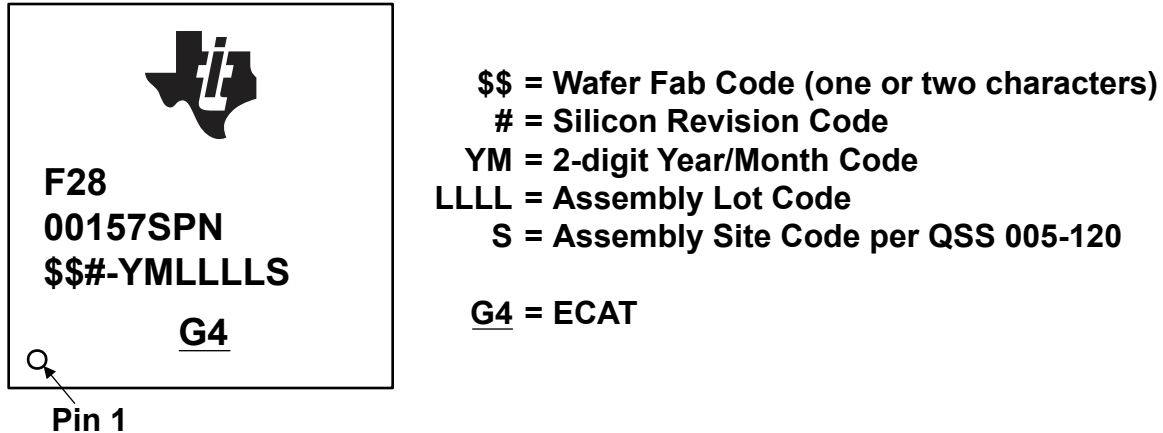
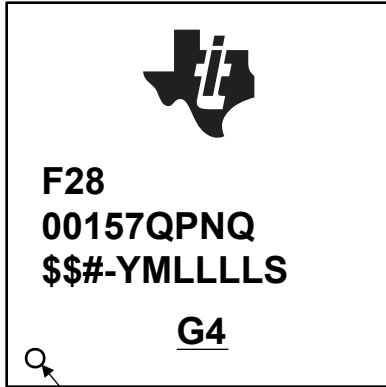


Figure 9-2. Package Symbolization for PN Package

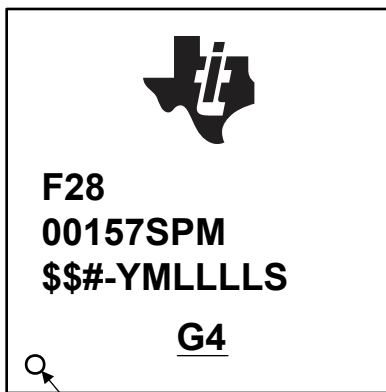


Pin 1

Figure 9-3. Package Symbolization for PN Package (AEC-Q100 Grade 1 Qualification)

\$\$ = Wafer Fab Code (one or two characters)
= Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code per QSS 005-120

G4 = ECAT

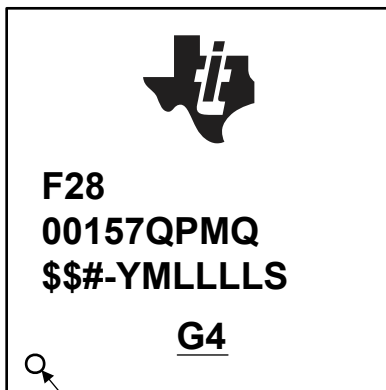


Pin 1

Figure 9-4. Package Symbolization for PM Package

\$\$ = Wafer Fab Code (one or two characters)
= Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code per QSS 005-120

G4 = ECAT

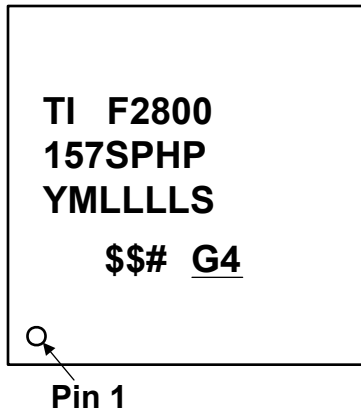


Pin 1

Figure 9-5. Package Symbolization for PM Package (AEC-Q100 Grade 1 Qualification)

\$\$ = Wafer Fab Code (one or two characters)
= Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code per QSS 005-120

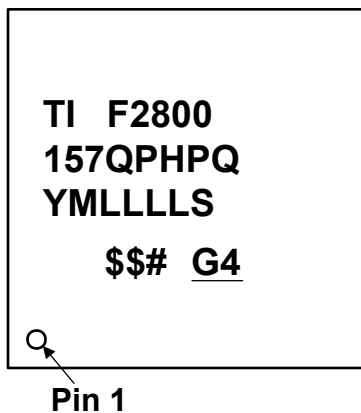
G4 = ECAT



\$\$ = Wafer Fab Code (one or two characters)
= Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code per QSS 005-120

G4 = ECAT

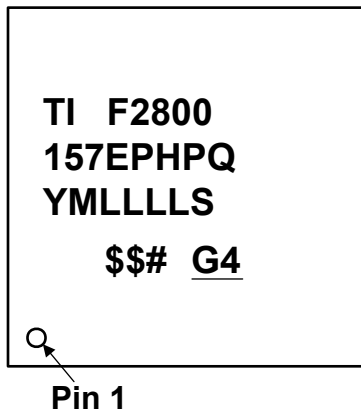
Figure 9-6. Package Symbolization for PHP Package



\$\$ = Wafer Fab Code (one or two characters)
= Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code per QSS 005-120

G4 = ECAT

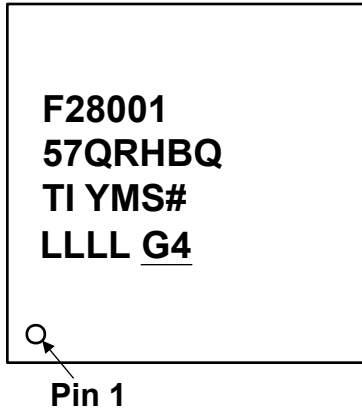
Figure 9-7. Package Symbolization for PHP Package (AEC-Q100 Grade 1 Qualification)



\$\$ = Wafer Fab Code (one or two characters)
= Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code per QSS 005-120

G4 = ECAT

Figure 9-8. Package Symbolization for PHP Package (AEC-Q100 Grade 0 Qualification)



= Silicon Revision Code
 YM = 2-digit Year/Month Code
 LLLL = Assembly Lot Code
 S = Assembly Site Code per QSS 005-120

 G4 = ECAT

Figure 9-9. Package Symbolization for RHB Package (AEC-Q100 Grade 1 Qualification)

Table 9-1. Revision Identification

| SILICON REVISION CODE | SILICON REVISION | REVID ⁽¹⁾ Address: 0x5D00C | COMMENTS |
|-----------------------|------------------|------------------------------------------|---------------------------------------------------------|
| Blank | 0 | 0x0000 0001 | This silicon revision is available as TMX. |
| A | A | 0x0000 0002 | This silicon revision is available as both TMX and TMS. |
| B | B | 0x0000 0003 | This silicon revision is available as TMS. |

(1) Silicon Revision ID

9.4 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions follow. To view all available tools and software for C2000™ real-time control MCUs, visit the [C2000 real-time control MCUs – Design & development](#) page.

Development Tools

[TI Resource Explorer](#)

To enhance your experience, be sure to check out the TI Resource Explorer to browse examples, libraries, and documentation for your applications.

Software Tools

[C2000Ware for C2000 MCUs](#)

C2000Ware for C2000™ MCUs is a cohesive set of software and documentation created to minimize development time. It includes device-specific drivers, libraries, and peripheral examples.

[DigitalPower SDK](#)

DigitalPower SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based digital power system development time targeted for various AC-DC, DC-DC and DC-AC power supply applications. The software includes firmware that runs on C2000 digital power evaluation modules (EVMs) and TI designs (TIDs), which are targeted for solar, telecom, server, electric vehicle chargers and industrial power delivery applications. DigitalPower SDK provides all the needed resources at every stage of development and evaluation in a digital power applications.

[MotorControl SDK](#)

MotorControl SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI designs (TIDs), which are targeted for industrial drive and other motor control, MotorControl SDK provides all the needed resources at every stage of development and evaluation for high-performance motor control applications.

[Code Composer Studio™ integrated development environment \(IDE\)](#)

Code Composer Studio is an integrated development environment (IDE) for TI's microcontrollers and processors. It comprises a suite of tools used to develop and debug embedded applications. Code Composer Studio is available for download across Windows®, Linux® and macOS® desktops. It can also be used in the cloud by visiting <https://dev.ti.com>. Code Composer Studio includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler and many other features. The intuitive IDE takes you through each step of the application development flow. Familiar tools and interfaces make getting started faster than ever before. The desktop version of Code Composer Studio combines the advantages of the Eclipse software framework with advanced capabilities from TI resulting in a compelling feature-rich environment. The cloud-based Code Composer Studio leverages the Theia application framework enabling development in the cloud without needing to download and install large amounts of software.

[SysConfig System configuration tool](#)

SysConfig is a comprehensive collection of graphical utilities for configuring pins, peripherals, radios, subsystems, and other components. SysConfig helps you manage, expose and resolve conflicts visually so that you have more time to create differentiated applications. The tool's output includes C header and code files that can be used with software development kit (SDK) examples or used to configure custom software. The SysConfig tool automatically selects the pinmux settings that satisfy the entered requirements. The SysConfig tool is delivered integrated in CCS, as a standalone installer, or can be used via the dev.ti.com cloud tools portal. For more information about the SysConfig system configuration tool, visit the [System configuration tool](#) page.

[C2000 Third-party search tool](#)

TI has partnered with multiple companies to offer a wide range of solutions and services for TI C2000 devices. These companies can accelerate your path to production using C2000 devices. Download this search tool to quickly browse third-party details and find the right third-party to meet your needs.

UniFlash Standalone Flash Tool

UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

Models

Various models are available for download from the product Design & development pages. These models include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the Design tools & simulation section of the Design & development page for each device.

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the [C2000™ real-time control MCUs – Support & training](#) site.

9.5 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral follows.

Errata

[TMS320F280015x Real-Time MCUs Silicon Errata](#) describes known advisories on silicon and provides workarounds.

Technical Reference Manual

[TMS320F280015x Real-Time Microcontrollers Technical Reference Manual](#) details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the F280015x real-time microcontrollers.

CPU User's Guides

[TMS320C28x CPU and Instruction Set Reference Guide](#) describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

[TMS320C28x Extended Instruction Sets Technical Reference Manual](#) describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

Peripheral Guides

[C2000 Real-Time Control Peripherals Reference Guide](#) describes the peripheral reference guides of the 28x DSPs.

Tools Guides

[TMS320C28x Assembly Language Tools v22.6.0.LTS User's Guide](#) describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

[TMS320C28x Optimizing C/C++ Compiler v22.6.0.LTS User's Guide](#) describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

Application Reports

The [SMT & packaging application notes](#) website lists documentation on TI's surface mount technology (SMT) and application notes on a variety of packaging-related topics.

[Semiconductor Packing Methodology](#) describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

[Calculating Useful Lifetimes of Embedded Processors](#) provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

[An Introduction to IBIS \(I/O Buffer Information Specification\) Modeling](#) discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures, and future trends.

[Serial Flash Programming of C2000™ Microcontrollers](#) discusses using a flash kernel and ROM loaders for serial programming a device.

[The Essential Guide for Developing With C2000™ Real-Time Microcontrollers](#) provides a deeper look into the components that differentiate the C2000 Microcontroller Unit (MCU) as it pertains to Real-Time Control Systems.

9.6 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.7 Trademarks

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9.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.9 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from July 4, 2023 to November 20, 2023 (from Revision A (July 2023) to Revision B (November 2023))

| | Page |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Global: Information on the TMS320F2800156-Q1 (Grade 1), TMS320F2800155-Q1, TMS320F2800155, TMS320F2800154-Q1, TMS320F2800153-Q1, and TMS320F2800152-Q1 devices is now Production Data.. | 1 |
| • Global: Information on the TMS320F2800157-Q1 (Grade 0) and TMS320F2800156-Q1 (Grade 0) devices is preview information only (not Production Data)..... | 1 |
| • <i>Features</i> section: Changed Security features under "On-chip memory" feature..... | 1 |
| • <i>Features</i> section: Updated "Functional Safety-Compliant" features. Updated "Safety-related certification" features. Added link to Functional Safety Certificate..... | 1 |
| • <i>Package Information</i> table: Removed "Preview information (not Production Data)" footnote..... | 2 |
| • <i>Device Comparison</i> table: Changed "Code security for on-chip flash and RAM" to "Security: JTAGLOCK, Zero-pin boot, Dual-zone security"..... | 7 |
| • <i>Device Comparison</i> table: Changed footnote about preview information..... | 7 |
| • <i>Digital Inputs and Outputs on ADC Pins (AGPIOs)</i> section: Updated section..... | 41 |
| • <i>Current Consumption Graphs</i> section added..... | 55 |
| • <i>Operating Mode Power Example</i> table footnote updated to clarify T _A 150°C values as estimated maximum allowable values..... | 60 |
| • <i>External Supervisor Usage</i> section: Updated section..... | 63 |
| • <i>Supply Slew Rate</i> section: Updated section..... | 68 |
| • <i>Recommended Operating Conditions Applicability to the PMM</i> section: Added section..... | 68 |
| • <i>Testing</i> section: Updated section..... | 84 |
| • <i>RAM Parameters</i> table: Updated table..... | 92 |
| • <i>ROM Parameters</i> table: Updated table..... | 92 |
| • <i>ADC Electrical Data and Timing</i> section: Updated "The ADC inputs should be kept below VDDA + 0.3 V ..." note..... | 115 |
| • <i>Block Diagram</i> section: Added "Each reference 12-bit DAC can be configured to drive a reference voltage into the negative input of the respective comparator" paragraph. Added "Reference DAC Block Diagram" figure..... | 125 |
| • <i>I2C Electrical Data and Timing</i> section: Updated "A pullup resistor must be chosen to meet the I2C standard timings ..." paragraph in Note..... | 150 |
| • <i>I2C Timing Requirements</i> table: Added footnotes..... | 150 |
| • <i>Lockstep Compare Module (LCM)</i> section: Updated section..... | 178 |
| • <i>Security</i> section: Changed <i>Dual Code Security Module</i> section to <i>Security</i> section..... | 188 |
| • <i>Functional Safety</i> section: Added section..... | 192 |
| • <i>Automotive Pump Resources</i> section: Updated list of Reference Designs and Associated Training Videos. | 200 |
| • <i>Automotive HVAC Compressor Resources</i> section: Updated list of Reference Designs and Associated Training Videos..... | 203 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| F2800152QPHPRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F2800 152QPHPQ | Samples |
| F2800152QRHBRQ1 | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | F28001 52QRHBQ | Samples |
| F2800153QPHPRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F2800 153QPHPQ | Samples |
| F2800153QRHBRQ1 | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | F28001 53QRHBQ | Samples |
| F2800154QPHPRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F2800 154QPHPQ | Samples |
| F2800154QPMRQ1 | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00154QPMQ F28 | Samples |
| F2800154QPNRQ1 | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00154QPNQ F28 | Samples |
| F2800154QRHBRQ1 | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | F28001 54QRHBQ | Samples |
| F2800155QPHPRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F2800 155QPHPQ | Samples |
| F2800155QPMRQ1 | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00155QPMQ F28 | Samples |
| F2800155QPNRQ1 | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00155QPNQ F28 | Samples |
| F2800155QRHBRQ1 | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | F28001 55QRHBQ | Samples |
| F2800155SPHPR | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F2800 155SPHP | Samples |
| F2800155SPMR | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00155SPM F28 | Samples |
| F2800155SPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00155SPN F28 | Samples |
| F2800156EPHPQ1 | ACTIVE | HTQFP | PHP | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 150 | F2800 156EPHPQ | Samples |
| F2800156EPHRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 150 | F2800 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| | | | | | | | | | | 156EPHPQ | |
| F2800156QPHPQ1 | ACTIVE | HTQFP | PHP | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F2800 156QPHPQ | Samples |
| F2800156QPHPRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F2800 156QPHPQ | Samples |
| F2800156QPMQ1 | ACTIVE | LQFP | PM | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00156QPMQ F28 | Samples |
| F2800156QPMRQ1 | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00156QPMQ F28 | Samples |
| F2800156QPQ1 | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00156QPQ F28 | Samples |
| F2800156QPNRQ1 | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00156QPNQ F28 | Samples |
| F2800156QRHBRQ1 | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | F28001 56QRHBQ | Samples |
| F2800157EPHPQ1 | ACTIVE | HTQFP | PHP | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 150 | F2800 157EPHPQ | Samples |
| F2800157EPHPRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 150 | F2800 157EPHPQ | Samples |
| F2800157QPHPQ1 | ACTIVE | HTQFP | PHP | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F2800 157QPHPQ | Samples |
| F2800157QPHPRQ1 | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F2800 157QPHPQ | Samples |
| F2800157QPMQ1 | ACTIVE | LQFP | PM | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00157QPMQ F28 | Samples |
| F2800157QPMRQ1 | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00157QPMQ F28 | Samples |
| F2800157QPQ1 | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00157QPQ F28 | Samples |
| F2800157QPNRQ1 | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00157QPNQ F28 | Samples |
| F2800157QRHBRQ1 | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | F28001 57QRHBQ | Samples |
| F2800157SPHP | ACTIVE | HTQFP | PHP | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F2800 157SPHP | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| F2800157SPHPR | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F2800 157SPHP | Samples |
| F2800157SPM | ACTIVE | LQFP | PM | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00157SPM F28 | Samples |
| F2800157SPMR | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00157SPM F28 | Samples |
| F2800157SPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00157SPN F28 | Samples |
| F2800157SPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 00157SPN F28 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF TMS320F2800155, TMS320F2800155-Q1, TMS320F2800157, TMS320F2800157-Q1 :

- Catalog : [TMS320F2800155](#), [TMS320F2800157](#)
- Automotive : [TMS320F2800155-Q1](#), [TMS320F2800157-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| F2800152QPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| F2800152QRHBRQ1 | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| F2800153QPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| F2800153QRHBRQ1 | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| F2800154QPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| F2800154QPMPRQ1 | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F2800154QPNRQ1 | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 16.0 | 16.0 | 2.0 | 24.0 | 24.0 | Q2 |
| F2800154QRHBRQ1 | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| F2800155QPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| F2800155QPMPRQ1 | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F2800155QPNRQ1 | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 16.0 | 16.0 | 2.0 | 24.0 | 24.0 | Q2 |
| F2800155QRHBRQ1 | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| F2800155SPHPR | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| F2800155SPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F2800155SPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 16.0 | 16.0 | 2.0 | 24.0 | 24.0 | Q2 |
| F2800156EPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |

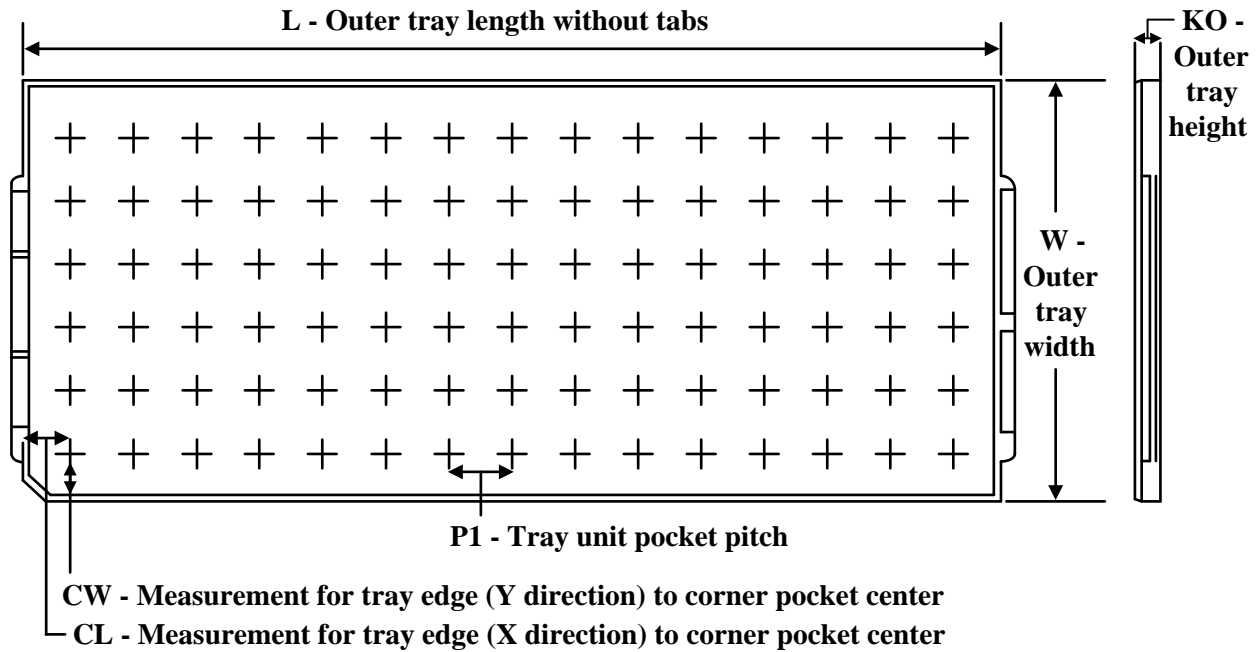
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| F2800156QPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| F2800156QPMRQ1 | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F2800156QPNRQ1 | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 16.0 | 16.0 | 2.0 | 24.0 | 24.0 | Q2 |
| F2800156QRHBRQ1 | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| F2800157EPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| F2800157QPHPRQ1 | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| F2800157QPMRQ1 | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F2800157QPNRQ1 | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 16.0 | 16.0 | 2.0 | 24.0 | 24.0 | Q2 |
| F2800157QRHBRQ1 | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| F2800157SPHPR | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| F2800157SPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F2800157SPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 16.0 | 16.0 | 2.0 | 24.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| F2800152QPHPRQ1 | HTQFP | PHP | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F2800152QRHBRQ1 | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| F2800153QPHPRQ1 | HTQFP | PHP | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F2800153QRHBRQ1 | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| F2800154QPHPRQ1 | HTQFP | PHP | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F2800154QPMRQ1 | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F2800154QPNRQ1 | LQFP | PN | 80 | 1000 | 367.0 | 367.0 | 55.0 |
| F2800154QRHBRQ1 | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| F2800155QPHPRQ1 | HTQFP | PHP | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F2800155QPMRQ1 | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F2800155QPNRQ1 | LQFP | PN | 80 | 1000 | 367.0 | 367.0 | 55.0 |
| F2800155QRHBRQ1 | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| F2800155SPHPR | HTQFP | PHP | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F2800155SPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F2800155SPNR | LQFP | PN | 80 | 1000 | 367.0 | 367.0 | 55.0 |
| F2800156EPHPRQ1 | HTQFP | PHP | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F2800156QPHPRQ1 | HTQFP | PHP | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F2800156QPMRQ1 | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| F2800156QPNRQ1 | LQFP | PN | 80 | 1000 | 367.0 | 367.0 | 55.0 |
| F2800156QRHBRQ1 | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| F2800157EPHPRQ1 | HTQFP | PHP | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F2800157QPHPRQ1 | HTQFP | PHP | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F2800157QPMRQ1 | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F2800157QPNRQ1 | LQFP | PN | 80 | 1000 | 367.0 | 367.0 | 55.0 |
| F2800157QRHBRQ1 | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| F2800157SPHPR | HTQFP | PHP | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F2800157SPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F2800157SPNR | LQFP | PN | 80 | 1000 | 367.0 | 367.0 | 55.0 |

TRAY


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|----------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| F2800156EPHPQ1 | PHP | HTQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| F2800156QPHPQ1 | PHP | HTQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| F2800156QPMQ1 | PM | LQFP | 64 | 160 | 8 X 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |
| F2800156QPNQ1 | PN | LQFP | 80 | 119 | 7 X 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| F2800157EPHPQ1 | PHP | HTQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| F2800157QPHPQ1 | PHP | HTQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| F2800157QPMQ1 | PM | LQFP | 64 | 160 | 8 X 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |
| F2800157QPNQ1 | PN | LQFP | 80 | 119 | 7 X 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| F2800157SPHP | PHP | HTQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| F2800157SPM | PM | LQFP | 64 | 160 | 8 X 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |
| F2800157SPN | PN | LQFP | 80 | 119 | 7 X 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |

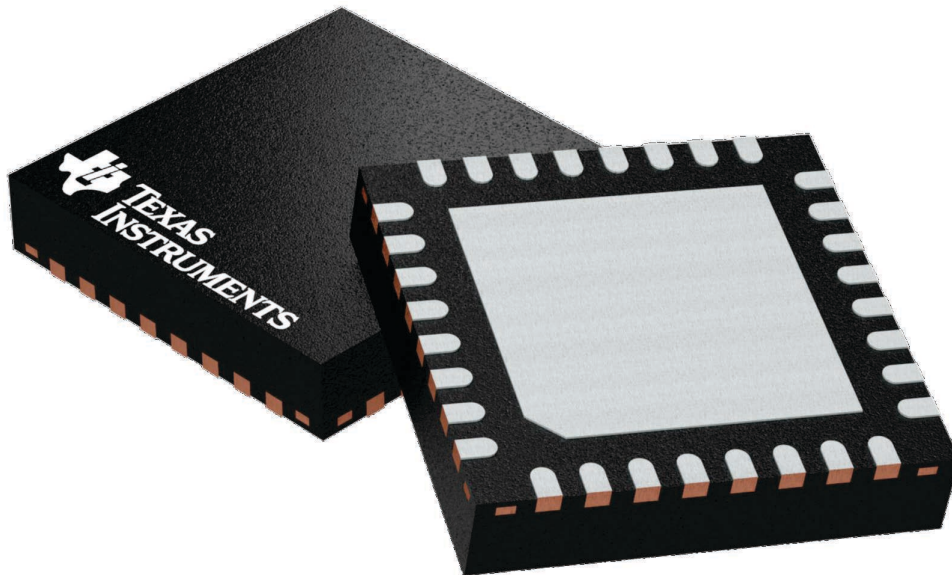
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

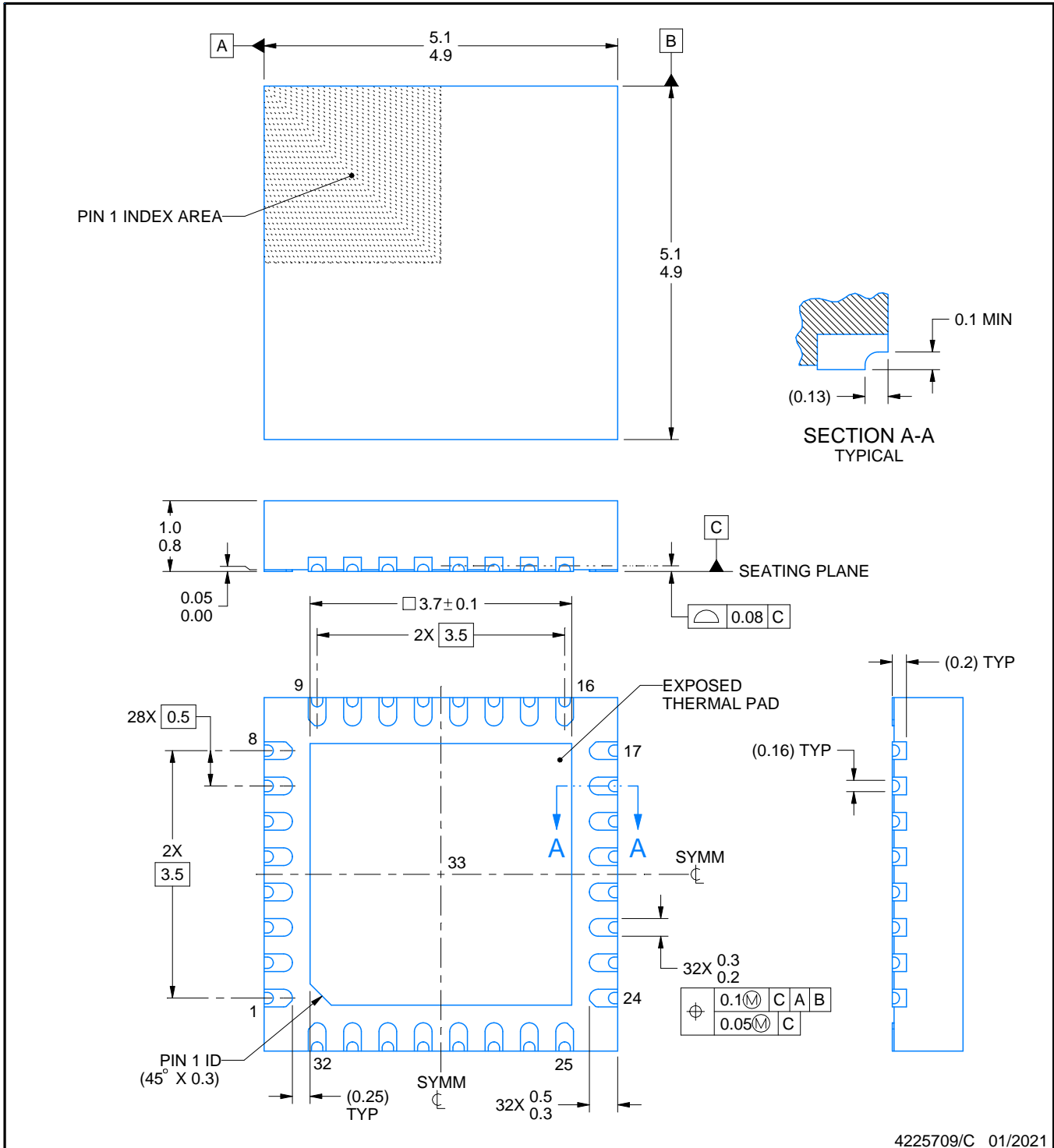
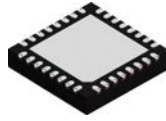
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A



4225709/C 01/2021

NOTES:

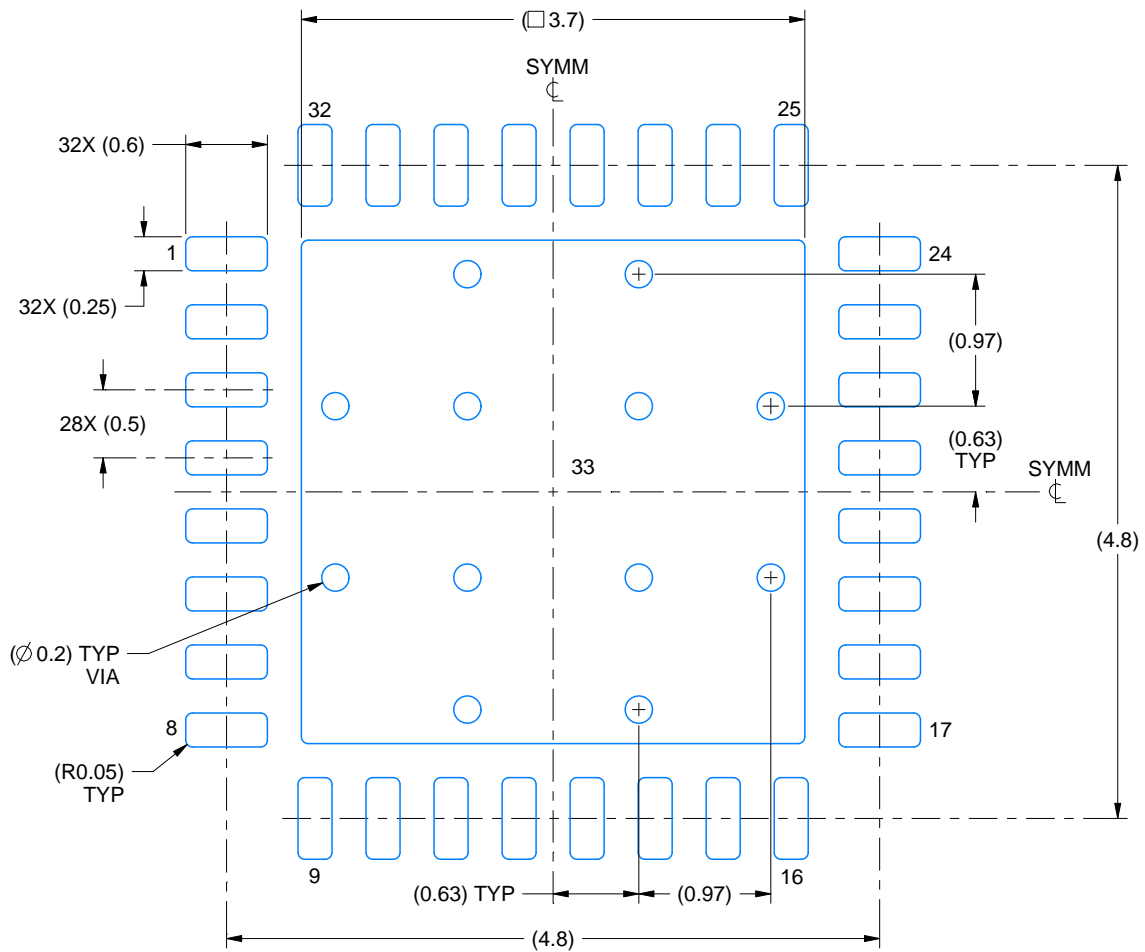
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

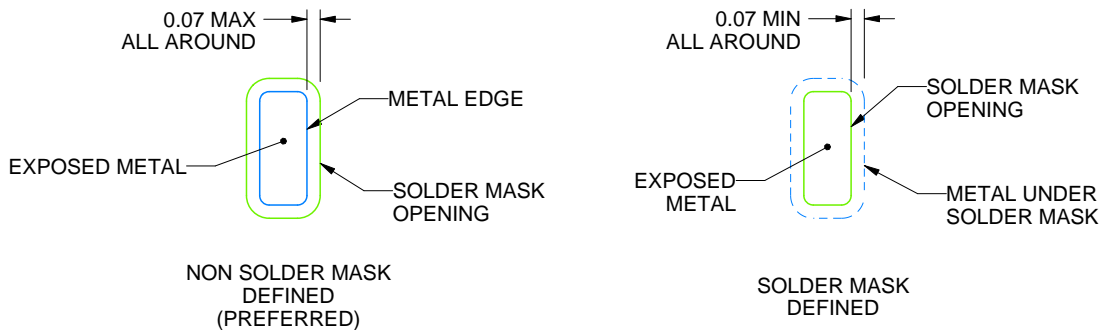
RHB0032U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4225709/C 01/2021

NOTES: (continued)

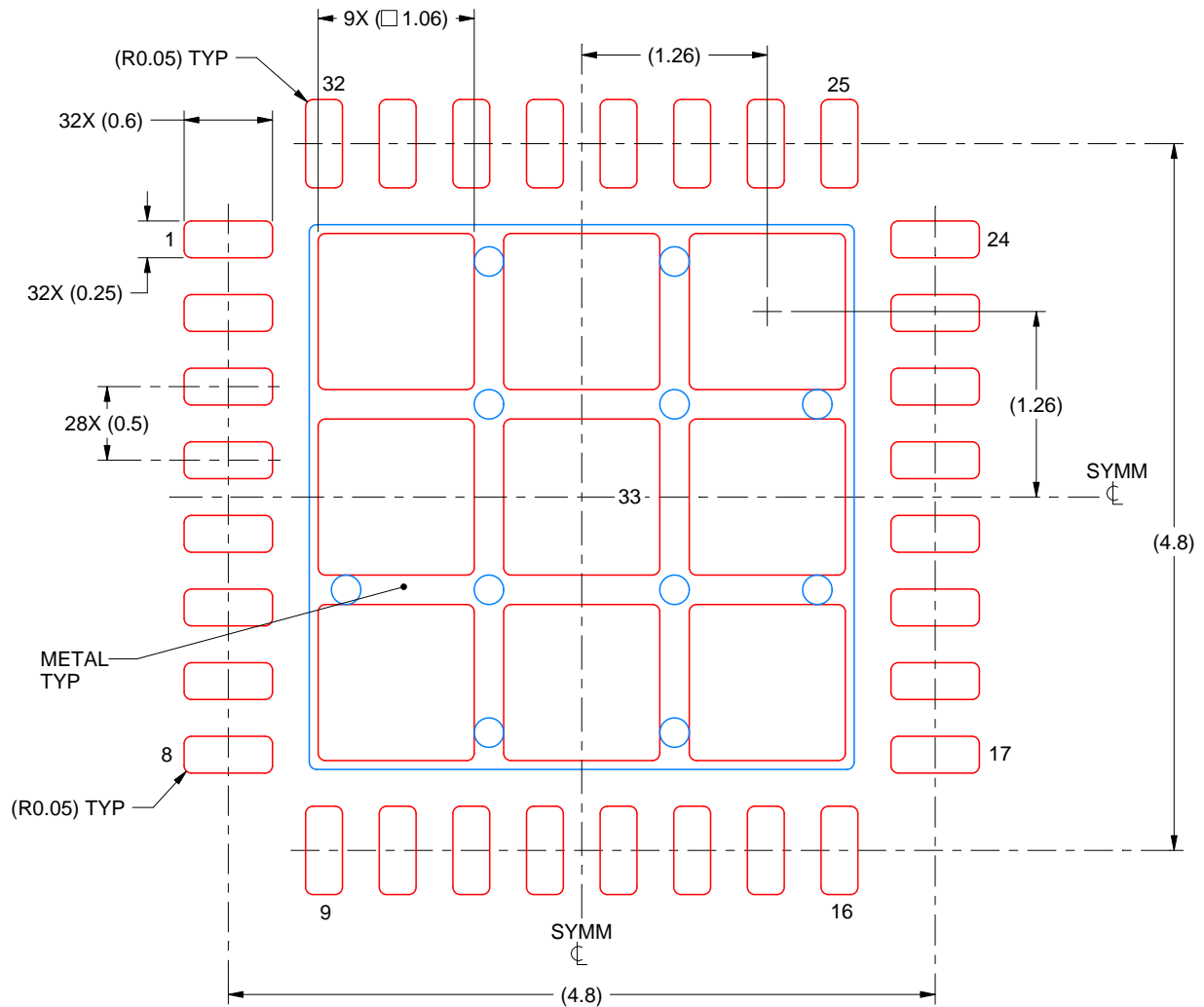
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225709/C 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PM0064A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

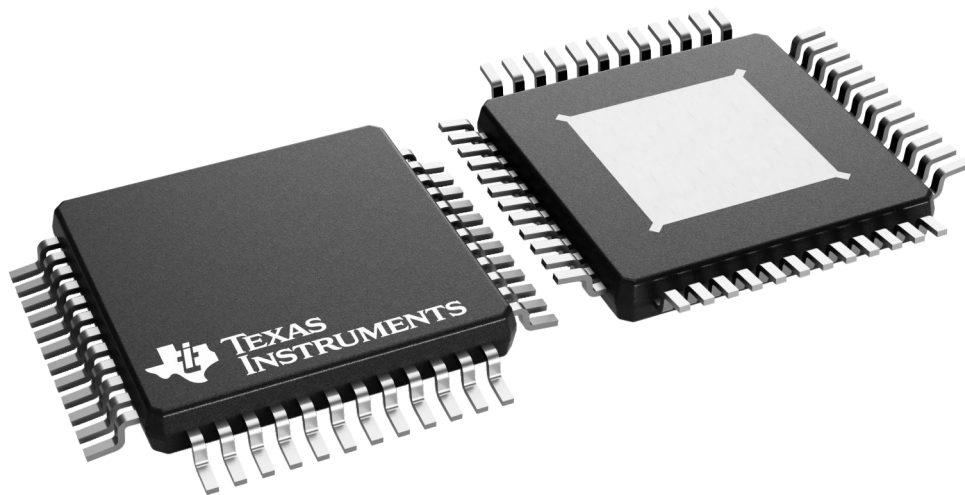
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

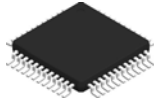
QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



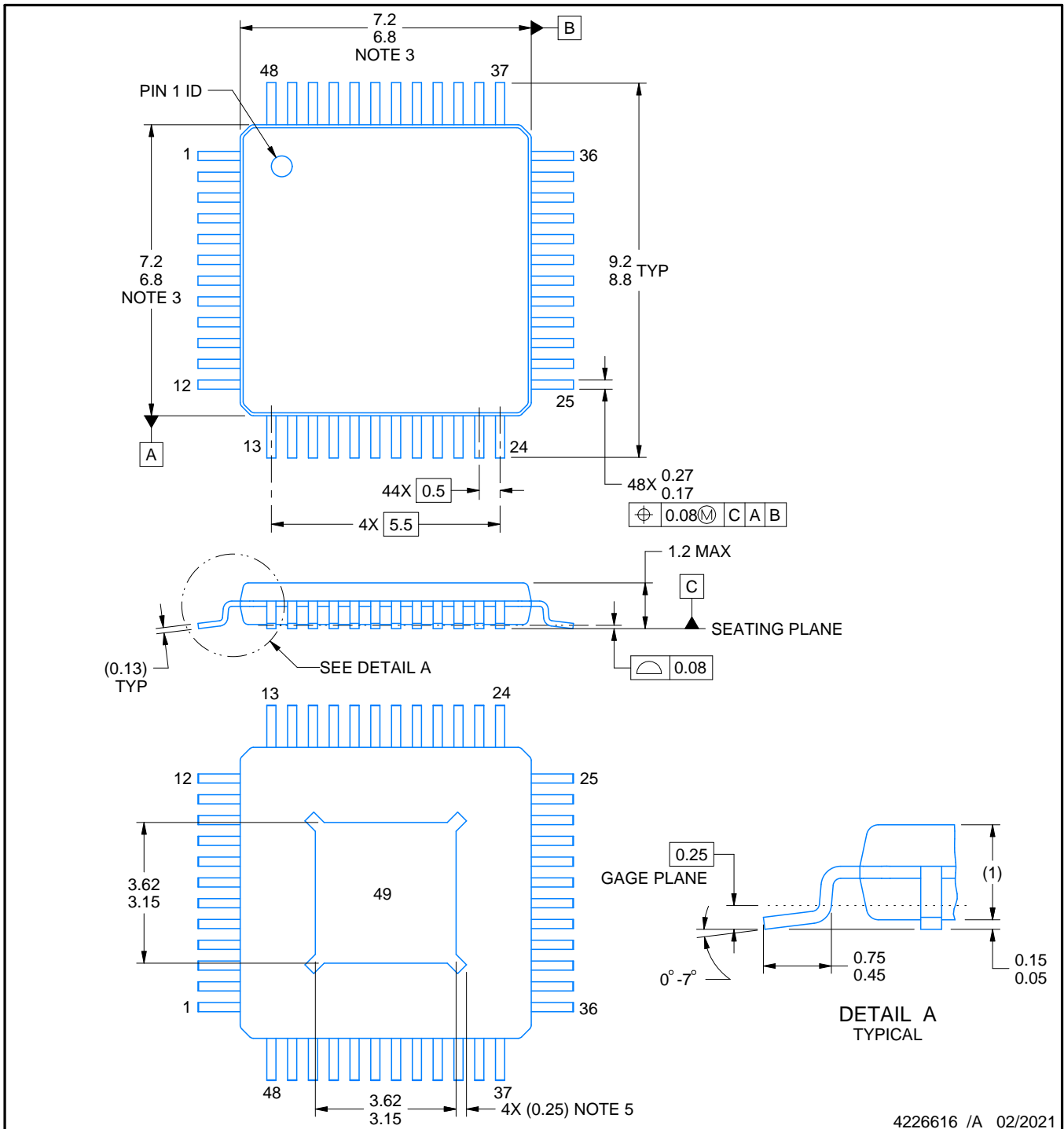
4226443/A

PHP0048E



PACKAGE OUTLINE

PowerPAD™ HTQFP - 1.2 mm max height



4226616 /A 02/2021

PowerPAD is a trademark of Texas Instruments.

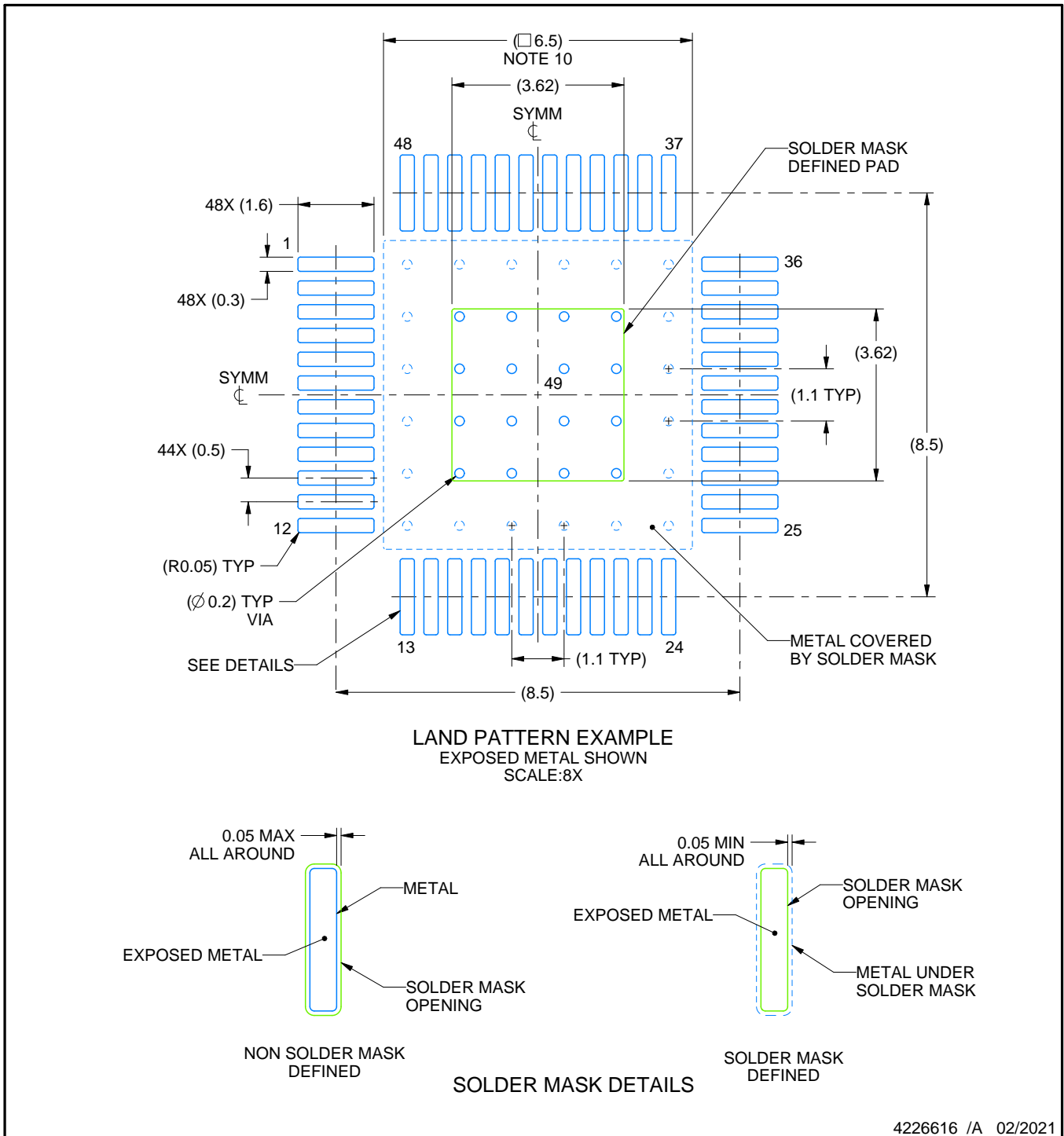
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.

EXAMPLE BOARD LAYOUT

PHP0048E

PowerPAD™ HTQFP - 1.2 mm max height



4226616 /A 02/2021

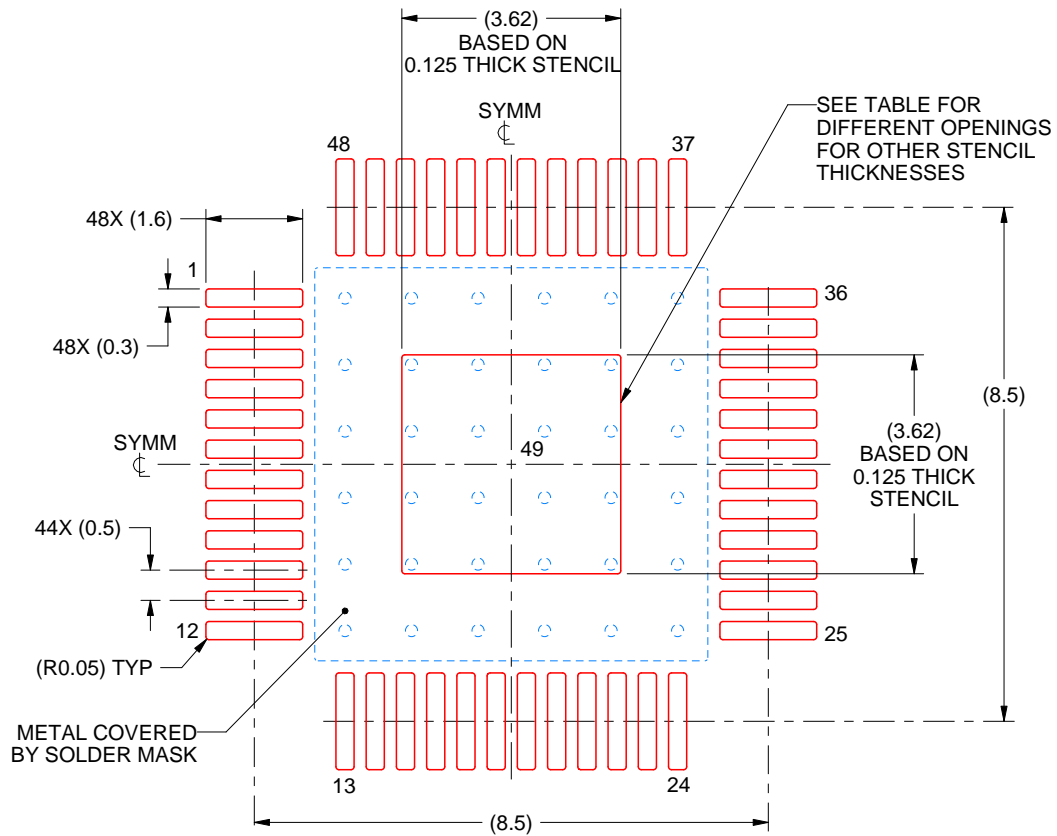
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

PHP0048E

PowerPAD™ HTQFP - 1.2 mm max height



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1 | 4.05 X 4.05 |
| 0.125 | 3.62 x 3.62 (SHOWN) |
| 0.150 | 3.30 x 3.30 |
| 0.175 | 3.06 x 3.06 |

4226616 /A 02/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PN0080A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



4215166/A 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

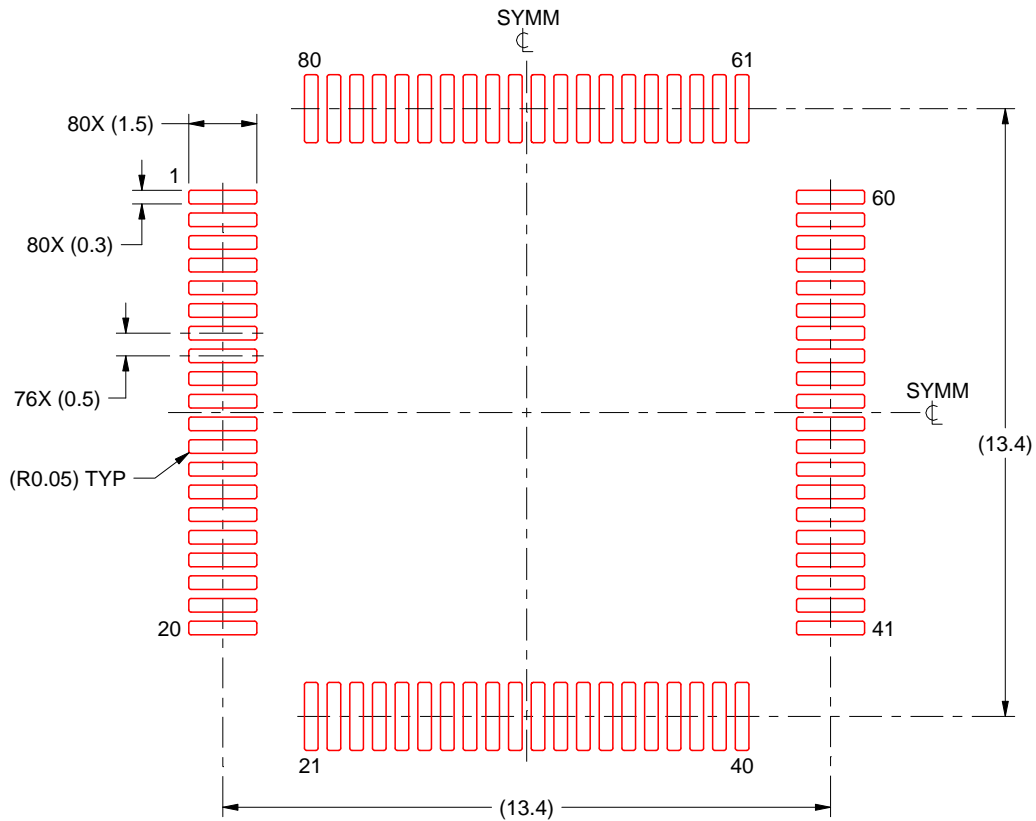
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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