

# INA155

For most current data sheet and other product information, visit [www.burr-brown.com](http://www.burr-brown.com)

## Single-Supply, Rail-to-Rail Output, CMOS INSTRUMENTATION AMPLIFIER

### FEATURES

- RAIL-TO-RAIL OUTPUT SWING: Within 10mV
- LOW OFFSET VOLTAGE:  $\pm 200\mu\text{V}$
- LOW OFFSET DRIFT:  $\pm 5\mu\text{V}/^\circ\text{C}$
- INTERNAL FIXED GAIN = 10V/V OR 50V/V
- SPECIFIED TEMPERATURE RANGE:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- LOW INPUT BIAS CURRENT: 0.2pA
- WIDE BANDWIDTH: 550kHz in  $G = 10$
- HIGH SLEW RATE:  $6.5\text{V}/\mu\text{s}$
- LOW COST
- SO-8 AND TINY MSOP-8 PACKAGES

### APPLICATIONS

- INDUSTRIAL SENSOR AMPLIFIERS  
Bridge, RTD, Thermocouple, Flow, Position
- MEDICAL EQUIPMENT  
ECG, EEG, EMG Amplifiers
- DRIVING A/D CONVERTERS
- PCMCIA CARDS
- AUDIO PROCESSING
- COMMUNICATIONS
- TEST EQUIPMENT
- LOW COST AUTOMOTIVE INSTRUMENTATION

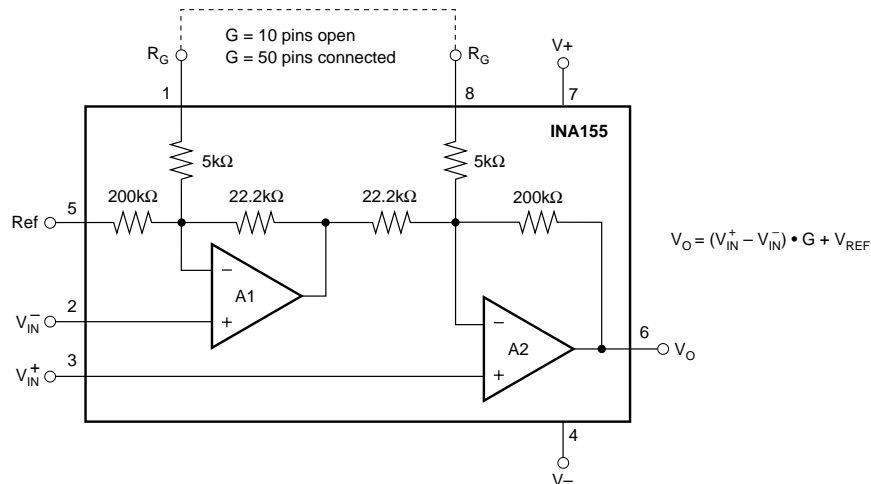
### DESCRIPTION

The INA155 is a low-cost CMOS instrumentation amplifier with rail-to-rail output swing optimized for low voltage, single-supply operation.

Wide bandwidth (550kHz in  $G = 10$ ) and high slew rate ( $6.5\text{V}/\mu\text{s}$ ) make the INA155 suitable for driving sampling A/D converters as well as general purpose and audio applications. Fast settling time allows use with higher speed sensors and transducers and rapid scanning data acquisition systems.

Gain can be set to 10V/V or 50V/V by pin strapping. Gains between these two values can be obtained with the addition of a single resistor. The INA155 is fully specified over the supply range of +2.7 to +5.5V.

The INA155 is available in MSOP-8 and SO-8 surface-mount packages. Both are specified for operation over the temperature range  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111  
Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS: $V_S = +2.7V$ to $+5.5V$

**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

At  $T_A = +25^{\circ}C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$ .  $R_G$  pins open ( $G = 10$ ), and  $Ref = V_S/2$ , unless otherwise noted.

PARAMETER	CONDITION	INA155E, U			INA155EA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT</b>								
Offset Voltage, RTI	$V_{OS}$		$\pm 0.2$	$\pm 1$		*	*	mV
<b>Over Temperature</b>				<b><math>\pm 1.5</math></b>		*	*	mV
Drift	$dV_{OS}/dT$		<b><math>\pm 5</math></b>			*	*	$\mu V/^{\circ}C$
vs Power Supply	PSRR		$\pm 50$	$\pm 200$		*	*	$\mu V/V$
<b>Over Temperature</b>				<b><math>\pm 250</math></b>		*	*	$\mu V/V$
vs Time			$\pm 0.4$			*	*	$\mu V/mo$
<b>INPUT VOLTAGE RANGE</b>								
Safe Input Voltage			$(V-) - 0.5$	$(V+) + 0.5$	*		*	V
Common-Mode Range <sup>(1)</sup>	$V_{CM}$		0.3	5.2 <sup>(2)</sup>	*		*	V
			0.2	2.5 <sup>(2)</sup>	*		*	V
Common-Mode Rejection Ratio	CMRR	$V_S = 5.5V, 0.6V < V_{CM} < 3.7V, G = 10$	92	100	80	*		dB
<b>Over Temperature</b>			<b>85</b>		<b>79</b>	*		dB
		$V_S = 5.5V, 0.6V < V_{CM} < 3.7V, G = 50$	86	90	77	*		dB
<b>Over Temperature</b>			<b>85</b>		<b>76</b>	*		dB
<b>INPUT IMPEDANCE</b>								
Differential			$10^{13} \parallel 3$			*		$\Omega \parallel pF$
Common-Mode			$10^{13} \parallel 3$			*		$\Omega \parallel pF$
<b>INPUT BIAS CURRENT</b>								
Input Bias Current	$I_B$		$\pm 1$	$\pm 10$		*	*	pA
Offset Current	$I_{OS}$		$\pm 1$	$\pm 10$		*	*	pA
<b>NOISE, RTI</b>		$R_S = 0\Omega, G = 10$ or $50$						
Voltage Noise: $f = 0.1Hz$ to $10Hz$			4.5			*	*	$\mu V/Vp-p$
Voltage Noise Density: $f = 10Hz$			260			*	*	$nV/\sqrt{Hz}$
$f = 100Hz$			99			*	*	$nV/\sqrt{Hz}$
$f = 1kHz$			40			*	*	$nV/\sqrt{Hz}$
Current Noise: $f = 1kHz$			2			*	*	$fA/\sqrt{Hz}$
<b>GAIN</b>			10	50	*		*	V/V
Gain Equation			$G = 10 + 400k\Omega/(10k\Omega + R_G)$			*	*	V/V
Gain Error <sup>(3)</sup>		$V_S = 5.5V, V_O = 0.01V$ to $5.49V, G = 10$	$\pm 0.02$	$\pm 0.1$		*	*	%
<b>vs Temperature</b>			<b><math>\pm 2</math></b>	<b><math>\pm 10</math></b>		*	*	ppm/ $^{\circ}C$
		$V_S = 5.5V, V_O = 0.05V$ to $5.45V, G = 50$	$\pm 0.05$	$\pm 0.25$		*	*	%
<b>vs Temperature</b>			<b><math>\pm 15</math></b>	<b><math>\pm 30</math></b>		*	*	ppm/ $^{\circ}C$
Nonlinearity		$V_S = 5.5V, G = 10$ or $50$	$\pm 0.005$	$\pm 0.015$		*	*	% of FSR
<b>Over Temperature</b>				<b><math>\pm 0.015</math></b>		*	*	% of FSR
<b>OUTPUT</b>								
Voltage Output Swing from Rail		$R_L = 10k\Omega, G_{ERR} < 0.1\%$	5	10		*	*	mV
<b>Over Temperature</b>				<b>10</b>		*	*	mV
Short-Circuit Current		Short Circuit to Ground	$\pm 50$			*	*	mA
Capacitance Load (stable operation)			See Typical Curve			*	*	
<b>FREQUENCY RESPONSE</b>								
Bandwidth, $-3dB$	BW	$G = 10$	550			*	*	kHz
		$G = 50$	110			*	*	kHz
Slew Rate	SR	$V_S = 5.5V, C_L = 100pF$	6.5			*	*	V/ $\mu s$
Settling Time: 0.1%	$t_S$	$V_S = 5.5V, V_O = 2V$ Step, $C_L = 100pF, G = 10$	5			*	*	$\mu s$
		$V_S = 5.5V, V_O = 2V$ Step, $C_L = 100pF, G = 50$	11			*	*	$\mu s$
0.01%		$V_S = 5.5V, V_O = 2V$ Step, $C_L = 100pF, G = 10$	8			*	*	$\mu s$
		$V_S = 5.5V, V_O = 2V$ Step, $C_L = 100pF, G = 50$	15			*	*	$\mu s$
Overload Recovery		50% Input Overload	0.2			*	*	$\mu s$
Total Harmonic Distortion + Noise	THD+N		See Typical Curve			*	*	
<b>POWER SUPPLY</b>								
Specified Voltage Range			+2.7	+5.5	*		*	V
Operating Voltage Range			+2.5 to +6			*	*	V
Quiescent Current		$V_{IN} = 0, I_O = 0$	1.7	2.1		*	*	mA
<b>Over Temperature</b>		<b><math>V_{IN} = 0, I_O = 0</math></b>		<b>2.6</b>		*	*	mA
<b>TEMPERATURE RANGE</b>								
Specified Range			-40	+85	*		*	$^{\circ}C$
Operating Range			-65	+150	*		*	$^{\circ}C$
Storage Range			-65	+150	*		*	$^{\circ}C$
Thermal Resistance	$\theta_{JA}$							
MSOP-8 Surface Mount			150			*	*	$^{\circ}C/W$
SO-8 Surface Mount			150			*	*	$^{\circ}C/W$

\* Same as INA155E, U.

NOTES: (1) For further information, refer to typical performance curves on common-mode input range. (2) Operation above  $(V+) - 1.8V$  (max) results in reduced common-mode rejection. See discussion and Figure 6 in the text of this data sheet. (3) Does not include error and TCR of additional optional gain-setting resistor in series with  $R_G$ , if used.

# SPECIFICATIONS: $V_S = +2.7V$ to $+5.5V$

**Boldface** limits apply over the specified temperature range,  $T_A = -55^{\circ}C$  to  $+125^{\circ}C$

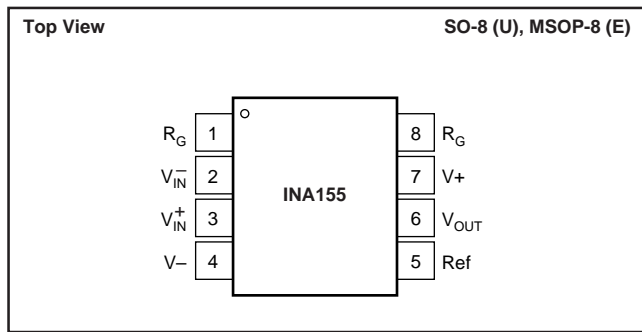
At  $T_A = +25^{\circ}C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$ .  $R_G$  pins open ( $G = 10$ ), and  $Ref = V_S/2$ , unless otherwise noted.

PARAMETER	CONDITION	INA155E, U			INA155EA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT</b>								
Offset Voltage, RTI	$V_{OS}$		$\pm 0.2$	$\pm 1$		*	*	mV
<b>Over Temperature</b>				$\pm 2$		*	*	mV
Drift	$dV_{OS}/dT$		$\pm 5$			*	*	$\mu V/^{\circ}C$
vs Power Supply	PSRR		$\pm 50$	$\pm 200$		*	*	$\mu V/V$
<b>Over Temperature</b>				$\pm 250$		*	*	$\mu V/V$
vs Time			$\pm 0.4$			*	*	$\mu V/mo$
<b>INPUT VOLTAGE RANGE</b>								
Safe Input Voltage		$(V-) - 0.5$		$(V+) + 0.5$	*		*	V
Common-Mode Range <sup>(1)</sup>	$V_{CM}$	0.3		5.2 <sup>(2)</sup>	*		*	V
		0.2		2.5 <sup>(2)</sup>	*		*	V
Common-Mode Rejection Ratio	CMRR	$V_S = 5.5V, 0.6V < V_{CM} < 3.7V, G = 10$	92	100	80	*		dB
<b>Over Temperature</b>			<b>82</b>		<b>78</b>	*		dB
		$V_S = 5.5V, 0.6V < V_{CM} < 3.7V, G = 50$	86	90	77	*		dB
<b>Over Temperature</b>			<b>84</b>		<b>76</b>	*		dB
<b>INPUT IMPEDANCE</b>								
Differential			$10^{13} \parallel 3$			*		$\Omega \parallel pF$
Common-Mode			$10^{13} \parallel 3$			*		$\Omega \parallel pF$
<b>INPUT BIAS CURRENT</b>								
Input Bias Current	$I_B$		$\pm 1$	$\pm 10$		*	*	pA
Offset Current	$I_{OS}$		$\pm 1$	$\pm 10$		*	*	pA
<b>NOISE, RTI</b>		$R_S = 0\Omega, G = 10$ or $50$						
Voltage Noise: $f = 0.1Hz$ to $10Hz$			4.5			*	*	$\mu V/Vp-p$
Voltage Noise Density: $f = 10Hz$			260			*	*	$nV/\sqrt{Hz}$
$f = 100Hz$			99			*	*	$nV/\sqrt{Hz}$
$f = 1kHz$			40			*	*	$nV/\sqrt{Hz}$
Current Noise: $f = 1kHz$			2			*	*	$fA/\sqrt{Hz}$
<b>GAIN</b>			10	50	*		*	V/V
Gain Equation			$G = 10 + 400k\Omega/(10k\Omega + R_G)$			*	*	V/V
Gain Error <sup>(3)</sup>		$V_S = 5.5V, V_O = 0.01V$ to $5.49V, G = 10$	$\pm 0.02$	$\pm 0.1$		*	*	%
<b>vs Temperature</b>			<b><math>\pm 2</math></b>	<b><math>\pm 10</math></b>		*	*	ppm/ $^{\circ}C$
		$V_S = 5.5V, V_O = 0.05V$ to $5.45V, G = 50$	$\pm 0.05$	$\pm 0.25$		*	*	%
<b>vs Temperature</b>			<b><math>\pm 15</math></b>	<b><math>\pm 30</math></b>		*	*	ppm/ $^{\circ}C$
Nonlinearity		$V_S = 5.5V, G = 10$ or $50$	$\pm 0.005$	$\pm 0.015$		*	*	% of FSR
<b>Over Temperature</b>				<b><math>\pm 0.015</math></b>		*	*	% of FSR
<b>OUTPUT</b>								
Voltage Output Swing from Rail		$R_L = 10k\Omega, G_{ERR} < 0.1\%$	5	10		*	*	mV
<b>Over Temperature</b>				<b>10</b>		*	*	mV
Short-Circuit Current		Short Circuit to Ground	$\pm 50$			*	*	mA
Capacitance Load (stable operation)			See Typical Curve			*	*	
<b>FREQUENCY RESPONSE</b>								
Bandwidth, $-3dB$	BW	$G = 10$	550			*	*	kHz
		$G = 50$	110			*	*	kHz
Slew Rate	SR	$V_S = 5.5V, C_L = 100pF$	6.5			*	*	V/ $\mu s$
Settling Time: 0.1%	$t_S$	$V_S = 5.5V, V_O = 2V$ Step, $C_L = 100pF, G = 10$	5			*	*	$\mu s$
		$V_S = 5.5V, V_O = 2V$ Step, $C_L = 100pF, G = 50$	11			*	*	$\mu s$
		$V_S = 5.5V, V_O = 2V$ Step, $C_L = 100pF, G = 10$	8			*	*	$\mu s$
		$V_S = 5.5V, V_O = 2V$ Step, $C_L = 100pF, G = 50$	15			*	*	$\mu s$
Overload Recovery		50% Input Overload	0.2			*	*	$\mu s$
Total Harmonic Distortion + Noise	THD+N		See Typical Curve			*	*	
<b>POWER SUPPLY</b>								
Specified Voltage Range			+2.7	+5.5	*		*	V
Operating Voltage Range			+2.5 to +6			*	*	V
Quiescent Current		$V_{IN} = 0, I_O = 0$	1.7	2.1		*	*	mA
<b>Over Temperature</b>		<b><math>V_{IN} = 0, I_O = 0</math></b>		<b>2.8</b>		*	*	mA
<b>TEMPERATURE RANGE</b>								
Specified Range			-55	+125	*		*	$^{\circ}C$
Operating Range			-65	+150	*		*	$^{\circ}C$
Storage Range			-65	+150	*		*	$^{\circ}C$
Thermal Resistance	$\theta_{JA}$							
MSOP-8 Surface Mount			150			*	*	$^{\circ}C/W$
SO-8 Surface Mount			150			*	*	$^{\circ}C/W$

\* Same as INA155E, U.

NOTES: (1) For further information, refer to typical performance curves on common-mode input range. (2) Operation above  $(V+) - 1.8V$  (max) results in reduced common-mode rejection. See discussion and Figure 6 in the text of this data sheet. (3) Does not include error and TCR of additional optional gain-setting resistor in series with  $R_G$ , if used.

## PIN CONFIGURATION



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage, V+ to V- .....	7.5V
Signal Input Terminals, Voltage <sup>(2)</sup> .....	(V-) - 0.5V to (V+) + 0.5V
Current <sup>(2)</sup> .....	10mA
Output Short-Circuit <sup>(3)</sup> .....	Continuous
Operating Temperature .....	-65°C to +150°C
Storage Temperature .....	-65°C to +150°C
Junction Temperature .....	+150°C
Lead Temperature (soldering, 10s) .....	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short circuit to ground.

## PACKAGE/ORDERING INFORMATION

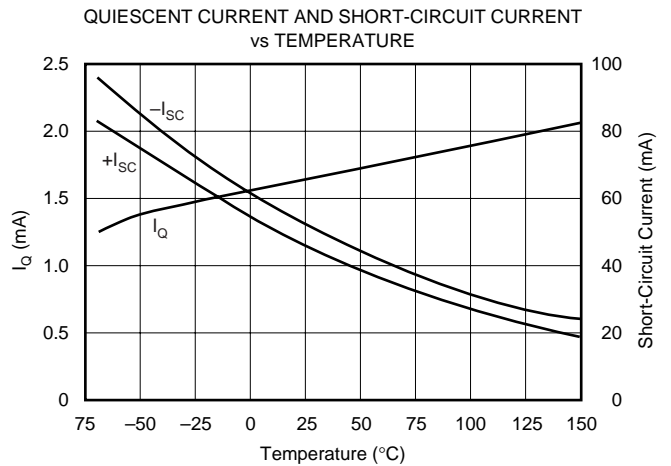
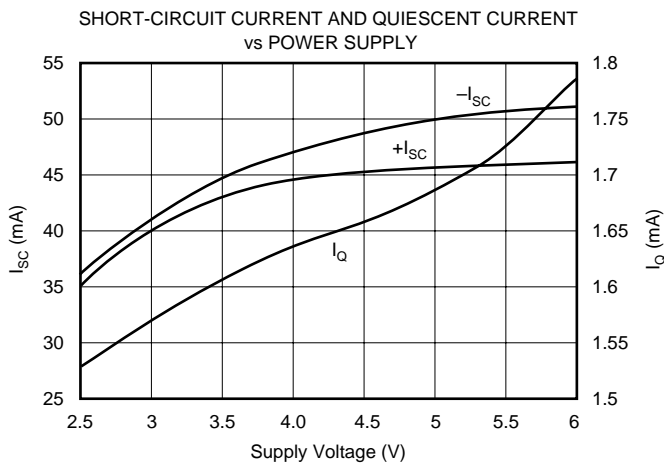
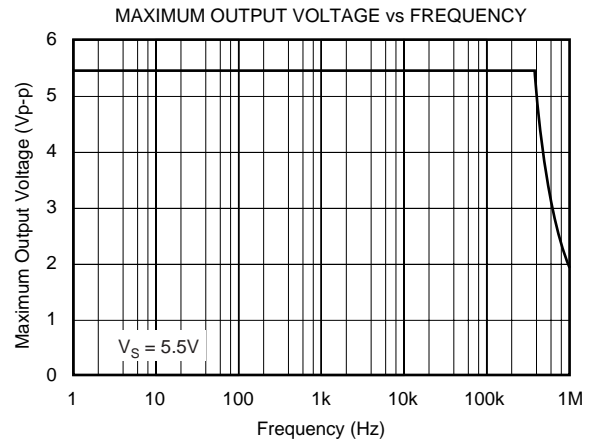
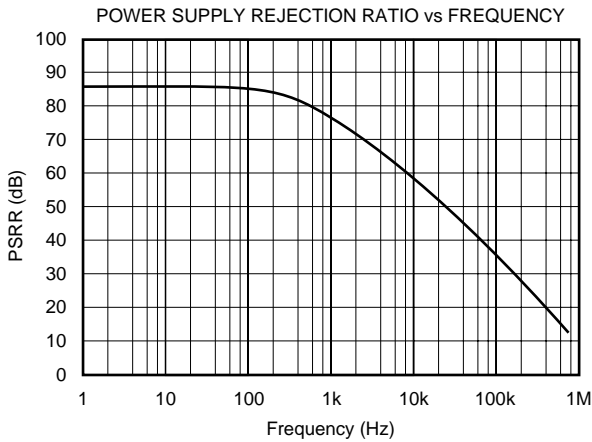
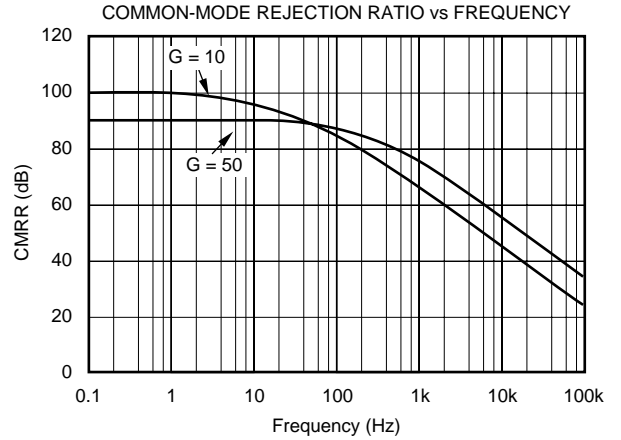
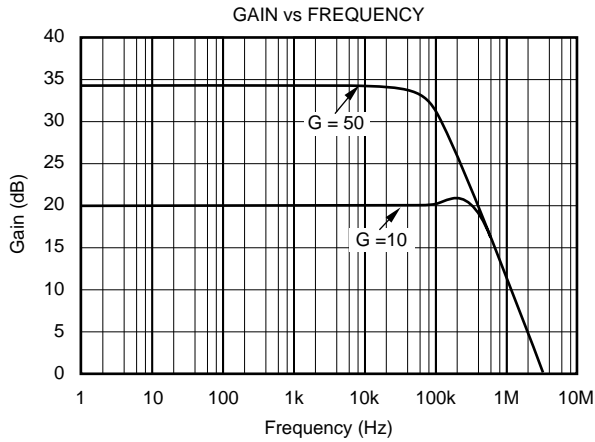
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER <sup>(1)</sup>	TRANSPORT MEDIA
INA155U	SO-8	182	-55°C to +125°C	INA155U	INA155U	Rails
"	"	"	"	"	INA155U/2K5	Tape and Reel
INA155UA	SO-8	182	-55°C to +125°C	INA155UA	INA155UA	Rails
"	"	"	"	"	INA155UA/2K5	Tape and Reel
INA155E	MSOP-8	337	-55°C to +125°C	A55	INA155E/250	Tape and Reel
"	"	"	"	"	INA155E/2K5	Tape and Reel
INA155EA	MSOP-8	337	-55°C to +125°C	A55	INA155EA/250	Tape and Reel
"	"	"	"	"	INA155EA/2K5	Tape and Reel

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "INA155UA/2K5" will get a single 2500-piece Tape and Reel.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

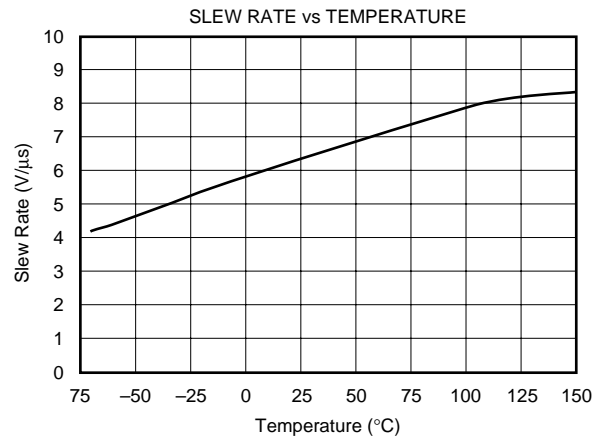
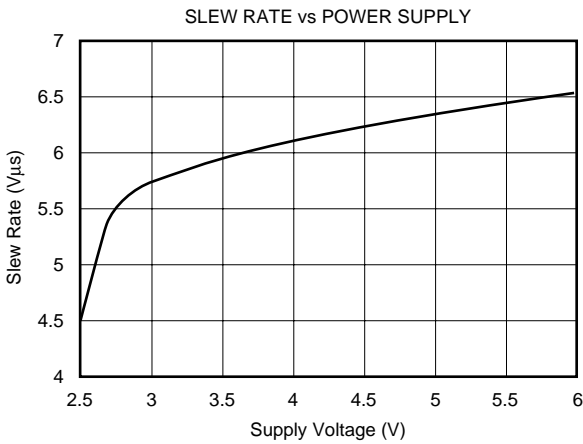
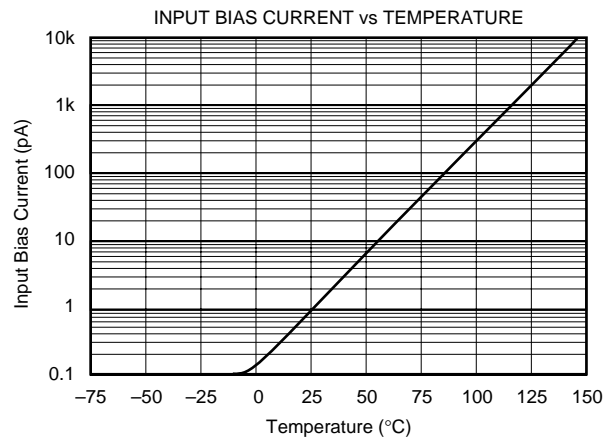
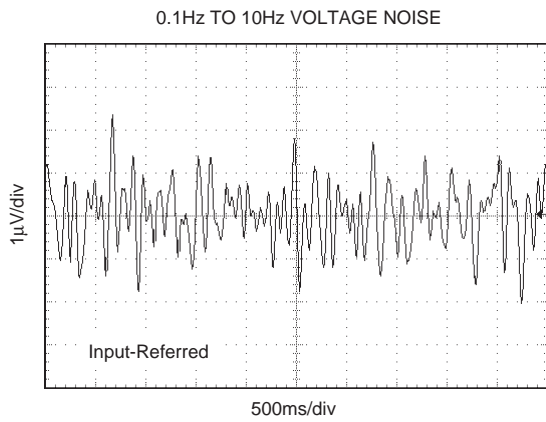
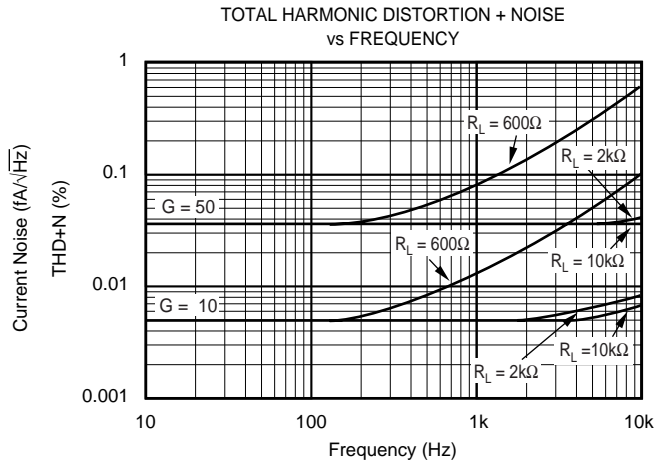
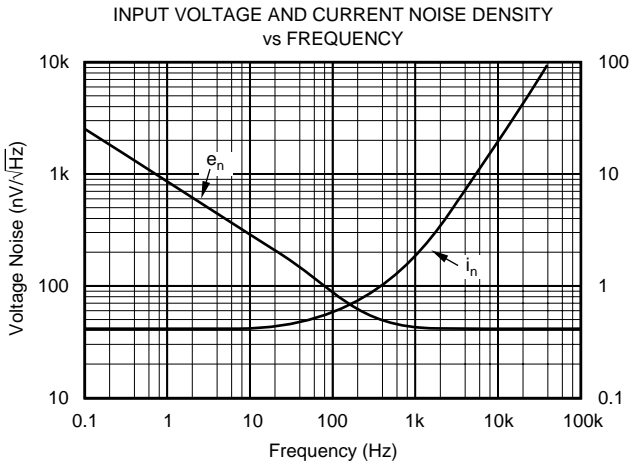
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5.5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ .  $R_G$  pins open ( $G = 10$ ), and  $\text{Ref} = V_S/2$ , unless otherwise noted.



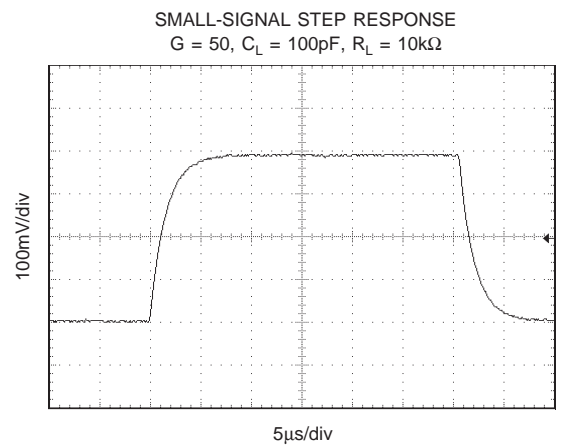
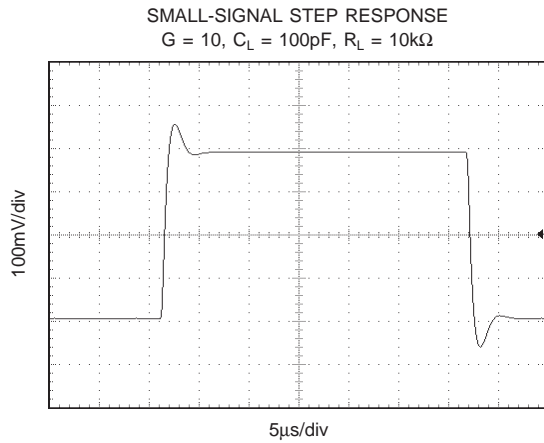
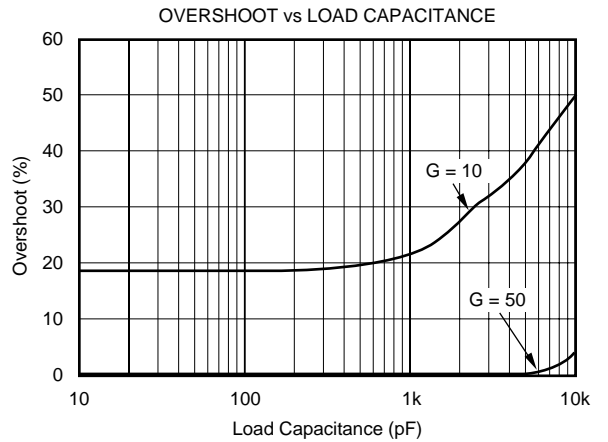
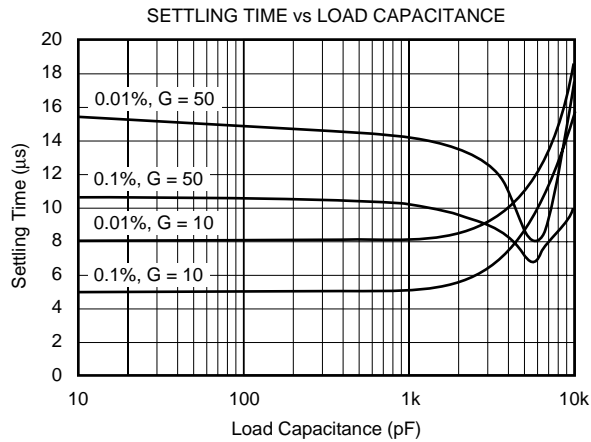
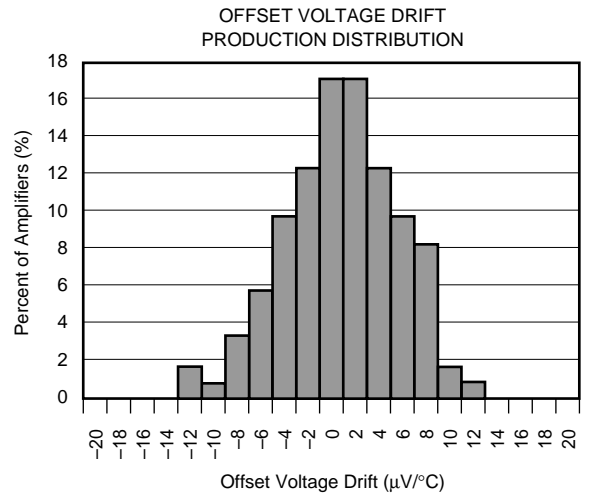
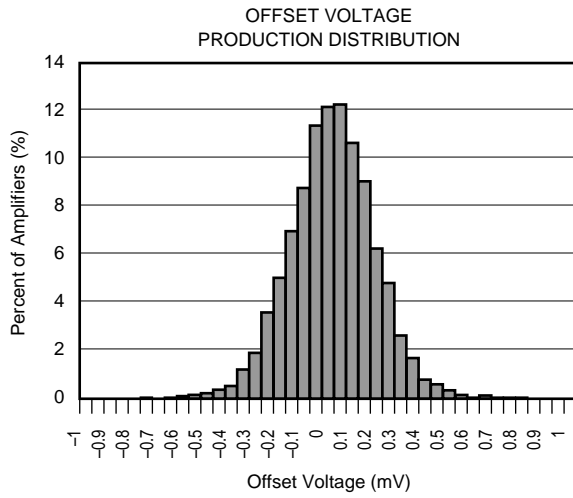
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5.5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ .  $R_G$  pins open ( $G = 10$ ), and  $\text{Ref} = V_S/2$ , unless otherwise noted.



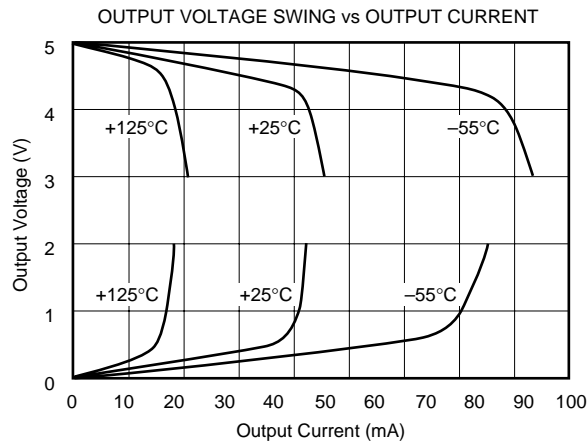
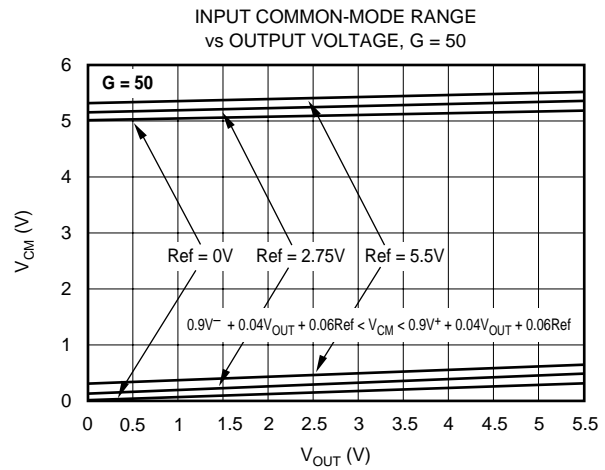
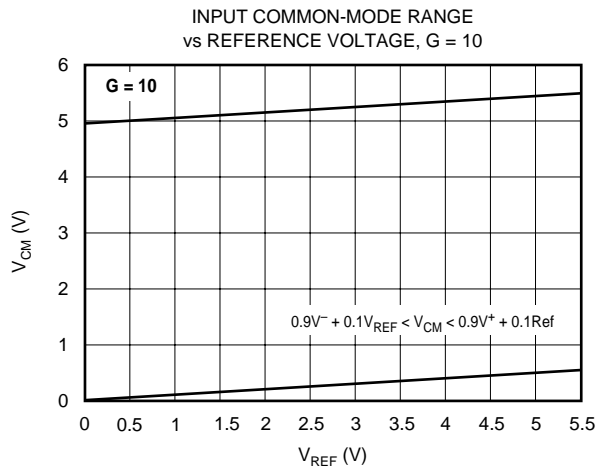
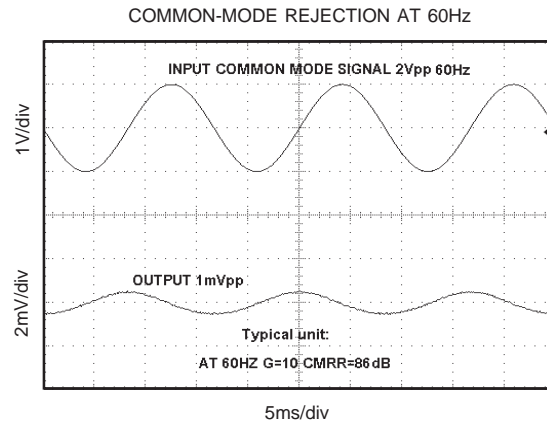
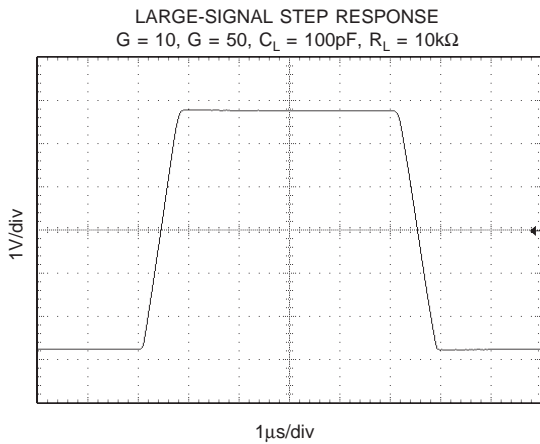
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5.5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ .  $R_G$  pins open ( $G = 10$ ), and  $\text{Ref} = V_S/2$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5.5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ .  $R_G$  pins open ( $G = 10$ ), and  $\text{Ref} = V_S/2$ , unless otherwise noted.





# APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA155. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference terminal, Ref, which is normally set to  $V_S/2$ . This must be a low-impedance connection to ensure good common-mode rejection. A resistance of  $200\Omega$  in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMRR.

In addition, for the  $G = 50$  configuration, the connection between pins 1 and 8 must be low-impedance. A connection impedance of  $20\Omega$  can cause a 0.2% shift in gain error.

# OPERATING VOLTAGE

The INA155 is fully specified and guaranteed over the supply range  $+2.7V$  to  $+5.5V$ , with key parameters guaranteed over the temperature range of  $-55^\circ C$  to  $+125^\circ C$ . Parameters that vary significantly with operating voltages, load conditions or temperature are shown in the Typical Performance Curves.

The INA155 can be operated from either single or dual power supplies. By adjusting the voltage applied to the reference terminal, the input common-mode voltage range and the output range can be adjusted within the bounds shown in the Typical Performance Curves. Figure 2 shows a bridge amplifier circuit operated from a single  $+5V$  power supply. The bridge provides a relatively small differential voltage on top of an input common-mode voltage near  $2.5V$ .

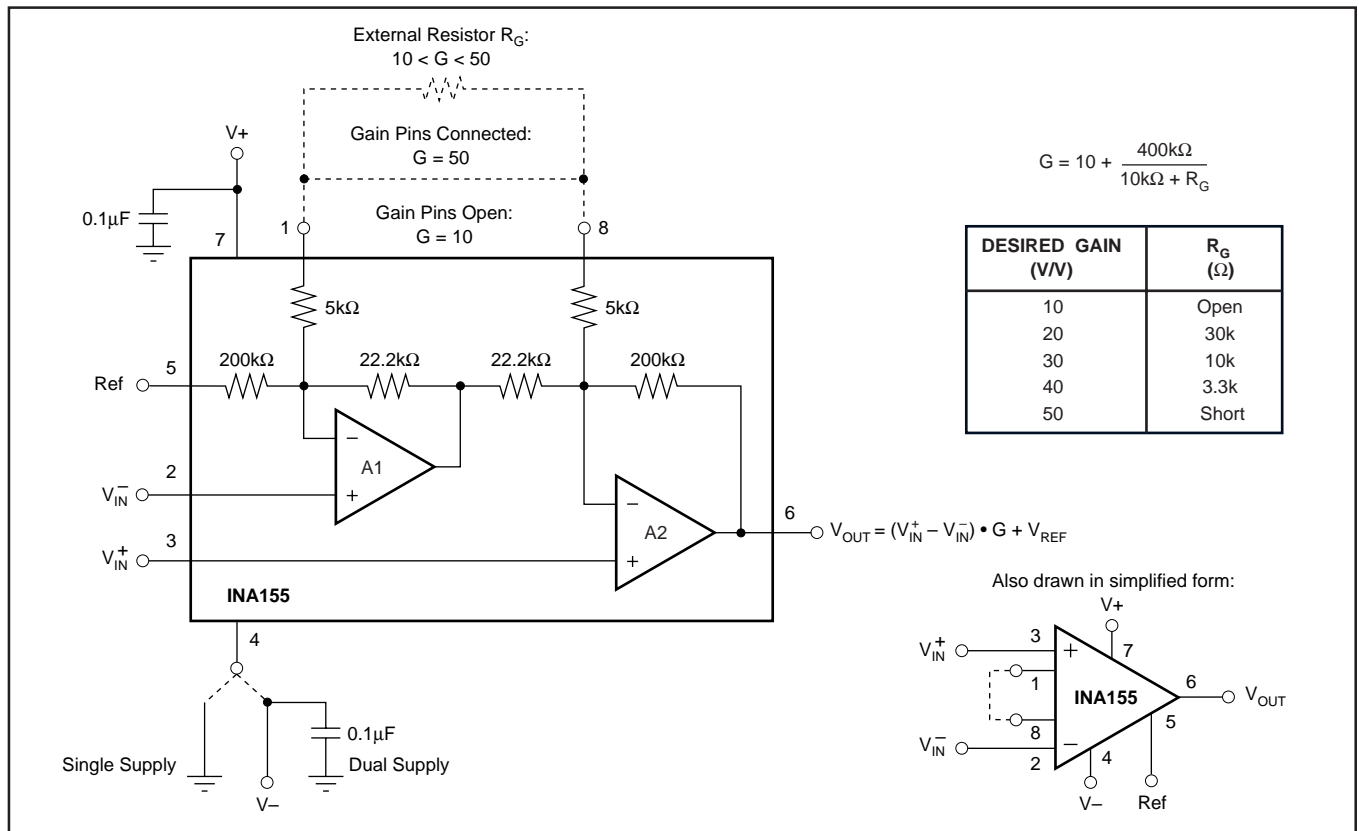


FIGURE 1. Basic Connections.

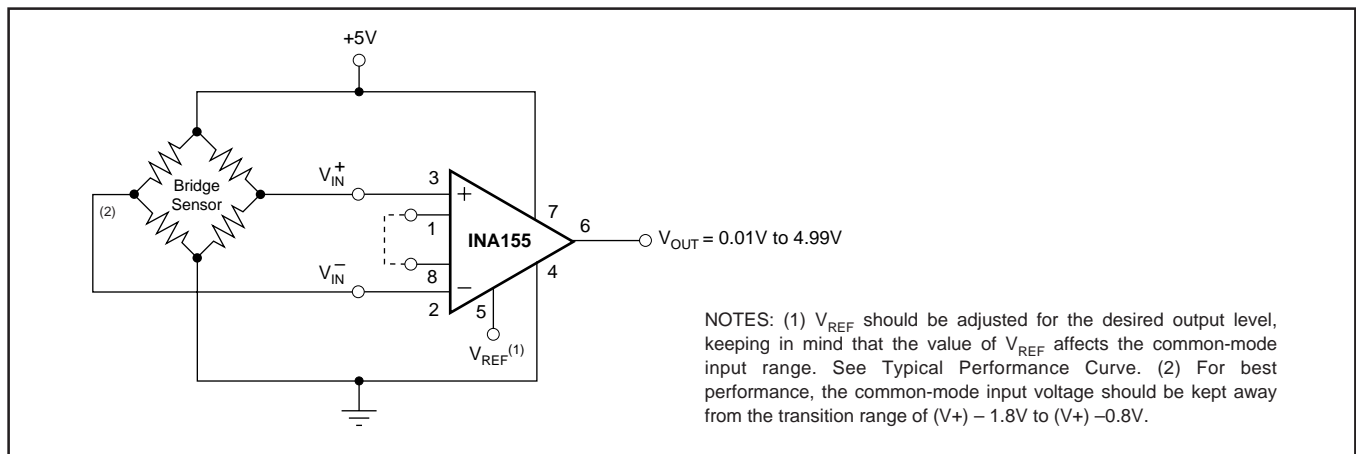


FIGURE 2. Single-Supply Bridge Amplifier.

## SETTING THE GAIN

Gain of 10 is achieved simply by leaving the two gain pins (1 and 8) open. Gain of 50 is achieved by connecting the gain pins together directly. In the  $G = 10$  configuration, the gain error is less than 0.1%. In the  $G = 50$  configuration, the gain error is less than 0.25%.

Gain can be set to any value between 10 and 50 by connecting a resistor  $R_G$  between the gain pins according to the following equation:

$$10 + 400k\Omega / (10k\Omega + R_G) \quad (1)$$

This is demonstrated in Figure 1 and is shown with the commonly used gains and resistor  $R_G$  values. However, because the absolute value of internal resistors is not guaranteed, using the INA155 in this configuration will increase the gain error and gain error drift with temperature, as shown in Figure 3.

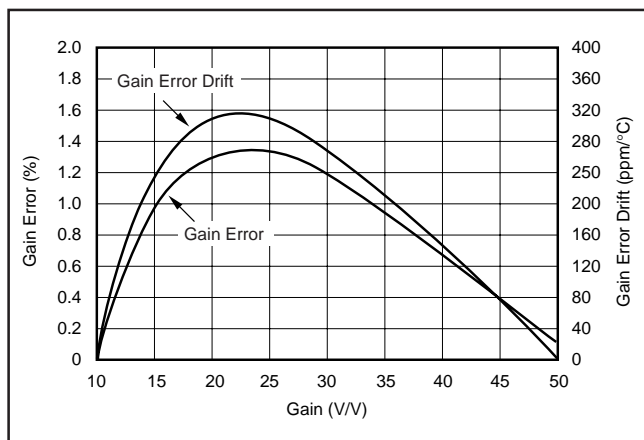


FIGURE 3. Typical Gain Error and Gain Error Drift with External Resistor.

## OFFSET TRIMMING

The INA155 is laser trimmed for low offset voltage. In most applications, no external offset adjustment is required. However, if necessary, the offset can be adjusted by applying a correction voltage to the reference terminal. Figure 4 shows

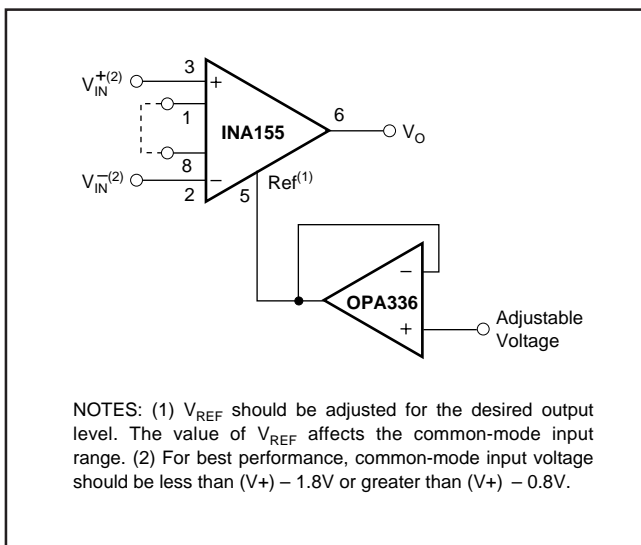


FIGURE 4. Optional Trimming of Output Offset Voltage.

an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is added to the output signal. An op amp buffer is used to provide low impedance at the Ref terminal to preserve good common-mode rejection.

## INPUT BIAS CURRENT RETURN

The input impedance of the INA155 is extremely high—approximately  $10^{13}\Omega$ , making it ideal for use with high-impedance sources. However, a path must be provided for the input bias current of both inputs. This input bias current is less than 10pA and is virtually independent of the input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 5 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential that exceeds the common-mode range and the input amplifier will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple in Figure 5). With higher source impedance, using two equal resistors provides a balanced input with advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

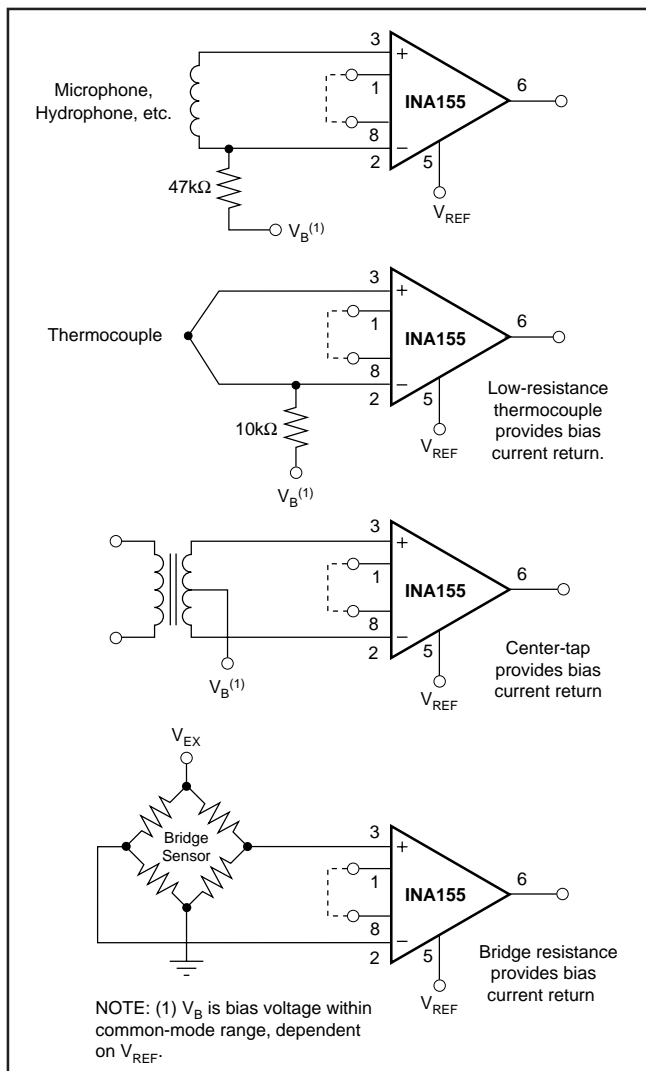


FIGURE 5. Providing an Input Common-Mode Current Path.

## INPUT COMMON-MODE RANGE

The input common-mode range of the INA155 for various operating conditions is shown in the Typical Performance Curves. The common-mode input range is limited by the output voltage swing of A1, an internal circuit node. For the  $G = 10$  configuration, output voltage of A1 can be expressed as:

$$V_{OUTA1} = -\frac{1}{9}V_{REF} + (1 + \frac{1}{9})V_{IN-} \quad (2)$$

Using this equation given that the output of A1 can swing to within 10mV of either rail, the input common-mode voltage range can be calculated. When the input common-mode range is exceeded (A1's output is saturated), A2 can still be in linear operation and respond to changes in the non-inverting input voltage. However, the output voltage will be invalid.

The common-mode range for the  $G = 50$  configuration is included in the Typical Performance Curve, "Input Common-Mode Range vs Output Voltage."

## INPUT RANGE FOR BEST ACCURACY

The internal amplifiers have rail-to-rail input stages, achieved by using complementary n- and p-channel input pairs. The common-mode input voltage determines whether the p-channel or the n-channel input stage is operating. The transition between the input stages is gradual and occurs between  $(V+) - 1.8V$  to  $(V+) - 0.8V$ . Due to these characteristics operating the INA155 with input voltages within the transition region of  $(V+) - 1.8V$  to  $(V+) - 0.8V$  results in a shift in input offset voltage and reduced common-mode and power supply rejection performance. Typical patterns of the offset voltage change throughout the input common-mode range are illustrated in Figure 6. The INA155 can be operated below or above the transition region with excellent results. Figure 7 demonstrates the use of the INA155 in a single-supply, high-side current monitor. In this application, the INA155 is operated above the transition region.

## RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For resistive loads greater than 10k $\Omega$ , the output voltage can swing to within a few millivolts of the supply rail while maintaining low gain error. For heavier loads and over temperature, see the typical performance curve "Output Voltage Swing vs Output Current." The INA155's low output impedance at high frequencies makes it suitable for directly driving Capacitive Digital-to-Analog (CDAC) input A/D converters, as shown in Figure 9.

## INPUT PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than 500mV. Momentary voltages greater than 500mV beyond the power supply can be tolerated if the current on the input pins is limited to 10mA. This is easily accomplished with input resistors  $R_{LIM}$  as shown in Figure 8. Many input signals are inherently current-limited to less than 10mA, therefore, a limiting resistor is not required.

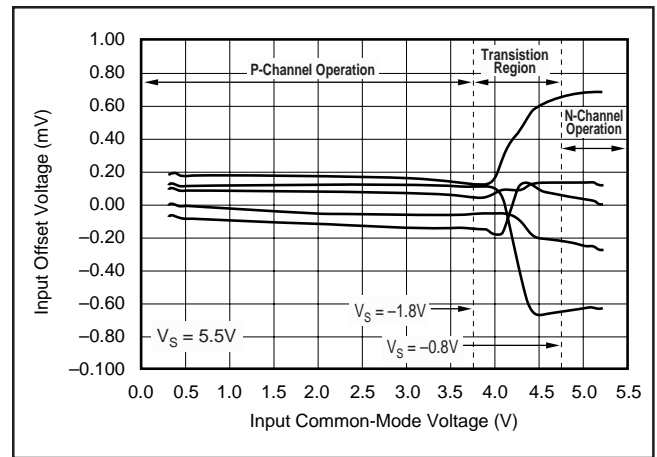


FIGURE 6. Input Offset Voltage Changes with Common-Mode Voltage.

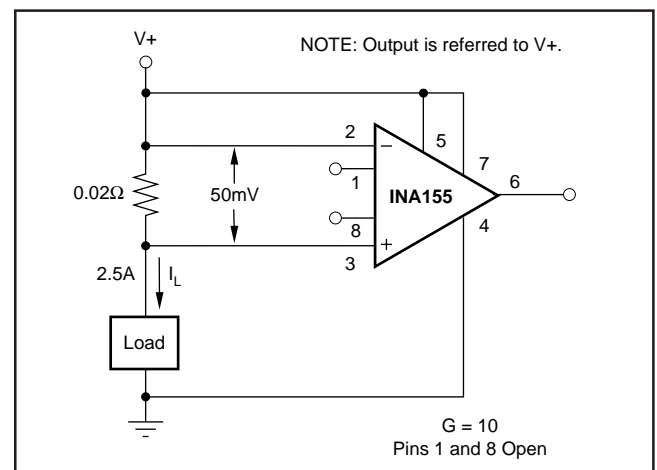


FIGURE 7. Single-Supply, High-Side Current Monitor.

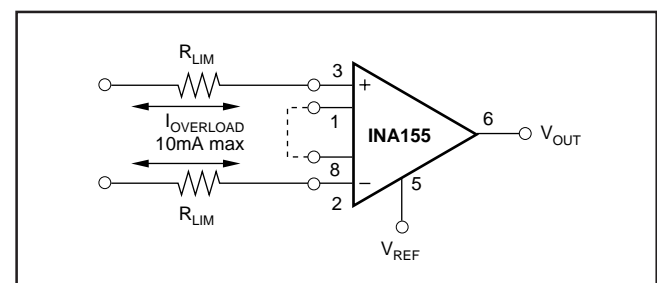


FIGURE 8. Input Current Protection for Voltages Exceeding the Supply Voltage.

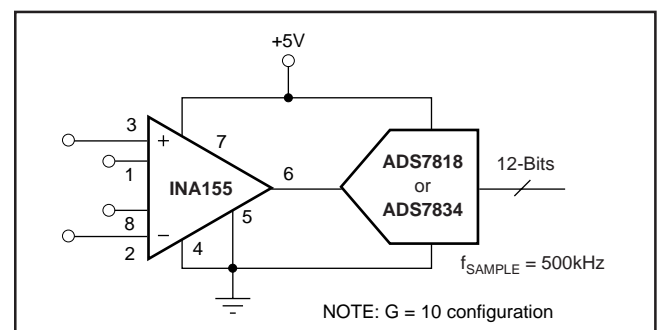


FIGURE 9. INA155 Directly Drives Capacitive-Input, High-Speed A/D Converter.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA155E/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	A55	<a href="#">Samples</a>
INA155EA/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR		A55	<a href="#">Samples</a>
INA155EA/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR		A55	<a href="#">Samples</a>
INA155U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-2-260C-1 YEAR		INA 155U	<a href="#">Samples</a>
INA155U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR		INA 155U	<a href="#">Samples</a>
INA155UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-2-260C-1 YEAR		INA 155U A	<a href="#">Samples</a>
INA155UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR		INA 155U A	<a href="#">Samples</a>
INA155UG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-2-260C-1 YEAR		INA 155U	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA155U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA155UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA155U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA155UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA155U	D	SOIC	8	75	506.6	8	3940	4.32
INA155UA	D	SOIC	8	75	506.6	8	3940	4.32
INA155UG4	D	SOIC	8	75	506.6	8	3940	4.32



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [Instrumentation Amplifiers](#) category:*

*Click to view products by [Texas Instruments](#) manufacturer:*

Other Similar products are found below :

[ISL28274FAZ](#) [INA350ABSIDSGR](#) [HT8620ARZ](#) [TPA1286-SO1R](#) [AD624AD/+](#) [RS633EHXM](#) [SGM620XS8G/TR](#) [INA848IDR](#)  
[INA351AIDSGR](#) [AD620RX](#) [ADA4530-1ARZ-RL](#) [AD8421ARMZ-RL](#) [TPA1286-VS1R](#) [MCP6N16-100EMF](#) [JM38510/13501BGA](#)  
[MCP6N16-001E/MF](#) [AD8422BRMZ-R7](#) [AD8426BCPZ-R7](#) [INA188IDRJR](#) [AD8220BRMZ-R7](#) [LTC1100CN8#PBF](#) [INA333AIDGKRG4](#)  
[INA826SIDRCT](#) [INA826SIDRCR](#) [AD8221ARMZ](#) [AD8226ARZ-RL](#) [AD694JN](#) [AD8420ARMZ-RL](#) [AD620ANZ](#) [AD621BR](#) [AD622ANZ](#)  
[AD623ANZ](#) [AD623BNZ](#) [AD625BDZ](#) [AD694JNZ](#) [AD620SQ/883B](#) [AD8220ARMZ-R7](#) [AD8220WARMZ](#) [AD8221ARMZ-R7](#)  
[AD8224ACPZ-R7](#) [AD8222ACPZ-R7](#) [AD8222ACPZ-RL](#) [AD8223ARMZ-R7](#) [AD8222HACPZ-R7](#) [AD8226ARMZ](#) [AD8228ARMZ-R7](#)  
[AD8236ARMZ-R7](#) [AD8237ARMZ](#) [AD8237ARMZ-R7](#) [AD8250ARMZ](#)