TEXAS INSTRUMENTS

**ISO7320C, ISO7320FC, ISO7321C, ISO7321FC**

ZHCSDI8C –JANUARY 2015–REVISED APRIL 2015

# ISO732x 耐用 EMC 低功耗双通道数字隔离器

## 1 特性

- 信号传输速率：25Mbps
- 输入时使用集成噪声滤波器
- 默认输出"高"和"低"选项
- 低功耗：每通道的 $I_{CC}$ 典型值（1Mbps时）：
  - ISO7320：1.2mA（5V 电源供电时），0.9mA（3.3V 电源供电时）
  - ISO7321：1.7mA（5V 电源供电时），1.2mA（3.3V 电源供电时）
- 低传播延迟：典型值 33ns（5V 电源供电时）
- 3.3V 和 5V 电平转换
- 宽温度范围：-40°C 至 125°C
- 65KV/μs 瞬态抗扰度，典型值（5V 电源供电时）
- 优异的电磁兼容性 (EMC)
  - 系统级静电放电 (ESD)、瞬态放电 (EFT) 以及抗浪涌保护
  - 低辐射
- 隔离隔栅寿命：> 25 年
- 可由 3.3V 和 5V 电压供电
- 窄体小尺寸集成电路 (SOIC)-8 封装
- 安全及管理批准：
  - 符合 DIN V VDE V 0884-10 和 DIN EN 61010-1 标准的 4242 $V_{PK}$ 隔离中的 4242 VPK 部分
  - 符合 UL 1577 标准且长达 1 分钟的 3000$V_{RMS}$ 隔离
  - CSA 组件接受通知 5A，IEC 60950-1、IEC 60601-1 和 IEC 61010-1 标准中 CSA 组件接受列表项的"（审批正在审理中）"
  - 通过 GB4943.1-2011 CQC 认证

## 2 应用

- 在下列应用中的光电耦合器替代产品：
  - 工业用 FieldBus
    - ProfiBus
    - ModBus
    - DeviceNet™ 数据总线
  - 伺服控制接口
  - 电机控制
  - 电源
  - 电池组

## 3 说明

ISO732x 可提供符合 UL 标准的长达 1 分钟且高达 3000 $V_{RMS}$ 的电流隔离，以及符合 VDE 标准的 4242 $V_{PK}$ 隔离。 这些器件具有两个隔离通道，其逻辑输入和输出缓冲器由二氧化硅 (SiO$_2$) 绝缘隔栅分离开来。 ISO7320 的两个通道方向相同，而 ISO7321 的两个通道方向相反。 如果出现输入功率或信号损失，则后缀为"F"的器件默认输出"低"电平，后缀没有"F"的器件则默认输出"高"电平。 更多详细信息，请参见 *器件功能模式*。 与隔离电源配合使用，这些器件可防止数据总线或者其它电路上的噪声电流进入本地接地并且干扰或损坏敏感电路。 ISO732x 已针对恶劣环境集成了噪声滤波器，在此类环境下，器件的输入引脚上可能会出现短噪音脉冲。 ISO732x 具有晶体管晶体管逻辑电路 (TTL) 输入阈值，工作电压范围为 3V 到 5.5V。 凭借创新的芯片设计和布线技术，ISO732x 的电磁兼容性得到了显著增强，从而可确保提供系统级 ESD、EFT 和浪涌保护并符合辐射标准。
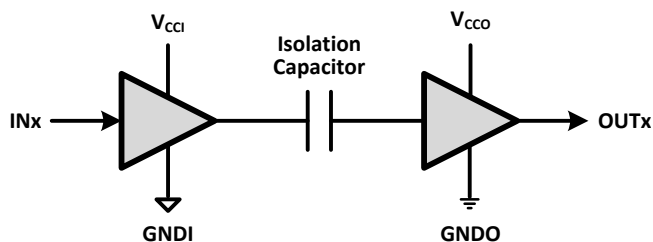
**器件信息**[1]

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| ISO7320C | SOIC (8) | 4.90mm x 3.91mm |
| ISO7320FC | | |
| ISO7321C | | |
| ISO7321FC | | |

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

部分增加了脚注。

**简化电路原理图**



(1) $V_{CCI}$ 和 GNDI 分别是输入通道的电源和接地连接。

(2) $V_{CCO}$ 和 GNDO 分别是输出通道的电源和接地连接。

English Data Sheet: SLLSEK8

# 目录

# 4 修订历史记录

**Changes from Revision B (April 2015) to Revision C**                                              **Page**

- 已添加"和 DINEN 61010-1 标准"至*特性* ................................................................................................................ 1
- 已删除*特性* ....................................................................................................................................................... 1
- Changed From: $V_{CC1}$ To: $V_{CCI}$ in Figure 11 ....................................................................................................... 9
- Changed From: $V_{CC1}$ To: $V_{CCI}$ and From: $V_{CC2}$ To: $V_{CCO}$ in Figure 13 ..................................................................... 9
- Deleted IEC from the section title: Insulation and Safety-Related Specifications for D-8 Package ................................... 11
- Changed the CTI Test Conditions in *Insulation and Safety-Related Specifications for D-8 Package* ............................... 11
- Changed $V_{ISO}$ Test Condition in the *Insulation Characteristics* table ............................................................................. 12

**Changes from Revision A (March 2015) to Revision B**                                              **Page**

- 将器件状态从：产品预览改为：量产 ........................................................................................................................ 1

**Changes from Original (January 2015) to Revision A**                                              **Page**

- 从仅首页更改为完整数据表。 ................................................................................................................................ 1
- 将 $V_{CC1}$ 更改为 $V_{CCI}$、$V_{CC2}$ 更改为 $V_{CCO}$、GND1 更改为 GNDI、GND2 更改为 GND0，并在*简化电路原理图*..................... 1

# 5 Pin Configuration and Functions

**ISO7320**
**D PACKAGE**
**(TOP VIEW)**

**ISO7321**
**D PACKAGE**
**(TOP VIEW)**
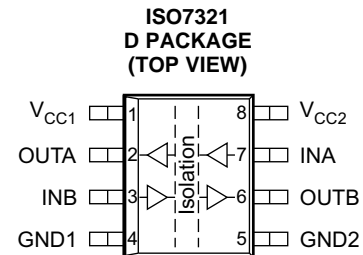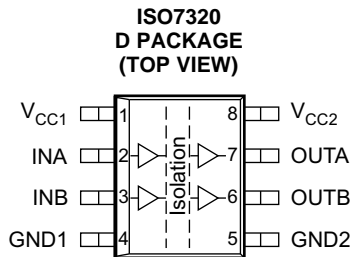
**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | ISO7320 | ISO7321 | | |
| INA | 2 | 7 | I | Input, channel A |
| INB | 3 | 3 | I | Input, channel B |
| GND1 | 4 | 4 | – | Ground connection for $V_{CC1}$ |
| GND2 | 5 | 5 | – | Ground connection for $V_{CC2}$ |
| OUTA | 7 | 2 | O | Output, channel A |
| OUTB | 6 | 6 | O | Output, channel B |
| $V_{CC1}$ | 1 | 1 | – | Power supply, $V_{CC1}$ |
| $V_{CC2}$ | 8 | 8 | – | Power supply, $V_{CC2}$ |

# 6 Specifications

## 6.1 Absolute Maximum Ratings[1]

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC1}$ , $V_{CC2}$[2] |  | −0.5 | 6 | V |
| Voltage [2] | INx, OUTx | −0.5 | $V_{CC}$+ 0.5[3] | V |
| Output current, $I_O$ |  |  | ±15 | mA |
| Junction temperature, $T_J$ |  |  | 150 | °C |
| Storage temperature, $T_{stg}$ |  | −65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

## 6.2 ESD Ratings

|  |  | VALUE | UNIT |
|---|---|---|---|
| $V_{ESD}$ | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±4000 | V |
|  | Charged device model (CDM), per JEDEC specification JESD22-C101[2] | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

|  |  | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Supply voltage | 3 |  | 5.5 | V |
| $I_{OH}$ | High-level output current | −4 |  |  | mA |
| $I_{OL}$ | Low-level output current |  |  | 4 | mA |
| $V_{IH}$ | High-level input voltage | 2 |  | 5.5 | V |
| $V_{IL}$ | Low-level input voltage | 0 |  | 0.8 | V |
| $t_{ui}$ | Input pulse duration | 40 |  |  | ns |
| $1 / t_{ui}$ | Signaling rate | 0 |  | 25 | Mbps |
| $T_J$ [1] | Junction temperature |  |  | 136 | °C |
| $T_A$ | Ambient temperature | -40 | 25 | 125 | °C |

(1) To maintain the recommended operating conditions for $T_J$, see the *Thermal Information* table.

## 6.4 Thermal Information

| THERMAL METRIC[1] |  |  | D PACKAGE | UNIT |
|---|---|---|---|---|
|  |  |  | (8) PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance |  | 121 | °C/W |
| $R_{\theta JCtop}$ | Junction-to-case (top) thermal resistance |  | 67.9 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance |  | 61.6 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter |  | 21.5 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter |  | 61.1 | |
| $R_{\theta JCbot}$ | Junction-to-case (bottom) thermal resistance |  | N/A | |
| $P_D$ (ISO7320) | Maximum power dissipation by ISO7320 | $V_{CC1}$ = $V_{CC2}$ = 5.5 V, $T_J$ = 150°C, $C_L$ = 15 pF, Input a 12.5 MHz 50% duty-cycle square wave | 56 | mW |
| $P_{D1}$ (ISO7320) | Maximum power dissipation by side-1 of ISO7320 |  | 15 | |
| $P_{D2}$ (ISO7320) | Maximum power dissipation by side-2 of ISO7320 |  | 41 | |
| $P_D$ (ISO7321) | Maximum power dissipation by ISO7321 | $V_{CC1}$ = $V_{CC2}$ = 5.5 V, $T_J$ = 150°C, $C_L$ = 15 pF, Input a 12.5 MHz 50% duty-cycle square wave | 67 | mW |
| $P_{D1}$ (ISO7321) | Maximum power dissipation by side-1 of ISO7321 |  | 33.5 | |
| $P_{D2}$ (ISO7321) | Maximum power dissipation by side-2 of ISO7321 |  | 33.5 | |

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

## 6.5 Electrical Characteristics, 5 V

$V_{CC1}$ and $V_{CC2}$ at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 mA; see Figure 11 | | $V_{CCO}^{(1)}$– 0.5 | 4.7 | | V |
| | | $I_{OH}$ = –20 µA; see Figure 11 | | $V_{CCO}^{(1)}$ – 0.1 | 5 | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA; see Figure 11 | | | 0.2 | 0.4 | V |
| | | $I_{OL}$ = 20 µA; see Figure 11 | | | 0 | 0.1 | |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | | | 460 | | mV |
| $I_{IH}$ | High-level input current | IN = $V_{CC}$ | | | | 10 | µA |
| $I_{IL}$ | Low-level input current | IN = 0 V | | –10 | | | µA |
| CMTI | Common-mode transient immunity | $V_I$ = $V_{CC}$ or 0 V; see Figure 13. | | 25 | 65 | | kV/µs |
| **SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic $I_{CC}$ measurement)** | | | | | | | |
| **ISO7320** | | | | | | | |
| $I_{CC1}$ | | DC to 1 Mbps | DC Input: $V_I$ = $V_{CC}$ or 0 V, AC Input: $C_L$ = 15pF | | 0.4 | 0.9 | mA |
| $I_{CC2}$ | | | | | 2 | 3.2 | |
| $I_{CC1}$ | Supply current for $V_{CC1}$ and $V_{CC2}$ | 10 Mbps | $C_L$ = 15pF | | 0.8 | 1.4 | |
| $I_{CC2}$ | | | | | 3.2 | 4.4 | |
| $I_{CC1}$ | | 25 Mbps | $C_L$ = 15pF | | 1.4 | 2.3 | |
| $I_{CC2}$ | | | | | 4.9 | 6.8 | |
| **ISO7321** | | | | | | | |
| $I_{CC1}$ , $I_{CC2}$ | | DC to 1 Mbps | DC Input: $V_I$ = $V_{CC}$ or 0 V, AC Input: $C_L$ = 15pF | | 1.7 | 2.8 | mA |
| $I_{CC1}$ , $I_{CC2}$ | Supply current for $V_{CC1}$ and $V_{CC2}$ | 10 Mbps | $C_L$ = 15pF | | 2.5 | 3.7 | |
| $I_{CC1}$ , $I_{CC2}$ | | 25 Mbps | $C_L$ = 15pF | | 3.7 | 5.4 | |

(1)   $V_{CCO}$ is supply voltage, $V_{CC1}$ or $V_{CC2}$, for the output channel being measured.

## 6.6 Electrical Characteristics, 3.3 V

$V_{CC1}$ and $V_{CC2}$ at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

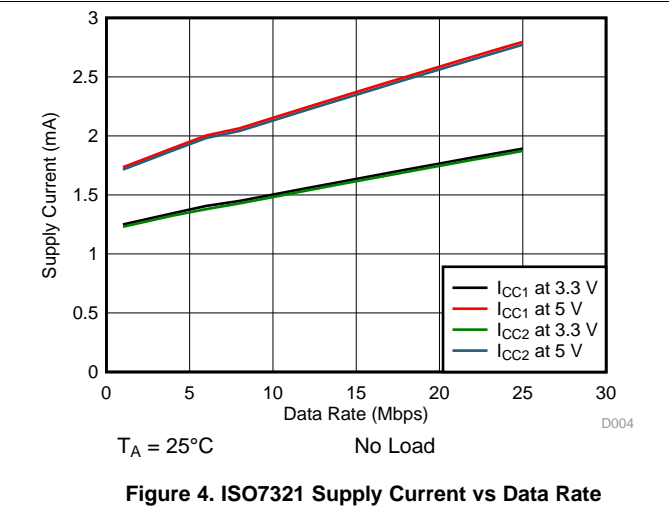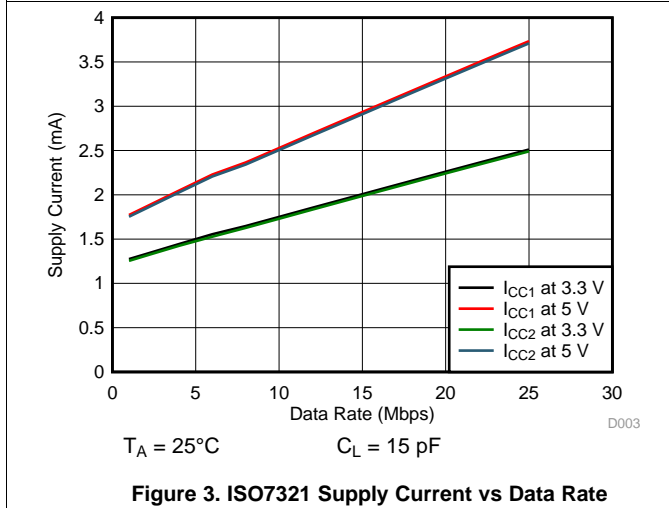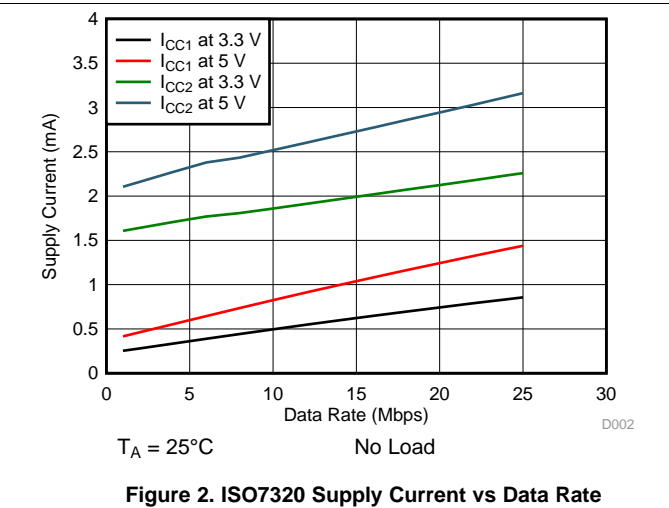| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –4 mA; see Figure 11 | | $V_{CCO}^{(1)}$– 0.5 | 3 | | V |
| | | $I_{OH}$ = –20 µA; see Figure 11 | | $V_{CCO}^{(1)}$ – 0.1 | 3.3 | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA; see Figure 11 | | | 0.2 | 0.4 | V |
| | | $I_{OL}$ = 20 µA; see Figure 11 | | | 0 | 0.1 | |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | | | 450 | | mV |
| $I_{IH}$ | High-level input current | IN = $V_{CC}$ | | | | 10 | µA |
| $I_{IL}$ | Low-level input current | IN = 0 V | | -10 | | | µA |
| CMTI | Common-mode transient immunity | $V_I$ = $V_{CC}$ or 0 V; see Figure 13 | | 25 | 50 | | kV/µs |
| **SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic $I_{CC}$ measurement)** | | | | | | | |
| **ISO7320** | | | | | | | |
| $I_{CC1}$ | | DC to 1 Mbps | DC Input: $V_I$ = $V_{CC}$ or 0 V, AC Input: $C_L$ = 15pF | | 0.2 | 0.5 | mA |
| $I_{CC2}$ | | | | | 1.5 | 2.5 | |
| $I_{CC1}$ | Supply current for $V_{CC1}$ and $V_{CC2}$ | 10 Mbps | $C_L$ = 15pF | | 0.5 | 0.8 | |
| $I_{CC2}$ | | | | | 2.2 | 3.2 | |
| $I_{CC1}$ | | 25 Mbps | $C_L$ = 15pF | | 0.9 | 1.4 | |
| $I_{CC2}$ | | | | | 3.3 | 4.7 | |
| **ISO7321** | | | | | | | |
| $I_{CC1}$ , $I_{CC2}$ | | DC to 1 Mbps | DC Input: $V_I$ = $V_{CC}$ or 0 V, AC Input: $C_L$ = 15pF | | 1.2 | 2 | mA |
| $I_{CC1}$ , $I_{CC2}$ | Supply current for $V_{CC1}$ and $V_{CC2}$ | 10 Mbps | $C_L$ = 15pF | | 1.7 | 2.5 | |
| $I_{CC1}$ , $I_{CC2}$ | | 25 Mbps | $C_L$ = 15pF | | 2.5 | 3.6 | |

(1)   $V_{CCO}$ is supply voltage, $V_{CC1}$ or $V_{CC2}$, for the output channel being measured.

## 6.7 Switching Characteristics, 5 V

$V_{CC1}$ and $V_{CC2}$ at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 11 | 20 | 33 | 57 | ns |
| PWD[1] | Pulse width distortion $|t_{PHL} - t_{PLH}|$ | | | | 4 | ns |
| $t_{sk(o)}$[2] | Channel-to-channel output skew time | ISO7320 | | | 2 | ns |
| | | ISO7321 | | | 17 | |
| $t_{sk(pp)}$[3] | Part-to-part skew time | | | | 23 | ns |
| $t_r$ | Output signal rise time | See Figure 11 | | 2.4 | | ns |
| $t_f$ | Output signal fall time | | | 2.1 | | ns |
| $t_{fs}$ | Fail-safe output delay time from input power loss | See Figure 12 | | 7.5 | | µs |

(1)  Also known as pulse skew.
(2)  $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3)  $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
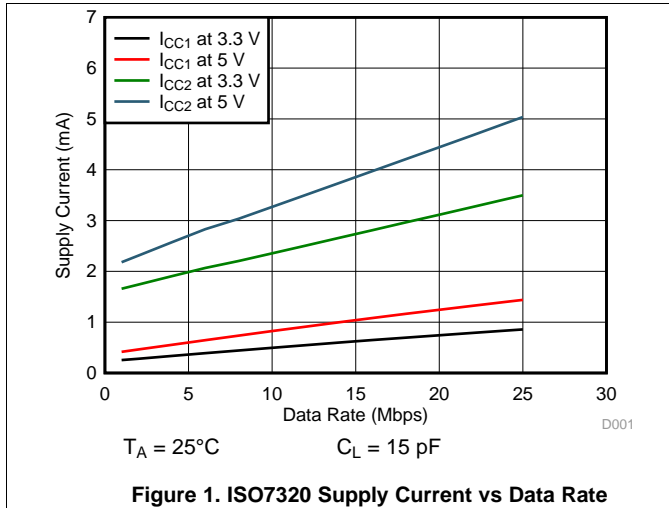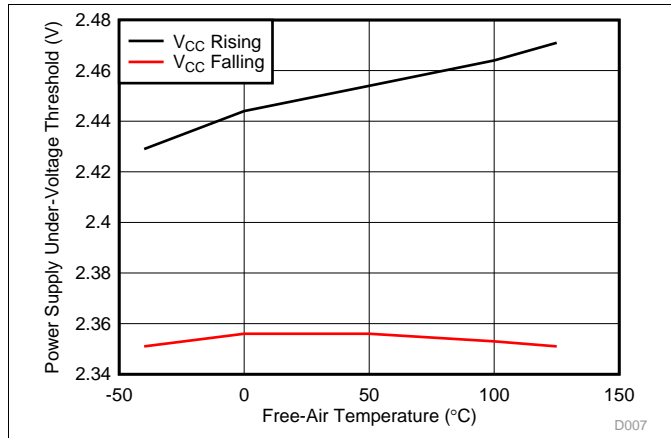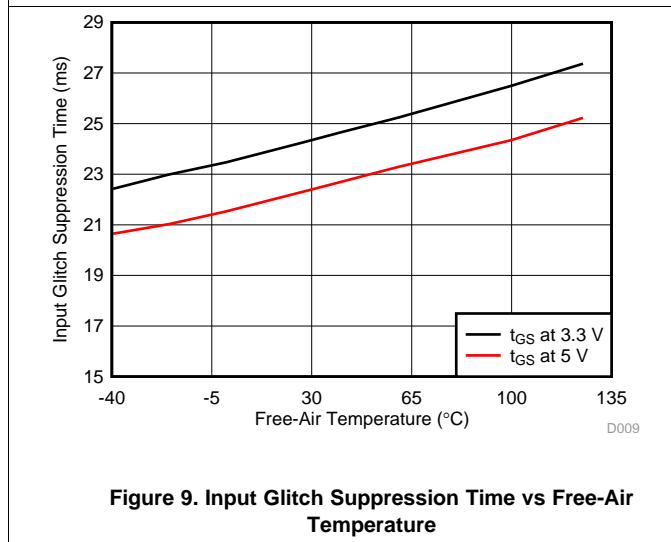
## 6.8 Switching Characteristics, 3.3 V

$V_{CC1}$ and $V_{CC2}$ at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT3 |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 11 | 22 | 37 | 66 | ns |
| PWD[1] | Pulse width distortion $|t_{PHL} - t_{PLH}|$ | | | | 3 | ns |
| $t_{sk(o)}$[2] | Channel-to-channel output skew time | ISO7320 | | | 3 | ns |
| | | ISO7321 | | | 16 | |
| $t_{sk(pp)}$[3] | Part-to-part skew time | | | | 28 | ns |
| $t_r$ | Output signal rise time | See Figure 11 | | 3.1 | | ns |
| $t_f$ | Output signal fall time | | | 2.6 | | ns |
| $t_{fs}$ | Fail-safe output delay time from input power loss | See Figure 12 | | 7.4 | | µs |

(1)  Also known as pulse skew.
(2)  $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3)  $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 6.9 Typical Characteristics



**Figure 1. ISO7320 Supply Current vs Data Rate**



**Figure 2. ISO7320 Supply Current vs Data Rate**



**Figure 3. ISO7321 Supply Current vs Data Rate**



**Figure 4. ISO7321 Supply Current vs Data Rate**



**Figure 5. High-Level Output Voltage vs High-Level Output Current**



**Figure 6. :Low-Level Output Voltage vs Low-Level Output Current**
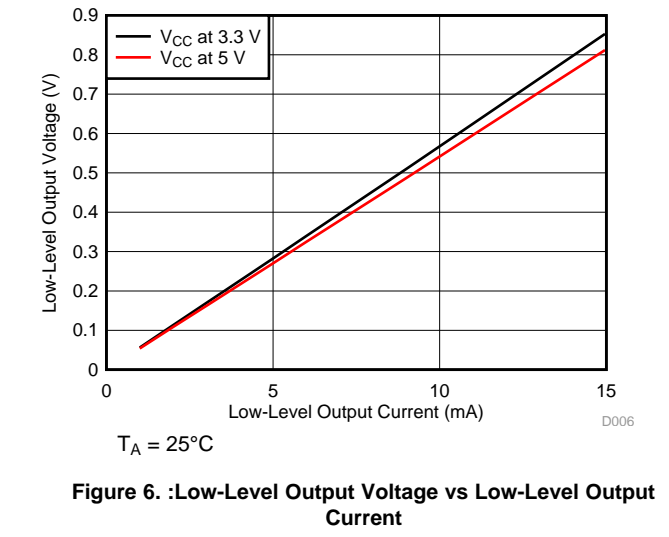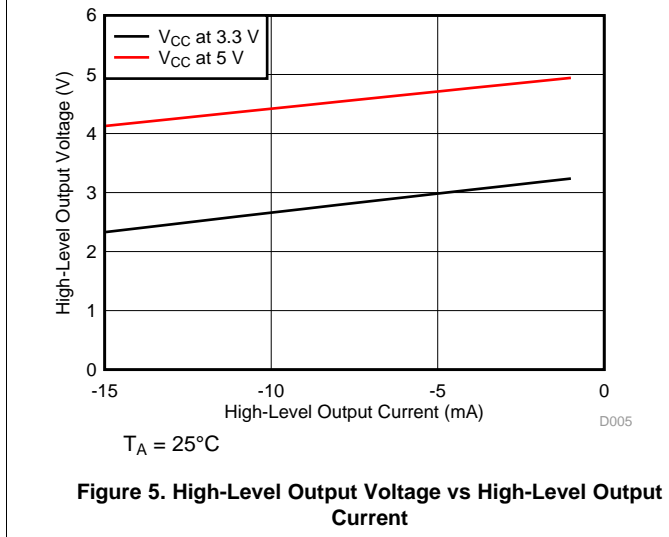
## Typical Characteristics (continued)



Figure 7. Power Supply Under Voltage Threshold vs Free-Air Temperature
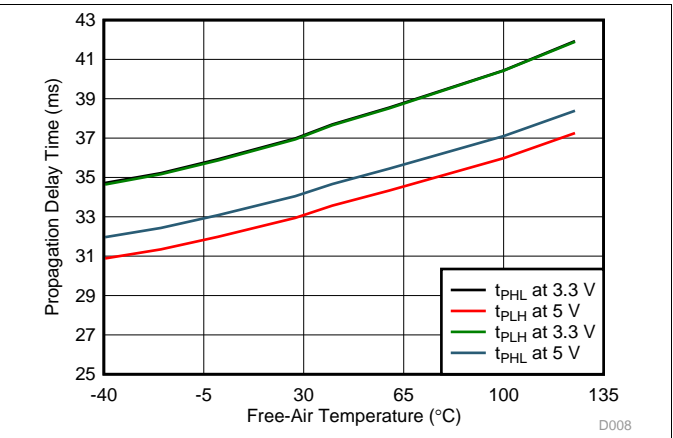


Figure 8. Propagation Delay Time vs Free-Air Temperature



Figure 9. Input Glitch Suppression Time vs Free-Air Temperature
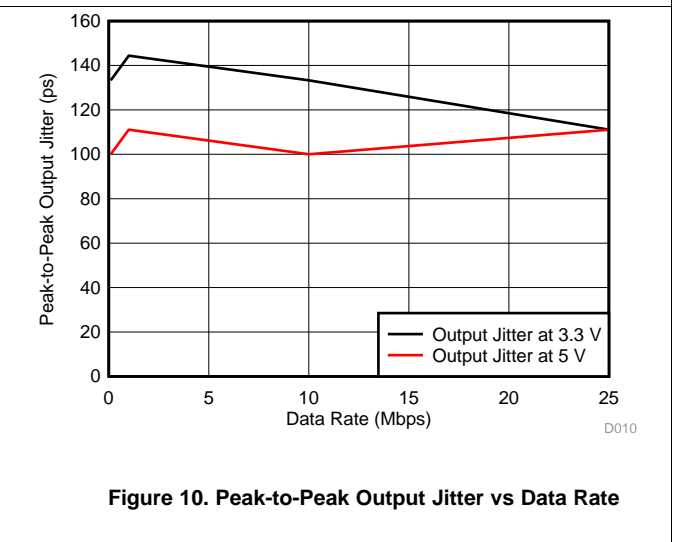


Figure 10. Peak-to-Peak Output Jitter vs Data Rate

# 7 Parameter Measurement Information
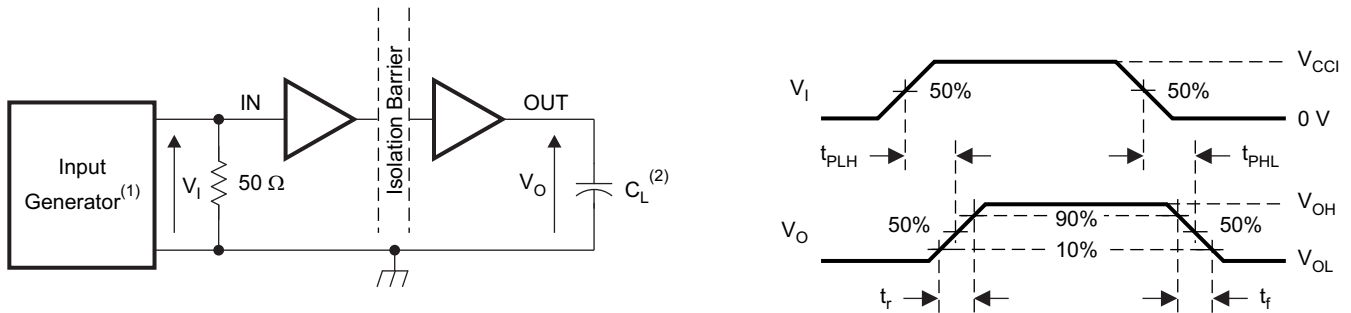


(1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.

(2) $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 11. Switching Characteristic Test Circuit and Voltage Waveforms**
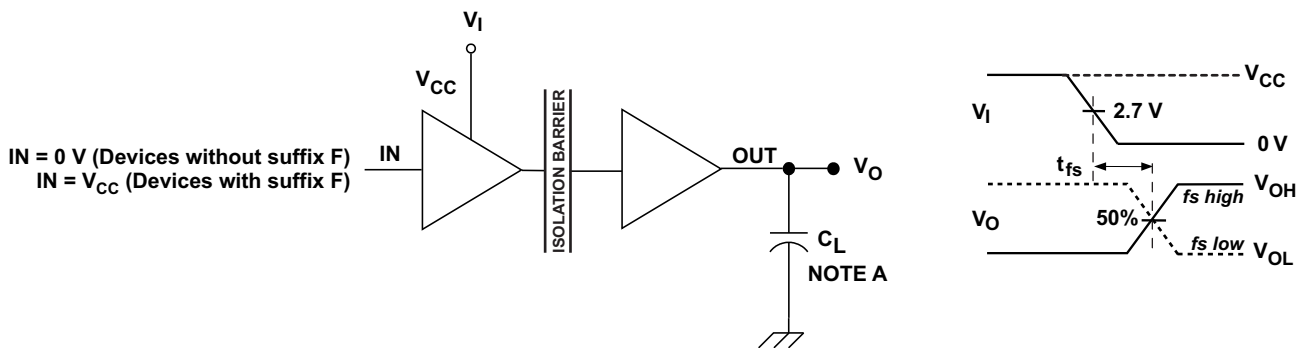


A.  $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 12. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms**
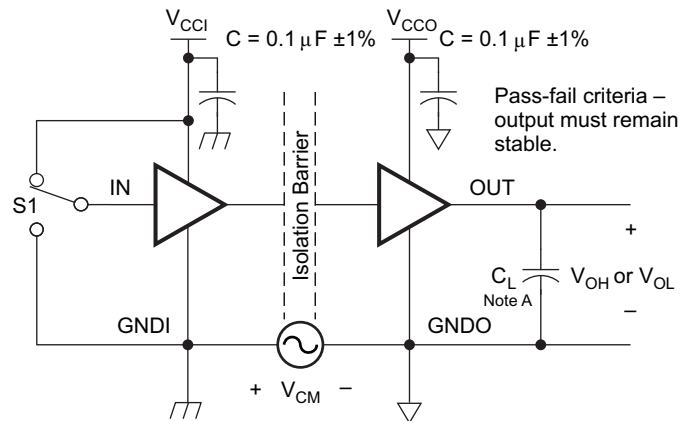


(1) $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 13. Common-Mode Transient Immunity Test Circuit**

# 8 Detailed Description

## 8.1 Overview

The isolator in Figure 14 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency (HF) channel with a bandwidth from 100 kbps up to 25 Mbps, and a low-frequency (LF) channel covering the range from 100 kbps down to DC.

In principle, a single-ended input signal entering the HF channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transient pulses, which then are converted into CMOS levels by a comparator. The transient pulses at the input of the comparator can be either above or below the common mode voltage VREF depending on whether the input bit transitioned from 0 to 1 or 1 to 0. The comparator threshold is adjusted based on the expected bit transition. A decision logic (DCL) at the output of the HF channel comparator measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high-frequency to the low-frequency channel.

## 8.2 Functional Block Diagram
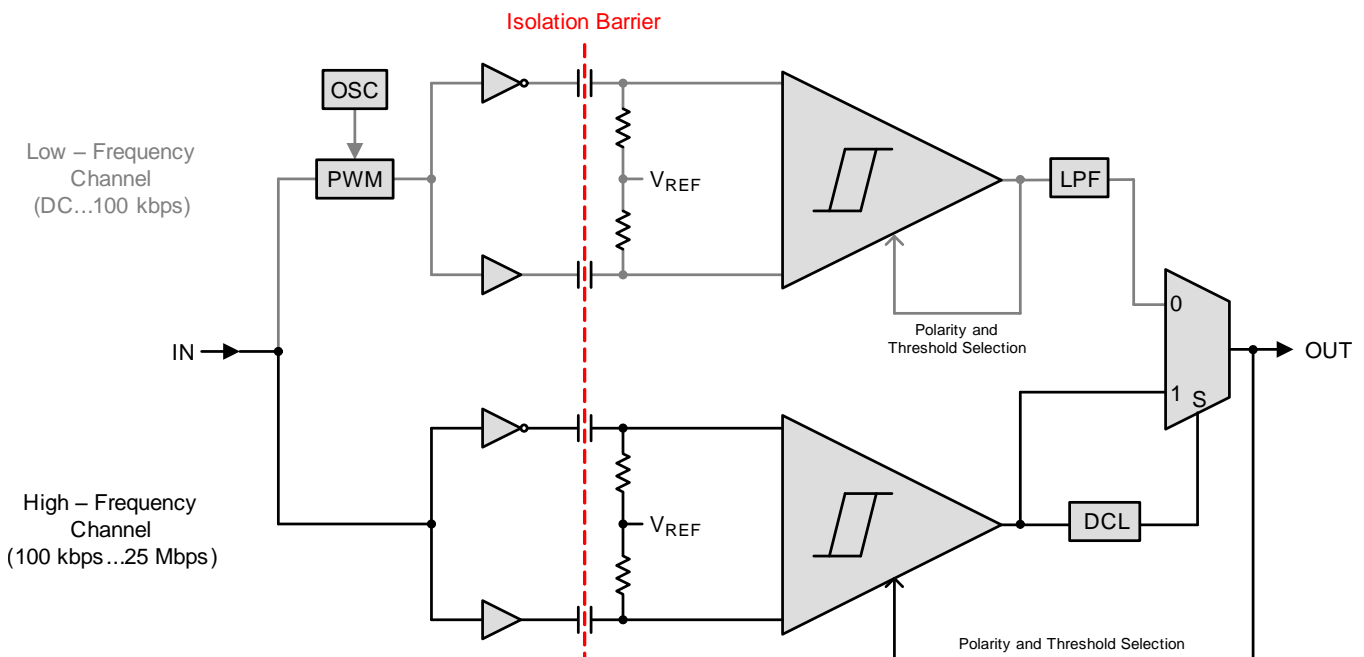


**Figure 14. Conceptual Block Diagram of a Digital Capacitive Isolator**

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

## 8.3 Feature Description

| PRODUCT | CHANNEL DIRECTION | RATED ISOLATION | MAX DATA RATE | DEFAULT OUTPUT |
|---|---|---|---|---|
| ISO7320C | Same | 3000 $V_{RMS}$ / 4242 $V_{PK}$ [1] | 25 Mbps | High |
| ISO7320FC | | | | Low |
| ISO7321C | Opposite | | | High |
| ISO7321FC | | | | Low |

(1)   See the *Regulatory Information* section for detailed Isolation Ratings

### 8.3.1  High Voltage Feature Description

#### 8.3.1.1  *Insulation and Safety-Related Specifications for D-8 Package*

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| L(I01) | Minimum air gap (clearance) | Shortest terminal-to-terminal distance through air | 4 | | | mm |
| L(I02) | Minimum external tracking (creepage) | Shortest terminal-to-terminal distance across the package surface | 4 | | | mm |
| CTI | Tracking resistance (comparative tracking index) | DIN EN 60112 (VDE 0303-11); IEC 60112 | 400 | | | V |
| DTI | Minimum internal gap (internal clearance) | Distance through insulation | 13 | | | µm |
| $R_{IO}$ | Isolation resistance, input to output[1] | $V_{IO}$ = 500 V, $T_A$ = 25°C | $10^{12}$ | | | Ω |
| | | $V_{IO}$ = 500 V, 100°C ≤ $T_A$ ≤ 125°C | $10^{11}$ | | | Ω |
| $C_{IO}$ | Isolation capacitance, input to output[1] | $V_{IO}$ = 0.4 sin (2πft), f = 1 MHz | | | 1.5 | pF |
| $C_I$ | Input capacitance[2] | $V_I$ = $V_{CC}$/2 + 0.4 sin (2πft), f = 1 MHz, $V_{CC}$ = 5 V | | | 1.8 | pF |

(1)   All pins on each side of the barrier tied together creating a two-terminal device.
(2)   Measured from input pin to ground.

---

**NOTE**

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

---

### 8.3.1.2  Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER[1] | | TEST CONDITIONS | SPECIFICATION | UNIT |
|---|---|---|---|---|
| $V_{IOWM}$ | Maximum isolation working voltage | | 400 | $V_{RMS}$ |
| $V_{IORM}$ | Maximum repetitive peak voltage per DIN V VDE V 0884-10 | | 566 | $V_{PK}$ |
| $V_{PR}$ | Input-to-output test voltage per DIN V VDE V 0884-10 | After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC | 680 | $V_{PK}$ |
| | | Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 s, Partial Discharge < 5 pC | 906 | |
| | | Method b1, $V_{PR} = V_{IORM}$ x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC | 1062 | |
| $V_{IOTM}$ | Maximum transient overvoltage per DIN V VDE V 0884-10 | $V_{TEST} = V_{IOTM}$ t = 60 sec (qualification) t= 1 sec (100% production) | 4242 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage per DIN V VDE V 0884-10 | Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.3$ x $V_{IOSM} = 7800$ $V_{PK}$ (qualification) | 6000 | $V_{PK}$ |
| $V_{ISO}$ | Withstand isolation voltage per UL 1577 | $V_{TEST} = V_{ISO} = 3000$ $V_{RMS}$, t = 60 sec (qualification); $V_{TEST} = 1.2$ x $V_{ISO} = 3600$ $V_{RMS}$, t = 1 sec (100% production) | 3000 | $V_{RMS}$ |
| $R_S$ | Insulation resistance | $V_{IO} = 500$ V at $T_S$ | >$10^9$ | Ω |
| | Pollution degree | | 2 | |

(1)  Climatic Classification 40/125/21

### Table 1. IEC 60664-1 Ratings Table

| PARAMETER | TEST CONDITIONS | SPECIFICATION |
|---|---|---|
| Basic isolation group | Material group | II |
| Installation classification | Rated mains voltage ≤ 150 $V_{RMS}$ | I–IV |
| | Rated mains voltage ≤ 300 $V_{RMS}$ | I–III |

### 8.3.1.3  Regulatory Information

| VDE | CSA | UL | CQC |
|---|---|---|---|
| Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 | Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 61010-1 | Recognized under UL 1577 Component Recognition Program | Certified according to GB4943.1-2011 |
| Basic Insulation Maximum Transient Overvoltage, 4242 $V_{PK}$ Maximum Surge Isolation Voltage, 6000 $V_{PK}$ Maximum Repetitive Peak Voltage, 566 $V_{PK}$ | 400 $V_{RMS}$ Basic Insulation and 200 $V_{RMS}$ Reinforced Insulation working voltage per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2; 300 $V_{RMS}$ Basic Insulation working voltage per CSA 61010-1-12 and IEC 61010-1 3rd Ed. | Single protection, 3000 $V_{RMS}$ [1] | Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 $V_{RMS}$ maximum working voltage |
| Certificate number: 40016131 | Master contract number: 220991 | File number: E181974 | Certificate number: CQC15001121656 |

(1)  Production tested ≥ 3600 $V_{RMS}$ for 1 second in accordance with UL 1577.

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### 8.3.1.4 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_S$ | Safety input, output, or supply current | $R_{\theta JA}$ = 121 °C/W, $V_I$ = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 188 | mA |
| | | $R_{\theta JA}$ = 121 °C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 287 | |
| $T_S$ | Maximum case temperature | | | | 150 | °C |

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolut Maximun Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.
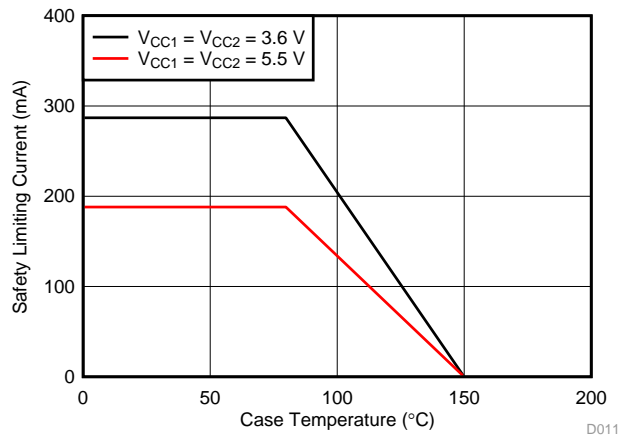


Figure 15. $\theta_{JC}$ Thermal Derating Curve per DIN V VDE V 0884-10

## 8.4 Device Functional Modes

**Table 2. Function Table[1]**

| $V_{CCI}$ | $V_{CCO}$ | INA, INB | OUTA, OUTB | |
|---|---|---|---|---|
| | | | ISO7320C, ISO7321C | ISO7320FC, ISO7321FC |
| PU | PU | H | H | H |
| | | L | L | L |
| | | Open | H[2] | L[3] |
| PD | PU | X | H[2] | L[3] |
| X | PD | X | Undetermined | Undetermined |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$; PU = Powered up ($V_{CC} \geq 3$ V); PD = Powered down ($V_{CC} \leq 2.1$ V); X = Irrelevant; H = High level; L = Low level; Open = Not connected
(2) In fail-safe condition, output defaults to high level
(3) In fail-safe condition, output defaults to low level

### 8.4.1 Device I/O Schematics
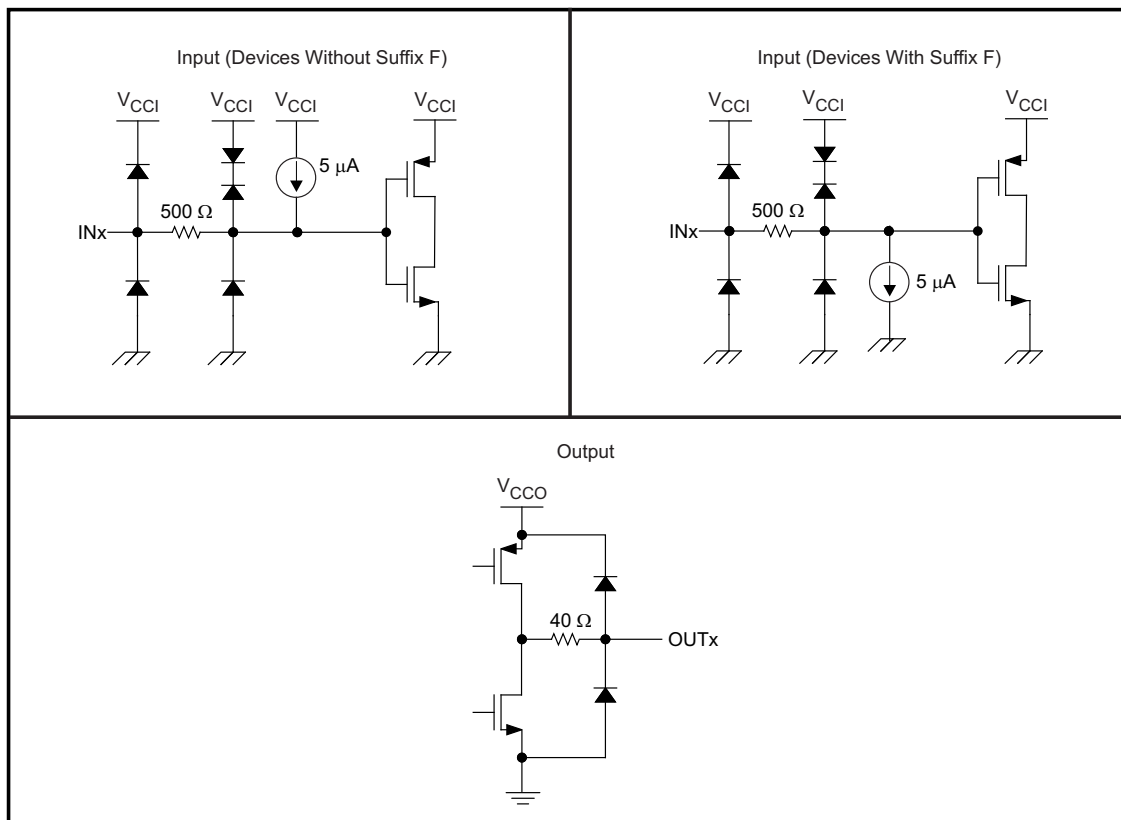


**Figure 16. Device I/O Schematics**

# 9 Applications and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

ISO732x utilize single-ended TTL-logic switching technology. Its supply voltage range is from 3 V to 5.5 V for both supplies, $V_{CC1}$ and $V_{CC2}$. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (i.e. µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

## 9.2 Typical Application

ISO7321 can be used with Texas Instruments' mixed signal micro-controller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4-20 mA current loop.
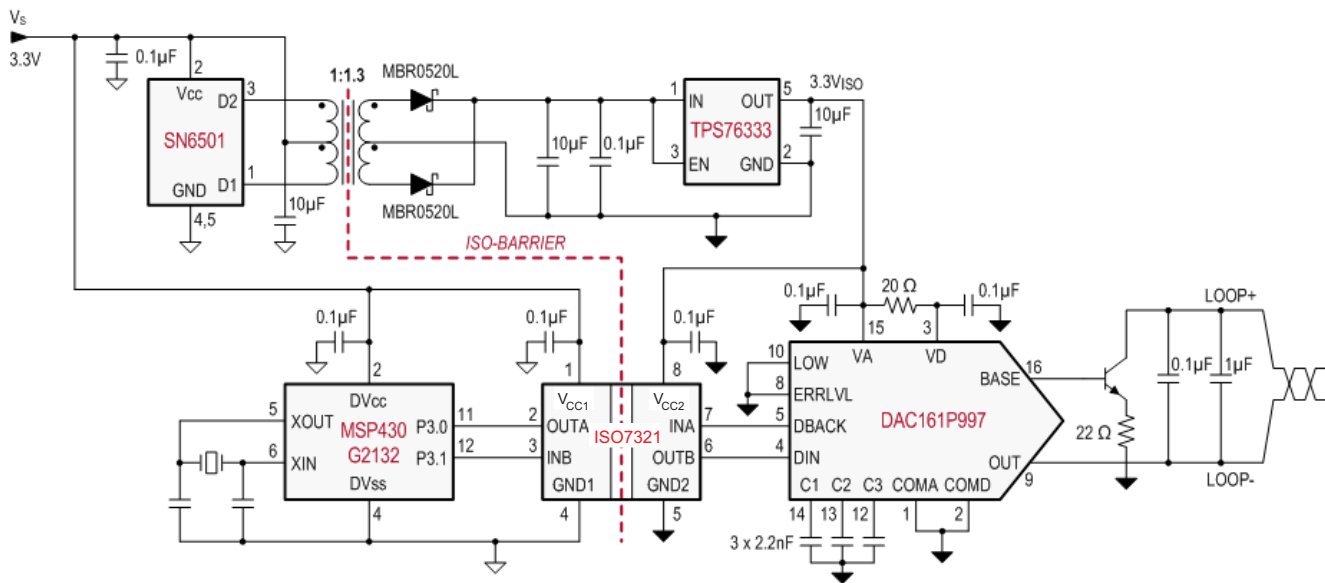


**Figure 17. Typical ISO7321 Application Circuit**

## Typical Application (continued)

### 9.2.1  Design Requirements

#### 9.2.1.1  Typical Supply Current Equations

**ISO7320:**

At $V_{CC1} = V_{CC2} = 5$ V
- $I_{CC1} = 0.3838 + (0.0431 \times f)$
- $I_{CC2} = 2.74567 + (0.08433 \times f) + (0.01 \times f \times C_L)$

At $V_{CC1} = V_{CC2} = 3.3$ V
- $I_{CC1} = 0.2394 + (0.02355 \times f)$
- $I_{CC2} = 2.10681 + (0.04374 \times f) + (0.007045 \times f \times C_L)$

**ISO7321:**

At $V_{CC1} = V_{CC2} = 5$ V
- $I_{CC1}$ and $I_{CC2} = 1.5877 + (0.066 \times f) + (0.00123 \times f \times C_L)$

At $V_{CC1} = V_{CC2} = 3.3$ V
- $I_{CC1}$ and $I_{CC2} = 1.187572 + (0.019399 \times f) + (0.0019029 \times f \times C_L)$

$I_{CC1}$ and $I_{CC2}$ are typical supply currents measured in mA, f is data rate measured in Mbps, $C_L$ is the capacitive load measured in pF.

### 9.2.2  Detailed Design Procedure

#### 9.2.2.1  Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO732x incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

### 9.2.3  Application Performance Curves

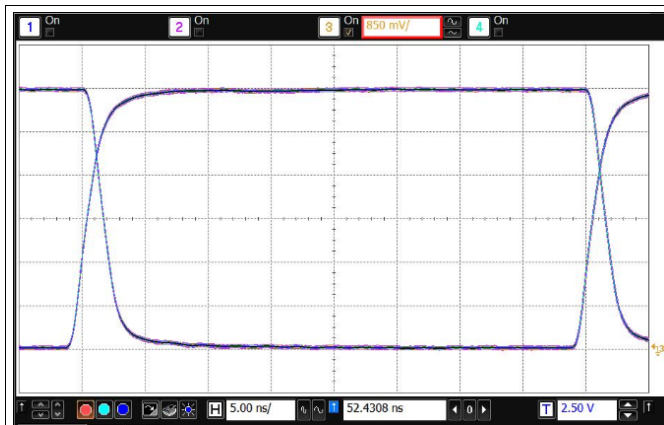Typical eye diagrams of ISO732x below indicate low jitter and wide open eye at the maximum data rate of 25 Mbps.



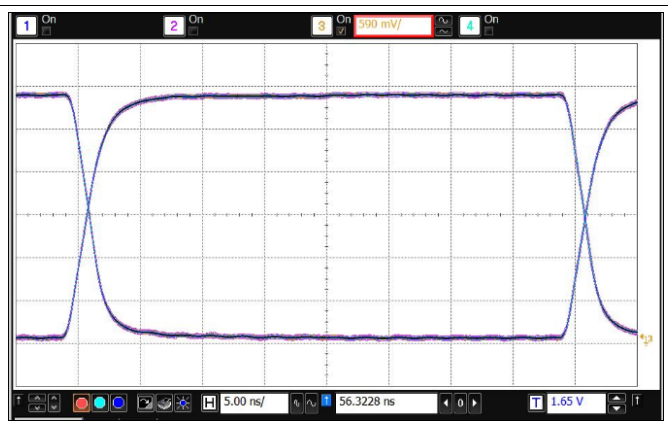Figure 18. Eye Diagram at 25 Mbps, 5 V and 25°C



Figure 19. Eye Diagram at 25 Mbps, 3.3 V and 25°C

# 10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins ($V_{CC1}$ & $V_{CC2}$). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 datasheet (SLLSEA0) .

# 11 Layout

## 11.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

## 11.2 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 20). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in$^2$.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

## 11.3 Layout Example
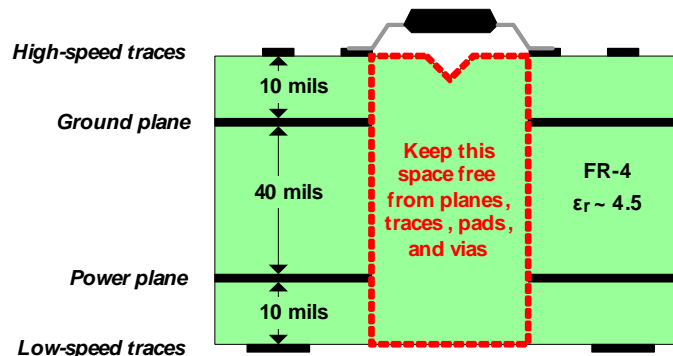


**Figure 20. Recommended Layer Stack**

## 12  器件和文档支持

### 12.1  相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **3.** 相关链接

| 器件 | 产品文件夹 | 样片与购买 | 技术文档 | 工具与软件 | 支持与社区 |
|---|---|---|---|---|---|
| ISO7320C | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| ISO7320FC | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| ISO7321C | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| ISO7321FC | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

### 12.2  商标

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### 12.3  静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.4  术语表

SLYZ022 — *TI* 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

《隔离相关术语》，SLLA353

## 13  机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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| 放大器和线性器件 | www.ti.com.cn/amplifiers | 计算机及周边 | www.ti.com.cn/computer |
| 数据转换器 | www.ti.com.cn/dataconverters | 消费电子 | www.ti.com/consumer-apps |
| DLP® 产品 | www.dlp.com | 能源 | www.ti.com/energy |
| DSP - 数字信号处理器 | www.ti.com.cn/dsp | 工业应用 | www.ti.com.cn/industrial |
| 时钟和计时器 | www.ti.com.cn/clockandtimers | 医疗电子 | www.ti.com.cn/medical |
| 接口 | www.ti.com.cn/interface | 安防应用 | www.ti.com.cn/security |
| 逻辑 | www.ti.com.cn/logic | 汽车电子 | www.ti.com.cn/automotive |
| 电源管理 | www.ti.com.cn/power | 视频和影像 | www.ti.com.cn/video |
| 微控制器 (MCU) | www.ti.com.cn/microcontrollers | | |
| RFID 系统 | www.ti.com.cn/rfidsys | | |
| OMAP应用处理器 | www.ti.com/omap | | |
| 无线连通性 | www.ti.com.cn/wirelessconnectivity | 德州仪器在线技术支持社区 | www.deyisupport.com |

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7320CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7320C | Samples |
| ISO7320CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7320C | Samples |
| ISO7320FCD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7320FC | Samples |
| ISO7320FCDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7320FC | Samples |
| ISO7321CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7321C | Samples |
| ISO7321CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7321C | Samples |
| ISO7321FCD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7321FC | Samples |
| ISO7321FCDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 7321FC | Samples |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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![Texas Instruments logo]

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|-------------------------------------------------------|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|------|-----------|---------|---------|---------|---------|---------|--------|---------------|
| ISO7320CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7320FCDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7321CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO7321FCDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ISO7320CDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 38.0 |
| ISO7320FCDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 38.0 |
| ISO7321CDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 38.0 |
| ISO7321FCDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 38.0 |

# 重要声明

| 产品 | | 应用 | |
|---|---|---|---|
| 数字音频 | www.ti.com.cn/audio | 通信与电信 | www.ti.com.cn/telecom |
| 放大器和线性器件 | www.ti.com.cn/amplifiers | 计算机及周边 | www.ti.com.cn/computer |
| 数据转换器 | www.ti.com.cn/dataconverters | 消费电子 | www.ti.com/consumer-apps |
| DLP® 产品 | www.dlp.com | 能源 | www.ti.com/energy |
| DSP - 数字信号处理器 | www.ti.com.cn/dsp | 工业应用 | www.ti.com.cn/industrial |
| 时钟和计时器 | www.ti.com.cn/clockandtimers | 医疗电子 | www.ti.com.cn/medical |
| 接口 | www.ti.com.cn/interface | 安防应用 | www.ti.com.cn/security |
| 逻辑 | www.ti.com.cn/logic | 汽车电子 | www.ti.com.cn/automotive |
| 电源管理 | www.ti.com.cn/power | 视频和影像 | www.ti.com.cn/video |
| 微控制器 (MCU) | www.ti.com.cn/microcontrollers | | |
| RFID 系统 | www.ti.com.cn/rfidsys | | |
| OMAP应用处理器 | www.ti.com/omap | | |
| 无线连通性 | www.ti.com.cn/wirelessconnectivity | 德州仪器在线技术支持社区 | www.deyisupport.com |

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