

EMC 性能优异的 ISO772x-Q1 高速双通道增强型数字隔离器

1 特性

- 汽车电子 应用认证
- 具有符合 AEC-Q100 标准的下列结果：
 - 器件温度 1 级：-40°C 至 +125°C 的环境运行温度范围
 - 器件人体放电模型 (HBM) 静电放电 (ESD) 分类等级 3A
 - 器件组件充电模式 (CDM) ESD 分类等级 C6
- 信号传输速率：高达 100Mbps
- 宽电源电压范围：2.25V 至 5.5V
- 2.25V 和 5V 电平转换
- 默认输出高电平和低电平选项
- 低功耗，1Mbps 时每通道的电流典型值为 1.7mA
- 低传播延迟：典型值为 11ns（由 5V 电源供电）
- 高共模瞬态抗扰度 (CMTI)：±100kV/μs（典型值）
- 优异的电磁兼容性 (EMC)
 - 系统级静电放电 (ESD)、瞬态放电 (EFT) 以及抗浪涌保护
 - 低辐射
- 隔离栅寿命：> 40 年
- 宽体小外形尺寸集成电路 (SOIC) (DW-16) 和窄体小外形尺寸集成电路 (SOIC) (D-8) 封装选项
- 安全相关认证：
 - VDE 增强型隔离，符合 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 标准
 - 符合 UL 1577 的 5000V_{RMS} (DW) 和 3000V_{RMS} (D) 隔离额定值
 - CSA 组件验收通知 5A、IEC 60950-1 和 IEC 60601-1 终端设备标准
 - 符合 GB4943.1-2011 的 CQC 认证
 - 符合 EN 60950-1 和 EN 61010-1 标准的 TUV 认证
 - 完成 DW 封装的 VDE、UL、CSA 和 TUV 认证；已规划其他所有认证

2 应用

- 混合动力电动汽车
- 电机控制
- 电源
- 太阳能逆变器

3 说明

ISO772x-Q1 器件是高性能双通道数字隔离器，可提供符合 UL 1577 的 5000V_{RMS} (DW 封装) 和 3000V_{RMS} (D 封装) 隔离额定值。这些器件还通过了 VDE、TUV、CSA 和 CQC 认证。

在隔离互补金属氧化物半导体 (CMOS) 或者低电压互补金属氧化物半导体 (LVCMOS) 数字 I/O 的同时，ISO772x-Q1 器件还可提供高电磁抗扰度和低辐射，同时具备低功耗特性。每个隔离通道都有一个由二氧化硅 (SiO₂) 绝缘隔栅分开的逻辑输入和输出缓冲器。ISO7720-Q1 器件具有两条同向通道，而 -Q1 器件具有两条反向通道。如果输入功率或信号出现损失，不带后缀 F 的器件默认输出高电平，带后缀 F 的器件默认输出低电平。更多详细信息，请参见 [Device Functional Modes](#) 器件功能模式 部分。

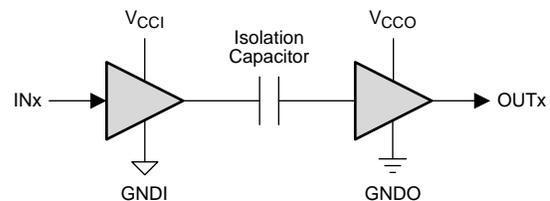
与隔离式电源一起使用时，这些器件有助于防止数据总线或者其他电路上的噪声电流进入本地接地并且干扰或损坏敏感电路。凭借创新型芯片设计和布线技术，ISO772x-Q1 器件的电磁兼容性得到了显著增强，可缓解系统级 ESD、EFT 和浪涌问题并符合辐射标准。ISO772x-Q1 系列器件可提供 16 引脚 SOIC 宽体 (DW) 和 8 引脚 SOIC 窄体 (D) 封装。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
ISO7720-Q1	SOIC (D)	4.90mm x 3.91mm
ISO7721-Q1	SOIC (DW)	10.30mm x 7.50mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

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V_{CCI} 和 GNDI 分别是输入通道的电源和接地连接。

V_{CCO} 和 GNDO 分别是输出通道的电源和接地连接。



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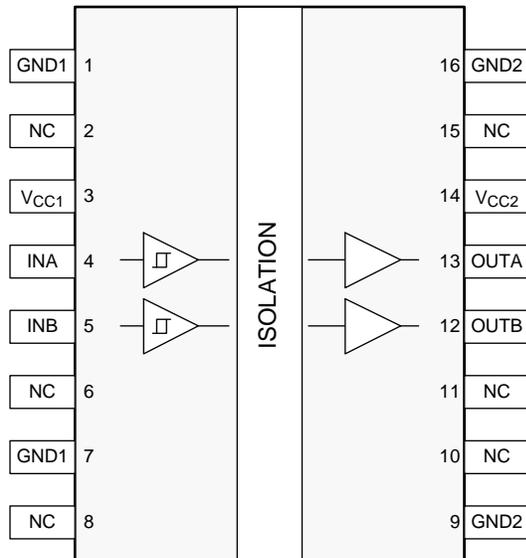
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

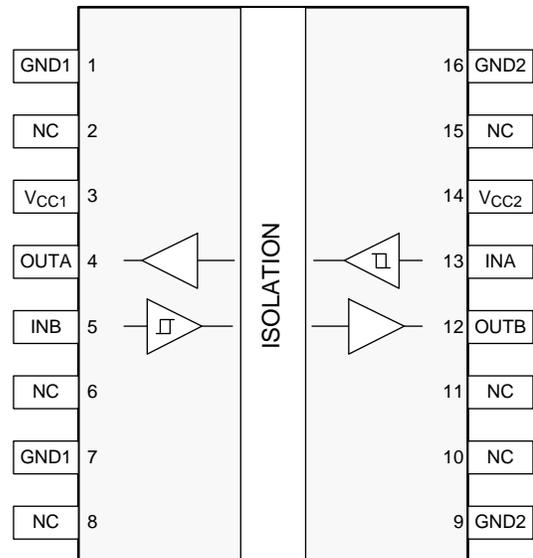
日期	修订版本	注释
2017 年 3 月	*	首次发布。

5 Pin Configuration and Functions

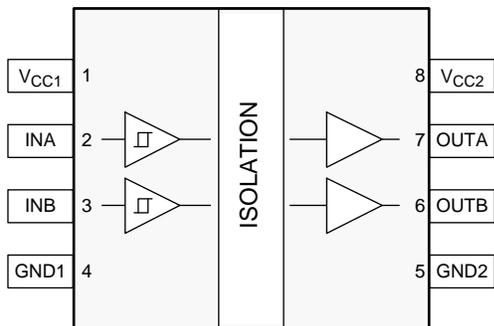
ISO7720-Q1 DW Package
16-Pin SOIC
Top View



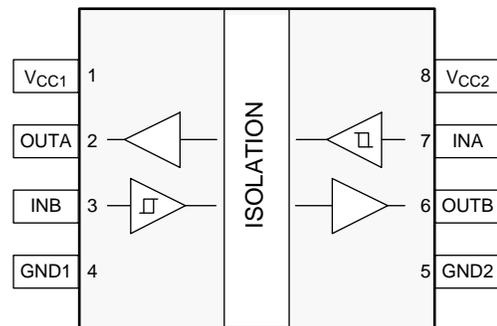
ISO7721-Q1 DW Package
16-Pin SOIC
Top View



ISO7720-Q1 D Package
8-Pin SOIC
Top View



ISO7721-Q1 D Package
8-Pin SOIC
Top View



Pin Functions

NAME	PIN				I/O	DESCRIPTION
	DW PACKAGE		D PACKAGE			
	ISO7720-Q1	ISO7721-Q1	ISO7720-Q1	ISO7721-Q1		
GND1	1, 7	1, 7	4	4	—	Ground connection for V_{CC1}
GND2	9	9	5	5	—	Ground connection for V_{CC2}
	16	16				
INA	4	13	2	7	I	Input, channel A
INB	5	5	3	3	I	Input, channel B
NC	2, 6, 8, 10, 11, 15	2, 6, 8, 10, 11, 15	—	—	—	Not connected
OUTA	13	4	7	2	O	Output, channel A
OUTB	12	12	6	6	O	Output, channel B
V_{CC1}	3	3	1	1	—	Power supply, V_{CC1}
V_{CC2}	14	14	8	8	—	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

 See ⁽¹⁾.

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage ⁽²⁾	-0.5	6	V
V	Voltage at INx, OUTx	-0.5	$V_{CC} + 0.5$ ⁽³⁾	V
I_O	Output current	-15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
- (3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±6000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising		2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling	1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis	100	200		mV
I_{OH}	High-level output current	$V_{CCO}^{(1)} = 5\text{ V}$		-4	mA
		$V_{CCO} = 3.3\text{ V}$		-2	
		$V_{CCO} = 2.5\text{ V}$		-1	
I_{OL}	Low-level output current	$V_{CCO} = 5\text{ V}$		4	mA
		$V_{CCO} = 3.3\text{ V}$		2	
		$V_{CCO} = 2.5\text{ V}$		1	
V_{IH}	High-level input voltage	$0.7 \times V_{CCI}^{(1)}$		V_{CCI}	V
V_{IL}	Low-level input voltage	0		$0.3 \times V_{CCI}$	V
DR	Signaling rate	0		100	Mbps
T_A	Ambient temperature	-40	25	125	°C

- (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISO772x-Q1		UNIT
		DW (SOIC)	D (SOIC)	
		16 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.5	137.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	49.6	54.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	71.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.3	7.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	49.2	70.7	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7720-Q1						
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50 MHz 50% duty cycle square wave			100	mW
P_{D1}	Maximum power dissipation by side-1	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50 MHz 50% duty cycle square wave			20	mW
P_{D2}	Maximum power dissipation by side-2	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50 MHz 50% duty cycle square wave			80	mW
ISO7721-Q1						
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50 MHz 50% duty cycle square wave			100	mW
P_{D1}	Maximum power dissipation by side-1	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50 MHz 50% duty cycle square wave			50	mW
P_{D2}	Maximum power dissipation by side-2	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50 MHz 50% duty cycle square wave			50	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE		UNIT
			DW-16	D-8	
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	8	4	mm
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	8	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V _{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 300 V _{RMS}	I-IV	I-III	
		Rated mains voltage ≤ 600 V _{RMS}	I-IV	n/a	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	n/a	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12⁽²⁾					
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	637	V _{PK}
V _{IOVM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) test	1000	450	V _{RMS}
		DC voltage	1414	637	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); t = 1 s (100% production)	8000	4242	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 60065, 1.2/50 μs waveform, V _{TEST} = 1.6 × V _{IOSM} (qualification)	8000	5000	V _{PK}
q _{pd}	Apparent charge ⁽⁴⁾	Method a, After Input/Output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤5	≤5	
		Method b1; At routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s	≤5	≤5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.4 × sin(2πft), f = 1 MHz	~0.5	~0.5	pF
R _{IO}	Isolation resistance ⁽⁵⁾	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	>10 ⁹	
	Pollution degree		2	2	
	Climatic category		55/125/21	5/125/21	
UL 1577					
V _{ISO}	Withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s(qualification); V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production)	5000	3000	V _{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

DW package devices certified according to VDE, CSA, UL, and TUV; All other certifications are planned.

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Certified under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Maximum transient isolation voltage, 8000 V _{PK} (DW-16, Reinforced) and 4242 V _{PK} (D-8); Maximum repetitive peak isolation voltage, 1414 V _{PK} (DW-16, Reinforced) and 637 V _{PK} (D-8); Maximum surge isolation voltage, 8000 V _{PK} (DW-16, Reinforced) and 5000 V _{PK} (D-8)	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V _{RMS} (DW-16) and 400 V _{RMS} (D-8) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V _{RMS} (DW-16) max working voltage	DW-16: Single protection, 5000 V _{RMS} ; D-8: Single protection, 3000 V _{RMS}	DW-16: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V _{RMS} maximum working voltage; D-8: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V _{RMS} maximum working voltage	5000 V _{RMS} (DW-16) and 3000 V _{RMS} (D-8) Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V _{RMS} (DW-16) and 300 V _{RMS} (D-8) 5000 V _{RMS} (DW-16) and 3000 V _{RMS} (D-8) Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 V _{RMS} (DW-16) and 400 V _{RMS} (D-8)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certification planned	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I _S	Safety input, output, or supply current	R _{θJA} = 86.5 °C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 1			263	mA
		R _{θJA} = 86.5 °C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 1			401	
		R _{θJA} = 86.5 °C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C, see Figure 1			525	
P _S	Safety input, output, or total power	R _{θJA} = 86.5 °C/W, T _J = 150°C, T _A = 25°C, see Figure 2			1445	mW
T _S	Maximum safety temperature				150	°C
D-8 PACKAGE						
I _S	Safety input, output, or supply current	R _{θJA} = 137.7 °C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 3			165	mA
		R _{θJA} = 137.7 °C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 3			252	
		R _{θJA} = 137.7 °C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C, see Figure 3			330	
P _S	Safety input, output, or total power	R _{θJA} = 137.7 °C/W, T _J = 150°C, T _A = 25°C, see Figure 4			908	mW
T _S	Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage $I_{OH} = -4\text{ mA}$; see Figure 13	$V_{CCO}^{(1)} - 0.4$	4.8		V
V_{OL}	Low-level output voltage $I_{OL} = 4\text{ mA}$; see Figure 13		0.2	0.4	V
$V_{IT+(IN)}$	Rising input threshold voltage		$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input threshold voltage	$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current $V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
I_{IL}	Low-level input current $V_{IL} = 0\text{ V}$ at INx	-10			μA
CMTI	Common-mode transient immunity $V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200\text{ V}$; see Figure 15	85	100		$\text{kV}/\mu\text{s}$
C_I	Input Capacitance ⁽²⁾ $V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{CC} = 5\text{ V}$		2		pF

 (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

(2) Measured from input pin to ground.

6.10 Supply Current Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO7720-Q1							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7720-Q1), $V_I = 0\text{ V}$ (ISO7720-Q1 with F suffix)	I_{CC1}		0.8	1.1	mA	
		I_{CC2}		1.1	1.7		
	$V_I = 0\text{ V}$ (ISO7720-Q1), $V_I = V_{CCI}$ (ISO7720-Q1 with F suffix)	I_{CC1}		2.9	4.2		
		I_{CC2}		1.2	1.9		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		1.8		2.7
			I_{CC2}		1.3		1.9
		10 Mbps	I_{CC1}		1.9		2.7
			I_{CC2}		2.2		3
		100 Mbps	I_{CC1}		2.5	3.2	
			I_{CC2}		11.6	14	
ISO7721-Q1							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7721-Q1), $V_I = 0\text{ V}$ (ISO7721-Q1 with F suffix)	I_{CC1}, I_{CC2}		1	1.6	mA	
		I_{CC1}, I_{CC2}		2.2	3.2		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		1.7		2.4
		10 Mbps	I_{CC1}, I_{CC2}		2.2		3
		100 Mbps	I_{CC1}, I_{CC2}		7.3		9

6.11 Electrical Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2 \text{ mA}$; see Figure 13	$V_{CCO}^{(1)} - 0.3$	3.2		V
V_{OL}	Low-level output voltage	$I_{OL} = 2 \text{ mA}$; see Figure 13		0.1	0.3	V
$V_{IT+(IN)}$	Rising input voltage threshold			$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input voltage threshold		$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0 \text{ V}$ at INx	-10			μA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200 \text{ V}$; see Figure 15	85	100		$\text{kV}/\mu\text{s}$

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

6.12 Supply Current Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7720-Q1						
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7720-Q1), $V_I = 0 \text{ V}$ (ISO7720-Q1 with F suffix)	I_{CC1}		0.8	1.1	mA
		I_{CC2}		1.1	1.7	
	$V_I = 0 \text{ V}$ (ISO7720-Q1), $V_I = V_{CCI}$ (ISO7720-Q1 with F suffix)	I_{CC1}		2.9	4.2	
		I_{CC2}		1.2	1.9	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	1 Mbps	I_{CC1}		1.8	2.7
			I_{CC2}		1.2	1.9
		10 Mbps	I_{CC1}		1.9	2.7
			I_{CC2}		1.9	2.6
		100 Mbps	I_{CC1}		2.2	3.1
			I_{CC2}		8.6	11
ISO7721-Q1						
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7721-Q1), $V_I = 0 \text{ V}$ (ISO7721-Q1 with F suffix)	I_{CC1}, I_{CC2}		1	1.6	mA
		I_{CC1}, I_{CC2}		2.2	3.2	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		1.6	2.4
		10 Mbps	I_{CC1}, I_{CC2}		2	2.8
		100 Mbps	I_{CC1}, I_{CC2}		5.6	7

6.13 Electrical Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage $I_{OH} = -1\text{ mA}$; see Figure 13	$V_{CCO}^{(1)} - 0.2$	2.45		V
V_{OL}	Low-level output voltage $I_{OL} = 1\text{ mA}$; see Figure 13		0.05	0.2	V
$V_{IT+(IN)}$	Rising input voltage threshold		$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input voltage threshold	$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current $V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
I_{IL}	Low-level input current $V_{IL} = 0\text{ V}$ at INx	-10			μA
CMTI	Common-mode transient immunity $V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200\text{ V}$; see Figure 15	85	100		$\text{kV}/\mu\text{s}$

 (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

6.14 Supply Current Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO7720-Q1							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7720-Q1), $V_I = 0\text{ V}$ (ISO7720-Q1 with F suffix)	I_{CC1}		0.8	1.1	mA	
		I_{CC2}		1.1	1.7		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		1.8		2.7
			I_{CC2}		1.3		1.9
		10 Mbps	I_{CC1}		1.9		2.7
			I_{CC2}		1.7		2.4
		100 Mbps	I_{CC1}		2.2	3	
			I_{CC2}		6.8	9	
ISO7721-Q1							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7721-Q1), $V_I = 0\text{ V}$ (ISO7721-Q1 with F suffix)	I_{CC1}, I_{CC2}		1	1.6	mA	
		I_{CC1}, I_{CC2}		2.2	3.2		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		1.6		2.4
		10 Mbps	I_{CC1}, I_{CC2}		1.9		2.7
		100 Mbps	I_{CC1}, I_{CC2}		4.6		6

6.15 Switching Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL} Propagation delay time	See Figure 13	6	11	16	ns
PWD Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			0.5	4.9	ns
$t_{sk(o)}$ Channel-to-channel output skew time ⁽²⁾	Same direction channels			4	ns
$t_{sk(pp)}$ Part-to-part skew time ⁽³⁾				4.5	ns
t_r Output signal rise time	See Figure 13		1.8	3.9	ns
t_f Output signal fall time				1.9	3.9
t_{DO} Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 14		0.1	0.3	μ s
t_{ie} Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL} Propagation delay time	See Figure 13	6	11	16	ns
PWD Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				0.5	5
$t_{sk(o)}$ Channel-to-channel output skew time ⁽²⁾	Same direction channels			4.1	ns
$t_{sk(pp)}$ Part-to-part skew time ⁽³⁾				4.5	ns
t_r Output signal rise time	See Figure 13		0.7	3	ns
t_f Output signal fall time				0.7	3
t_{DO} Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 14		0.1	0.3	μ s
t_{ie} Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

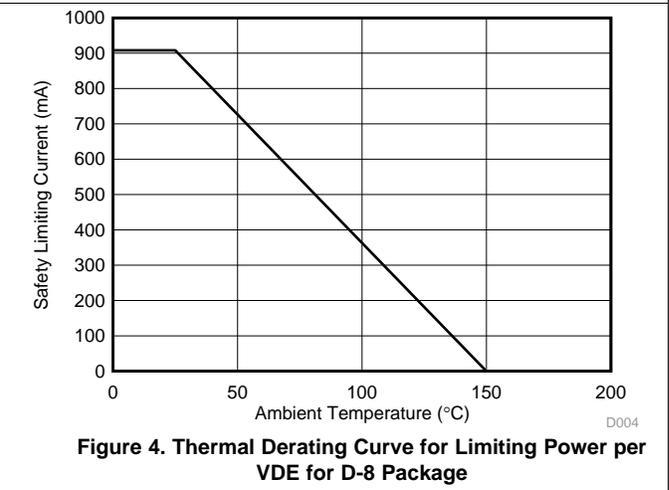
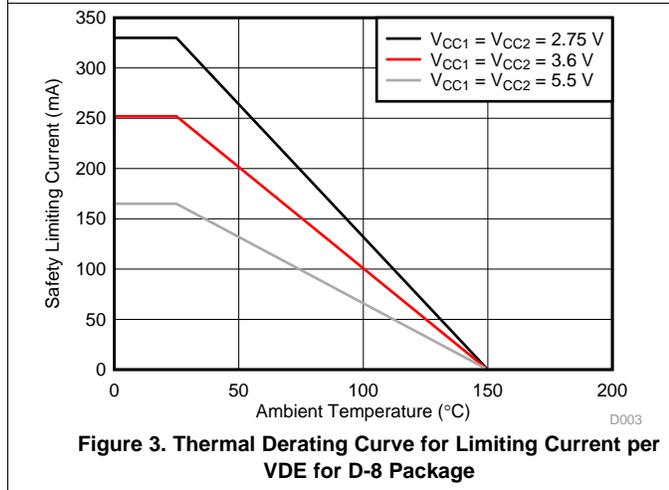
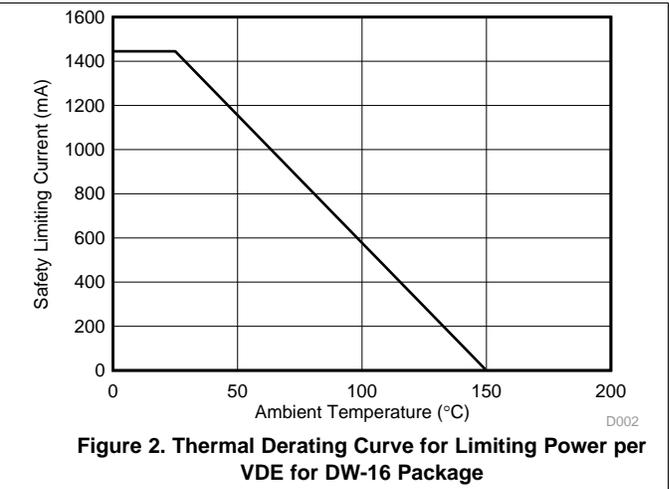
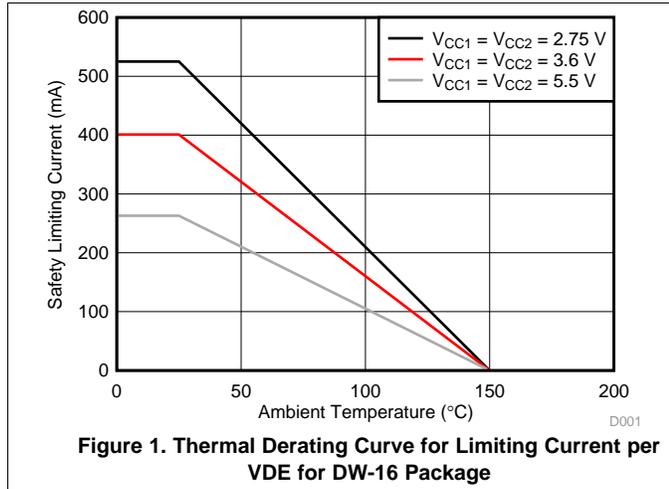
6.17 Switching Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL} Propagation delay time	See Figure 13	7.5	12	18.5	ns
PWD Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				0.5	5.1
$t_{sk(o)}$ Channel-to-channel output skew time ⁽²⁾	Same direction channels			4.1	ns
$t_{sk(pp)}$ Part-to-part skew time ⁽³⁾				4.6	ns
t_r Output signal rise time	See Figure 13		1	3.5	ns
t_f Output signal fall time				1	3.5
t_{DO} Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 14		0.1	0.3	μ s
t_{ie} Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Insulation Characteristics Curves



6.19 Typical Characteristics

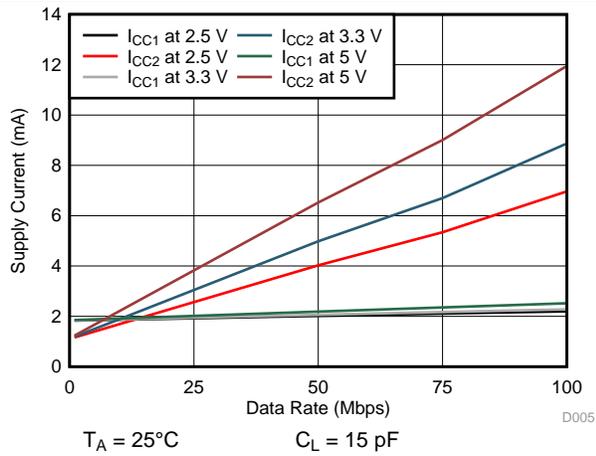


Figure 5. ISO7720-Q1 Supply Current vs Data Rate (With 15-pF Load)

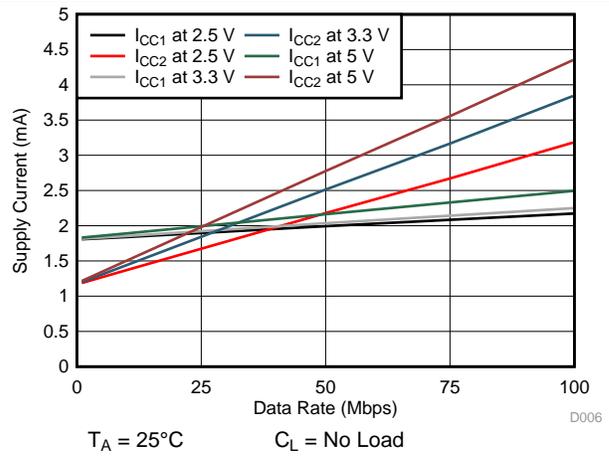


Figure 6. ISO7720-Q1 Supply Current vs Data Rate (With No Load)

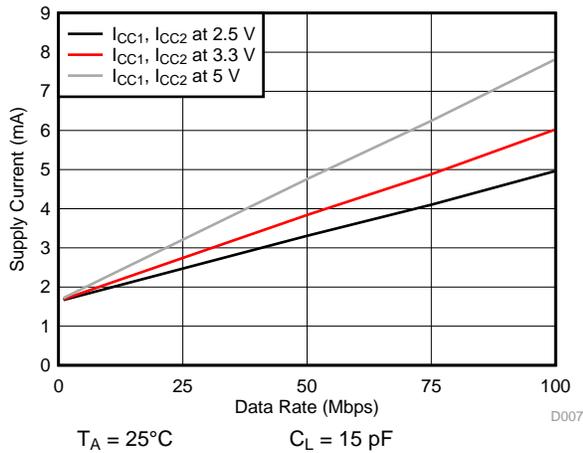


Figure 7. ISO7721-Q1 Supply Current vs Data Rate (With 15-pF Load)

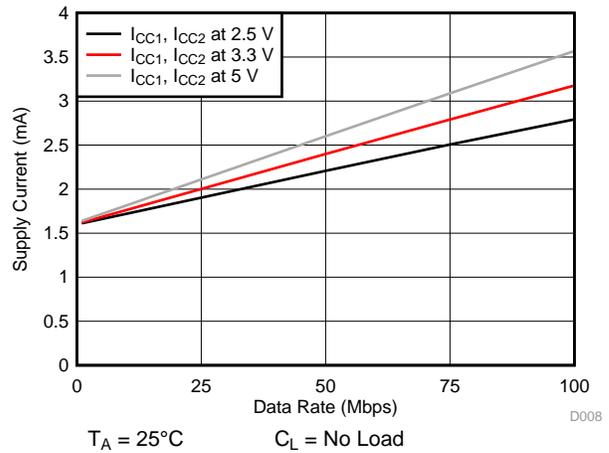


Figure 8. ISO7721-Q1 Supply Current vs Data Rate (With No Load)

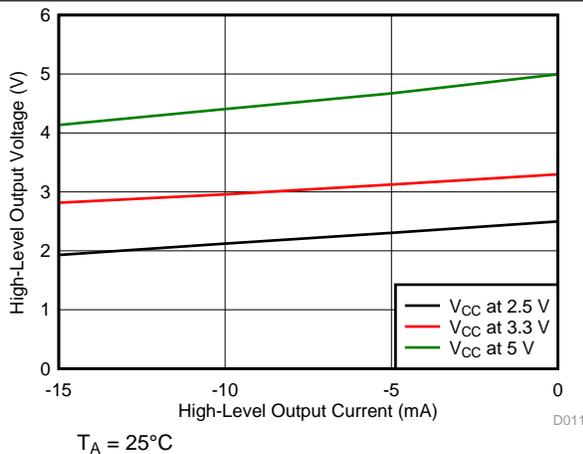


Figure 9. High-Level Output Voltage vs High-level Output Current

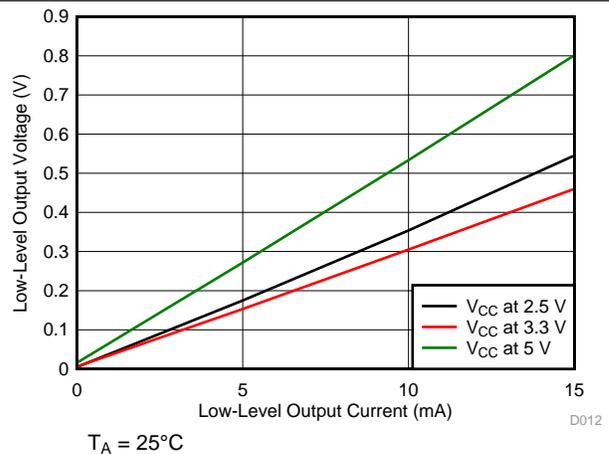
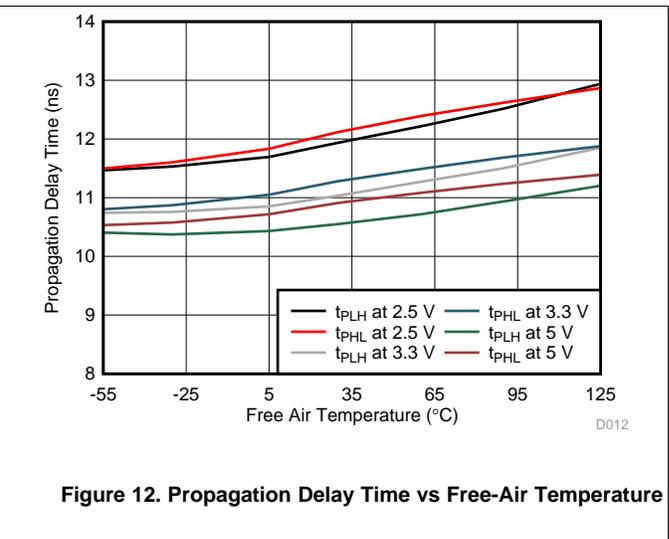
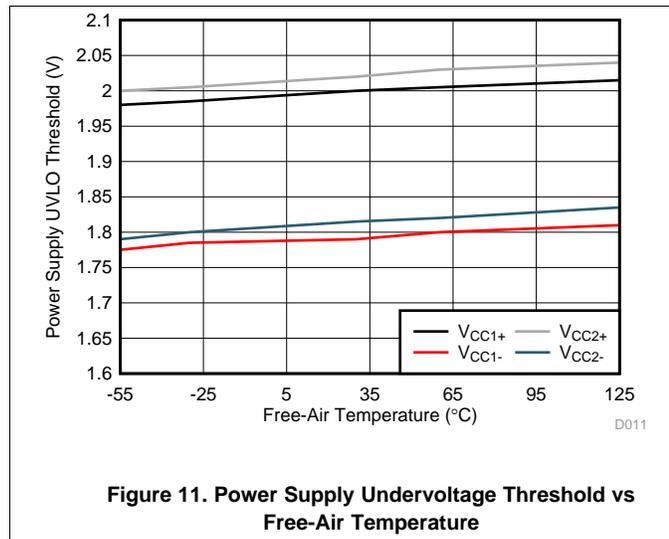
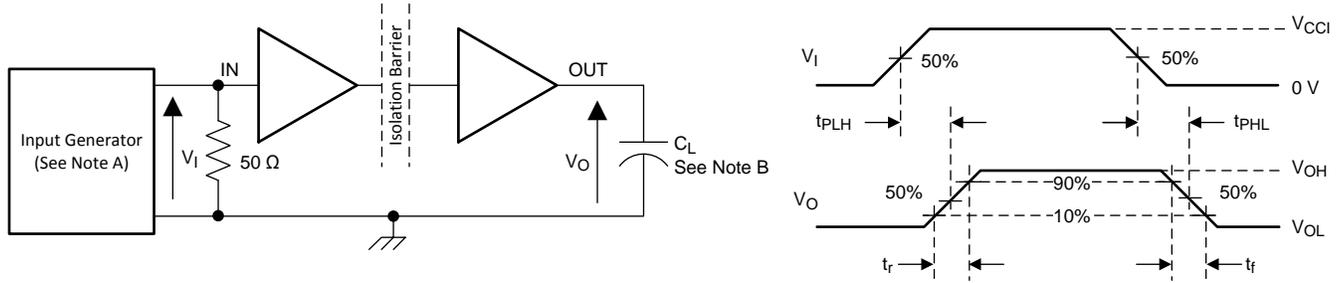


Figure 10. Low-Level Output Voltage vs Low-Level Output Current

Typical Characteristics (continued)

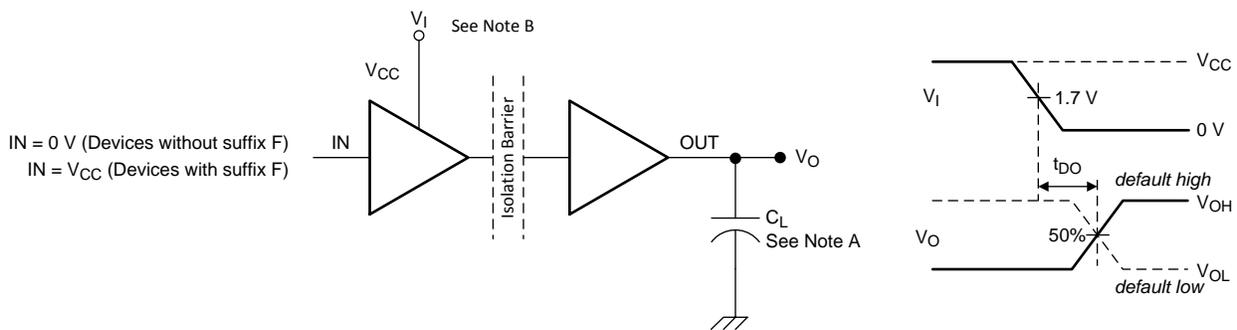


7 Parameter Measurement Information



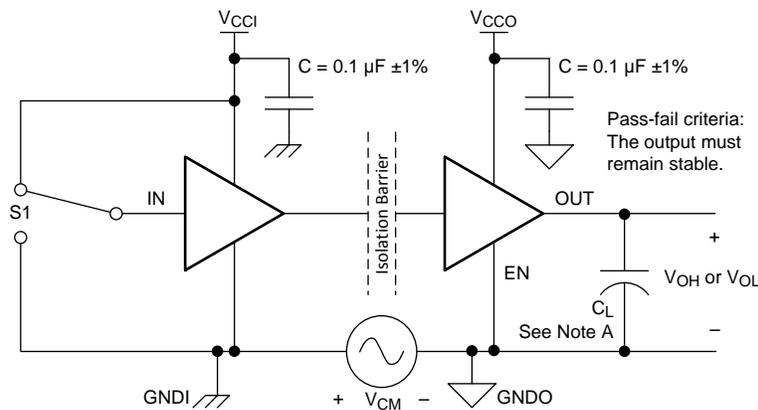
- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. Switching Characteristics Test Circuit and Voltage Waveforms



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within ±20%.
- B. Power Supply Ramp Rate = 10 mV/ns

Figure 14. Default Output Delay Time Test Circuit and Voltage Waveforms



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within ±20%.

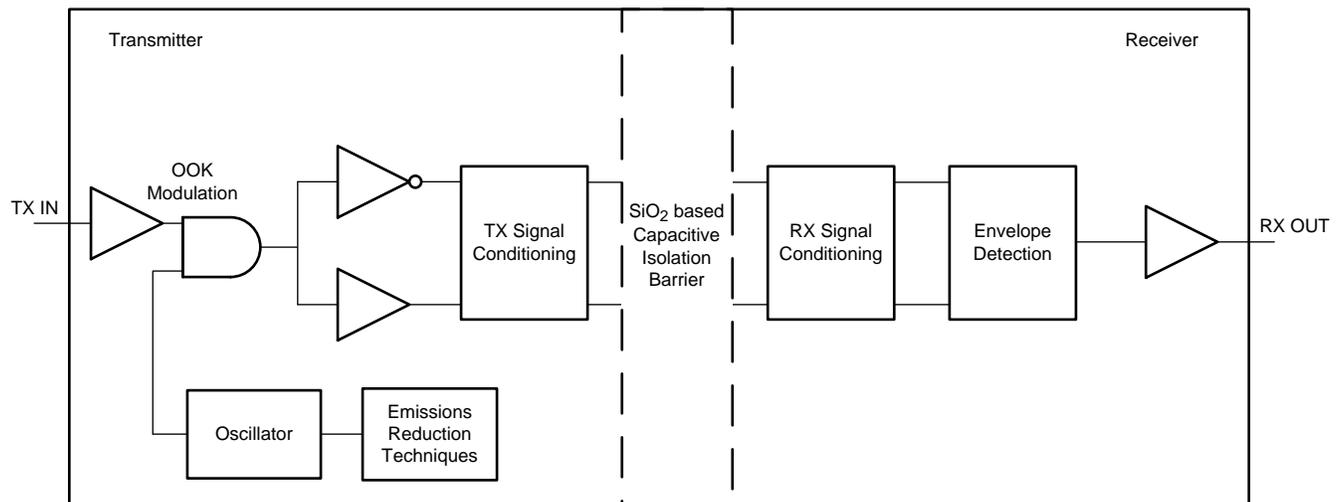
Figure 15. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO772x-Q1 family of devices has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Figure 16](#), shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram



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Figure 16. Conceptual Block Diagram of a Digital Capacitive Isolator

[Figure 17](#) shows a conceptual detail of how the OOK scheme works.

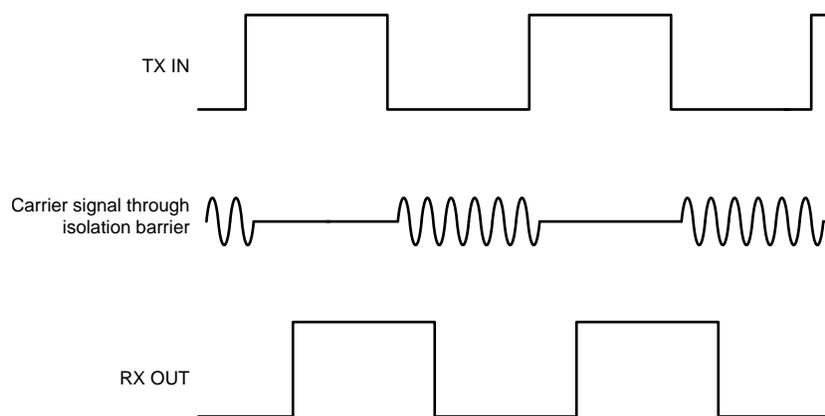


Figure 17. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

The ISO772x-Q1 family of devices is available in two channel configurations and default output state options to enable a variety of application uses. [Table 1](#) lists the device features of the ISO772x-Q1 devices.

Table 1. Device Features

PART NUMBER	MAXIMUM DATA RATE	CHANNEL DIRECTION	DEFAULT OUTPUT STATE	PACKAGE	RATED ISOLATION ⁽¹⁾
ISO7720-Q1	100 Mbps	2 Forward, 0 Reverse	High	DW-16	5000 V _{RMS} / 8000 V _{PK}
				D-8	3000 V _{RMS} / 4242 V _{PK}
ISO7720-Q1 with F suffix	100 Mbps	2 Forward, 0 Reverse	Low	DW-16	5000 V _{RMS} / 8000 V _{PK}
				D-8	3000 V _{RMS} / 4242 V _{PK}
ISO7721-Q1	100 Mbps	1 Forward, 1 Reverse	High	DW-16	5000 V _{RMS} / 8000 V _{PK}
				D-8	3000 V _{RMS} / 4242 V _{PK}
ISO7721-Q1 with F suffix	100 Mbps	1 Forward, 1 Reverse	Low	DW-16	5000 V _{RMS} / 8000 V _{PK}
				D-8	3000 V _{RMS} / 4242 V _{PK}

(1) See the [Safety-Related Certifications](#) section for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO772x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

8.4 Device Functional Modes

Table 2 lists the functional modes for the ISO772x-Q1 devices.

Table 2. Function Table⁽¹⁾

V _{CCI}	V _{CCO}	INPUT (IN _x) ⁽²⁾	OUTPUT (OUT _x)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When IN _x is open, the corresponding channel output goes to the default high logic state. The default is <i>High</i> for ISO772x-Q1 and <i>Low</i> for ISO772x-Q1 with F suffix.
PD	PU	X	Default	Default mode: When V _{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. The default is <i>High</i> for ISO772x-Q1 and <i>Low</i> for ISO772x-Q1 with F suffix. When V _{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V _{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V _{CCO} is unpowered, a channel output is undetermined ⁽³⁾ . When V _{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

- (1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level
- (2) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.
- (3) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.

8.4.1 Device I/O Schematics

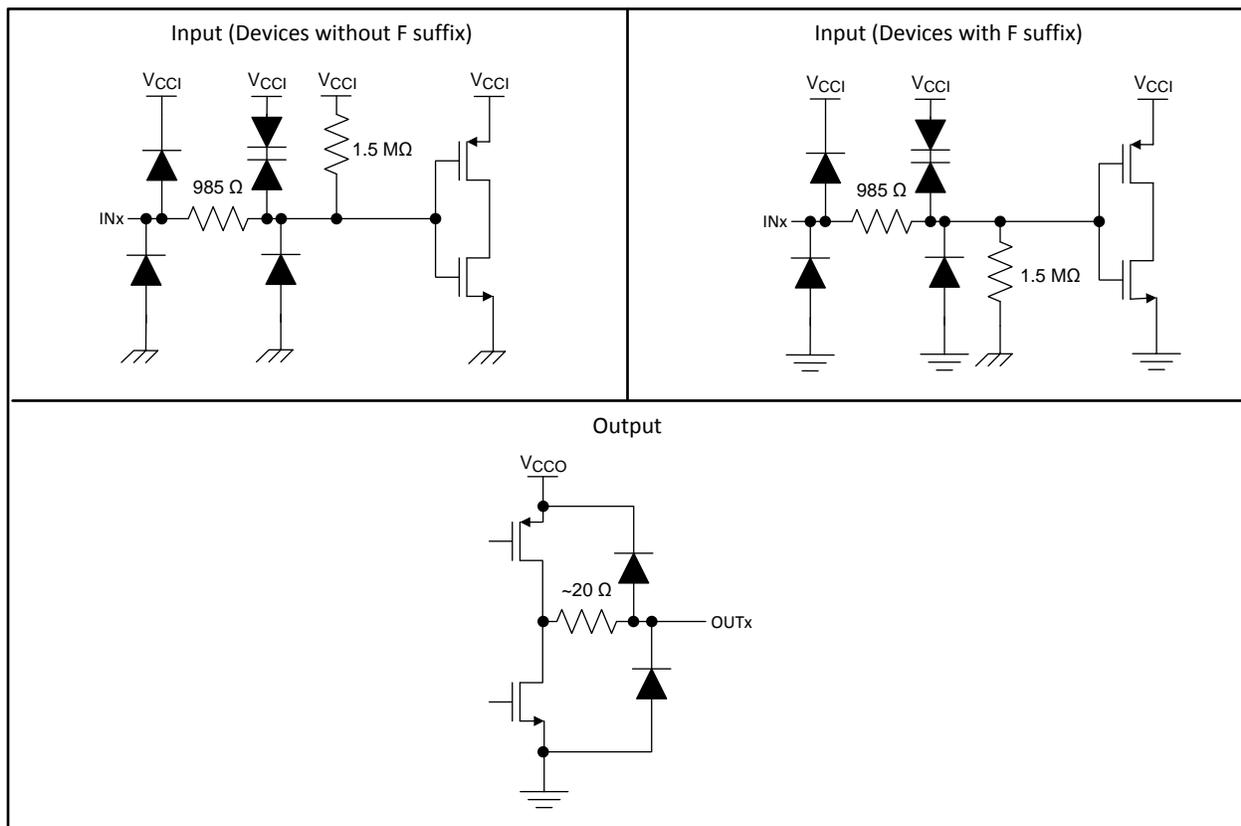


Figure 18. Device I/O Schematics

Typical Application (continued)

9.2.1 Design Requirements

To design with these devices, use the parameters listed in [Table 3](#).

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 μ F
Decoupling capacitor from V_{CC2} and GND2	0.1 μ F

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO772x-Q1 devices only require two external bypass capacitors to operate.

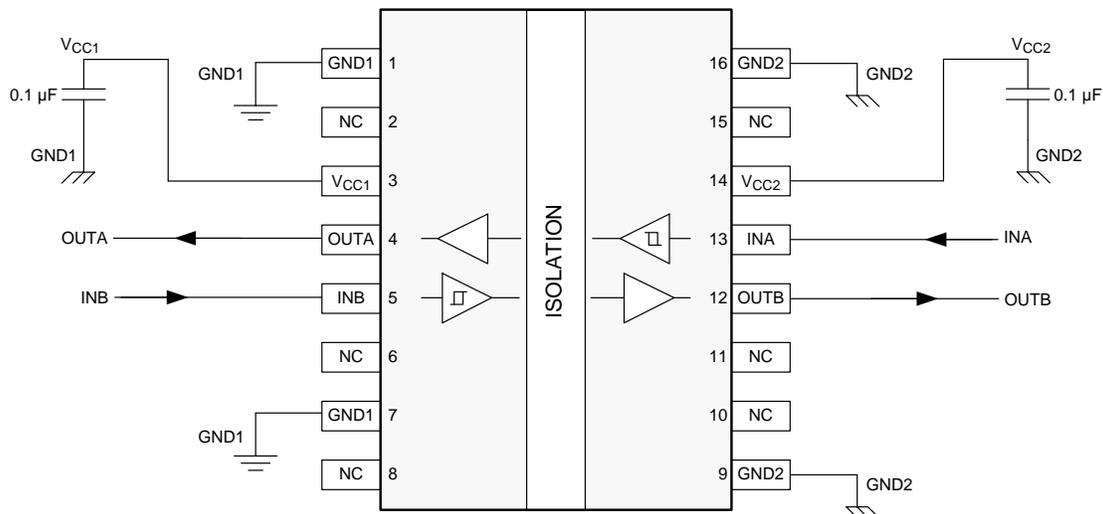
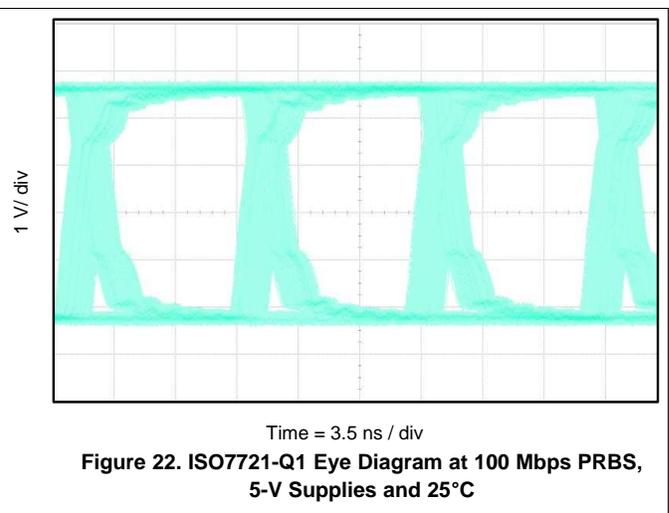
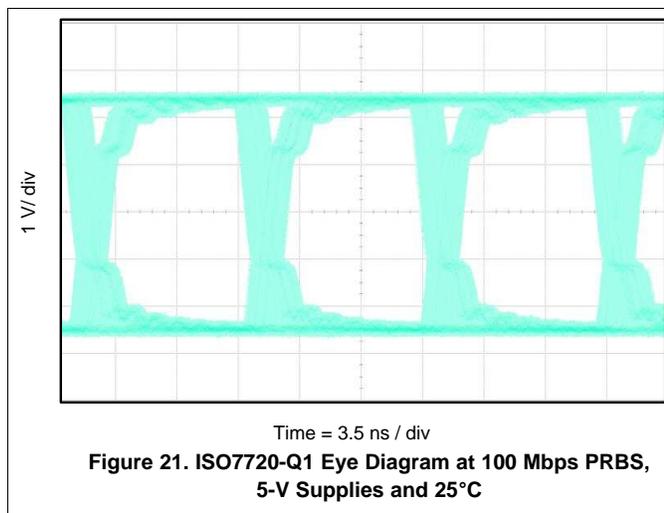


Figure 20. Typical ISO7721-Q1 Circuit Hook-up

9.2.3 Application Curve

The following typical eye diagrams of the ISO772x-Q1 family of devices indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.



10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1- μ F bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' [SN6501-Q1](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501-Q1 Transformer Driver for Isolated Power Supplies](#).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 23](#)). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

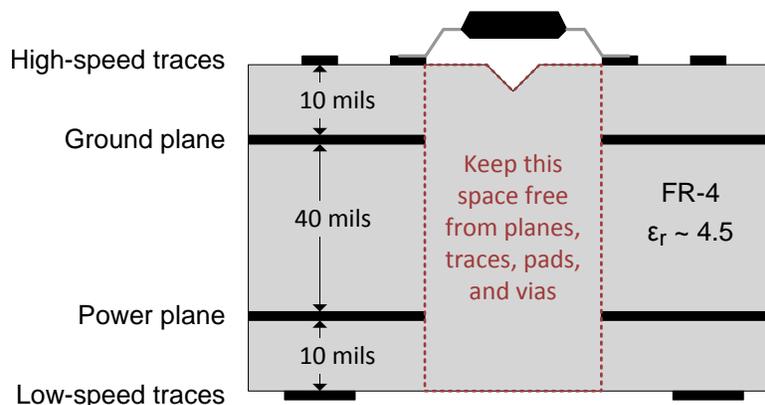


Figure 23. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- [数字隔离器设计指南](#)
- [隔离相关术语](#)
- [《用于隔离电源的 SN6501-Q1 变压器驱动器》](#)
- [《SN65HVD231Q 3.3V CAN 收发器》](#)
- [《TPS763xx-Q1 低功耗 150mA 低压降线性稳压器》](#)
- [《TMS320F2803x Piccolo™ 微控制器》](#)

12.2 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 4. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持与社区
ISO7720-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7721-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的**提醒我 (Alert me)** 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

Piccolo, E2E are trademarks of Texas Instruments.

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12.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

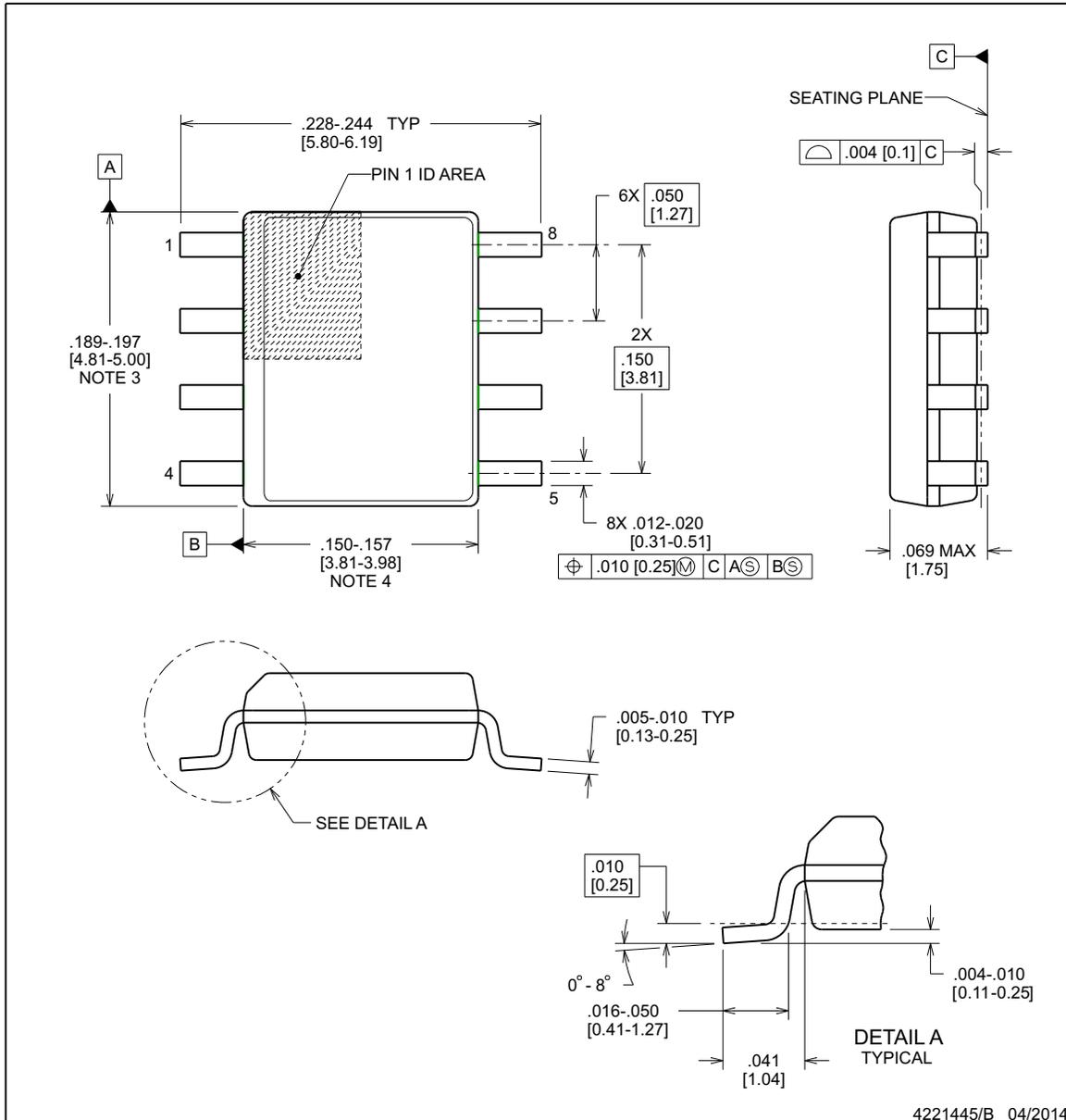
This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。


D0008B
PACKAGE OUTLINE
SOIC - 1.75 mm max height

SOIC


NOTES:

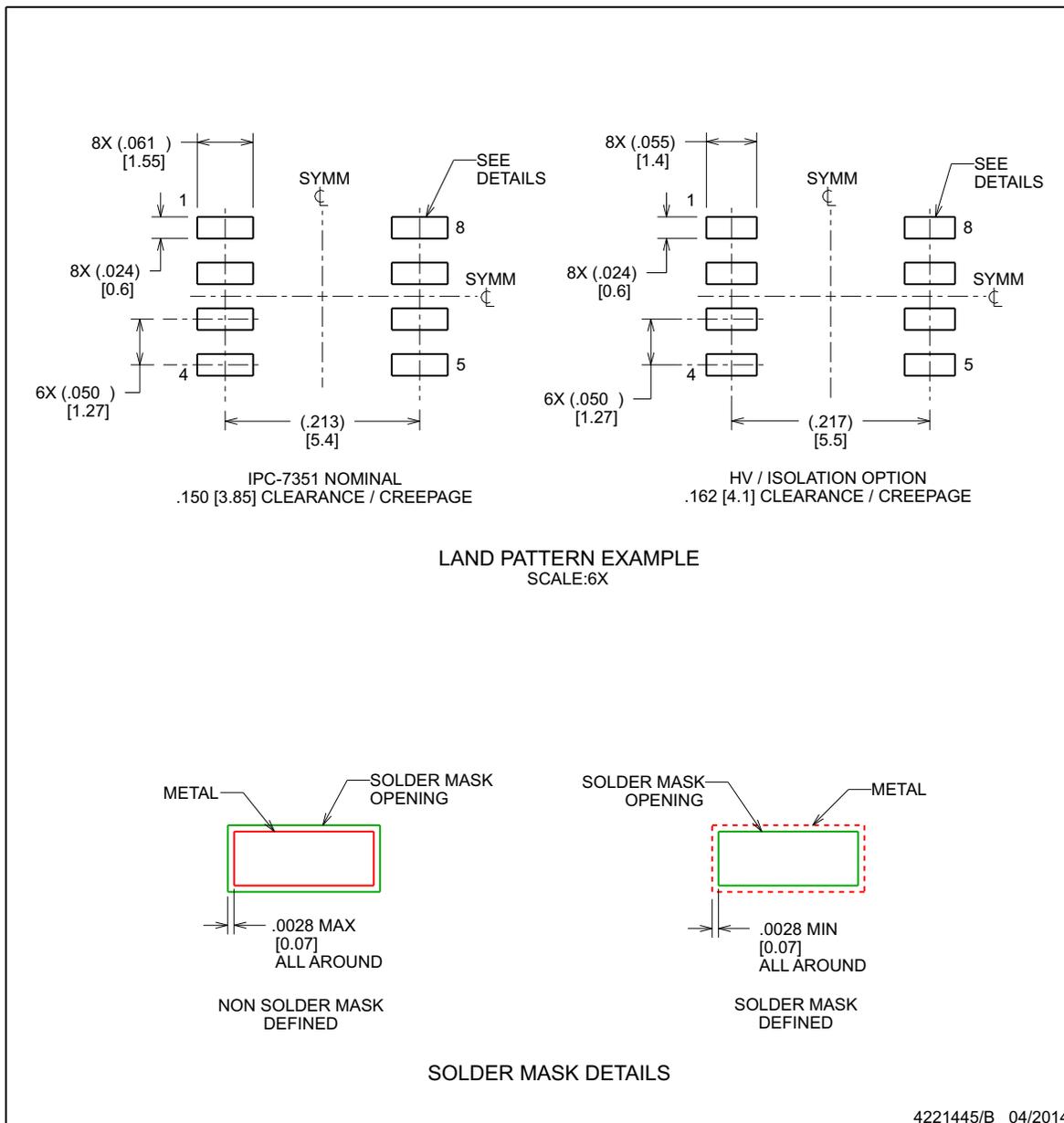
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15], per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

SOIC



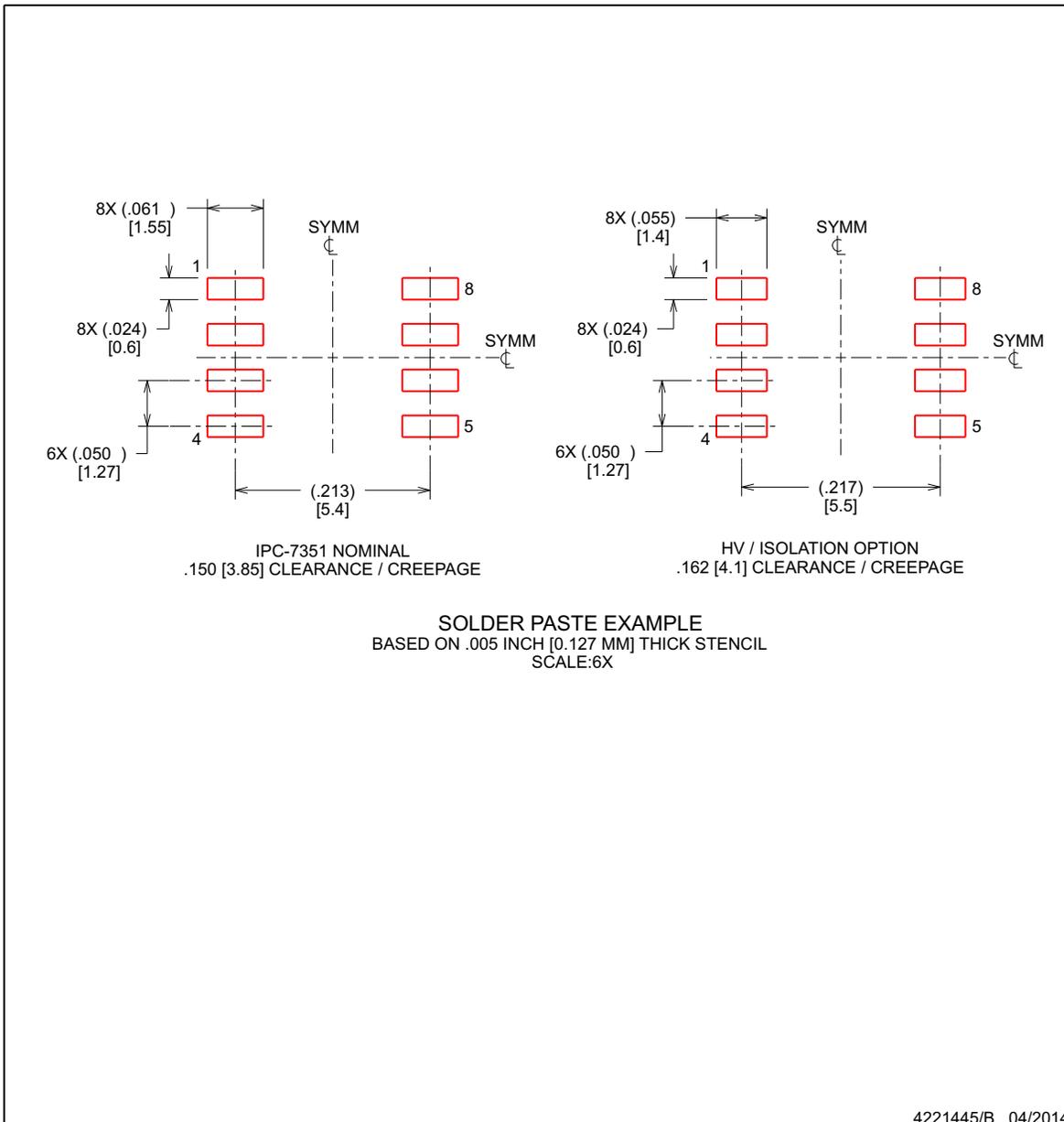
NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B
SOIC - 1.75 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

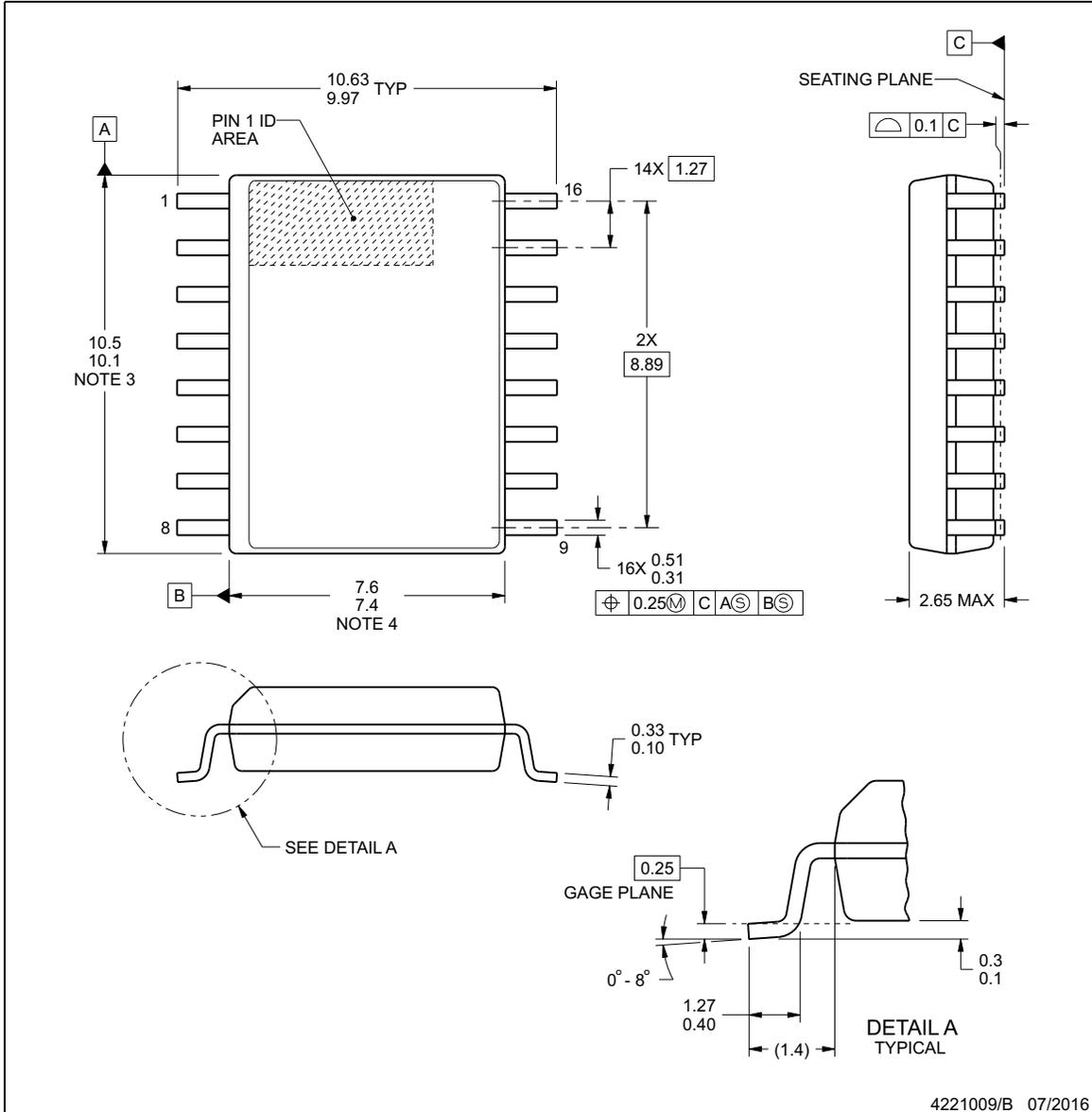


DW0016B

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

NOTES:

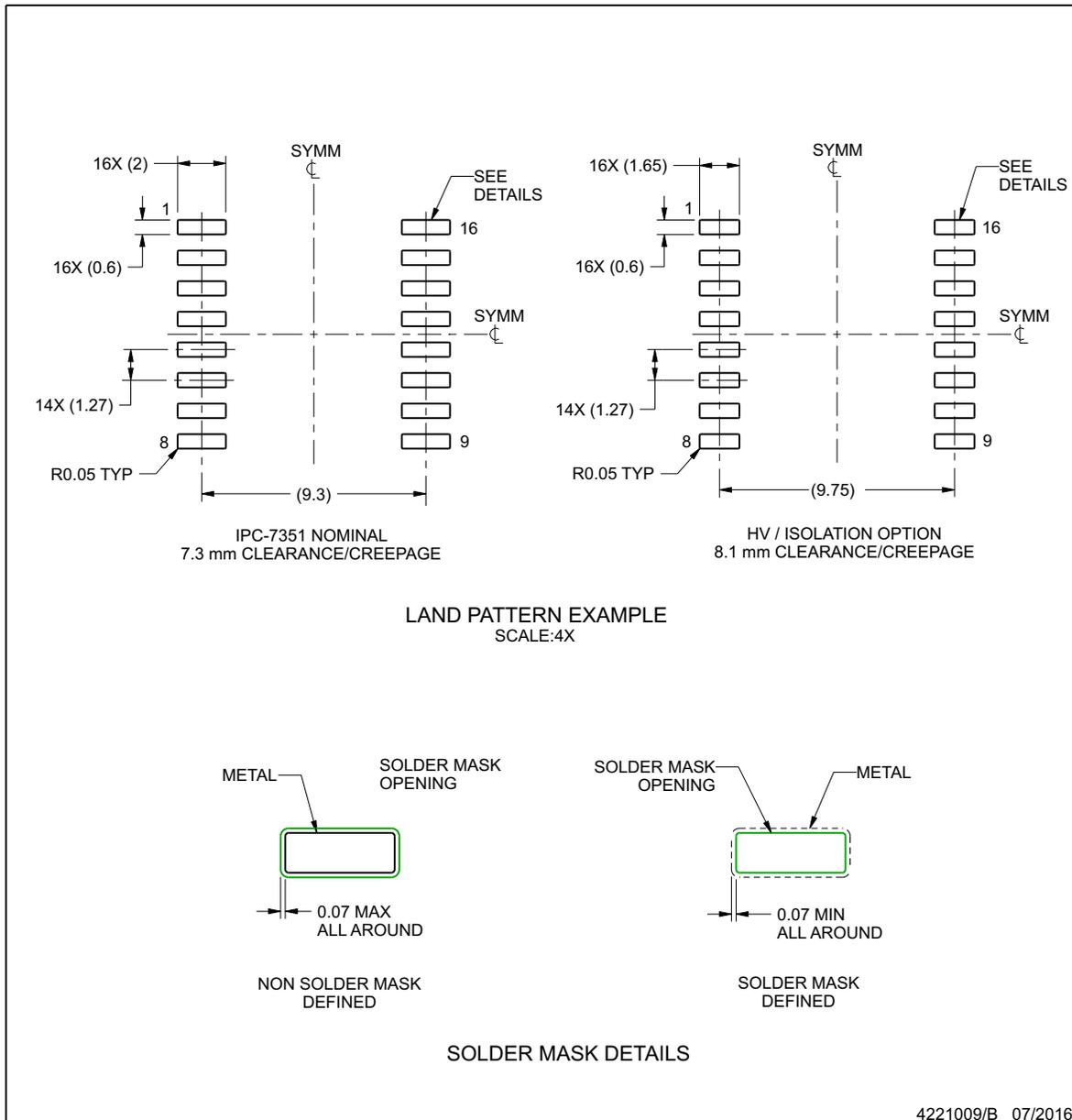
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

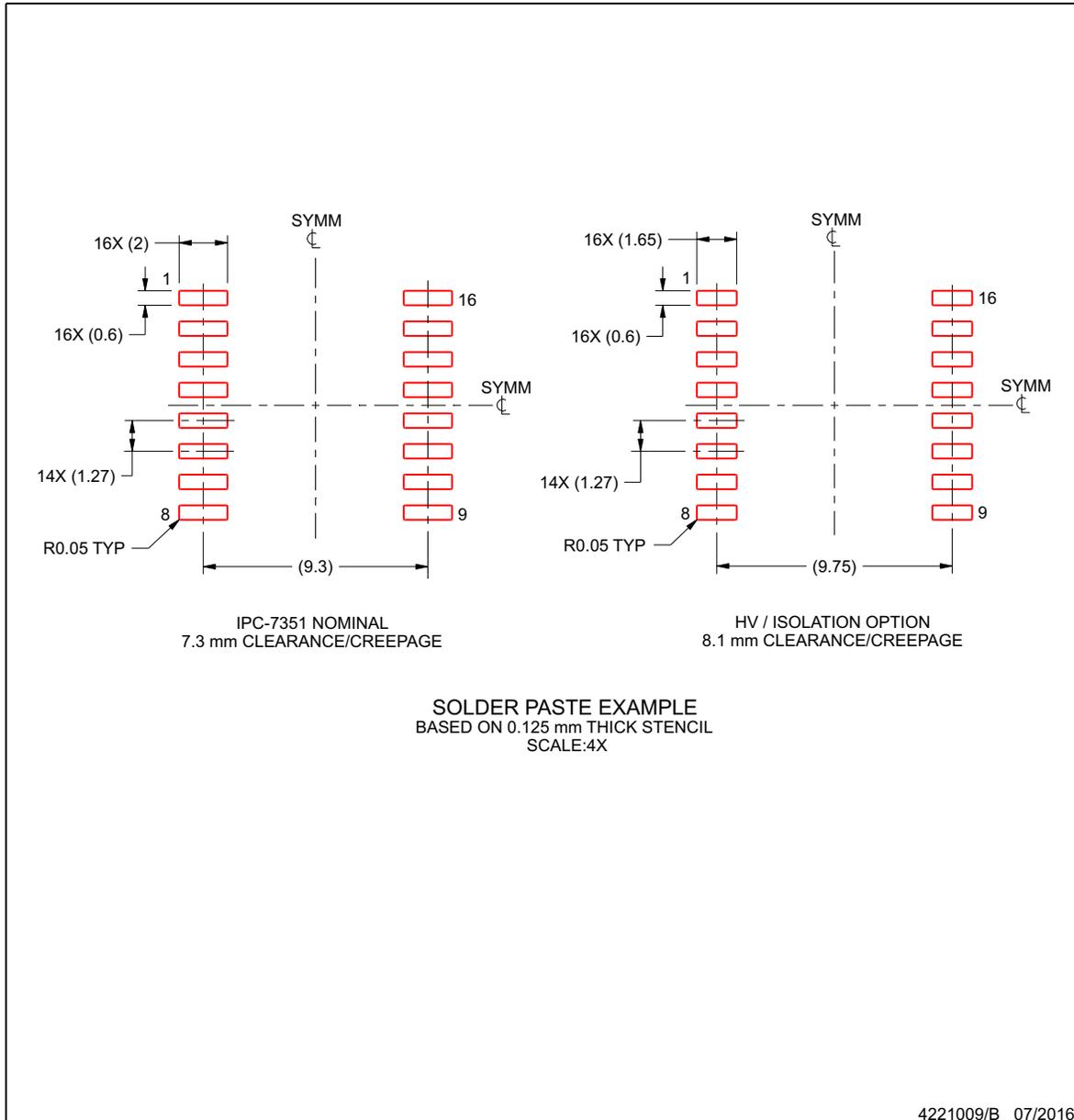
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7720FQDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7720FQ	Samples
ISO7720FQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7720FQ	Samples
ISO7720FQDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7720FQ	Samples
ISO7720FQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7720FQ	Samples
ISO7720QDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7720Q	Samples
ISO7720QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7720Q	Samples
ISO7720QDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7720Q	Samples
ISO7720QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7720Q	Samples
ISO7721FQDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7721FQ	Samples
ISO7721FQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7721FQ	Samples
ISO7721FQDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7721FQ	Samples
ISO7721FQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7721FQ	Samples
ISO7721QDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7721Q	Samples
ISO7721QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7721Q	Samples
ISO7721QDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7721Q	Samples
ISO7721QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7721Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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GENERIC PACKAGE VIEW

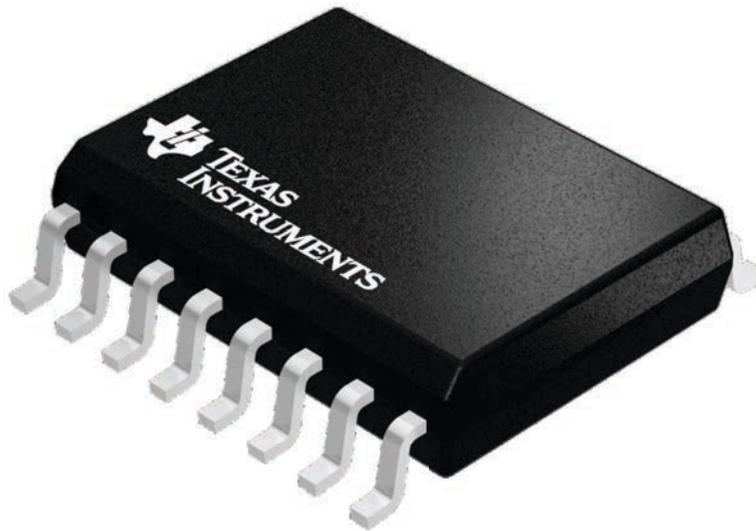
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



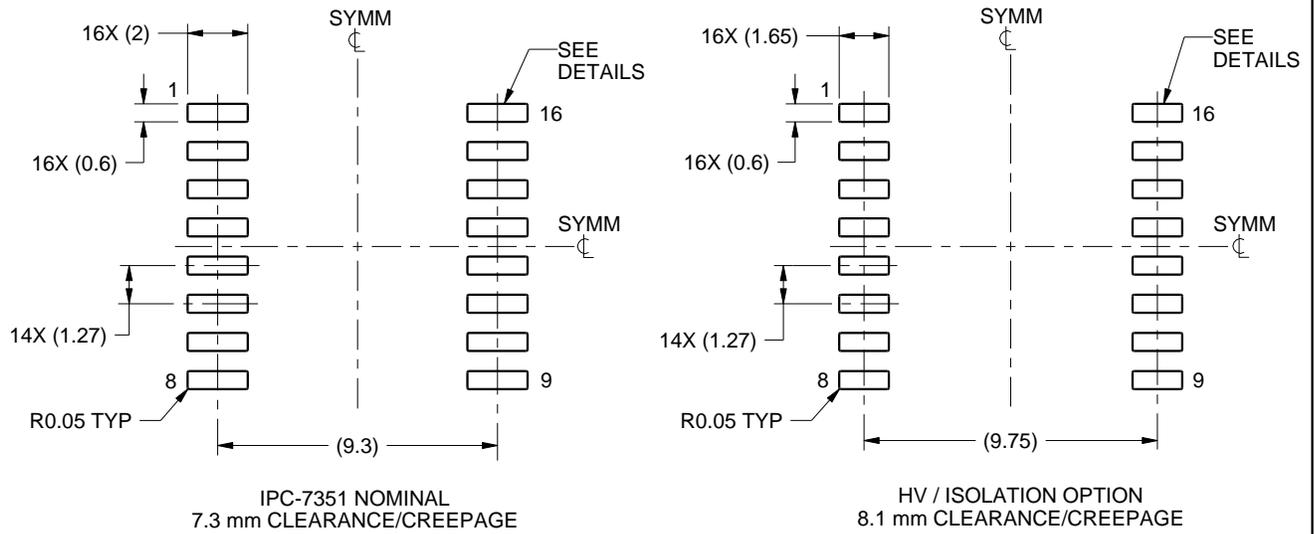
4224780/A

EXAMPLE BOARD LAYOUT

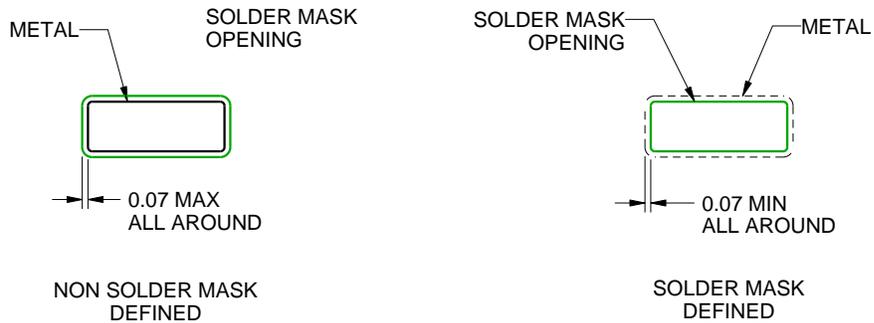
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

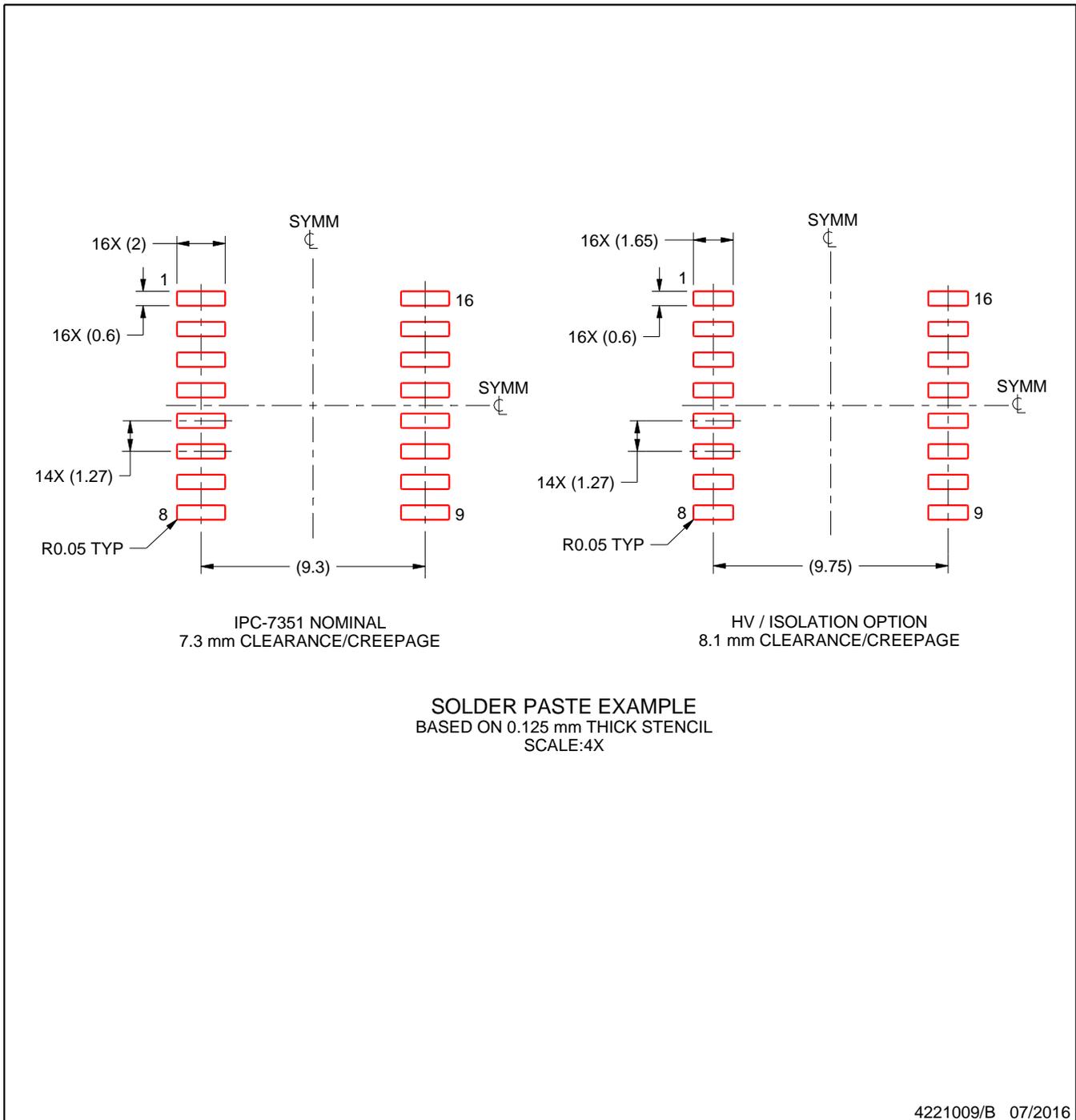
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

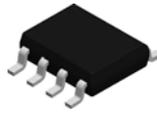
SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

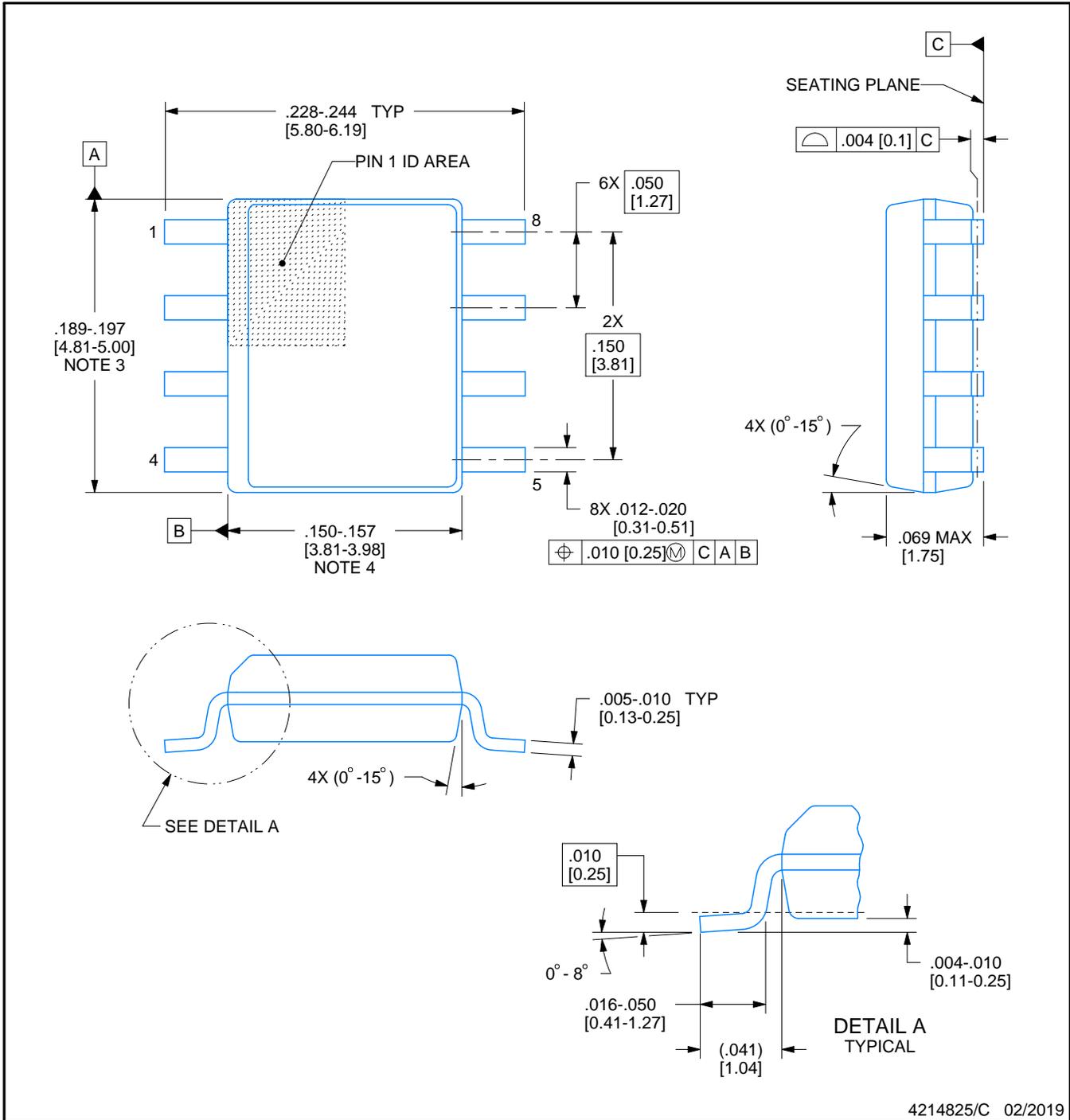


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

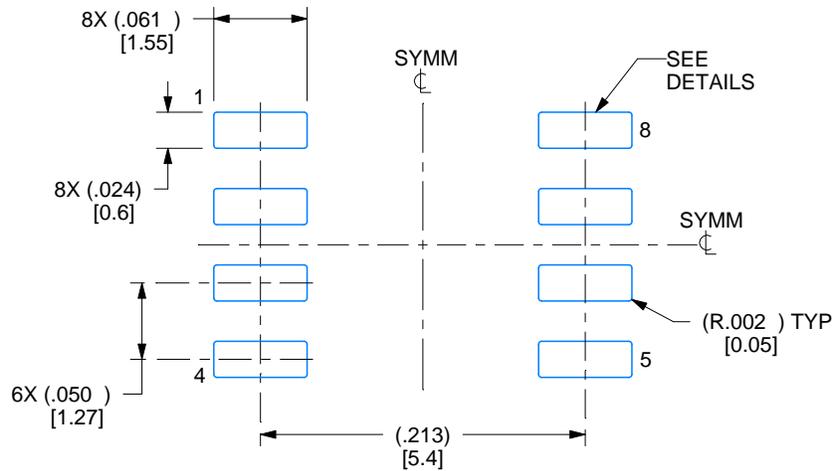
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

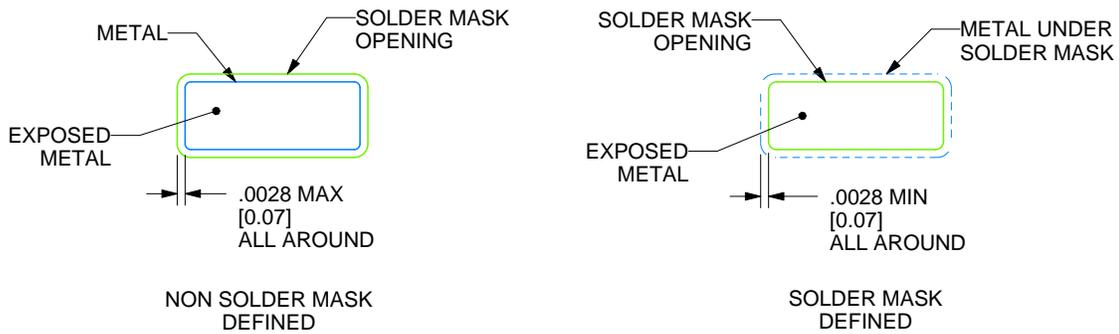
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

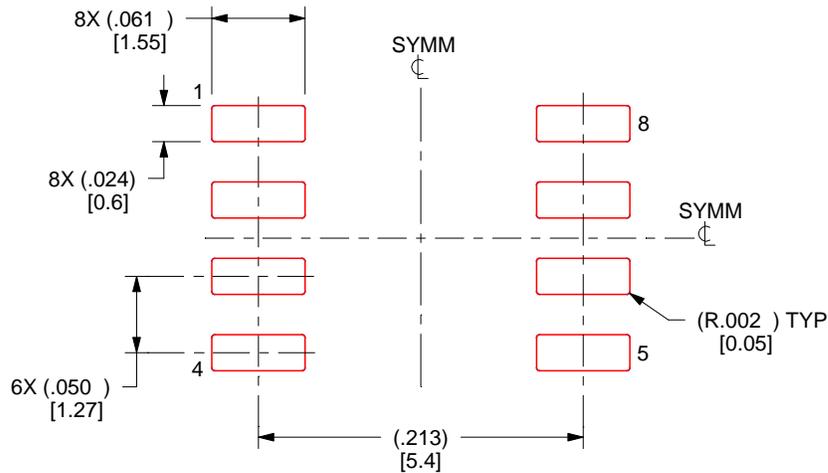
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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