ISO773x-Q1 EMC 性能优异的增强型高速三通道数字隔离器

1 特性

- 符合汽车类应用的 应用
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境运行温度范围
  - 器件 HBM ESD 分类等级 3A
  - 器件 CDM ESD 分类等级 C6
- 信号传输速率：高达 100Mbps
- 宽电源电压范围：2.25V 至 5.5V
- 2.25V 至 5.5V 电平转换
- 默认输出*高电平* 和*低电平* 选项
- 低功耗，电流典型值为 1.5mA/通道（1Mbps 时）
- 低传播延迟：典型值为 11ns（由 5V 电源供电）
- 高 CMTI：±100kV/μs（典型值）
- 优异的电磁兼容性 (EMC)
  - 系统级 ESD、EFT 和浪涌抗扰性
  - 低辐射
- 隔离栅寿命：> 40 年
- 宽体 SOIC (DW-16) 和 QSOP (DBQ-16) 封装选项
- 安全相关认证：
  - 符合 DIN V VDE V 0884-11:2017-01 标准的增强型绝缘
  - 符合 UL 1577 的 5000V_{RMS} (DW) 和 2500V_{RMS} (DBQ) 隔离额定值
  - CSA 组件验收通知 5A、IEC 60950-1 和 IEC 60601-1 终端设备标准
  - 符合 GB4943.1-2011 的 CQC 认证
  - 符合 EN 60950-1 和 EN 61010-1 的 TUV 认证
  - 除 DBQ-16 封装器件的 CQC 认证外，所有认证均已完成

2 应用

- 混合动力电动汽车
- 电机控制
- 电源
- 光伏逆变器
- 医疗设备

3 说明

ISO773x-Q1 器件是高性能三通道数字隔离器，可提供符合 UL 1577 的 5000V_{RMS}（DW 封装）和 3000V_{RMS}（DBQ 封装）隔离额定值。

该系列器件具有符合 VDE、CSA、TUV 和 CQC 标准的增强型隔离额定值。

在隔离 CMOS 或 LVCMOS 数字 I/O 时，ISO773x-Q1 系列器件可提供高电磁抗扰度和低辐射，并具备低功耗特性。每条隔离通道的逻辑输入和输出缓冲器均由二氧化硅 (SiO_2) 绝缘栅相隔离。该器件配有使能引脚，可用于将多主驱动 应用 中的相应输出置于高阻抗状态，也可用于降低功耗。ISO7730-Q1 器件具有三条全部同向的通道，而 ISO7731-Q1 器件具有两条正向通道和一条反向通道。如果输入功率或信号出现损失，不带后缀 F 的器件默认输出*高电平*，带后缀 F 的器件默认输出*低电平*。有关更多详细信息，请参阅 *Device Functional Modes*器件功能模式 部分。

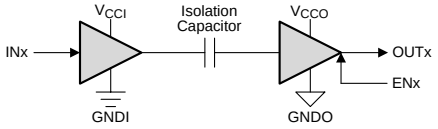
与隔离式电源结合使用时，该器件有助于防止数据总线或者其他电路中的噪声电流进入本地接地端，进而干扰或损坏敏感电路。凭借创新型芯片设计和布局技术，ISO773x-Q1 器件的电磁兼容性得到了显著增强，可轻松满足系统级 ESD、EFT、浪涌和辐射方面的合规性。ISO773x-Q1 系列器件采用 16 引脚宽体 SOIC 和 QSOP 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ISO7730-Q1 ISO7731-Q1	SOIC (DW)	10.30mm × 7.50mm
	SSOP (DBQ)	4.90mm × 3.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



V_{CCI} 和 GNDI 分别是输入通道的电源和接地连接引脚。

V_{CCO} 和 GNDO 分别是输出通道的电源和接地连接引脚。

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (May 2017) to Revision B **Page**

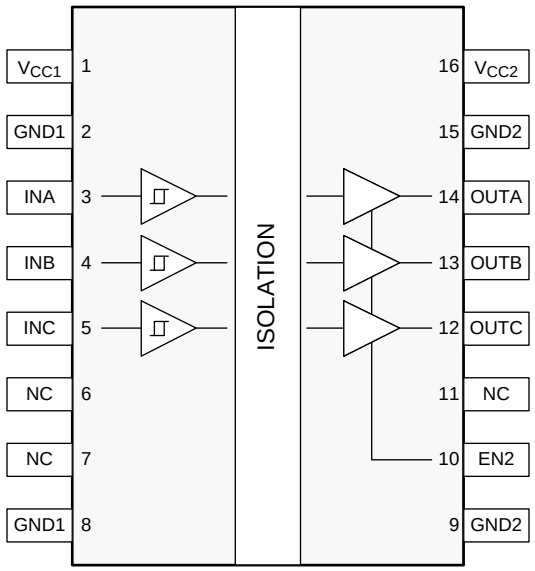
- 已更改 通篇更改了了 DIN 认证编号和认证状态 ... 1
- 已更改 将 DBQ 封装的隔离额定值从 2500V_{RMS} 更改成了 3000V_{RMS} ... 1
- Added V_{TEST} to the conditions for the maximum transient isolation voltage parameter in the *Insulation Specifications* table ... 6
- Changed the value for the DBQ package from 3600 VPK to 4242 V_{PK} throughout the document ... 6
- Changed the method b1 V_{ini} condition for apparent charge in the *Insulation Specifications* table ... 6

Changes from Original (November 2016) to Revision A **Page**

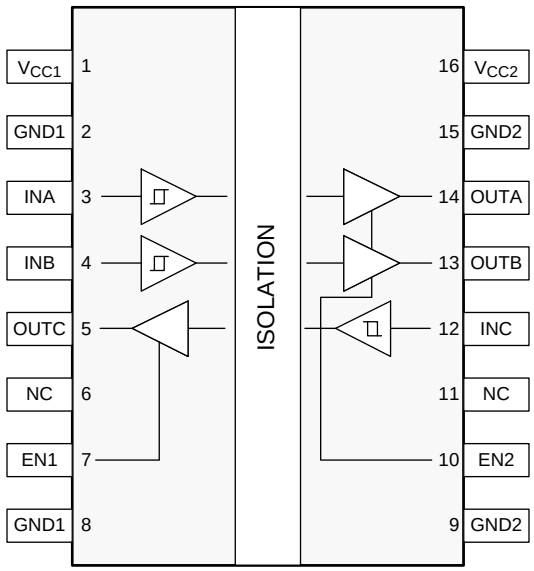
- Updated the *Safety-Related Certifications* table ... 7
- Changed the minimum CMTI from 40 to 85 in all *Electrical Characteristics* tables ... 8

5 Pin Configuration and Functions

ISO7730-Q1 DW and DBQ Packages
16-Pin SOIC-WB and QSOP
Top View



ISO7731-Q1 DW and DBQ Packages
16-Pin SOIC-WB and QSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	ISO7730-Q1	ISO7731-Q1		
EN1	—	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2, 8	2, 8	—	Ground connection for V_{CC1}
GND2	9, 15	9, 15	—	Ground connection for V_{CC2}
INA	3	3	I	Input, channel A
INB	4	4	I	Input, channel B
INC	5	12	I	Input, channel C
NC	6, 7, 11	6, 11	—	Not connected
OUTA	14	14	O	Output, channel A
OUTB	13	13	O	Output, channel B
OUTC	12	5	O	Output, channel C
V_{CC1}	1	1	—	Power supply, V_{CC1}
V_{CC2}	16	16	—	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)	–0.5	6	V
V	Voltage at INx, OUTx, ENx	–0.5	V_{CCX} + 0.5(3)	V
I_O	Output current	–15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±6000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO–)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{OH}	High-level output current	V_{CCO}(1) = 5 V	–4			mA
		V_{CCO} = 3.3 V	–2			
		V_{CCO} = 2.5 V	–1			
I_{OL}	Low-level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	
		V_{CCO} = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 × V_{CCI}(1)		V_{CCI}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CCI}	V
DR	Data rate		0		100	Mbps
T_A	Ambient temperature		-40	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.4 Thermal Information

THERMAL METRIC[1]		ISO773x-Q1		UNIT
		DW (SOIC)	DBQ (QSOP)	
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.4	109	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	44.9	46.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.9	60.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.1	35.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.5	60	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7730-Q1						
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			150	mW
P_{D1}	Maximum power dissipation by side-1				25	mW
P_{D2}	Maximum power dissipation by side-2				125	mW
ISO7731-Q1						
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			150	mW
P_{D1}	Maximum power dissipation by side-1				50	mW
P_{D2}	Maximum power dissipation by side-2				100	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION		UNIT
			DW-16	DBQ-16	
CLR	External clearance (1)	Shortest terminal-to-terminal distance through air	>8	>3.7	mm
CPG	External creepage (1)	Shortest terminal-to-terminal distance across the package surface	>8	>3.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I–IV	I–IV	
		Rated mains voltage ≤ 300 V_{RMS}	I–IV	I–III	
		Rated mains voltage ≤ 600 V_{RMS}	I–IV	n/a	
		Rated mains voltage ≤ 1000 V_{RMS}	I–III	n/a	
'DIN V VDE V 0884-11:2017-01 (2)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	566	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1000	400	V_{RMS}
		DC Voltage	1414	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	8000	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	Test method per IEC 60065, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	4000	V_{PK}
q_{pd}	Apparent charge (4)	Method a, After Input/Output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	≤5	
		Method b1; At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	≤5	
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.4 x sin (2πft), f = 1 MHz	~0.7	~0.7	pF
R_{IO}	Isolation resistance (5)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^9$	$>10^9$	
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

All certifications complete except CQC approval of DBQ-16 package devices

VDE	CSA	UL	CQC	TUV
Certified according to 'DIN V VDE V 0884-11:2017-01	Certified according to CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11 :2009/A1:2010/A12:2011/A2 :2013
Maximum transient isolation voltage, 8000 V_{PK} (DW-16) and 4242 V_{PK} (DBQ-16); Maximum repetitive peak isolation voltage, 1414 V_{PK} (DW-16, Reinforced) and 566 V_{PK} (DBQ-16); Maximum surge isolation voltage, 8000 V_{PK} (DW-16) and 4000 V_{PK} (DBQ-16)	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V_{RMS} (DW-16) and 370 V_{RMS} (DBQ-16) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (DW-16) max working voltage	**DW-16:** Single protection, 5000 V_{RMS}; **DBQ-16:** Single protection, 3000 V_{RMS}	**DW-16:** Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V_{RMS} maximum working voltage; **DBQ-16:** Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	5000 V_{RMS} (DW-16) and 3000 V_{RMS} (DBQ-16) Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} (DW-16) and 300 V_{RMS} (DBQ-16) 5000 V_{RMS} (DW-16) and 3000 V_{RMS} (DBQ-16) Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 V_{RMS} (DW -16) and 370 V_{RMS} (DBQ-16)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 81.4 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 1			279	mA
		$R_{\theta JA}$ = 81.4 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 1			427	
		$R_{\theta JA}$ = 81.4 °C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 1			558	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 81.4 °C/W, T_J = 150°C, T_A = 25°C, see Figure 3			1536	mW
T_S	Maximum safety temperature				150	°C
DBQ-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 109.0°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 2			209	mA
		$R_{\theta JA}$ = 109.0 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 2			319	
		$R_{\theta JA}$ = 109.0°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 2			417	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 109.0°C/W, T_J = 150°C, T_A = 25°C, see Figure 4			1147	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* is that of a device installed on a High-K test board for leaded surface mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 13	V_{CCO} (1) – 0.4	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 13		0.2	0.4	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 × V_{CCI}	0.7 × V_{CCI}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 × V_{CCI}	0.4 × V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 × V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; see Figure 16	85	100		kV/µs
C_I	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) Measured from input pin to ground.

6.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7730-Q1							
Supply current - disable	EN2 = 0 V; V_I = V_{CC1} (ISO7730-Q1); V_I = 0 V (ISO7730-Q1 with F suffix)		I_{CC1}		1	1.4	mA
			I_{CC2}		0.3	0.4	mA
	EN2 = 0 V; V_I = 0 V (ISO7730-Q1); V_I = V_{CC1} (ISO7730-Q1 with F suffix)		I_{CC1}		4.3	6	mA
			I_{CC2}		0.3	0.4	mA
Supply current - DC signal	EN2 = V_{CC2}; V_I = V_{CC1} (ISO7730-Q1); V_I = 0 V (ISO7730-Q1 with F suffix)		I_{CC1}		1	1.4	mA
			I_{CC2}		1.6	2.5	mA
	EN2 = V_{CC2}; V_I = 0 V (ISO7730-Q1); V_I = V_{CC1} (ISO7730-Q1 with F suffix)		I_{CC1}		4.3	6	mA
			I_{CC2}		1.8	2.7	mA
Supply current - AC signal	EN2 = V_{CCI}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.6	3.7	mA
			I_{CC2}		1.9	2.8	mA
		10 Mbps	I_{CC1}		2.7	3.8	mA
			I_{CC2}		3.3	4.5	mA
		100 Mbps	I_{CC1}		3.6	4.6	mA
			I_{CC2}		17.5	21	mA
ISO7731-Q1							
Supply current - disable	EN1 = EN2 = 0 V; V_I = V_{CCI} (1) (ISO7731-Q1); V_I = 0 V (ISO7731-Q1 with F suffix)		I_{CC1}		0.8	1.2	mA
			I_{CC2}		0.7	1	mA
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7731-Q1); V_I = V_{CCI} (ISO7731-Q1 with F suffix)		I_{CC1}		3	4.3	mA
			I_{CC2}		1.8	2.6	mA
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISO7731-Q1); V_I = 0 V (ISO7731-Q1 with F suffix)		I_{CC1}		1.3	1.7	mA
			I_{CC2}		1.6	2.2	mA
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7731-Q1); V_I = V_{CCI} (ISO7731-Q1 with F suffix)		I_{CC1}		3.5	5	mA
			I_{CC2}		2.8	4.1	mA
Supply current - AC signal	EN1 = EN2 = V_{CCI}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.7	3.4	mA
			I_{CC2}		2.3	3.3	mA
		10 Mbps	I_{CC1}		3	4	mA
			I_{CC2}		3.3	4.4	mA
		100 Mbps	I_{CC1}		8.5	11	mA
			I_{CC2}		13.1	16	mA

(1) V_{CCI} = Input-side V_{CC}

6.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 13	V_{CCO}(1) – 0.3	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see Figure 13		0.1	0.3	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 × V_{CCI}	0.7 × V_{CCI}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 × V_{CCI}	0.4 × V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 × V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; see Figure 16	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7730-Q1							
Supply current - disable	EN2 = 0 V; V_I = V_{CC1} (ISO7730-Q1); V_I = 0 V (ISO7730-Q1 with F suffix)		I_{CC1}		1	1.4	mA
			I_{CC2}		0.3	0.4	mA
	EN2 = 0 V; V_I = 0 V (ISO7730-Q1); V_I = V_{CC1} (ISO7730-Q1 with F suffix)		I_{CC1}		4.3	6	mA
			I_{CC2}		0.3	0.4	mA
Supply current - DC signal	EN2 = V_{CC2}; V_I = V_{CC1} (ISO7730-Q1); V_I = 0 V (ISO7730-Q1 with F suffix)		I_{CC1}		1	1.4	mA
			I_{CC2}		1.6	2.5	mA
	EN2 = V_{CC2}; V_I = 0 V (ISO7730-Q1); V_I = V_{CC1} (ISO7730-Q1 with F suffix)		I_{CC1}		4.3	6	mA
			I_{CC2}		1.8	2.7	mA
Supply current - AC signal	EN2 = V_{CCI}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.6	3.7	mA
			I_{CC2}		1.8	2.8	mA
		10 Mbps	I_{CC1}		2.7	3.8	mA
			I_{CC2}		2.8	3.9	mA
		100 Mbps	I_{CC1}		3.3	4.3	mA
			I_{CC2}		13	17	mA
ISO7731-Q1							
Supply current - disable	EN1 = EN2 = 0 V; V_I = V_{CCI}(1) (ISO7731-Q1); V_I = 0 V (ISO7731-Q1 with F suffix)		I_{CC1}		0.8	1.2	mA
			I_{CC2}		0.7	1	mA
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7731-Q1); V_I = V_{CCI} (ISO7731-Q1 with F suffix)		I_{CC1}		3	4.3	mA
			I_{CC2}		1.8	2.6	mA
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISO7731-Q1); V_I = 0 V (ISO7731-Q1 with F suffix)		I_{CC1}		1.3	1.7	mA
			I_{CC2}		1.6	2.2	mA
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7731-Q1); V_I = V_{CCI} (ISO7731-Q1 with F suffix)		I_{CC1}		3.5	5	mA
			I_{CC2}		2.8	4.1	mA
Supply current - AC signal	EN1 = EN2 = V_{CCI}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.4	3.4	mA
			I_{CC2}		2.2	3.3	mA
		10 Mbps	I_{CC1}		2.8	3.8	mA
			I_{CC2}		2.9	4	mA
		100 Mbps	I_{CC1}		6.7	8.5	mA
			I_{CC2}		10	12.5	mA

(1) V_{CCI} = Input-side V_{CC}

6.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see Figure 13	V_{CCO}(1) – 0.2	2.45		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see Figure 13		0.05	0.2	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 × V_{CCI}	0.7 × V_{CCI}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 × V_{CCI}	0.4 × V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 × V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; see Figure 16	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7730-Q1							
Supply current - disable	EN2 = 0 V; V_I = V_{CC1} (ISO7730-Q1); V_I = 0 V (ISO7730-Q1 with F suffix)		I_{CC1}		1	1.4	mA
			I_{CC2}		0.3	0.4	mA
	EN2 = 0 V; V_I = 0 V (ISO7730-Q1); V_I = V_{CC1} (ISO7730-Q1 with F suffix)		I_{CC1}		4.3	6	mA
			I_{CC2}		0.3	0.4	mA
Supply current - DC signal	EN2 = V_{CC2}; V_I = V_{CC1} (ISO7730-Q1); V_I = 0 V (ISO7730-Q1 with F suffix)		I_{CC1}		1	1.4	mA
			I_{CC2}		1.6	2.5	mA
	EN2 = V_{CC2}; V_I = 0 V (ISO7730-Q1); V_I = V_{CC1} (ISO7730-Q1 with F suffix)		I_{CC1}		4.3	6	mA
			I_{CC2}		1.8	2.7	mA
Supply current - AC signal	EN2 = V_{CC2}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.6	3.7	mA
			I_{CC2}		1.8	2.7	mA
		10 Mbps	I_{CC1}		2.6	3.8	mA
			I_{CC2}		2.5	3.6	mA
		100 Mbps	I_{CC1}		3.1	4.2	mA
			I_{CC2}		10.2	14	mA
ISO7731-Q1							
Supply current - disable	EN1 = EN2 = 0 V; V_I = V_{CCI}(1) (ISO7731-Q1); V_I = 0 V (ISO7731-Q1 with F suffix)		I_{CC1}		0.8	1.2	mA
			I_{CC2}		0.7	1	mA
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7731-Q1); V_I = V_{CCI} (ISO7731-Q1 with F suffix)		I_{CC1}		3	4.3	mA
			I_{CC2}		1.8	2.6	mA
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISO7731-Q1); V_I = 0 V (ISO7731-Q1 with F suffix)		I_{CC1}		1.3	1.7	mA
			I_{CC2}		1.6	2.2	mA
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7731-Q1); V_I = V_{CCI} (ISO7731-Q1 with F suffix)		I_{CC1}		3.5	5	mA
			I_{CC2}		2.8	4.1	mA
Supply current - AC signal	EN1 = EN2 = V_{CCI}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.4	3.4	mA
			I_{CC2}		2.2	3.2	mA
		10 Mbps	I_{CC1}		2.7	3.7	mA
			I_{CC2}		2.7	3.8	mA
		100 Mbps	I_{CC1}		5.6	7	mA
			I_{CC2}		8	10	mA

(1) V_{CCI} = Input-side V_{CC}

6.15 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 13	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 13		1.3	3.9	ns
t_f	Output signal fall time			1.4	3.9	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 14		8	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			8	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO773x-Q1			7	20	ns
	Enable propagation delay, high impedance-to-high output for ISO773x-Q1 with F suffix			3	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO773x-Q1			3	8.5	µs
	Enable propagation delay, high impedance-to-low output for ISO773x-Q1 with F suffix			7	20	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 15		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.6		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 13	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.1	5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 13		1.3	3	ns
t_f	Output signal fall time			1.3	3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 14		17	30	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			17	30	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO773x-Q1			17	30	ns
	Enable propagation delay, high impedance-to-high output for ISO773x-Q1 with F suffix			3.2	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO773x-Q1			3.2	8.5	µs
	Enable propagation delay, high impedance-to-low output for ISO773x-Q1 with F suffix			17	30	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 15		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.6		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.17 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 13	7.5	12	18.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.2	5.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction Channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.6	ns
t_r	Output signal rise time	See Figure 13		1	3.5	ns
t_f	Output signal fall time			1	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 14		22	40	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			22	40	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO773x-Q1			18	40	ns
	Enable propagation delay, high impedance-to-high output for ISO773x-Q1 with F suffix			3.3	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO773x-Q1			3.3	8.5	µs
	Enable propagation delay, high impedance-to-low output for ISO773x-Q1 with F suffix			18	40	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 15		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.6		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Insulation Characteristics Curves

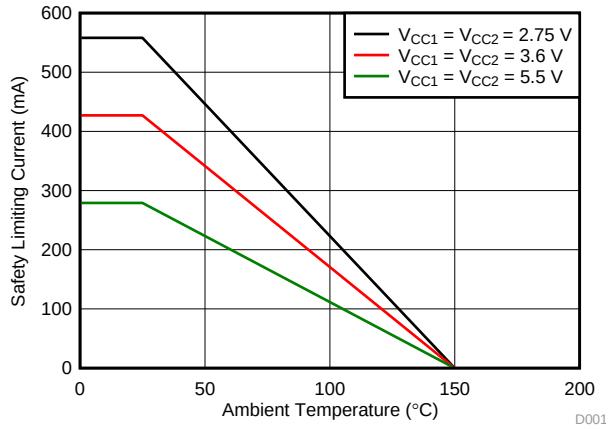


Figure 1. Thermal Derating Curve for Safety Limiting Current per VDE for DW-16 Package

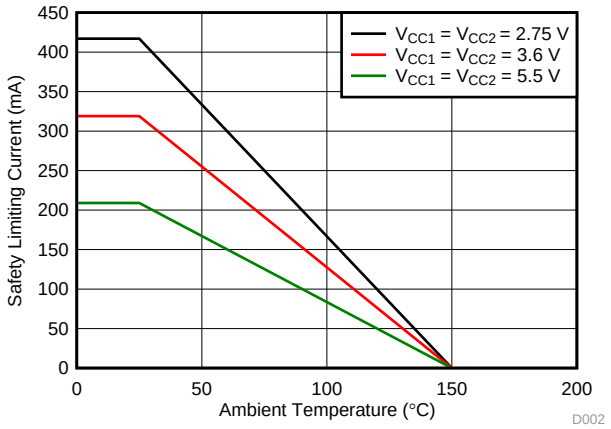


Figure 2. Thermal Derating Curve for Safety Limiting Current per VDE for DBQ-16 Package

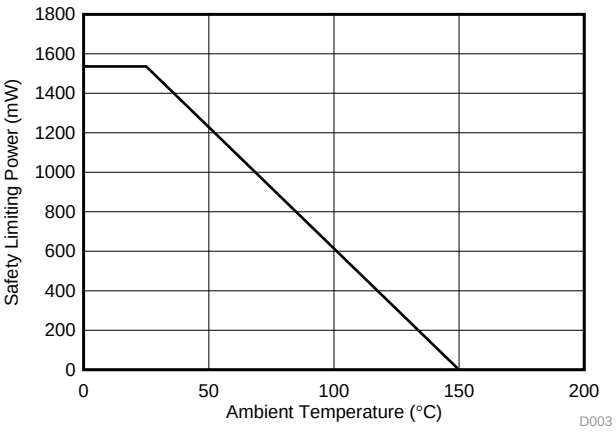


Figure 3. Thermal Derating Curve for Safety Limiting Power per VDE for DW-16 Package

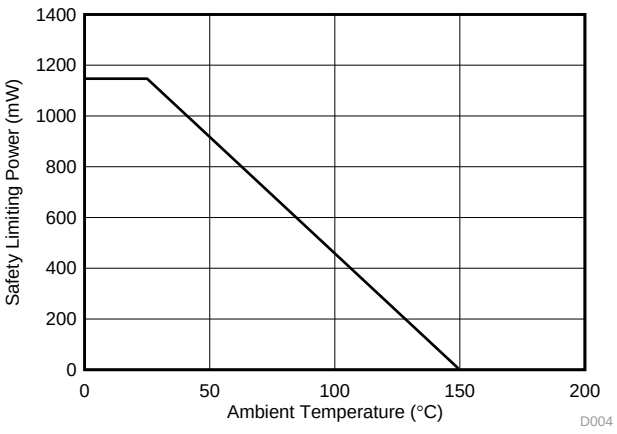
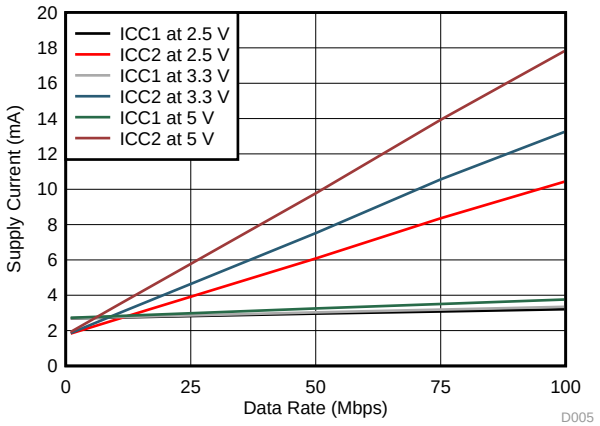


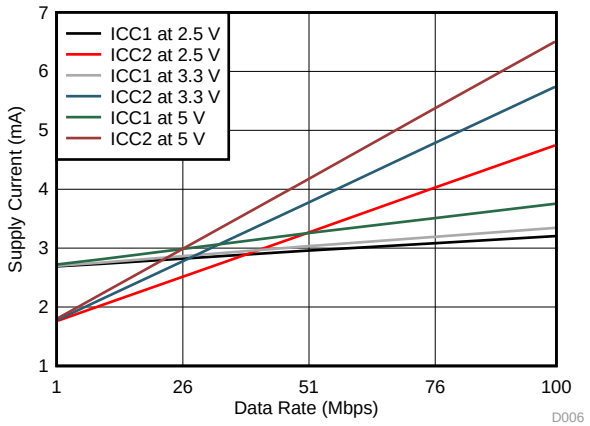
Figure 4. Thermal Derating Curve for Safety Limiting Power per VDE for DBQ-16 Package

6.19 Typical Characteristics



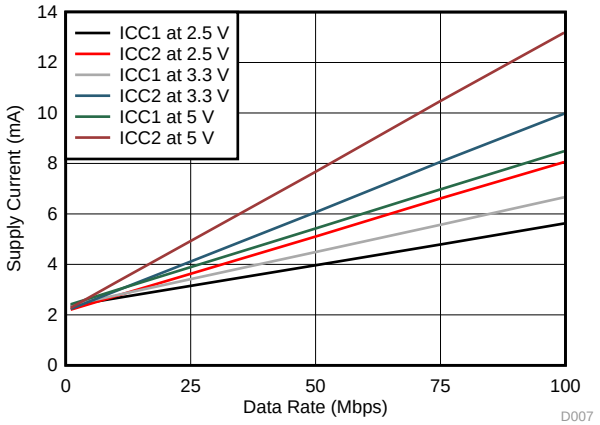
T_A = 25°C C_L = 15 pF

Figure 5. ISO7730-Q1 Supply Current vs Data Rate (With 15-pF Load)



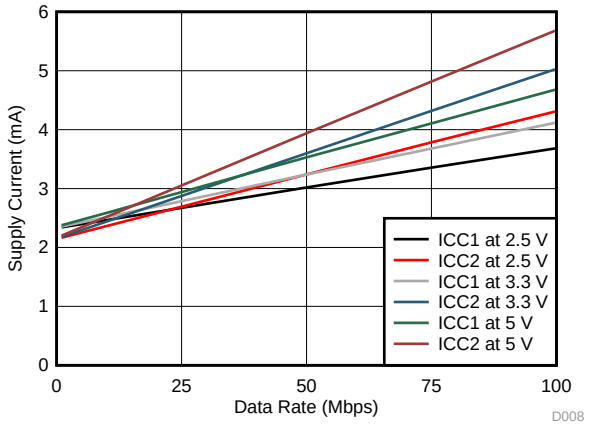
T_A = 25°C C_L = No Load

Figure 6. ISO7730-Q1 Supply Current vs Data Rate (With No Load)



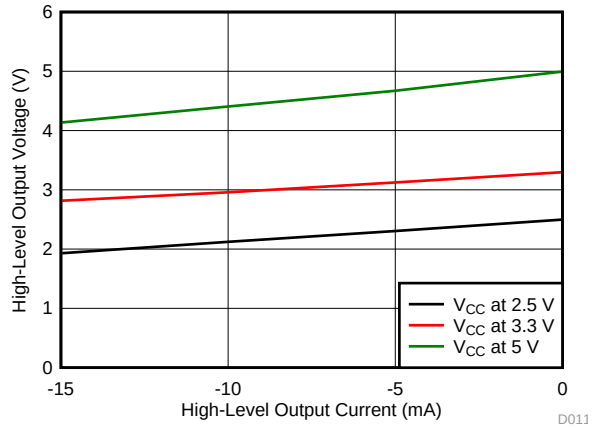
T_A = 25°C C_L = 15 pF

Figure 7. ISO7731-Q1 Supply Current vs Data Rate (With 15-pF Load)



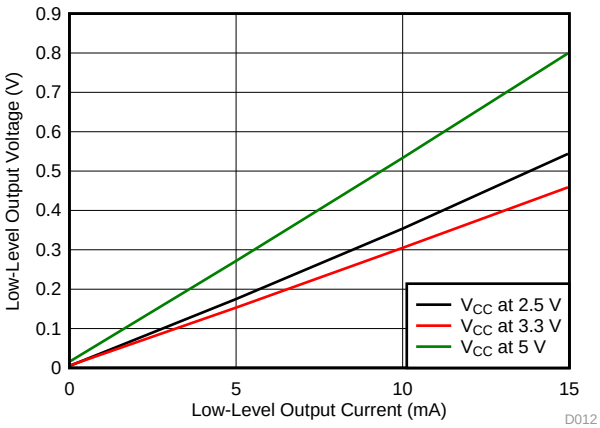
T_A = 25°C C_L = No Load

Figure 8. ISO7731-Q1 Supply Current vs Data Rate (With No Load)



T_A = 25°C

Figure 9. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

Figure 10. Low-Level Output Voltage vs Low-Level Output Current

Typical Characteristics (continued)

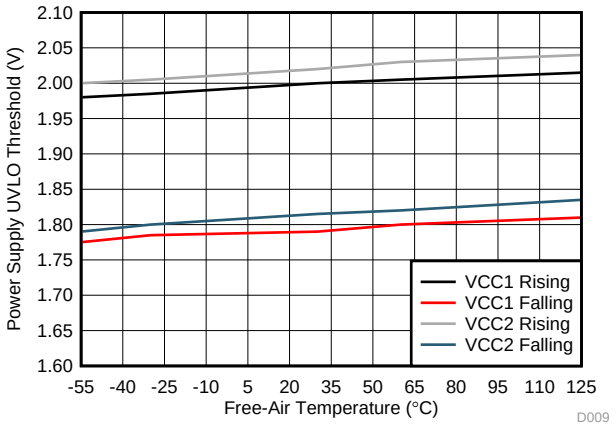


Figure 11. Power Supply Undervoltage Threshold vs Free-Air Temperature

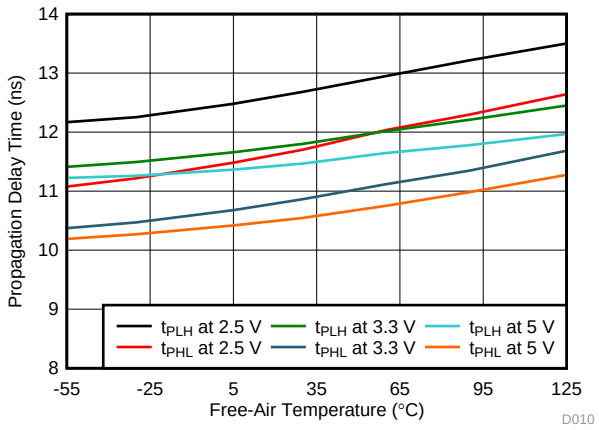
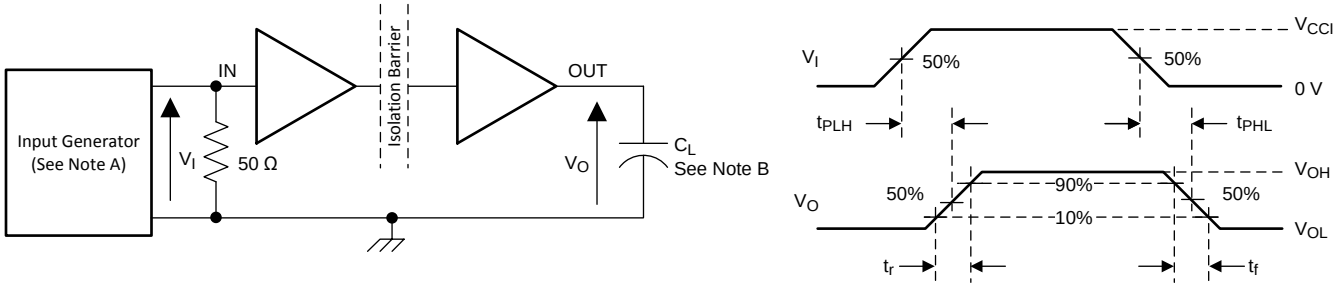


Figure 12. Propagation Delay Time vs Free-Air Temperature

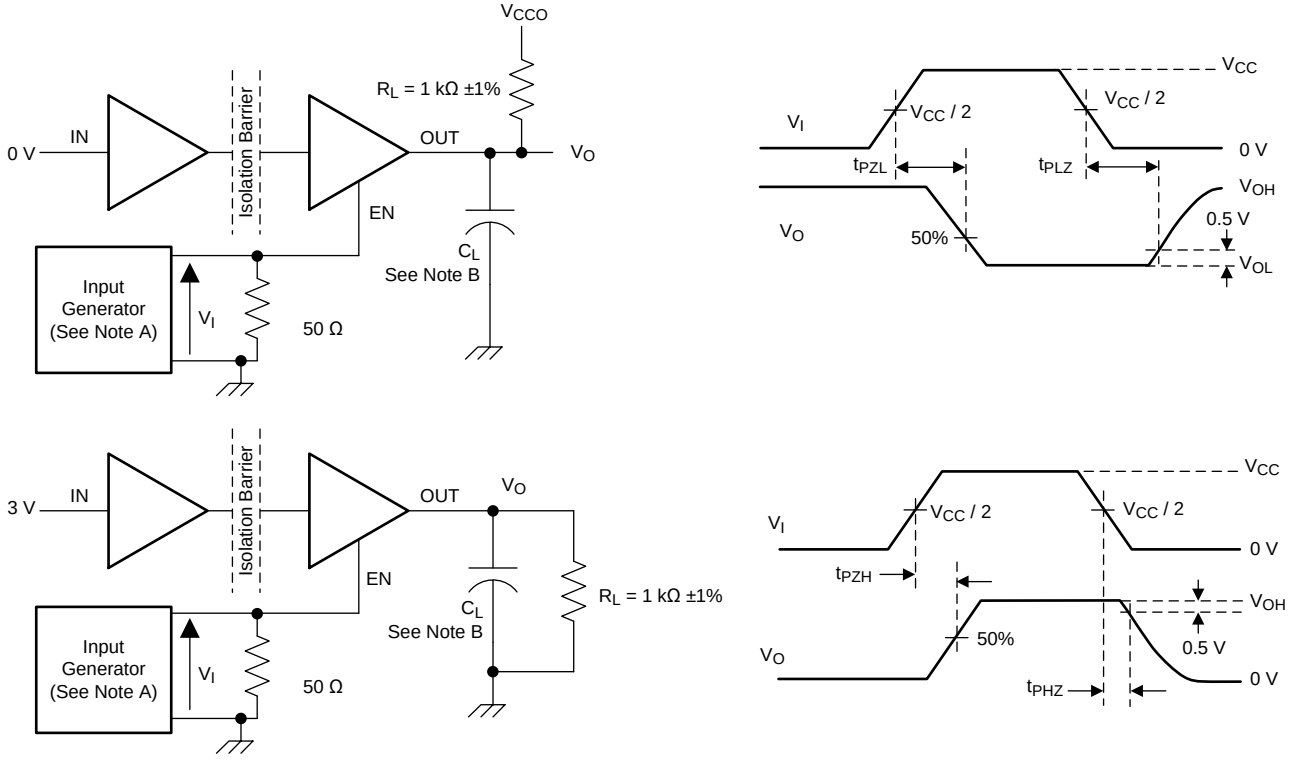
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. Switching Characteristics Test Circuit and Voltage Waveforms

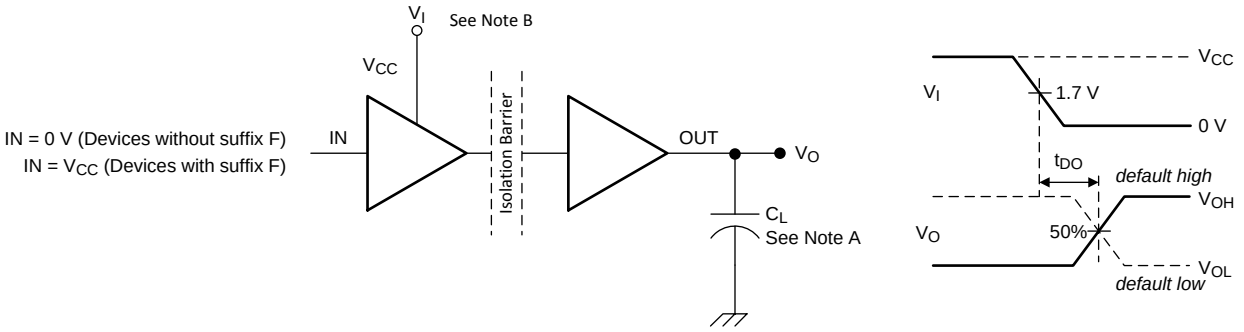


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 14. Enable/Disable Propagation Delay Time Test Circuit and Waveform

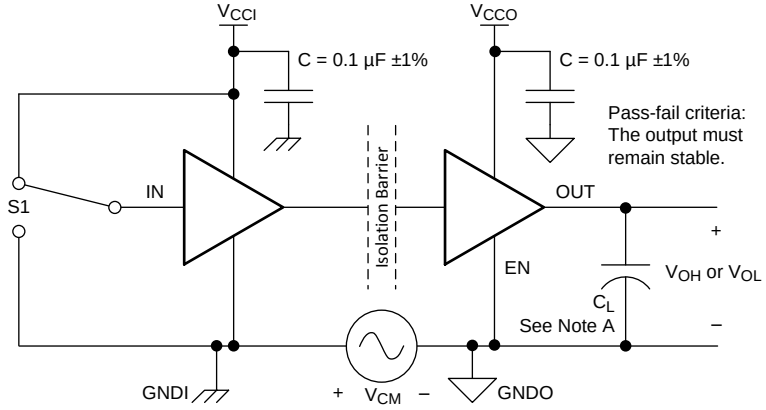
Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

Figure 15. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 16. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO773x-Q1 family of devices has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO773x-Q1 family of devices also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 17, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

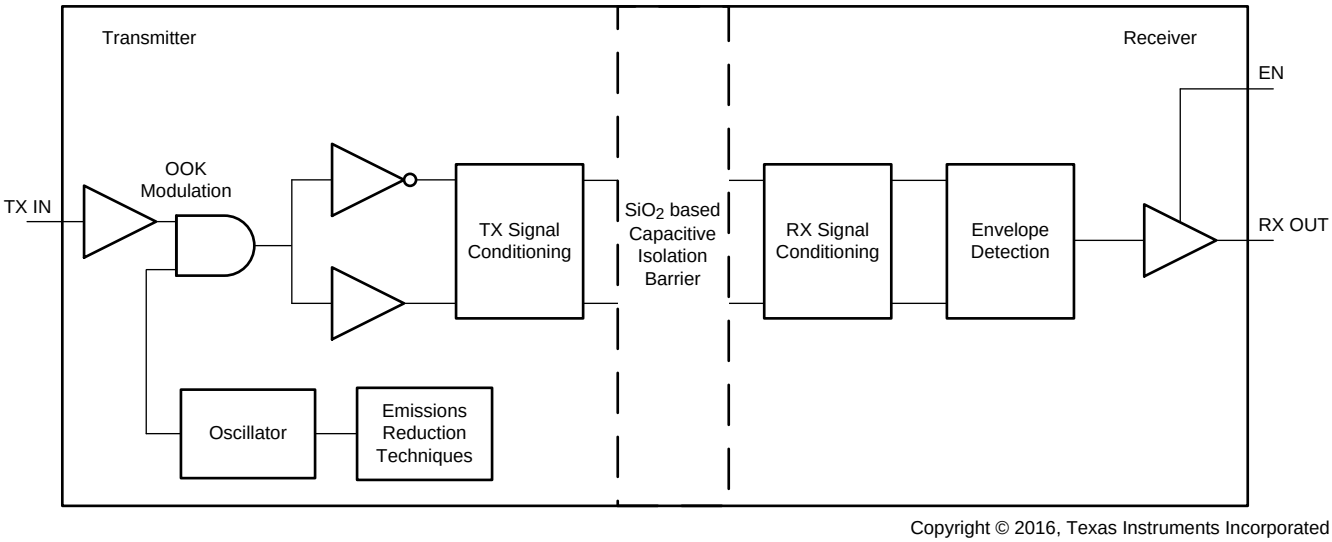


Figure 17. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 18 shows a conceptual detail of how the ON-OFF keying scheme works.

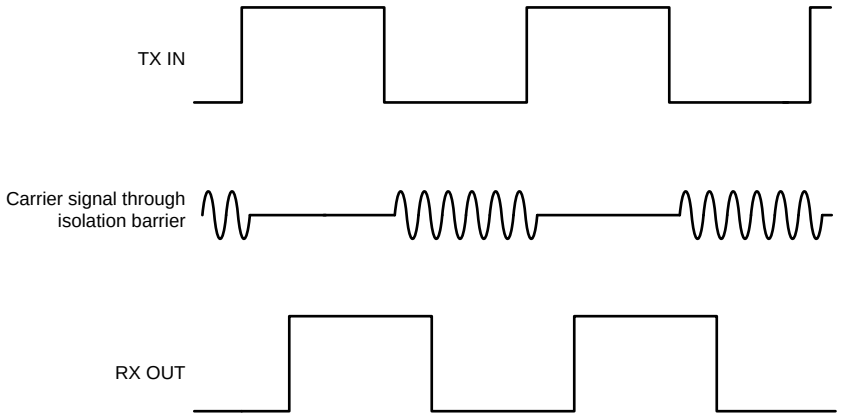


Figure 18. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

Table 1 provides an overview of the device features.

Table 1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION(1)
ISO7730-Q1	3 Forward, 0 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7730-Q1 with F suffix	3 Forward, 0 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7731-Q1	2 Forward, 1 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7731-Q1 with F suffix	2 Forward, 1 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}

(1) See *Safety-Related Certifications* for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO773x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

8.4 Device Functional Modes

Table 2 lists the functional modes for the ISO773x-Q1 devices.

Table 2. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is *High* for ISO773x-Q1 and *Low* for ISO773x-Q1 with F suffix.
X	PU	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for IISO773x-Q1 and *Low* for ISO773x-Q1 with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of its input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(3). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of its input

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.

8.4.1 Device I/O Schematics

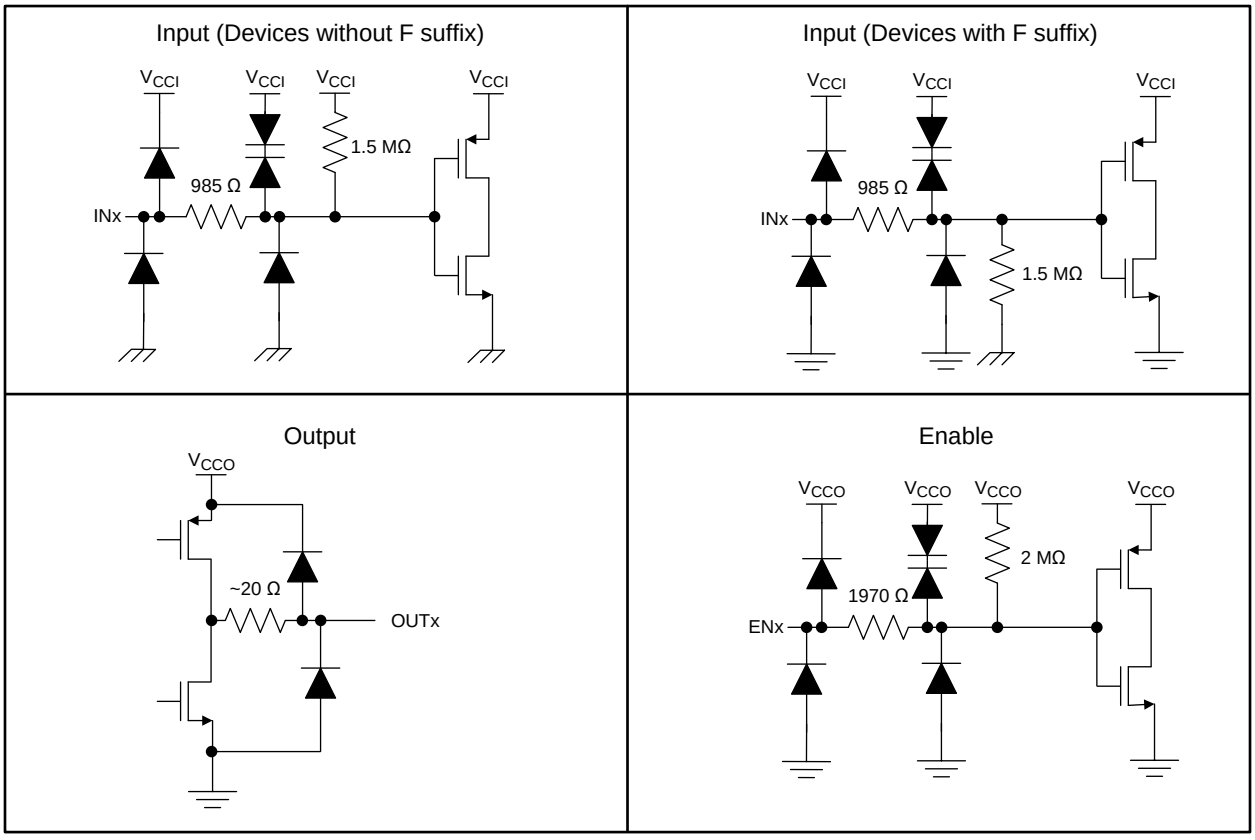


Figure 19. Device I/O Schematics

9 Application and Implementation

NOTE

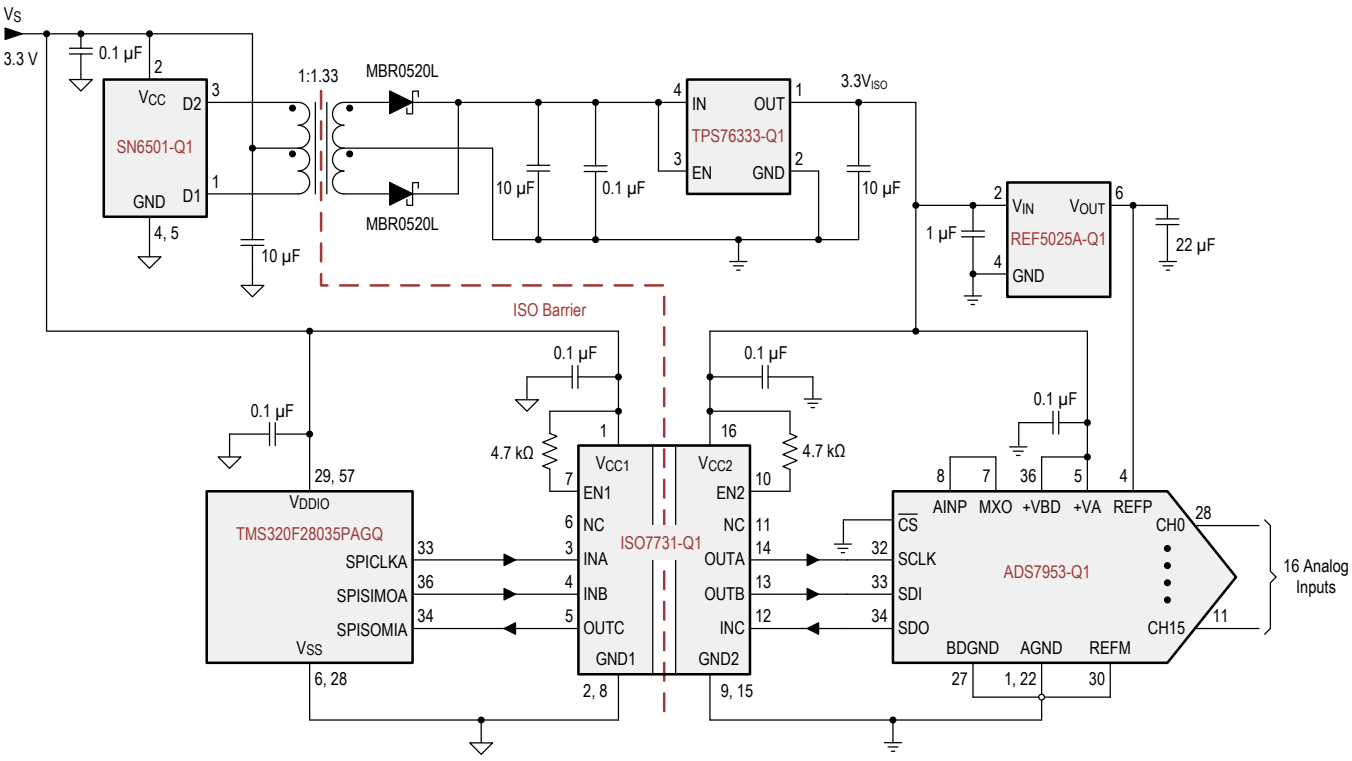
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO773x-Q1 devices are high-performance, triple-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for multi-master driving applications and reduce power consumption. The ISO773x-Q1 family of devices use single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7731-Q1 device combined with Texas Instruments' Piccolo™ microcontroller, analog-to-digital receiver, transformer driver, and voltage regulator can create an isolated serial peripheral interface (SPI) as shown in Figure 20.



Multiple pins and discrete components are omitted for clarity.

Figure 20. Isolated SPI for an Analog Input Module With 16 Inputs and a Single Slave

Typical Application (continued)

9.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO773x-Q1 family of devices only requires two external bypass capacitors to operate. Figure 21 and Figure 22 show the typical circuit hook-up for the devices.

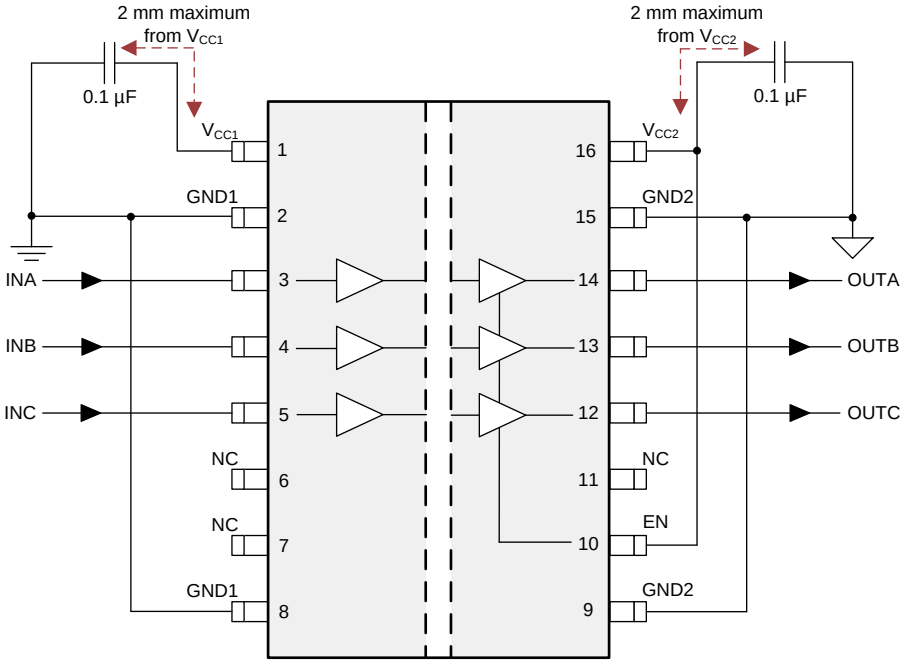


Figure 21. Typical ISO7730-Q1 Circuit Hook-Up

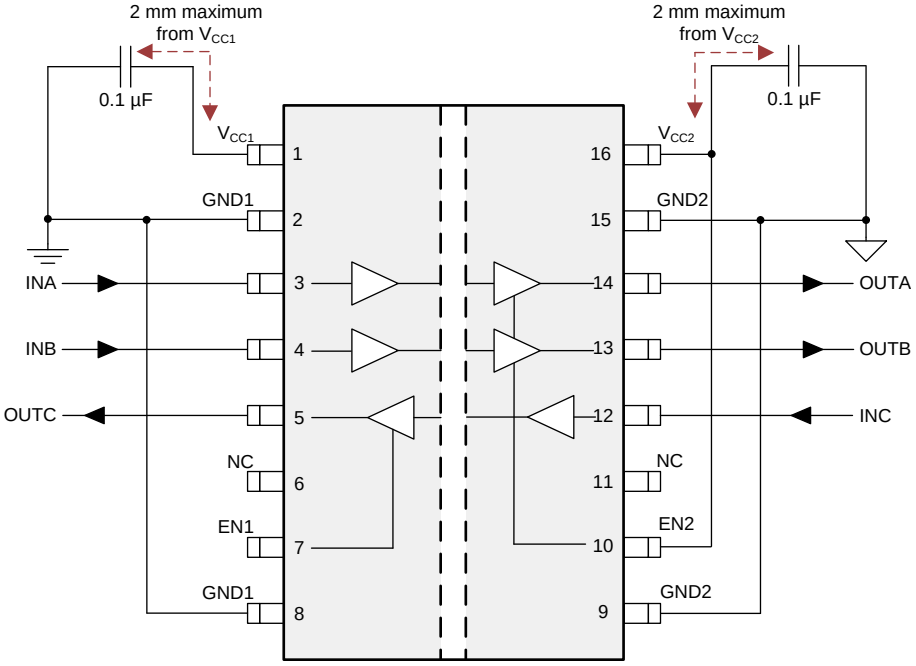


Figure 22. Typical ISO7731-Q1 Circuit Hook-Up

9.2.3 Application Curves

The following typical eye diagrams of the ISO773x-Q1 family of devices indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.

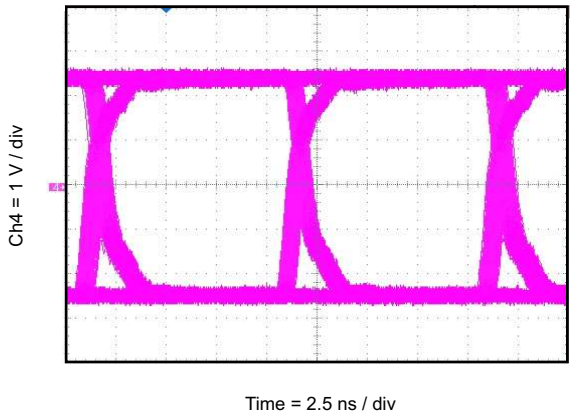


Figure 23. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 5 V and 25°C

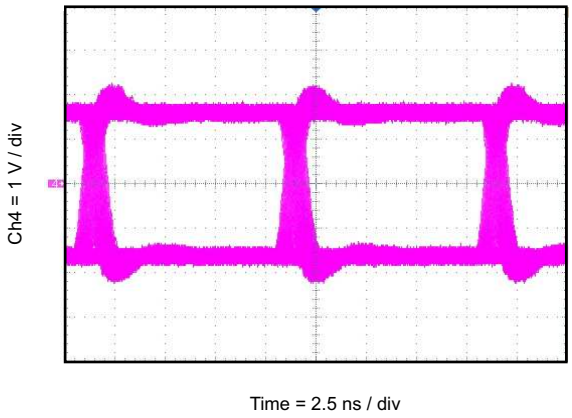


Figure 24. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 3.3 V and 25°C

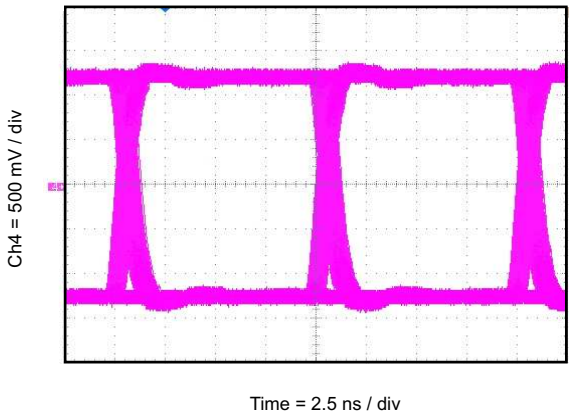


Figure 25. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 2.5 V and 25°C

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501-Q1. For such applications, detailed power supply design and transformer selection recommendations are available in the *SN6501-Q1 Transformer Driver for Isolated Power Supplies* data sheet.

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 26). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

11.2 Layout Example

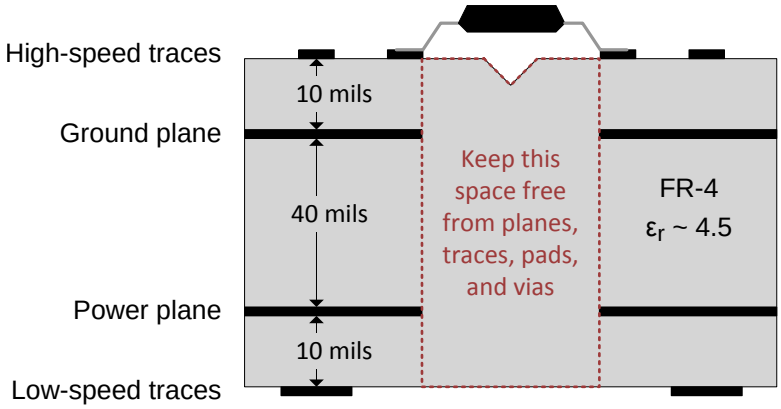


Figure 26. Layout Example Schematic

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《数字隔离器设计指南》*
- 德州仪器 (TI)，*《隔离相关术语》*
- 德州仪器 (TI)，*《REF50xxA-Q1 低噪声、极低漂移、精密电压基准》数据表*
- 德州仪器 (TI)，*《SN6501-Q1 用于隔离式电源的变压器驱动器》数据表*
- 德州仪器 (TI)，TPS76333-Q1*《低功耗 150mA 低压降线性稳压器》数据表*
- 德州仪器 (TI)，TMS320F28035*《Piccolo™ 微控制器》数据表*

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **4.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
ISO7730-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7731-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.5 商标

Piccolo, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

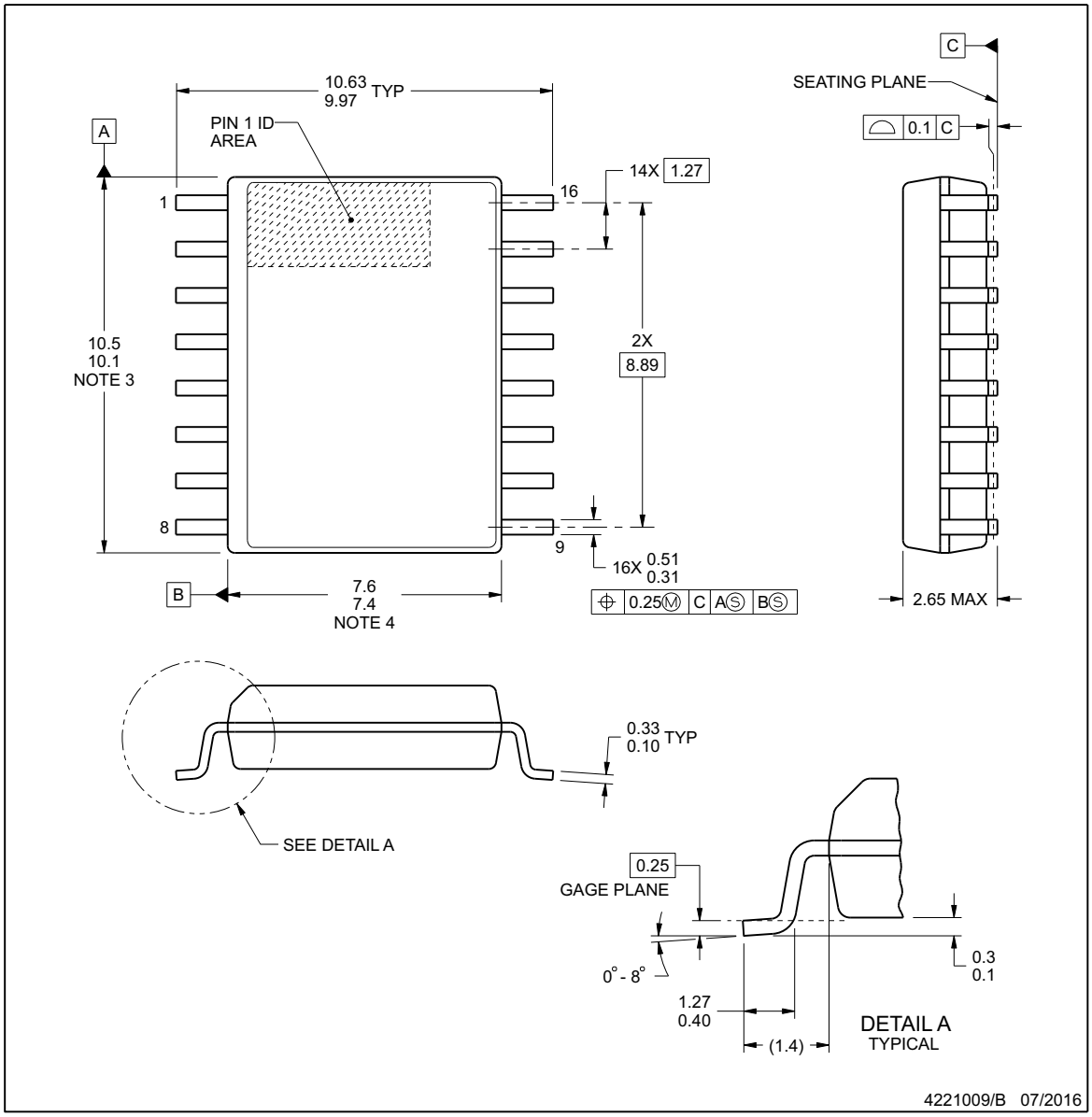
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



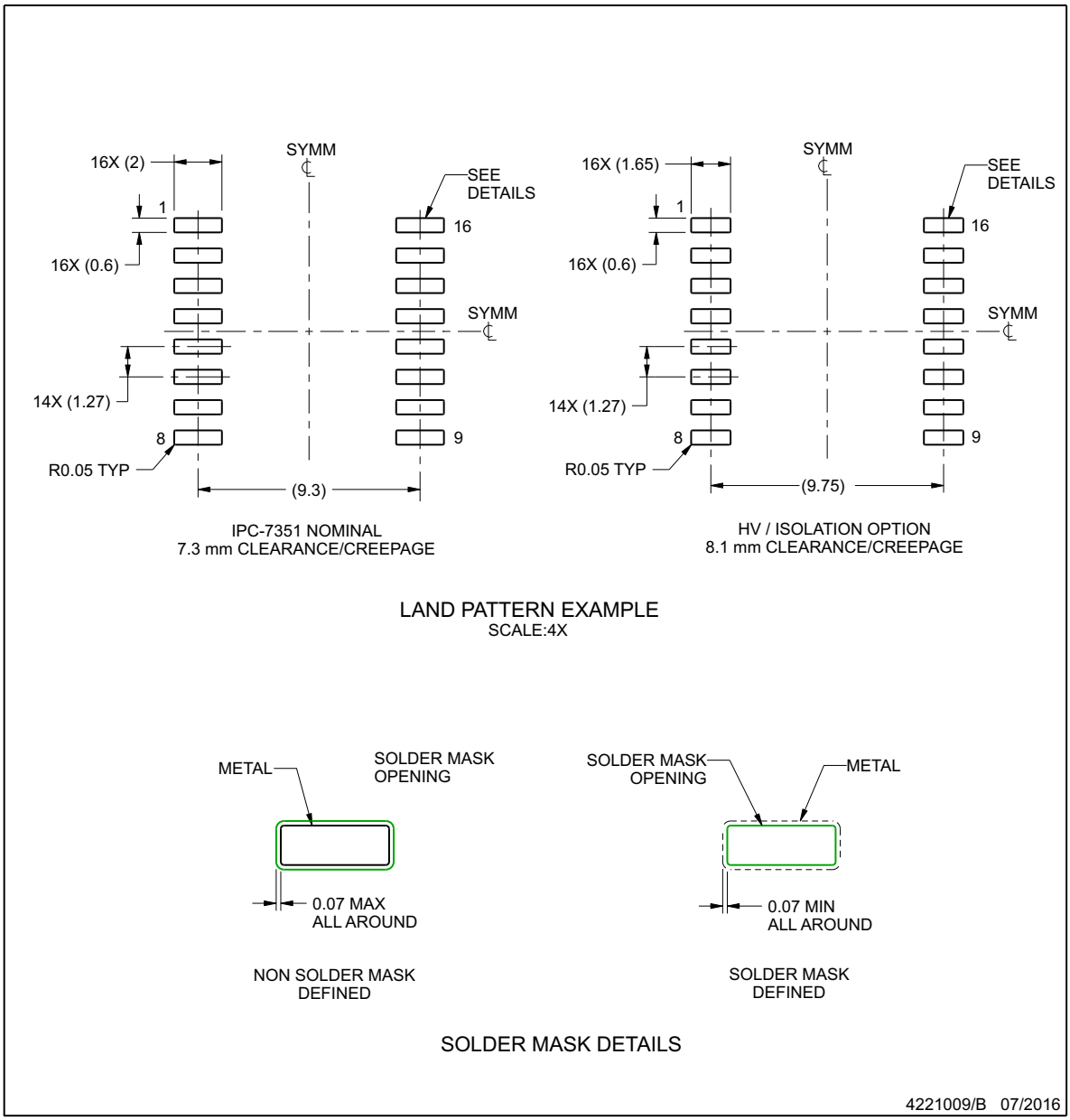
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B **SOIC - 2.65 mm max height**

SOIC



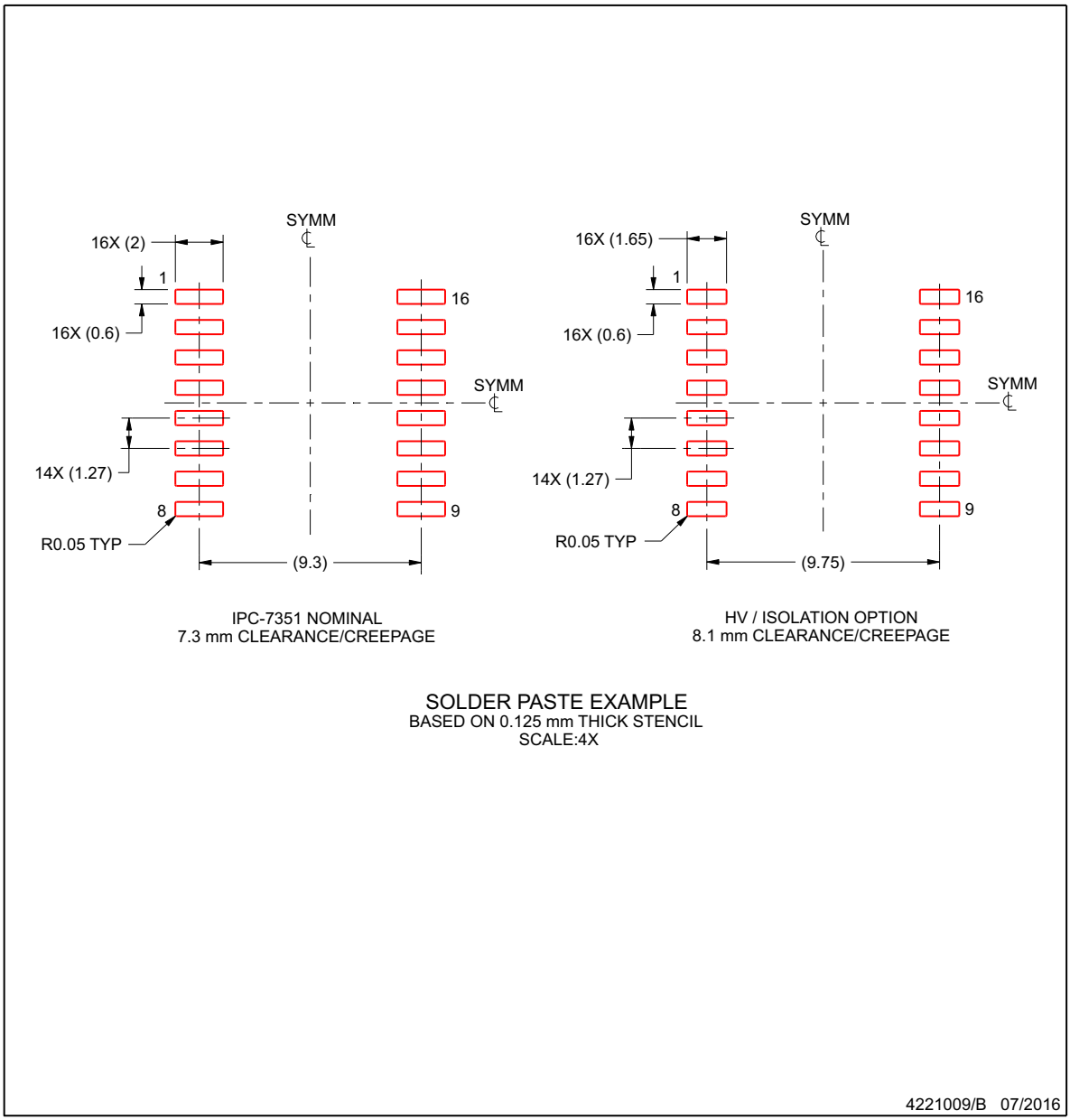
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B — **SOIC - 2.65 mm max height**

SOIC



NOTES: (continued)

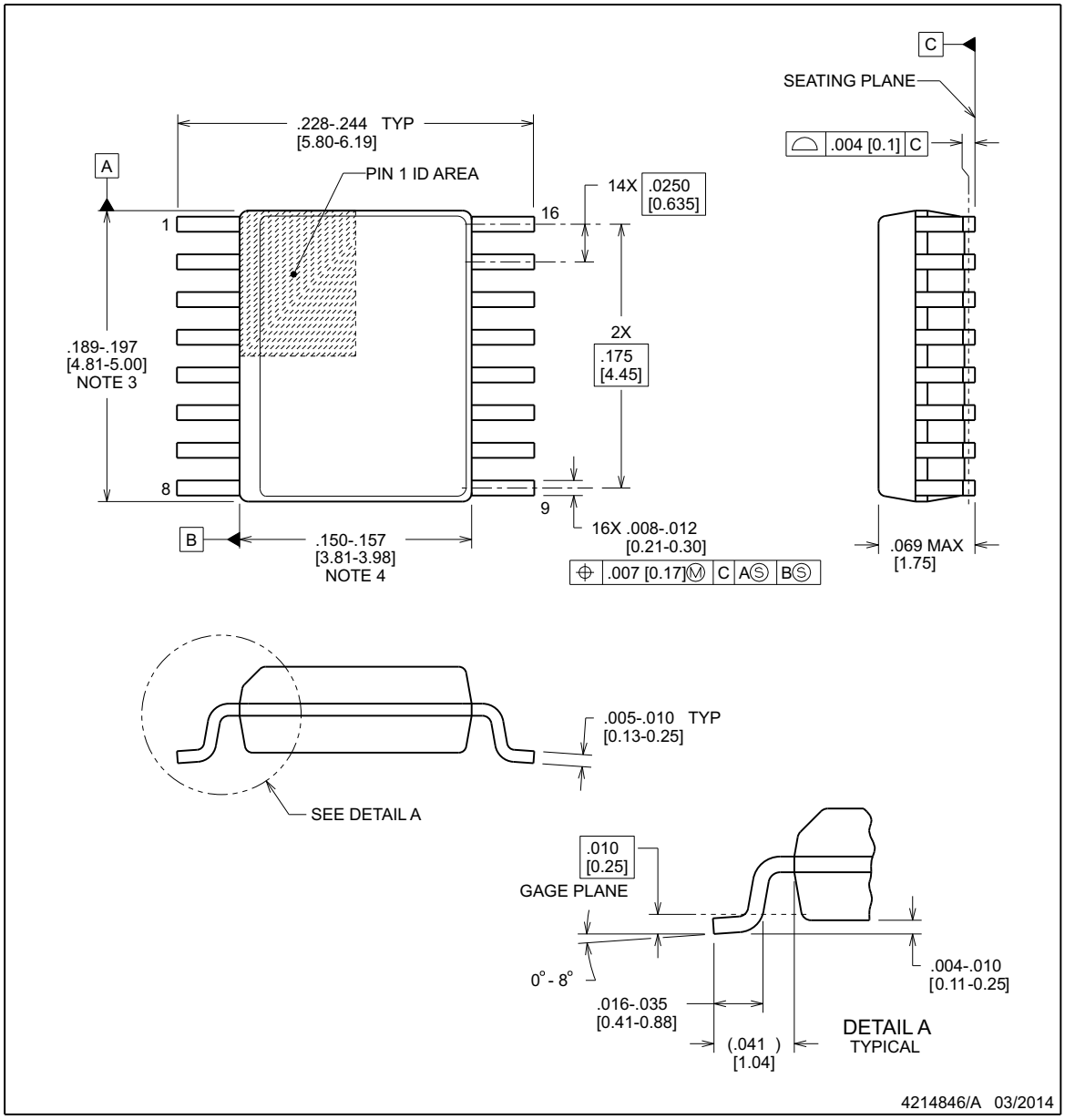
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



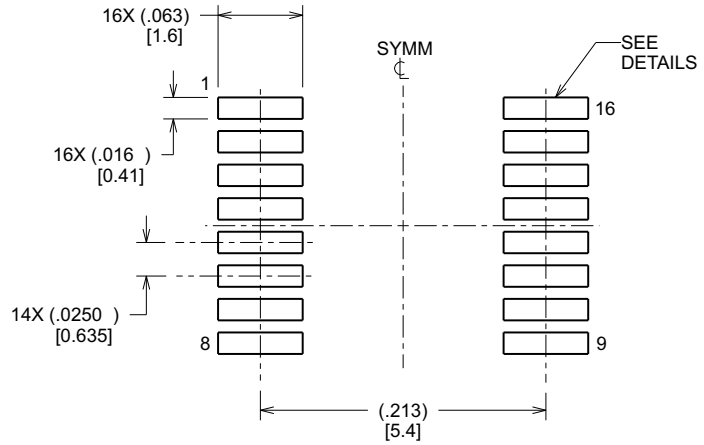
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

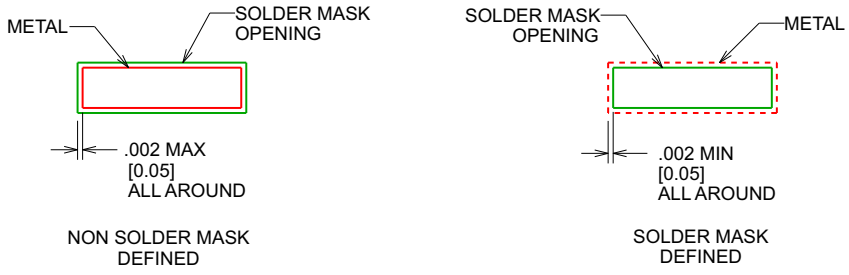
EXAMPLE BOARD LAYOUT

DBQ0016A — **SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

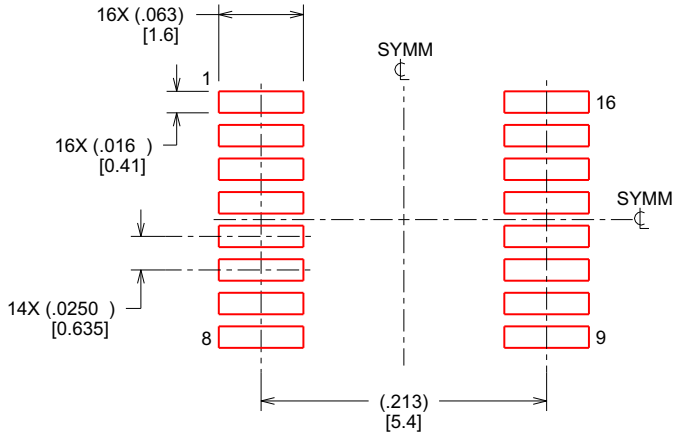
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7730FQDBQQ1	ACTIVE	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7730FQ	Samples
ISO7730FQDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7730FQ	Samples
ISO7730FQDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7730FQ	Samples
ISO7730FQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7730FQ	Samples
ISO7730QDBQQ1	ACTIVE	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7730Q	Samples
ISO7730QDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7730Q	Samples
ISO7730QDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7730Q	Samples
ISO7730QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7730Q	Samples
ISO7731FQDBQQ1	ACTIVE	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7731FQ	Samples
ISO7731FQDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7731FQ	Samples
ISO7731FQDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7731FQ	Samples
ISO7731FQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7731FQ	Samples
ISO7731QDBQQ1	ACTIVE	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7731Q	Samples
ISO7731QDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7731Q	Samples
ISO7731QDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7731Q	Samples
ISO7731QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7731Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

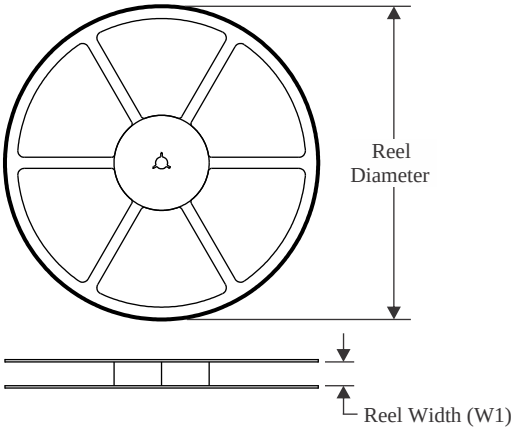
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

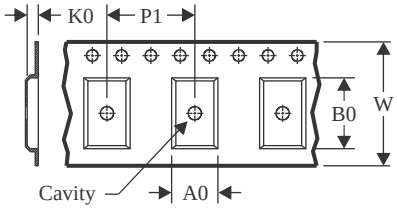
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

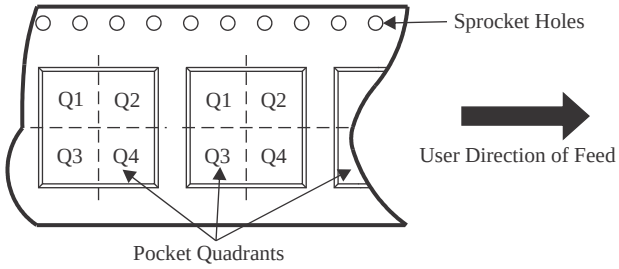


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

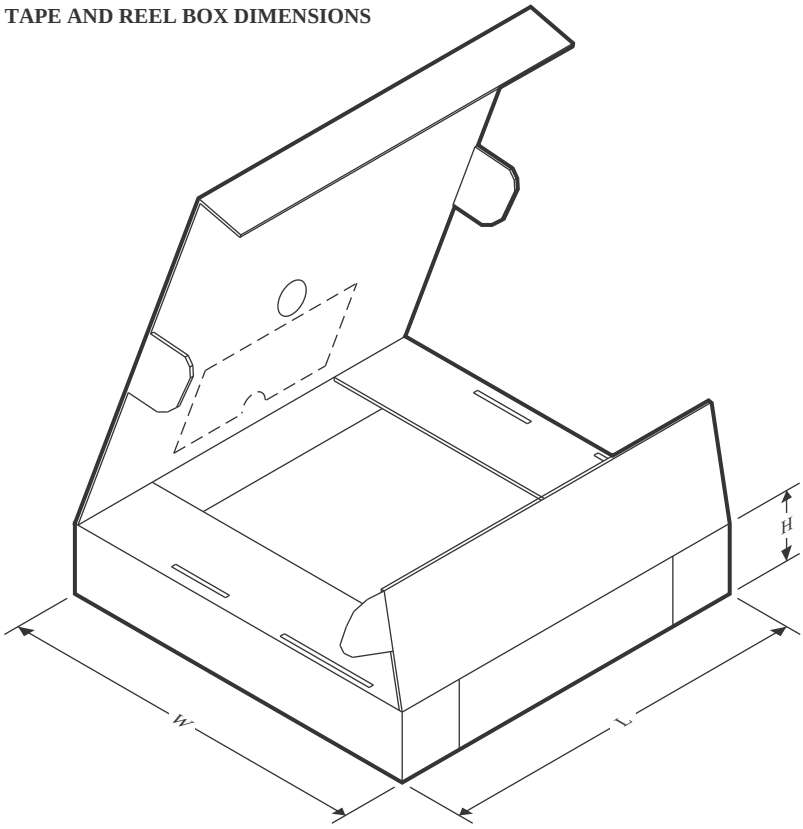
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7730FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7730FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7730QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7731FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7731QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

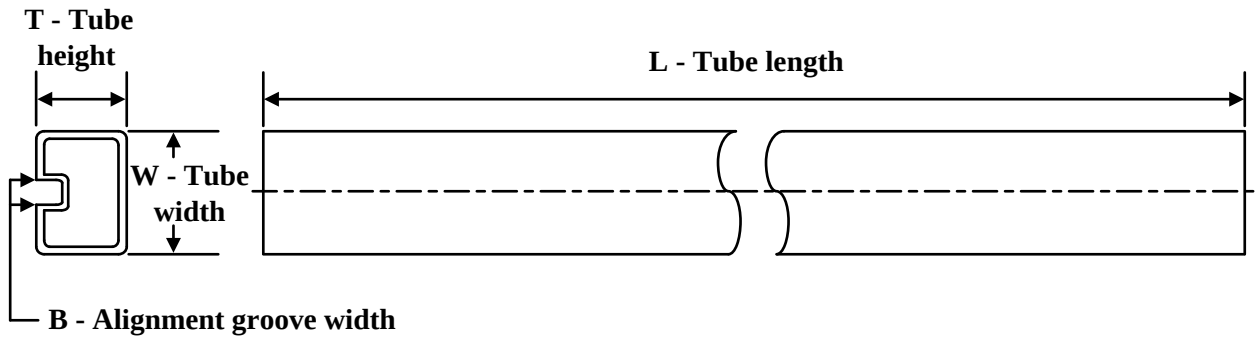
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7730FQDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7730FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7730FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7730FQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7730QDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7730QDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7730QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7730QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7731FQDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7731FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7731FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7731FQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7731QDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7731QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7731QDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7731QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7730FQDBQQ1	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7730FQDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7730FQDWQ1	DW	SOIC	16	40	507	12.83	5080	6.6
ISO7730QDBQQ1	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7730QDWQ1	DW	SOIC	16	40	507	12.83	5080	6.6
ISO7730QDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7731FQDBQQ1	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7731FQDWQ1	DW	SOIC	16	40	507	12.83	5080	6.6
ISO7731FQDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7731QDBQQ1	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7731QDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7731QDWQ1	DW	SOIC	16	40	507	12.83	5080	6.6

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