具有功率限制功能的 LM5069 正高电压热插拔和浪涌电流控制器

1 特性

- 宽工作电压范围：9V 至 80V
- 浪涌电流限制，用于将电路板安全插入带电电源
- 外部导通器件中的可编程最大功耗
- 可调节电流限制
- 针对严重过流事件的断路器功能
- 适用于外部 N 沟道 MOSFET 的内部高侧电荷泵和栅极驱动器
- 可调节欠压锁定 (UVLO) 和迟滞
- 可调节过压锁定 (OVLO) 和迟滞
- 初始插入计时器可使振铃和瞬变在系统连接之后消除
- 可编程故障计时器可避免干扰性跳变
- 高电平有效、开漏电源正常状态输出
- 提供故障锁存和自动重启版本
- 10 引脚 VSSOP 封装

2 应用

- 服务器背板系统
- 基站配电系统
- 固态断路器
- 24V 和 48V 工业系统

3 说明

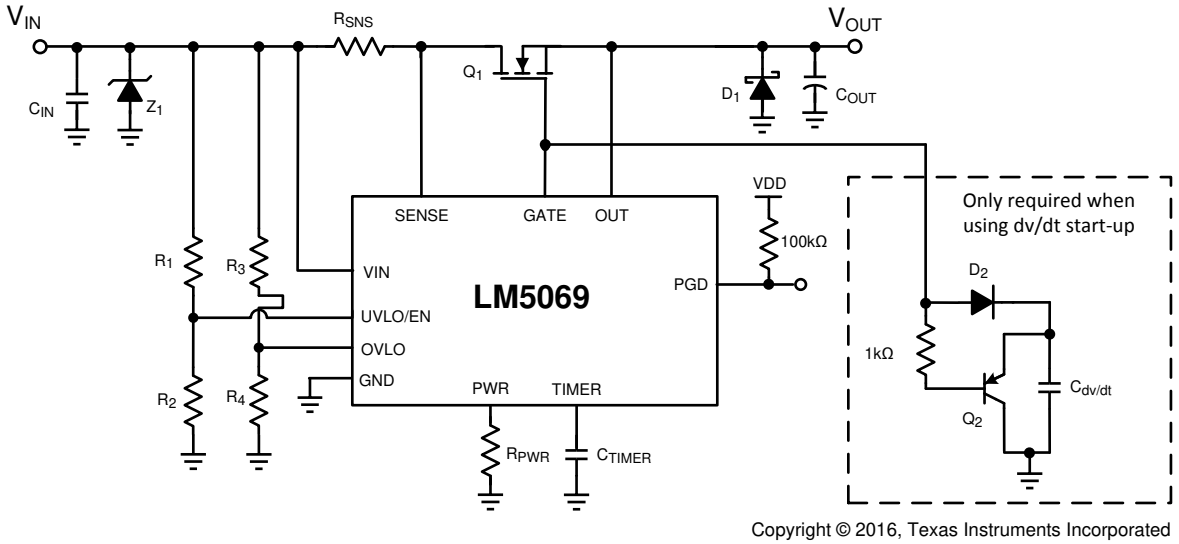
LM5069 正电压热插拔控制器可在从带电系统背板或其他热插拔电源插入和移除电路板期间，为电源连接提供智能控制。LM5069 可提供浪涌电流控制以限制系统电压下降和瞬变。外部串行导通 N 沟道 MOSFET 中的电流限制和功率耗散可进行编程，从而确保其在安全工作区 (SOA) 内工作。当输出电压低于 1.25V 输入电压时，会显示电源正常输出。输入欠压和过压锁定电平和迟滞，以及初始插入延迟时间和故障监测时间均可进行编程。在故障监测之后 LM5069-1 闭锁，同时 LM5069-2 以固定占空比自动重启。LM5069 采用 10 引脚 VSSOP 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM5069	VSSOP (10)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (February 2019) to Revision G **Page**

- Added *Device Comparison* table ... 3

Changes from Revision E (November 2016) to Revision F **Page**

- Updated the *Absolute Maximum Ratings* section ... 4

Changes from Revision D (May 2013) to Revision E **Page**

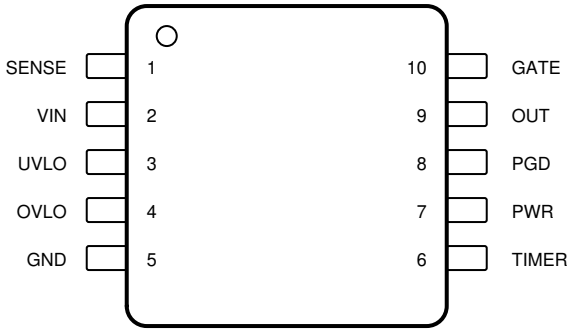
- 已添加 *ESD 额定值表，特性 说明* 部分，*器件功能模式，应用和实施*部分，*电源建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- Added *Thermal Information* table ... 4

5 Device Comparison

DEVICE NUMBER	RETRY BEHAVIOR AFTER FAULT	PACKAGE
LM5069-1	Latch Off on Fault	VSSOP (10)
LM5069-2	Auto Retry on Fault	

6 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SENSE	I	Current sense input: The voltage across the current sense resistor (R_S) is measured from VIN to this pin. If the voltage across R_S reaches 55 mV the load current is limited and the fault timer activates.
2	VIN	I	Positive supply input: A small ceramic bypass capacitor close to this pin is recommended to suppress transients which occur when the load current is switched off.
3	UVLO	I	Undervoltage lockout: An external resistor divider from the system input voltage sets the undervoltage turnon threshold. An internal 21-µA current source provides hysteresis. The enable threshold at the pin is 2.5 V. This pin can also be used for remote shutdown control.
4	OVLO	I	Overvoltage lockout: An external resistor divider from the system input voltage sets the overvoltage turnoff threshold. An internal 21-µA current source provides hysteresis. The disable threshold at the pin is 2.5 V.
5	GND	—	Circuit ground
6	TIMER	I/O	Timing capacitor: An external capacitor connected to this pin sets the insertion time delay and the fault timeout period. The capacitor also sets the restart timing of the LM5069-2.
7	PWR	I	Power limit set: An external resistor connected to this pin, in conjunction with the current sense resistor (R_S), sets the maximum power dissipation allowed in the external series pass MOSFET.
8	PGD	O	Power Good indicator: An open drain output. When the external MOSFET V_{DS} decreases below 1.25 V, the PGD indicator is active (high). When the external MOSFET V_{DS} increases above 2.5 V the PGD indicator switches low.
9	OUT	I	Output feedback: Connect to the output rail (external MOSFET source). Internally used to determine the MOSFET V_{DS} voltage for power limiting, and to control the PGD indicator.
10	GATE	O	Gate drive output: Connect to the external MOSFET's gate. This pin's voltage is typically 12 V above the OUT pin when enabled.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
VIN to GND(3)	–0.3	100	V
SENSE, OUT, and PGD to GND	–0.3	100	V
GATE to GND(3)	–0.3	100	V
OUT to GND (1 -ms transient) (4)	–1	100	V
UVLO to GND	–0.3	100	V
OVLO to GND	–0.3	7	V
VIN to SENSE	–0.3	0.3	V
Maximum junction temperature, T_{JMAX}		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The GATE pin voltage is typically 12 V above VIN when the LM5069 is enabled. Therefore, the Absolute Maximum Ratings for VIN (100 V) applies only when the LM5069 is disabled, or for a momentary surge to that voltage because the Absolute Maximum Rating for the GATE pin is also 100 V.
(4) Select external MOSFET with VGS(th) voltage higher than V_{OUT} during -ve transient. This avoids MOSFET getting turned-ON during -ve transient.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±500	

(1) The Human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VIN	Supply voltage	9	80	V
	PGD off voltage	0	80	V
T_J	Junction temperature	–40	125	°C

(1) For detailed information on soldering plastic VSSOP packages, see *Absolute Maximum Ratings for Soldering* (SNOA549) available from Texas Instruments.

7.4 Thermal Information

THERMAL METRIC(1)		LM5069 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	156	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	74.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Minimum and maximum limits are specified through test, design, or statistical correlation at T_J= –40°C to 125°C. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only. VIN = 48 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (VIN PIN)						
I_{IN-EN}	Input current, enabled	UVLO > 2.5 V and OVLO < 2.5 V		1.3	1.6	mA
I_{IN-DIS}	Input current, disabled	UVLO < 2.5 V or OVLO > 2.5 V		480	650	µA
POR_{IT}	Power-On reset threshold at VIN to trigger insertion timer	VIN increasing		7.6	8	V
POR_{EN}	Power-On reset threshold at VIN to enable all functions	VIN increasing		8.4	9	V
POR_{EN-HYS}	POR_{EN} hysteresis	VIN decreasing		90		mV
OUT PIN						
I_{OUT-EN}	OUT bias current, enabled	OUT = VIN, Normal operation		11		µA
$I_{OUT-DIS}$	OUT bias current, disabled (1)	Disabled, OUT = 0 V, SENSE = VIN		50		
UVLO, OVLO PINS						
$UVLO_{TH}$	UVLO threshold		2.45	2.5	2.55	V
$UVLO_{HYS}$	UVLO hysteresis current	UVLO = 1 V	12	21	30	µA
$UVLO_{DEL}$	UVLO delay	Delay to GATE high		55		µs
		Delay to GATE low		11		
$UVLO_{BIAS}$	UVLO bias current	UVLO = 48 V			1	µA
$OVLO_{TH}$	OVLO threshold		2.4	2.5	2.6	V
$OVLO_{HYS}$	OVLO hysteresis current	OVLO = 2.6 V	12	21	30	µA
$OVLO_{DEL}$	OVLO delay	Delay to GATE high		55		µs
		Delay to GATE low		11		
$OVLO_{BIAS}$	OVLO bias current	OVLO = 2.4 V			1	µA
POWER LIMIT (PWR PIN)						
PWR_{LIM-1}	Power limit sense voltage (VIN-SENSE)	SENSE-OUT = 48 V, R_{PWR} = 150 kΩ	19	25	31	mV
PWR_{LIM-2}		SENSE-OUT = 24 V, R_{PWR} = 75 kΩ		25		mV
I_{PWR}	PWR pin current	V_{PWR} = 2.5 V		20		µA
GATE CONTROL (GATE PIN)						
I_{GATE}	Source current	Normal operation, GATE-OUT = 5 V	10	16	22	µA
	Sink current	UVLO < 2.5 V	1.75	2	2.6	mA
		VIN to SENSE = 150 mV or VIN < POR_{IT}, V_{GATE} = 5 V	45	110	175	mA
V_{GATE}	Gate output voltage in normal operation	GATE-OUT voltage	11.4	12	12.6	V

(1) OUT bias current (disabled) due to leakage current through an internal 1-MΩ resistance from SENSE to VOUT.

Electrical Characteristics (continued)

Minimum and maximum limits are specified through test, design, or statistical correlation at T_J= –40°C to 125°C. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only. VIN = 48 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
V_{CL}	Threshold voltage	VIN-SENSE voltage	48.5	55	61.5	mV
t_{CL}	Response time	VIN-SENSE stepped from 0 mV to 80 mV		45		µs
I_{SENSE}	SENSE input current	Enabled, SENSE = OUT		23		µA
		Disabled, OUT = 0 V		60		
CIRCUIT BREAKER						
V_{CB}	Threshold voltage	VIN to SENSE	80	105	130	mV
t_{CB}	Response time	VIN to SENSE stepped from 0 mV to 150 mV, time to GATE low, no load		0.44	1.2	µs
TIMER (TIMER PIN)						
V_{TMRH}	Upper threshold		3.76	4	4.16	V
V_{TMRL}	Lower threshold	Restart cycles (LM5069-2)	1.187	1.25	1.313	V
		End of 8th cycle (LM5069-2)		0.3		V
		Re-enable Threshold (LM5069-1)		0.3		V
I_{TIMER}	Insertion time current		3	5.5	8	µA
	Sink current, end of insertion time	TIMER pin = 2 V	1	1.5	2	mA
	Fault detection current		51	85	120	µA
	Fault sink current		1.25	2.5	3.75	µA
DC_{FAULT}	Fault restart duty cycle	LM5069-2 only		0.5%		
t_{FAULT}	Fault to GATE low delay	TIMER pin reaches 4 V		12		µs
POWER GOOD (PGD PIN)						
PGD_{TH}	Threshold measured at SENSE-OUT	Decreasing	0.67	1.25	1.85	V
		Increasing, relative to decreasing threshold	0.95	1.25	1.55	
PGD_{VOL}	Output low voltage	I_{SINK} = 2 mA		60	150	mV
PGD_{IOH}	Off leakage current	V_{PGD} = 80 V			5	µA

7.6 Typical Characteristics

T_J = 25°C and V_{IN} = 48 V (unless otherwise noted)

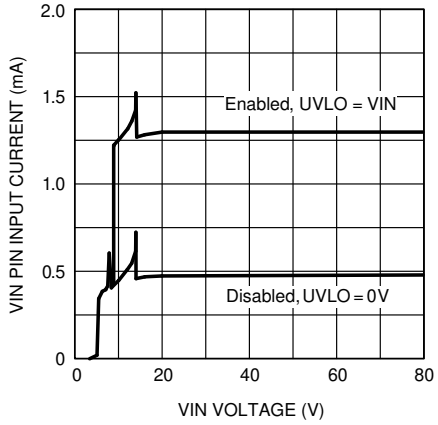


Figure 1. VIN Pin Input Current vs VIN

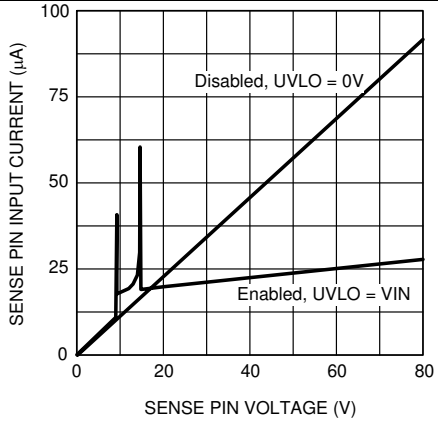


Figure 2. SENSE Pin Input Current

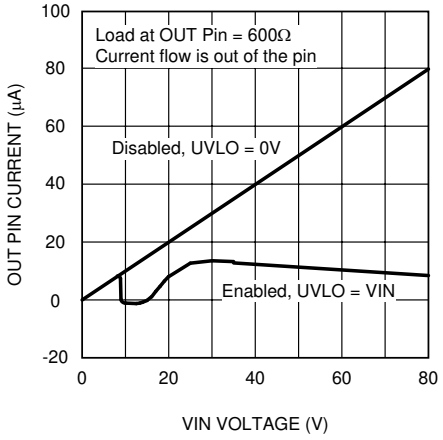


Figure 3. OUT Pin Current

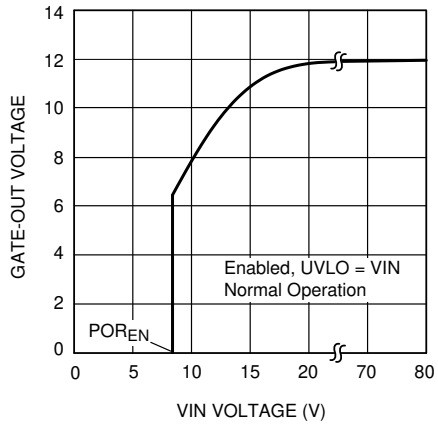


Figure 4. GATE Pin Voltage vs V_{IN}

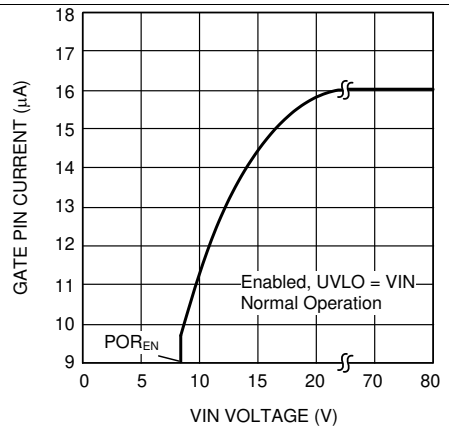


Figure 5. GATE Pin Source Current vs V_{IN}

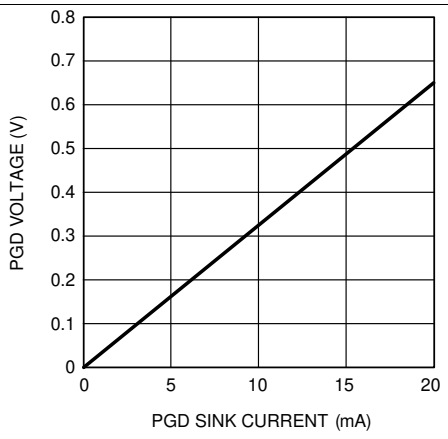


Figure 6. PGD Pin Low Voltage vs Sink Current

Typical Characteristics (continued)

T_J = 25°C and V_{IN} = 48 V (unless otherwise noted)

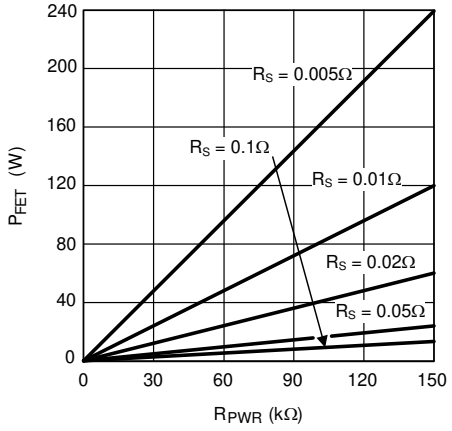


Figure 7. MOSFET Power Dissipation Limit vs R_{PWR} and R_S

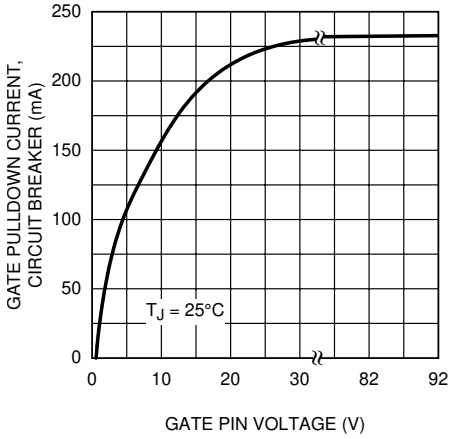


Figure 8. GATE Pulldown Current, Circuit Breaker vs GATE Voltage

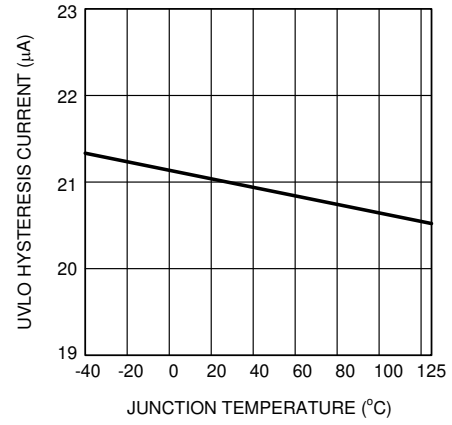


Figure 9. UVLO Hysteresis Current vs Temperature

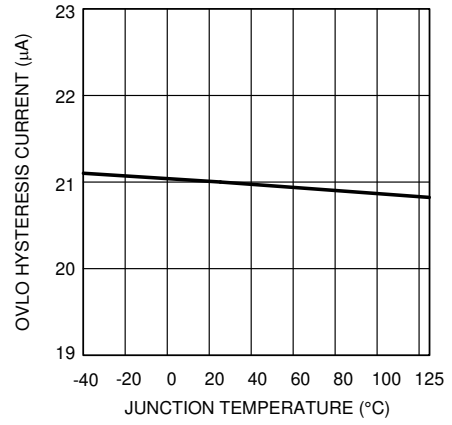


Figure 10. OVLO Hysteresis Current vs Temperature

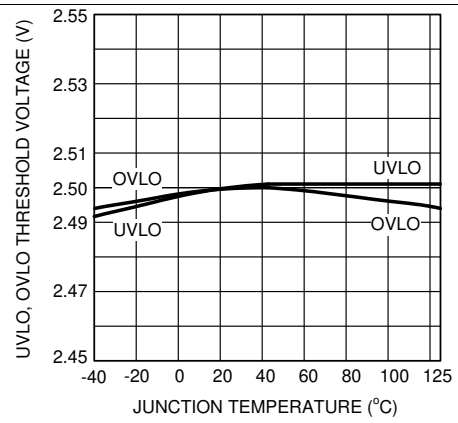


Figure 11. UVLO, OVLO Threshold vs Temperature

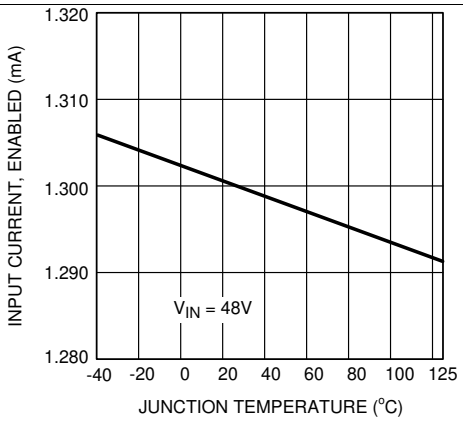


Figure 12. Input Current, Enabled vs Temperature

Typical Characteristics (continued)

T_J = 25°C and V_{IN} = 48 V (unless otherwise noted)

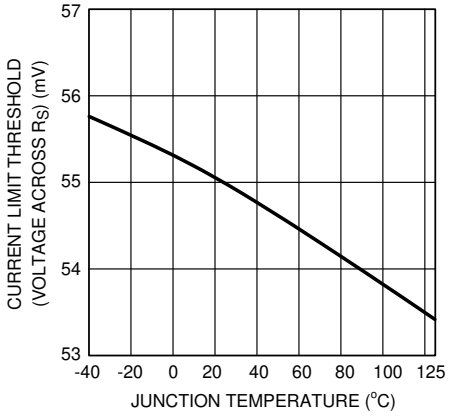


Figure 13. Current Limit Threshold vs Temperature

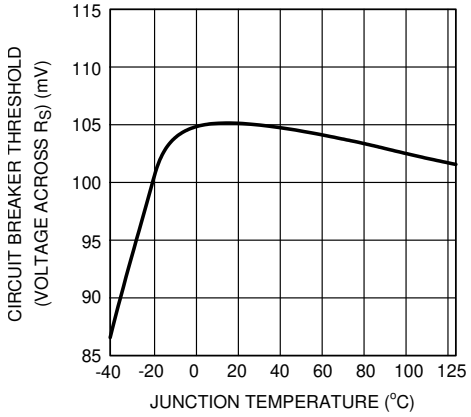


Figure 14. Circuit Breaker Threshold vs Temperature

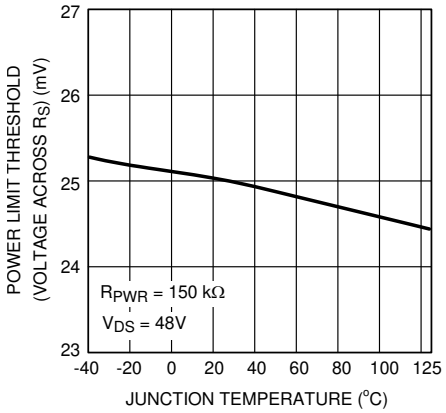


Figure 15. Power Limit Threshold vs Temperature

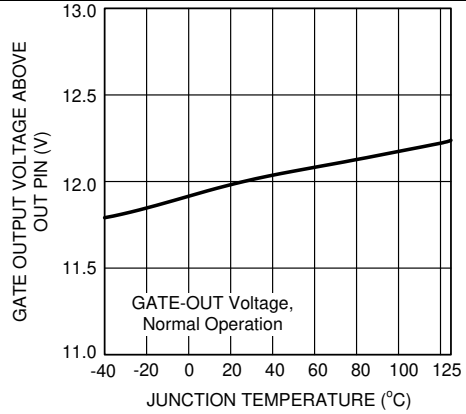


Figure 16. GATE Output Voltage vs Temperature

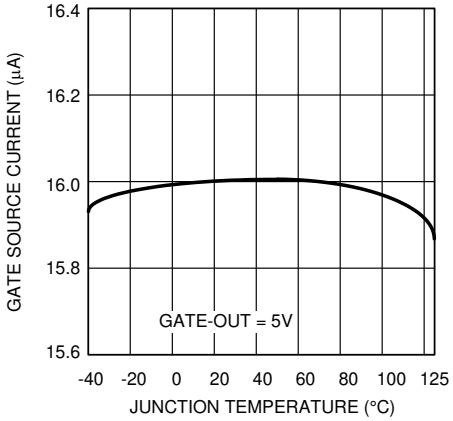


Figure 17. GATE Source Current vs Temperature

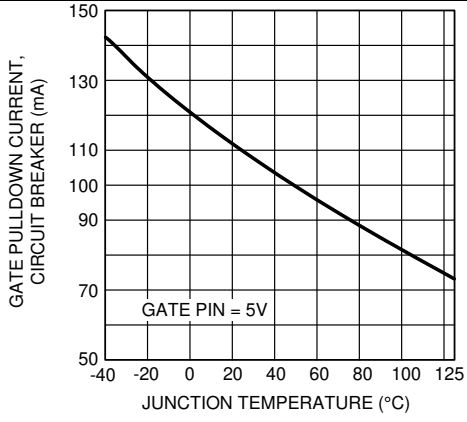


Figure 18. GATE Pulldown Current, Circuit Breaker vs Temperature

Typical Characteristics (continued)

T_J = 25°C and V_{IN} = 48 V (unless otherwise noted)

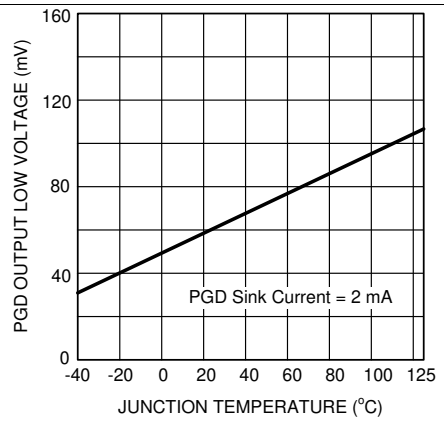


Figure 19. PGD Low Voltage vs Temperature

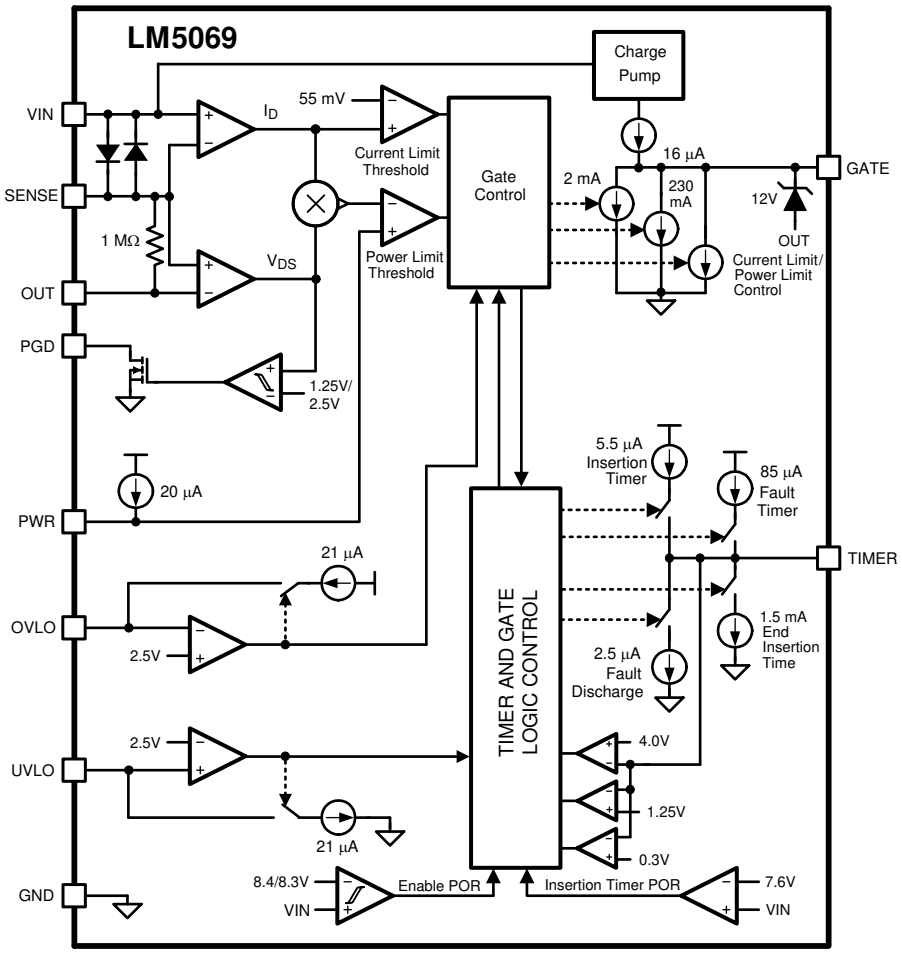
8 Detailed Description

8.1 Overview

The inline protection functionality of the LM5069 is designed to control the in-rush current to the load upon insertion of a circuit card into a live backplane or other hot power source, thereby limiting the voltage sag on the backplane's supply voltage and the dV/dt of the voltage applied to the load. Effects on other circuits in the system are minimized, preventing possible unintended resets. A controlled shutdown when the circuit card is removed can also be implemented using the LM5069.

In addition to a programmable current limit, the LM5069 monitors and limits the maximum power dissipation in the series pass device to maintain operation within the device Safe Operating Area (SOA). Either current limiting or power limiting for an extended period of time results in the shutdown of the series pass device. In this event, the LM5069-1 latches off while the LM5069-2 retries an infinite number of times to recover after the fault is removed. The circuit breaker function quickly switches off the series pass device upon detection of a severe overcurrent condition. Programmable undervoltage lockout (UVLO) and overvoltage lockout (OVLO) circuits shut down the LM5069 when the system input voltage is outside the desired operating range.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Current Limit

The current limit threshold is reached when the voltage across the sense resistor R_S (VIN to SENSE) reaches 55 mV. In the current limiting condition, the GATE voltage is controlled to limit the current in MOSFET Q1. While the current limit circuit is active, the fault timer is active as described in *Fault Timer and Restart*. If the load current falls below the current limit threshold before the end of the fault timeout period, the LM5069 resumes normal operation. For proper operation, the R_S resistor value must be no larger than 100 mΩ.

8.3.2 Circuit Breaker

If the load current increases rapidly (for example, the load is short-circuited) the current in the sense resistor (R_S) may exceed the current limit threshold before the current limit control loop is able to respond. If the current exceeds twice the current limit threshold (105 mV/R_S), Q1 is quickly switched off by the 230-mA pulldown current at the GATE pin, and a fault timeout period begins. When the voltage across R_S falls below 105 mV the 230-mA pulldown current at the GATE pin is switched off, and the gate voltage of Q1 is then determined by the current limit or the power limit functions. If the TIMER pin reaches 4 V before the current limiting or power limiting condition ceases, Q1 is switched off by the 2-mA pulldown current at the GATE pin as described in *Fault Timer and Restart*.

8.3.3 Power Limit

An important feature of the LM5069 is the MOSFET power limiting. The Power Limit function can be used to maintain the maximum power dissipation of MOSFET Q1 within the device SOA rating. The LM5069 determines the power dissipation in Q1 by monitoring its drain-source voltage (SENSE to OUT), and the drain current through the sense resistor (VIN to SENSE). The product of the current and voltage is compared to the power limit threshold programmed by the resistor at the PWR pin. If the power dissipation reaches the limiting threshold, the GATE voltage is modulated to reduce the current in Q1. While the power limiting circuit is active, the fault timer is active as described in *Fault Timer and Restart*.

8.3.4 Undervoltage Lockout (UVLO)

The series pass MOSFET (Q1) is enabled when the input supply voltage (V_{SYS}) is within the operating range defined by the programmable undervoltage lockout (UVLO) and overvoltage lockout (OVLO) levels. Typically the UVLO level at V_{SYS} is set with a resistor divider (R1-R3) as shown in Figure 30. When V_{SYS} is below the UVLO level, the internal 21-µA current source at UVLO is enabled, the current source at OVLO is off, and Q1 is held off by the 2-mA pulldown current at the GATE pin. As V_{SYS} is increased, raising the voltage at UVLO above 2.5 V, the 21-µA current source at UVLO is switched off, increasing the voltage at UVLO, providing hysteresis for this threshold. With the UVLO pin above 2.5 V, Q1 is switched on by the 16-µA current source at the GATE pin if the insertion time delay has expired (Figure 22). See *Application and Implementation* for a procedure to calculate the values of the threshold setting resistors (R1-R3). The minimum possible UVLO level at V_{SYS} can be set by connecting the UVLO pin to VIN. In this case Q1 is enabled when the VIN voltage reaches the POR_{EN} threshold.

8.3.5 Overvoltage Lockout (OVLO)

The series pass MOSFET (Q1) is enabled when the input supply voltage (V_{SYS}) is within the operating range defined by the programmable undervoltage lockout (UVLO) and overvoltage lockout (OVLO) levels. If V_{SYS} raises the OVLO pin voltage above 2.5 V, Q1 is switched off by the 2-mA pulldown current at the GATE pin, denying power to the load. When the OVLO pin is above 2.5 V, the internal 21-µA current source at OVLO is switched on, raising the voltage at OVLO to provide threshold hysteresis. When V_{SYS} is reduced below the OVLO level Q1 is enabled. See *Application and Implementation* for a procedure to calculate the threshold setting resistor values.

8.3.6 Power Good Pin

During turnon, the Power Good pin (PGD) is high until the voltage at VIN increases above ≅ 5 V. PGD then switches low, remaining low as the VIN voltage increases. When the voltage at OUT increases to within 1.25 V of the SENSE pin (V_{DS} <1.25 V), PGD switches high. PGD switches low if the V_{DS} of Q1 increases above 2.5 V. A pullup resistor is required at PGD as shown in Figure 20. The pullup voltage (V_{PGD}) can be as high as 80 V, with transient capability to 100 V, and can be higher or lower than the voltages at VIN and OUT.

Feature Description (continued)

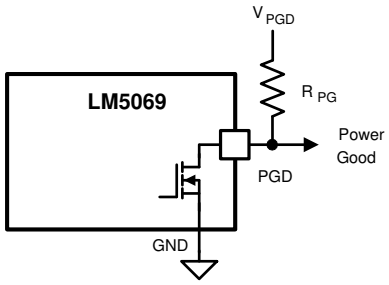


Figure 20. Power Good Output

If a delay is required at PGD, suggested circuits are shown in Figure 21. In Figure 21a, capacitor C_{PG} adds delay to the rising edge, but not to the falling edge. In Figure 21b, the rising edge is delayed by R_{PG1} + R_{PG2} and C_{PG}, while the falling edge is delayed a lesser amount by R_{PG2} and C_{PG}. Adding a diode across R_{PG2} (Figure 21c) allows for equal delays at the two edges, or a short delay at the rising edge and a long delay at the falling edge.

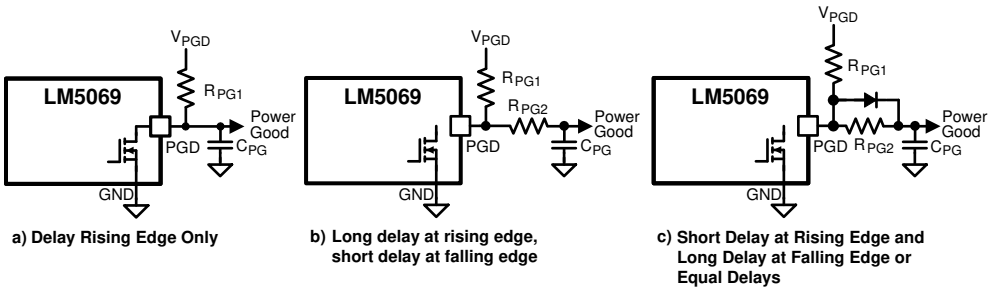


Figure 21. Adding Delay to the Power Good Output Pin

8.4 Device Functional Modes

The LM5069 hot swap controller has a power up sequence which can be broken down into 3x distinct sections: Insertion Time, In-Rush Limiting, and Normal Operation. Once the device reaches normal operation, the GATE and TIMER behavior depends on whether a fault condition is present or not on the output.

8.4.1 Power Up Sequence

The VIN operating range of the LM5069 is 9 V to 80 V, with a transient capability to 100 V. See *Functional Block Diagram* and Figure 22, as the voltage at VIN initially increases, the external N-channel MOSFET (Q1) is held off by an internal 230-mA pulldown current at the GATE pin. The strong pulldown current at the GATE pin prevents an inadvertent turnon as the MOSFET's gate-to-drain (Miller) capacitance is charged. Additionally, the TIMER pin is initially held at ground. When the VIN voltage reaches the POR_{IT} threshold (7.6 V) the insertion time begins. During the insertion time, the capacitor at the TIMER pin (C_T) is charged by a 5.5-µA current source, and Q1 is held off by a 2-mA pulldown current at the GATE pin regardless of the VIN voltage. The insertion time delay allows ringing and transients at VIN to settle before Q1 can be enabled. The insertion time ends when the TIMER pin voltage reaches 4 V. C_T is then quickly discharged by an internal 1.5-mA pulldown current. After the insertion time, the LM5069 control circuitry is enabled when VIN reaches the POR_{EN} threshold (8.4 V). The GATE pin then switches on Q1 when V_{SYS} exceeds the UVLO threshold (UVLO pin >2.5 V). If V_{SYS} is above the UVLO threshold at the end of the insertion time, Q1 switches on at that time. The GATE pin charge pump sources 16 µA to charge Q1's gate capacitance. The maximum gate-to-source voltage of Q1 is limited by an internal 12-V Zener diode.

Device Functional Modes (continued)

As the voltage at the OUT pin increases, the LM5069 monitors the drain current and power dissipation of MOSFET Q1. In-rush current limiting and/or power limiting circuits actively control the current delivered to the load. During the in-rush limiting interval (t2 in Figure 22) an internal 85-µA fault timer current source charges C_T. If Q1's power dissipation and the input current reduce below their respective limiting thresholds before the TIMER pin reaches 4 V, the 85-µA current source is switched off, and C_T is discharged by the internal 2.5-µA current sink (t3 in Figure 22). The in-rush limiting interval is complete when the voltage at the OUT pin increases to within 1.25 V of the input voltage (V_{SYS}), and the PGD pin switches high.

If the TIMER pin voltage reaches 4 V before in-rush current limiting or power limiting ceases (during t2), a fault is declared and Q1 is turned off. See *Fault Timer and Restart* for a complete description of the fault mode.

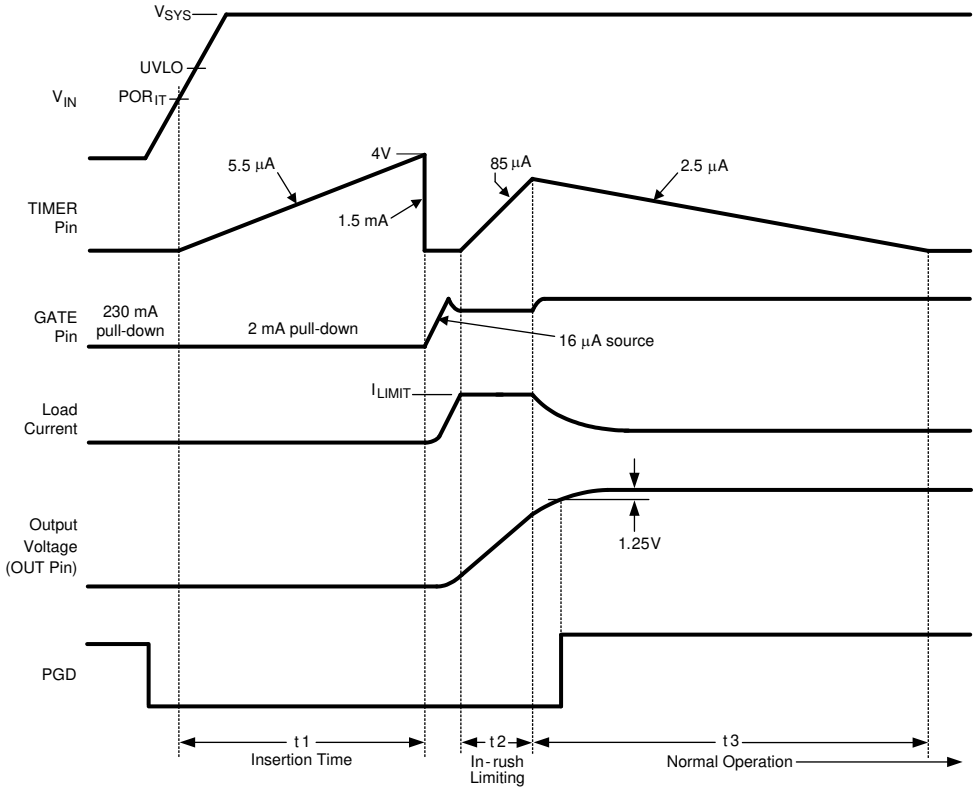


Figure 22. Power-Up Sequence (Current Limit Only)

8.4.2 Gate Control

A charge pump provides internal bias voltage above the output voltage (OUT pin) to enhance the N-Channel MOSFET's gate. The gate-to-source voltage is limited by an internal 12-V Zener diode. During normal operating conditions (t3 in Figure 22) the gate of Q1 is held charged by an internal 16-µA current source to approximately 12 V above OUT. If the maximum V_{GS} rating of Q1 is less than 12 V, an external Zener diode of lower voltage must be added between the GATE and OUT pins. The external Zener diode must have a forward current rating of at least 250 mA.

When the system voltage is initially applied, the GATE pin is held low by a 230-mA pulldown current. This helps prevent an inadvertent turnon of the MOSFET through its drain-gate capacitance as the applied system voltage increases.

During the insertion time (t1 in Figure 22) the GATE pin is held low by a 2-mA pulldown current. This maintains Q1 in the off-state until the end of t1, regardless of the voltage at VIN or UVLO.

Following the insertion time, during t2 in Figure 22, the gate voltage of Q1 is modulated to keep the current or power dissipation level from exceeding the programmed levels. While in the current or power limiting mode the TIMER pin capacitor is charging. If the current and power limiting cease before the TIMER pin reaches 4 V the TIMER pin capacitor then discharges, and the circuit enters normal operation.

Device Functional Modes (continued)

If the in-rush limiting condition persists such that the TIMER pin reached 4 V during t2, the GATE pin is then pulled low by the 2-mA pulldown current. The GATE pin is then held low until either a power-up sequence is initiated (LM5069-1), or until the end of the restart sequence (LM5069-2). See *Fault Timer and Restart*.

If the system input voltage falls below the UVLO threshold, or rises above the OVLO threshold, the GATE pin is pulled low by the 2-mA pulldown current to switch off Q1.

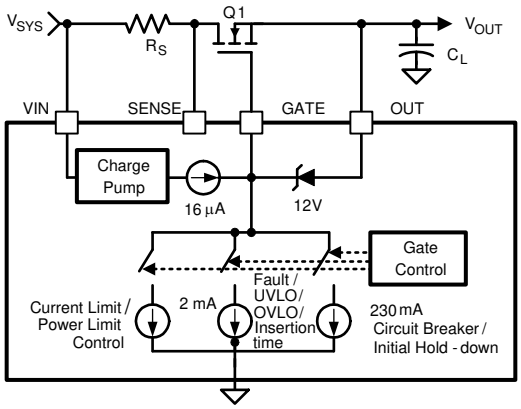


Figure 23. Gate Control

8.4.3 Fault Timer and Restart

When the current limit or power limit threshold is reached during turnon or as a result of a fault condition, the gate-to-source voltage of Q1 is modulated to regulate the load current and power dissipation. When either limiting function is activated, an 85-µA fault timer current source charges the external capacitor (C_T) at the TIMER pin as shown in Figure 25 (fault timeout period). If the fault condition subsides during the fault timeout period before the TIMER pin reaches 4 V, the LM5069 returns to the normal operating mode and C_T is discharged by the 2.5-µA current sink. If the TIMER pin reaches 4 V during the fault timeout period, Q1 is switched off by a 2-mA pulldown current at the GATE pin. The subsequent restart procedure then depends on which version of the LM5069 is in use.

The LM5069-1 latches the GATE pin low at the end of the fault timeout period. C_T is then discharged to ground by the 2.5-µA fault current sink. The GATE pin is held low by the 2-mA pulldown current until a power-up sequence is externally initiated by cycling the input voltage (V_{SYS}), or momentarily pulling the UVLO pin below 2.5 V with an open-collector or open-drain device as shown in Figure 24. The voltage at the TIMER pin must be <0.3 V for the restart procedure to be effective.

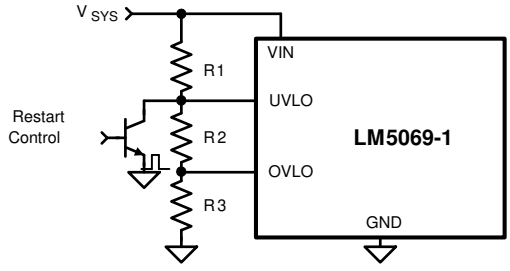


Figure 24. Latched Fault Restart Control

The LM5069-2 provides an automatic restart sequence which consists of the TIMER pin cycling between 4 V and 1.25 V seven times after the fault timeout period, as shown in Figure 25. The period of each cycle is determined by the 85-µA charging current, and the 2.5-µA discharge current, and the value of the capacitor C_T. When the TIMER pin reaches 0.3 V during the eighth high-to-low ramp, the 16-µA current source at the GATE pin turns on Q1. If the fault condition is still present, the fault timeout period and the restart cycle repeat.

Device Functional Modes (continued)

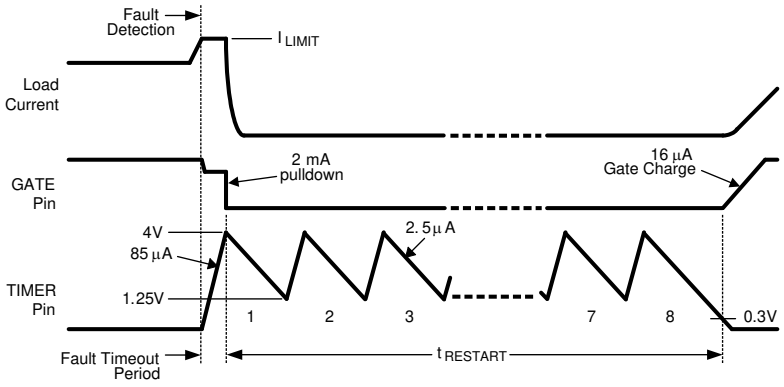


Figure 25. Restart Sequence (LM5069-2)

8.4.4 Shutdown Control

The load current can be remotely switched off by taking the UVLO pin below its 2.5-V threshold with an open collector or open-drain device, as shown in Figure 26. Upon releasing the UVLO pin the LM5069 switches on the load current with in-rush current and power limiting.

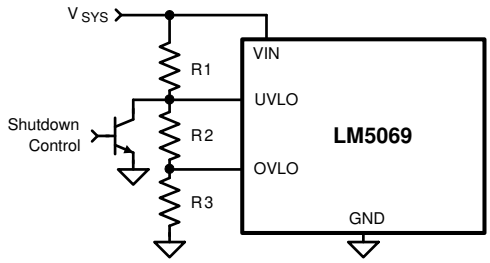


Figure 26. Shutdown Control

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM5069 is a hot swap controller which is used to manage inrush current and protect in case of faults. When designing a hot swap, three key scenarios must be considered:

- Start-up
- Output of a hot swap is shorted to ground when the hot swap is on. This is often referred to as a hot-short.
- Powering up a board when the output and ground are shorted. This is usually called a start-into-short.

All of these scenarios place a lot of stress on the hot swap MOSFET and thus special care is required when designing the hot swap circuit to keep the MOSFET within its SOA (Safe Operating Area). Detailed design examples are provided in the following sections. Solving all of the equations by hand is cumbersome and can result in errors. Instead, TI recommends using the LM5069 Design Calculator provided on the product page.

9.2 Typical Application

9.2.1 48-V, 10-A Hot Swap Design

This section describes the design procedure for a 48-V, 10-A hot swap design.

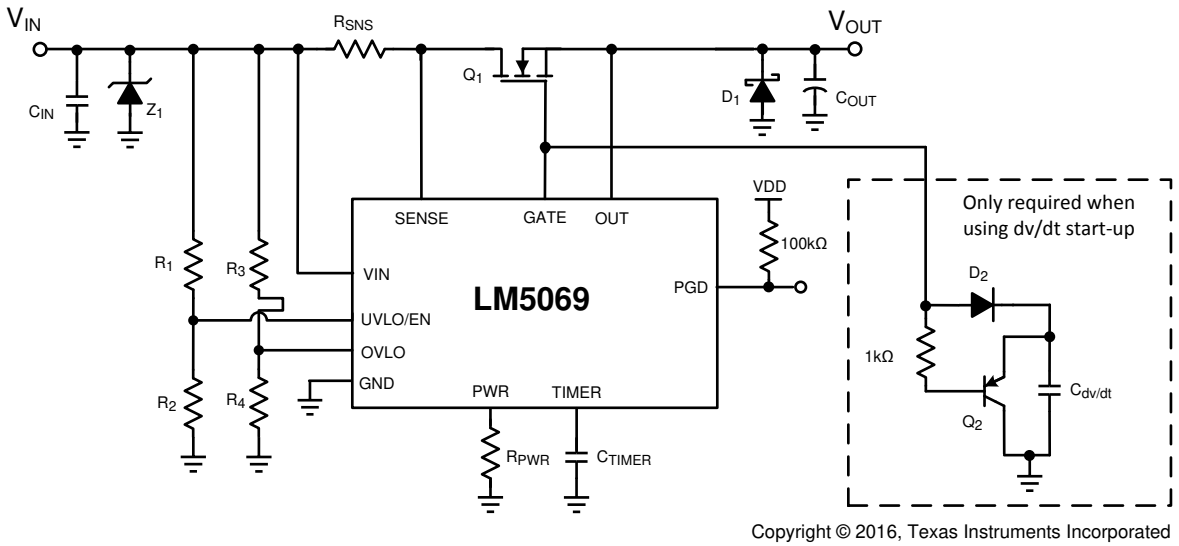


Figure 27. Typical Application Schematic

9.2.1.1 Design Requirements

Table 1 summarizes the design parameters that must be known before designing a hot swap circuit. When charging the output capacitor through the hot swap MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor (½CV^2). Thus, both the input voltage and output capacitance determine the stress experienced by the MOSFET. The maximum load current drives the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and the thermal properties of

Typical Application (continued)

the PCB ($R_{\theta CA}$) drive the selection of the MOSFET R_{DSON} and the number of MOSFETs used. $R_{\theta CA}$ is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET. Note that the drain is not electrically connected to the ground plane and thus the ground plane cannot be used to help with heat dissipation. For this design example $R_{\theta CA}$ = 30°C/W is used, which is similar to the LM5069 EVM. It's a good practice to measure the $R_{\theta CA}$ of a given design after the physical PCBs are available.

Finally, it's important to understand what test conditions the hot swap must pass. In general, a hot swap is designed to pass both a *Hot-Short* and a *Start into a Short*. Also, TI recommends keeping the load OFF until the hot swap is fully powered up. Starting the load early causes unnecessary stress on the MOSFET and could lead to MOSFET failures or a failure to start-up.

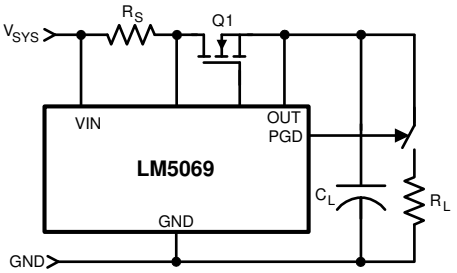


Figure 28. No Load Current During Turnon

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage range	18 to 30 V
Maximum load current	10 A
Lower UVLO threshold	17 V
Upper UVLO threshold	18 V
Lower OVLO threshold	30 V
Upper OVLO threshold	31 V
Maximum output capacitance of the hot swap	330 µF
Maximum ambient temperature	55°C
MOSFET RθCA (function of layout)	30°C/W
Pass *Hot-short* on output?	Yes
Pass a *Start into short*?	Yes
Is the load off until PG asserted?	Yes
Can a hot board be plugged back in?	No

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Select R_{SNS} and CL setting

The LM5069 monitors the current in the external MOSFET (Q1) by measuring the voltage across the sense resistor (RS), connected from VIN to SENSE. When the voltage difference across the VIN and SENSE pins (VCL) is greater than 55 mV (typical), the LM5069 begins modulating the MOSFET gate. Size R_{SNS} for maximum or minimum V_{CL} for applications that require ensured shutoff or ensured conduction. R_{SNS} is sized to exhibit minimum V_{CL} across R_{SNS} at maximum load current in Equation 1.

$$R_{SNS} = \frac{V_{CL,MIN}}{I_{LIM}} = \frac{48.5\,mV}{10\,A} = 0.00485\,\Omega \quad (1)$$

Typically sense resistors are only available in discrete value. We choose the next smallest discrete value, 4 mΩ. If a precise current limit is desired, a sense resistor along with a resistor divider can be used as shown in Figure 29.

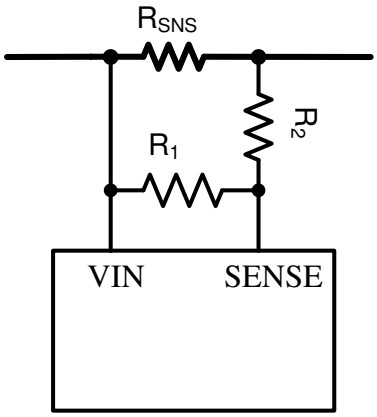


Figure 29. SENSE Resistor Divider

If using a resistor divider, then the next larger available sense resistor must be chosen (5 mΩ in this example). The ratio of R1 and R2 can then be calculated with Equation 2.

$$\frac{R_1}{R_2} = \frac{R_{SNS,CLC}}{R_{SNS} - R_{SNS,CLC}} = \frac{4.8\,m\Omega}{5m\Omega - 4.8\,m\Omega} = 24 \tag{2}$$

Note that the SENSE pin pulls 23 µA of current, which creates an offset across R2. TI recommends keeping R2 below 10 Ω to reduce the offset that this introduces. In addition, the 1% resistors add to the current monitoring error. Finally, if the resistor divider approach is used, compute the effective sense resistance ($R_{SNS,\ EFF}$) using Equation 3 and use that in all equations instead of R_{SNS}.

$$R_{SNS,EFF} = \frac{R_{SNS} \times R_1}{R_1 + R_2} \tag{3}$$

Note that for many applications, a precise current limit may not be required. In that case, it's simpler to pick the next smaller available sense resistor.

9.2.1.2.2 Selecting the Hot Swap FET(s)

It is critical to select the correct MOSFET for a hot swap design. The device must meet the following requirements:

- The V_{DS} rating must be sufficient to handle the maximum system voltage along with any ringing caused by transients.
- The SOA of the FET must be sufficient to handle all usage cases: start-up, hot-short, start into short.
- R_{DSON} must be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, TI recommends keeping the steady state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating must be above the maximum load current and the pulsed drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements also pass these two.

For this design the SUM40N15-38 was selected. After selecting the MOSFET, the maximum steady state case temperature can be computed as Equation 4.

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times R_{DSON,MAX}\,(T_J) \tag{4}$$

Note that the R_{DSON} is a strong function of junction temperature, which for most MOSFETs is close to the case temperature. A few iterations of the above equations may be necessary to converge on the final R_{DSON} and $T_{C,MAX}$ value. According to the CSD19536KTT datasheet, its R_{DSON} is approximately 1.2× at 65°C. Equation 5 uses this R_{DSON} value to compute the $T_{C,MAX}$.

$$T_{C,MAX} = 55°C + 30° \frac{C}{W} \times (10\,A)^2 \times (1.2 \times 2.4\,m\Omega) = 63.64°C \tag{5}$$

This maximum steady state case temperature does not indicate that a second MOSFET may be required to reduce and distribute power dissipation during normal operation.

As an aside, when using parallel MOSFETs, the maximum steady state case temperature can be computed in Equation 6.

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times \left(\frac{I_{LOAD,MAX}}{\#\,of\,MOSFETs} \right)^2 \times R_{DSON}\,(T_J) \tag{6}$$

Iterate until the computed $T_{C,MAX}$ is using two parallel MOSFETs is less than to the junction temperature assumed for R_{DSON}. Then, no further iterations are necessary.

9.2.1.2.3 Select Power Limit

In general, a lower-power limit setting is preferred to reduce the stress on the MOSFET. However, when the LM5069 is set to a very low power limit setting, it has to regulate the FET current and hence the voltage across the sense resistor (V_{SNS}) to a very low value. V_{SNS} can be computed as shown in Equation 7.

$$V_{SNS} = \frac{P_{LIM} \times R_{SNS}}{V_{DS}} \tag{7}$$

To avoid significant degradation of the power limiting accuracy, a V_{SNS} of less than 5 mV is not recommended. Based on this requirement the minimum allowed power limit can be computed in Equation 8.

$$P_{LIM,MIN} = \frac{V_{SNS,MIN} \times V_{IN,MAX}}{R_{SNS}} = \frac{5\,mV \times 30\,V}{4\,m\Omega} = 37.5\,W \tag{8}$$

To avoid significant degradation of the power limiting accuracy a VSNS of less than 5 mV is not recommended. Based on this requirement, the minimum allowed power limit can be computed with Equation 9.

$$R_{PWR} = 1.30 \times 10^5 \times R_{SNS}\,(P_{LIM} - 1.18\,mV \times \frac{V_{DS}}{R_{SNS}}) \tag{9}$$

Note that the minimum R_{PWR} would occur when V_{DS} = $V_{IN,MAX}$. We can then compute the minimum R_{PWR} with Equation 10.

$$R_{PWR} = 1.30 \times 10^5 \times 4\,m\Omega \left(37.5\,W - 1.18\,mV \times \frac{30\,V}{4\,m\Omega} \right) = 14.9\,k\Omega \tag{10}$$

To obtain the smallest accurate power limit, the next largest available resistor must be selected. In this case a 15.8-kΩ resistor was chosen, which sets a 39.23-W power limit.

9.2.1.2.4 Set Fault Timer

The fault timer runs when the hot swap is in power limit or current limit, which is the case during start-up. Thus the timer has to be sized large enough to prevent a time-out during start-up. If the part starts directly into current limit ($I_{LIM} \times V_{DS} < P_{LIM}$) the maximum start time can be computed with Equation 11.

$$t_{start,max} = \frac{C_{OUT} \times V_{IN,MAX}}{I_{LIM}} \tag{11}$$

For most designs (including this example), $I_{LIM} \times V_{DS} > P_{LIM}$, so the hot swap starts in power limit and transition into current limit. In that case, the estimated start time can be computed with Equation 12.

$$t_{start} = \frac{C_{OUT}}{2} \times \left[\frac{V_{IN,MAX}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}^2} \right] = \frac{330\mu F}{2} \times \left[\frac{(30\,V)^2}{39.23\,W} + \frac{39.23\,W}{(10\,A)^2} \right] = 3.85\,ms \tag{12}$$

Note that the above start-time assumes constant, typical current limit and power limit values. The actual startup time is slightly longer, as the power limit is a function of Vds and decreases as the output voltage increases. To ensure that the timer never times out during start-up, TI recommends setting the minimum fault time (t_{flt}) to be greater than the start time (t_{start}) by adding an additional margin of 50% of the fault time. This accounts for the variation in power limit, timer current, and timer capacitance. Thus C_{TIMER} can be computed with Equation 13.

$$C_{TIMER} = \frac{t_{flt} \times i_{timer(typ)}}{v_{timer(typ)}} \times 1.5 = \frac{3.85ms \times 85\mu A}{4V} \times 1.5 = 123nF \tag{13}$$

The next largest available C_{TIMER} is chosen as 150 nf. Once the C_{TIMER} is chosen the actual programmed fault time can be computed with Equation 14.

$$t_{flt} = \frac{C_{TIMER} \times v_{timer,typ}}{i_{timer,typ}} = \frac{150\,nF \times 4\,V}{85\,\mu A} = 7.06\,ms \tag{14}$$

This is the typical time that the LM5069 shuts off the CSD19536KTT MOSFET.

9.2.1.2.5 Check MOSFET SOA

Once the power limit and fault timer are chosen, it's critical to check that the FET stays within its SOA during all test conditions. During a *Hot-Short*, the circuit breaker trips and the LM5069 restarts into power limit until the timer runs out. In the worst case, the MOSFET's V_{DS} equals $V_{IN,MAX}$, I_{DS} equals P_{LIM} / $V_{IN,MAX}$ and the stress event lasts for t_{flt}. For this design example, the MOSFET has 30 V, 1.25 A across it for 7.06 ms.

Based on the SOA of the CSD19536KTT, it can handle 30 V, 9 A for 10 ms and it can handle 30 V, 20 A for 1 ms. The SOA for 7.06 ms can be extrapolated by approximating SOA versus time as a power function as shown Equation 15 through Equation 18.

$$I_{SOA}(t) = a \times t^m \tag{15}$$

$$m = \frac{\ln \frac{I_{SOA}(t_1)}{I_{SOA}(t_2)}}{\ln\left(\frac{t_1}{t_2}\right)} = \frac{\ln\left(\frac{20\,A}{9\,A}\right)}{\ln\left(\frac{1ms}{10ms}\right)} = -0.346 \tag{16}$$

$$a = \frac{I_{SOA}(t_1)}{t_1^m} = \frac{20\,A}{(1ms)^{-0.346}} = 20\,A \times (1ms)^{0.346} \tag{17}$$

$$I_{SOA}(7.06\,ms) = 20\,A \times (1ms)^{0.346} \times (7.06\,ms)^{-0.346} = 10.17\,A \tag{18}$$

Note that the SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be much hotter during a hot-short. The SOA must be derated based on $T_{C,MAX}$ using Equation 19.

$$I_{SOA}(7.06\,ms, T_{C,MAX}) = I_{SOA}(7.06\,ms, 25\,°C) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{T_{J,ABSMAX} - 25\,°C} \tag{19}$$

$$= 10.17\,A \times \frac{175\,°C - 63.6\,°C}{175\,°C - 25\,°C} = 7.55\,A \tag{20}$$

Based on this calculation the MOSFET can handle 7.55 A, 30 V for 7.06 ms at elevated case temperature, and is required to handle 1.25 A during a hot-short. This means the MOSFET is not at risk of getting damaged during a hot-short. In general, TI recommends for the MOSFET to be able to handle a minimum of 1.3× more power than what is required during a hot-short to provide margin to cover the variance of the power limit and fault time.

9.2.1.2.6 Set Undervoltage and Overvoltage Threshold

By programming the UVLO and OVLO thresholds the LM5069 enables the series pass device (Q1) when the input supply voltage (V_{SYS}) is within the desired operational range. If V_{SYS} is below the UVLO threshold, or above the OVLO threshold, Q1 is switched off, denying power to the load. Hysteresis is provided for each threshold.

9.2.1.2.6.1 Option A

The configuration shown in Figure 30 requires three resistors (R1-R3) to set the thresholds.

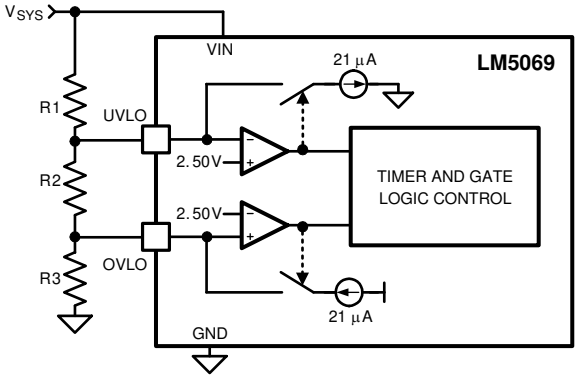


Figure 30. UVLO and OVLO Thresholds Set By R1-R3

The procedure to calculate the resistor values is as follows:

1. Choose the upper UVLO threshold (V_{UVH}), and the lower UVLO threshold (V_{UVL}).
2. Choose the upper OVLO threshold (V_{OVH}).
3. The lower OVLO threshold (V_{OVL}) cannot be chosen in advance in this case, but is determined after the values for R1-R3 are determined. If V_{OVL} must be accurately defined in addition to the other three thresholds, see Option B below.

The resistors are calculated with Equation 21, Equation 22, and Equation 23.

$$R1 = \frac{V_{UVH} - V_{UVL}}{21\ \mu A} = \frac{V_{UV(HYS)}}{21\ \mu A} \quad (21)$$

$$R3 = \frac{2.5V \times R1 \times V_{UVL}}{V_{OVH} \times (V_{UVL} - 2.5V)} \quad (22)$$

$$R2 = \frac{2.5V \times R1}{V_{UVL} - 2.5V} - R3 \quad (23)$$

The lower OVLO threshold is calculated from Equation 24.

$$V_{OVL} = [(R1 + R2) \times (\frac{(2.5V)}{R3} - 21\ \mu A)] + 2.5V \quad (24)$$

As an example, assume the application requires the following thresholds: V_{UVH} = 36 V, V_{UVL} = 32 V, V_{OVH} = 60 V.

$$R1 = \frac{36V - 32V}{21\ \mu A} = \frac{4V}{21\ \mu A} = 190.5\ k\Omega \quad (25)$$

$$R3 = \frac{2.5V \times 190.5\ k\Omega \times 32V}{60V \times (32V - 2.5V)} = 8.61\ k\Omega \quad (26)$$

$$R2 = \frac{2.5V \times 190.5\ k\Omega}{(32V - 2.5V)} - 8.61\ k\Omega = 7.53\ k\Omega \quad (27)$$

The lower OVLO threshold calculates to 55.8 V, and the OVLO hysteresis is 4.2 V. Note that the OVLO hysteresis is always slightly greater than the UVLO hysteresis in this configuration. When the R1-R3 resistor values are known, the threshold voltages and hysteresis are calculated from Equation 28 through Equation 33.

$$V_{UVH} = 2.5V + [R1 \times (21\ \mu A + \frac{2.5V}{(R2 + R3)})] \quad (28)$$

$$V_{UVL} = \frac{2.5V \times (R1 + R2 + R3)}{R2 + R3} \quad (29)$$

$$V_{UV(HYS)} = R1 \times 21\ \mu A \quad (30)$$

$$V_{OVH} = \frac{2.5V \times (R1 + R2 + R3)}{R3} \quad (31)$$

$$V_{OVL} = [(R1 + R2) \times \frac{(2.5V)}{R3} - 21\ \mu A)] + 2.5V \quad (32)$$

$$V_{OV(HYS)} = (R1 + R2) \times 21\ \mu A \quad (33)$$

9.2.1.2.6.2 Option B

If all four thresholds must be accurately defined, the configuration in Figure 31 can be used.

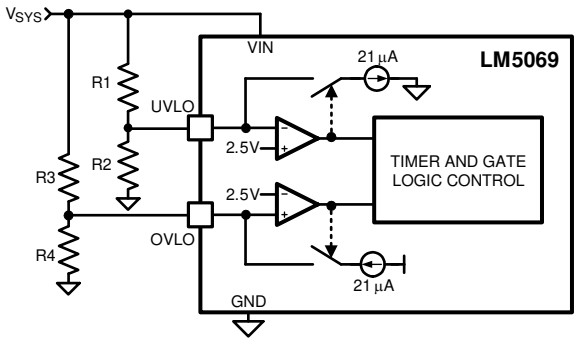


Figure 31. Programming the Four Thresholds

The four resistor values are calculated as follows:

1. Choose the upper UVLO threshold (V_{UVH}) and lower UVLO threshold (V_{UVL}) with Equation 34 and Equation 35.

$$R1 = \frac{V_{UVH} - V_{UVL}}{21\ \mu A} = \frac{V_{UV(HYS)}}{21\ \mu A} \quad (34)$$

$$R2 = \frac{2.5V \times R1}{(V_{UVL} - 2.5V)} \quad (35)$$

2. Choose the upper OVLO threshold (V_{OVH}) and lower OVLO threshold (V_{OVL}) with Equation 36 and Equation 37.

$$R3 = \frac{V_{OVH} - V_{OVL}}{21\ \mu A} = \frac{V_{OV(HYS)}}{21\ \mu A} \quad (36)$$

$$R4 = \frac{2.5V \times R3}{(V_{OVH} - 2.5V)} \quad (37)$$

As an example, assume the application requires the following thresholds: V_{UVH} = 22 V, V_{UVL} = 17 V, V_{OVH} = 60 V, and V_{OVL} = 58 V. Therefore $V_{UV(HYS)}$ = 5 V, and $V_{OV(HYS)}$ = 2 V. The resistor values are:

- R1 = 238 kΩ, R2 = 41 kΩ
- R3 = 95.2 kΩ, R4 = 4.14 kΩ

Where the R1-R4 resistor values are known, the threshold voltages and hysteresis are calculated from Equation 38 to Equation 43.

$$V_{UVH} = 2.5V + [R1 \times (\frac{2.5V}{R2} + 21\ \mu A)] \quad (38)$$

$$V_{UVL} = \frac{2.5V \times (R1 + R2)}{R2} \quad (39)$$

$$V_{UV(HYS)} = R1 \times 21\ \mu A \quad (40)$$

$$V_{OVH} = \frac{2.5V \times (R3 + R4)}{R4} \quad (41)$$

$$V_{OVL} = 2.5V + [R3 \times (\frac{2.5V}{R4} - 21\ \mu A)] \quad (42)$$

$$V_{OV(HYS)} = R3 \times 21\ \mu A \quad (43)$$

9.2.1.2.6.3 Option C

The minimum UVLO level is obtained by connecting the UVLO pin to VIN as shown in Figure 32. Q1 is switched on when the VIN voltage reaches the POR_{EN} threshold (≅8.4 V). An external transistor can be connected to UVLO to provide remote shutdown control, and to restart the LM5069-1 after a fault detection. The OVLO thresholds are set using R3, R4. Their values are calculated using the procedure in Option B.

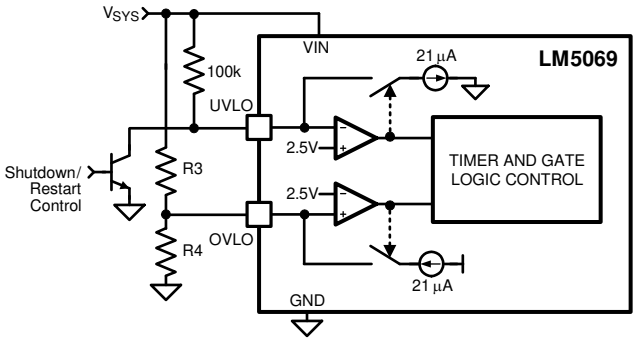


Figure 32. UVLO = POR_{EN} With Shutdown/Restart Control

9.2.1.2.6.4 Option D

The OVLO function can be disabled by grounding the OVLO pin. The UVLO thresholds are set as described in Option B or Option C.

For this design example, option B is used and the following values are targeted: V_{UVH} = 10 V, V_{UVL} = 9 V, V_{OVH} = 15 V, V_{OVL} = 14 V. R1, R2, R3, and R4 are computed using Equation 44 through Equation 47.

$$R1 = \frac{V_{UVH} - V_{UVL}}{21\mu A} = \frac{18\,V - 17\,V}{21\mu A} = 47.62k \quad (44)$$

$$R2 = \frac{2.5\,V \times R1}{\left(V_{UVL} - 2.5\,V\right)} = \frac{2.5\,V \times 47.62k}{\left(17\,V - 2.5\,V\right)} = 8.21k \quad (45)$$

$$R3 = \frac{V_{OVH} - V_{OVL}}{21\mu A} = \frac{31\,V - 30\,V}{21\mu A} = 47.62k \quad (46)$$

$$R4 = \frac{2.5\,V \times R3}{\left(V_{OVH} - 2.5\,V\right)} = \frac{2.5\,V \times 47.62k}{\left(31V - 2.5\,V\right)} = 4.18k \quad (47)$$

Nearest available 1% resistors must be chosen. Set R1 = 47.5 kΩ, R2 = 8.25 kΩ, R3 = 47.5 kΩ, and R4 = 4.22 kΩ.

9.2.1.2.7 Input and Output Protection

Proper operation of the LM5069 hot swap circuit requires a voltage clamping element present on the supply side of the connector into which the hot swap circuit is plugged in. A TVS is ideal, as depicted in Figure 27. The TVS is necessary to absorb the voltage transient generated whenever the hot swap circuit shuts off the load current. This effect is the most severe during a hot-short when a large current is suddenly interrupted when the FET shuts off. The TVS must be chosen to have minimal leakage current at $V_{IN,MAX}$ and to clamp the voltage to under 30 V during hot-short events. For many high-power applications intended to clamp at 30 V, SMBJ30A-13-F is a good choice.

9.2.1.2.8 Final Schematic and Component Values

Figure 27 shows the schematic used to implement the requirements described in the previous section. In addition, Table 2 below provides the final component values that were used to meet the design requirements for a 12-V, 40-A hot swap design. The *Application Curves* are based on these component values.

Table 2. Component Values

COMPONENT	VALUE
Rsns	4 mΩ
R1	47.5 kΩ
R2	8.25 kΩ
R3	47.5 kΩ
R4	4.22 kΩ
R_{PWR}	15.8 kΩ
Q1	CSD19536KTT
Z1	SMBJ30A-13-F
D1	MBR3100
C_{TIMER}	150 nF
C_{OUT}	330 µF

9.2.1.3 Application Curves

Figure 33. Start-Up

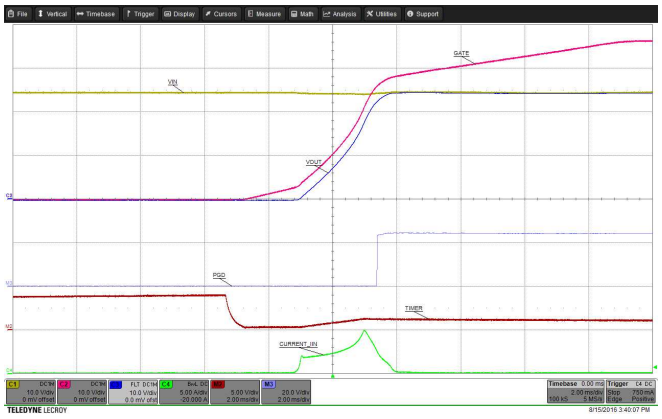


Figure 34. Start-Up (Zoomed In)

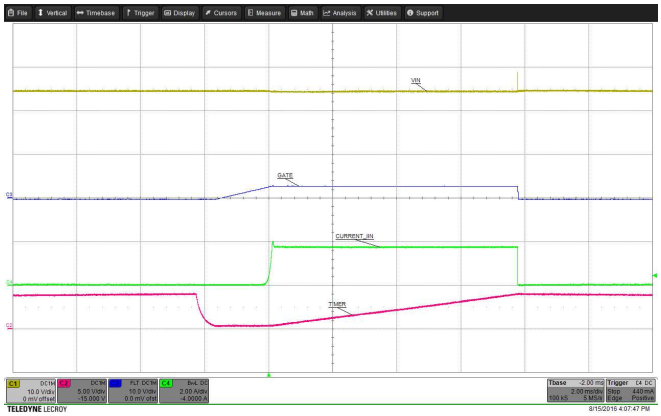


Figure 35. Start-Up into Short Circuit

Figure 36. Undervoltage

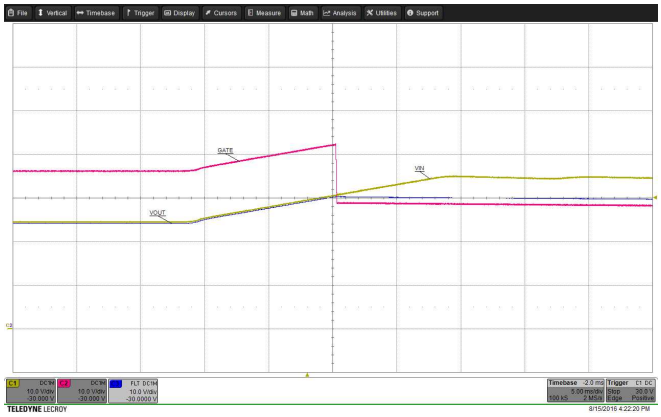


Figure 37. Overvoltage

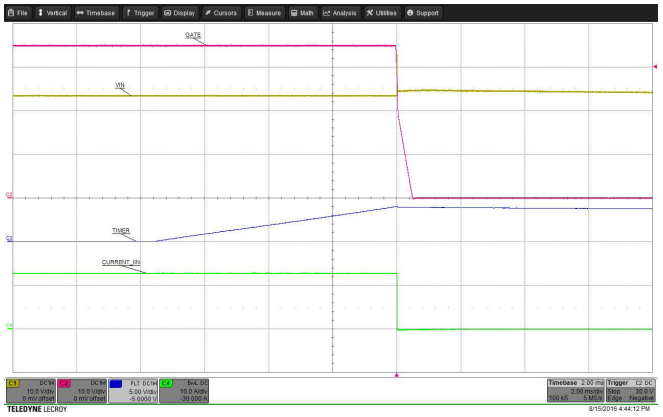


Figure 38. Gradual Overcurrent

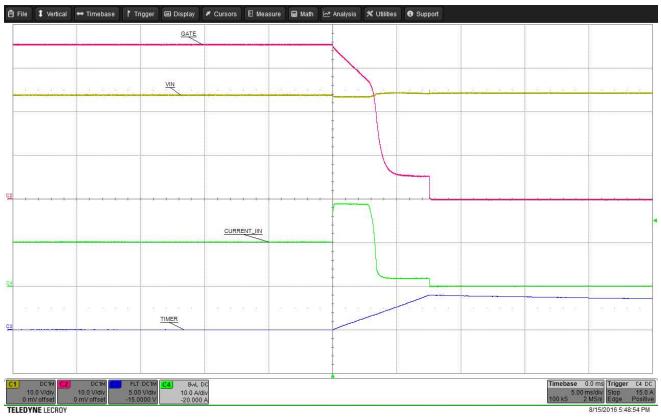


Figure 39. Load Step

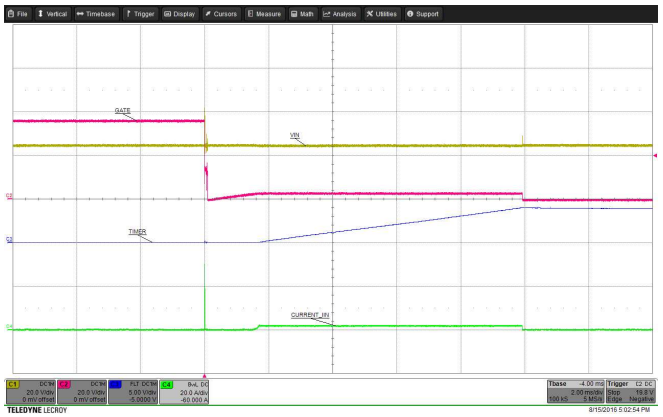


Figure 40. Hot-Short on Output

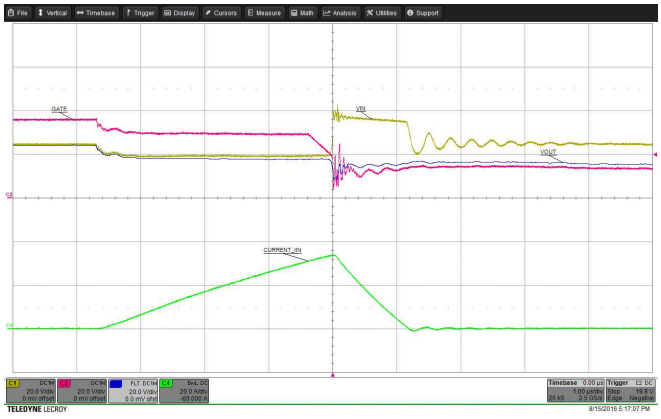


Figure 41. Hot-Short (Zoomed In)

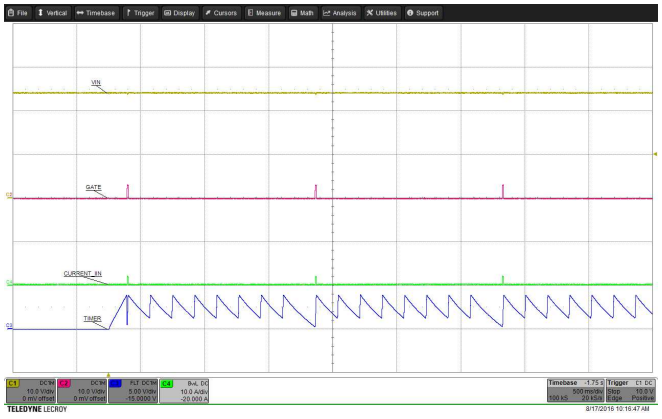


Figure 42. Auto-Retry

10 Power Supply Recommendations

In general, the LM5069 behavior is more reliable if it is supplied from a very regulated power supply. However, high-frequency transients on a backplane are not uncommon due to adjacent card insertions or faults. If this is expected in the end system, TI recommends placing a 1-µF ceramic capacitor to ground close to the drain of the hot swap MOSFET. This reduces the common mode voltage seen by VIN and SENSE. Additional filtering may be necessary to avoid nuisance trips.

11 Layout

11.1 Layout Guidelines

11.1.1 PC Board Guidelines

The following guidelines must be followed when designing the PC board for the LM5069:

- Place the LM5069 close to the board's input connector to minimize trace inductance from the connector to the FET.
- Note that special care must be taken when placing the bypass capacitor for the VIN pin. During hot shorts, there is a very large dV/dt on input voltage after the MOSFET turns off. If the bypass capacitor is placed right next to the pin and the trace from Rsns to the pin is long, an LC filter is formed. As a result, a large differential voltage can develop between VIN and SENSE. To avoid this, place the bypass capacitor close to Rsns instead of the VIN pin.

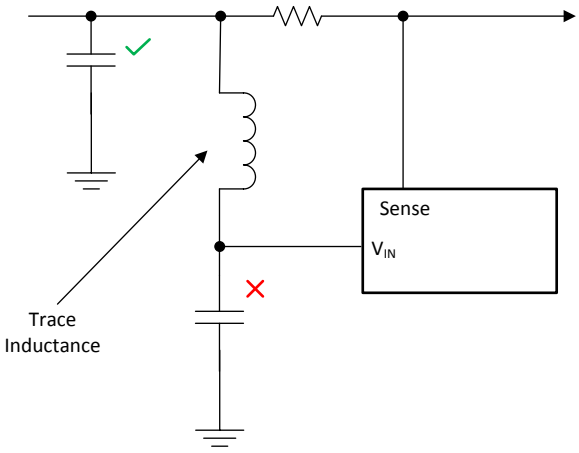


Figure 43. Layout Trace Inductance

- The sense resistor (R_S) must be close to the LM5069, and connected to it using the Kelvin techniques shown in Figure 46.
- The high current path from the board's input to the load (via Q1), and the return path, must be parallel and close to each other to minimize loop inductance.
- The ground connection for the various components around the LM5069 must be connected directly to each other, and to the LM5069's GND pin, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- Provide adequate heat sinking for the series pass device (Q1) to help reduce stresses during turnon and turnoff.
- The board's edge connector can be designed to shut off the LM5069 as the board is removed, before the supply voltage is disconnected from the LM5069. In Figure 45 the voltage at the UVLO pin goes to ground before V_{SYS} is removed from the LM5069 due to the shorter edge connector pin. When the board is inserted into the edge connector, the system voltage is applied to the LM5069's VIN pin before the UVLO voltage is taken high.

11.1.2 System Considerations

A) Continued proper operation of the LM5069 hot swap circuit requires capacitance be present on the supply side of the connector into which the hot swap circuit is plugged in, as depicted in Figure 44. The capacitor in the *Live Backplane* section is necessary to absorb the transient generated whenever the hot swap circuit shuts off the load current. If the capacitance is not present, inductance in the supply lines generate a voltage transient at shut-off which can exceed the absolute maximum rating of the LM5069, resulting in its destruction.

B) If the load powered via the LM5069 hot swap circuit has inductive characteristics, a diode is required across the LM5069's output. The diode provides a recirculating path for the load's current when the LM5069 shuts off that current. Adding the diode prevents possible damage to the LM5069 as the OUT pin is taken below ground by the inductive load at shutoff. See Figure 44.

Layout Guidelines (continued)

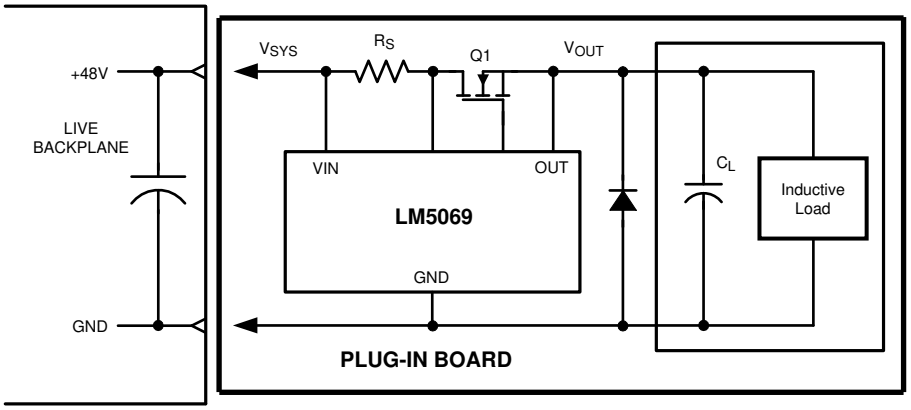


Figure 44. Output Diode Required for Inductive Loads

11.2 Layout Example

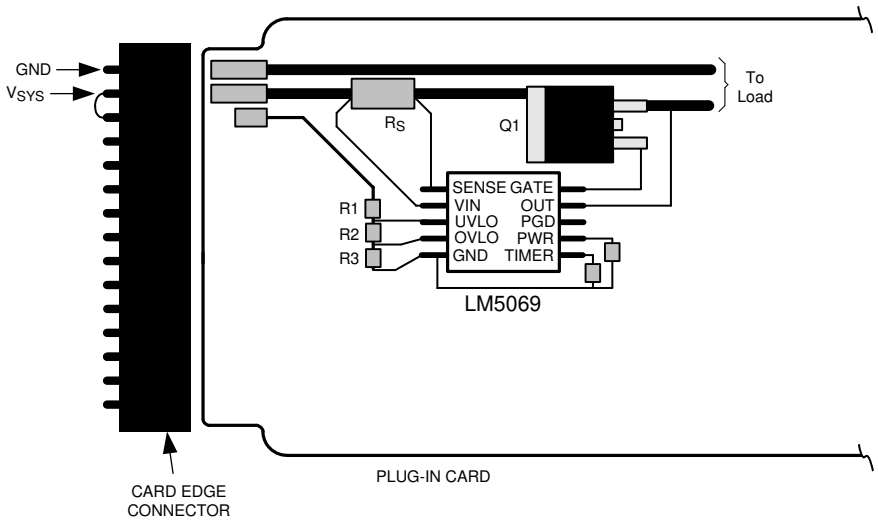


Figure 45. Recommended Board Connector Design

Layout Example (continued)

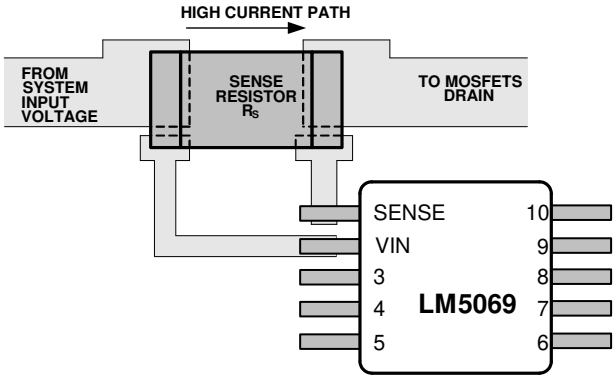


Figure 46. Sense Resistor Connections

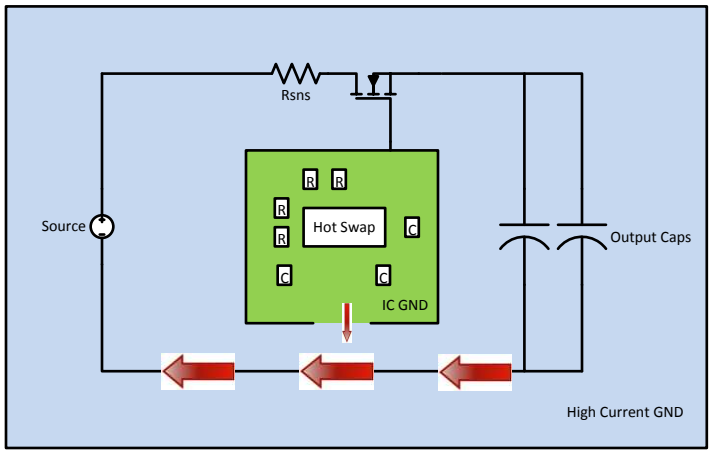


Figure 47. LM5069 Quiet IC Ground Layout

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

要了解 LM5069 设计计算器，请前往 ti.com.cn 查看产品文件夹下的工具和软件。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- *《焊接的绝对最大额定值》*(SNOA549)
- *可靠的热插拔设计* (SLVA673)

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5069MM-1/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SNAB	Samples
LM5069MM-2	NRND	VSSOP	DGS	10	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	SNBB	
LM5069MM-2/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SNBB	Samples
LM5069MMX-1/NOPB	ACTIVE	VSSOP	DGS	10	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SNAB	Samples
LM5069MMX-2/NOPB	ACTIVE	VSSOP	DGS	10	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SNBB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

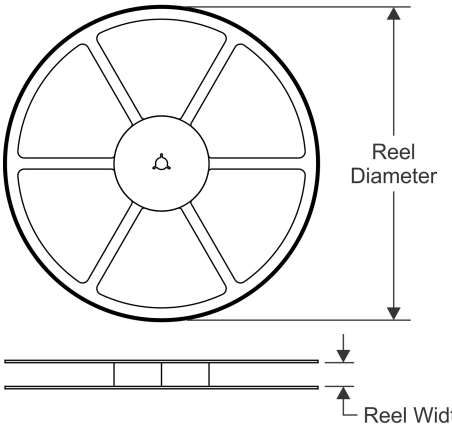
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

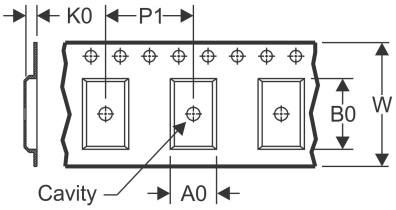
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

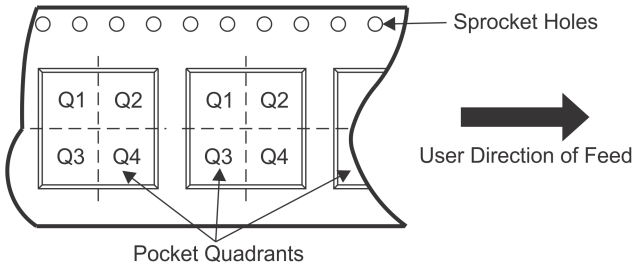


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

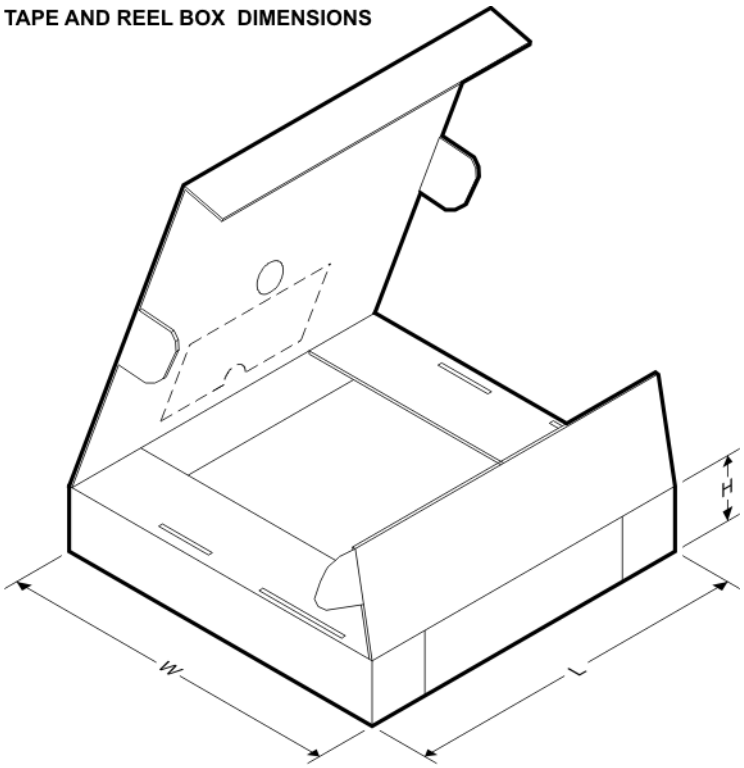
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5069MM-1/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5069MM-2	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5069MM-2/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5069MMX-1/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5069MMX-2/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

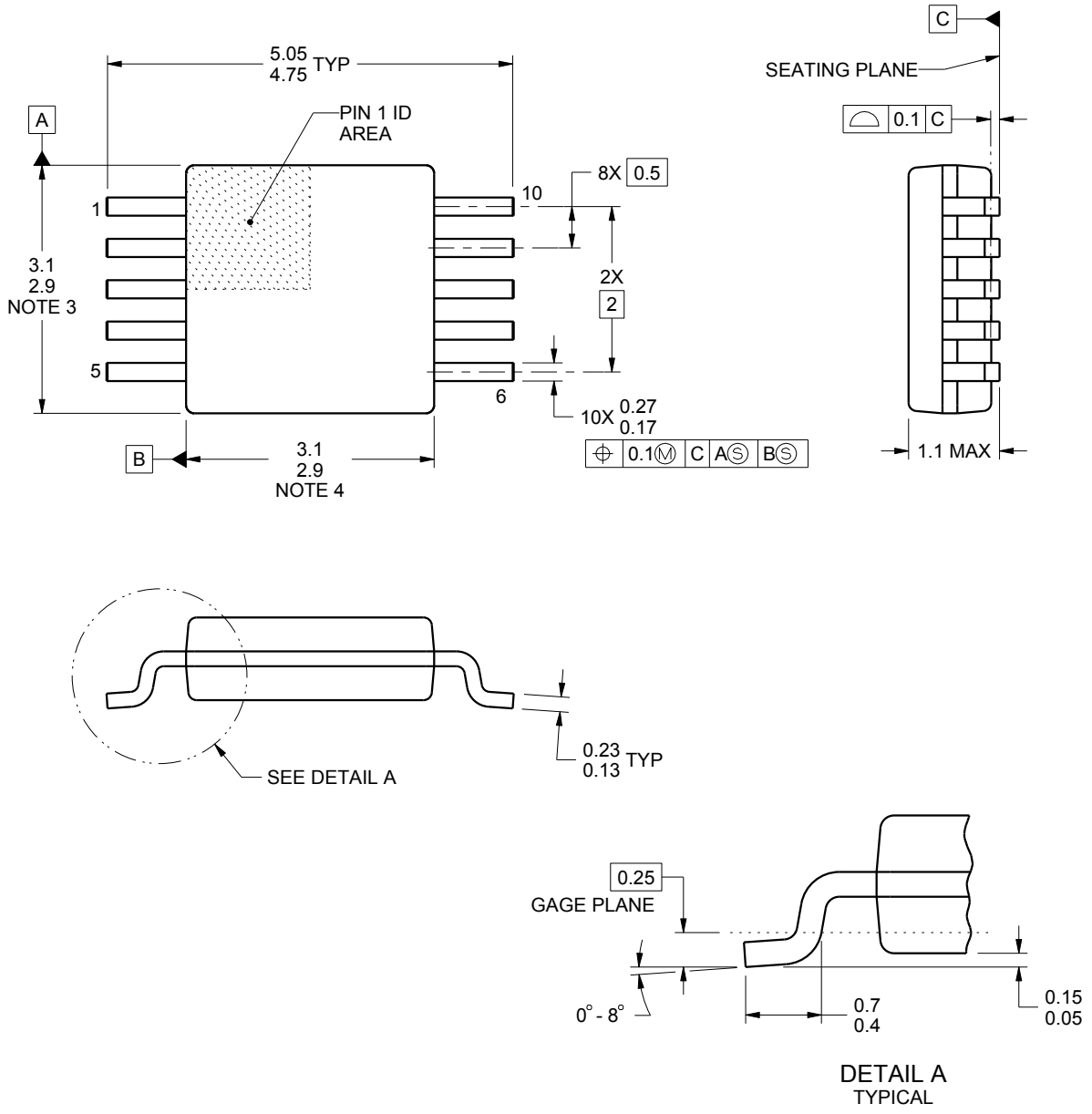
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5069MM-1/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM5069MM-2	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM5069MM-2/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM5069MMX-1/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM5069MMX-2/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

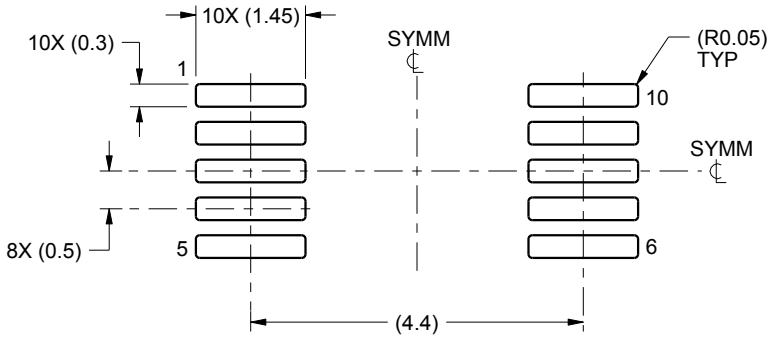
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

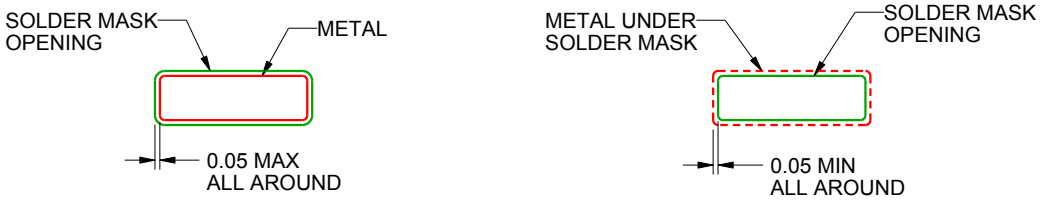


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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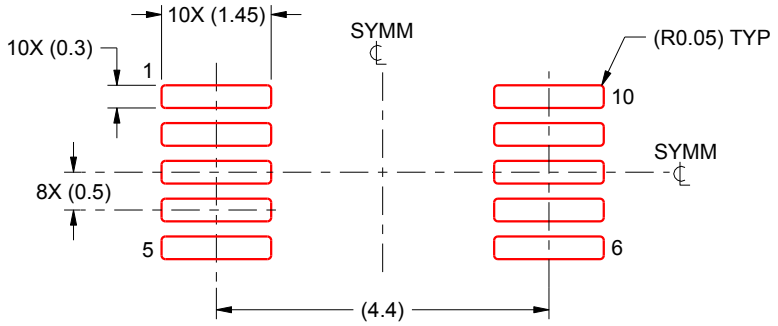
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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