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National Semiconductor

December 1, 2008

LM5104
High Voltage Half-Bridge Gate Driver with Adaptive Delay

General Description

The LM5104 High Voltage Gate Driver is designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck configuration. The floating high-side driver is capable of working with supply voltages up to 100V. The high side and low side gate drivers are controlled from a single input. Each change in state is controlled in an adaptive manner to prevent shoot-through issues. In addition to the adaptive transition timing, an additional delay time can be added, proportional to an external setting resistor. An integrated high voltage diode is provided to charge high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high side gate driver. Undervoltage lockout is provided on both the low side and the high side power rails. This device is available in the standard SOIC-8 pin and the LLP-10 pin packages.

Features

- Drives both a high side and low side N-channel MOSFET
- Adaptive rising and falling edges with programmable additional delay
- Single input control
- Bootstrap supply voltage range up to 118V DC
- Fast turn-off propagation delay (25 ns typical)
- Drives 1000 pF loads with 15 ns rise and fall times
- Supply rail under-voltage lockout

Typical Applications

- Current Fed Push-Pull Power Converters
- High Voltage Buck Regulators
- Active Clamp Forward Power Converters
- Half and Full Bridge Converters

Package

- SOIC-8
- LLP-10 (4 mm x 4 mm)

Simplified Block Diagram

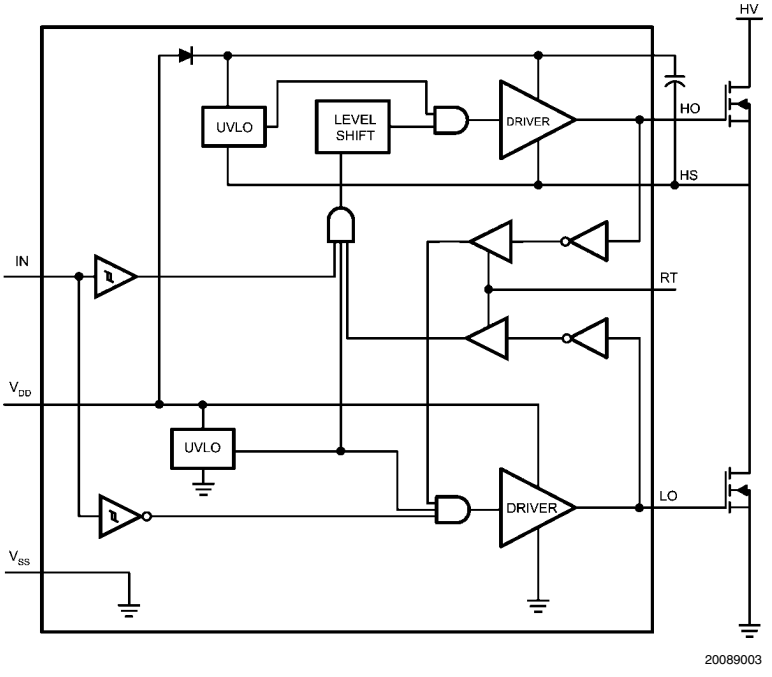
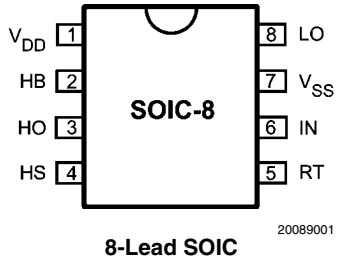
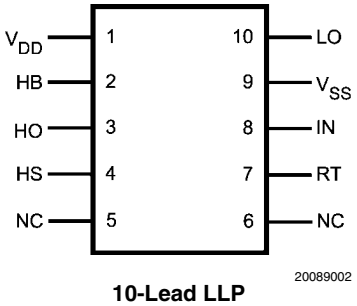


FIGURE 1.

Connection Diagram



8-Lead SOIC
See NS Package Number M08A



10-Lead LLP
See NS Package Number SDC10A

FIGURE 2.

Ordering Information

Ordering Number	Package Type	NSC Package Drawing	Supplied As
LM5104M	SOIC-8	M08A	Shipped with Anti-Static Rails
LM5104MX	SOIC-8	M08A	2500 shipped as Tape & Reel
LM5104SD	LLP-10	SDC10A	1000 shipped as Tape & Reel
LM5104SDX	LLP-10	SDC10A	4500 shipped as Tape & Reel

Pin Descriptions

Pin		Name	Description	Application Information
SOIC-8	LLP-10			
1	1	V_{DD}	Positive gate drive supply	Locally decouple to V_{SS} using low ESR/ESL capacitor, located as close to IC as possible.
2	2	HB	High side gate driver bootstrap rail	Connect the positive terminal of bootstrap capacitor to the HB pin and connect negative terminal to HS. The Bootstrap capacitor should be placed as close to IC as possible.
3	3	HO	High side gate driver output	Connect to gate of high side MOSFET with short low inductance path.
4	4	HS	High side MOSFET source connection	Connect to bootstrap capacitor negative terminal and source of high side MOSFET.
5	7	RT	Deadtime programming pin	Resistor from RT to ground programs the deadtime between high and low side transitions.The resistor should be located close to the IC to minimize noise coupling from adjacent traces.
6	8	IN	Control input	Logic 1 equals High Side ON and Low Side OFF. Logic 0 equals High Side OFF and Low Side ON.
7	9	V_{SS}	Ground return	All signals are referenced to this ground.
8	10	LO	Low side gate driver output	Connect to the gate of the low side MOSFET with a short low inductance path.

Note: For LLP-10 package, it is recommended that the exposed pad on the bottom of the LM5100 / LM5101 be soldered to ground plane on the PC board, and the ground plane should extend out from beneath the IC to help dissipate the heat. Pins 5 and 6 have no connection.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{DD} to V_{SS}	–0.3V to +18V
V_{HB} to V_{HS}	–0.3V to +18V
IN to V_{SS}	–0.3V to V_{DD} + 0.3V
LO Output	–0.3V to V_{DD} + 0.3V
HO Output	V_{HS} – 0.3V to V_{HB} + 0.3V
V_{HS} to V_{SS}	–1V to +100V
V_{HB} to V_{SS}	118V
RT to V_{SS}	–0.3V to 5V
Junction Temperature	+150°C
Storage Temperature Range	–55°C to +150°C
ESD Rating HBM (Note 2)	2 kV

Recommended Operating Conditions

V_{DD}	+9V to +14V
HS	–1V to 100V
HB	V_{HS} + 8V to V_{HS} + 14V
HS Slew Rate	<50V/ns
Junction Temperature	–40°C to +125°C

Electrical Characteristics

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, RT = 100kΩ. No Load on LO or HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	LI = HI = 0V		0.4	**0.6**	mA
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		1.9	**3**	mA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V		0.06	**0.2**	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.3	**3**	mA
I_{HBS}	HB to V_{SS} Current, Quiescent	V_{HS} = V_{HB} = 100V		0.05	**10**	µA
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.08		mA
INPUT PINS						
V_{IL}	Low Level Input Voltage Threshold		**0.8**	1.8		V
V_{IH}	High Level Input Voltage Threshold			1.8	**2.2**	V
R_I	Input Pulldown Resistance		**100**	200	**500**	kΩ
TIME DELAY CONTROLS						
V_{RT}	Nominal Voltage at RT		**2.7**	3	**3.3**	V
I_{RT}	RT Pin Current Limit	RT = 0V	**0.75**	1.5	**2.25**	mA
T_{D1}	Delay Timer, RT = 10 kΩ		**58**	90	**130**	ns
T_{D2}	Delay Timer, RT = 100 kΩ		**140**	200	**270**	ns
UNDER VOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold		**6.0**	6.9	**7.4**	V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		**5.7**	6.6	**7.1**	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA		0.60	**0.9**	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA		0.85	**1.1**	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100 mA		0.8	**1.5**	Ω
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 100 mA		0.25	**0.4**	V
V_{OHL}	High-Level Output Voltage	I_{LO} = –100 mA V_{OHL} = V_{DD} – V_{LO}		0.35	**0.55**	V
I_{OHL}	Peak Pullup Current	V_{LO} = 0V		1.6		A
I_{OLL}	Peak Pulldown Current	V_{LO} = 12V		1.8		A

Symbol	Parameter	Conditions	Min	Typ	Max	Units
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA		0.25	**0.4**	V
V_{OHH}	High-Level Output Voltage	I_{HO} = –100 mA, $V_{OHH} = V_{HB} - V_{HO}$		0.35	**0.55**	V
I_{OHH}	Peak Pullup Current	V_{HO} = 0V		1.6		A
I_{OLH}	Peak Pulldown Current	V_{HO} = 12V		1.8		A
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	SOIC-8		170		°C/W
		LLP-10 (Note 3)		40		

Switching Characteristics

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified, $V_{DD} = V_{HB}$ = 12V, $V_{SS} = V_{HS}$ = 0V, No Load on LO or HO .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LPHL}	Lower Turn-Off Propagation Delay (IN Rising to LO Falling)			25	**56**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (IN Falling to HO Falling)			25	**56**	ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		15		ns
t_R, t_F	Either Output Rise/Fall Time (3V to 9V)	C_L = 0.1 µF		0.6		µs
t_{BS}	Bootstrap Diode Turn-Off Time	I_F = 20 mA, I_R = 200 mA		50		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. 2 kV for all pins except Pin 2, Pin 3 and Pin 4 which are rated at 500V.

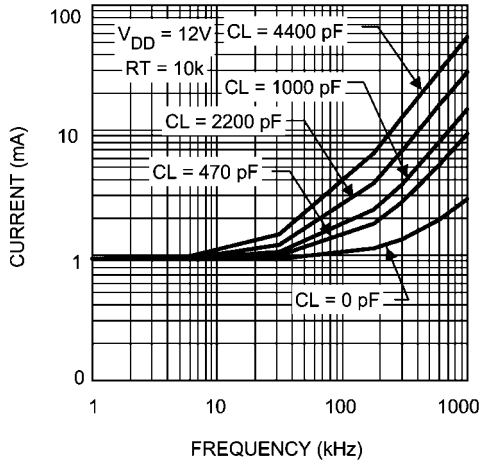
Note 3: 4 layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

Note 4: Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 5: The θ_{JA} is not a given constant for the package and depends on the printed circuit board design and the operating environment.

Typical Performance Characteristics

I_{DD} vs Frequency



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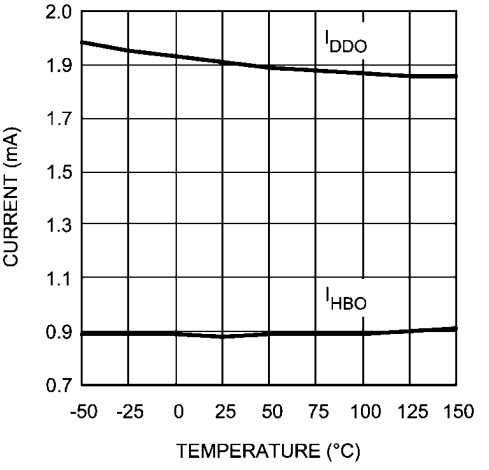
Operating Current vs Temperature



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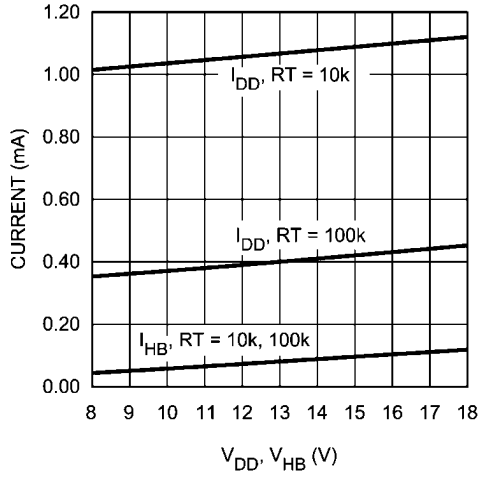
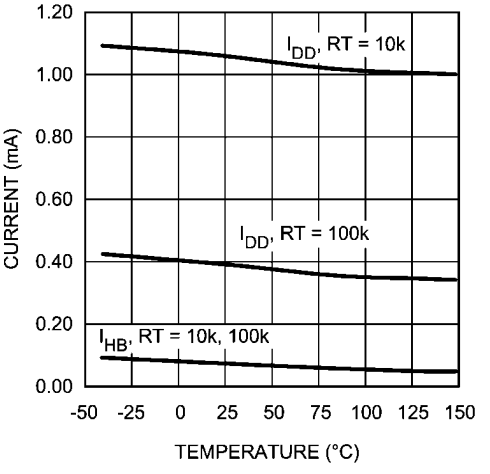
Quiescent Current vs Supply Voltage



20089012

Quiescent Current vs Temperature



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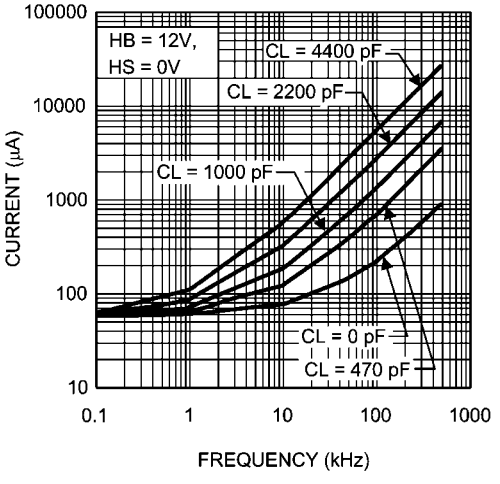
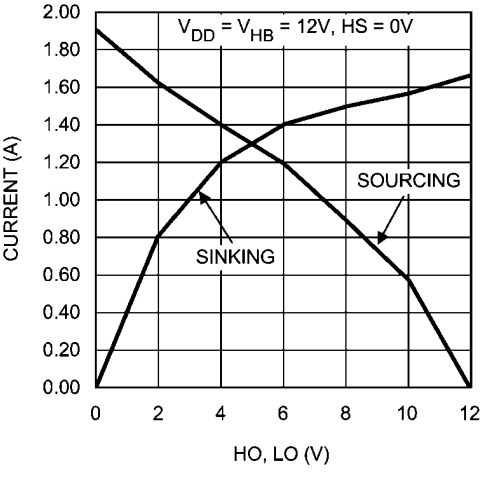
I_{HB} vs Frequency



20089017

HO & LO Peak Output Current vs Output Voltage



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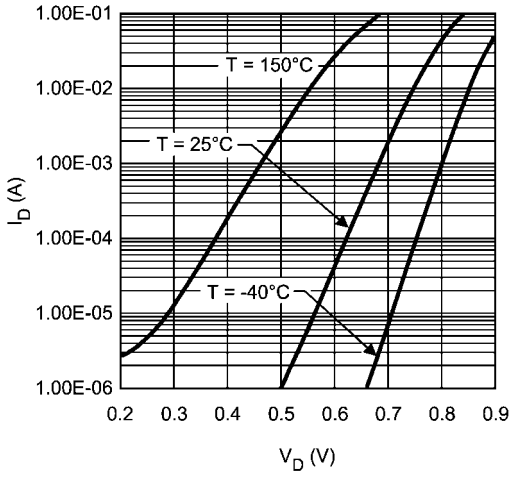
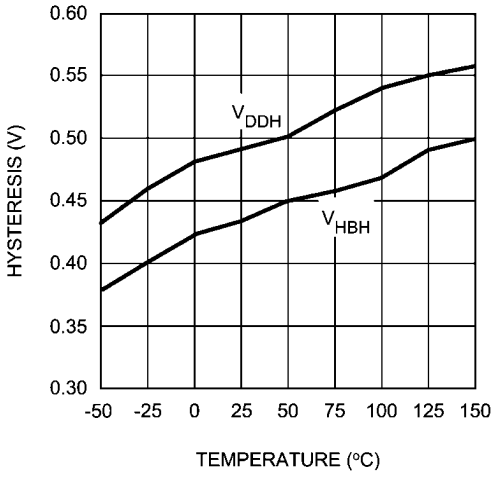
Diode Forward Voltage



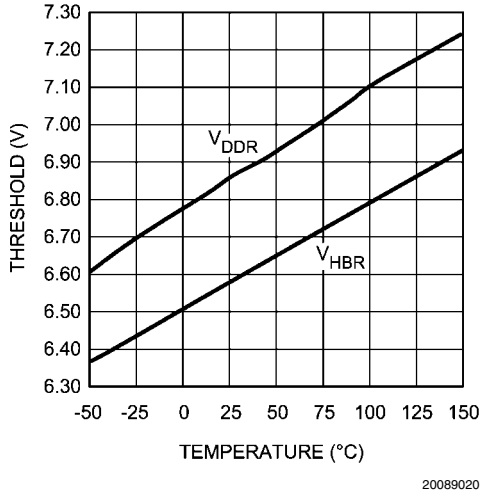
20089016

Undervoltage Threshold Hysteresis vs Temperature



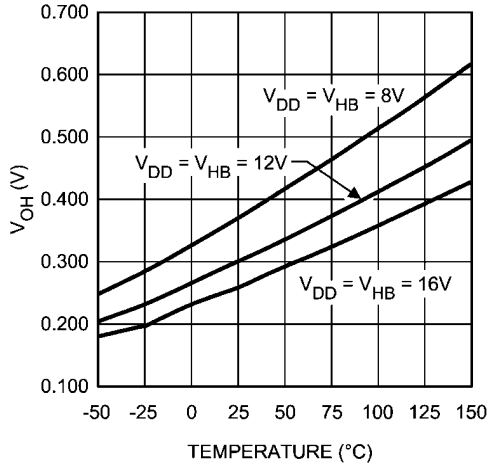
20089019

Undervoltage Rising Threshold vs Temperature



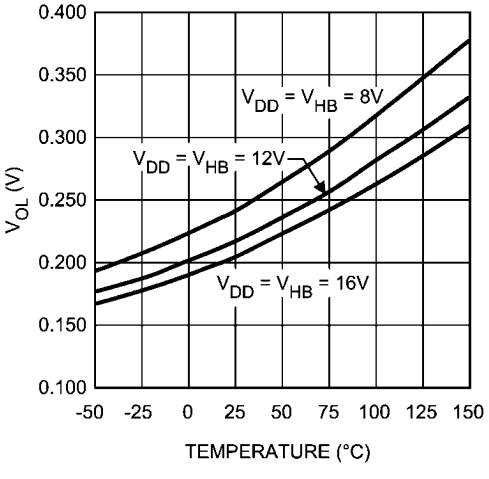
20089020

LO & HO Gate Drive—High Level Output Voltage vs Temperature



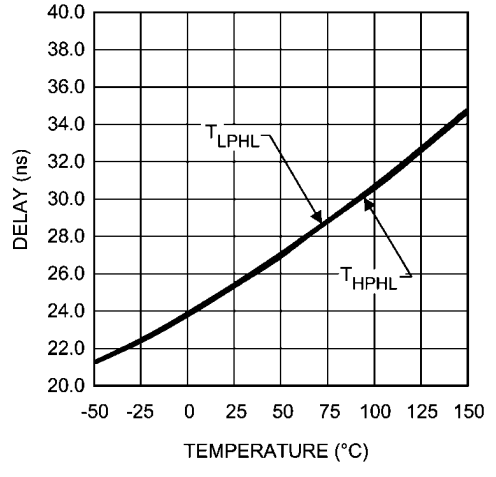
20089021

LO & HO Gate Drive—Low Level Output Voltage vs Temperature



20089022

Turn Off Propagation Delay vs Temperature



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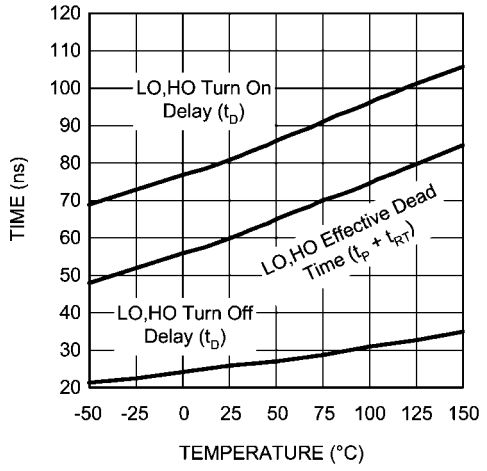
Timing vs Temperature RT = 10K



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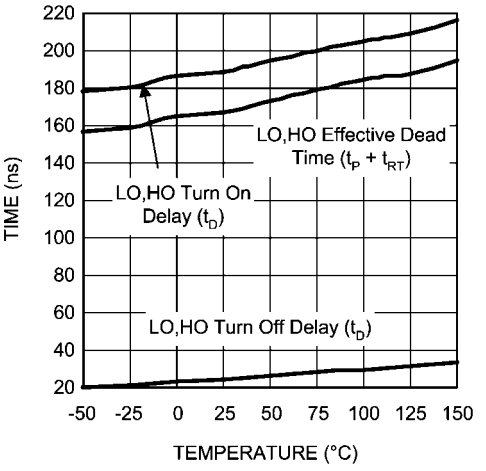
Timing vs Temperature RT = 100K



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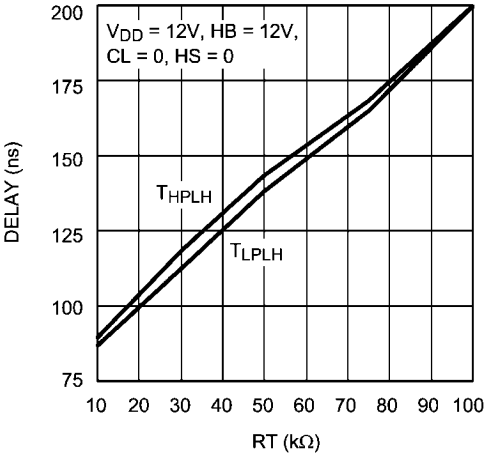
Turn On Delay vs RT Resistor Value



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LM5104 Waveforms

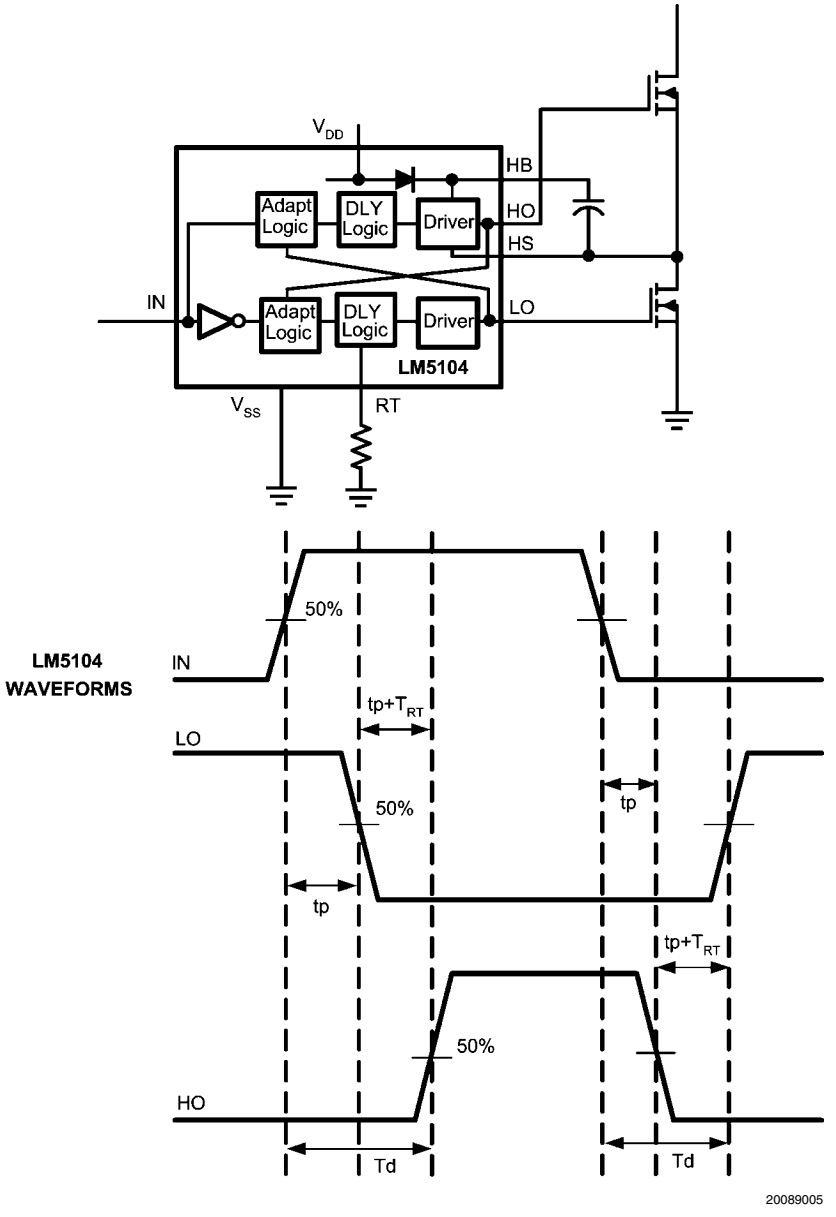


FIGURE 3. Application Timing Waveforms

Operational Description

ADAPTIVE SHOOT-THROUGH PROTECTION

LM5104 is a high voltage, high speed dual output driver designed to drive top and bottom MOSFET's connected in synchronous buck or half-bridge configuration, from one externally provided PWM signal. LM5104 features adaptive delay to prevent shoot-through current through top and bottom MOSFETs during switching transitions. Referring to the timing diagram *Figure 3*, the rising edge of the PWM input (IN) turns off the bottom MOSFET (LO) after a short propagation delay (t_P). An adaptive circuit in the LM5104 monitors the bottom gate voltage (LO) and triggers a programmable delay generator when the LO pin falls below an internally set threshold (≈ Vdd/2). The gate drive of the upper MOSFET (HO) is disabled until the deadtime expires. The upper gate is enabled after the TIMER delay (t_P+T_{RT}) , and the upper MOSFET turns-on. The additional delay of the timer prevents lower and upper MOSFETs from conducting simultaneously, thereby preventing shoot-through.

A falling transition on the PWM signal (IN) initiates the turn-off of the upper MOSFET and turn-on of the lower MOSFET. A short propagation delay (t_P) is encountered before the upper gate voltage begins to fall. Again, the adaptive shoot-through circuitry and the programmable deadtime TIMER delays the lower gate turn-on time. The upper MOSFET gate voltage is monitored and the deadtime delay generator is triggered when the upper MOSFET gate voltage with respect to ground drops below an internally set threshold (≈ Vdd/2). The lower gate drive is momentarily disabled by the timer and

turns on the lower MOSFET after the deadtime delay expires (t_P+T_{RT}).

The RT pin is biased at 3V and current limited to 1mA. It is designed to accommodate a resistor between 5K and 100K, resulting in an effective dead-time proportional to RT and ranging from 90ns to 200ns. RT values below 5K will saturate the timer and are not recommended.

Startup and UVLO

Both top and bottom drivers include under-voltage lockout (UVLO) protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (V_{HB} – V_{HS}) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn-on the external MOSFETs, and the built-in hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to V_{DD} pin of LM5104, the top and bottom gates are held low until V_{DD} exceeds UVLO threshold, typically about 6.9V. Any UVLO condition on the bootstrap capacitor will disable only the high side output (HO).

LAYOUT CONSIDERATIONS

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR/ESL capacitor must be connected close to the IC, and between V_{DD} and V_{SS} pins and between HB and HS pins to support high peak currents being drawn from V_{DD} during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (V_{SS}).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
   a) The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
5. The resistor on the RT pin must be placed very close to the IC and seperated from high current paths to avoid noise coupling to the time delay generator which could disrupt timer operation.

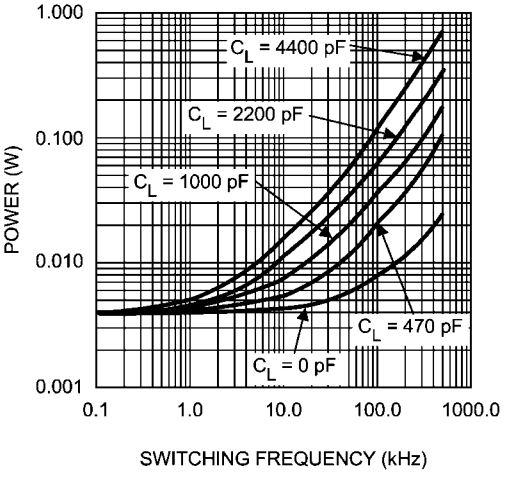
POWER DISSIPATION CONSIDERATIONS

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

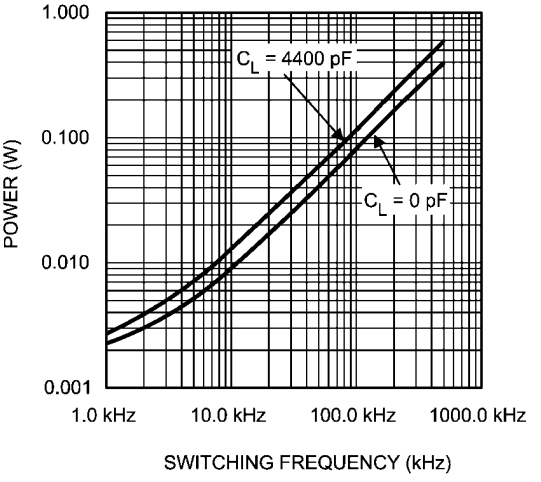
Gate Driver Power Dissipation (LO + HO)
V_{CC} = 12V, Neglecting Diode Losses



20089006

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

Diode Power Dissipation V_{IN} = 80V



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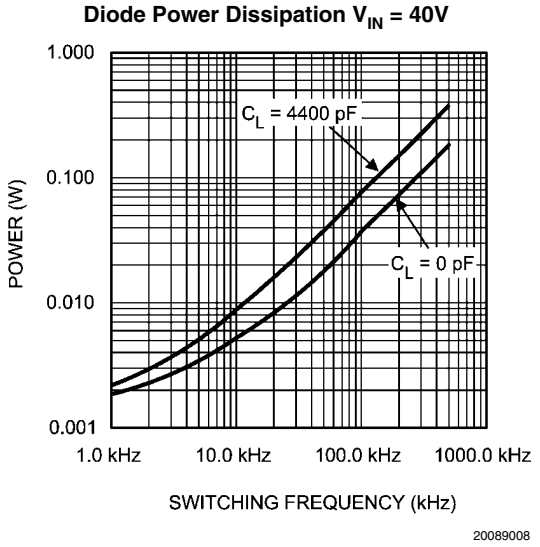


The total IC power dissipation can be estimated from the above plots by summing the gate drive losses with the bootstrap diode losses for the intended application. Because the diode losses can be significant, an external diode placed in parallel with the internal bootstrap diode (refer to *Figure 4*) can be helpful in removing power from the IC. For this to be effective, the external diode must be placed close to the IC to minimize series inductance and have a significantly lower forward voltage drop than the internal diode.

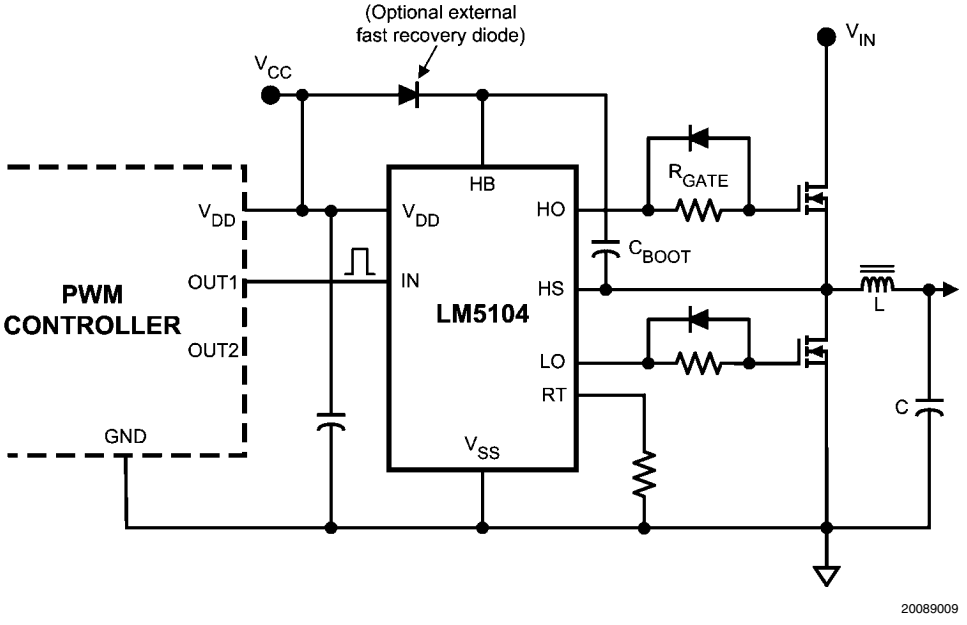
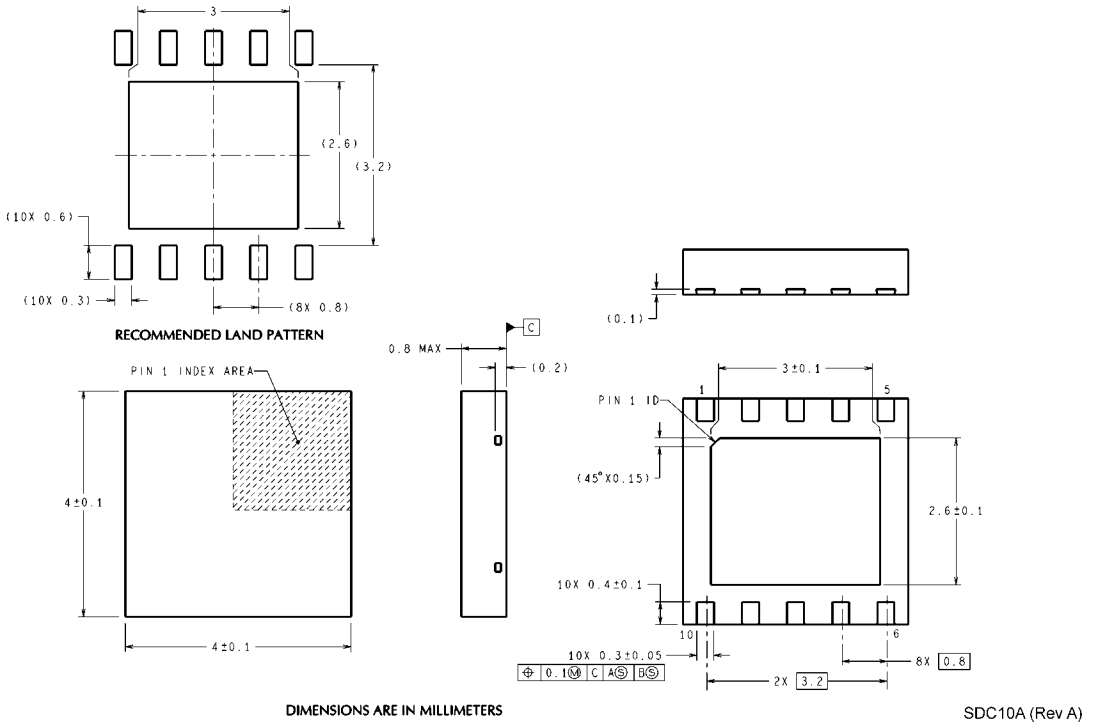


FIGURE 4. LM5104 Driving MOSFETs Connected in Synchronous Buck Configuration

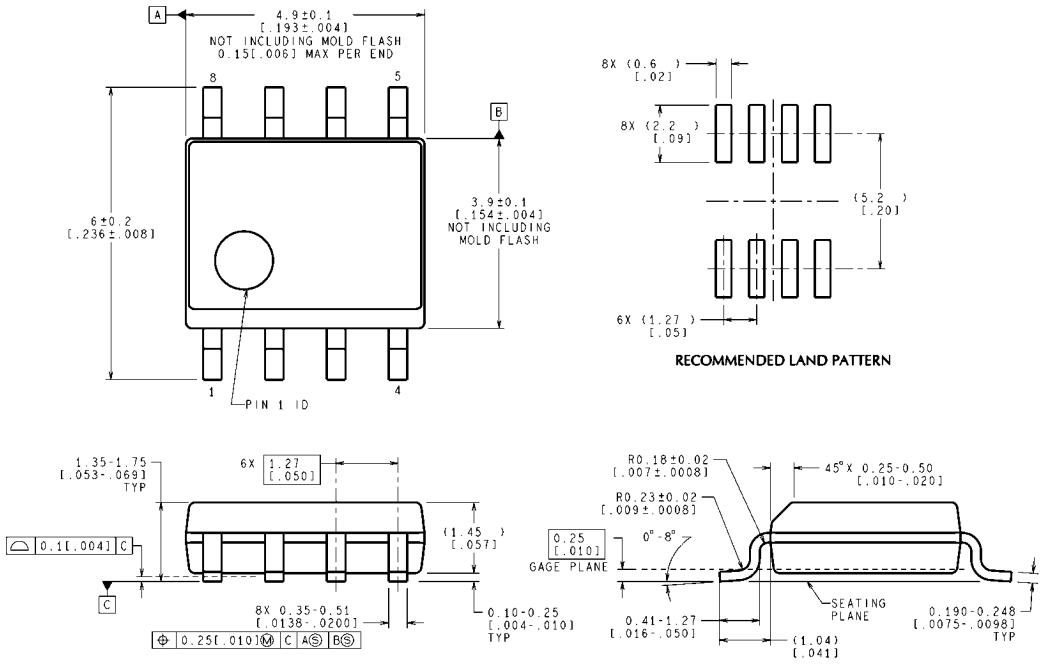
Physical Dimensions inches (millimeters) unless otherwise noted



Notes: Unless otherwise specified

1. Standard lead finish to be 200 microinches/5.00 micrometers minimum tin/lead (solder) on copper.
2. Pin 1 identification to have half of full circle option.
3. No JEDEC registration as of Feb. 2000.

LLP-10 Outline Drawing
NS Package Number SDC10A



M08A (Rev L)

Notes: Unless otherwise specified

1. For solder thickness and composition, see “Solder Information” in the packaging section of the National Semiconductor web page (www.national.com).
2. Maximum allowable metal burr on lead tips at the package edges is 76 microns.
3. No JEDEC registration as of May 2003.

SOIC-8 Outline Drawing
NS Package Number M08A

Notes

Notes

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