LM5109B-Q1 高电压 1A 峰值半桥栅极驱动器

1 特性

- 符合汽车类 应用标准
- 具有符合 AEC-Q100 标准的下列结果
  - 器件温度 1 级
  - 器件人体放电模型 (HBM) 静电放电 (ESD) 分类等级 1C
  - 器件组件充电模型 (CDM) ESD 分类等级 C4A
- 可驱动高侧和低侧 N 沟道金属氧化物半导体场效应晶体管 (MOSFET)
- 1A 峰值输出电流（1.0A 灌电流/1.0A 拉电流）
- 独立的晶体管-晶体管逻辑电路/互补金属氧化物半导体 (TTL/CMOS) 兼容输入
- 自举电源电压高达 108V（直流）
- 短暂传播时间（典型值为 30ns）
- 可以 15ns 的上升和下降时间驱动 1000pF 负载
- 优异的传播延迟匹配（典型值为 2ns)
- 电源轨欠压锁定
- 低功耗
- 耐热增强型晶圆级小外形无引线 (WSON)-8 封装

2 应用

- 推挽转换器
- 半桥和全桥电源转换器
- 固态电机驱动器
- 双开关正向电源转换器

3 说明

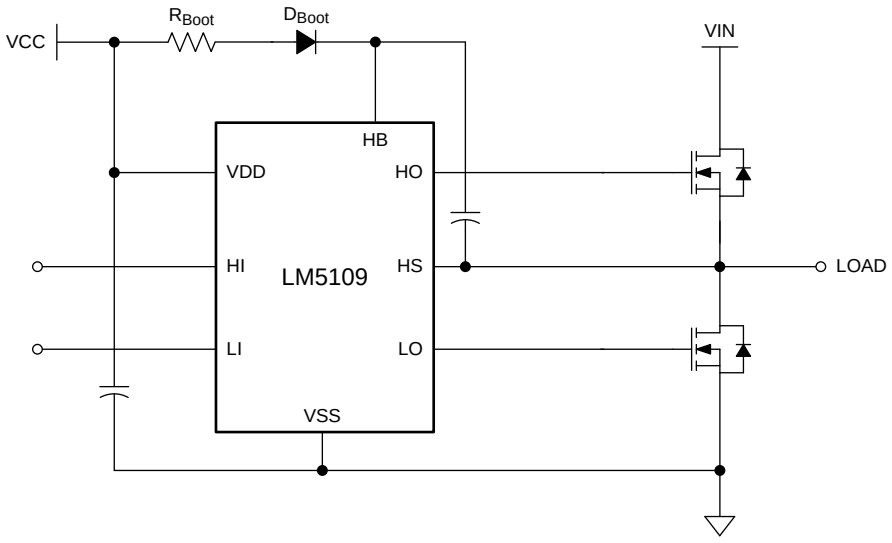
LM5109B-Q1 是一款具有成本效益的高电压栅极驱动器，设计用于驱动采用同步降压或半桥配置的高侧和低侧 N 沟道 MOSFET。悬空高侧驱动器能够在高达 90V 的电源轨电压下工作。输出通过兼容 TTL/CMOS 的逻辑输入阈值独立控制。稳健可靠的电平转换技术同时拥有高运行速度和低功耗特性，并且可提供从控制输入逻辑到高侧栅极驱动器的干净电平转换。该器件在低侧和高侧电源轨上提供了欠压锁定功能。该器件采用耐热增强型 WSON(8) 封装。

器件信息(1)

部件号	封装	封装尺寸（标称值）
LM5109B-Q1	WSON (8)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化的应用示意图



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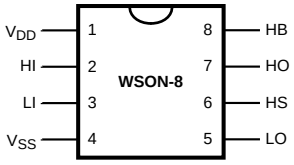
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (November 2015) to Revision A	Page
• 已将器件状态由“产品预览”更改为“量产数据”并发布为完整数据表	1

5 Pin Configuration and Functions

NGT Package
8-Pin WSON
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION	APPLICATIONS INFORMATION
NO.(2)	NAME			
1	V_{DD}	P	Positive gate drive supply	Locally decouple to V_{SS} using low ESR/ESL capacitor located as close to IC as possible.
2	HI	I	High side control input	The HI input is TTL/CMOS Compatible input thresholds. Unused HI input should be tied to ground and not left open.
3	LI	I	Low side control input	The LI input is TTL/CMOS Compatible input thresholds. Unused LI input should be tied to ground and not left open.
4	V_{SS}	G	Ground reference	All signals are referenced to this ground.
5	LO	O	Low side gate driver output	Connect to the gate of the low-side N-MOS device.
6	HS	P	High side source connection	Connect to the negative terminal of the bootstrap capacitor and to the source of the high-side N-MOS device.
7	HO	O	High side gate driver output	Connect to the gate of the high-side N-MOS device.
8	HB	P	High side gate driver positive supply rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal of the bootstrap capacitor to HS. The bootstrap capacitor should be placed as close to IC as possible.

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output
(2) For WSON-8 package, it is recommended that the exposed pad on the bottom of the package be soldered to ground plane on the PCB and the ground plane should extend out from underneath the package to improve heat dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{DD} to V_{SS}	–0.3	18	V
HB to HS	–0.3	18	V
LI or HI to V_{SS}	–0.3	V_{DD} + 0.3	V
LO to V_{SS}	–0.3	V_{DD} + 0.3	V
HO to V_{SS}	V_{HS} – 0.3	V_{HB} + 0.3	V
HS to V_{SS}(2)	–5	90	V
HB to V_{SS}		108	V
Junction temperature	–40	150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) In the application, the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed –1 V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} – 15 V. For example, if V_{DD} = 10 V, the negative transients at HS must not exceed –5 V.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	1500	V
	Charged-device model (CDM), per AEC Q100-011	750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{DD}	8		14	V
HS(1)	–1		90	V
HB	V_{HS}+8		V_{HS}+14	V
HS Slew Rate			< 50	V/ns
Junction Temperature	–40		125	°C

(1) In the application, the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed –1 V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} – 15 V. For example, if V_{DD} = 10 V, the negative transients at HS must not exceed –5 V.

6.4 Thermal Information

THERMAL METRIC(1)		LM5109B-Q1 NGT (WSON) 8-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

T_J = 25°C (unless otherwise noted)
V_{DD} = V_{HB} = 12 V, V_{SS} = V_{HS} = 0 V, No Load on LO or HO.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Supply Currents							
I_{DD}	V_{DD} Quiescent Current	LI = HI = 0V	T_J = 25°C		0.3		mA
			T_J = –40°C to 125°C			0.6	
I_{DDO}	V_{DD} Operating Current	f = 500 kHz	T_J = 25°C		1.8		mA
			T_J = –40°C to 125°C			2.9	
I_{HB}	Total HB Quiescent Current	LI = HI = 0V	T_J = 25°C		0.06		mA
			T_J = –40°C to 125°C			0.2	
I_{HBO}	Total HB Operating Current	f = 500 kHz	T_J = 25°C		1.4		mA
			T_J = –40°C to 125°C			2.8	
I_{HBS}	HB to V_{SS} Current, Quiescent	V_{HS} = V_{HB} = 90V	T_J = 25°C		0.1		µA
			T_J = –40°C to 125°C			10	
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz			0.5		mA
Input Pins Li and Hi							
V_{IL}	Low Level Input Voltage Threshold	T_J = 25°C			1.8		V
		T_J = –40°C to 125°C		0.8			
V_{IH}	High Level Input Voltage Threshold	T_J = 25°C			1.8		V
		T_J = –40°C to 125°C				2.2	
R_I	Input Pulldown Resistance	T_J = 25°C			200		kΩ
		T_J = –40°C to 125°C		100		500	
Under Voltage Protection							
V_{DDR}	V_{DD} Rising Threshold	V_{DDR} = V_{DD} - V_{SS}	T_J = 25°C		6.7		V
			T_J = –40°C to 125°C	6.0		7.4	
V_{DDH}	V_{DD} Threshold Hysteresis				0.5		V
V_{HBR}	HB Rising Threshold	V_{HBR} = V_{HB} - V_{HS}	T_J = 25°C		6.6		V
			T_J = –40°C to 125°C	5.7		7.1	
V_{HBH}	HB Threshold Hysteresis				0.4		V
LO Gate Driver							
V_{OLL}	Low-Level Output Voltage	I_{LO} = 100 mA, V_{OHL} = V_{LO} – V_{SS}	T_J = 25°C		0.38		V
			T_J = –40°C to 125°C			0.65	
V_{OHL}	High-Level Output Voltage	I_{LO} = −100 mA, V_{OHL} = V_{DD}– V_{LO}	T_J = 25°C		0.72		V
			T_J = –40°C to 125°C			1.20	
I_{OHL}	Peak Pullup Current	V_{LO} = 0V			1.0		A
I_{OLL}	Peak Pulldown Current	V_{LO} = 12V			1.0		A

Electrical Characteristics (continued)

T_J = 25°C (unless otherwise noted)
V_{DD} = V_{HB} = 12 V, V_{SS} = V_{HS} = 0 V, No Load on LO or HO.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HO Gate Driver							
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA, V_{OLH} = V_{HO}– V_{HS}	T_J = 25°C		0.38		V
			T_J = –40°C to 125°C			0.65	
V_{OHH}	High-Level Output Voltage	I_{HO} = −100 mA, V_{OHH} = V_{HB}– V_{HO}	T_J = 25°C		0.72		V
			T_J = –40°C to 125°C			1.20	
I_{OHH}	Peak Pullup Current	V_{HO} = 0V			1.0		A
I_{OLH}	Peak Pulldown Current	V_{HO} = 12V			1.0		A

6.6 Switching Characteristics

T_J = 25°C (unless otherwise noted)
V_{DD} = V_{HB} = 12 V, V_{SS} = V_{HS} = 0 V, No Load on LO or HO.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LPHL}	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	T_J = 25°C		30		ns
		T_J = –40°C to 125°C			56	
t_{HPHL}	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	T_J = 25°C		30		ns
		T_J = –40°C to 125°C			56	
t_{LPLH}	Lower Turn-On Propagation Delay (LI Rising to LO Rising)	T_J = 25°C		32		ns
		T_J = –40°C to 125°C			56	
t_{HPLH}	Upper Turn-On Propagation Delay (HI Rising to HO Rising)	T_J = 25°C		32		ns
		T_J = –40°C to 125°C			56	
t_{MON}	Delay Matching: Lower Turn-On and Upper Turn-Off	T_J = 25°C		2		ns
		T_J = –40°C to 125°C			15	
t_{MOFF}	Delay Matching: Lower Turn-Off and Upper Turn-On	T_J = 25°C		2		ns
		T_J = –40°C to 125°C			15	
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		15		ns
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns

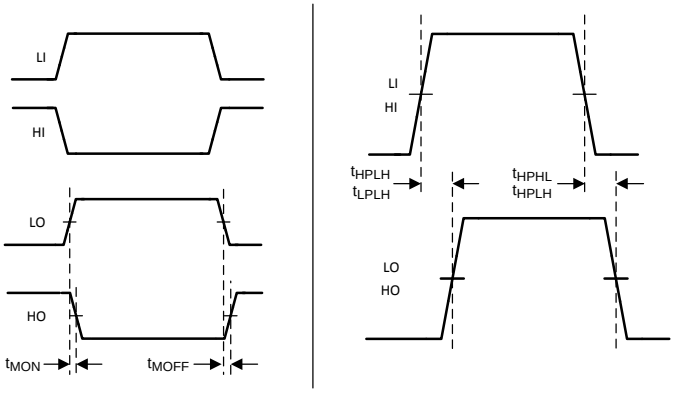


Figure 1. Typical Test Timing Diagram

6.7 Typical Characteristics

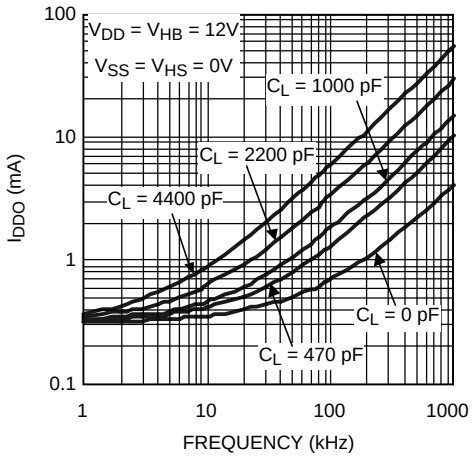
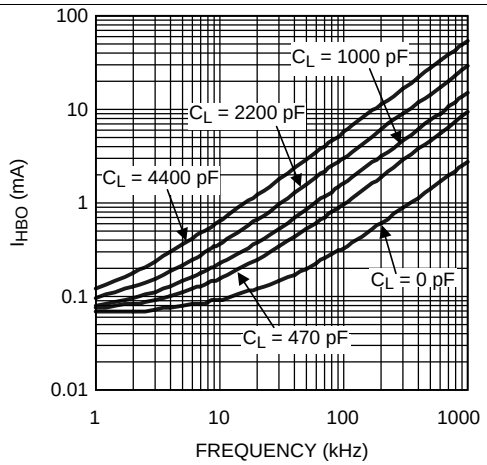


Figure 2. V_{DD} Operating Current vs Frequency



V_{DD} = V_{HB} = 12 V V_{SS} = V_{HS} = 0 V

Figure 3. HB Operating Current vs Frequency

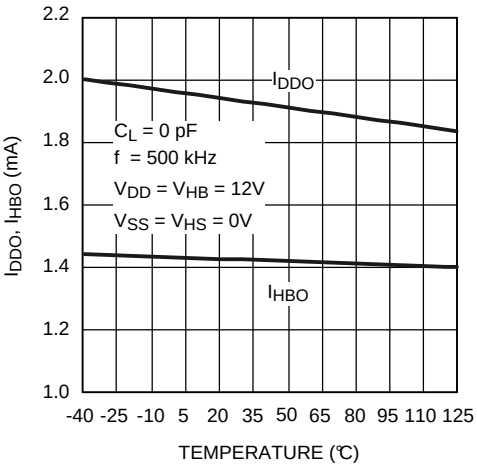


Figure 4. Operating Current vs Temperature

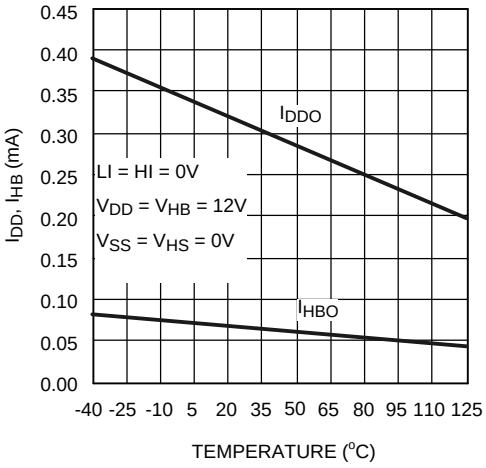


Figure 5. Quiescent Current vs Temperature

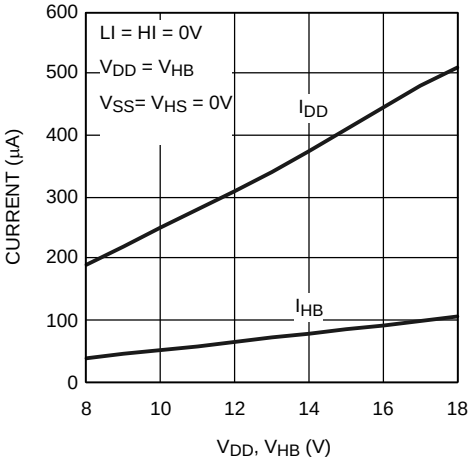


Figure 6. Quiescent Current vs Voltage

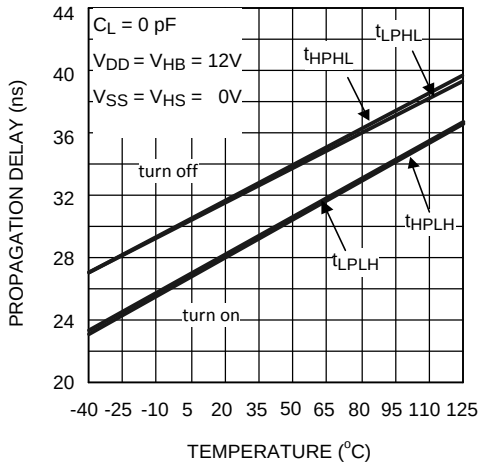


Figure 7. Propagation Delay vs Temperature

Typical Characteristics (continued)

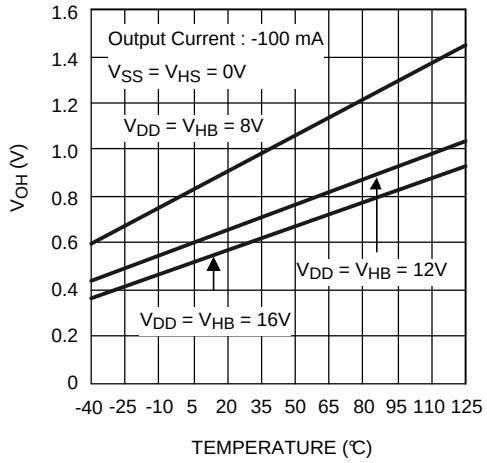


Figure 8. LO and HO High Level Output Voltage vs Temperature

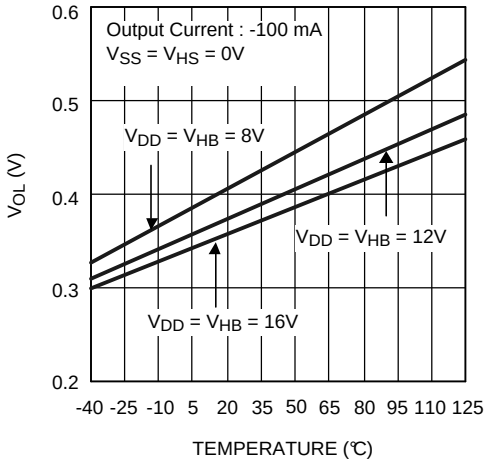


Figure 9. LO and HO Low Level Output Voltage vs Temperature

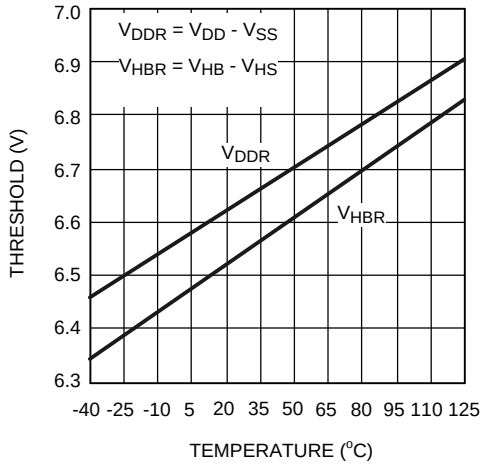


Figure 10. Undervoltage Rising Thresholds vs Temperature

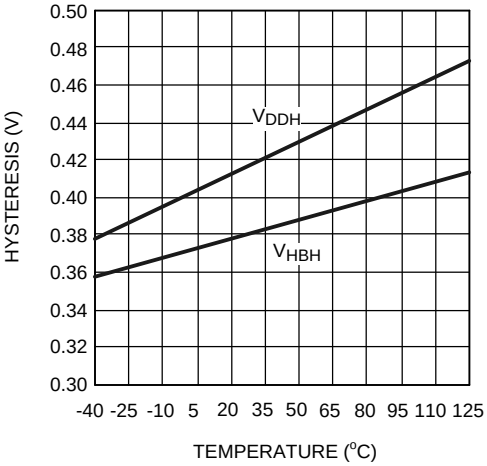


Figure 11. Undervoltage Hysteresis vs Temperature

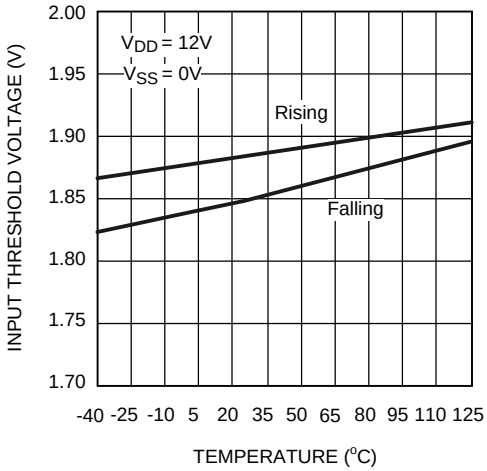


Figure 12. Input Thresholds vs Temperature

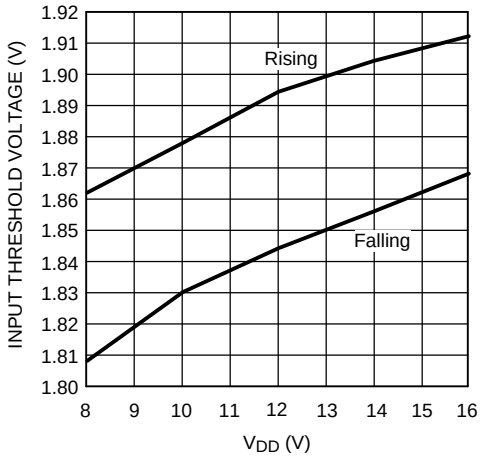


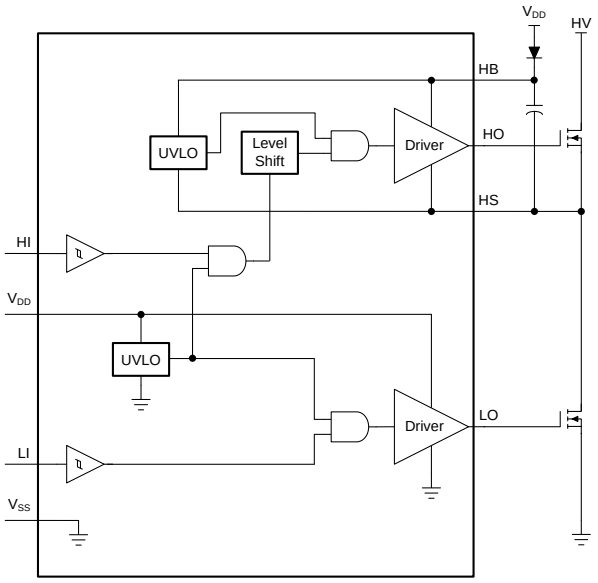
Figure 13. Input Thresholds vs Supply Voltage

7 Detailed Description

7.1 Overview

The LM5109B-Q1 is a cost-effective, high voltage gate driver designed to drive both the high-side and the low-side N-channel FETs in a synchronous buck or a half-bridge configuration. The outputs are independently controlled with TTL/CMOS compatible input thresholds. The floating high-side driver is capable of working with HB voltage up to 108 V. An external high voltage diode must be provided to charge high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high side gate driver. Under-voltage lockout (UVLO) is provided on both the low side and the high side power rails.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Start-up and UVLO

Both top and bottom drivers include UVLO protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage ($V_{HB–HS}$) independently. The UVLO circuit inhibits each output until sufficient supply voltage is available to turn on the external MOSFETs, and the built-in UVLO hysteresis prevents chattering during supply voltage variations. When the supply voltage is applied to the VDD pin of the LM5109B-Q1, the top and bottom gates are held low until V_{DD} exceeds the UVLO threshold, typically about 6.7 V. Any UVLO condition on the bootstrap capacitor ($V_{HB–HS}$) will only disable the high- side output (HO).

Table 1. VDD UVLO Feature Logic Operation

Condition (V_{HB-HS}>V_{HBR} for all case below)	HI	LI	HO	LO
V_{DD}-V_{SS} < V_{DDR} during device start-up	H	L	L	L
V_{DD}-V_{SS} < V_{DDR} during device start-up	L	H	L	L
V_{DD}-V_{SS} < V_{DDR} during device start-up	H	H	L	L
V_{DD}-V_{SS} < V_{DDR} during device start-up	L	L	L	L
V_{DD}-V_{SS} < V_{DDR} – V_{DDH} after device start-up	H	L	L	L
V_{DD}-V_{SS} < V_{DDR} – V_{DDH} after device start-up	L	H	L	L
V_{DD}-V_{SS} < V_{DDR} – V_{DDH} after device start-up	H	H	L	L
V_{DD}-V_{SS} < V_{DDR} – V_{DDH} after device start-up	L	L	L	L

Table 2. VHB-HS UVLO Feature Logic Operation

Condition (V_{DD}>V_{DDR} for all case below)	HI	LI	HO	LO
V_{HB-HS} < V_{HBR} during device start-up	H	L	L	L
V_{HB-HS} < V_{HBR} during device start-up	L	H	L	H
V_{HB-HS} < V_{HBR} during device start-up	H	H	L	H
V_{HB-HS} < V_{HBR} during device start-up	L	L	L	L
V_{HB-HS} < V_{HBR} – V_{HBH} after device start-up	H	L	L	L
V_{HB-HS} < V_{HBR} – V_{HBH} after device start-up	L	H	L	H
V_{HB-HS} < V_{HBR} – V_{HBH} after device start-up	H	H	L	H
V_{HB-HS} < V_{HBR} – V_{HBH} after device start-up	L	L	L	L

7.3.2 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output which is referenced to the HS pin and provides excellent delay matching with the low-side driver.

7.3.3 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance, and high peak current capability of both outputs allow for efficient switching of the power MOSFETs. The low-side output stage is referenced to VSS and the high-side is referenced to HS.

7.4 HS Transient Voltages Below Ground

The HS node will always be clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than –0.3 V below HS can activate parasitic transistors resulting in excessive current flow from the HB supply, possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible in order to be effective.
2. HB to HS operating voltage should be 15 V or less. Hence, if the HS pin transient voltage is –5 V, VDD should be ideally limited to 10 V to keep HB to HS below 15 V.
3. Low ESR bypass capacitors from HB to HS and from VDD to VSS are essential for proper operation. The capacitor should be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductances with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

7.5 Device Functional Modes

The device operates in normal mode and UVLO mode. See **Start-up and UVLO** for more information on UVLO operation mode. In normal mode when the V_{DD} and $V_{HB–HS}$ are above UVLO threshold, the output stage is dependent on the states of the HI and LI pins. The output HO and LO will be low if input state is floating.

Table 3. INPUT/OUTPUT Logic Table

HI	LI	HO(1)	LO(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
Floating	**Floating**	L	L

(1) HO is measured with respect to the HS.
(2) LO is measured with respect to the VSS.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To operate fast switching of power MOSFETs at high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3 V logic signal which cannot effectively turn on a power switch. Level shift circuit is needed to boost the 3.3 V signal to the gate-drive voltage (such as 12 V) in order to fully turn-on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver IC physically close to the power switch), driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The LM5109B-Q1 is the high voltage gate drivers designed to drive both the high-side and low-side N-Channel MOSFETs in a half-bridge/full bridge configuration or in a synchronous buck circuit. The floating high side driver is capable of operating with supply voltages up to 90V. This allows for N-Channel MOSFETs control in half-bridge, full-bridge, push-pull, two switch forward and active clamp topologies. The outputs are independently controlled. Each channel is controlled by its respective input pins (HI and LI), allowing full and independent flexibility to control ON and OFF state of the output.

8.2 Typical Application

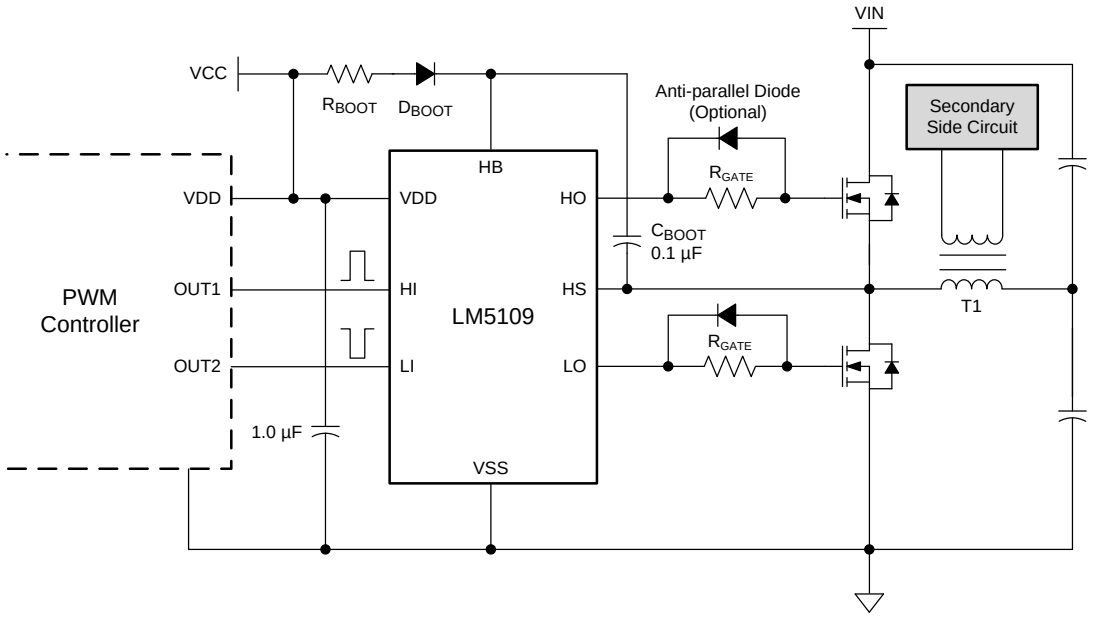


Figure 14. LM5109B-Q1 Driving MOSFETs in a Half Bridge Converter

Typical Application (continued)

8.2.1 Design Requirements

Table 4. Design Example

PARAMETER	VALUE
Gate Driver	LM5109B-Q1
MOSFET	CSD19534KCS
V_{DD}	10 V
Q_G	17 nC
f_{SW}	500 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Select Bootstrap and VDD Capacitor

The bootstrap capacitor must maintain the V_{HB-HS} voltage above the UVLO threshold for normal operation. Calculate the maximum allowable drop across the bootstrap capacitor with Equation 1.

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL} = 10\ V - 1\ V - 6.7\ V = 2.3\ V \quad (1)$$

where

- V_{DD} = Supply voltage of the gate drive IC;
- V_{DH} = Bootstrap diode forward voltage drop;
- $V_{HBL} = V_{HBRmax} - V_{HBH}$, HB falling threshold;

Then, the total charge needed per switching cycle could be estimated by Equation 2.

$$Q_{Total} = Q_G + I_{HBS} \times \frac{D_{Max}}{f_{SW}} + \frac{I_{HB}}{f_{SW}} = 17\ nC + 10\ \mu A \times \frac{0.95}{500\ kHz} + \frac{0.2\ mA}{500\ kHz} = 17.5\ nC \quad (2)$$

where

- Q_G: Total MOSFET gate charge
- I_{HBS}: HB to VSS Leakage current
- D_{Max}: Converter maximum duty cycle
- I_{HB}: HB Quiescent current

Therefore, the minimum C_{Boot} should be:

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{HB}} = \frac{17.5\ nC}{2.3\ V} = 7.6\ nF \quad (3)$$

In practice, the value of the C_{Boot} capacitor should be greater than calculated to allow for situations where the power stage may skip pulse due to load transients. It is recommended to have enough margins and place the bootstrap capacitor as close to the HB and HS pins as possible.

$$C_{Boot} = 100\ nF \quad (4)$$

As a general rule the local V_{DD} bypass capacitor should be 10 times greater than the value of C_{Boot}, as shown in Equation 5.

$$C_{VDD} = 1\ \mu F \quad (5)$$

The bootstrap and bias capacitors should be ceramic types with X7R dielectric. The voltage rating should be twice that of the maximum V_{DD} considering capacitance tolerances once the devices have a DC bias voltage across them and to ensure long-term reliability.

8.2.2.2 Select External Bootstrap Diode and Its Series Resistor

The bootstrap capacitor is charged by the V_{DD} through the external bootstrap diode every cycle when low side MOSFET turns on. The charging of the capacitor involves high peak currents, and therefore transient power dissipation in the bootstrap diode may be significant and the conduction loss also depends on its forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

For the selection of external bootstrap diodes, please refer to the application note SNVA083A. Bootstrap resistor R_{BOOT} is selected to reduce the inrush current in D_{BOOT} and limit the ramp up slew rate of voltage of V_{HB-HS} during each switching cycle, especially when HS pin have excessive negative transient voltage. R_{BOOT} recommended value is between 2 Ω and 10 Ω depending on diode selection. A current limiting resistor of 2.2 Ω is selected to limit inrush current of bootstrap diode, and the estimated peak current on the D_{Boot} is shown in Equation 6.

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{DH}}{R_{Boot}} = \frac{10\ V - 1\ V}{2.2\ \Omega} \approx 4\ A$$

where

- V_{DH} is the Bootstrap diode forward voltage drop (6)

8.2.2.3 Selecting External Gate Driver Resistor

External Gate Driver Resistor, R_{GATE}, is sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the current coming out of the gate driver.

Peak HO pull-up current are calculated by the following equations.

$$I_{OHH} = \frac{V_{DD} - V_{DH}}{R_{HOH} + R_{Gate} + R_{GFET\_Int}} = \frac{10\ V - 1\ V}{1.2\ V / 100\ mA + 4.7\ \Omega + 2.2\ \Omega} = 0.48\ A$$

where

- I_{OHH} – Peak pull-up current;
- V_{DH} – Bootstrap diode forward voltage drop;
- R_{HOH} – Gate driver internal HO pull-up resistance, provide by driver datasheet directly or estimated from the testing conditions, i.e. $R_{HOH}=V_{OHH}/I_{HO}$;
- R_{Gate} – External gate drive resistance;
- $R_{(GFET\_Int)}$ – MOSFET internal gate resistance, provided by transistor datasheet; (7)

Similarly, Peak HO pull-down current is shown in Equation 8.

$$I_{OLH} = \frac{V_{DD} - V_{DH}}{R_{HOL} + R_{Gate} + R_{GFET\_Int}}$$

where

- R_{HOL} is HO pull-down resistance (8)

Peak LO pullup current is shown in Equation 9.

$$I_{OHL} = \frac{V_{DD}}{R_{LOH} + R_{Gate} + R_{GFET\_Int}}$$

where

- R_{LOH} is LO pull-up resistance. (9)

Peak LO pulldown current is shown in Equation 10.

$$I_{OLL} = \frac{V_{DD}}{R_{LOL} + R_{Gate} + R_{FET\_Int}}$$

where

- R_{LOL} is LO pull-down resistance (10)

For some scenarios, if the applications require fast turn-off, an anti-paralleled diode on R_{Gate} could be used to bypass the external gate drive resistor and speed-up turn-off transition.

8.2.2.4 Estimate the Driver Power Loss

The total driver IC power dissipation can be estimated through the following components.

1. Static power losses, P_{QC}, due to quiescent current – I_{DD} and I_{HB};

$$P_{QC} = V_{DD} \times I_{DD} + (V_{DD} - V_{DH}) \times I_{HB} \quad (11)$$

2. Level-shifter losses, P_{IHBS}, due high side leakage current – IHBS;

$$P_{IHBS} = V_{HB} \times I_{HBS} \times D \quad (12)$$

where

- D is high side switch duty cycle

3. Dynamic losses, $P_{QG1\&2}$, due to the FETs gate charge – Q_G;

$$P_{QG1\&2} = 2 \times V_{DD} \times Q_G \times f_{SW} \times \frac{R_{GD\_R}}{R_{GD\_R} + R_{Gate} + R_{GFET\_Int}} \quad (13)$$

where

- Q_G is total FETs gate charge;
- f_{SW} is switching frequency;
- R_{GD_R} is average value of pull-up and pull-down resistor;
- R_{Gate} is external gate drive resistor;
- R_{GFET_Int} is internal FETs gate resistor;

4. Level-shifter dynamic losses, P_{LS}, during high side switching due to required level-shifter charge on each switching cycle – Q_P;

$$P_{LS} = V_{HB} \times Q_P \times f_{SW} \quad (14)$$

In this example, the estimated gate driver loss in LM5109B-Q1 is shown in Equation 15.

$$P_{LM5109BQ} = 10\ V \times 0.6\ mA + 9\ V \times 0.2\ mA + 72\ V \times 10\ \mu A \times 0.95 + 2 \times 10 \times 17\ nC \times 500\ kHz \times \frac{12\ \Omega}{12\ \Omega + 4.7\ \Omega + 2.2\ \Omega} + 72\ V \times 0.5\ nC \times 500\ kHz = 0.134\ W \quad (15)$$

For a given ambient temperature, the maximum allowable power loss of the IC can be defined as shown in Equation 16.

$$P_{LM5109BQ} = \frac{T_J - T_A}{R_{\theta JA}} \quad (16)$$

where

- $P_{LM5109BQ}$ = The total power dissipation of the driver
- T_J = Junction temperature
- T_A = Ambient temperature
- $R_{\theta JA}$ = Junction-to-ambient thermal resistance

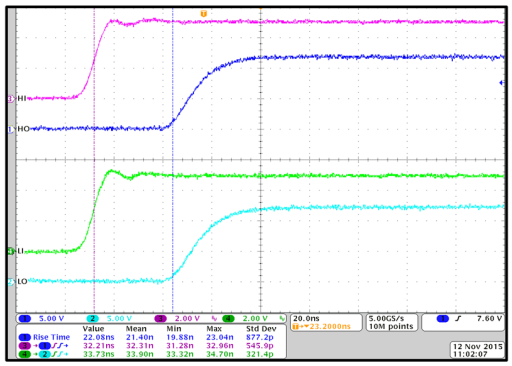
The thermal metrics for the driver package is summarized in the Thermal Information section of the datasheet. For detailed information regarding the thermal information table, please refer to the Texas Instruments application note entitled *Semiconductor and IC Package Thermal Metrics* (SPRA953.).

8.2.3 Application Curves

Figure 15 and Figure 16 shows the rising/falling time and turn-on/off propagation delay testing waveform in room temperature, and waveform measurement data (see the bottom part of the waveform). Each channel, HI/LI/HO/LO, is labeled and displayed on the left hand of the waveforms.

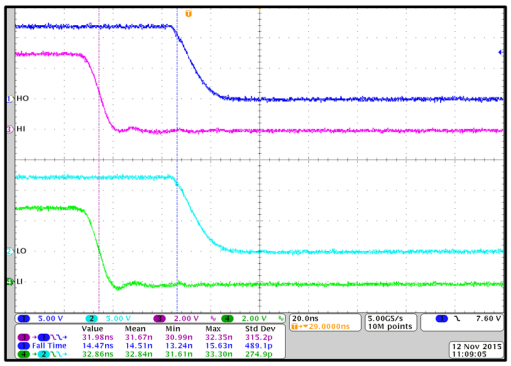
The testing condition: load capacitance is 1 nF, V_{DD} = 12 V, f_{SW} = 500 kHz.

HI and LI share one same input from function generator, therefore, besides the propagation delay and rising/falling time, the difference of the propagation delay between HO and LO gives the propagation delay matching data.



C_L = 1 nF V_{DD} = 12 V f_{SW} = 500 kHz

Figure 15. Rising Time and Turn-On Propagation Delay



C_L = 1 nF V_{DD} = 12 V f_{SW} = 500 kHz

Figure 16. Falling Time and Turn-Off Propagation Delay

9 Power Supply Recommendations

The recommended bias supply voltage range for LM5109B-Q1 is from 8 V to 14 V. The lower end of this range is governed by the internal under voltage-lockout (UVLO) protection feature of the V_{DD} supply circuit blocks. The upper-end of this range is driven by the 18-V absolute maximum voltage rating of the V_{DD}. It is recommended to keep a 4-V margin to allow for transient voltage spikes.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the V_{DD} voltage drops, the device continues to operate in normal mode as far as the voltage drop do not exceeds the hysteresis specification, V_{DDH}. If the voltage drop is more than hysteresis specification, the device will shut down. Therefore, while operating at or near the 8-V range, the voltage ripple on the auxiliary power supply output should be smaller than the hysteresis specification of LM5109B-Q1 to avoid triggering device-shutdown.

A local bypass capacitor should be placed between the VDD and GND pins. And this capacitor should be located as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100 nF ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220 nF to 10 µF, for IC bias requirements. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore, a 22-nF to 220-nF local decoupling capacitor is recommended between the HB and HS pins.

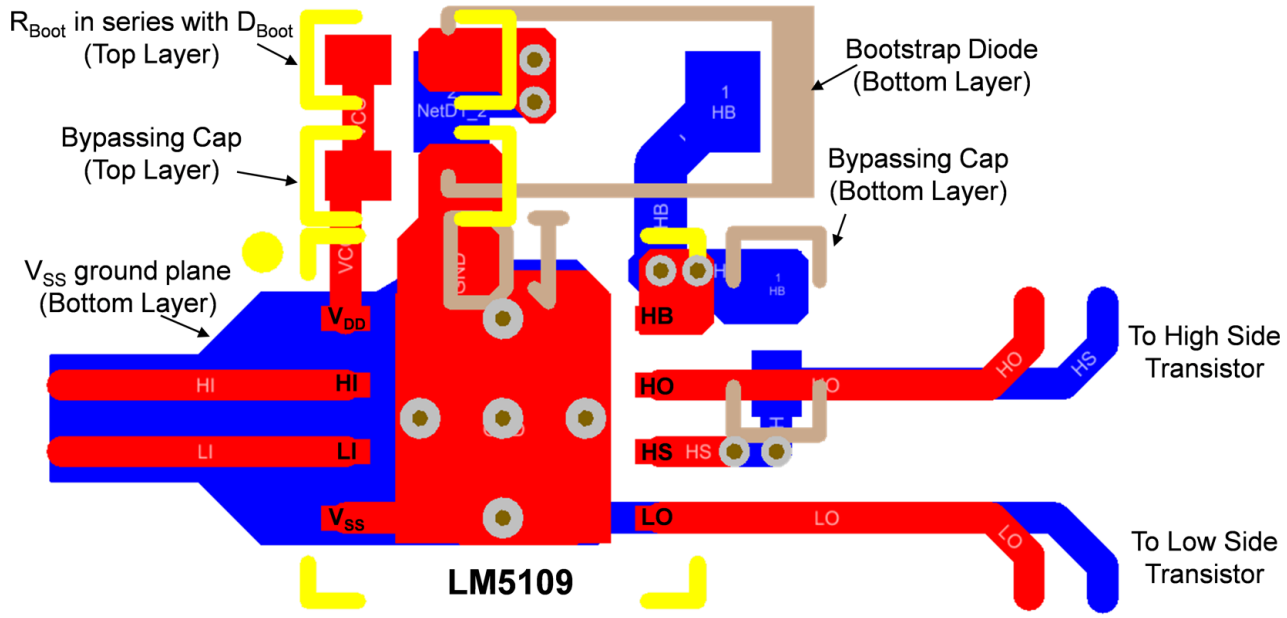
10 Layout

10.1 Layout Guidelines

Optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low ESR/ESL capacitors must be connected close to the IC between VDD and VSS pins and between HB and HS pins to support high peak currents drawn from VDD and HB during the turn-on of the external MOSFETs.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the MOSFET drain and ground (VSS).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances between the source of the high side MOSFET and the drain of the low side MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
   – The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver should be placed as close as possible to the MOSFETs.
   – The second consideration is the high current path that includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and the low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

10.2 Layout Example



11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.3 静电放电警告

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11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5109BQNGTRQ1	ACTIVE	WSON	NGT	8	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L5109Q	Samples
LM5109BQNGTTQ1	ACTIVE	WSON	NGT	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L5109Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

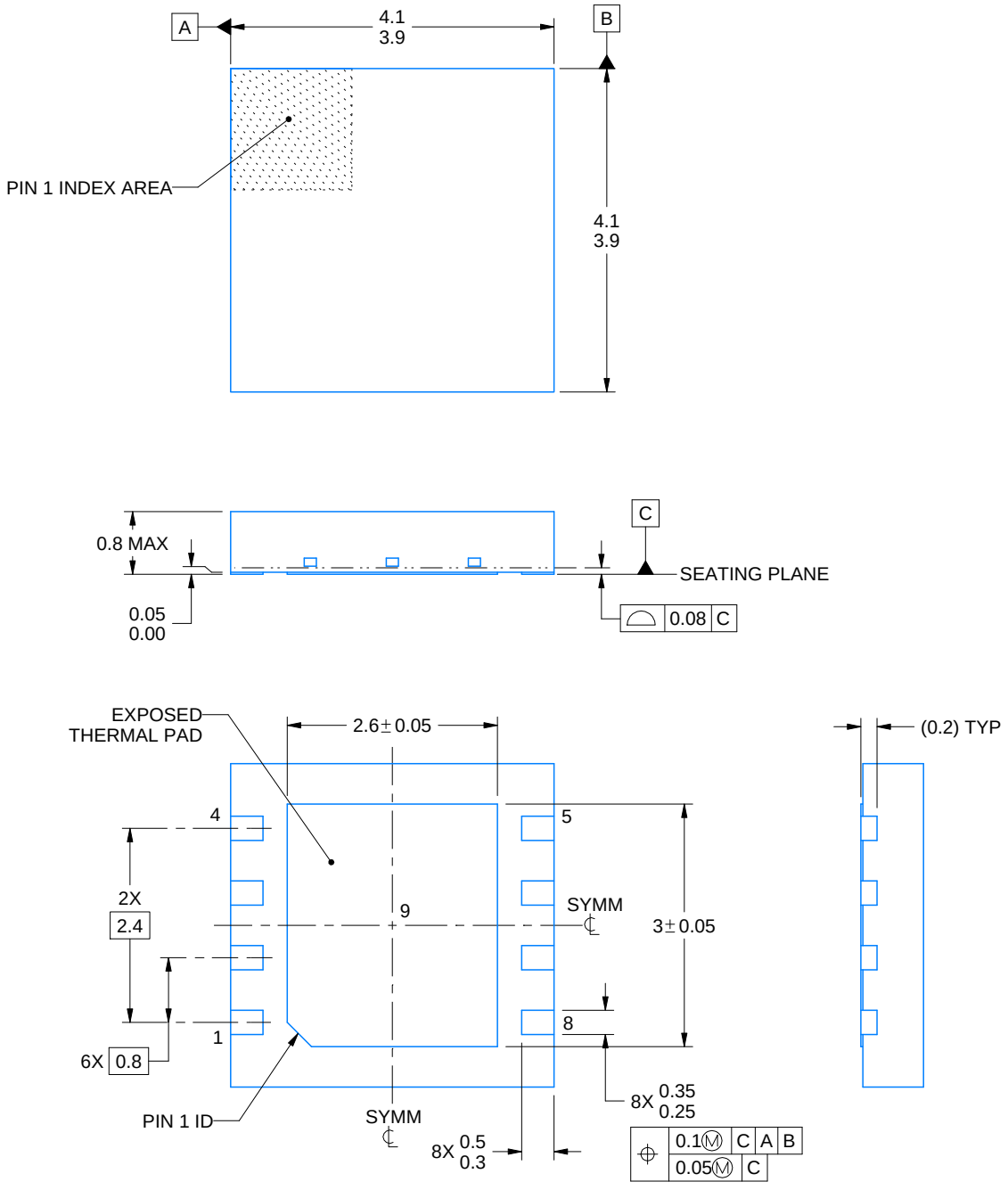
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

NGT0008A

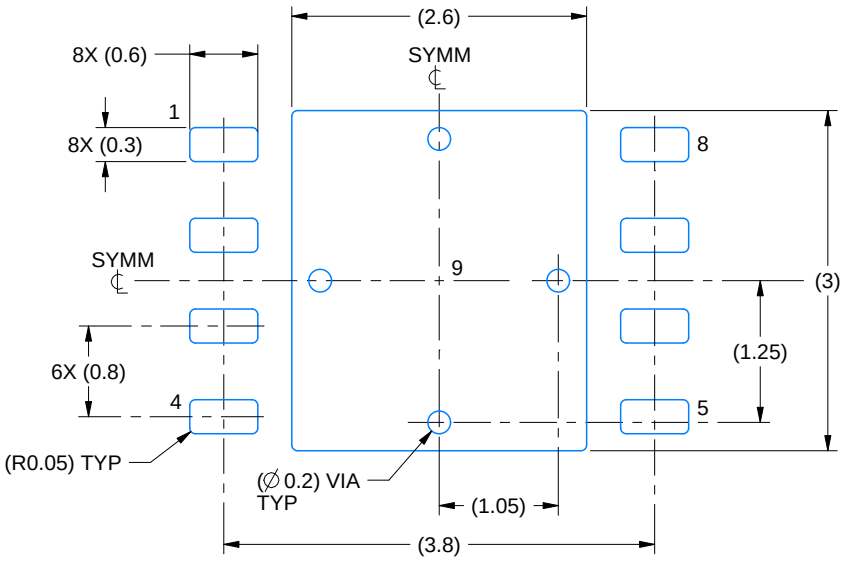
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

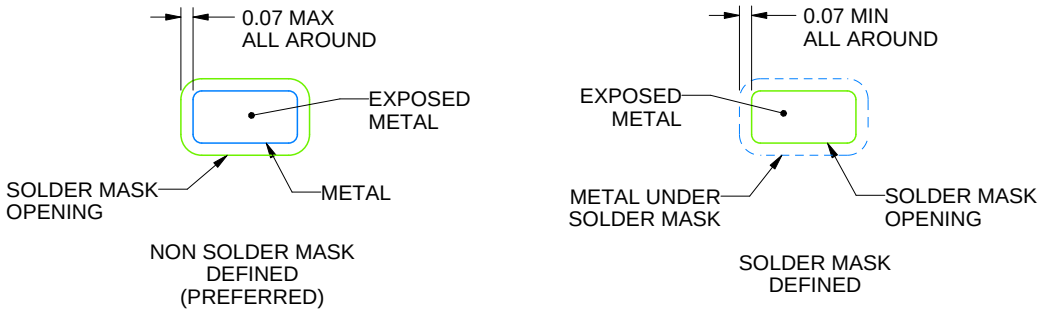


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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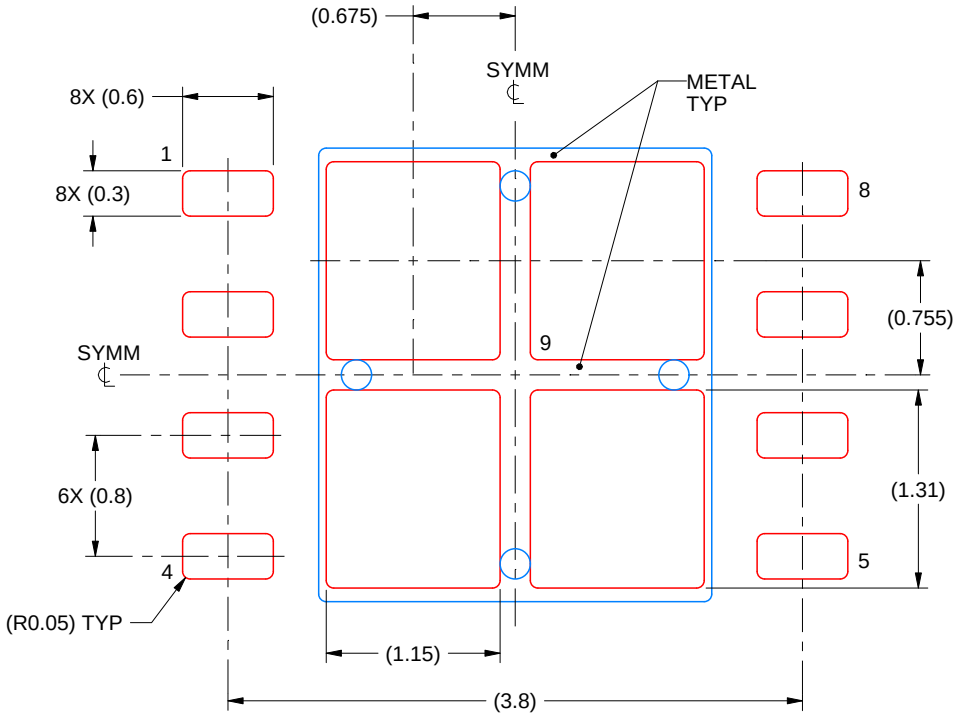
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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