LM5155x-Q1 2.2MHz 宽输入非同步升压、SEPIC、反激式控制器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C 至 +125°C T_A
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 适用于汽车和便携式电池应用的宽输入工作范围
  - 3.5V 至 45V 工作范围
  - 当 BIAS = VCC 时，为 2.97V 至 16V
  - BIAS 电压大于等于 3.5V 时最小升压电源电压为 1.5V
  - 高达 50V 的输入瞬态保护
- 最小电池消耗
  - 低关断电流 (I_Q ≤ 2.6μA)
  - 低工作电流 (I_Q ≤ 480μA)
- 解决方案尺寸小、成本低
  - 最大开关频率为 2.2MHz
  - 具有可湿性侧面的 12 引脚 WSON 封装 (3mm × 2mm)
  - 集成的误差放大器支持在没有光耦合器的情况下进行初级侧稳压（反激）
  - 启动期间下冲最小化（启停应用）
- 低功耗、高效率
  - 100mV ±7% 低限流阈值
  - 强大的 1.5A 峰值标准 MOSFET 驱动器
  - 支持外部 VCC 电源
- 避免 AM 频带干扰和串扰
  - 可选的时钟同步
  - 100kHz 至 2.2MHz 的动态可编程开关频率
- 集成型保护特性
  - 在输入电压范围内具有恒定峰值电流限制
  - 可选断续模式短路保护（参阅*器件比较表*）
  - 可编程线路 UVLO
  - OVP 保护
  - 热关断保护
- 精确的 ±1% 精度反馈基准
- 可编程额外斜率补偿
- 可调软启动
- PGOOD 指示器
- 使用 LM5155x 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 汽车启停应用
- 高电压激光雷达电源
- 无光耦合器的多输出反激式应用
- 汽车尾灯 LED 偏置电源
- 宽输入升压、SEPIC 和反激式电源模块
- 便携式扬声器应用
- 电池供电的升压、SEPIC 和反激式应用

3 说明

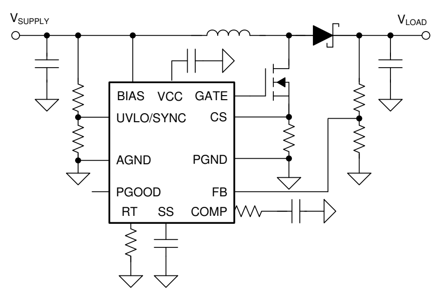
LM5155x-Q1（LM5155-Q1 和 LM51551-Q1）是一款采用峰值电流模式控制、具有宽输入范围的非同步升压控制器。该器件可用于升压、SEPIC 和反激式拓扑。

如果 BIAS 引脚连接到 VCC 引脚，则 M5155x-Q1 可由单节电池（最低电压为 2.97V）供电。如果 BIAS 引脚电压高于 3.5V，则该器件可使用低至 1.5V 的输入电源电压。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
LM5155x-Q1	WSON (12)	3.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型升压应用

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (June 2020) to Revision E (January 2021)	Page
• 更新了整个文档的表、图和交叉参考的编号格式。	1

Changes from Revision C (January 2020) to Revision D (June 2020)	Page
• Removed "TBD" from the title of 图 9-16	17

Changes from Revision B (July 2019) to Revision C (January 2020)	Page
• 向“特性”列表添加了“提供功能安全”	1

Changes from Revision A (December 2018) to Revision B (July 2019)	Page
• 将“预告信息”更改为“量产数据”并添加了 LM51551-Q1	1

5 Description (continued)

The internal VCC regulator also supports BIAS pin operation up to 45 V (50-V absolute maximum) for automotive load dump. The switching frequency is dynamically programmable with an external resistor from 100 kHz to 2.2 MHz. Switching at 2.2 MHz minimizes AM band interference and allows for a small solution size and fast transient response.

The device features a 1.5-A standard MOSFET driver and a low 100-mV current limit threshold. The device also supports the use of an external VCC supply to improve efficiency. Low operating current and pulse-skipping operation improve efficiency at light loads.

The device has built-in protection features such as cycle-by-cycle current limit, overvoltage protection, line UVLO, and thermal shutdown. Hiccup mode overload protection is available in the LM51551-Q1 device option. Additional features include low shutdown I_Q, programmable soft start, programmable slope compensation, precision reference, power-good indicator, and external clock synchronization.

6 Device Comparison Table

DEVICE OPTION	HICCUP MODE PROTECTION	INTERNAL REFERENCE
LM5155-Q1	Disabled	1 V
LM51551-Q1	Enabled	1 V

7 Pin Configuration and Functions

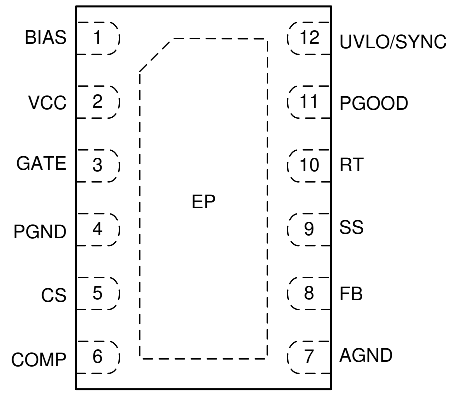


图 7-1. 12-Pin WSON With Wettable Flanks DSS Package (Top View)

表 7-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	BIAS	P	Supply voltage input to the VCC regulator. Connect a bypass capacitor from this pin to PGND.
2	VCC	P	Output of the internal VCC regulator and supply voltage input of the MOSFET driver. Connect a ceramic bypass capacitor from this pin to PGND.
3	GATE	O	N-channel MOSFET gate drive output. Connect directly to the gate of the N-channel MOSFET through a short, low inductance path.
4	PGND	G	Power ground pin. Connect directly to the ground connection of the sense resistor through a low inductance wide and short path.
5	CS	I	Current sense input pin. Connect to the positive side of the current sense resistor through a short path.
6	COMP	O	Output of the internal transconductance error amplifier. Connect the loop compensation components between this pin and PGND.
7	AGND	G	Analog ground pin. Connect to the analog ground plane through a wide and short path.
8	FB	I	Inverting input of the error amplifier. Connect a voltage divider from the output to this pin to set output voltage in boost/SEPIC topologies. Connect the low-side feedback resistor to AGND.
9	SS	I	Soft-start time programming pin. An external capacitor and an internal current source set the ramp rate of the internal error amplifier reference during soft start. Connect the ground connection of the capacitor to AGND.
10	RT	I	Switching frequency setting pin. The switching frequency is programmed by a single resistor between RT and AGND.
11	PGOOD	O	Power-good indicator. An open-drain output which goes low if FB is below the under voltage threshold. Connect a pullup resistor to the system voltage rail.
12	UVLO/EN/ SYNC	I	Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a resistor divider. The internal clock can be synchronized to an external clock by applying a negative pulse signal into the UVLO/EN/ SYNC pin. This pin must not be left floating. Connect to BIAS pin if not used. Connect the low-side UVLO resistor to AGND.
—	EP	—	Exposed pad of the package. The exposed pad must be connected to AGND and the large ground copper plane to decrease thermal resistance.

(1) G = Ground, I = Input, O = Output, P = Power

8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range[(1)]

		MIN	MAX	UNIT
Input	BIAS to AGND	–0.3	50	V
	UVLO to AGND	–0.3	V_{BIAS}+0.3	
	SS to AGND[(2)]	–0.3	3.8	
	RT to AGND[(2)]	–0.3	3.8	
	FB to AGND	–0.3	3.8	
	CS to AGND(DC)	–0.3	0.3	
	CS to AGND(100ns transient)	–1		
	CS to AGND(20ns transient)	–2		
	PGND to AGND	–0.3	0.3	
Output	VCC to AGND	–0.3	18[(3)]	V
	GATE to AGND (100ns transient)	–1		
	GATE to AGND (50ns transient)	–2		
	PGOOD to AGND[(4)]	–0.3	18	
	COMP to AGND[(5)]	–0.3		
Junction temperature, T_J [(6)]		–40	150	°C
Storage temperature, T_{stg}		–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This pin is not specified to have an external voltage applied.
(3) 18 V or V_{BIAS} + 0.3 V whichever is lower
(4) The maximum current sink is limited to 1 mA when V_{PGOOD}>V_{BIAS}.
(5) This pin has an internal max voltage clamp which can handle up to 1.6 mA.
(6) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)] HBM ESD Classification Level 2		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	All pins	±500	
			Corner pins (1, 6, 7, and 12)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise specified)[1]

		MIN	NOM	MAX	UNIT
V_{BIAS}	Bias input[2]	2.97		45	V
V_{VCC}	VCC voltage[3]	2.97		16	V
V_{UVLO}	UVLO input	0		45	V
V_{FB}	FB input	0		3.7	V
f_{SW}	Typical switching frequency	100		2200	kHz
f_{SYNC}	Synchronization pulse frequency	100		2200	kHz
T_J	Operating junction temperature[4]	–40		150	°C

(1) *Operating Ratings* are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.
(2) BIAS pin operating range is from 2.97 V to 16 V when VCC is directly connected to BIAS. BIAS pin operating range is from 3.5 V to 45 V when VCC is supplied from the internal VCC regulator.
(3) This pin voltage should be less than V_{BIAS} + 0.3 V.
(4) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

8.4 Thermal Information

THERMAL METRIC [1]		LM5155x-Q1 DSS(WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (LM5155EVM-BST)	37.0	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter (LM5155EVM-BST)	1.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter (LM5155EVM-BST)	18.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = -40°C to 125°C. Unless otherwise stated, V_{BIAS} = 12 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{SHUTDOWN(BIAS)}$	BIAS shutdown current	V_{BIAS} = 12 V, V_{UVLO} = 0 V		2.6	5	uA
$I_{OPERATING(BIAS)}$	BIAS operating current	V_{BIAS} = 12 V, V_{UVLO} = 2 V, V_{FB} = V_{REF}, R_T = 220 kΩ		480	540	uA
VCC REGULATOR						
$V_{VCC-REG}$	VCC regulation	V_{BIAS} = 8 V, No load	6.5	6.85	7	V
	VCC regulation	V_{BIAS} = 8 V, I_{VCC} = 35 mA	6.5			V
$V_{VCC-UVLO(RISING)}$	VCC UVLO threshold	VCC rising	2.75	2.85	2.95	V
	VCC UVLO hysteresis	VCC falling		0.063		V
I_{VCC-CL}	VCC sourcing current limit	V_{BIAS} = 10 V, V_{VCC} = 0 V	35	105		mA
ENABLE						
$V_{EN(RISING)}$	Enable threshold	EN rising	0.4	0.52	0.7	V

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = -40°C to 125°C. Unless otherwise stated, V_{BIAS} = 12 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{EN(FALLING)}$	Enable threshold	EN falling	0.33	0.49	0.63	V
$V_{EN(HYS)}$	Enable hysteresis	EN falling		0.03		V
UVLO/SYNC						
$V_{UVLO(RISING)}$	UVLO / SYNC threshold	UVLO rising	1.425	1.5	1.575	V
$V_{UVLO(FALLING)}$	UVLO / SYNC threshold	UVLO falling	1.370	1.45	1.520	V
$V_{UVLO(HYS)}$	UVLO / SYNC threshold hysteresis	UVLO falling		0.05		V
I_{UVLO}	UVLO hysteresis current	V_{UVLO} = 1.6 V	4	5	6	uA
SS						
I_{SS}	Soft-start current		9	10	11	uA
	SS pull-down switch R_{DSON}			55		Ω
PULSE WIDTH MODULATION						
fsw1	Switching frequency	R_T = 220 kΩ	85	100	115	kHz
fsw2	Switching frequency	R_T = 9.09 kΩ	1980	2200	2420	kHz
$t_{ON(MIN)}$	Minimum on-time	R_T = 9.09 kΩ		50		ns
D_{MAX1}	Maximum duty cycle limit	R_T = 9.09 kΩ	80%	85%	90%	
D_{MAX2}	Maximum duty cycle limit	R_T = 220 kΩ	90%	93%	96%	
CURRENT SENSE						
I_{SLOPE}	Peak slope compensation current	R_T = 220 kΩ	22.5	30	37.5	uA
V_{CLTH}	Current Limit threshold (CS-PGND)		93	100	107	mV
HICCUP MODE PROTECTION (LM51551)						
	Hiccup enable cycles			64		Cycles
	Hiccup timer reset cycles			8		Cycles
ERROR AMPLIFIER						
V_{REF}	FB reference	LM5155, LM51551	0.99	1	1.01	V
Gm	Transconductance			2		mA/V
	COMP sourcing current	V_{COMP} = 1.2 V	180			uA
	COMP clamp voltage	COMP rising (V_{UVLO} = 2.0V)	2.5	2.8		V
	COMP clamp voltage	COMP falling		1	1.1	V
OVP						
V_{OVTH}	Over-voltage threshold	FB rising (referece to V_{REF})	107%	110%	113%	
	Over-voltage threshold	FB falling (referece to V_{REF})		105%		
PGOOD						
	PGOOD pull-down switch R_{DSON}	1 mA sinking		90		Ω
V_{UVTH}	Undervoltage threshold	FB falling (referece to V_{REF})	87%	90%	93%	
	Undervoltage threshold	FB rising (referece to V_{REF})		95%		
MOSFET DRIVER						
	High-state voltage drop	100 mA sinking		0.25		V
	Low-state voltage drop	100 mA sourcing		0.15		V
THERMAL SHUTDOWN						
T_{TSD}	Thermal shutdown threshold	Temperature rising		175		°C
	Thermal shutdown hysteresis			15		°C

8.6 Typical Characteristics

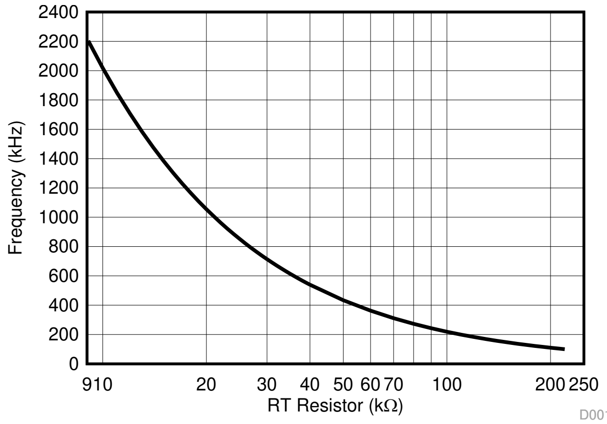


图 8-1. Frequency vs RT Resistance

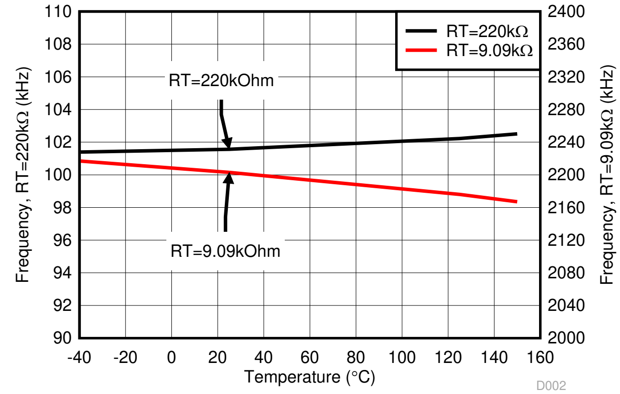


图 8-2. Frequency vs Temperature

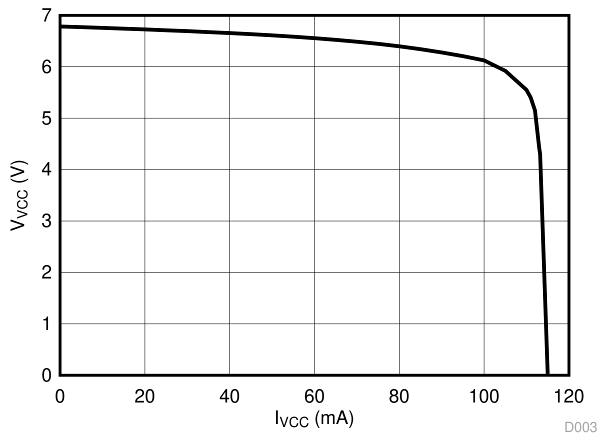


图 8-3. V_{VCC} vs I_{VCC}

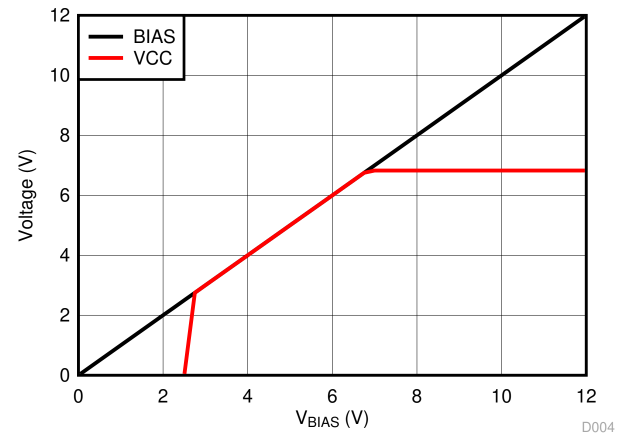


图 8-4. V_{VCC} vs V_{BIAS} (No Load)

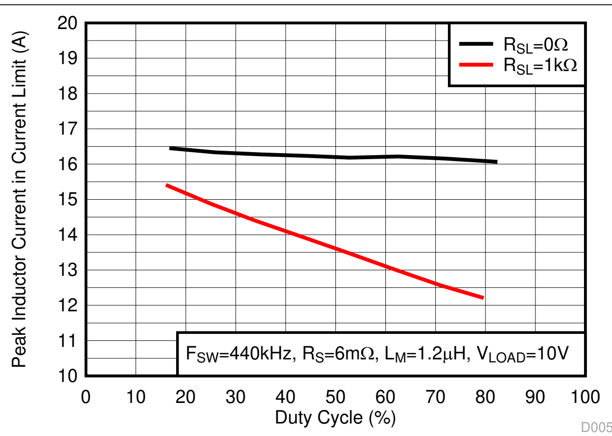


图 8-5. Peak Current Limit vs Duty Cycle

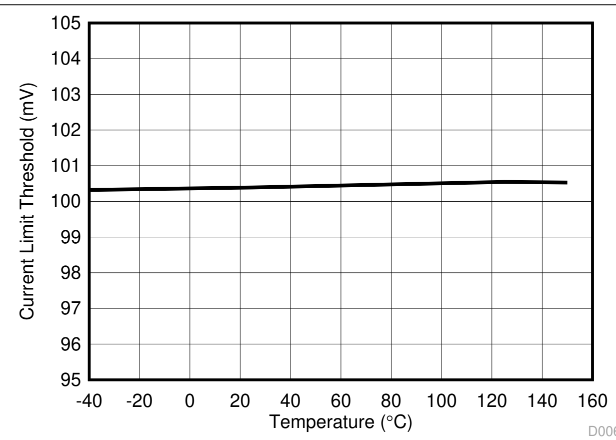


图 8-6. Current Limit Threshold vs Temperature

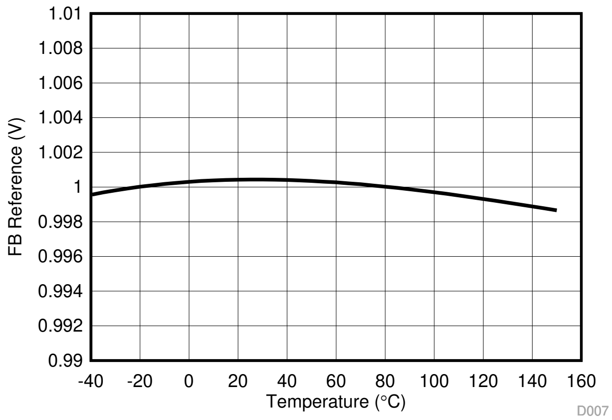


图 8-7. FB Reference vs Temperature

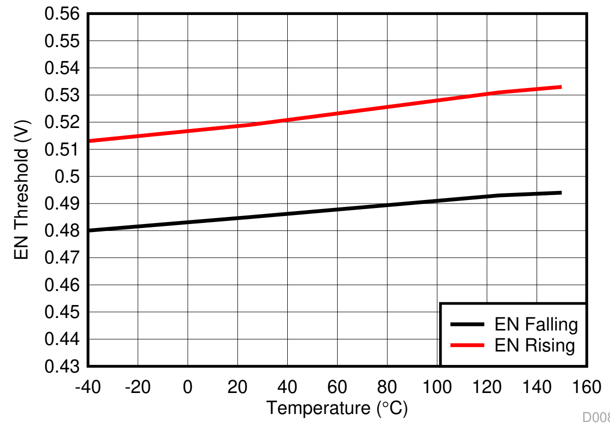


图 8-8. EN Threshold vs Temperature

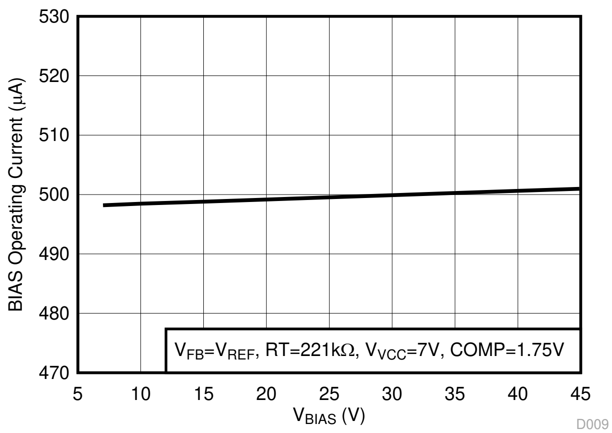


图 8-9. $I_{OPERATING(BIAS)}$including RT current vs V_{BIAS}

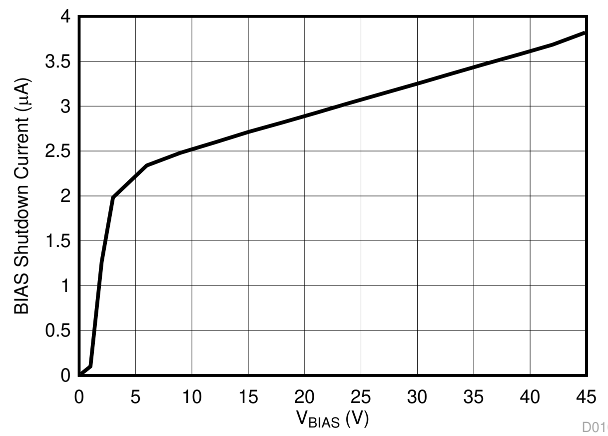


图 8-10. $I_{SHUTDOWN(BIAS)}$ vs V_{BIAS}

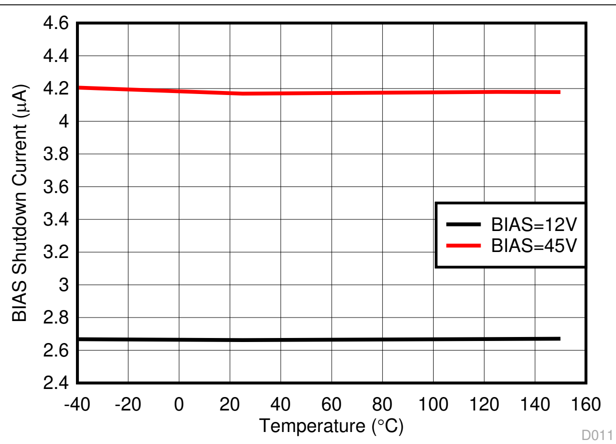


图 8-11. $I_{SHUTDOWN}$ vs Temperature

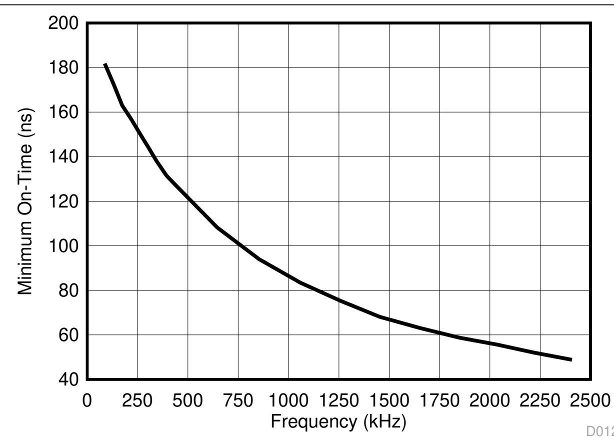


图 8-12. $t_{ON(MIN)}$ vs Frequency

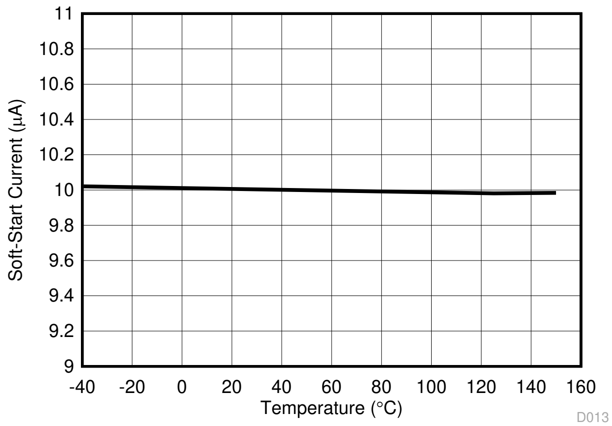


图 8-13. I_{SS} vs Temperature

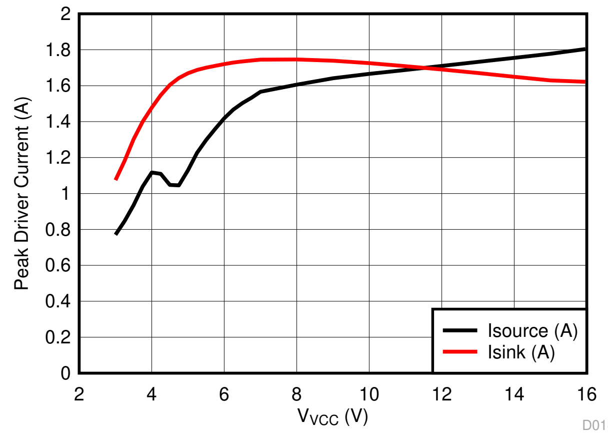


图 8-14. Peak Driver Current vs VCC

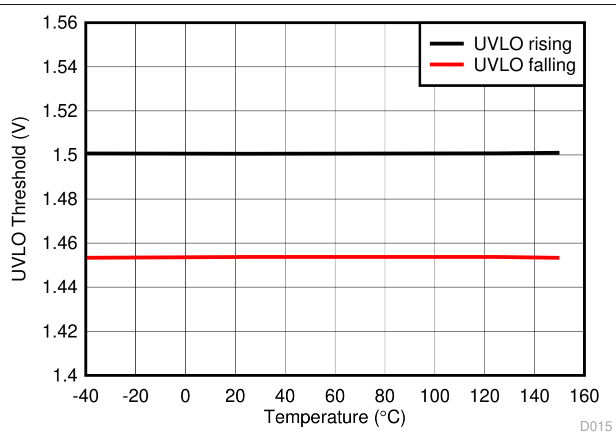


图 8-15. UVLO Threshold vs Temperature

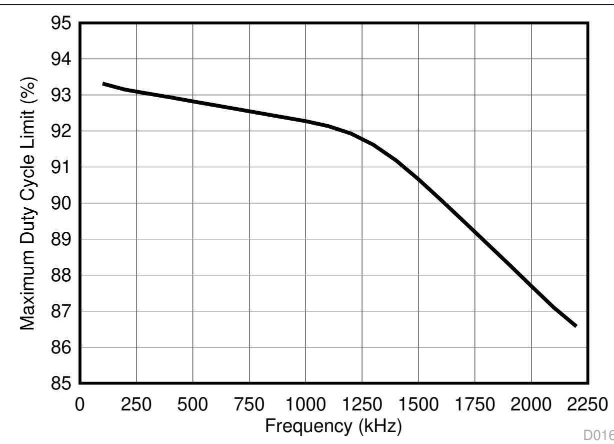


图 8-16. Maximum Duty Cycle vs Frequency

9 Detailed Description

9.1 Overview

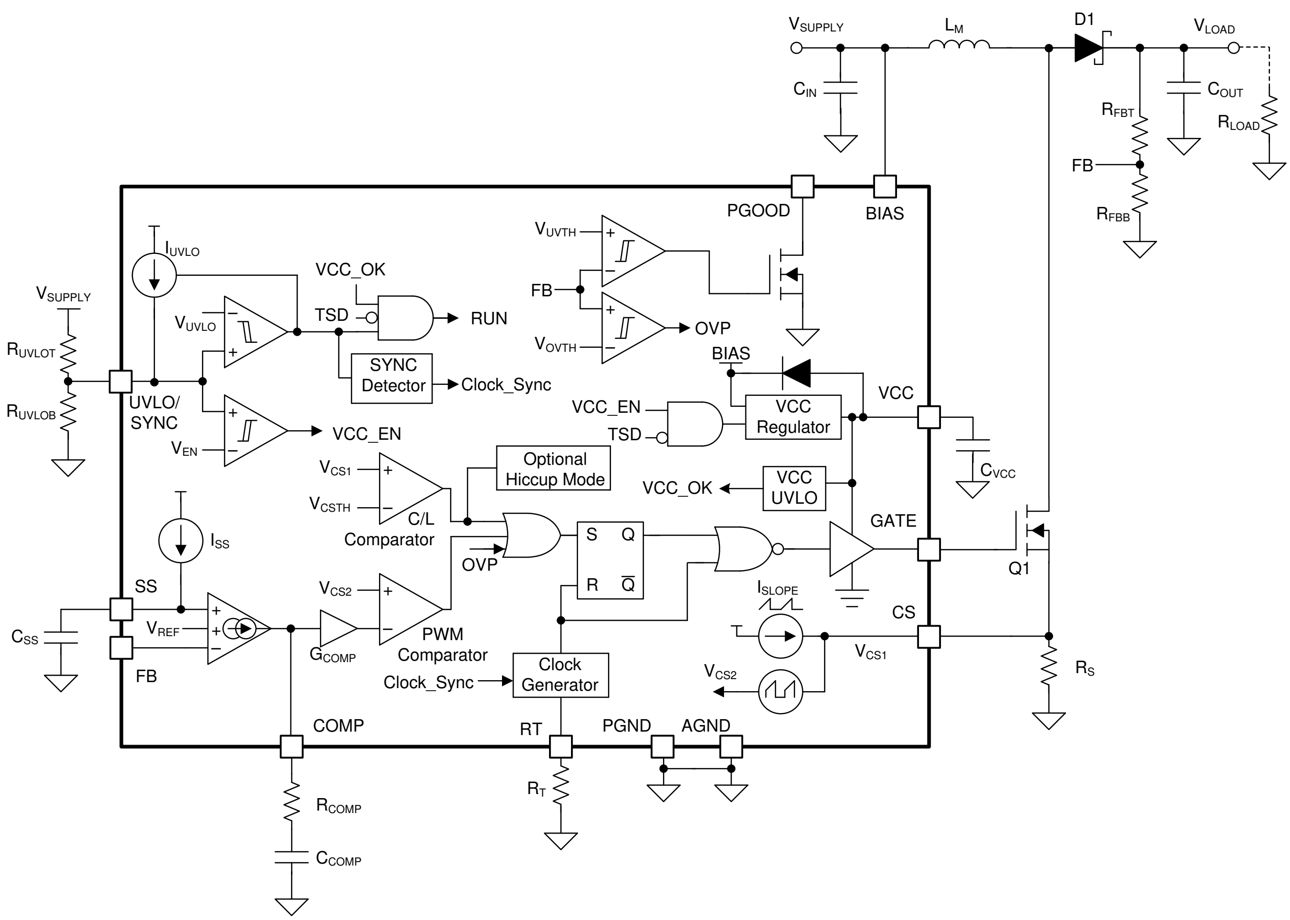
The LM5155x-Q1 device is a wide input range, non-synchronous boost controller that uses peak-current-mode control. The device can be used in boost, SEPIC, and flyback topologies.

The LM5155x-Q1 device can start up from a 1-cell battery with a minimum of 2.97 V if the BIAS pin is connected to the VCC pin. It can operate with the input supply voltage as low as 1.5 V if the BIAS pin is greater than 3.5 V. The internal VCC regulator also supports BIAS pin operation up to 45 V (50-V absolute maximum) for automotive load dump. The switching frequency is dynamically programmable with an external resistor from 100 kHz to 2.2 MHz. Switching at 2.2 MHz minimizes AM band interference and allows for a small solution size and fast transient response.

The device features a 1.5-A standard MOSFET driver and a low 100-mV current limit threshold. The device also supports the use of an external VCC supply to improve efficiency. Low operating current and pulse skipping operation improve efficiency at light loads.

The device has built-in protection features such as cycle-by-cycle current limit, overvoltage protection, line UVLO, and thermal shutdown. Hiccup mode overload protection is available in the LM51551-Q1 device option. Additional features include low shutdown I_Q, programmable soft start, programmable slope compensation, precision reference, power good indicator, and external clock synchronization.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Line Undervoltage Lockout (UVLO/SYNC Pin)

The device has a dual-level UVLO circuit. During power-on, if the BIAS pin voltage is greater than 2.7 V, the UVLO pin voltage is in between the enable threshold (V_{EN}), and the UVLO threshold (V_{UVLO}) for more than 1.5 µs (see 节 9.3.5 for more details), the device starts up and an internal configuration starts. The device typically requires a 65-µs internal start-up delay before entering standby mode. In standby mode, the VCC regulator and RT regulator are operational, SS pin is grounded, and there is no switching at the GATE output.

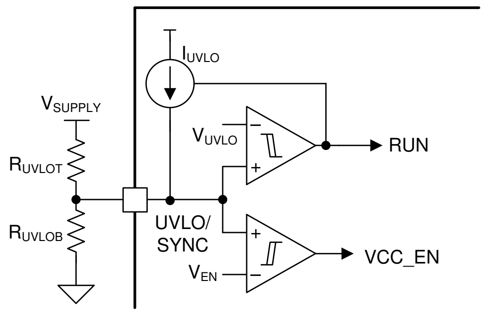


图 9-1. Line UVLO and Enable

When the UVLO pin voltage is above the UVLO threshold, the device enters run mode. In run mode, a soft-start sequence starts if the VCC voltage is greater than 4.5 V, or 50 µs after the VCC voltage exceeds the 2.85-V VCC UV threshold ($V_{VCC-UVLO}$), whichever comes first. UVLO hysteresis is accomplished with an internal 50-mV voltage hysteresis and an additional 5- µ A current source that is switched on or off. When the UVLO pin voltage exceeds the UVLO threshold, the current source is enabled to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the UVLO threshold, the current source is disabled, causing the voltage at the UVLO pin to fall quickly. When the UVLO pin voltage is less than the enable threshold (V_{EN}), the device enters shutdown mode after a 35-µs (typical) delay with all functions disabled.

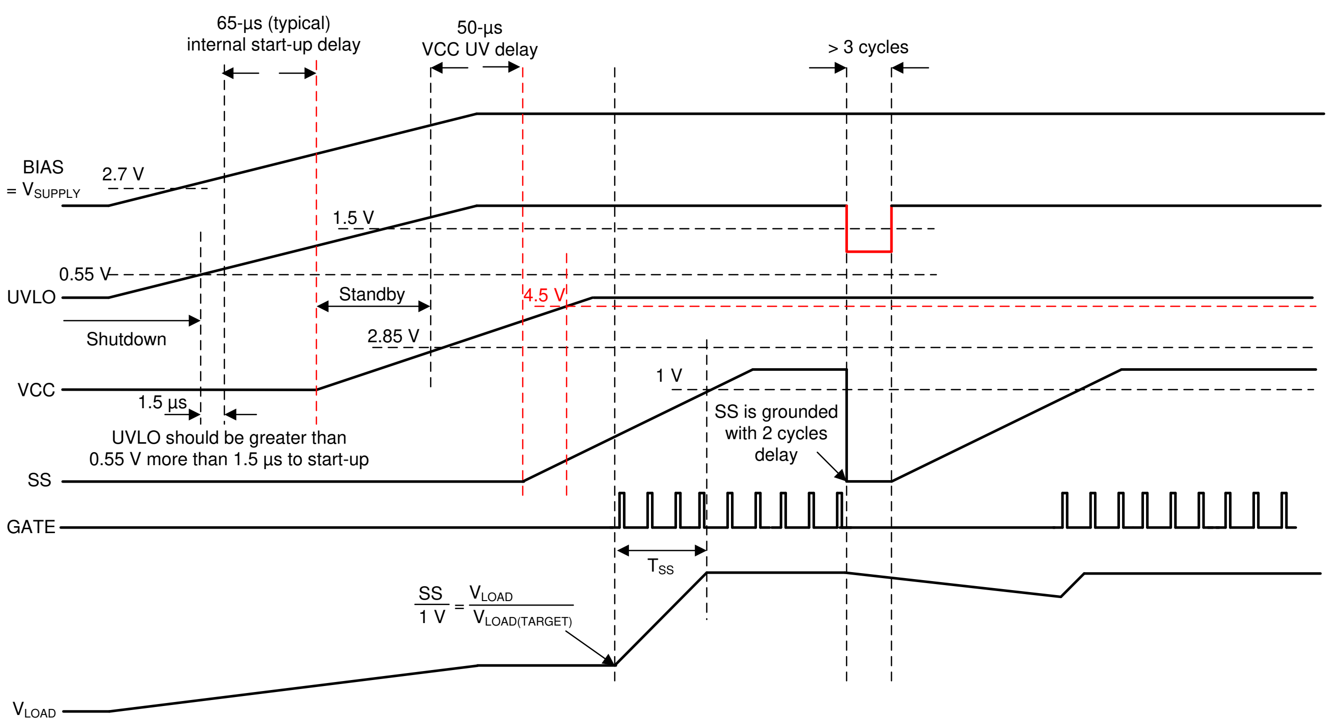


图 9-2. Boost Start-Up Waveforms Case 1: Start-Up by 2.85-V VCC UVLO, UVLO Toggle After Start-Up

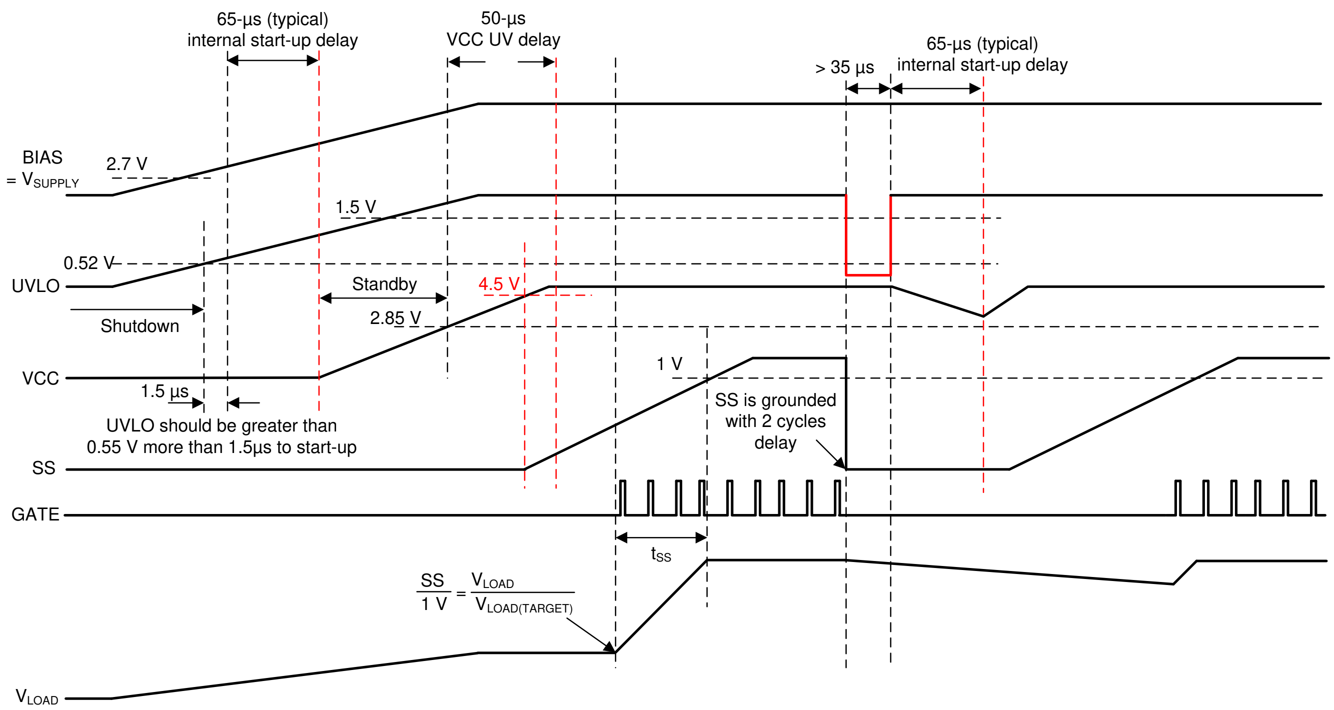


图 9-3. Boost Start-Up Waveforms Case 2: Start-Up When VCC > 4.5 V, EN Toggle After Start-Up

The external UVLO resistor divider must be designed so that the voltage at the UVLO pin is greater than 1.5 V (typical) when the input voltage is in the desired operating range. The values of R_{UVLOT} and R_{UVLOB} can be calculated as shown in 方程式 1 and 方程式 2.

$$R_{UVLOT} = \frac{V_{SUPPLY(ON)} \times \frac{V_{UVLO(FALLING)}}{V_{UVLO(RISING)}} - V_{SUPPLY(OFF)}}{I_{UVLO}} \tag{1}$$

where

- $V_{SUPPLY(ON)}$ is the desired start-up voltage of the converter.
- $V_{SUPPLY(OFF)}$ is the desired turnoff voltage of the converter.

$$R_{UVLOB} = \frac{V_{UVLO(RISING)} \times R_{UVLOT}}{V_{SUPPLY(ON)} - V_{UVLO(RISING)}} \tag{2}$$

A UVLO capacitor (C_{UVLO}) is required in case the input voltage drops below the $V_{SUPPLY(OFF)}$ momentarily during the start-up or during a severe load transient at the low input voltage. If the required UVLO capacitor is large, an additional series UVLO resistor (R_{UVLOS}) can be used to quickly raise the voltage at the UVLO pin when the 5-µA hysteresis current turns on.

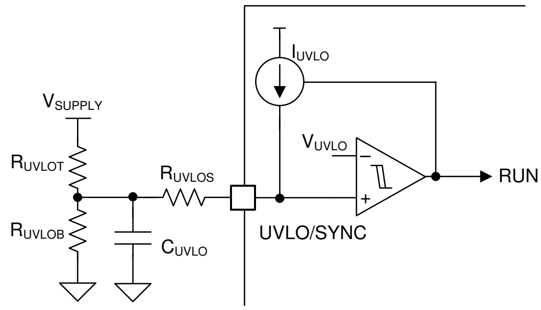


图 9-4. Line UVLO using Three UVLO Resistors

Do not leave the UVLO pin floating. Connect to the BIAS pin if not used.

9.3.2 High Voltage VCC Regulator (BIAS, VCC Pin)

The device has an internal wide input VCC regulator which is sourced from the BIAS pin. The wide input VCC regulator allows the BIAS pin to be connected directly to supply voltages from 3.5 V to 45 V.

The VCC regulator turns on when the device is in the standby or run mode. When the BIAS pin voltage is below the VCC regulation target, the VCC output tracks the BIAS with a small dropout voltage. When the BIAS pin voltage is greater than the VCC regulation target, the VCC regulator provides a 6.85-V supply for the N-channel MOSFET driver.

The VCC regulator sources current into the capacitor connected to the VCC pin with a minimum of 35-mA capability. The recommended VCC capacitor value is from 1 µF to 4.7 µF.

The device supports a wide input range from 3.5 V to 45 V in normal configuration. By connecting the BIAS pin directly to the VCC pin, the device supports inputs from 2.97 V to 16 V. This configuration is recommended when the device starts up from a 1-cell battery.

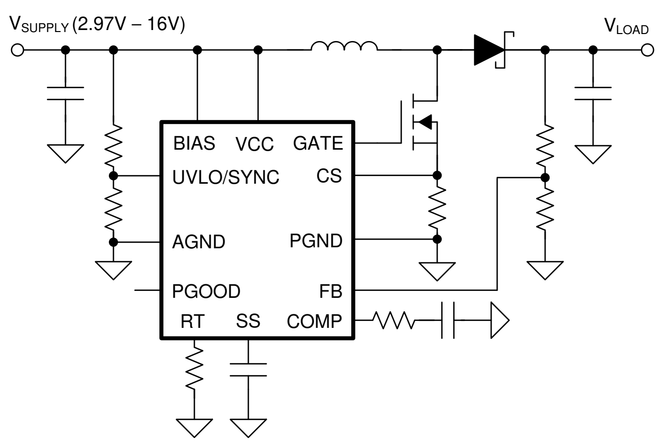


图 9-5. 2.97-V Start-Up (BIAS = VCC)

The minimum supply voltage after start-up can be further decreased by supplying the BIAS pin from the boost converter output or from an external power supply as shown in 图 9-6.

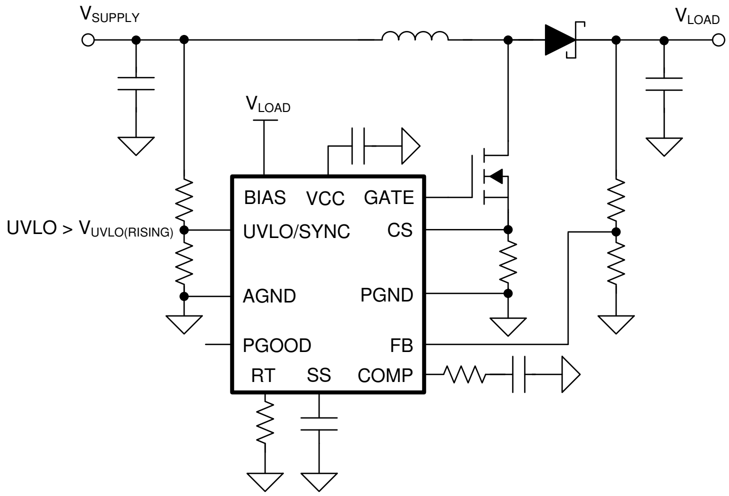


图 9-6. Decrease the Minimum Operating Voltage After Start-Up

In flyback topology, the internal power dissipation of the device can be decreased by supplying the VCC using an additional transformer winding. In this configuration, the external VCC supply voltage must be greater than the VCC regulation target ($V_{VCC\text{-}REG}$), and the BIAS pin voltage must be greater the VCC voltage because the VCC regulator includes a diode between VCC and BIAS.

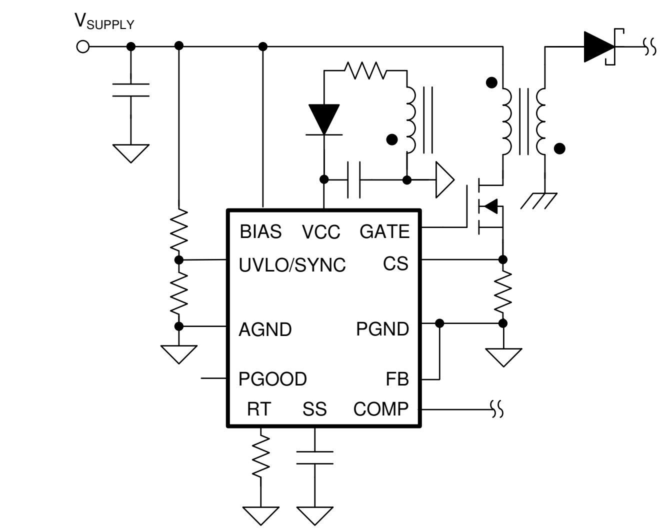


图 9-7. External VCC Supply (BIAS ≥ VCC)

If the voltage of the external VCC bias supply is greater than the BIAS pin voltage, use an external blocking diode from the input power supply to the BIAS pin to prevent the external bias supply from passing current to the boost input supply through VCC.

9.3.3 Soft Start (SS Pin)

The soft-start feature helps the converter gradually reach the steady state operating point, thus reducing start-up stresses and surges. The device regulates the FB pin to the SS pin voltage or the internal reference, whichever is lower.

At start-up, the internal 10-µA soft-start current source (I_{SS}) turns on 50 µs after the VCC voltage exceeds the 2.85-VCC UV threshold, or if the VCC voltage is greater than 4.5 V, whichever comes first. The soft-start current gradually increases the voltage on an external soft-start capacitor connected to the SS pin. This results in a gradual rise of the output voltage. The SS pin is pulled down to ground by an internal switch when the VCC is less than VCC UVLO threshold, the UVLO is less than the UVLO threshold, during hiccup mode off-time or thermal shutdown.

In boost topology, soft-start time (t_{SS}) varies with the input supply voltage. The soft-start time in boost topology is calculated as shown in 方程式 3.

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \times \left(1 - \frac{V_{SUPPLY}}{V_{LOAD}}\right) \tag{3}$$

In SEPIC topology, the soft-start time (t_{SS}) is calculated as follows.

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \tag{4}$$

TI recommends choosing a soft-start time long enough so that the converter can start up without going into an overcurrent state. See 节 *9.3.10* for more detailed information.

图 9-8 shows an implementation of primary side soft start in flyback topology.

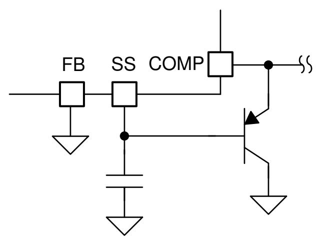


图 9-8. Primary-Side Soft-Start in Flyback

图 9-9 shows an implementation of secondary side soft start in flyback topology.

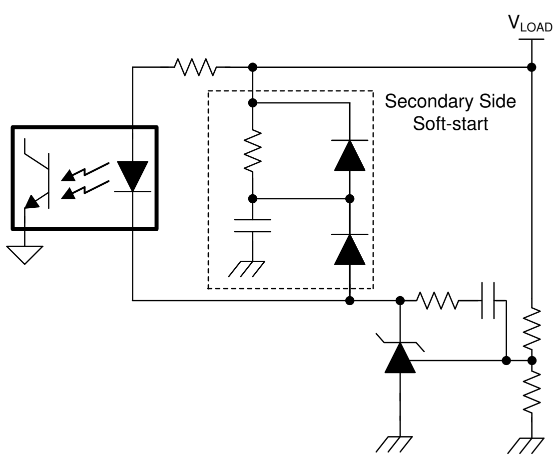


图 9-9. Secondary-Side Soft Start in Flyback

9.3.4 Switching Frequency (RT Pin)

The switching frequency of the device can be set by a single RT resistor connected between the RT and the AGND pins. The resistor value to set the RT switching frequency (f_{RT}) is calculated as shown in 方程式 5.

$$R_T = \frac{2.21 \times 10^{10}}{f_{RT(TYPICAL)}} - 955 \tag{5}$$

The RT pin is regulated to 0.5 V by the internal RT regulator when the device is enabled.

9.3.5 Clock Synchronization (UVLO/SYNC Pin)

The switching frequency of the device can be synchronized to an external clock by pulling down the UVLO/SYNC pin. The internal clock of the device is synchronized at the falling edge, but ignores the falling edge input during the forced off-time which is determined by the maximum duty cycle limit. The external synchronization clock must pull down the UVLO/SYNC pin voltage below 1.45 V (typical). The duty cycle of the pulldown pulse is not limited, but the minimum pulldown pulse width must be greater than 150 ns, and the minimum pullup pulse width must be greater than 250 ns. 图 9-10 shows an implementation of the remote shutdown function. The UVLO pin can be pulled down by a discrete MOSFET or an open-drain output of an MCU. In this configuration, the device stops switching immediately after the UVLO pin is grounded, and the device shuts down 35 µs (typical) after the UVLO pin is grounded.

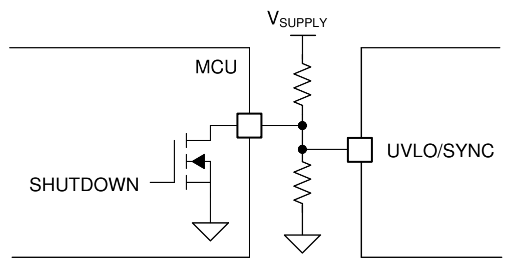


图 9-10. UVLO and Shutdown

图 9-11 shows an implementation of shutdown and clock synchronization functions together. In this configuration, the device stops switching immediately when the UVLO pin is grounded, and the device shuts down if the f_{SYNC} stays in high logic state for longer than 35 µs (typical) (UVLO is in low logic state for more than 35 µs (typical)). The device runs at f_{SYNC} if clock pulses are provided after the device is enabled.

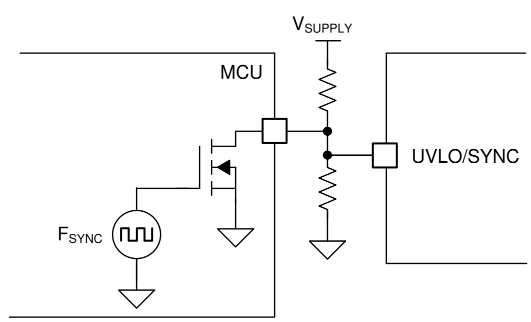


图 9-11. UVLO, Shutdown, and Clock Synchronization

图 9-13 and 图 9-14 show implementations of standby and clock synchronization functions together. In this configuration, the device stops switching immediately if f_{SYNC} stays in high logic state and enters standby mode if f_{SYNC} stays in high logic state for longer than two switching cycles. The device runs at the f_{SYNC} if clock pulses are provided. Because the device can be enabled when the UVLO pin voltage is greater than the enable threshold for more than 1.5 µs, the configurations in 图 9-13 and 图 9-14 are recommended if the external clock synchronization pulses are provided from the start before the device is enabled. This 1.5-µs requirement can be relaxed when the duty cycle of the synchronization pulse is greater than 50%. 图 9-12 shows the required minimum duty cycle to start up by synchronization pulses. When the switching frequency is greater than 1.1 MHz, the UVLO pin voltage should be greater than the enable threshold for more than 1.5 µs before applying the external synchronization pulse.

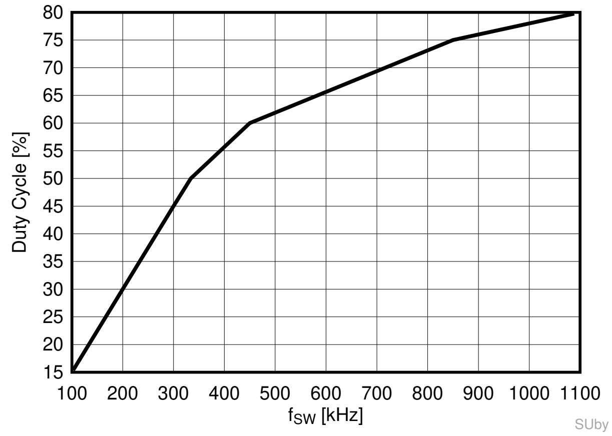


图 9-12. Required Duty Cycle to Start up by SYNC

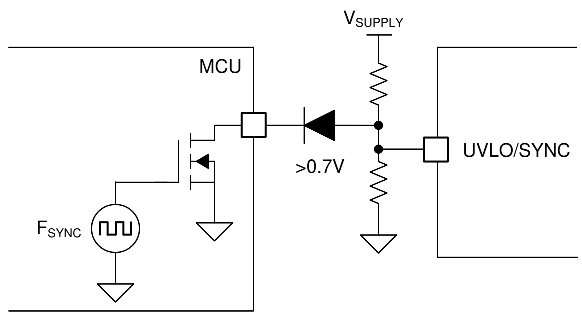


图 9-13. UVLO, Standby, and Clock Synchronization (a)

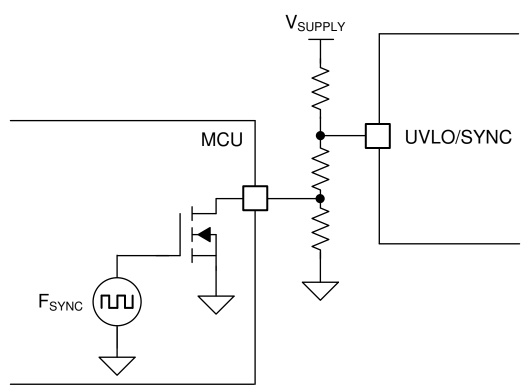


图 9-14. UVLO, Standby, and Clock Synchronization (b)

If the UVLO function is not required, the shutdown and clock synchronization functions can be implemented together by using one push-pull output of the MCU. In this configuration, the device shuts down if f_{SYNC} stays in low logic state for longer than 35 µs (typical). The device is enabled if f_{SYNC} stays in high logic state for longer than 1.5 µs. The device runs at the f_{SYNC} if clock pulses are provided after the device is enabled. Also, in this configuration, it is recommended to apply the external clock pulses after the BIAS is supplied. By limiting the current flowing into the UVLO pin below 1 mA using a current limiting resistor, the external clock pulses can be supplied before the BIAS is supplied (see 图 9-15).

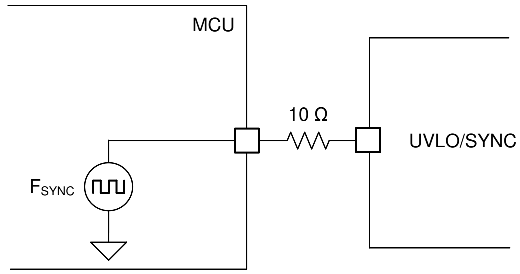


图 9-15. Shutdown and Clock Synchronization

图 9-16 shows an implementation of inverted enable using external circuit.

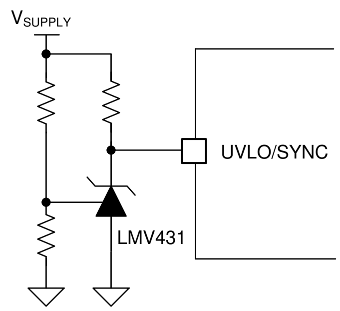


图 9-16. Inverted UVLO

The external clock frequency (f_{SYNC}) must be within +25% and –30% of $f_{RT(TYPICAL)}$. Because the maximum duty cycle limit and the peak current limit with slope resistor (R_{SL}) are affected by the clock synchronization, take extra care when using the clock synchronization function. See *节 9.3.6*, *节 9.3.7*, and *节 9.3.11* for more information.

9.3.6 Current Sense and Slope Compensation (CS Pin)

The device has a low-side current sense and provides both fixed and optional programmable slope compensation ramps, which help to prevent subharmonic oscillation at high duty cycle. Both fixed and programmable slope compensation ramps are added to the sensed inductor current input for the PWM operation, but only the programmable slope compensation ramp is added to the sensed inductor current input (see 图 9-17). For an accurate peak current limit operation over the input supply voltage, TI recommends using only the fixed slope compensation (see 图 8-5).

The device can generate the programmable slope compensation ramp using an external slope resistor (R_{SL}) and a sawtooth current source with a slope of 30 µA × f_{RT}. This current flows out of the CS pin.

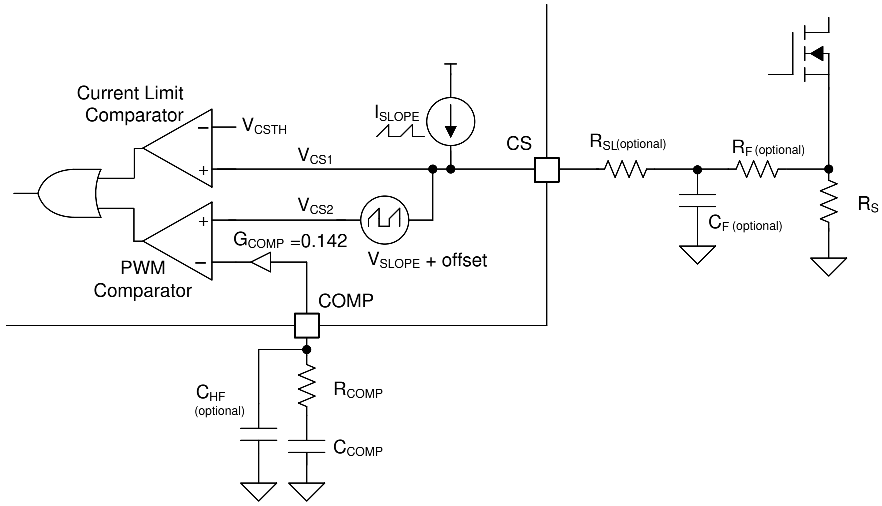


图 9-17. Current Sensing and Slope Compensation

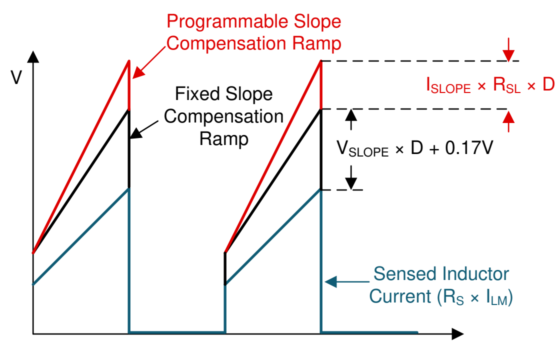


图 9-18. Slope Compensation Ramp (a) at PWM Comparator Input

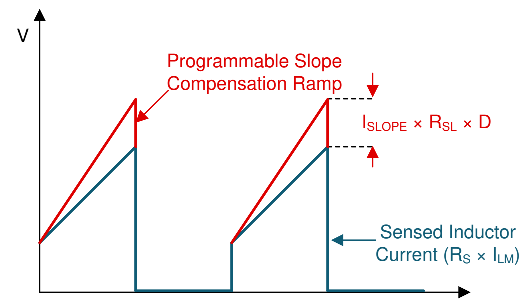


图 9-19. Slope Compensation Ramp (b) at Current Limit Comparator Input

Use 方程式 6 to calculate the value of the peak slope current (I_{SLOPE}) and use 方程式 7 to calculate the value of the peak slope voltage (V_{SLOPE}).

$$I_{SLOPE} = 30\mu A \times \frac{f_{RT}}{f_{SYNC}} \tag{6}$$

$$V_{SLOPE} = 40mV \times \frac{f_{RT}}{f_{SYNC}} \tag{7}$$

where

- $f_{SYNC} = f_{RT}$ if clock synchronization is not used.

According to peak current mode control theory, the slope of the compensation ramp must be greater than half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle. Therefore, the minimum amount of slope compensation in boost topology should satisfy the following inequality:

$$0.5 \times \frac{(V_{LOAD} + V_F) - V_{SUPPLY}}{L_M} \times R_S \times Margin < 40mV \times f_{SW} \tag{8}$$

where

- V_F is a forward voltage drop of D1, the external diode.

The recommended value for margin to cover non-ideal factors is 1.2. If required, R_{SL} can be added to further increase the slope of the compensation ramp. Typically 82% of the sensed inductor current falling slope is known as an optimal amount of the slope compensation. The R_{SL} value to achieve 82% of the sensed inductor current falling slope is calculated as shown in 方程式 9.

$$0.82 \times \frac{(V_{LOAD} + V_F) - V_{SUPPLY}}{L_M} \times R_S = (30uA \times R_{SL} + 40mV) \times f_{SW} \tag{9}$$

If clock synchronization is not used, the f_{SW} frequency equals the f_{RT} frequency. If clock synchronization is used, the f_{SW} frequency equals the f_{SYNC} frequency. The maximum value for the R_{SL} resistance is 2 kΩ.

9.3.7 Current Limit and Minimum On-time (CS Pin)

The device provides cycle-by-cycle peak current limit protection that turns off the MOSFET when the sum of the inductor current and the programmable slope compensation ramp reaches the current limit threshold (V_{CLTH}). Peak inductor current limit ($I_{PEAK-CL}$) in steady state is calculated as shown in 方程式 10.

$$I_{PEAK-CL} = \frac{V_{CLTH} - 30\mu A \times R_{SL} \times \frac{f_{RT}}{f_{SYNC}} \times D}{R_S} \tag{10}$$

The practical duty cycle is greater than the estimated due to voltage drops across the MOSFET and sense resistor. The estimated duty cycle is calculated as shown in 方程式 11.

$$D = 1 - \frac{V_{SUPPLY}}{V_{LOAD} + V_F} \tag{11}$$

Boost converters have a natural pass-through path from the supply to the load through the high-side power diode (D1). Because of this path and the minimum on-time limitation of the device, boost converters cannot provide current limit protection when the output voltage is close to or less than the input supply voltage. The minimum on-time is shown in 图 8-12 and is calculated as 方程式 12.

$$t_{ON(MIN)} \approx \frac{800 \times 10^{-15}}{\frac{1}{8 \times R_T} + 4 \times 10^{-6}} \tag{12}$$

If required, a small external RC filter (R_F, C_F) at the CS pin can be added to overcome the large leading edge spike of the current sense signal. Select an R_F value in the range of 10 Ω to 200 Ω and a C_F value in the range of 100 pF to 2 nF. Because of the effect of this RC filter, the peak current limit is not valid when the on-time is less than 2 × R_F × C_F. To fully discharge the C_F during the off-time, the RC time constant should satisfy the following inequality.

$$3 \times R_F \times C_F < \frac{1 - D}{f_{SW}} \tag{13}$$

9.3.8 Feedback and Error Amplifier (FB, COMP Pin)

The feedback resistor divider is connected to an internal transconductance error amplifier which features high output resistance (R_O = 10 MΩ) and wide bandwidth (BW = 7 MHz). The internal transconductance error amplifier sources current which is proportional to the difference between the FB pin and the SS pin voltage or the internal reference, whichever is lower. The internal transconductance error amplifier provides symmetrical sourcing and sinking capability during normal operation and reduces its sinking capability when the FB is greater than OVP threshold.

To set the output regulation target, select the feedback resistor values as shown in 方程式 14.

$$V_{LOAD} = V_{REF} \times \left(\frac{R_{FBT}}{R_{FBB}} + 1 \right) \tag{14}$$

The output of the error amplifier is connected to the COMP pin, allowing the use of a Type 2 loop compensation network. R_{COMP}, C_{COMP}, and optional C_{HF} loop compensation components configure the error amplifier gain and phase characteristics to achieve a stable loop response. The absolute maximum voltage rating of the FB pin is 3.8 V. If necessary, especially during automotive load dump transient, the feedback resistor divider input can be clamped with an external zener diode.

The COMP pin features internal clamps. The maximum COMP clamp limits the maximum COMP pin voltage below its absolute maximum rating even in shutdown. The minimum COMP clamp limits the minimum COMP pin voltage in order to start switching as soon as possible during no load to heavy load transition. The minimum COMP clamp is disabled when FB is connected to ground in flyback topology.

9.3.9 Power-Good Indicator (PGOOD Pin)

The device has a power-good indicator (PGOOD) to simplify sequencing and supervision. The PGOOD switches to a high impedance open-drain state when the FB pin voltage is greater than the feedback undervoltage threshold (V_{UVTH}), the VCC is greater than the VCC UVLO threshold and the UVLO/EN is greater than the EN threshold. A 25-μs deglitch filter prevents any false pulldown of the PGOOD due to transients. The recommended minimum pullup resistor value is 10 kΩ.

Due to the internal diode path from the PGOOD pin to the BIAS pin, the PGOOD pin voltage cannot be greater than V_{BIAS} + 0.3 V.

9.3.10 Hiccup Mode Overload Protection (LM51551 Only)

To further protect the converter during prolonged current limit conditions, the LM51551 device option provides a hiccup mode overload protection. The internal hiccup mode fault timer of the LM51551 counts the PWM clock cycles when the cycle-by-cycle current limiting occurs. When the hiccup mode fault timer detects 64 cycles of current limiting, an internal hiccup mode off timer forces the device to stop switching and pulls down SS. Then, the device will restart after 32 768 cycles of hiccup mode off-time. The 64 cycle hiccup mode fault timer is reset if eight consecutive switching cycles occur without exceeding the current limit threshold. The soft-start time must be long enough not to trigger the hiccup mode protection during soft-start time because the hiccup mode fault timer is enabled during the soft start.

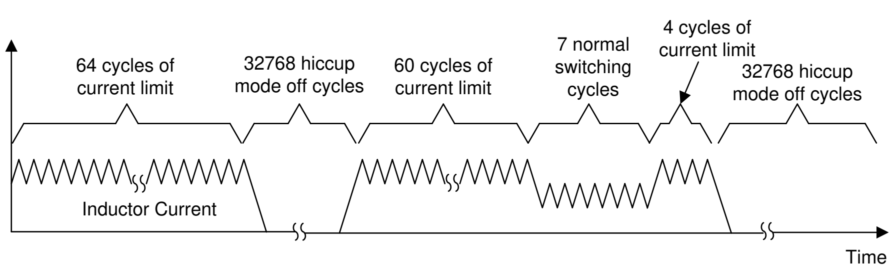


图 9-20. Hiccup Mode Overload Protection

To avoid an unexpected hiccup mode operation during a harsh load transient condition, it is recommended to have more margin when programming the peak-current limit.

9.3.11 Maximum Duty Cycle Limit and Minimum Input Supply Voltage

When designing boost converters, the maximum duty cycle should be reviewed at the minimum supply voltage. The minimum input supply voltage that can achieve the target output voltage is limited by the maximum duty cycle limit, and it can be estimated as follows.

$$V_{SUPPLY(MIN)} \approx (V_{LOAD} + V_F) \times (1 - D_{MAX}) + I_{SUPPLY(MAX)} \times R_{DCR} + I_{SUPPLY(MAX)} \times (R_{DS(ON)} + R_S) \times D_{MAX} \quad (15)$$

where

- $I_{SUPPLY(MAX)}$ = the maximum input current.
- R_{DCR} = the DC resistance of the inductor.
- $R_{DS(ON)}$ = the on-resistance of the MOSFET.

$$D_{MAX1} = 1 - 0.1 \times \frac{f_{SYNC}}{f_{RT}} \quad (16)$$

$$D_{MAX2} = 1 - 100ns \times f_{SW} \quad (17)$$

The minimum input supply voltage can be further decreased by supplying f_{SYNC} which is less than f_{RT}. D_{MAX} is D_{MAX1} or D_{MAX2}, whichever is lower.

9.3.12 MOSFET Driver (GATE Pin)

The device provides an N-channel MOSFET driver that can source or sink a peak current of 1.5 A. The peak sourcing current is larger when supplying an external VCC that is higher than the 6.75-V VCC regulation target. During start-up, especially when the input voltage range is below the VCC regulation target, the VCC voltage must be sufficient to completely enhance the MOSFET. If the MOSFET drive voltage is lower than the MOSFET gate plateau voltage during start-up, the boost converter may not start up properly and it can stick at the maximum duty cycle in a high power dissipation state. This condition can be avoided by selecting a lower threshold N-channel MOSFET switch and setting the $V_{SUPPLY(ON)}$ greater than 6 to 7 V. Since the internal VCC regulator has a limited sourcing capability, the MOSFET gate charge should satisfy the following inequality.

$$Q_{G@VCC} \times f_{SW} < 35mA \quad (18)$$

An internal 1-MΩ resistor is connected between GATE and PGND to prevent a false turnon during shutdown. In boost topology, a switch node dV/dT must be limited during the 65-µs internal start-up delay to avoid a false turnon, which is caused by the coupling through C_{DG} parasitic capacitance of the MOSFET.

9.3.13 Overvoltage Protection (OVP)

The device has OVP for the output voltage. OVP is sensed at the FB pin. If the voltage at the FB pin rises above the overvoltage threshold (V_{OVTH}), OVP is triggered and switching stops. During OVP, the internal error amplifier is operational, but the maximum source and sink capability is decreased to 40 µA.

9.3.14 Thermal Shutdown (TSD)

An internal thermal shutdown turns off the VCC regulator, disables switching, and pulls down the SS when the junction temperature exceeds the thermal shutdown threshold (T_{TSD}). After the temperature is decreased by 15°C, the VCC regulator is enabled again and the device performs a soft start.

9.4 Device Functional Modes

9.4.1 Shutdown Mode

If the UVLO pin voltage is below the enable threshold for longer than 35 µs (typical), the device goes to the shutdown mode with all functions disabled. In shutdown mode, the device decreases the BIAS pin current consumption to below 2.6 µA (typical).

9.4.2 Standby Mode

If the UVLO pin voltage is greater than the enable threshold and below the UVLO threshold for longer than 1.5 µs, the device is in standby mode with the VCC regulator operational, RT regulator operational, SS pin grounded, and no switching at the GATE output. The PGOOD is activated when the VCC voltage is greater than the VCC UV threshold.

9.4.3 Run Mode

If the UVLO pin voltage is above the UVLO threshold and the VCC voltage is sufficient, the device enters RUN mode. In this mode, soft start starts 50 µs after the VCC voltage exceeds the 2.85 VCC UV threshold, or if the VCC voltage is greater than 4.5 V, whichever comes first.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

See the *How to Design a Boost Converter Using LM5155-Q1* application note for information on loop response and component selections for the boost converter.

10.2 Typical Application

图 10-1 shows all optional components to design a boost converter.

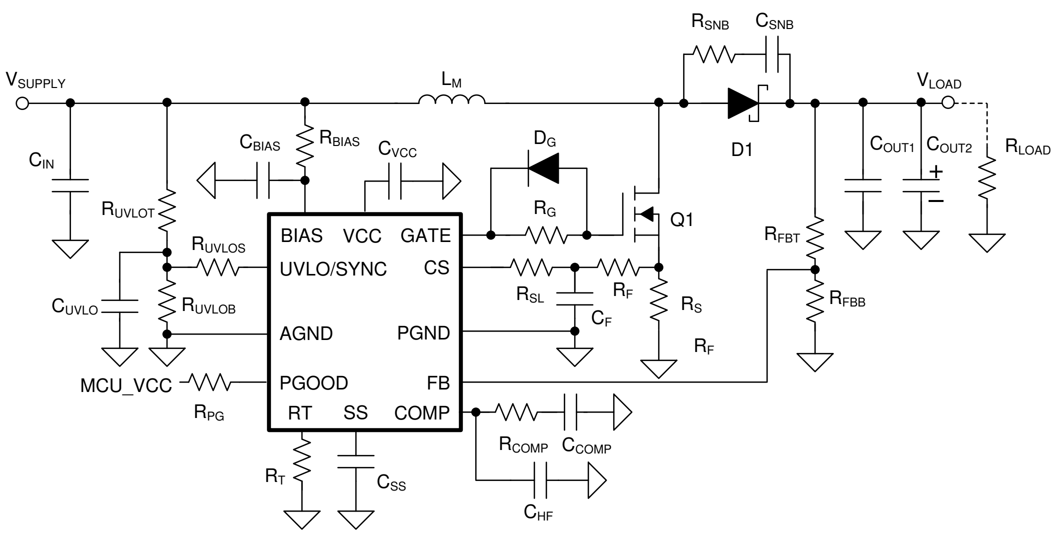


图 10-1. Typical Boost Converter Circuit With Optional Components

10.2.1 Design Requirements

表 10-1 shows the intended input, output, and performance parameters for this application example.

表 10-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Minimum input supply voltage ($V_{SUPPLY(MIN)}$)	6 V
Target output voltage (V_{LOAD})	24 V
Maximum load current (I_{LOAD})	2 A (≈ 48 Watt)
Typical switching frequency (f_{SW})	440 kHz

10.2.2 Detailed Design Procedure

Use the Quick Start Calculator to expedite the process of designing of a regulator for a given application based on the LM5155-Q1 device. Download the *LM5155 Boost Controller Quick Start Calculator*.

10.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5155x-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.

3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2.2.2 Recommended Components

表 10-2 shows a recommended list of materials for this typical application.

表 10-2. List of Materials

REFERENCE DESIGNATOR	QTY.	SPECIFICATION	MANUFACTURER	PART NUMBER[(1)]
R_T	1	RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060349K9FKEA
R_{FBT}	1	RES, 47.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060347K0FKEA
R_{FBB}	1	RES, 2.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06032K00JNEA
L_M	1	Inductor, Shielded, Composite, 6.8 µH, 18.5 A, 0.01 Ω, SMD	Coilcraft	XAL1010-682MEB
R_S	1	RES, 0.008, 1%, 3 W, AEC-Q200 Grade 0, 2512 WIDE	Susumu	KRL6432E-M-R008-F-T1
R_{SL}	1	RES, 0, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL
C_{OUT1}	3	CAP, CERM, 4.7 µF, 50 V, ±10%, X7R, 1210	TDK	C3225X7R1H475K250AB
C_{OUT2} (Bulk)	2	CAP, Aluminum Polymer, 100 µF, 50 V, ±20%, 0.025 Ω, AEC-Q200 Grade 2, D10xL10mm SMD	Chemi-Con	HHXB500ARA101MJA0G
C_{IN1}	6	CAP, CERM, 10 µF, 50 V, ±10%, X7R, 1210	MuRata	GRM32ER71H106KA12L
C_{IN2} (Bulk)	1	CAP, Polymer Hybrid, 100 µF, 50 V, ±20%, 28 Ω, 10x10 SMD	Panasonic	EEHZC1H101P
Q1	1	MOSFET, N-CH, 40 V, 50 A, AEC-Q101, SON-8	Infineon	IPC50N04S5L5R5ATMA1
D1	1	Schottky, 60 V, 10 A, AEC-Q101, CFP15	Nexperia	PMEG060V100EPDZ
R_{COMP}	1	RES, 11.3 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060311K3FKEA
C_{COMP}	1	CAP, CERM, 0.022 µF, 100 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E2X7R2A223K080AA
C_{HF}	1	CAP, CERM, 220 pF, 20 V, ±5%, C0G/NP0, AEC-Q200 Grade 1, 0603	TDK	CGA3E2C0G1H221J080AA
R_{UVLOT}	1	RES, 21.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060321K0FKEA
R_{UVLOB}	1	RES, 7.32 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06037K32FKEA
R_{UVLOS}	0	N/A	N/A	N/A
C_{SS}	1	CAP, CERM, 0.22 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E3X7R1H224K080AB
D_G	0	N/A	N/A	N/A
R_G	1	RES, 0, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL
C_F	1	CAP, CERM, 100 pF, 50 V, ±1%, C0G/NP0, 0603	Kemet	C0603C101F5GACTU
R_F	1	RES, 100, 1%, 0.1 W, 0603	Yageo America	RC0603FR-07100RL
R_{SNB}	0	N/A	N/A	N/A
C_{SNB}	0	N/A	N/A	N/A
R_{BIAS}	1	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Panasonic	ERJ-3GEY0R00V
C_{BIAS}	1	CAP, CERM, 0.01 µF, 50 V, ±10%, X7R, 0603	Samsung Electro-Mechanics	CL10B103KB8NCNC

表 10-2. List of Materials (continued)

REFERENCE DESIGNATOR	QTY.	SPECIFICATION	MANUFACTURER	PART NUMBER[1]
C_{VCC}	1	CAP, CERM, 1 µF, 16 V, ±20%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCM188R71C105MA64D
R_{PG}	1	RES, 24.9 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0724K9L

(1) See the *Third-party Products Disclaimer*.

10.2.2.3 Inductor Selection (L_M)

When selecting the inductor, consider three key parameters: inductor current ripple ratio (RR), falling slope of the inductor current, and RHP zero frequency (f_{RHP}).

Inductor current ripple ratio is selected to have a balance between core loss and copper loss. The falling slope of the inductor current must be low enough to prevent subharmonic oscillation at high duty cycle (additional R_{SL} resistor is required if not). Higher f_{RHP} (= lower inductance) allows a higher crossover frequency and is always preferred when using a small value output capacitor.

The inductance value can be selected to set the inductor current ripple between 30% and 70% of the average inductor current as a good compromise between RR, F_{RHP}, and inductor falling slope.

10.2.2.4 Output Capacitor (C_{OUT})

There are a few ways to select the proper value of output capacitor (C_{OUT}). The output capacitor value can be selected based on output voltage ripple, output overshoot, or undershoot due to load transient.

The ripple current rating of the output capacitors must be enough to handle the output ripple current. By using multiple output capacitors, the ripple current can be split. In practice, ceramic capacitors are placed closer to the diode and the MOSFET than the bulk aluminum capacitors in order to absorb the majority of the ripple current.

10.2.2.5 Input Capacitor

The input capacitors decrease the input voltage ripple. The required input capacitor value is a function of the impedance of the source power supply. More input capacitors are required if the impedance of the source power supply is not low enough.

10.2.2.6 MOSFET Selection

The MOSFET gate driver of the device is sourced from the VCC. The maximum gate charge is limited by the 35-mA VCC sourcing current limit.

A leadless package is preferred for high switching-frequency designs. The MOSFET gate capacitance should be small enough so that the gate voltage is fully discharged during the off-time.

10.2.2.7 Diode Selection

A Schottky is the preferred type for D1 diode due to its low forward voltage drop and small reverse recovery charge. Low reverse leakage current is important parameter when selecting the Schottky diode. The diode must be rated to handle the maximum output voltage plus any switching node ringing. Also, it must be able to handle the average output current.

10.2.2.8 Efficiency Estimation

The total loss of the boost converter (P_{TOTAL}) can be expressed as the sum of the losses in the device (P_{IC}), MOSFET power losses (P_Q), diode power losses (P_D), inductor power losses (P_L), and the loss in the sense resistor (P_{RS}).

$$P_{TOTAL} = P_{IC} + P_Q + P_D + P_L + P_{RS} \tag{19}$$

P_{IC} can be separated into gate driving loss (P_G) and the losses caused by quiescent current (P_{IQ}).

$$P_{IC} = P_G + P_{IQ} \tag{20}$$

Each power loss is approximately calculated as follows:

$$P_G = Q_{G(@\,VCC)} \times V_{BIAS} \times f_{SW} \tag{21}$$

$$P_{IQ} = V_{BIAS} \times I_{BIAS} \tag{22}$$

I_{VIN} and I_{VOUT} values in each mode can be found in the supply current section of *节 8.5*.

P_Q can be separated into switching loss ($P_{Q(SW)}$) and conduction loss ($P_{Q(COND)}$).

$$P_Q = P_{Q(SW)} + P_{Q(COND)} \tag{23}$$

Each power loss is approximately calculated as follows:

$$P_{Q(SW)} = 0.5 \times (V_{LOAD} + V_F) \times I_{SUPPLY} \times (t_R + t_F) \times f_{SW} \tag{24}$$

t_R and t_F are the rise and fall times of the low-side N-channel MOSFET device. I_{SUPPLY} is the input supply current of the boost converter.

$$P_{Q(COND)} = D \times I_{SUPPLY}^2 \times R_{DS(ON)} \tag{25}$$

$R_{DS(ON)}$ is the on-resistance of the MOSFET and is specified in the MOSFET data sheet. Consider the $R_{DS(ON)}$ increase due to self-heating.

P_D can be separated into diode conduction loss (P_{VF}) and reverse recovery loss (P_{RR}).

$$P_D = P_{VF} + P_{RR} \tag{26}$$

Each power loss is approximately calculated as follows:

$$P_{VF} = (1 - D) \times V_F \times I_{SUPPLY} \tag{27}$$

$$P_{RR} = V_{LOAD} \times Q_{RR} \times f_{SW} \tag{28}$$

Q_{RR} is the reverse recovery charge of the diode and is specified in the diode data sheet. Reverse recovery characteristics of the diode strongly affect efficiency, especially when the output voltage is high.

P_L is the sum of DCR loss (P_{DCR}) and AC core loss (P_{AC}). DCR is the DC resistance of inductor which is mentioned in the inductor data sheet.

$$P_L = P_{DCR} + P_{AC} \tag{29}$$

Each power loss is approximately calculated as follows:

$$P_{DCR} = I_{SUPPLY}^2 \times R_{DCR} \tag{30}$$

$$P_{AC} = K \times \Delta I^{\beta} \times f_{SW}^{\alpha} \tag{31}$$

$$\Delta I = \frac{V_{SUPPLY} \times D \times \frac{1}{f_{SW}}}{L_M} \tag{32}$$

ΔI is the peak-to-peak inductor current ripple. K, α , and β are core dependent factors which can be provided by the inductor manufacturer.

P_{RS} is calculated as follows:

$$P_{RS} = D \times I_{SUPPLY}^2 \times R_S \tag{33}$$

Efficiency of the power converter can be estimated as follows:

$$\text{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{P_{TOTAL} + V_{LOAD} \times I_{LOAD}} \tag{34}$$

10.2.3 Application Curve

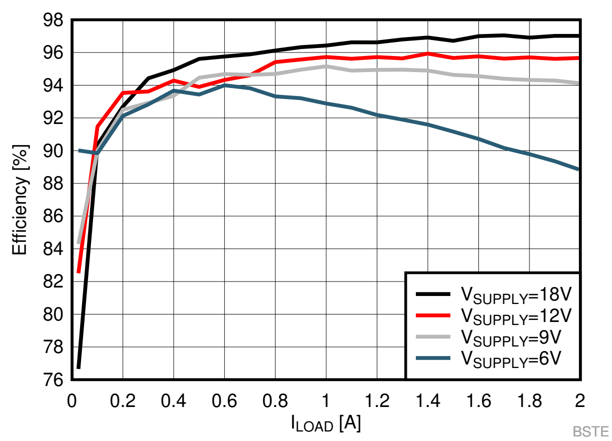


图 10-2. Efficiency

10.3 System Examples

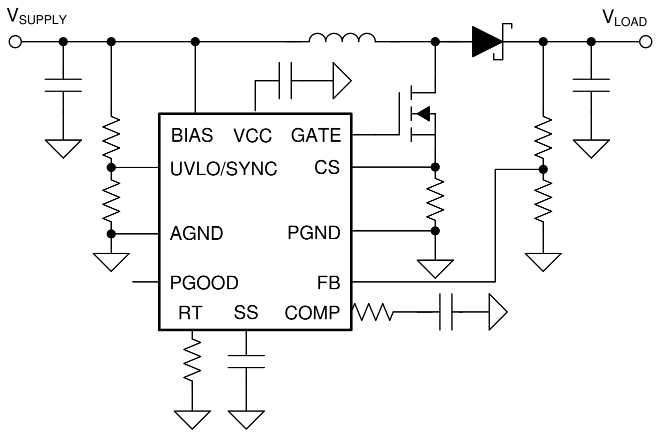


图 10-3. Typical Boost Application

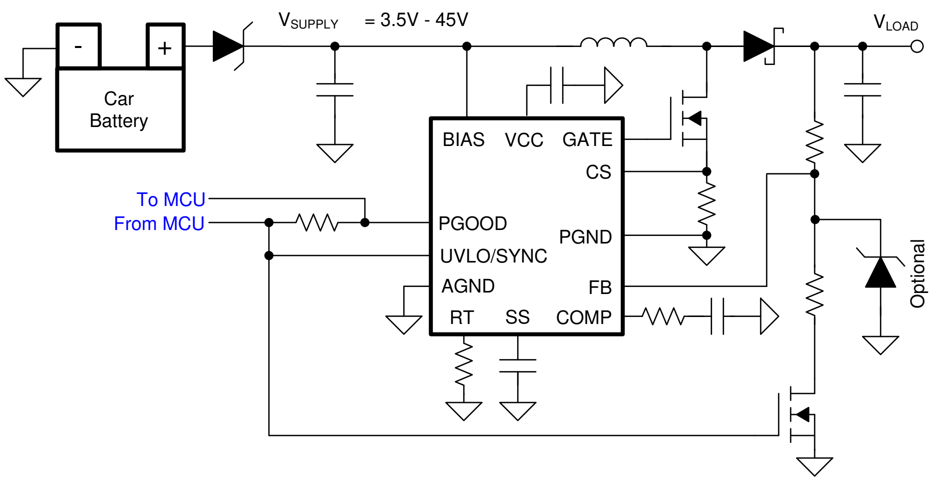


图 10-4. Typical Start-Stop Application

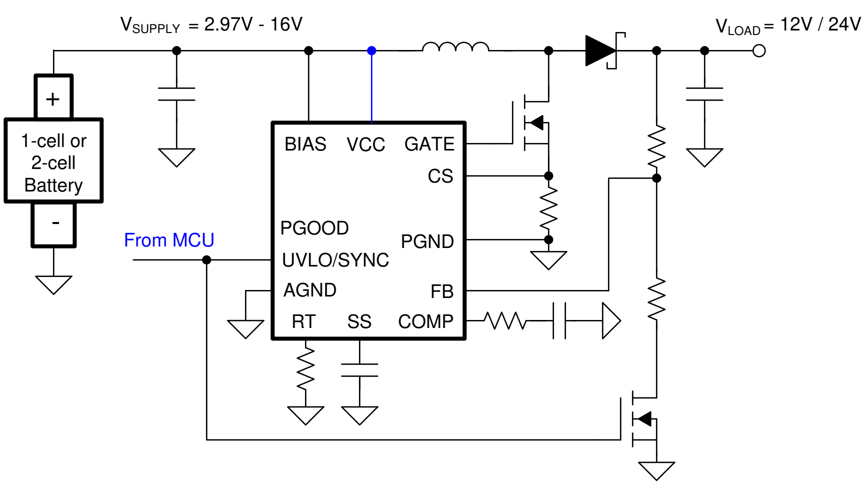


图 10-5. Emergency-call / Boost On-Demand / Portable Speaker

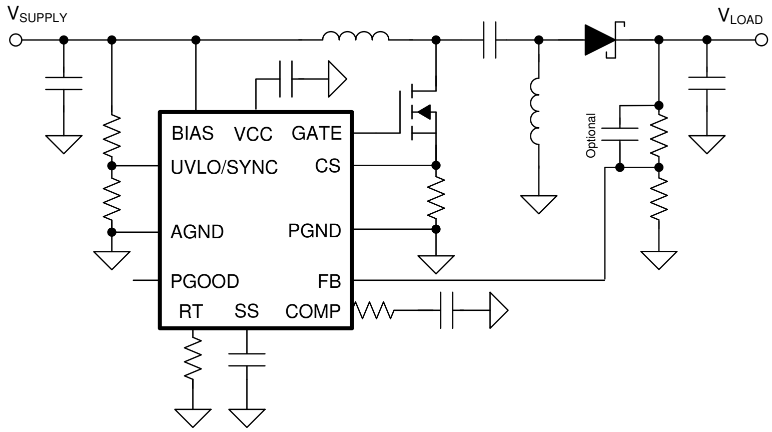


图 10-6. Typical SEPIC Application

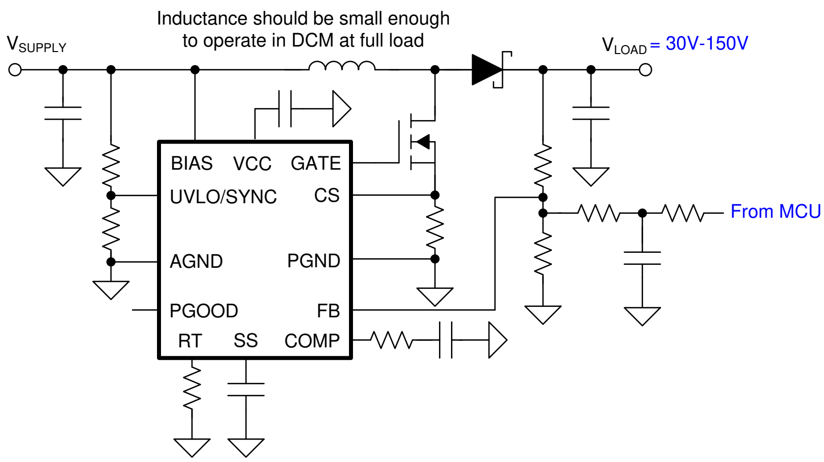


图 10-7. LIDAR Bias Supply 1

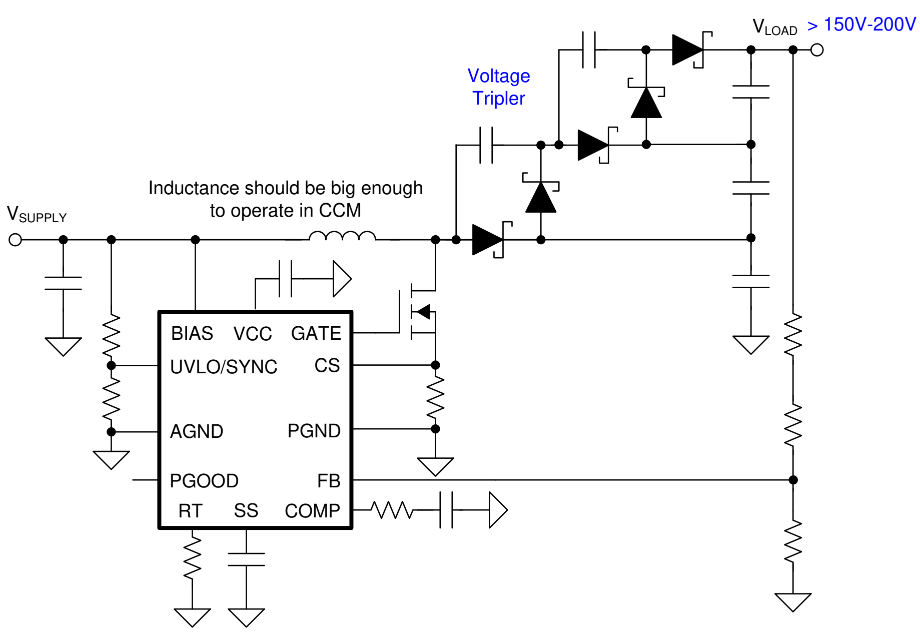


图 10-8. LIDAR Bias Supply 2

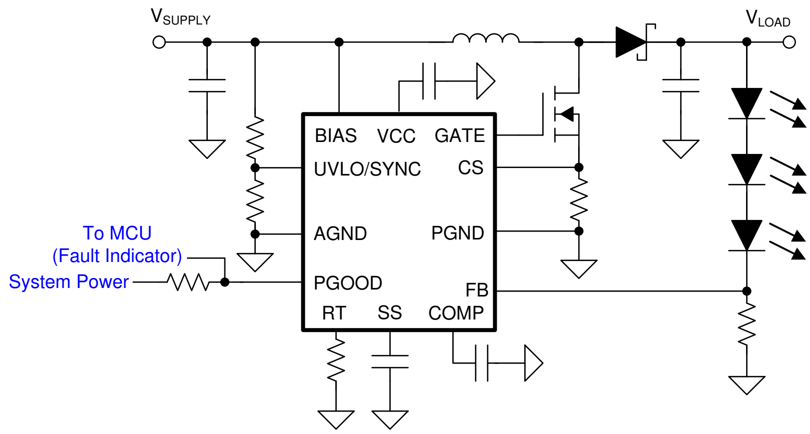


图 10-9. Low-Cost LED Driver

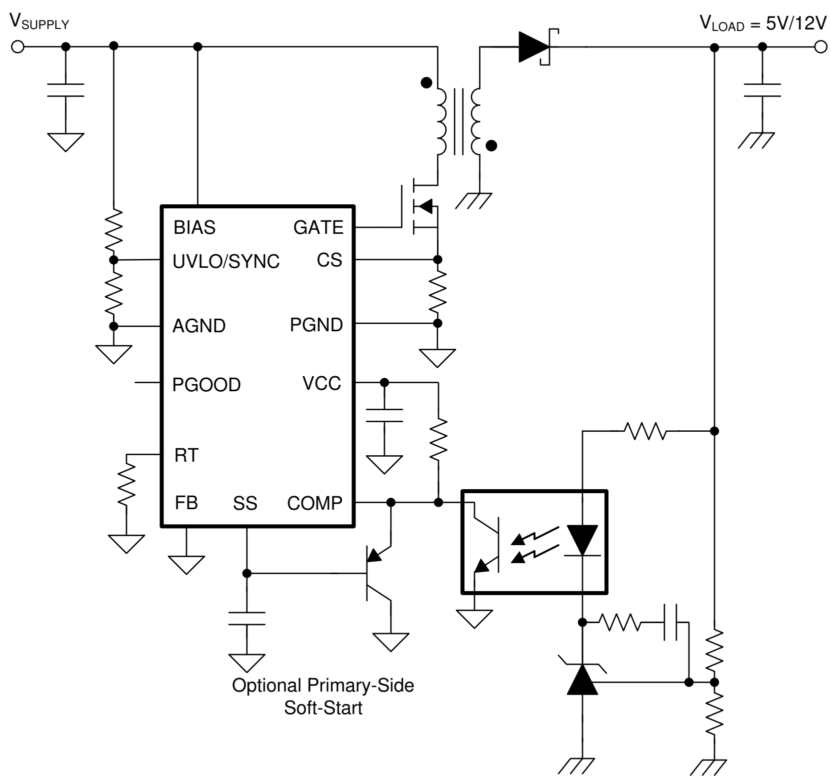


图 10-10. Secondary-Side Regulated Isolated Flyback

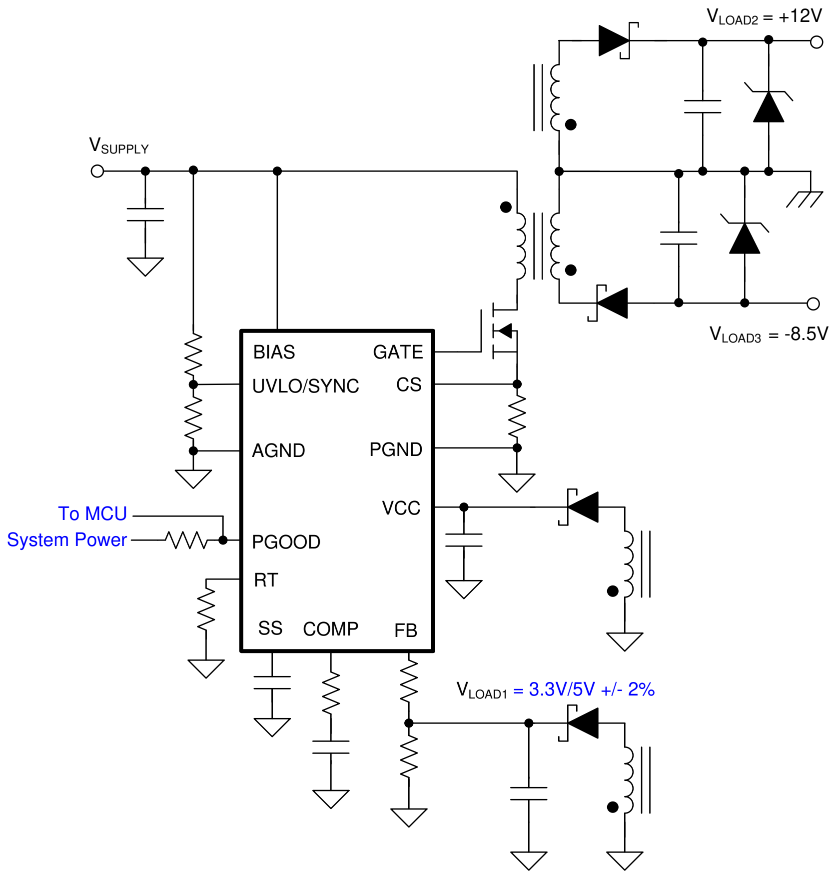


图 10-11. Primary-Side Regulated Multiple-Output Isolated Flyback

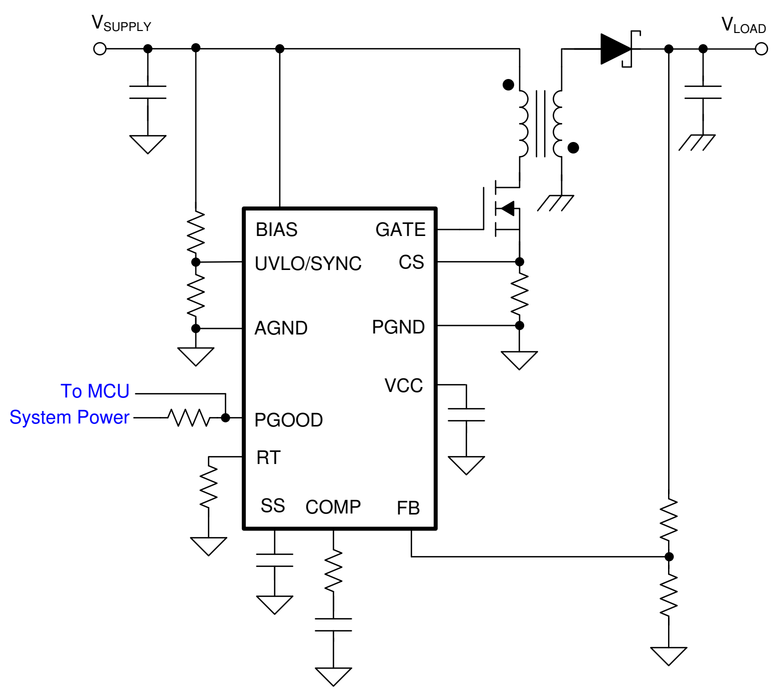


图 10-12. Typical Non-Isolated Flyback

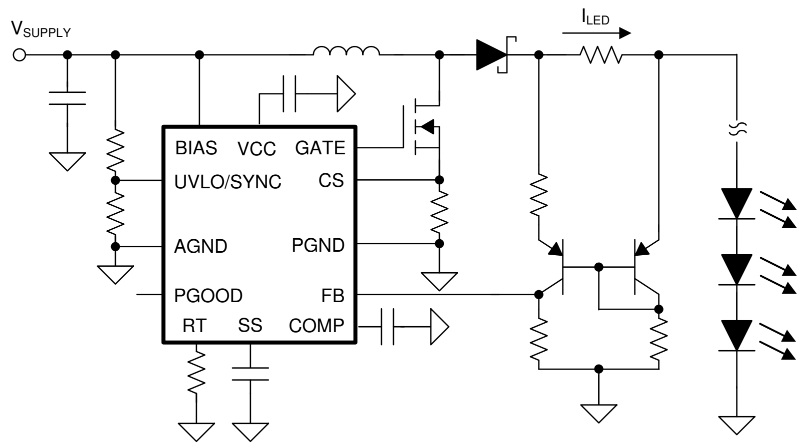


图 10-13. LED Driver with High-Side Current Sensing

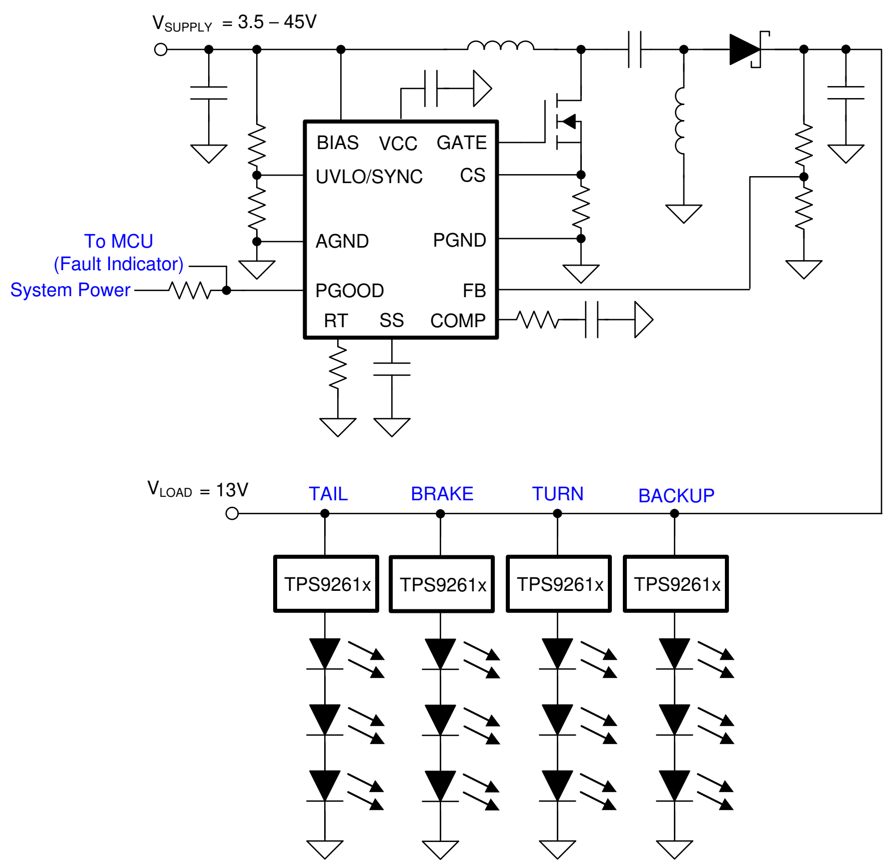


图 10-14. Dual-Stage Automotive Rear-Lights LED Driver

11 Power Supply Recommendations

The device is designed to operate from a power supply or a battery whose voltage range is from 1.5 V to 45 V. The input power supply must be able to supply the maximum boost supply voltage and handle the maximum input current at 1.5 V. The impedance of the power supply and battery including cables must be low enough that an input current transient does not cause an excessive drop. Additional input ceramic capacitors may be required at the supply input of the converter.

12 Layout

12.1 Layout Guidelines

The performance of switching converters heavily depends on the quality of the PCB layout. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimize generation of unwanted EMI.

- Put the Q1, D1, and R_S components on the board first.
- Use a small size ceramic capacitor for C_{OUT}.
- Make the switching loop (C_{OUT} to D1 to Q1 to R_S to C_{OUT}) as small as possible.
- Leave a copper area near the D1 diode for thermal dissipation.
- Put the device near the R_S resistor.
- Put the C_{VCC} capacitor as near the device as possible between the VCC and PGND pins.
- Use a wide and short trace to connect the PGND pin directly to the center of the sense resistor.
- Connect the CS pin to the center of the sense resistor. If necessary, use vias.
- Connect a filter capacitor between CS pin and power ground trace.
- Connect the COMP pin to the compensation components (R_{COMP} and C_{COMP}).
- Connect the C_{COMP} capacitor to the power ground trace.
- Connect the AGND pin directly to the analog ground plane. Connect the AGND pin to the R_{UVLOB}, R_T, C_{SS}, and R_{FBB} components.
- Connect the exposed pad to the AGND and PGND pins under the device.
- Connect the GATE pin to the gate of the Q1 FET. If necessary, use vias.
- Make the switching signal loop (GATE to Q1 to R_S to PGND to GATE) as small as possible.
- Add several vias under the exposed pad to help conduct heat away from the device. Connect the vias to a large ground plane on the bottom layer.

12.2 Layout Examples

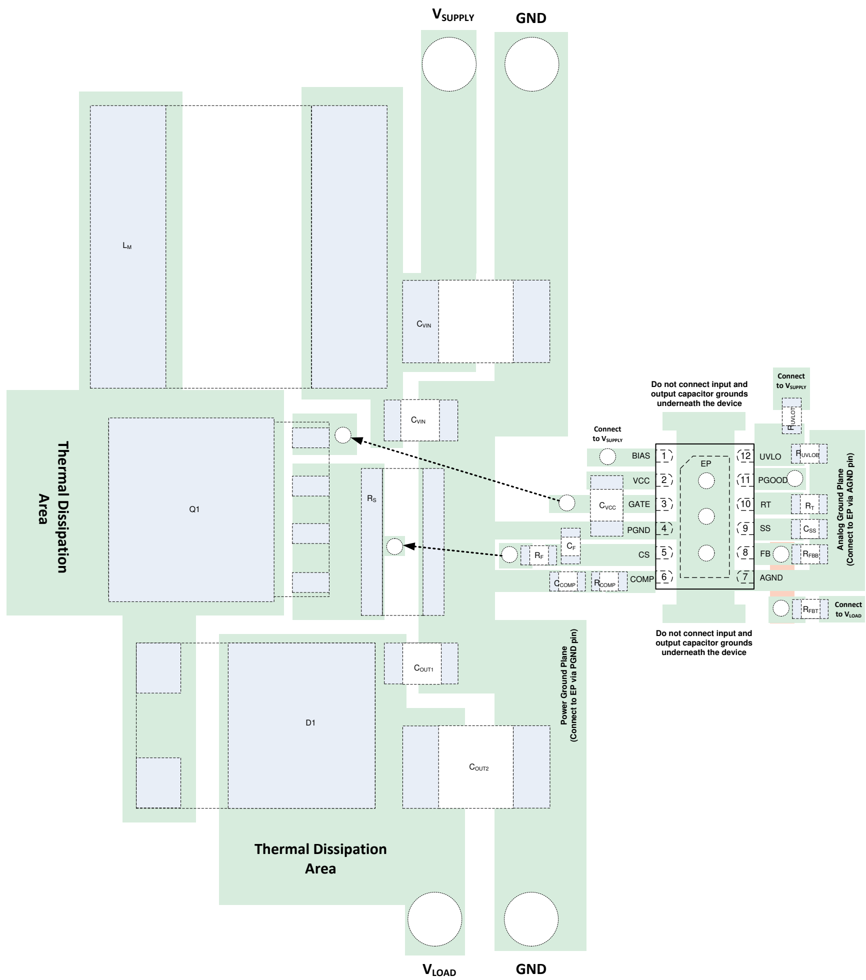


图 12-1. PCB Layout Example 1

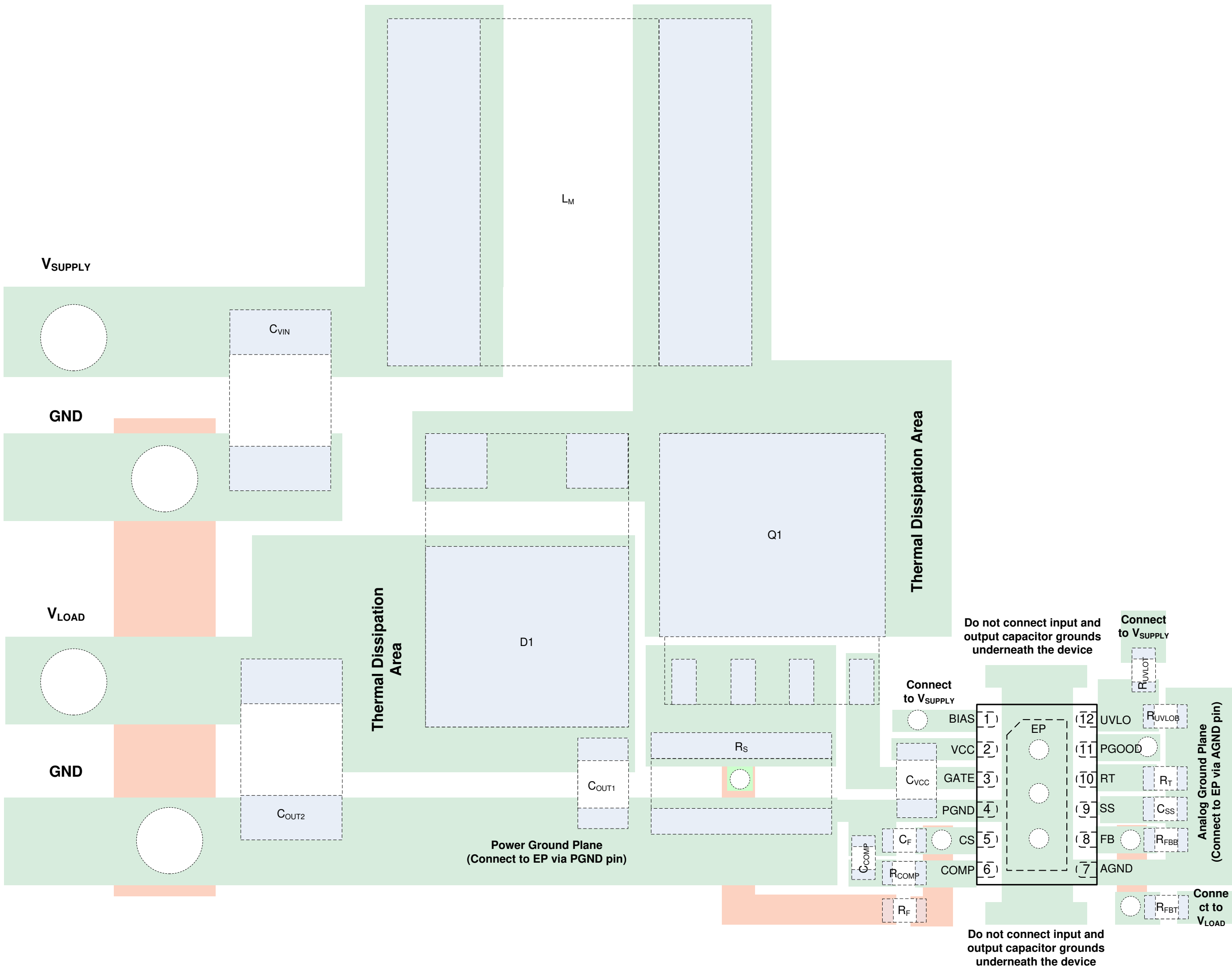


图 12-2. PCB Layout Example 2

13 Device and Documentation Support

13.1 Device Support

13.1.1 第三方产品免责声明

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13.1.2 Development Support

For development support see the following:

- *LM5155 Boost Controller Quick Start Calculator*

13.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5155x-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *LM5155EVM-BST User's Guide*
- Texas Instruments, *How to Design a Boost Converter Using LM5155-Q1*
- Texas Instruments, *LM5155EVM-FLY User's Guide*
- Texas Instruments, *How to Design an Isolated Flyback Converter Using LM5155-Q1*

13.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

13.5 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

13.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM51551QDSSRQ1	ACTIVE	WSON	DSS	12	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	1CW	Samples
LM51551QDSSTQ1	ACTIVE	WSON	DSS	12	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	1CW	Samples
LM5155QDSSRQ1	ACTIVE	WSON	DSS	12	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	CVR	Samples
LM5155QDSSTQ1	ACTIVE	WSON	DSS	12	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	CVR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

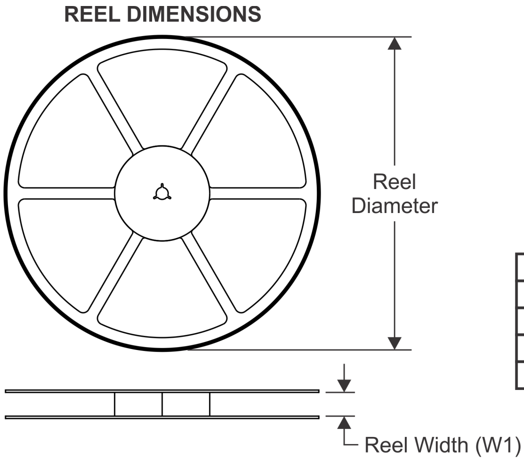
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

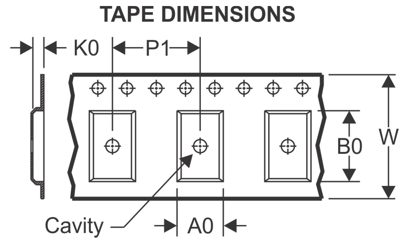
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

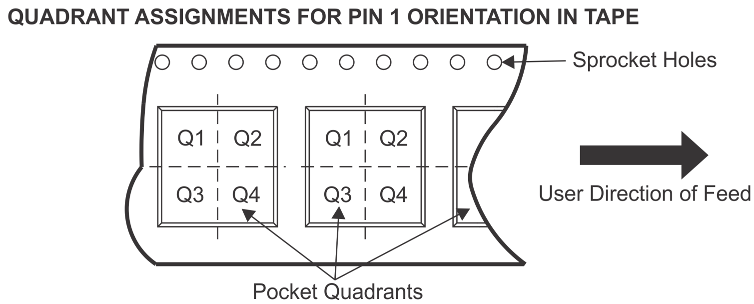
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





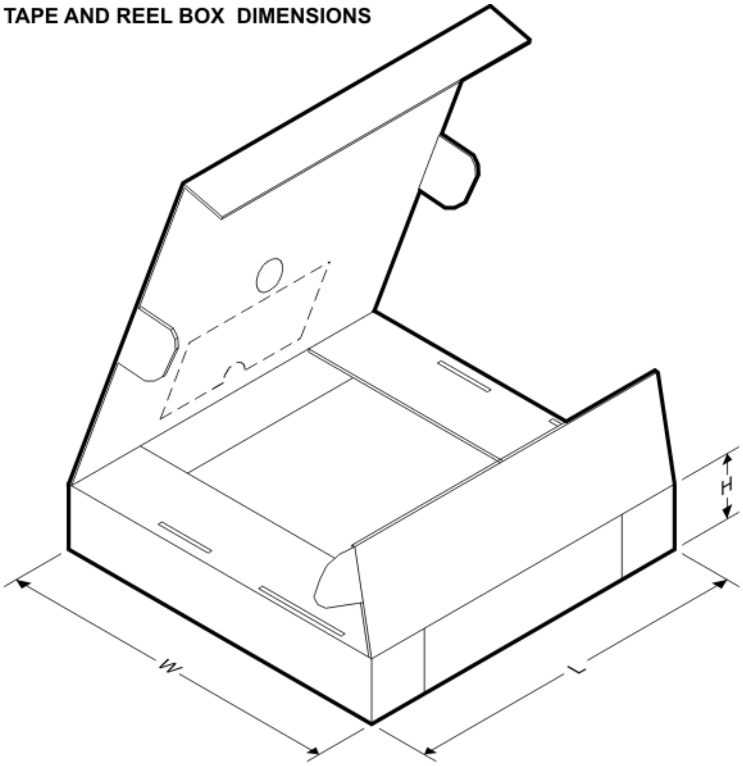
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM51551QDSSRQ1	WSON	DSS	12	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LM51551QDSSTQ1	WSON	DSS	12	250	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LM5155QDSSRQ1	WSON	DSS	12	3000	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
LM5155QDSSTQ1	WSON	DSS	12	250	180.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



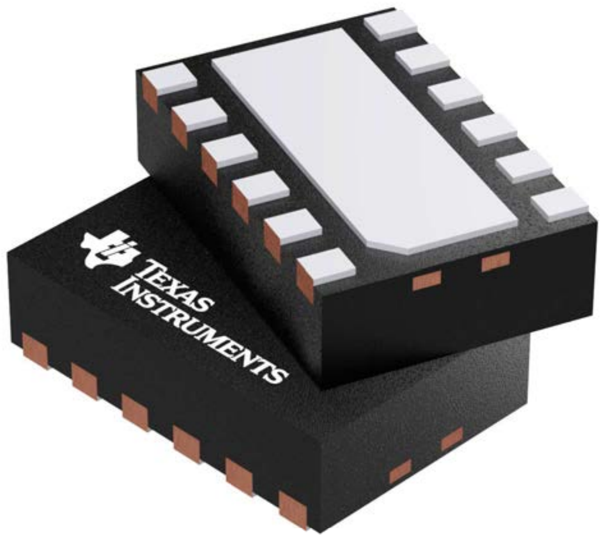
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM51551QDSSRQ1	WSON	DSS	12	3000	213.0	191.0	35.0
LM51551QDSSTQ1	WSON	DSS	12	250	213.0	191.0	35.0
LM5155QDSSRQ1	WSON	DSS	12	3000	213.0	191.0	35.0
LM5155QDSSTQ1	WSON	DSS	12	250	213.0	191.0	35.0

DSS 12

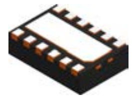
WSON - 0.8 mm max height

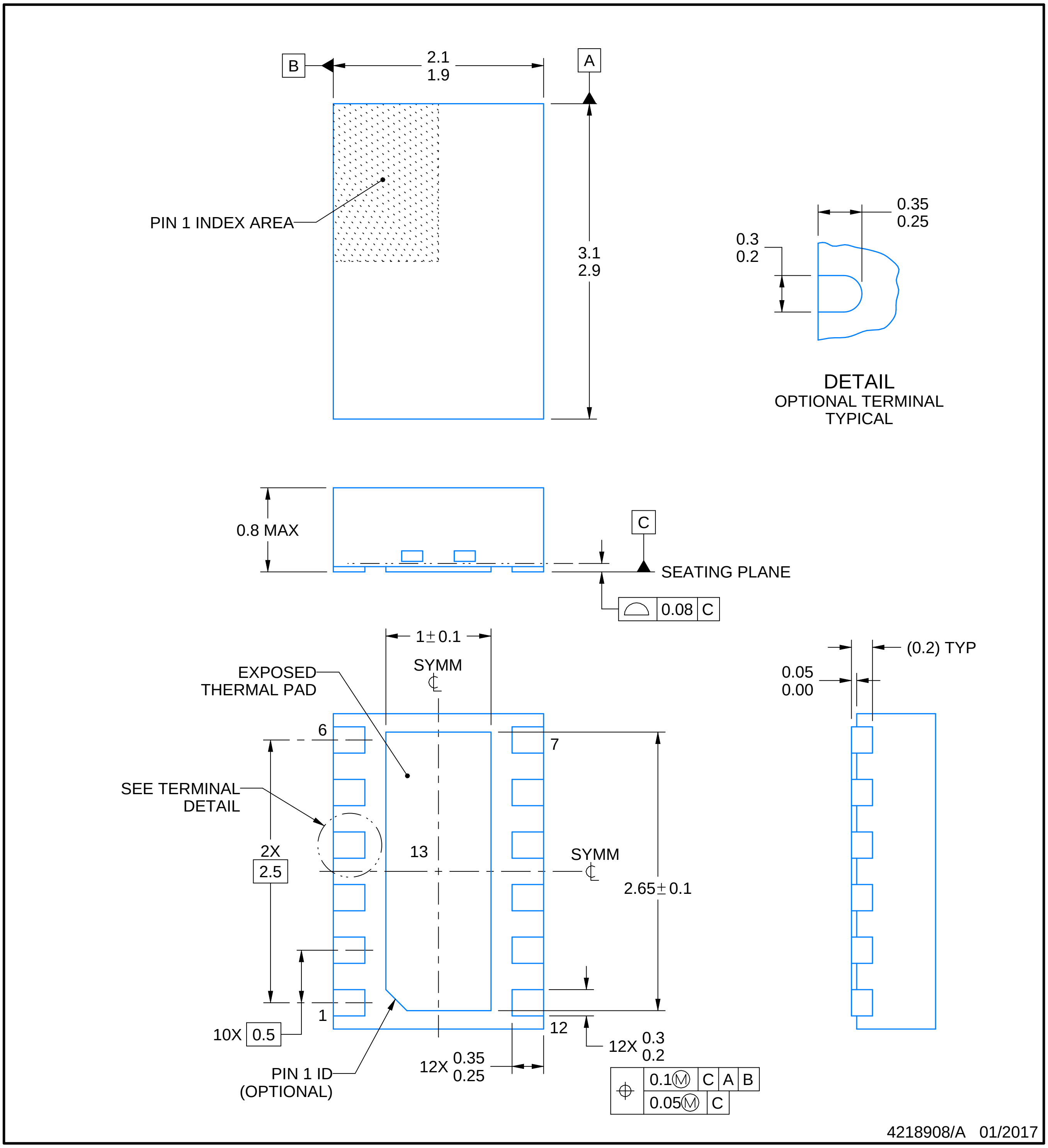
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

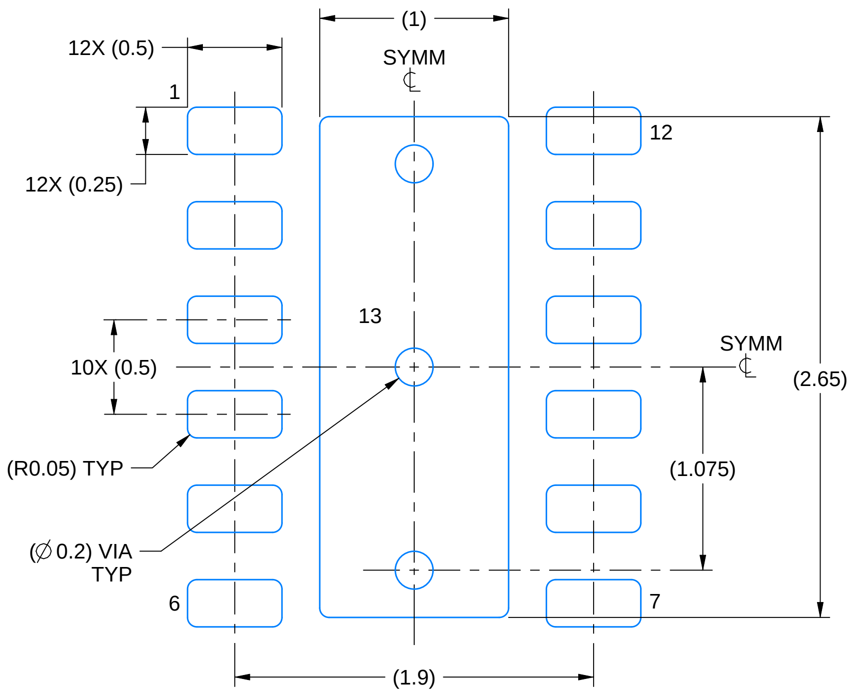
4209244/D



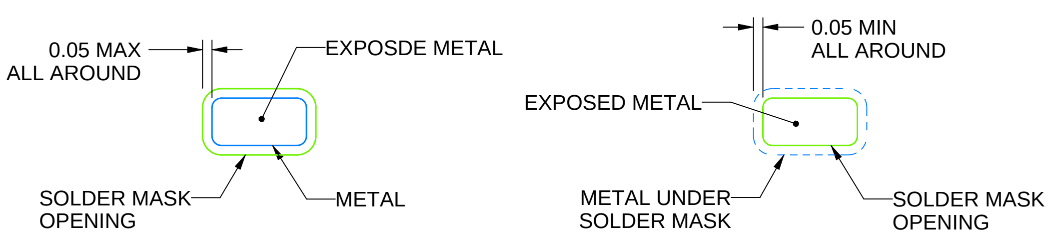


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



NON SOLDER MASK
DEFINED
(PREFERRED)

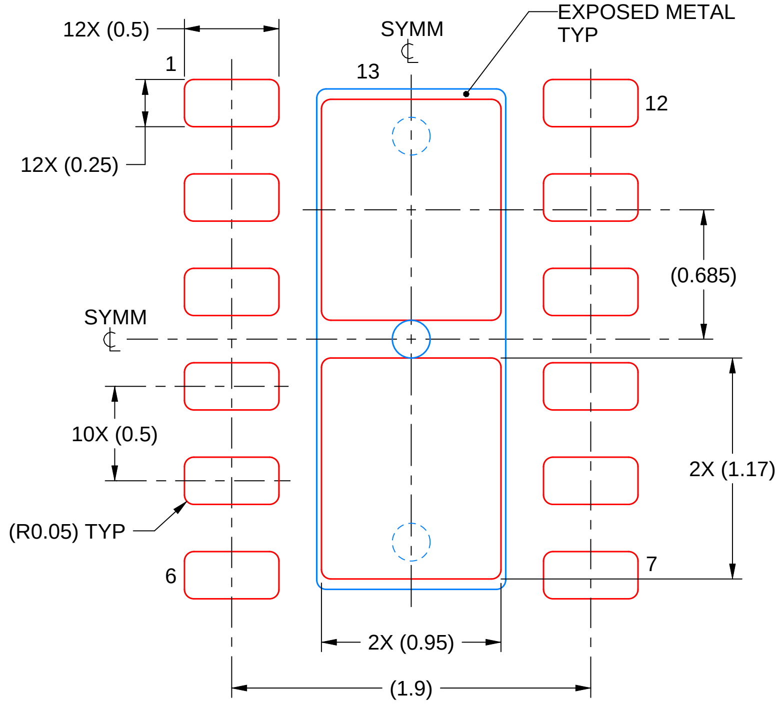
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218908/A 01/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



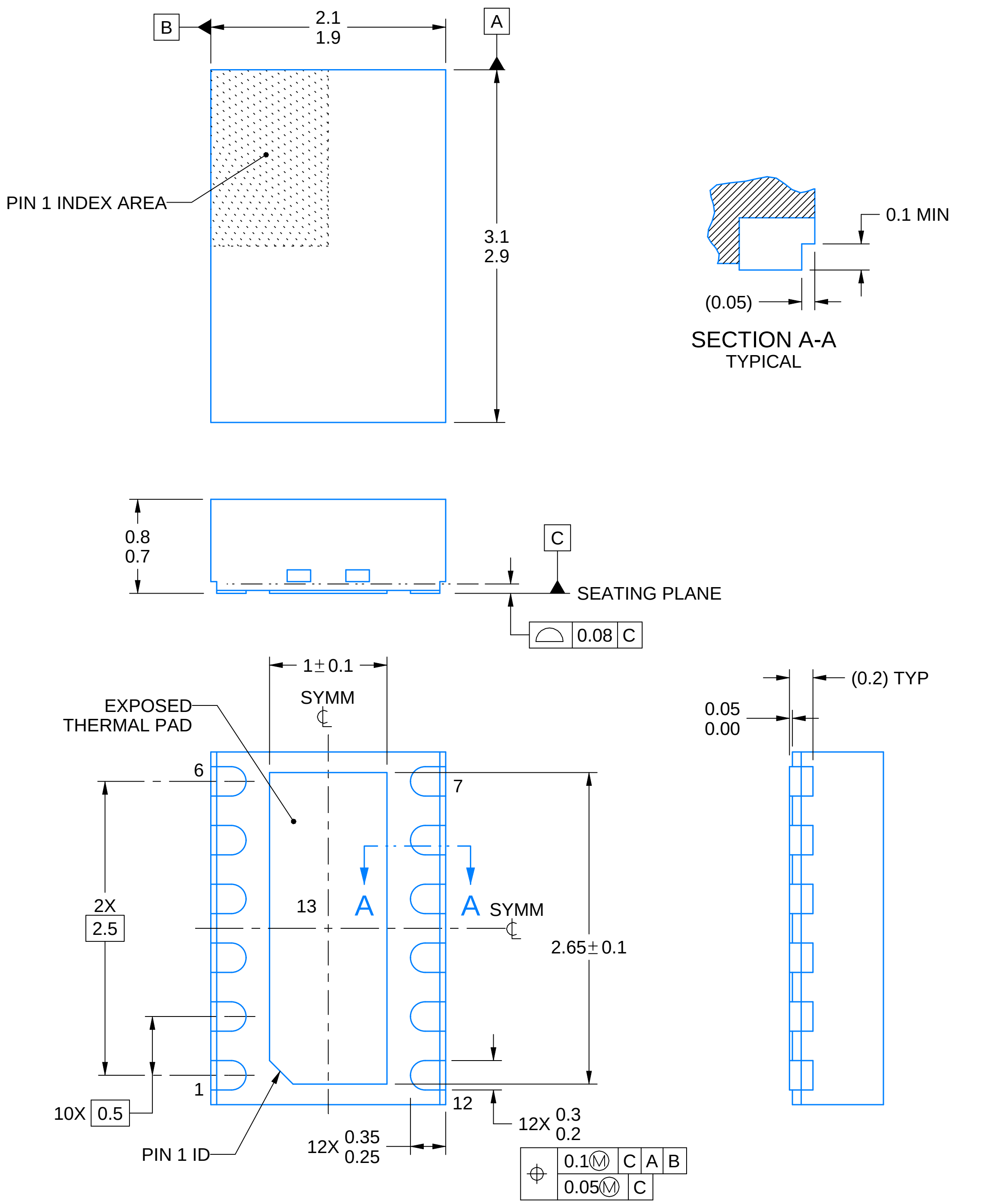
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:
83% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218908/A 01/2017

NOTES: (continued)

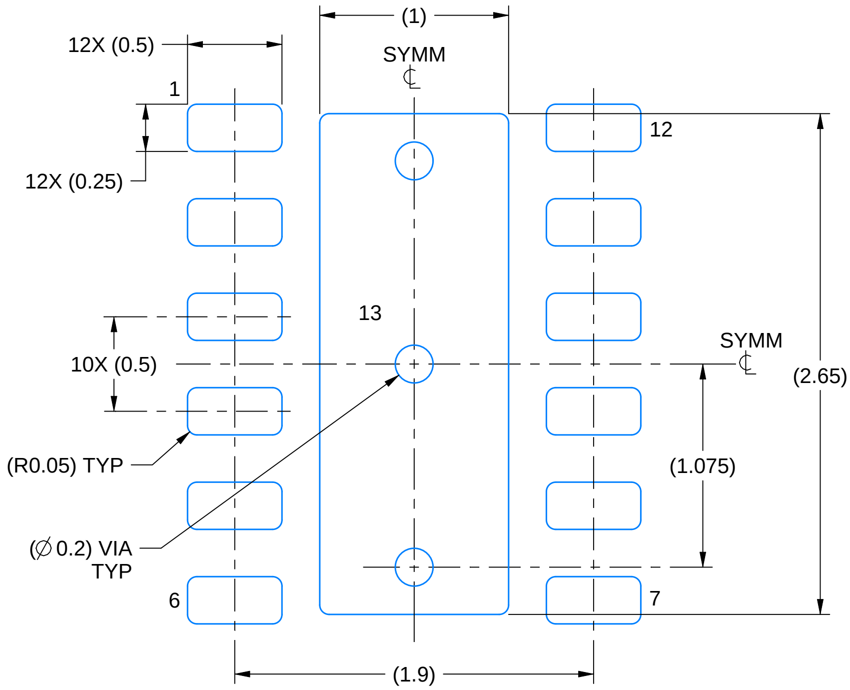
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



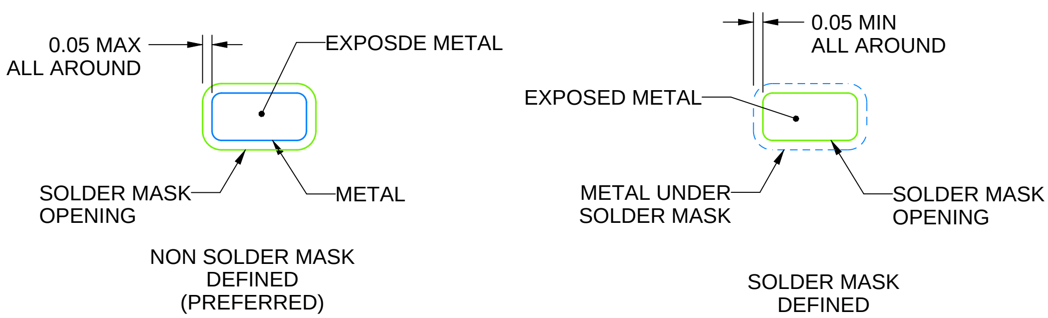
4224220/A 02/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

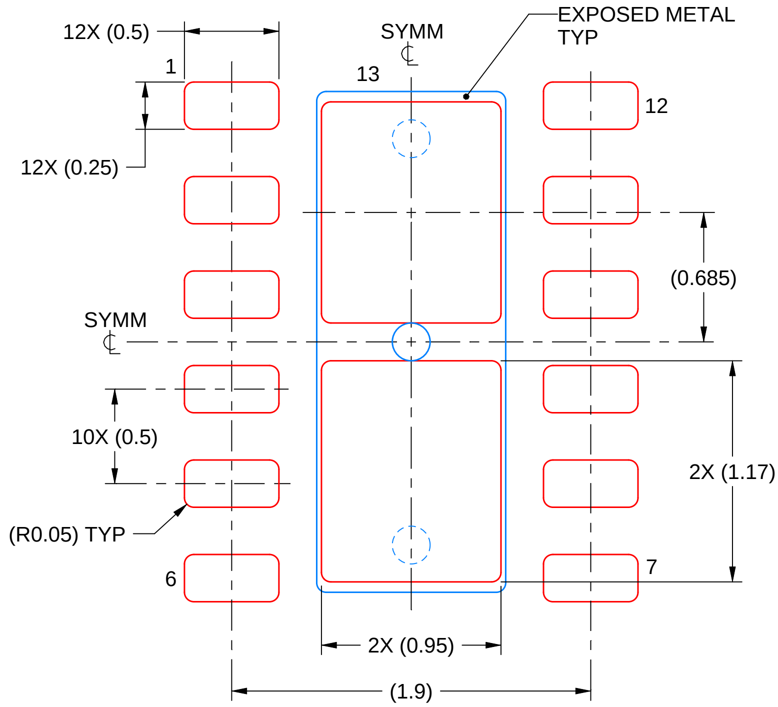


SOLDER MASK DETAILS

4224220/A 02/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:
83% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224220/A 02/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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