LM7171 Very High Speed, High Output Current, Voltage Feedback Amplifier

1 Features

- (Typical Unless Otherwise Noted)
- Easy-to-Use Voltage Feedback Topology
- Very High Slew Rate: 4100 V/µs
- Wide Unity-Gain Bandwidth: 200 MHz
- −3 dB Frequency @ A_V = +2: 220 MHz
- Low Supply Current: 6.5 mA
- High Open Loop Gain: 85 dB
- High Output Current: 100 mA
- Differential Gain and Phase: 0.01%, 0.02°
- Specified for ±15V and ±5V Operation

2 Applications

- HDSL and ADSL Drivers
- Multimedia Broadcast Systems
- Professional Video Cameras
- Video Amplifiers
- Copiers/Scanners/Fax
- HDTV Amplifiers
- Pulse Amplifiers and Peak Detectors
- CATV/Fiber Optics Signal Processing

3 Description

The LM7171 is a high speed voltage feedback amplifier that has the slewing characteristic of a current feedback amplifier, yet it can be used in all traditional voltage feedback amplifier configurations. The LM7171 is stable for gains as low as +2 or −1. It provides a very high slew rate at 4100V/µs and a wide unity-gain bandwidth of 200 MHz while consuming only 6.5 mA of supply current. It is ideal for video and high speed signal processing applications such as HDSL and pulse amplifiers. With 100 mA output current, the LM7171 can be used for video distribution, as a transformer driver or as a laser diode driver.

Operation on ±15 V power supplies allows for large signal swings and provides greater dynamic range and signal-to-noise ratio. The LM7171 offers low SFDR and THD, ideal for ADC/DAC systems. In addition, the LM7171 is specified for ±5 V operation for portable applications.

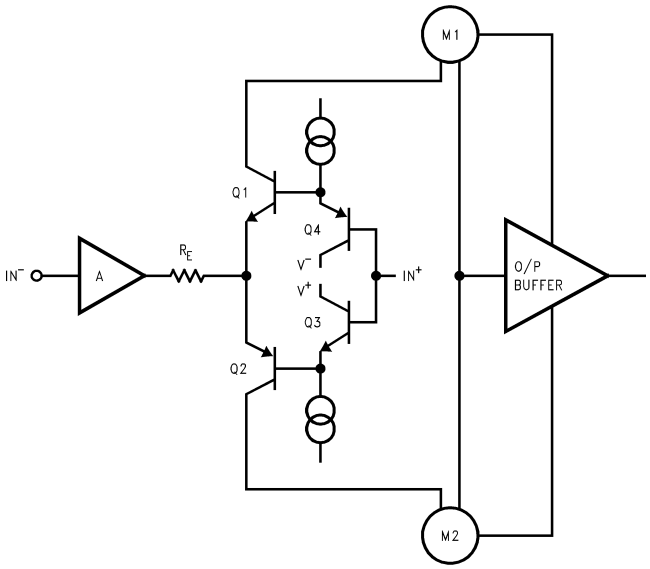
The LM7171 is built on TI's advanced VIP™ III (Vertically integrated PNP) complementary bipolar process.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM7171	SOIC (8)	4.90 mm × 3.91 mm
LM7171	PDIP (8)	9.81 mm × 6.35 mm

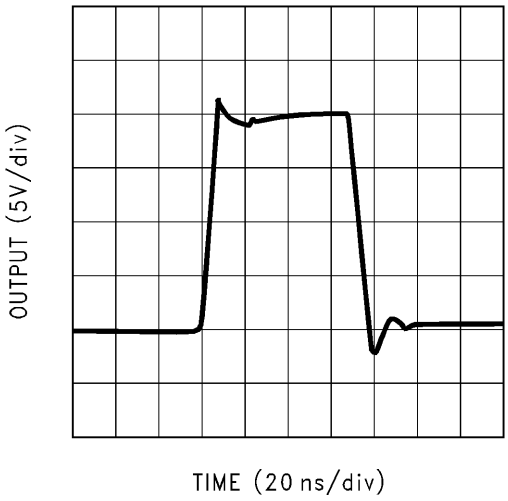
(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic Diagram



Note: M1 and M2 are current mirrors.

Large Signal Pulse Response
A_V = +2, V_S = ±15V



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2013) to Revision C — **Page**

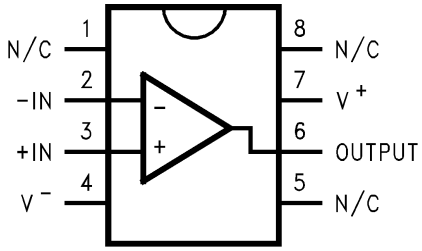
- Changed data sheet flow and layout to conform with new TI standards. Added the following sections: Device Information Table, Application and Implementation; Layout; Device and Documentation Support; Mechanical, Packaging, and Ordering Information ... 1
- Changed "Junction Temperature Range" to " Operating Temperature Range" and deleted T_J ... 4
- Deleted T_J = 25°C for Electrical Characteristics tables ... 5

Changes from Revision A (March 2013) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format ... 20

5 Pin Configuration and Functions

8-Pin
Package D
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
N/C	1	–	No Connection
-IN	2	I	Inverting Power Supply
+IN	3	I	Non-inverting Power Supply
V-	4	I	Supply Voltage
N/C	5	–	No Connection
OUTPUT	6	O	Output
V+	7	I	Supply Voltage
N/C	8	–	No Connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply Voltage (V^+–V^-)		36	V
Differential Input Voltage (2)		±10	V
Output Short Circuit to Ground (3)	Continuous		
Maximum Junction Temperature (4)		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input differential voltage is applied at V_S = ±15V.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}–T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	+150	°C
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2)		2500	V

(1) Human body model, 1.5 kΩ in series with 100 pF.
(2) JEDEC document JEP155 states that 2500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply Voltage		5.5V ≤ V_S ≤ 36		V
Operating Temperature Range: LM7171AI, LM7171BI	−40		+85	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For ensured specifications and the test conditions, see the Electrical Characteristics.

6.4 Thermal Information

THERMAL METRIC(1)		P (PDIP) 8 PINS	D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108°	172°	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 ±15V DC Electrical Characteristics

Unless otherwise noted, all limits are specified for V^+ = +15 V, V^- = –15 V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

	PARAMETER	TEST CONDITIONS	TYP (1)	LM7171AI LIMIT (2)	LM7171BI LIMIT (2)	UNIT
V_{OS}	Input Offset Voltage		0.2	1	3	mV
				4	**7**	max
TC V_{OS}	Input Offset Voltage Average Drift		35			µV/°C
I_B	Input Bias Current		2.7	10	10	µA
				12	**12**	max
I_{OS}	Input Offset Current		0.1	4	4	µA
				6	**6**	max
R_{IN}	Input Resistance	Common Mode	40			MΩ
		Differential Mode	3.3			
R_O	Open Loop Output Resistance		15			Ω
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V	105	85	75	dB
				80	**70**	min
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V	90	85	75	dB
				80	**70**	min
V_{CM}	Input Common-Mode Voltage Range	CMRR > 60 dB	±13.35			V
A_V	Large Signal Voltage Gain (3)	R_L = 1 kΩ	85	80	75	dB
				75	**70**	min
		R_L = 100Ω	81	75	70	dB
				70	**66**	min
V_O	Output Swing	R_L = 1 kΩ	13.3	13	13	V
				12.7	**12.7**	min
			−13.2	−13	−13	V
				−12.7	**−12.7**	max
		R_L = 100Ω	11.8	10.5	10.5	V
				9.5	**9.5**	min
			−10.5	−9.5	−9.5	V
				−9	**−9**	max
	Output Current (Open Loop) (4)	Sourcing, R_L = 100Ω	118	105	105	mA
				95	**95**	min
		Sinking, R_L = 100Ω	105	95	95	mA
				90	**90**	max
	Output Current (in Linear Region)	Sourcing, R_L = 100Ω	100			mA
		Sinking, R_L = 100Ω	100			
I_{SC}	Output Short Circuit Current	Sourcing	140			mA
		Sinking	135			
I_S	Supply Current		6.5	8.5	8.5	mA
				9.5	**9.5**	max

(1) Typical values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = ±5V, V_{OUT} = ±1V.
(4) The open loop output current is specified, by the measurement of the open loop output voltage swing, using 100Ω output load.

6.6 ±15V AC Electrical Characteristics

Unless otherwise noted, all limits are specified for V^+ = +15V, V^- = −15V, V_{CM} = 0V, and R_L = 1 kΩ.

PARAMETER		CONDITIONS	TYP(1)	LM7171AI LIMIT(2)	LM7171BI LIMIT(2)	UNIT
SR	Slew Rate (3)	A_V = +2, V_{IN} = 13 V_{PP}	4100			V/µs
		A_V = +2, V_{IN} = 10 V_{PP}	3100			
	Unity-Gain Bandwidth		200			MHz
	−3 dB Frequency	A_V = +2	220			MHz
φ_m	Phase Margin		50			Deg
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±5V R_L = 500Ω	42			ns
t_p	Propagation Delay	A_V = −2, V_{IN} = ±5V, R_L = 500Ω	5			ns
A_D	Differential Gain (4)		0.01%			
φ_D	Differential Phase (4)		0.02			Deg
	Second Harmonic Distortion(5)	f_{IN} = 10 kHz	−110			dBc
		f_{IN} = 5 MHz	−75			dBc
	Third Harmonic Distortion(5)	f_{IN} = 10 kHz	−115			dBc
		f_{IN} = 5 MHz	−55			dBc
e_n	Input-Referred Voltage Noise	f = 10 kHz	14			nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz	1.5			pA/√Hz

(1) Typical values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Slew Rate is the average of the raising and falling slew rates.
(4) Differential gain and phase are measured with A_V = +2, V_{IN} = 1 V_{PP} at 3.58 MHz and both input and output 75Ω terminated.
(5) Harmonics are measured with V_{IN} = 1 V_{PP}, A_V = +2 and R_L = 100Ω.

6.7 ±5V DC Electrical Characteristics

Unless otherwise noted, all limits are specified for V^+ = +5V, V^- = −5V, V_{CM} = 0V, and R_L = 1 kΩ. **Boldface** limits apply at the temperature extremes

	PARAMETER	TEST CONDITIONS	TYP (1)	LM7171AI LIMIT (2)	LM7171BI LIMIT (2)	UNIT
V_{OS}	Input Offset Voltage		0.3	1.5	3.5	mV
				4	**7**	max
TC V_{OS}	Input Offset Voltage Average Drift		35			µV/°C
I_B	Input Bias Current		3.3	10	10	µA
				12	**12**	max
I_{OS}	Input Offset Current		0.1	4	4	µA
				6	**6**	max
R_{IN}	Input Resistance	Common Mode	40			MΩ
		Differential Mode	3.3			
R_O	Output Resistance		15			Ω
CMRR	Common Mode Rejection Ratio	V_{CM} = ±2.5V	104	80	70	dB
				75	**65**	min
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V	90	85	75	dB
				80	**70**	min
V_{CM}	Input Common-Mode Voltage Range	CMRR > 60 dB	±3.2			V
A_V	Large Signal Voltage Gain (3)	R_L = 1 kΩ	78	75	70	dB
				70	**65**	min
		R_L = 100Ω	76	72	68	dB
				67	**63**	min
V_O	Output Swing	R_L = 1 kΩ	3.4	3.2	3.2	V
				3	**3**	min
			−3.4	−3.2	−3.2	V
				−3	**−3**	max
		R_L = 100Ω	3.1	2.9	2.9	V
				2.8	**2.8**	min
			−3.0	−2.9	−2.9	V
				−2.8	**−2.8**	max
	Output Current (Open Loop) (4)	Sourcing, R_L = 100Ω	31	29	29	mA
				28	**28**	min
		Sinking, R_L = 100Ω	30	29	29	mA
				28	**28**	max
I_{SC}	Output Short Circuit Current	Sourcing	135			mA
		Sinking	100			
I_S	Supply Current		6.2	8	8	mA
				9	**9**	max

(1) Typical values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±5V. For V_S = ±5V, V_{OUT} = ±1V.
(4) The open loop output current is specified, by the measurement of the open loop output voltage swing, using 100Ω output load.

6.8 ±5V AC Electrical Characteristics

Unless otherwise noted, all limits are specified for $V^+ = +5V$, $V^- = -5V$, $V_{CM} = 0V$, and $R_L = 1\ k\Omega$.

PARAMETER		TEST CONDITIONS	TYP(1)	LM7171AI LIMIT(2)	LM7171BI LIMIT(2)	UNIT
SR	Slew Rate (3)	$A_V = +2$, $V_{IN} = 3.5\ V_{PP}$	950			V/µs
	Unity-Gain Bandwidth		125			MHz
	−3 dB Frequency	$A_V = +2$	140			MHz
φ_m	Phase Margin		57			Deg
t_s	Settling Time (0.1%)	$A_V = -1$, $V_O = \pm 1V$, $R_L = 500\Omega$	56			ns
t_p	Propagation Delay	$A_V = -2$, $V_{IN} = \pm 1V$, $R_L = 500\Omega$	6			ns
A_D	Differential Gain (4)		0.02%			
φ_D	Differential Phase (5)		0.03			Deg
	Second Harmonic Distortion(6)	$f_{IN} = 10$ kHz	−102			dBc
		$f_{IN} = 5$ MHz	−70			dBc
	Third Harmonic Distortion(6)	$f_{IN} = 10$ kHz	−110			dBc
		$f_{IN} = 5$ MHz	−51			dBc
e_n	Input-Referred Voltage Noise	f = 10 kHz	14			nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz	1.8			pA/√Hz

(1) Typical values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Slew Rate is the average of the raising and falling slew rates.
(4) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For ensured specifications and the test conditions, see the Electrical Characteristics.
(5) Differential gain and phase are measured with $A_V = +2$, $V_{IN} = 1\ V_{PP}$ at 3.58 MHz and both input and output 75Ω terminated.
(6) Harmonics are measured with $V_{IN} = 1\ V_{PP}$, $A_V = +2$ and $R_L = 100\Omega$.

6.9 Typical Performance Characteristics

unless otherwise noted, T_A= 25°C

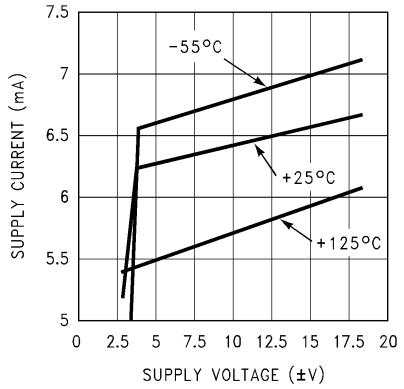


Figure 1. Supply Current vs. Supply Voltage

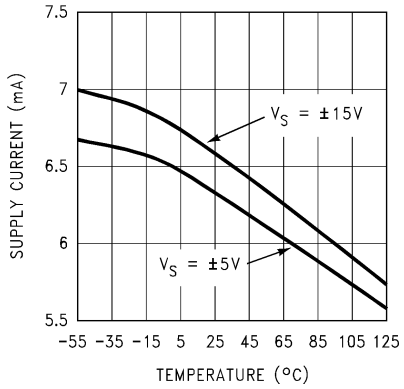


Figure 2. Supply Current vs. Temperature

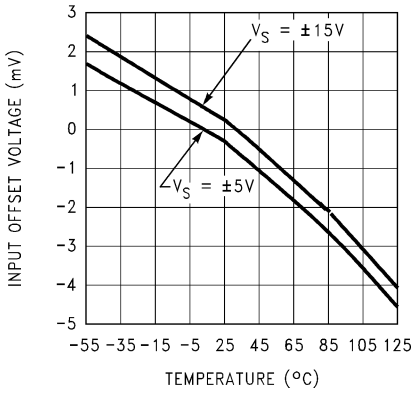


Figure 3. Input Offset Voltage vs. Temperature

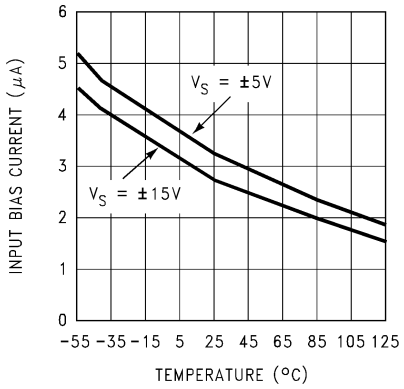


Figure 4. Input Bias Current vs. Temperature

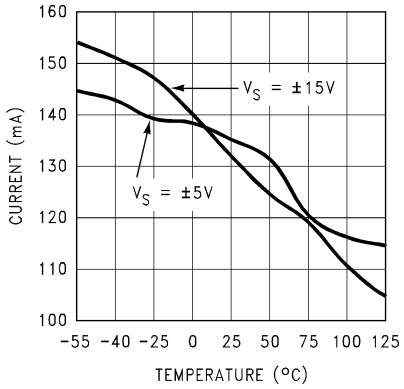


Figure 5. Short Circuit Current vs. Temperature (Sourcing)

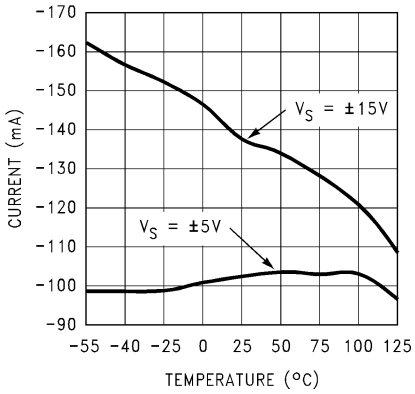


Figure 6. Short Circuit Current vs. Temperature (Sinking)

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

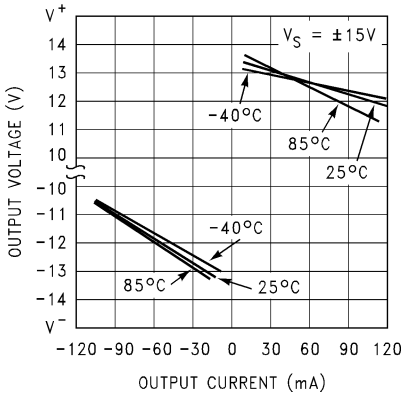


Figure 7. Output Voltage vs. Output Current

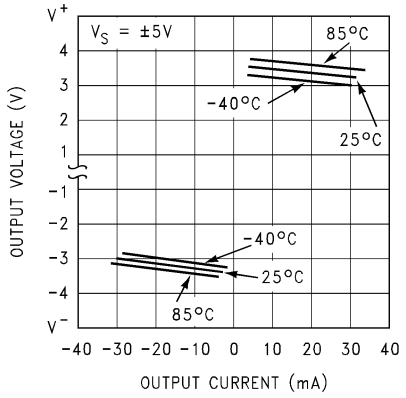


Figure 8. Output Voltage vs. Output Current

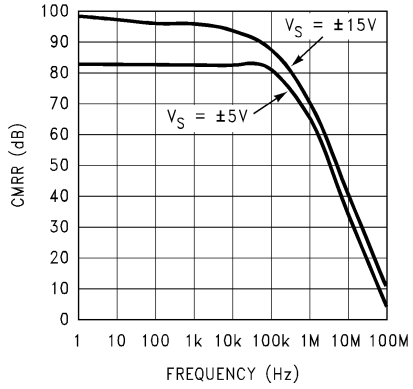


Figure 9. CMRR vs. Frequency

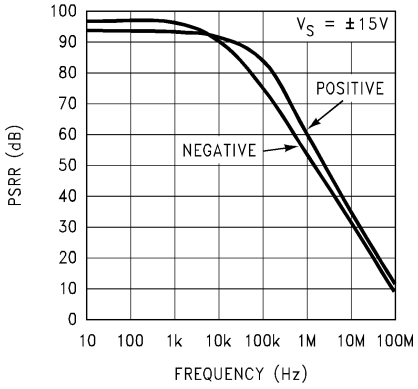


Figure 10. PSRR vs. Frequency

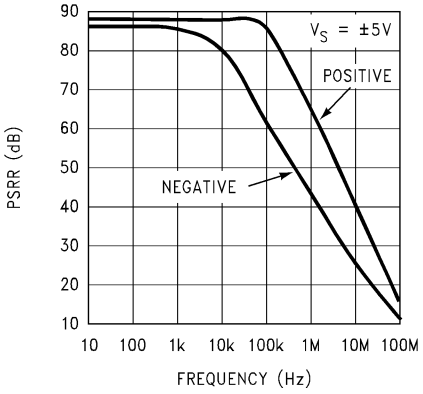


Figure 11. PSRR vs. Frequency

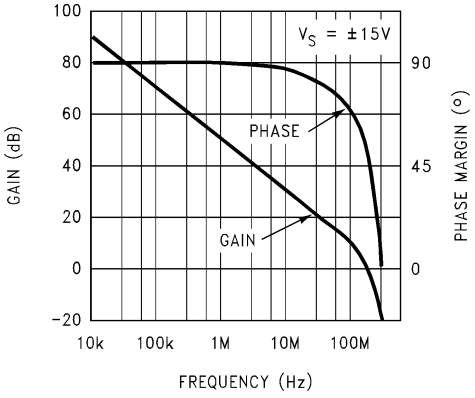


Figure 12. Open Loop Frequency Response

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

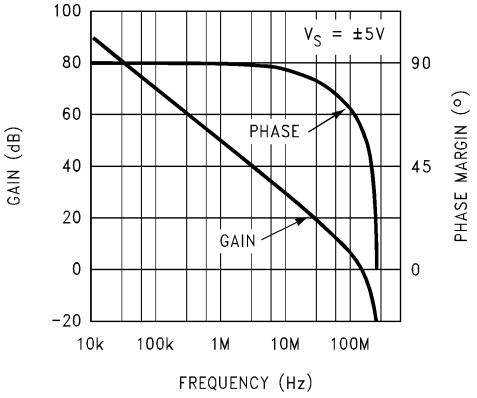


Figure 13. Open Loop Frequency Response

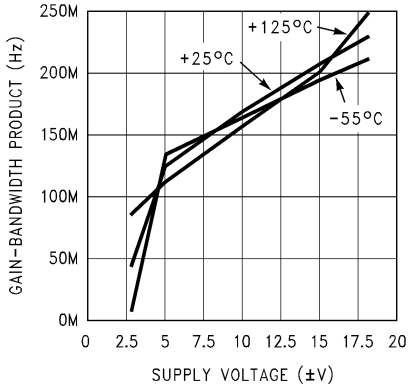


Figure 14. Gain-Bandwidth Product vs. Supply Voltage

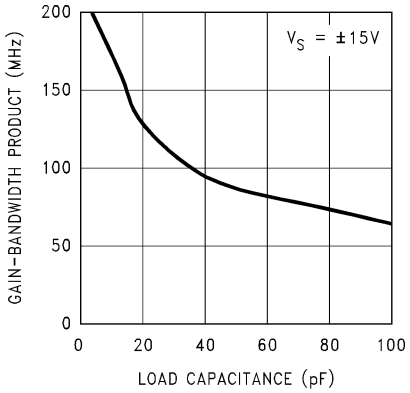


Figure 15. Gain-Bandwidth Product vs. Load Capacitance

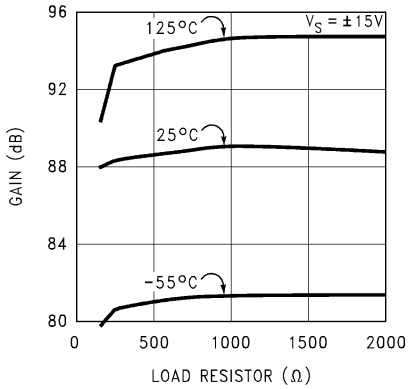


Figure 16. Large Signal Voltage Gain vs. Load

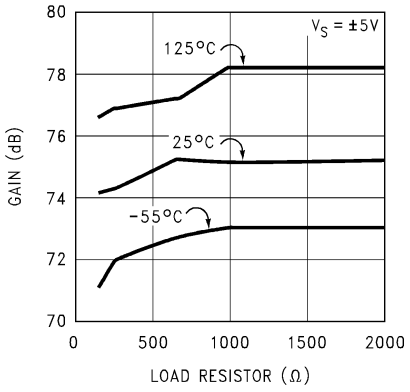


Figure 17. Large Signal Voltage Gain vs. Load

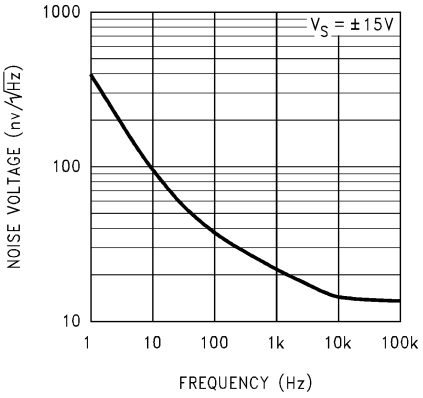


Figure 18. Input Voltage Noise vs. Frequency

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

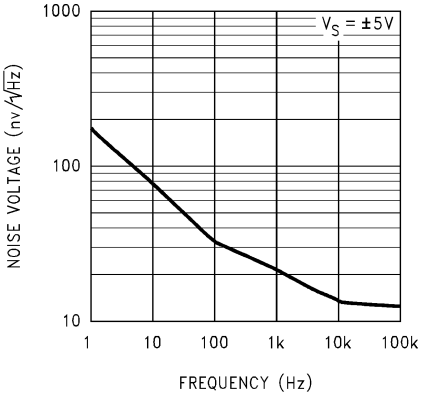


Figure 19. Input Voltage Noise vs. Frequency

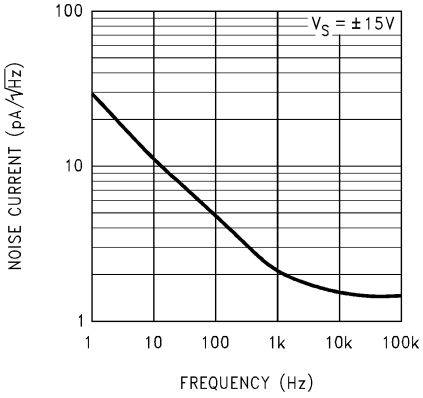


Figure 20. Input Current Noise vs. Frequency

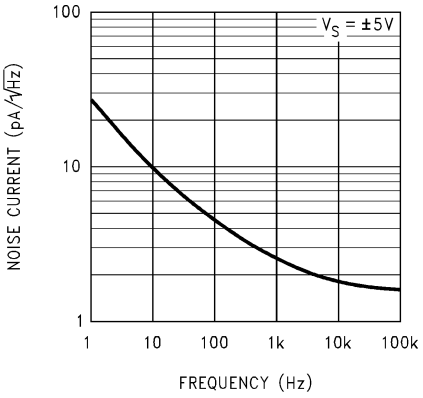


Figure 21. Input Current Noise vs. Frequency

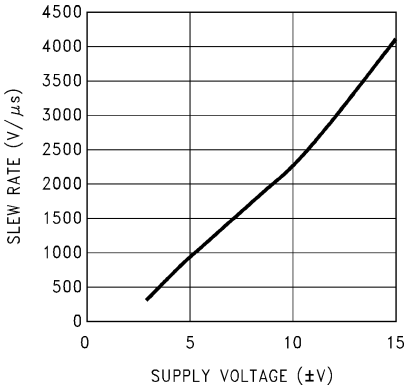


Figure 22. Slew Rate vs. Supply Voltage

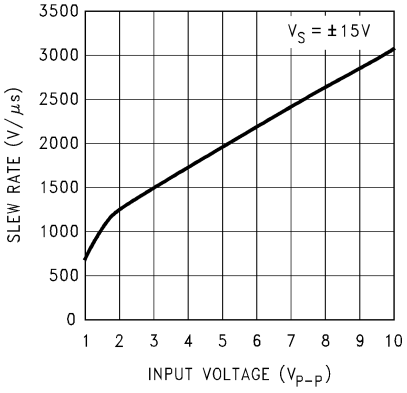


Figure 23. Slew Rate vs. Input Voltage

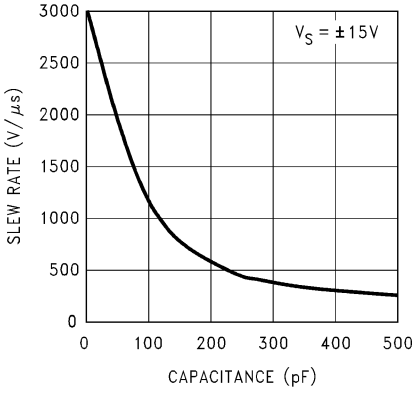


Figure 24. Slew Rate vs. Load Capacitance

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

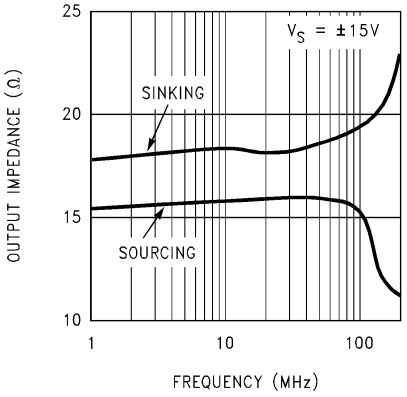


Figure 25. Open Loop Output Impedance vs. Frequency

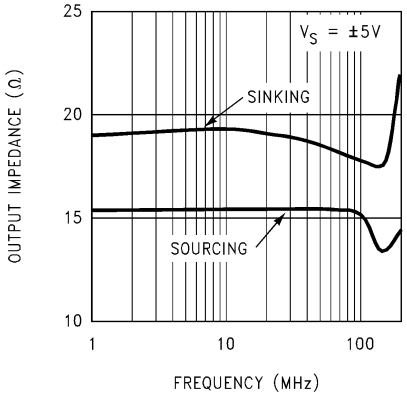


Figure 26. Open Loop Output Impedance vs Frequency

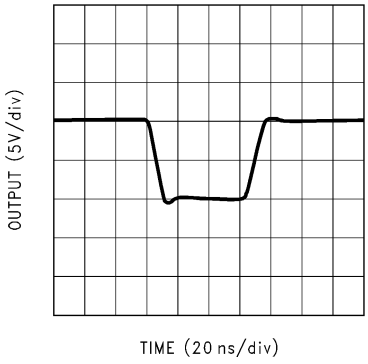


Figure 27. Large Signal Pulse Response A_V = −1, V_S = ±15V

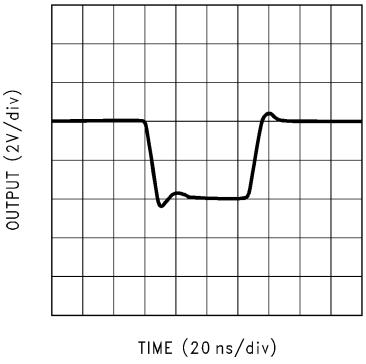


Figure 28. Large Signal Pulse Response A_V = −1, V_S = ±5V

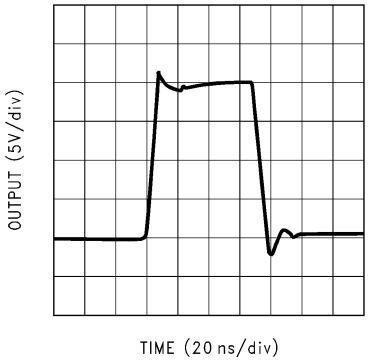


Figure 29. Large Signal Pulse Response A_V = +2, V_S = ±15V

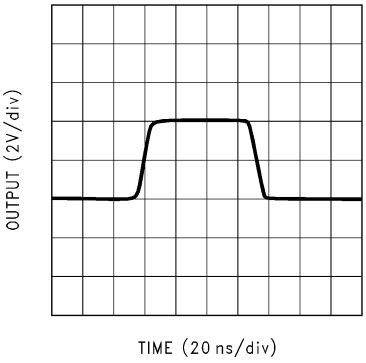


Figure 30. Large Signal Pulse Response A_V = +2, V_S = ±5V

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

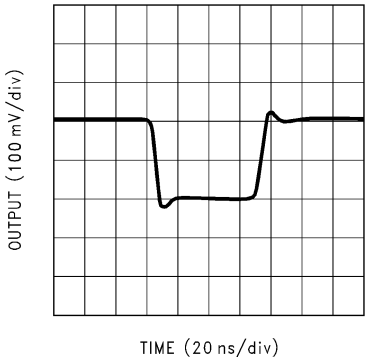


Figure 31. Small Signal Pulse Response A_V = −1, V_S = ±15V

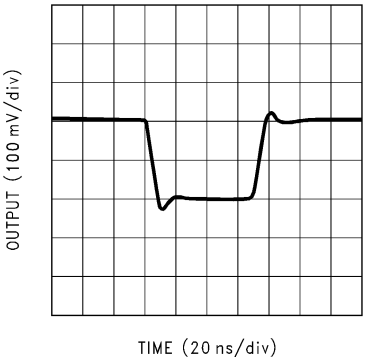


Figure 32. Small Signal Pulse Response A_V = −1, V_S = ±5V

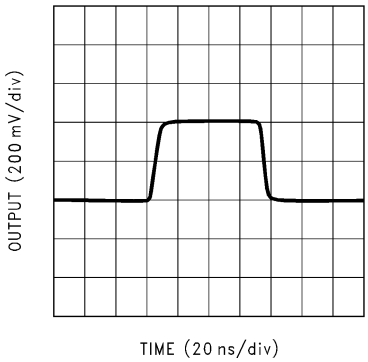


Figure 33. Small Signal Pulse Response A_V = +2, V_S = ±15V

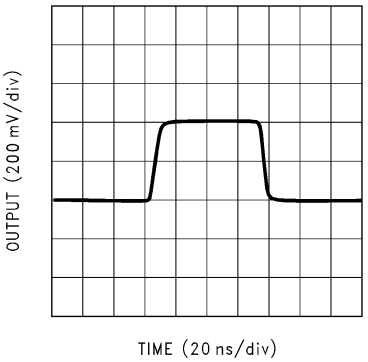


Figure 34. Small Signal Pulse Response A_V = +2, V_S = ±5V

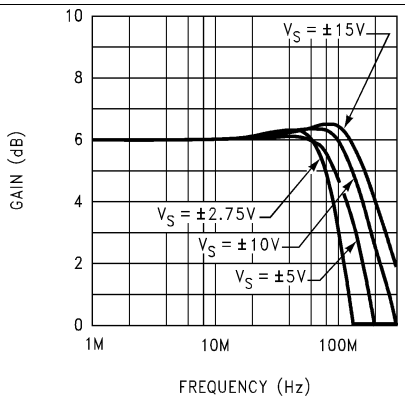


Figure 35. Closed Loop Frequency Response vs. Supply Voltage (A_V = +2)

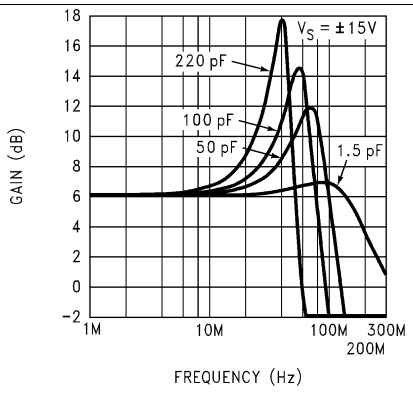


Figure 36. Closed Loop Frequency Response vs. Capacitive Load (A_V = +2)

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

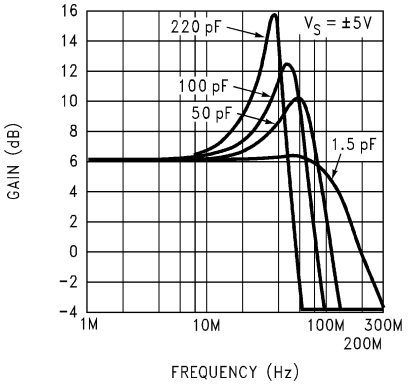


Figure 37. Closed Loop Frequency Response vs. Capacitive Load (A_V = +2)

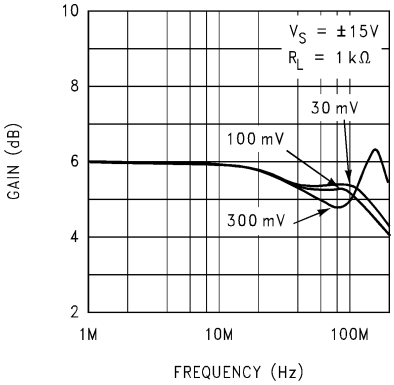


Figure 38. Closed Loop Frequency Response vs. Input Signal Level (A_V = +2)

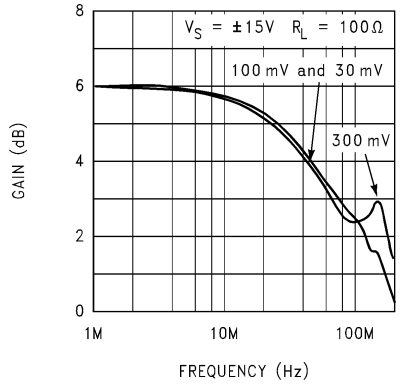


Figure 39. Closed Loop Frequency Response vs. Input Signal Level (A_V = +2)

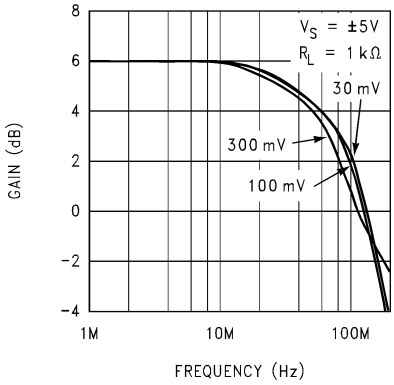


Figure 40. Closed Loop Frequency Response vs. Input Signal Level (A_V = +2)

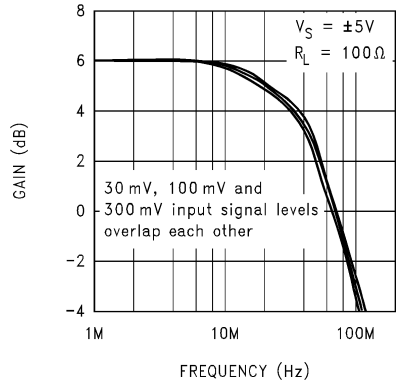


Figure 41. Closed Loop Frequency Response vs. Input Signal Level (A_V = +2)

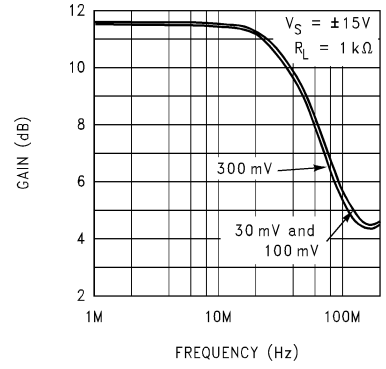


Figure 42. Closed Loop Frequency Response vs. Input Signal Level (A_V = +4)

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

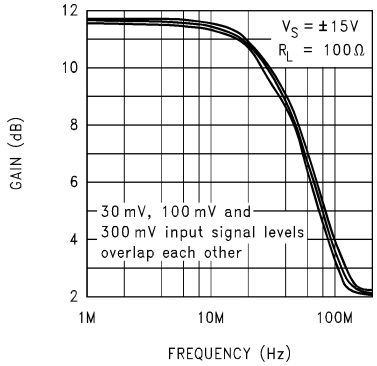


Figure 43. Closed Loop Frequency Response vs. Input Signal Level (A_V = +4)

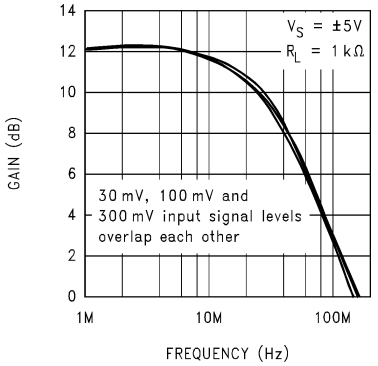


Figure 44. Closed Loop Frequency Response vs. Input Signal Level (A_V = +4)

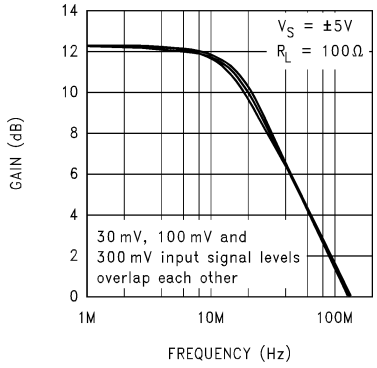


Figure 45. Closed Loop Frequency Response vs. Input Signal Level (A_V = +4)

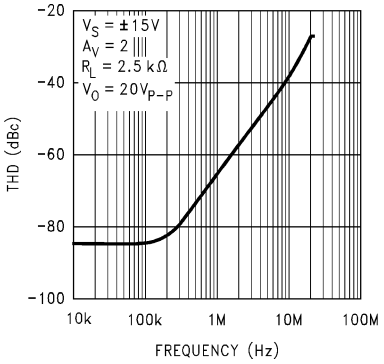


Figure 46. Total Harmonic Distortion vs. Frequency (1)

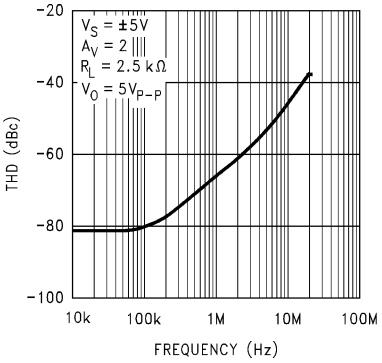


Figure 47. Total Harmonic Distortion vs. Frequency (1)

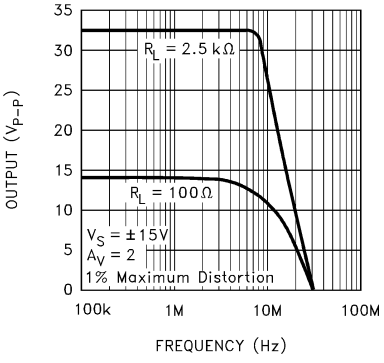


Figure 48. Undistorted Output Swing vs. Frequency

(1) The THD measurement at low frequency is limited by the test instrument.
(1) The THD measurement at low frequency is limited by the test instrument.

Typical Performance Characteristics (continued)

unless otherwise noted, T_A= 25°C

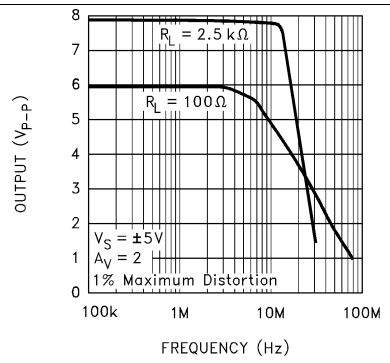


Figure 49. Undistorted Output Swing vs. Frequency

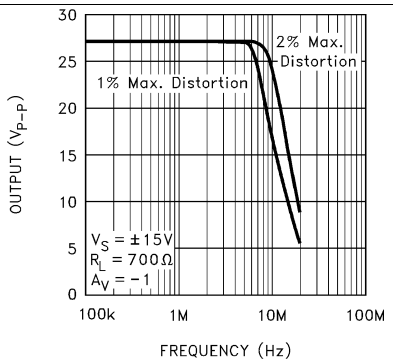


Figure 50. Undistorted Output Swing vs. Frequency

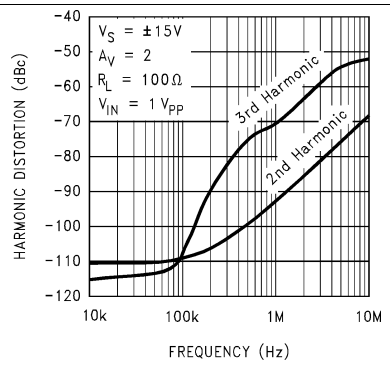


Figure 51. Harmonic Distortion vs. Frequency (1)

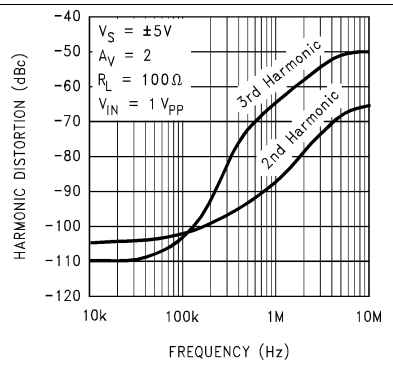


Figure 52. Harmonic Distortion vs. Frequency (1)

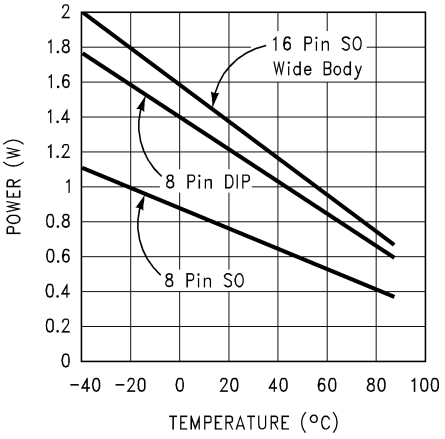


Figure 53. Maximum Power Dissipation vs. Ambient Temperature

(1) The THD measurement at low frequency is limited by the test instrument.
(1) The THD measurement at low frequency is limited by the test instrument.

7 Application and Implementation

7.1 Application Information

The LM7171 is a very high speed, voltage feedback amplifier. It consumes only 6.5 mA supply current while providing a unity-gain bandwidth of 200 MHz and a slew rate of 4100V/μs. It also has other great features such as low differential gain and phase and high output current.

The LM7171 is a true voltage feedback amplifier. Unlike current feedback amplifiers (CFAs) with a low inverting input impedance and a high non-inverting input impedance, both inputs of voltage feedback amplifiers (VFAs) have high impedance nodes. The low impedance inverting input in CFAs and a feedback capacitor create an additional pole that will lead to instability. As a result, CFAs cannot be used in traditional op amp circuits such as photodiode amplifiers, I-to-V converters and integrators where a feedback capacitor is required.

7.2 Circuit Operation

The class AB input stage in LM7171 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the LM7171 Simplified Schematic, Q1 through Q4 form the equivalent of the current feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

7.3 Slew Rate Characteristic

The slew rate of LM7171 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor R_E. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations. A curve of slew rate versus input voltage level is provided in *Typical Performance Characteristics*

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external resistor such as 1 kΩ in series with the input of LM7171, the bandwidth is reduced to help lower the overshoot.

7.4 Slew Rate Limitation

If the amplifier's input signal has too large of an amplitude at too high of a frequency, the amplifier is said to be slew rate limited; this can cause ringing in time domain and peaking in frequency domain at the output of the amplifier.

In *Typical Performance Characteristics*, there are several curves of A_V = +2 and A_V = +4 versus input signal levels. For the A_V = +4 curves, no peaking is present and the LM7171 responds identically to the different input signal levels of 30 mV, 100 mV and 300 mV.

For the A_V = +2 curves, with slight peaking occurs. This peaking at high frequency (>100 MHz) is caused by a large input signal at high enough frequency that exceeds the amplifier's slew rate. The peaking in frequency response does not limit the pulse response in time domain, and the LM7171 is stable with noise gain of ≥+2.

7.5 Compensation For Input Capacitance

The combination of an amplifier's input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value

$$C_F > (R_G \times C_{IN})/R_F \quad (1)$$

can be used to cancel that pole. For LM7171, a feedback capacitor of 2 pF is recommended. Figure 54 illustrates the compensation circuit.

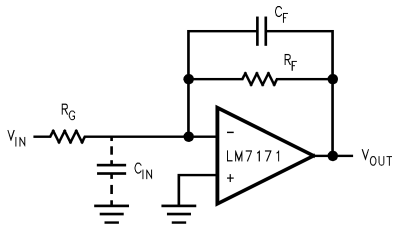


Figure 54. Compensating for Input Capacitance

7.6 Application Circuit

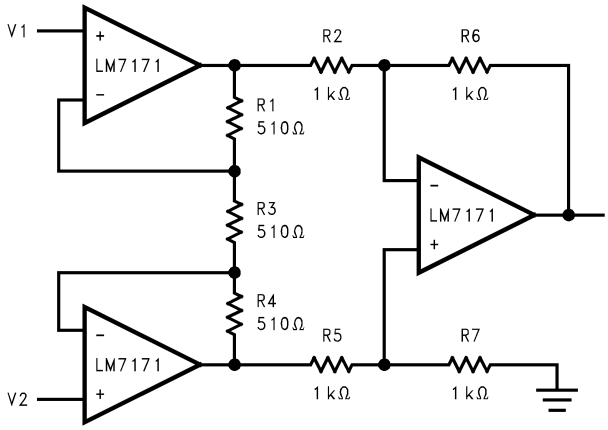


Figure 55. Fast Instrumentation Amplifier

$$V_{IN} = V_2 - V_1$$

if R6 = R2, R7 = R5, and R1 = R4

$$\frac{V_{OUT}}{V_{IN}} = \frac{R6}{R2}\left(1 + 2\frac{R1}{R3}\right) = 3$$

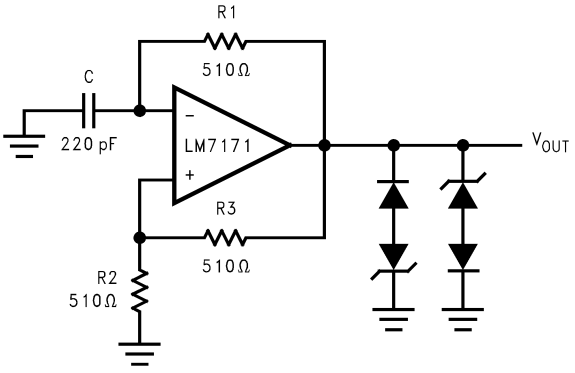


Figure 56. Multivibrator

Application Circuit (continued)

$$f = \frac{1}{2\left(R1\,C\ln\left(1 + 2\frac{R2}{R3}\right)\right)}$$

$f = 4$ MHz

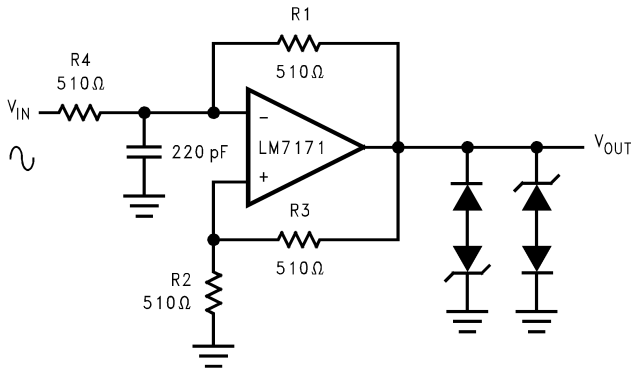


Figure 57. Pulse Width Modulator

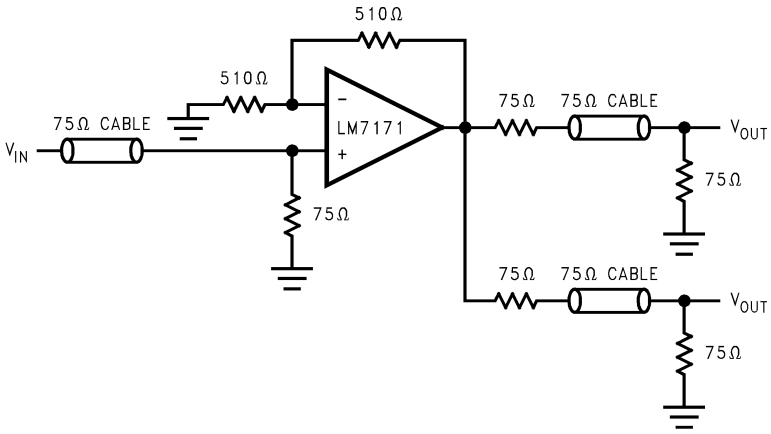


Figure 58. Video Line Driver

8 Power Supply Recommendations

8.1 Power Supply Bypassing

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Both positive and negative power supplies should be bypassed individually by placing 0.01 µF ceramic capacitors directly to power supply pins and 2.2 µF tantalum capacitors close to the power supply pins.

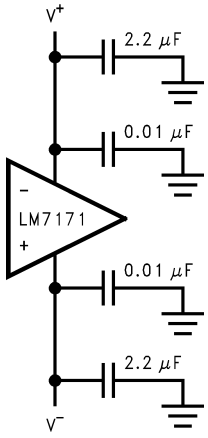


Figure 59. Power Supply Bypassing

8.2 Termination

In high frequency applications, reflections occur if signals are not properly terminated. Figure 60 shows a properly terminated signal while Figure 61 shows an improperly terminated signal.

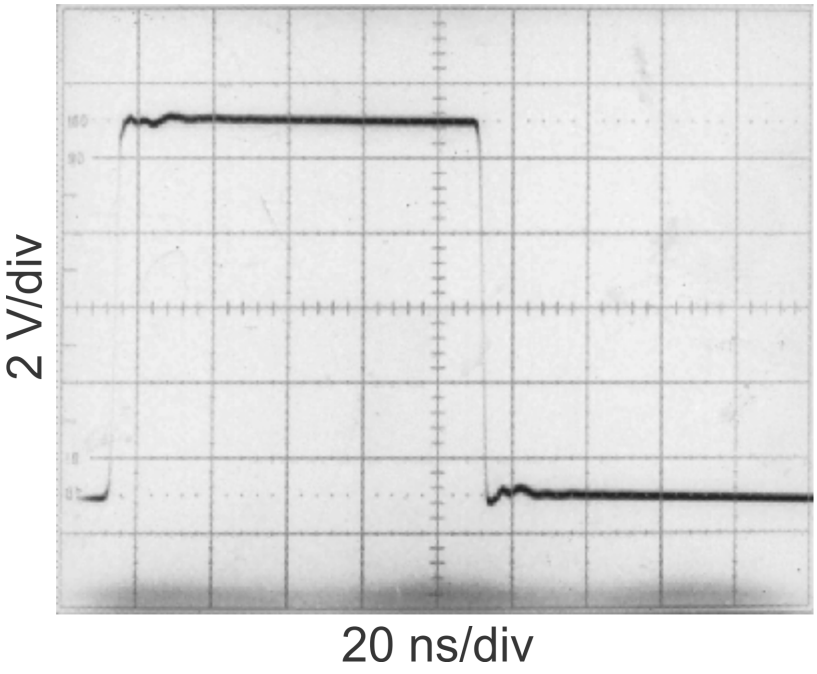


Figure 60. Properly Terminated Signal

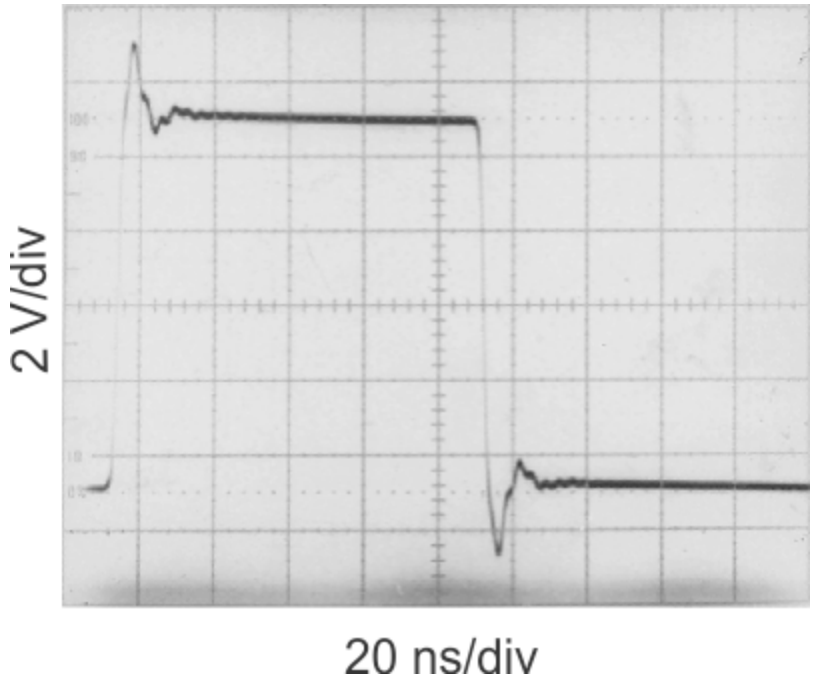


Figure 61. Improperly Terminated Signal

To minimize reflection, coaxial cable with matching characteristic impedance to the signal source should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75Ω characteristic impedance, and RG58 has 50Ω characteristic impedance.

8.3 Driving Capacitive Loads

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown in Figure 62. The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For LM7171, a 50Ω isolation resistor is recommended for initial evaluation. Figure 63 shows the LM7171 driving a 150 pF load with the 50Ω isolation resistor.

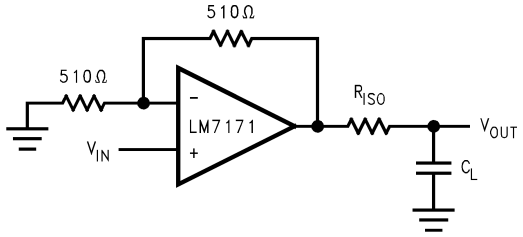


Figure 62. Isolation Resistor Used to Drive Capacitive Load

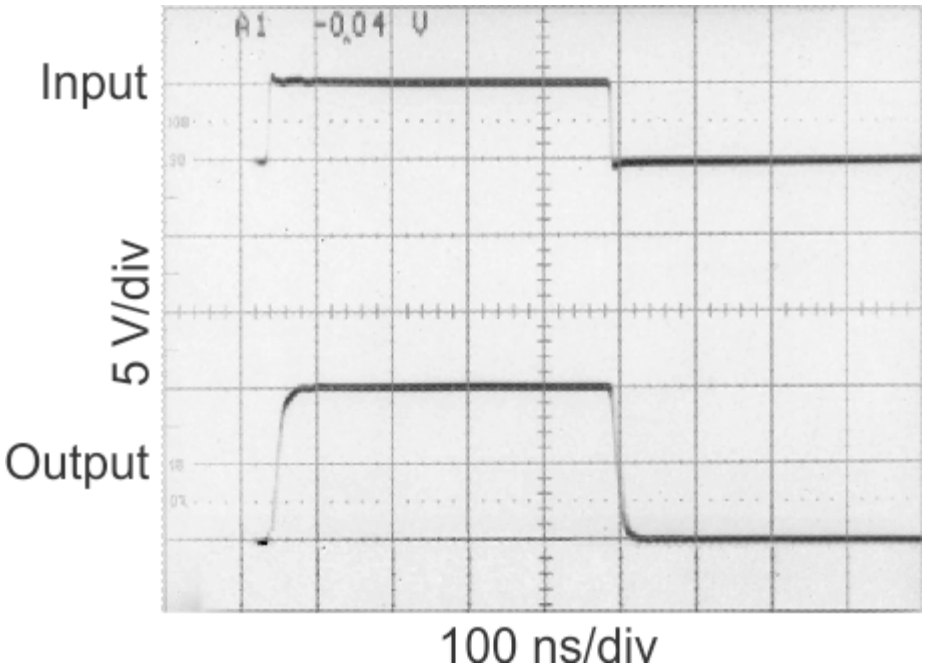


Figure 63. The LM7171 Driving a 150 pF Load with a 50 Ω Isolation Resistor

8.4 Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$$

where

- PD is the power dissipation in a device
- $T_{J(max)}$ is the maximum junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the thermal resistance of a particular package
- (2)

For example, for the LM7171 in a SOIC-8 package, the maximum power dissipation at 25°C ambient temperature is 730 mW.

Thermal resistance, $R_{\theta JA}$, depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher $R_{\theta JA}$ becomes. The 8-pin DIP package has a lower thermal resistance (108°C/W) than that of 8-pin SOIC (172°C/W). Therefore, for higher dissipation capability, use an 8-pin DIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L$$

where

- P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; it is not the power dissipated by the load.

Furthermore,

- $P_Q$is the supply current × total supply voltage with no load
- P_L is the output current × (voltage difference between supply voltage and output voltage of the same side of supply voltage) (3)

For example, the total power dissipated by the LM7171 with V_S = ±15V and output voltage of 10V into 1 kΩ is

$$P_D = P_Q + P_L \quad (4)$$

$$= (6.5\ mA) \times (30V) + (10\ mA) \times (15V - 10V) \quad (5)$$

$$= 195\ mW + 50\ mW \quad (6)$$

$$= 245\ mW \quad (7)$$

9 Layout

9.1 Layout Guidelines

9.1.1 Printed Circuit Board and High Speed Op Amps

There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy to have excessive ringing, oscillation and other degraded AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space needs to be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect high frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

9.1.2 Using Probes

Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance and low input capacitance. However, the probe ground leads provide a long ground loop that will produce errors in measurement. Instead, the probes can be grounded directly by removing the ground leads and probe jackets and using scope probe jacks.

9.1.3 Component Selection and Feedback Resistor

It is important in high speed applications to keep all component leads short. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For LM7171, a feedback resistor of 510Ω gives optimal performance.

10 Device and Documentation Support

10.1 Trademarks

VIP is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM7171AIM	NRND	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LM71 71AIM	
LM7171AIM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM71 71AIM	Samples
LM7171AIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM71 71AIM	Samples
LM7171BIM	NRND	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LM71 71BIM	
LM7171BIM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM71 71BIM	Samples
LM7171BIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM71 71BIM	Samples
LM7171BIN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM7171 BIN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

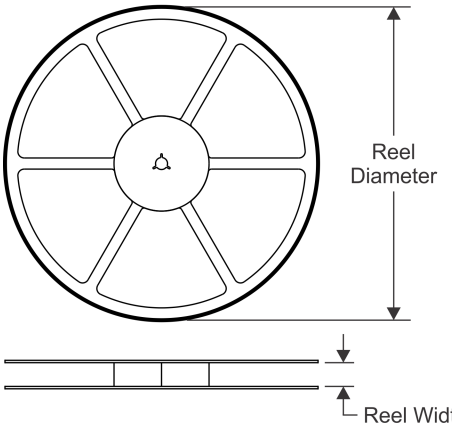
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

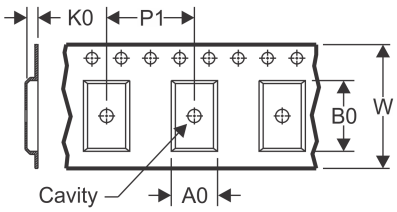
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

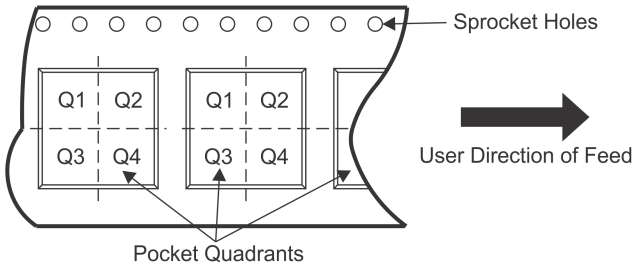


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

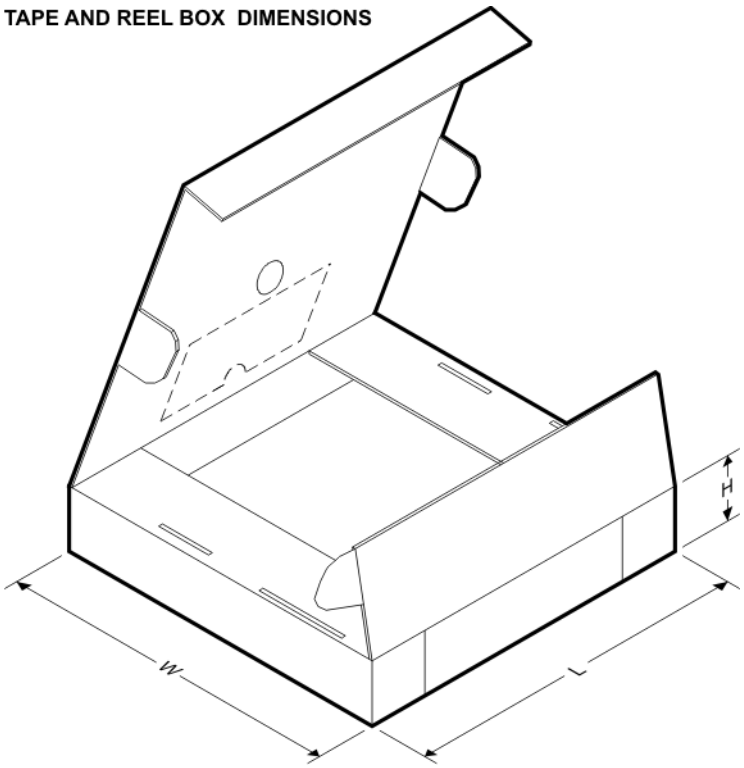
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7171AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM7171BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

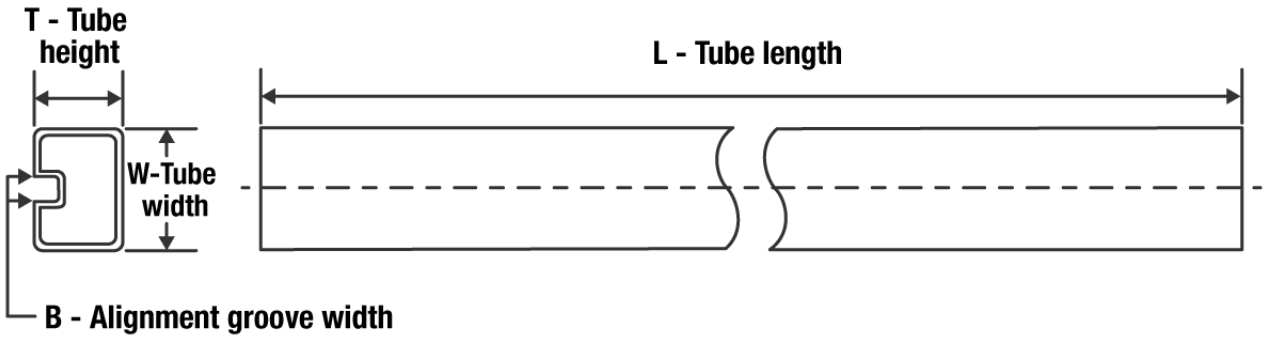
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

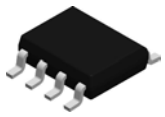
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7171AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM7171BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM7171AIM	D	SOIC	8	95	495	8	4064	3.05
LM7171AIM	D	SOIC	8	95	495	8	4064	3.05
LM7171AIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM7171BIM	D	SOIC	8	95	495	8	4064	3.05
LM7171BIM	D	SOIC	8	95	495	8	4064	3.05
LM7171BIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM7171BIN/NOPB	P	PDIP	8	40	502	14	11938	4.32

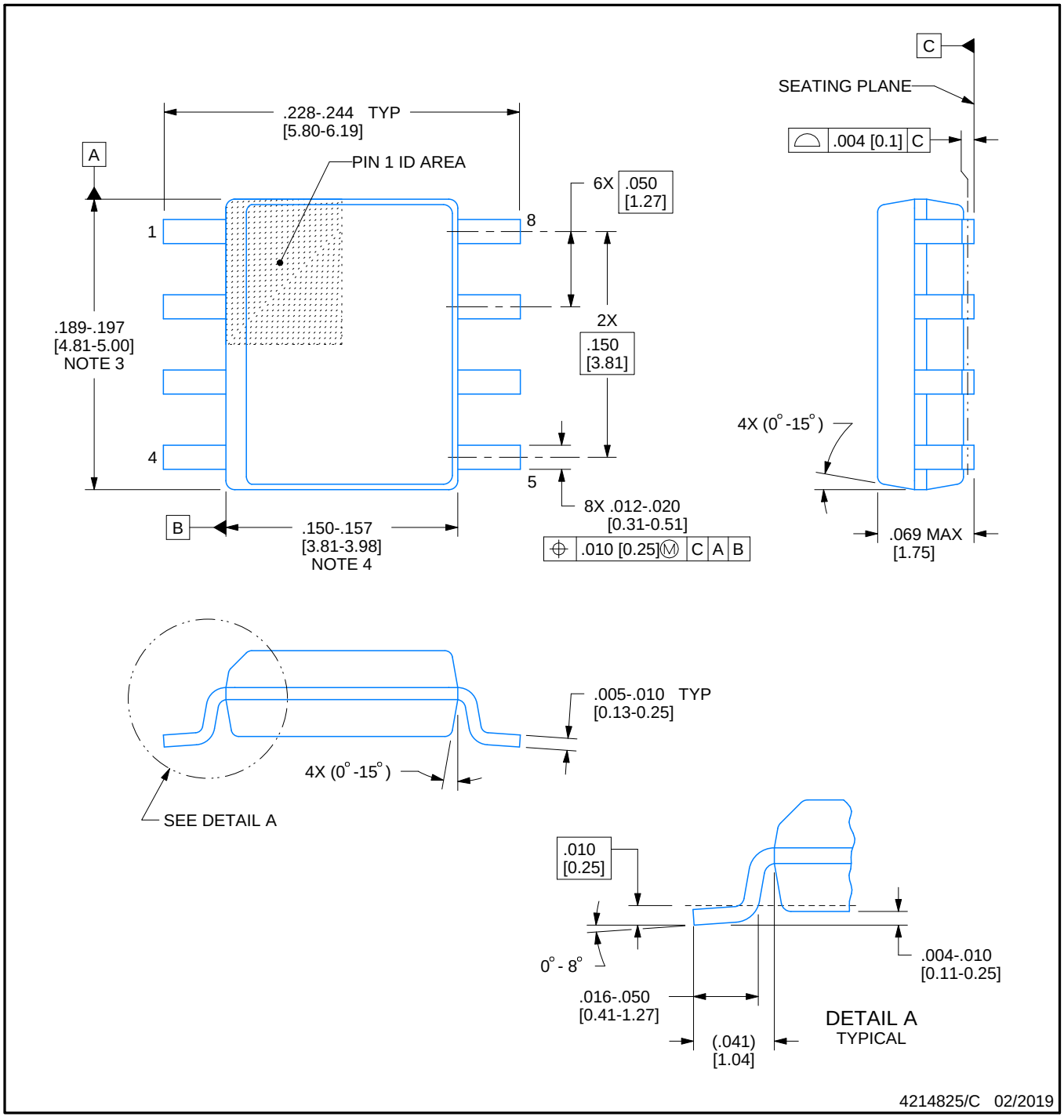


PACKAGE OUTLINE

D0008A

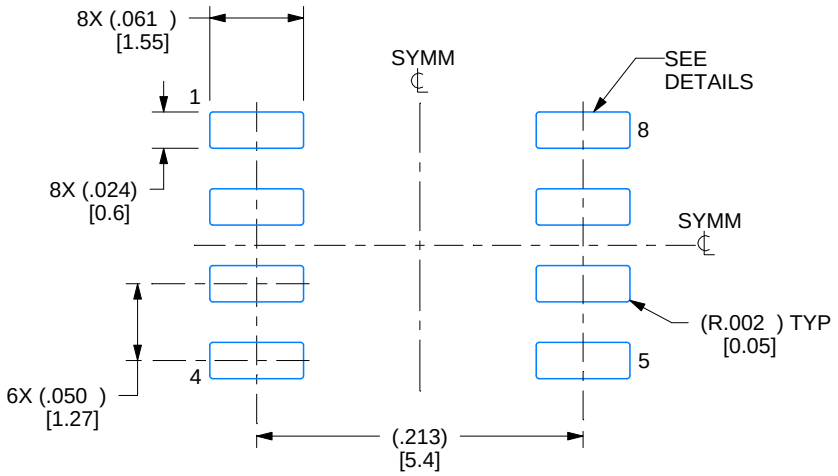
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

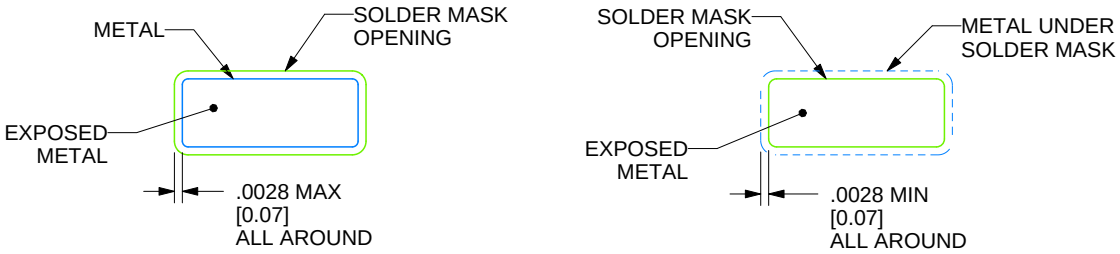


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

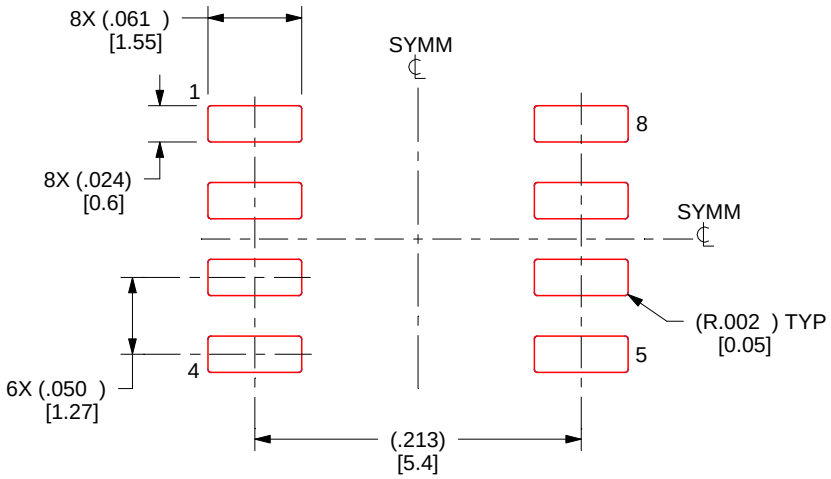
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



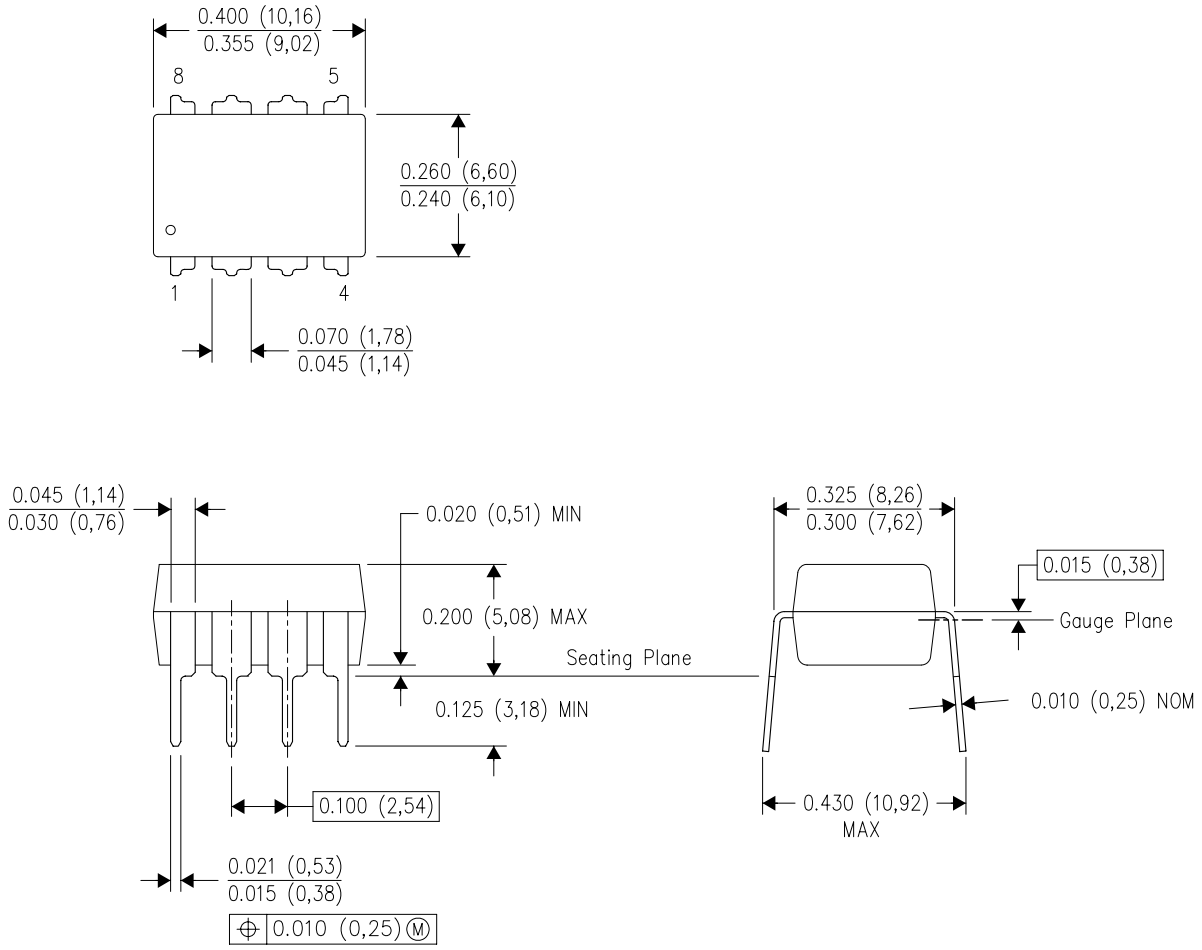
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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