LM7372 High Speed, High Output Current, Dual Operational Amplifier

1 Features

- −80 dBc Highest Harmonic Distortion @1 MHz, $2V_{PP}$
- Very High Slew Rate: 3000 V/µs
- Wide Gain Bandwidth Product: 120 MHz
- −3 dB Frequency @ A_V = +2: 200 MHz
- Low Supply Current: 13 mA (both amplifiers)
- High Open Loop Gain: 85 dB
- High Output Current: 150 mA
- Differential Gain and Phase: 0.01%, 0.02°

2 Applications

- HDSL and ADSL Drivers
- Multimedia Broadcast Systems
- Professional Video Cameras
- CATV/Fiber Optics Signal Processing
- Pulse Amplifiers and Peak Detectors
- HDTV Amplifiers

3 Description

The LM7372 is a high speed dual voltage feedback amplifier with the slewing characteristic of current feedback amplifiers. However, it can be used in all traditional voltage feedback amplifier configurations.

The LM7372 is stable for gains as low as +2 or −1. It provides a very high slew rate at 3000 V/µs and a wide gain bandwidth product of 120 MHz, while consuming only 6.5 mA/per amplifier of supply current. It is ideal for video and high speed signal processing applications such as xDSL and pulse amplifiers. With 150 mA output current, the LM7372 can be used for video distribution, as a transformer driver or as a laser diode driver.

Operation on ±15 V power supplies allows for large signal swings and provides greater dynamic range and signal-to-noise ratio. The LM7372 offers high SFDR and low THD, ideal for ADC/DAC systems. In addition, the LM7372 is specified for ±5 V operation for portable applications.

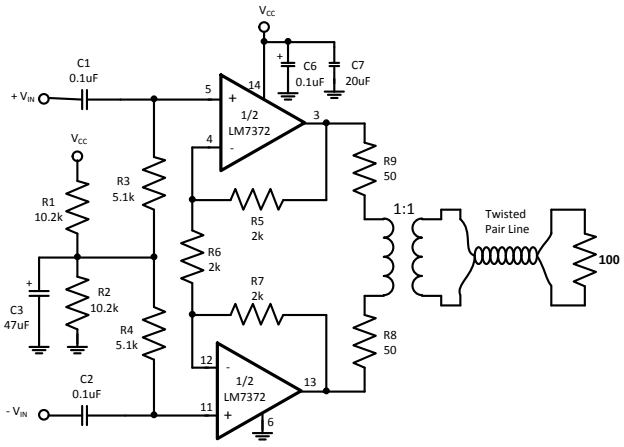
The LM7372 is built on TI's Advance VIP™ III (Vertically integrated PNP) complementary bipolar process.

Device Information(1)

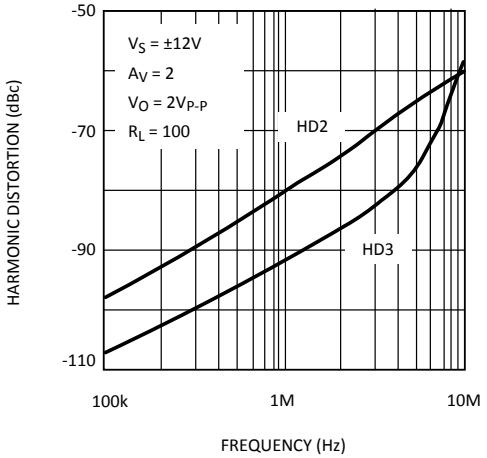
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM7372	DDA (8)	4.90 mm × 3.91 mm
LM7372	D (16)	9.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Single Supply Application (16-Pin SOIC)



Harmonic Distortion vs Frequency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2013) to Revision F — **Page**

- Changed data sheet structure and organization. Added, updated, or renamed the following sections: Device Information Table, Pin Configuration and Functions, Application and Implementation; Device and Documentation Support; Mechanical, Packaging, and Ordering Information ... 1
- Changed "Junction Temperature Range" to "Operating Temperature Range" ... 4
- Deleted T_J = 25°C for Electrical Characteristics tables ... 5

Changes from Revision D (March 2013) to Revision E — **Page**

- Changed layout of National Data Sheet to TI format ... 21

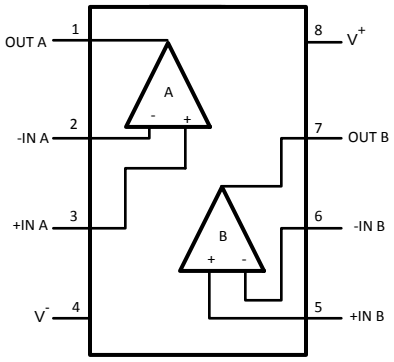
5 Pin Configuration and Functions

NOTE

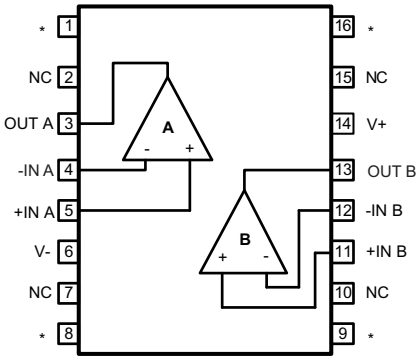
For SO PowerPAD package the exposed pad should be tied either to V^- or left electrically floating. Die attach material is conductive and is internally tied to V^-.

*** Heatsink Pins.** (1)

Package DDA
8-Pin SO PowerPAD
Top View



Package D
16-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NUMBER			
	DDA	D		
*	—	1,8,9,16	—	Heatsink Pin
-IN A	2	4	I	ChA Inverting Input
+IN A	3	5	I	ChA Non-inverting Input
-IN B	6	12	I	ChB Inverting Input
+IN B	5	11	I	ChB Non-inverting Input
NC	—	2, 7, 10, 15	—	No Connection
OUT A	1	3	O	Output A
OUT B	7	13	O	Output B
V^-	4	6	I	Negative Supply
V^+	8	14	I	Positive Supply

(1) The maximum power dissipation is a function of $T_{(JMAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{(JMAX)} – T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board. The value for $R_{\theta JA}$ is 106°C/W for the 16-Pin SOIC package. With a total area of 4sq. in of 1oz CU connected to pins 1,6,8,9 & 16, $R_{\theta JA}$ for the 16-Pin SOIC is decreased to 70°C/W. 8-Pin SO PowerPAD package $R_{\theta JA}$ is with 2 in^2 heatsink (top and bottom layer each) and 1 oz. copper (see Table 2 and *Application and Implementation*)

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
Suppy Voltage (V^+–V^-)			36	V
Differential Input Voltage (V_S = ±15V)			±10	V
Output Short Circuit to Ground (2)			Continuous	
Soldering Information	Infrared or Convection Reflow (20 sec.)		235	°C
	Wave Soldering Lead Temperature (10 sec.)		260	°C
Input Voltage			V^- to V^+	V
Maximum Junction Temperature (4)			150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation is a function of $T_{(JMAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{(JMAX)} – T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board. The value for $R_{\theta JA}$ is 106°C/W for the 16-Pin SOIC package. With a total area of 4sq. in of 1oz CU connected to pins 1,6,8,9 & 16, $R_{\theta JA}$ for the 16-Pin SOIC is decreased to 70°C/W. 8-Pin SO PowerPAD package $R_{\theta JA}$ is with 2 in^2 heatsink (top and bottom layer each) and 1 oz. copper (see Table 2 and *Application and Implementation*)

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge (1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2)		1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (3)		200	

(1) For testing purposes, ESD was applied using human body model, 1.5kΩ in series with 100pF. Machine model, 0Ω in series with 200pF.
(2) JEDEC document JEP155 states that 1500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 200-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions (1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage	9	36	V
Operating Temperature Range	−40	85	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

6.4 Thermal Information

THERMAL METRIC (1)		DDA	D	UNIT
		8 PINS (2)	16 PINS (2)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106	47	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{(JMAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{(JMAX)} – T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board. The value for $R_{\theta JA}$ is 106°C/W for the 16-Pin SOIC package. With a total area of 4sq. in of 1oz CU connected to pins 1,6,8,9 & 16, $R_{\theta JA}$ for the 16-Pin SOIC is decreased to 70°C/W. 8-Pin SO PowerPAD package $R_{\theta JA}$ is with 2 in^2 heatsink (top and bottom layer each) and 1 oz. copper (see Table 2 and *Application and Implementation*)

6.5 ±15V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for V_{CM} = 0V and R_L = 1kΩ. **Boldface** apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage			2.0	8.0 **10.0**	mV
TC V_{OS}	Input Offset Voltage Average Drift			12		µV/°C
I_B	Input Bias Current			2.7	10 **12**	µA
I_{OS}	Input Offset Current			0.1	4.0 **6.0**	µA
R_{IN}	Input Resistance	Common Mode		40		MΩ
		Differential Mode		3.3		MΩ
R_O	Open Loop Output Resistance			15		Ω
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V	75 **70**	93		dB
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V	75 **70**	90		dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 60dB		±13		V
A_V	Large Signal Voltage Gain(3)	R_L = 1kΩ	75 **70**	85		dB
		R_L = 100Ω	70 **66**	81		dB
V_O	Output Swing	R_L = 1kΩ	13 **12.7**	13.4		V
			−13 **−12.7**	−13.3		V
		I_{OUT} = − 150mA	11.8 **11.4**	12.4		V
		I_{OUT} = 150mA	−11.2 **−10.8**	−11.9		V
I_{SC}	Output Short Circuit Current	Sourcing		260		mA
		Sinking		250		mA
I_S	Supply Current (both Amps)			13	17 **19**	mA

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametic norm.
(3) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ± 10V. For V_S = ±5V, V_{OUT} = ±2V

6.6 ±15V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for V_{CM} = 0V and R_L = 1kΩ. **Boldface** apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
SR	Slew Rate(3)	A_V = +2, V_{IN} 13V_{P-P}		3000		V/µs
		A_V = +2, V_{IN} 10V_{P-P}		2000		
	Unity Bandwidth Product			120		MHz
	−3dB Frequency	A_V = +2		220		MHz
φ_m	Phase Margin	A_{VOL} = 6dB		70		deg
t_S	Settling Time (0.1%)	A_V = −1, A_O = ±5V, R_L = 500Ω		50		ns
t_P	Propagation Delay	A_V = −2, V_{IN} = ±5V, R_L = 500Ω		6.0		ns
A_D	Differential Gain(4)			0.01%		
φ_D	Differential Phase(4)			0.02		deg
hd2	Second Harmonic Distortion F_{IN} = 1MHz, A_V = +2	V_{OUT} = 2V_{P-P}, R_L = 100Ω		−80		dBc
		V_{OUT} = 16.8V_{P-P}, R_L = 100Ω		−73		dBc
hd3	Third Harmonic Distortion F_{IN} = 1MHz, A_V = +2	V_{OUT} = 2V_{P-P}, R_L = 100Ω		−91		dBc
		V_{OUT} = 16.8V_{P-P}, R_L = 100Ω		−67		dBc
IMD	Intermodulation Distortion	Fin 1 = 75kHz, Fin 2 = 85kHz V_{OUT} = 16.8V_{P-P}, R_L = 100Ω		−87		dBc
e_n	Input-Referred Voltage Noise	f = 10kHz		14		nV/√Hz
i_n	Input-Referred Current Noise	f = 10kHz		1.5		pA/√Hz

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametic norm.
(3) Slew Rate is the average of the rising and falling slew rates.
(4) Differential gain and phase are measured with A_V = +2, V_{IN} = 1V_{PP} at 3.58 MHz and output is 150Ω terminated.

6.7 ±5V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for V_{CM} = 0V and R_L = 1kΩ. **Boldface** apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage			2.2	8.0 **10.0**	mV
TC V_{OS}	Input Offset Voltage Average Drift			12		µV/°C
I_B	Input Bias Current			3.3	10 **12**	µA
I_{OS}	Input Offset Current			0.1	4 **6**	µA
R_{IN}	Input Resistance	Common Mode		40		MΩ
		Differential Mode		3.3		MΩ
R_O	Open Loop Output Resistance			15		Ω
CMRR	Common Mode Rejection Ratio	V_{CM} = ±2.5V	70 **65**	90		dB
PSRR	Power Supply Rejection Ratio	V_S = ±15V to ±5V	75 **70**	90		dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 60dB		±3		V
A_V	Large Signal Voltage Gain(3)	R_L = 1kΩ	70 **65**	78		dB
		R_L = 100Ω	64 **60**	72		dB

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametic norm.
(3) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For V_S = ±15V, V_{OUT} = ±10V. For V_S = ±5V, V_{OUT} = ±2V

±5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V_{CM} = 0V and R_L = 1kΩ. **Boldface** apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_O	Output Swing	R_L = 1kΩ	3.2 **3.0**	3.4		V
			−3.2 **−3.0**	−3.4		V
		I_{OUT} = − 80mA	2.5 **2.2**	2.8		V
		I_{OUT} = 80mA	−2.5 **−2.2**	−2.7		V
I_{SC}	Output Short Circuit Current	Sourcing		150		mA
		Sinking		150		mA
I_S	Supply Current (both Amps)			12.4	16 **18**	mA

6.8 ±5V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for V_{CM} = 0V and R_L = 1kΩ. **Boldface** apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
SR	Slew Rate(3)	A_V = +2, V_{IN} $3V_{P-P}$		700		V/µs
	Unity Bandwidth Product			100		MHz
	−3dB Frequency	A_V = +2		125		MHz
φ_m	Phase Margin			70		deg
t_S	Settling Time (0.1%)	A_V = −1, V_O = ±1V, R_L = 500Ω		70		ns
t_P	Propagation Delay	A_V = +2, V_{IN} = ±1V, R_L = 500Ω		7		ns
A_D	Differential Gain(4)			0.02%		
φ_D	Differential Phase(4)			0.03		deg
hd2	Second Harmonic Distortion F_{IN} = 1MHz, A_V = +2	V_{OUT} = $2V_{P-P}$, R_L = 100Ω		−84		dBc
hd3	Third Harmonic Distortion F_{IN} = 1MHz, A_V = +2	V_{OUT} = $2V_{P-P}$, R_L = 100Ω		−94		dBc
e_n	Input-Referred Voltage Noise	f = 10kHz		14		nV/√Hz
i_n	Input-Referred Current Noise	f = 10kHz		1.8		pA/√Hz

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametic norm.
(3) Slew Rate is the average of the rising and falling slew rates.
(4) Differential gain and phase are measured with A_V = +2, V_{IN} = $1V_{PP}$ at 3.58 MHz and output is 150Ω terminated.

6.9 Typical Performance Characteristics

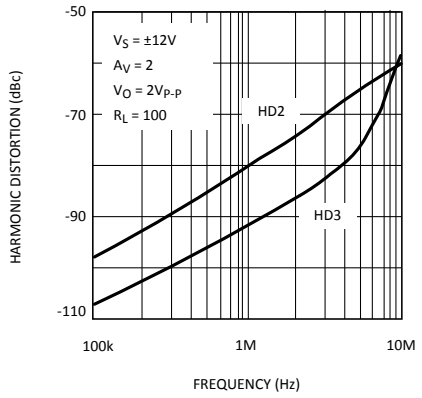


Figure 1. Harmonic Distortion vs Frequency

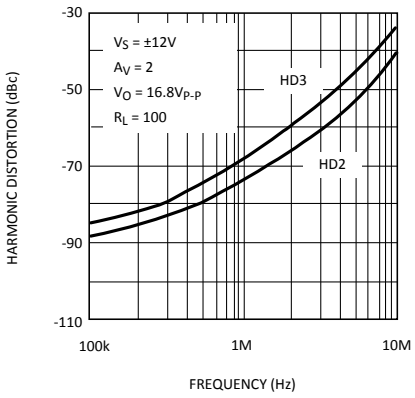


Figure 2. Harmonic Distortion vs Frequency

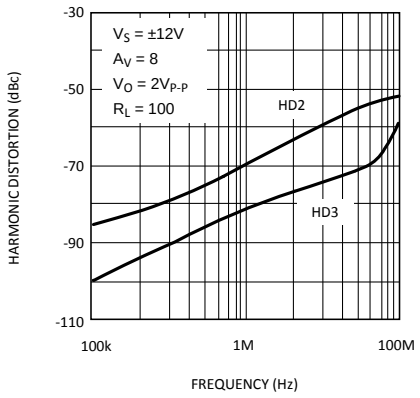


Figure 3. Harmonic Distortion vs Frequency

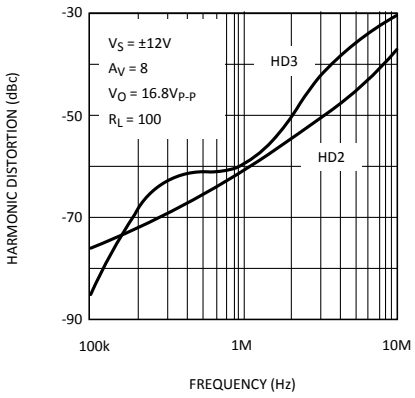


Figure 4. Harmonic Distortion vs Frequency

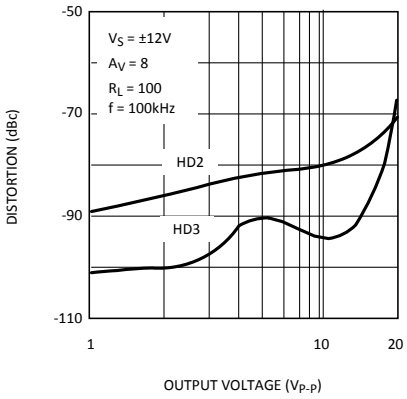


Figure 5. Harmonic Distortion vs

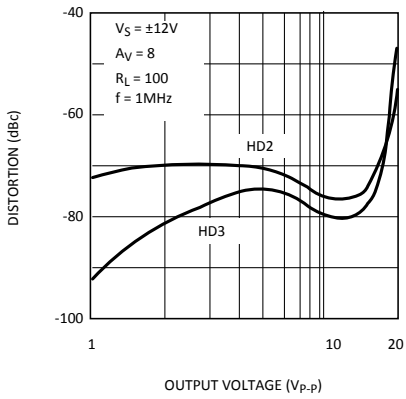


Figure 6. Harmonic Distortion vs Output Level

Typical Performance Characteristics (continued)

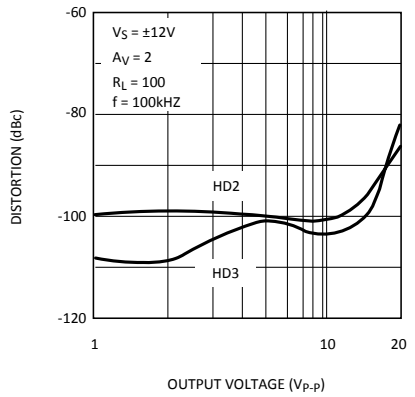


Figure 7. Harmonic Distortion vs Output Level

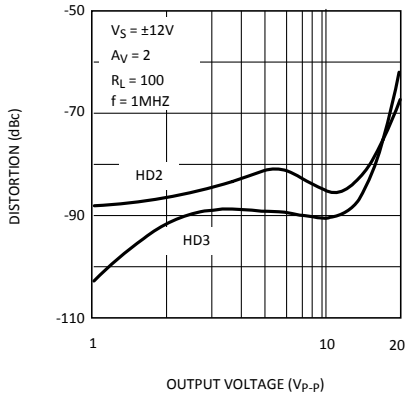


Figure 8. Harmonic Distortion vs Output Level

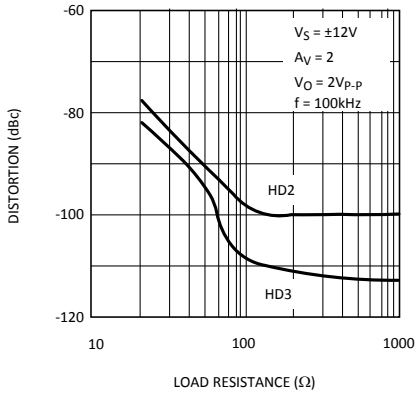


Figure 9. Harmonic Distortion vs Load Resistance

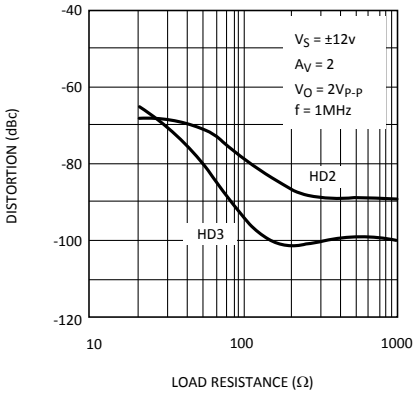


Figure 10. Harmonic Distortion vs Load Resistance

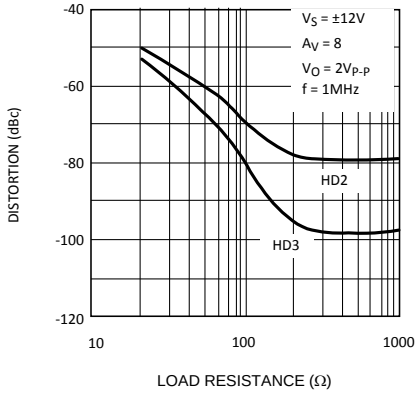


Figure 11. Harmonic Distortion vs Load Resistance

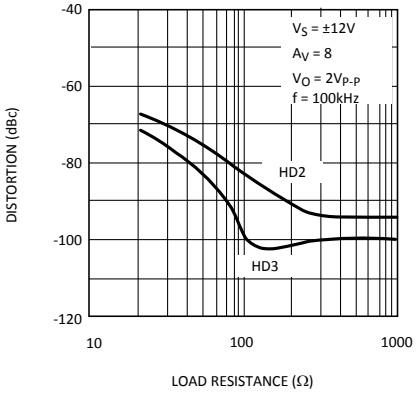


Figure 12. Harmonic Distortion vs Load Resistance

Typical Performance Characteristics (continued)

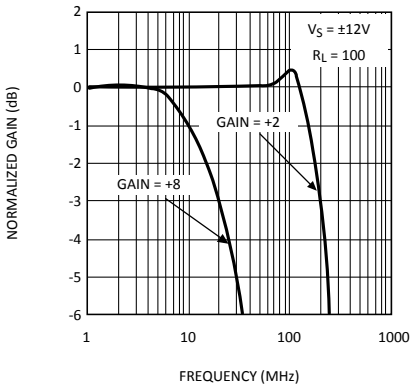


Figure 13. Frequency Response

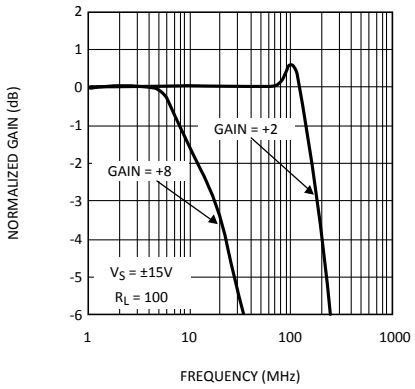


Figure 14. Frequency Response

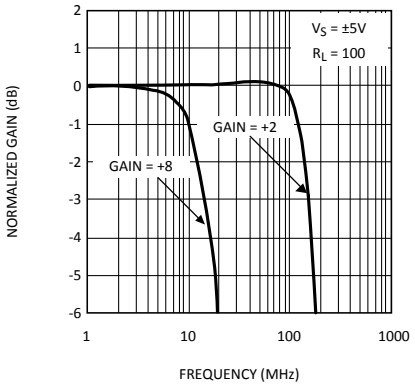


Figure 15. Frequency Response

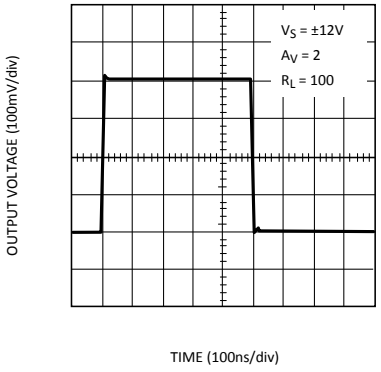


Figure 16. Small Signal Pulse Response

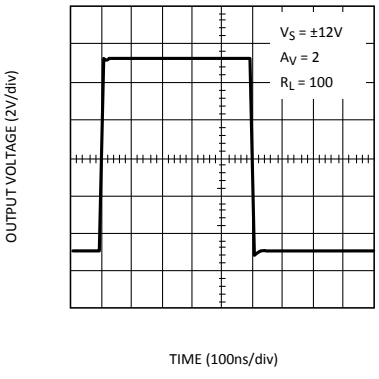


Figure 17. Large Signal Pulse Response

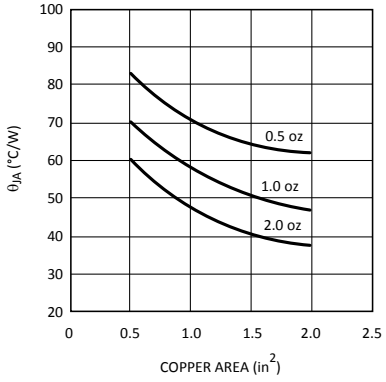


Figure 18. Thermal Performance of 8ld-SO PowerPAD

Typical Performance Characteristics (continued)

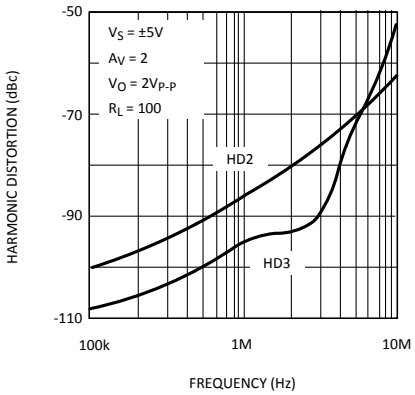


Figure 19. Harmonic Distortion vs Frequency

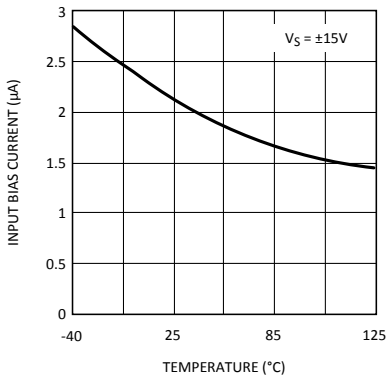


Figure 20. Input Bias Current (µA) vs Temperature

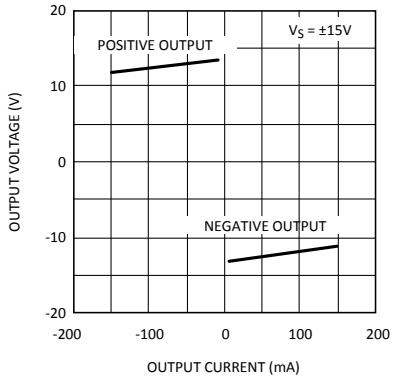


Figure 21. Output Voltage vs Output Current

7 Detailed Description

7.1 Functional Block Diagram

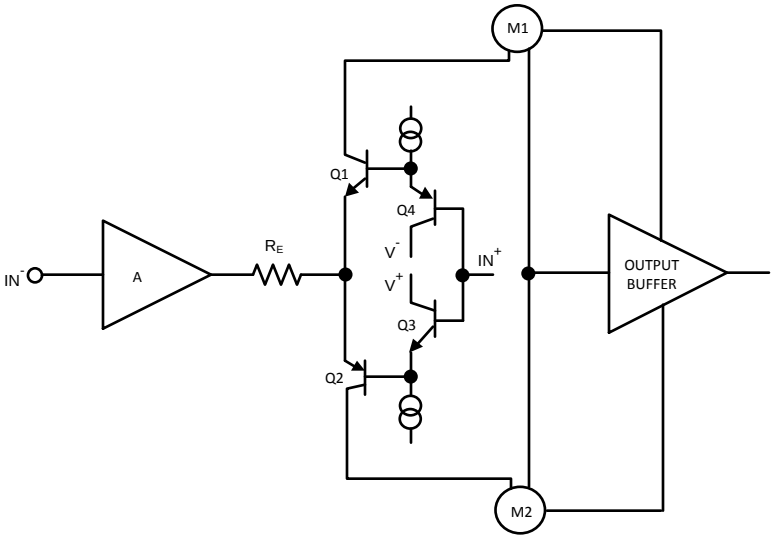


Figure 22. Simplified Schematic Diagram

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM7372 is a high speed dual operational amplifier with a very high slew rate and very low distortion. Like many other op amps, it is used in conventional voltage feedback amplifier applications, and has a class AB output stage in order to deliver high currents to low impedance loads. However, it draws a low quiescent supply current in most situations since the supply current increases when necessary to keep up with large output swing and/or high frequency (see *High Frequency/Large Signal Swing Considerations*). For most op amps in typical applications, this topology means that internal power dissipation is rarely an issue, even with the trend to smaller surface mount packages. However, TI has designed the LM7372 for applications where there are significant levels of power dissipation, and a way to effectively remove the internal heat generated by this power dissipation is needed in order to maintain the semiconductor junction temperature at acceptable levels. This is particularly important in environments with elevated ambient temperatures.

8.2 Typical Application

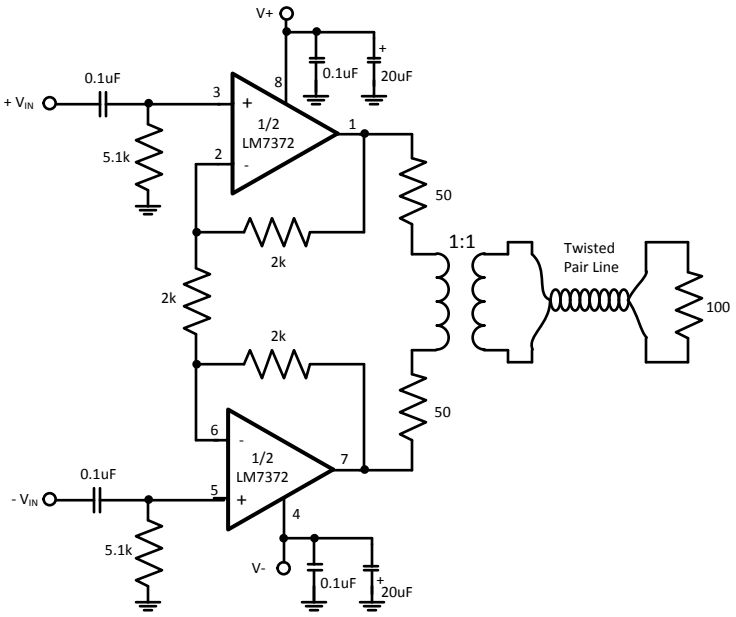


Figure 23. Split Supply Application (SO PowerPAD)

Typical Application (continued)

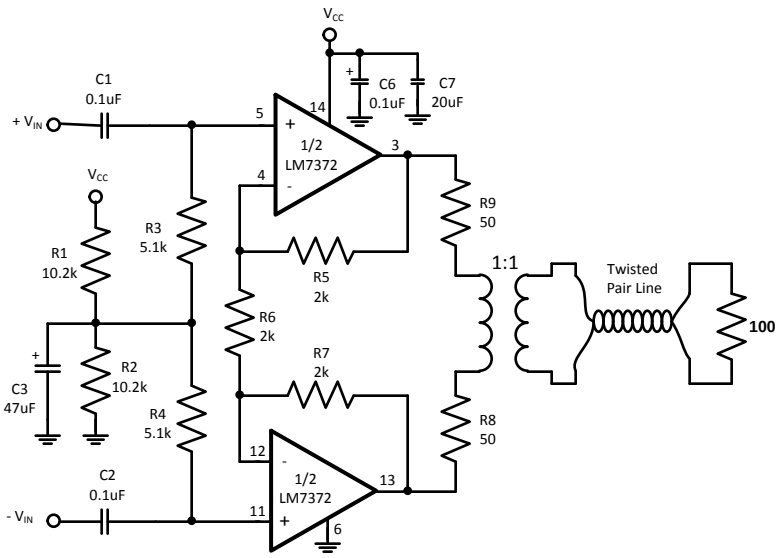


Figure 24. Single Supply Application (16-Pin SOIC)

8.3 Application Details

Several factors contribute to power dissipation and consequently higher semiconductor junction temperatures. Understanding these factors is necessary if the LM7372 is to perform to the desired specifications. Since different applications will have different dissipation levels and since there are various possible compromises between the ways these factors will contribute to the total junction temperature, this section will examine the typical application shown in Figure 24 as an example, and offer solutions when encountering excessive junction temperatures.

There are two major contributors to the internal power dissipation. The first is the product of the supply voltage and the LM7372 quiescent current when no signal is being delivered to the external load, and the second is the additional power dissipated while delivering power to the external load. For low frequency (<1MHz) applications, the LM7372 supply current specification will suffice to determine the quiescent power dissipation (see *High Frequency/Large Signal Swing Considerations* for cases where the frequency range exceeds 1MHz and the LM7372 supply current increases). The LM7372 quiescent supply current is given as 6.5 mA per amplifier, so with a 24-V supply, the power dissipation is:

$$P_Q = V_S \times 2I_q$$
$$= 24 \times 2 \times (6.5 \times 10^{-3})$$
$$= 312\text{mW}$$

where

- $(V_S = V^+ - V^-)$ (1)

This is already a high level of internal power dissipation, and in a small surface mount package with a thermal resistance of $R_{\theta JA}$ = 140°C/Watt -- a not unreasonable value for an 8-Pin SOIC package -- would result in a junction temperature 140°C/W x 0.312W = 43.7°C above the ambient temperature. A similar calculation using the worst case maximum supply current specification of 8.5 mA per amplifier at an 85°C ambient will yield a power dissipation of 456 mW with a junction temperature of 149°C, perilously close to the maximum permitted junction temperature of 150°C.

The second contributor to high junction temperature is the additional power dissipated internally when power is being delivered to the external load. This cause of temperature rise can be more difficult to calculate, even when the actual operating conditions are known.

Application Details (continued)

For a Class B output stage, one transistor of the output pair will conduct the load current as the output voltage swings positive, with the other transistor drawing no current, and hence dissipating no power. During the other half of the signal swing, this situation is reversed, with the lower transistor sinking the load current and the upper transistor cut off. The current in each transistor will be a half wave rectified version of the total load current. Ideally neither transistor will dissipate power when there is no signal swing, but will dissipate increasing power as the output current increases. However, as the signal voltage across the load increases with load current, the voltage across the output transistor (which is the difference voltage between the supply voltage and the instantaneous voltage across the load) will decrease and a point will be reached where the dissipation in the transistor will begin to decrease again. If the signal is driven into a square wave, ideally the transistor dissipation will fall to zero.

Therefore, for each amplifier, with an effective load each of R_L and a sine wave source, integration over the half cycle with a supply voltage V_S and a load voltage V_L yields the average power dissipation of:

$$P_D = V_S V_L/\pi R_L - V_L^2/2R_L$$

where

- V_S is the supply voltage
- V_L is the peak signal swing across the load R_L (2)

For the package, the power dissipation will be doubled since there are two amplifiers in the package, each contributing half the swing across the load.

The circuit in Single Supply Application, Figure 24, is using the LM7372 as the upstream driver in an ADSL application with Discrete MultiTone modulation. With DMT the upstream signal is spread into 32 adjacent channels each 4 kHz wide. For transmission over POTS, the regular telephone service, this upstream signal from the CPE (Customer Premise Equipment) occupies a frequency band from around 20 kHz up to a maximum frequency of 135 kHz. At first sight, these relatively low transmission frequencies certainly do not seem to require the use of very high speed amplifiers with GBW products in the range of hundreds of megahertz. However, the close spacing of multiple channels places stringent requirements on the linearity of the amplifier, since non-linearities in the presence of multiple tones will cause harmonic products to be generated that can easily interfere with the higher frequency down stream signals also present on the line. The need to deliver 3rd Harmonic distortion terms lower than −75 dBc is the reason for the LM7372 quiescent current levels. Each amplifier is running over 3mA in the output stage alone in order to minimize crossover distortion. The xDSL signal levels are adjusted to provide a given power level on the line, and in the case of ADSL, this is an average power of 13 dBm. For a line with a characteristic impedance of 100 Ω this is only 20 mW (= 1 mW x $10^{(13/10)}$). Because the transformer shown in Figure 24 is part of a transceiver circuit, two back-termination resistors are connected in series with each amplifier output. Therefore the equivalent R_L for each amplifier is also 100 Ω, and each amplifier is required to deliver 20 mW to this load.

Since $V_L^2/2RL = 20mW$ then $V_L = 2V(peak)$. (3)

Using Equation 2 with this value for signal swing and a 24V supply, the internal power dissipation per amplifier is 132.8mW. Adding the quiescent power dissipation to the amplifier dissipation gives the total package internal power dissipation as

$$P_{D(TOTAL)} = 312mW + (2 \times 132.8mW) = 578mW \quad (4)$$

This result is actually quite pessimistic because it assumes that the dissipation as a result of load current is simply added to the dissipation as a result of quiescent current. This is not correct, since the AB bias current in the output stage is diverted to load current as the signal swing amplitude increases from zero. In fact with load currents in excess of 3.3 mA, all the bias current is flowing in the load, consequently reducing the quiescent component of power dissipation. Also, it assumes a sine wave signal waveform when the actual waveform is composed of many tones of different phases and amplitudes which may demonstrate lower average power dissipation levels.

Application Details (continued)

The average current for a load power of 20 mW is 14.1 mA (= √(20mW/100)). Neglecting the AB bias current, this appears as a full-wave rectified current waveform in the supply current with a peak value of 19.9mA. The peak to average ratio for a waveform of this shape is 1.57, so the total average load current is 12.7 mA (= 19.9 mA/1.57). Adding this to the quiescent current, and subtracting the power dissipated in the load (20 mV x 2 = 40 mW) gives the same package power dissipation level calculated above (= (12.7 + 13) mA x 24 V –40 mV = 576 mW). Nevertheless, when the supply current peak swing is measured, it is found to be significantly lower because the AB bias current is contributing to the load current. The supply current has a peak swing of only 14 mA (compared to 19.9 mA) superimposed on the quiescent current, with a total average value of only 21 mA. Therefore, the total package power dissipation in this application is:

$$P_{D(TOTAL)} = (V_S \times I_{avg}) - \text{Power in Load}$$
$$= (24 \times 21)\text{mW} - 40\text{mW}$$
$$= 464\text{mW} \quad (5)$$

This level of power dissipation would not take the junction temperature in the 8-Pin SO PowerPAD package over the absolute maximum rating at elevated ambient temperatures (barely), but there is no margin to allow for component tolerances or signal variances.

To develop 20 mW in a 100 Ω requires each amplifier to deliver a peak voltage of only 2V, or 4V($_{P-P}$). This level of signal swing does not require a high supply voltage but the application uses a 24V supply. This is because the modulation technique uses a large number of tones to transmit the data. While the average power level is held to 20 mW, at any time the phase and amplitude of individual tones will be such as to generate a combined signal with a higher peak value than 2 V. For DMT this crest factor is taken to be around 5.33 so each amplifier has to be able to handle a peak voltage swing of:

$$V_{Lpeak} = 1.4 \times 5.33 = 7.5 \text{ V or } 15 \text{ V}(_{P-P}) \quad (6)$$

If other factors, such as transformer loss or even higher peak to average ratios are allowed for, this means the amplifiers must each swing between 16 to 18 V($_{P-P}$).

The required signal swing can be reduced by using a step-up transformer to drive the line. For example a 1:2 ratio will reduce the peak swing requirement by half, and this would allow the supply to be reduced by a corresponding amount. This is not recommended for the LM7372 in this particular application for two reasons. First, although the quiescent power contribution to the overall dissipation is reduced by about 150 mW, the internal power dissipation to drive the load remains the same, since the load for each amplifier is now 25 Ω instead of 100 Ω. Secondly, this is a transceiver application where downstream signals are simultaneously appearing at the transformer secondary. The down stream signals appear differentially across the back termination resistors and are now stepped down by the transformer turns ratio with a consequent loss in receiver sensitivity compared to using a 1:1 transformer. Any trade-off to reduce the supply voltage by an increase in turns ratio should bear these factors in mind, as well as the increased signal current levels required with lower impedance loads.

At an elevated ambient temperature of 85°C and with an average power dissipation of 464mW, a package thermal resistance between 60°C/W and 80°C/W will be needed to keep the maximum junction temperature in the range 110°C to 120°C. The SO PowerPAD package would be the package of choice here with ample board copper area to aid in heat dissipation (see Table 2).

For most standard surface mount packages (8-Pin SOIC, 14-Pin SOIC, 16-Pin SOIC, and so forth), the only means of heat removal from the die is through the bond wires to external copper connecting to the leads. Usually it will be difficult to reduce the thermal resistance of these packages below 100°C/W by these methods and several manufacturers, including Texas Instruments, offer package modifications to enhance the thermal characteristics.

Application Details (continued)

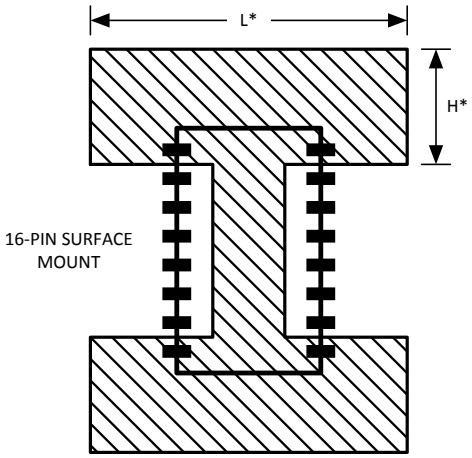


Figure 25. Copper Heatsink Patterns

The LM7372 is available in the 16-Pin SOIC package. Since only 8 pins are needed for the two operational amplifiers, the remaining pins are used for heat sink purposes. Each of the end pins, 1,8,9 & 16 are internally bonded to the lead frame and form an effective means of transferring heat to external copper. This external copper can be either electrically isolated or be part of the topside ground plane in a single supply application.

Figure 25 shows a copper pattern which can be used to dissipate internal heat from the LM7372. Table 1 gives some values of $R_{\theta JA}$ for different values of L and H with 1oz copper.

Table 1. 16-Pin SOIC Thermal Resistance with Area of Cu

L (in)	H (in)	$R_{\theta JA}$ (°C/W)
1	0.5	83
2	1	70
3	1.5	67

From Table 1 it is apparent that two areas of 1oz copper at each end of the package, each 2 in^2 in area (for a total of 2600mm^2) will be sufficient to hold the maximum junction temperature under 120°C with an 85°C ambient temperature.

An even better package for removing internally generated heat is a package with an exposed die attach paddle. Improved removal of internal heat can be achieved by directly connecting bond wires to the lead frame inside the package. Since this lead frame supports the die attach paddle, heat is transferred directly from the substrate to the outside copper by these bond wires. The LM7372 is also available in the 8-Pin SO PowerPAD package. For this package the entire lower surface of the paddle is not covered with plastic, which would otherwise act as a thermal barrier to heat transfer. Heat is transferred directly from the die through the paddle rather than through the small diameter bonding wires. Values of $R_{\theta JA}$ in °C/W for the SO PowerPAD package with various areas and weights of copper are tabulated in Table 2.

Table 2. Thermal Resistance of SO PowerPAD Package

COPPER	AREA	0.5 in^2 (EACH SIDE)	1.0 in^2 (EACH SIDE)	2.0 in^2 (EACH SIDE)
0.5 oz 1.0 oz 2.0 oz	Top Layer Only	115 91 74	105 79 60	102 72 52
0.5 oz 1.0 oz 2.0 oz	Bottom Layer Only	102 92 85	88 75 66	81 65 54
0.5 oz 1.0 oz 2.0 oz	Top And Bottom	83 71 63	70 57 48	63 47 37

Table 2 clearly demonstrates the superior thermal qualities of the exposed pad package. For example, using the topside copper only in the same way as shown for the SOIC package (Figure 25), the SO PowerPAD requires half the area of 1 oz copper (2 in^2, total or 1300mm^2), for a comparable thermal resistance of 72°C/Watt. This gives considerably more flexibility in the PCB layout aside from using less copper.

The shape of the heat sink shown in Figure 25 is necessary to allow external components to be connected to the package pins. If thermal vias are used beneath the SO PowerPAD to the bottom side ground plane, then a square pattern heat sink can be used and there is no restriction on component placement on the top side of the board. Even better thermal characteristics are obtained with bottom layer heat sinking. A 2 inch square of 0.5oz copper gives the same thermal resistance (81°C/W) as a competitive thermally enhanced 8-Pin SOIC package which needs two layers of 2 oz copper, each 4 in^2 (for a total of 5000 mm^2). With heavier copper, thermal resistances as low as 54°C/W are possible with bottom side heat sinking only, substantially improving the long term reliability since the maximum junction temperature is held to less than 110°C, even with an ambient temperature of 85°C. If both top and bottom copper planes are used, the thermal resistance can be brought to under 40°C/W.

8.3.1 High Frequency/Large Signal Swing Considerations

The LM7372 employs a unique input stage in order to support large slew rate and high output current capability with large output swings, with a relatively low quiescent current. This input architecture boosts the device supply current when the application demands it. The result is a supply current which increases at high enough frequencies when the output swing is large enough with added power dissipation as a consequence.

Figure 26 shows the amount of increase in supply current as a function of frequency for various sinusoidal output swing amplitudes:

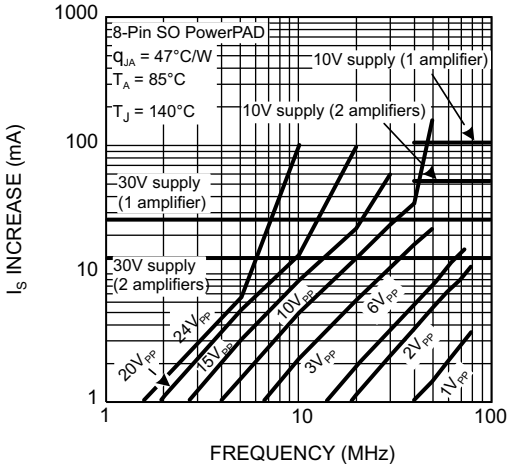


Figure 26. Power Supply Current Increase

Figure 26 shows that there could be 1 mA or more excess supply current per amplifier with close to full output swing (24 V_{PP}) when frequency is just above 1MHz (or at higher frequencies when the output swing is less). This boost in supply current enables the output to “keep up” with high frequency/large signal output swing, but in turn, increases the total package power dissipation and therefore raises the device junction temperature. As a consequence, it is necessary to pay special attention to the package heatsink design for these demanding applications, especially for ones that run at higher supply voltages. For that reason, Figure 26 has the safe operating limits for the 8-Pin SO PowerPAD package -- for example, “30V supply (2 amplifiers)” horizontal line -- superimposed on top of it (with T_J limit of 140°C when operated at 85°C ambient), so that the designer can readily decide whether or not there is need for additional heat sinking.

For example, if the LM7372 is operating similarly to the Figure 24 schematic with a single power supply of 10 V, it is safe to have up to 10 V_{PP} output swing at up to 40 MHz with no additional heat sinking. This is determined by inspecting Figure 24 where the "10 V supply (2 amplifiers)" safe operating limit intercepts the 10 V_{PP} swing graph at around 40 MHz Use the "10 V supply (1 amplifier) safe operating limit in cases where the second amplifier in the LM7372 package does not experience high frequency/high output swing conditions.

At any given “I_S increase” value (y axis), the product of frequency and output swing remains essentially constant for all output swing plots. This holds true for the lower frequency range before the plots experience a slope increase. Therefore, if the application example just discussed operates up to 60MHz instead, it is possible to calculate the junction-temperature-limited maximum output swing of 6.7 V_{PP}(= 40 MHz x 10V_{PP}/60 MHz) instead.

Please note that Figure 26 precludes any additional amplifier power dissipation related to load (this topic is discussed below in detail). This load current, if large enough, will reduce the operating frequency/output swing further. It is important to note that the LM7372 can be destroyed if it is allowed to dissipate enough power that compromises its maximum junction temperature limit of 150°C.

With the op amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power itself could include an average value (due to a DC load current) and an AC component. DC load current would flow if there is an output voltage offset, or the output AC average current is non-zero, or if the op amp operates in a single supply application where the output is maintained somewhere in the range of linear operation. Therefore:

$$P_{D(TOTAL)} = P_Q + P_{DC} + P_{AC} \quad (7)$$

$$P_Q = |I_S \bullet V_S| \text{ (Op Amp Quiescent Power Dissipation)} \quad (8)$$

$$P_{DC} = |I_O \bullet (V_R - V_O)| \text{ (DC Load Power)} \quad (9)$$

For P_{AC}, (AC Load Power) see Table 3

where:

- I_S = Supply Current
- V_S = Total Supply Voltage ($V^+ - V^-$)
- I_O = Average Load Current
- V_O = Average Output Voltage
- V_R = Reference Voltage (V^+ for sourcing and V^- for sinking current)

Table 3 shows the maximum AC component of the load power dissipated by the op amp for standard Sinusoidal, Triangular, and Square Waveforms:

Table 3. Normalized Maximum AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} (W.Ω/V^2)		
SINUSOIDAL	**TRIANGULAR**	**SQUARE**
50.7 x 10^{-3}	46.9 x 10^{-3}	62.5 x 10^{-3}

The table entries are normalized to V_S^2/R_L. These entries are computed at the output swing point where the amplifier dissipation is the highest for each waveform type. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor V_S^2/R_L. For example, with ±5V supplies, a 100-Ω load and triangular output waveform, power dissipation in the output stage is calculated as: P_{AC} = 46.9 x 10^{-3} x 10^2/100 = 46.9mW which contributes another 2.2°C (= 46.9mW x 47°C/W) rise to the LM7372 junction temperature in the 8-Pin SO PowerPAD package.

9 Power Supply Recommendations

The LM7372 is fabricated on a high voltage, high speed process. Using high supply voltages ensures adequate headroom to give low distortion with large signal swings. In Figure 24, a single 24 V supply is used. To maximize the output dynamic range the non-inverting inputs are biased to half supply voltage by the resistive divider R1, R2. The input signals are AC coupled and the coupling capacitors (C1, C2) can be scaled with the bias resistors (R3, R4) to form a high pass filter if unwanted coupling from the POTS signal occurs.

Supply decoupling is important at both low and high frequencies. The 10µF Tantalum and 0.1µF Ceramic capacitors should be connected close to the supply Pin 14. Note that the V^- pin (pin 6), and the PCB area associated with the heatsink (Pins 1,8,9 & 16) are at the same potential. Any layout should avoid running input signal leads close to this ground plane, or unwanted coupling of high frequency supply currents may generate distortion products.

Although this application shows a single supply, conversion to a split supply is straightforward. The half supply resistive divider network is eliminated and the bias resistors at the non-inverting inputs are returned to ground. For example, see Figure 23 where the pin numbers in Figure 23 are given for SO PowerPAD package, whereas those in Single Supply Application (16-Pin SOIC) are for the SOIC package. With a split supply, note that the ground plane and the heatsink copper must be separate and are at different potentials, with the heatsink (pin 4 of the SO PowerPAD, pins 6,1,8,9 and 16 of the SOIC) now at a negative potential (V^-).

In either configuration, the area under the input pins should be kept clear of copper (whether ground plane copper or heatsink copper) to avoid parasitic coupling to the inputs.

The LM7372 is stable with non inverting closed loop gains as low as +2. Typical of any voltage feedback operational amplifier, as the closed loop gain of the LM7372 is increased, there is a corresponding reduction in the closed loop signal bandwidth. For low distortion performance it is recommended to keep the closed loop bandwidth at least 10X the highest signal frequency. This is because there is less loop gain (the difference between the open loop gain and the closed loop gain) available at higher frequencies to reduce harmonic distortion terms.

10 Layout

10.1 Layout Guidelines

Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitance on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15, "Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers", SNOA367, for more information). Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Table 4. Printed Circuit Board Layout and Evaluation Boards

DEVICE	PACKAGE	EVALUATION BOARD PN
LM7372MA	16-Pin SOIC	None
LM7372MR	8-Pin SO PowerPAD	LMH730121

The DAP (die attach paddle) on the 8-Pin SO PowerPAD should be tied to V^-. It should not be tied to ground. See the respective Evaluation Board documentation.

11 Device and Documentation Support

11.1 Trademarks

VIP is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM7372IMA	NRND	SOIC	D	16	48	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LM7372IMA	
LM7372IMA/NOPB	ACTIVE	SOIC	D	16	48	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM7372IMA	Samples
LM7372IMAX/NOPB	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM7372IMA	Samples
LM7372MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	LM73 72MR	Samples
LM7372MRX	NRND	SO PowerPAD	DDA	8	2500	Non-RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	LM73 72MR	
LM7372MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	LM73 72MR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

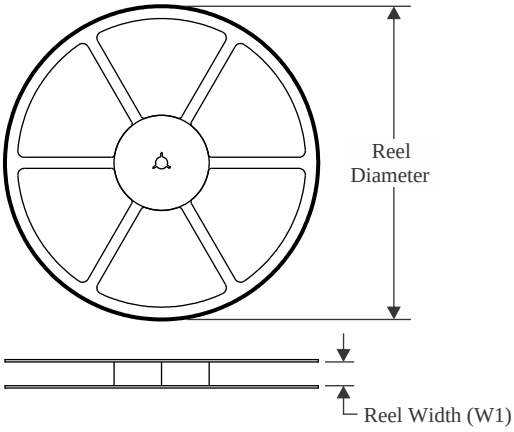
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

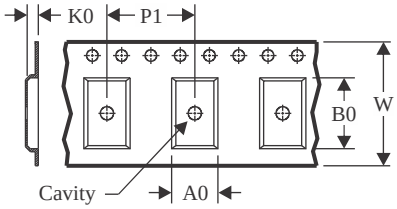
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

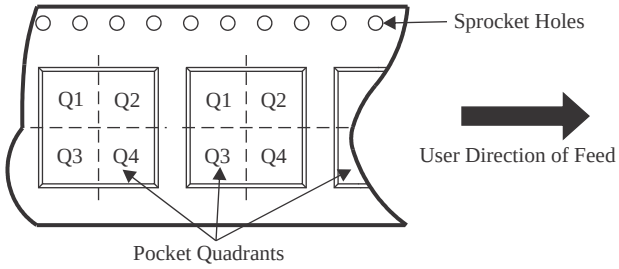


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

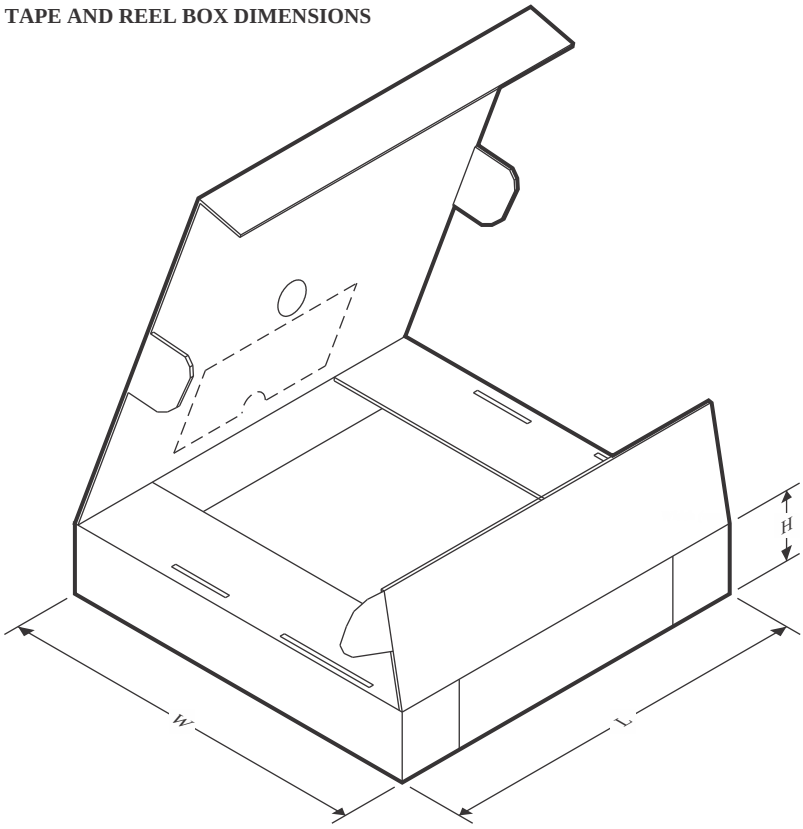
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7372IMAX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LM7372MRX	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM7372MRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

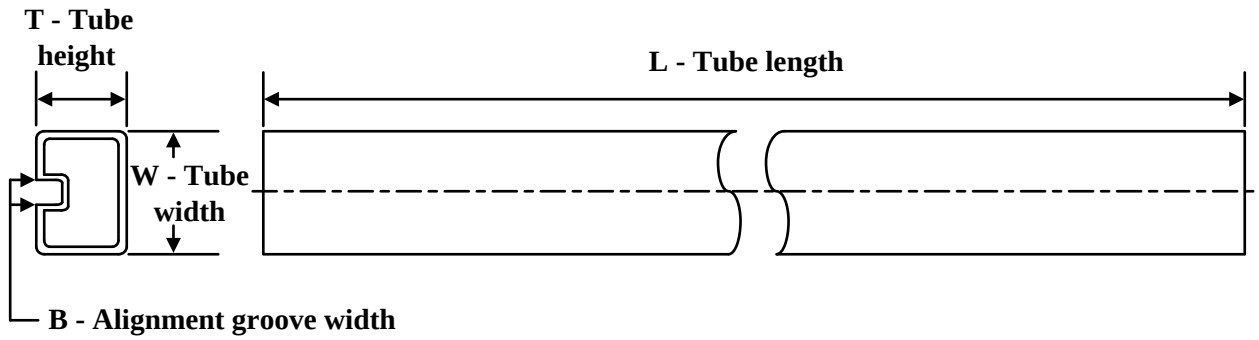
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7372IMAX/NOPB	SOIC	D	16	2500	356.0	356.0	35.0
LM7372MRX	SO PowerPAD	DDA	8	2500	356.0	356.0	35.0
LM7372MRX/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	35.0

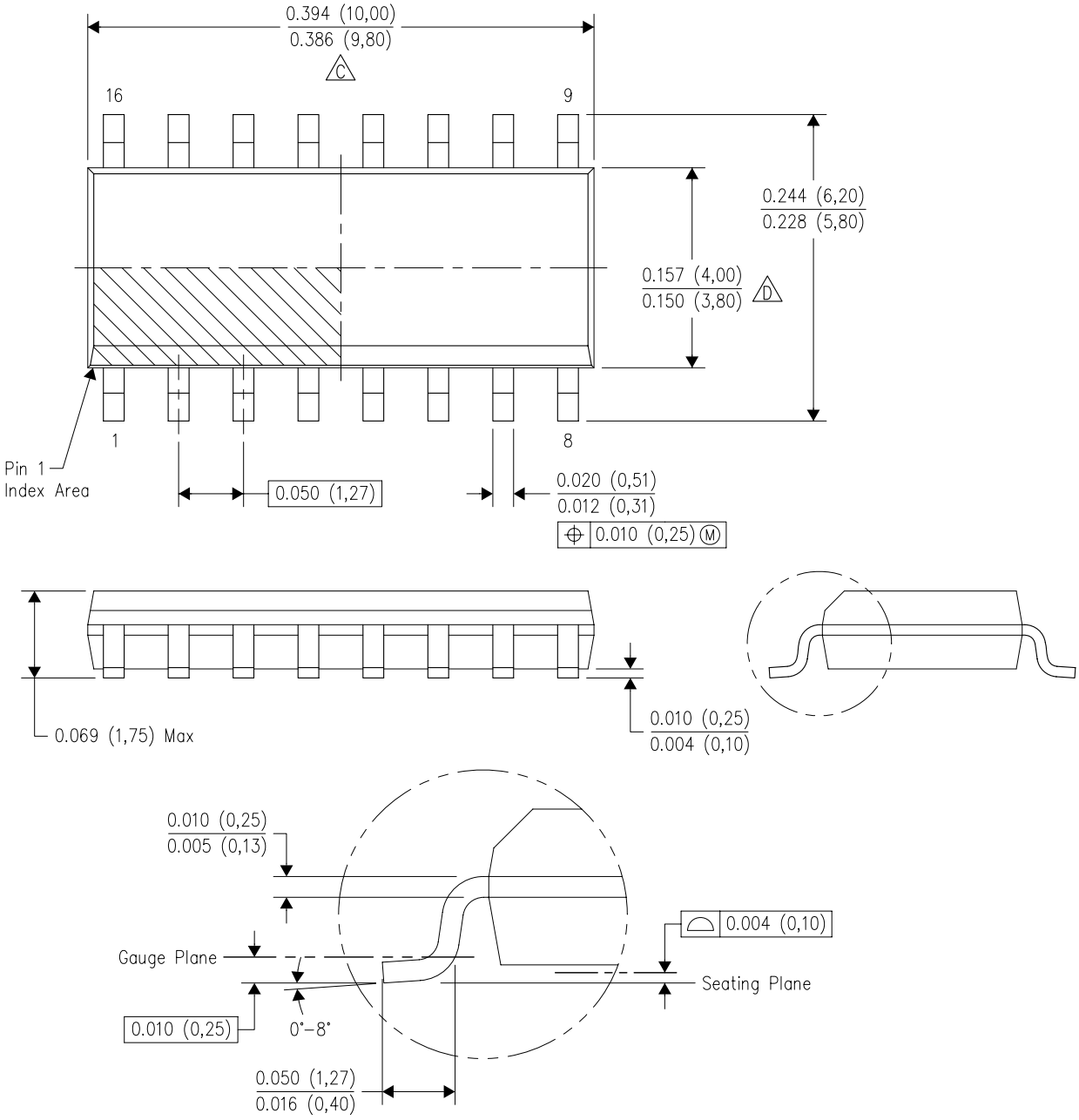
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM7372IMA	D	SOIC	16	48	495	8	4064	3.05
LM7372IMA	D	SOIC	16	48	495	8	4064	3.05
LM7372IMA/NOPB	D	SOIC	16	48	495	8	4064	3.05
LM7372MR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LM7372MR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



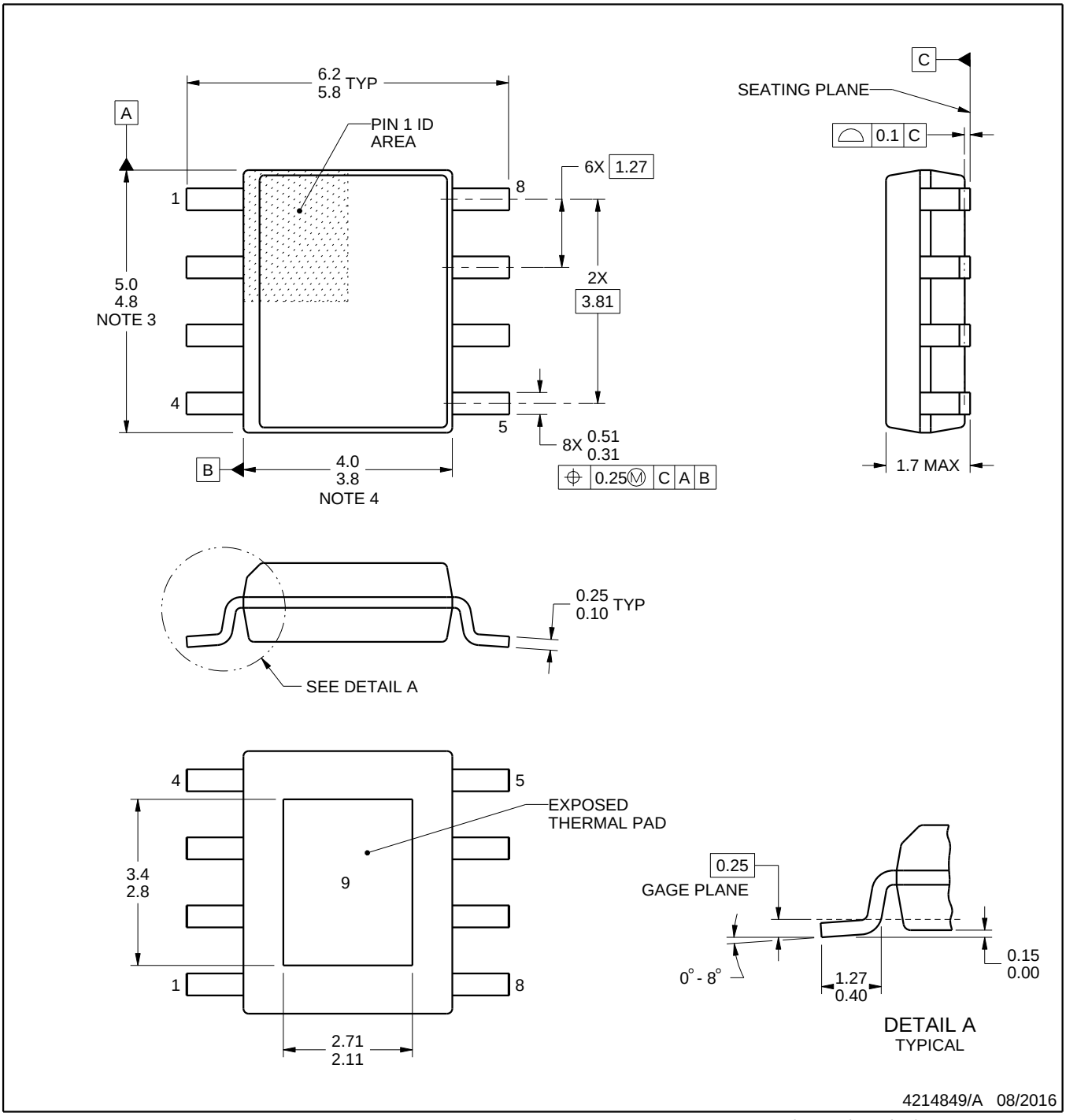
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

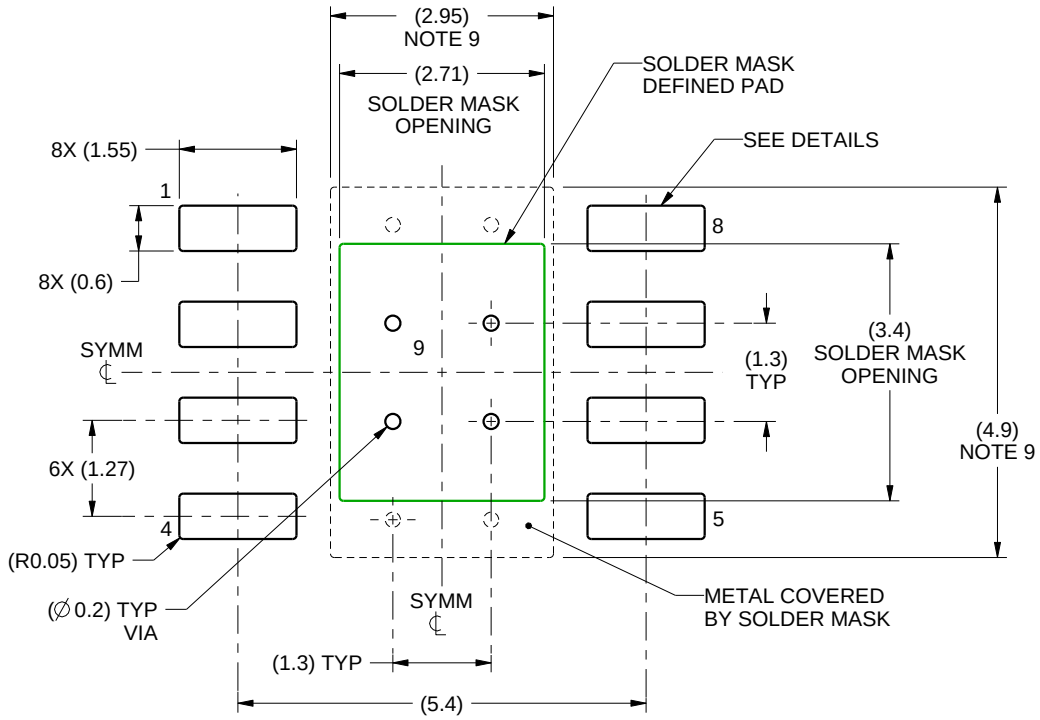
PLASTIC SMALL OUTLINE



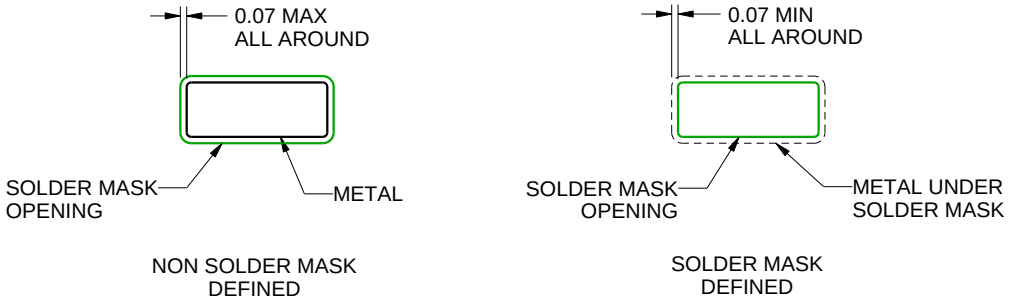
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

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NOTES: (continued)

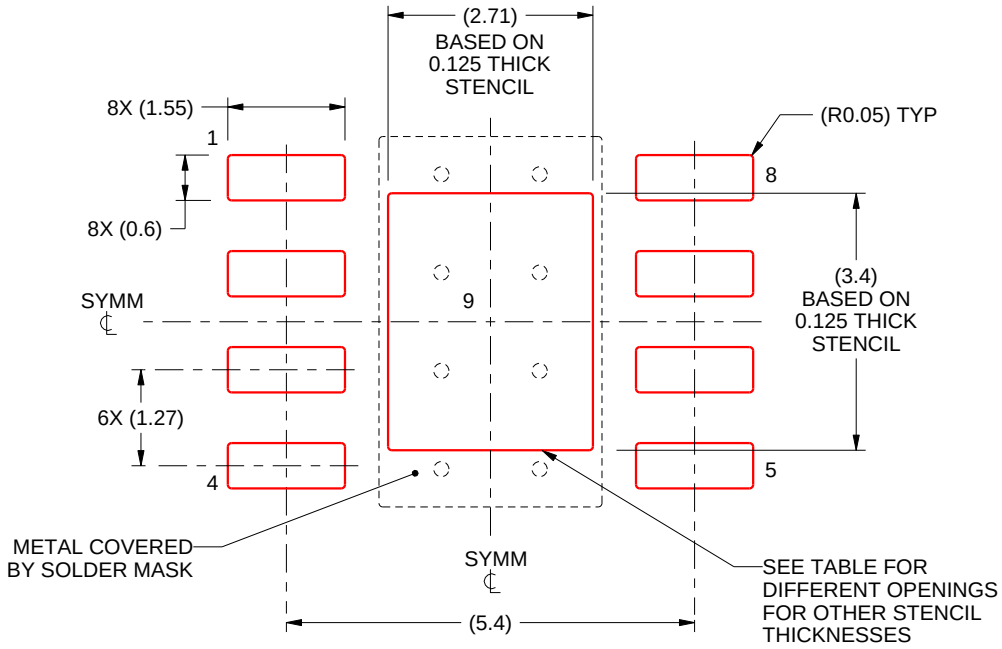
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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