

# LME49724 High Performance, High Fidelity, Fully-Differential Audio Operational Amplifier

Check for Samples: [LME49724](#)

## FEATURES

- Drives 600Ω Loads with Full Output Signal Swing
- Optimized for Superior Audio Signal Fidelity
- Output Short Circuit Protection
- PSRR and CMRR Exceed 100dB (typ)
- Available in SO PowerPad Package

## APPLICATIONS

- Ultra High Quality Audio Amplification
- High Fidelity Preamplifiers and Active Filters
- Simple Single-Ended to Differential Conversion
- State of the Art D-to-A Converters
- State of the Art A-to-D input Amplifiers
- Professional Audio
- High Fidelity Equalization and Crossover Networks
- High Performance Line Drivers and Receivers

## DESCRIPTION

The LME49724 is an ultra-low distortion, low noise, high slew rate fully-differential operational amplifier optimized and fully specified for high performance, high fidelity applications. Combining advanced leading-edge process technology with state of the art circuit design, the LME49724 fully-differential audio operational amplifier delivers superior audio signal amplification for outstanding audio performance. The LME49724 combines extremely low voltage noise density (2.1nV/√Hz) with vanishingly low THD+N (0.00003%) to easily satisfy the most demanding audio applications. To ensure that the most challenging loads are driven without compromise, the LME49724 has a high slew rate of ±18V/μs and an output current capability of ±80mA. Further, dynamic range is maximized by an output stage that drives 600Ω loads to 52V<sub>P-P</sub> while operating on a ±15V supply voltage.

The LME49724's outstanding CMRR (102dB), PSRR (125dB), and V<sub>OS</sub> (0.2mV) results in excellent operational amplifier DC performance.

The LME49724 has a wide supply range of ±2.5V to ±18V. Over this supply range the LME49724's input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49724 is unity gain stable. This Fully-Differential Audio Operational Amplifier achieves outstanding AC performance while driving complex loads with capacitive values as high as 100pF.

**Table 1. Key Specifications**

Power Supply Voltage Range		±2.5V to ±18V
THD+N (A <sub>V</sub> = 1, V <sub>OUT</sub> = 3V <sub>RMS</sub> , f <sub>IN</sub> = 1kHz)	R <sub>L</sub> = 2kΩ	0.00003% (typ)
	R <sub>L</sub> = 600Ω	0.00003% (typ)
Input Noise Density		2.1nV/√Hz (typ)
Slew Rate		±18V/μs (typ)
Gain Bandwidth Product		50 MHz (typ)
Open Loop Gain (R <sub>L</sub> = 600Ω)		125 dB (typ)
Input Bias Current		60nA (typ)
Input Offset Voltage		0.2mV (typ)
DC Gain Linearity Error		0.000009%



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Typical Application

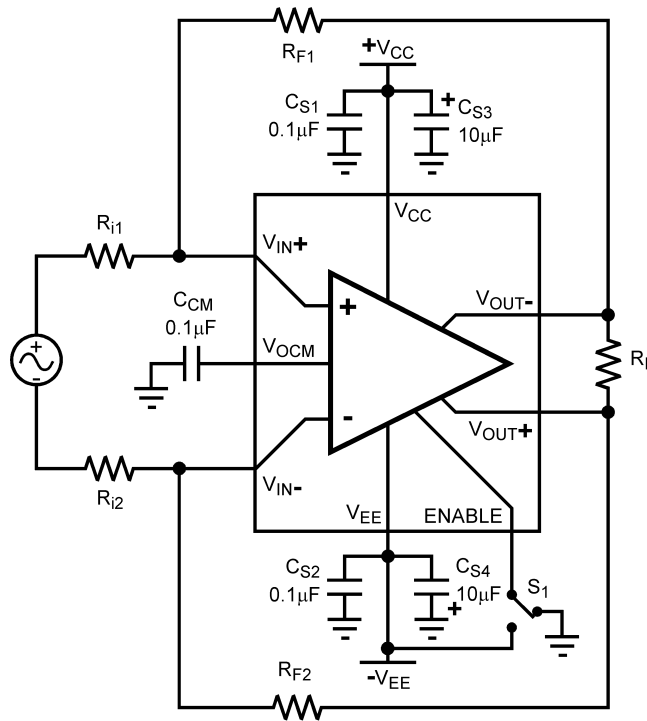


Figure 1. Typical Application Circuit

Connection Diagram

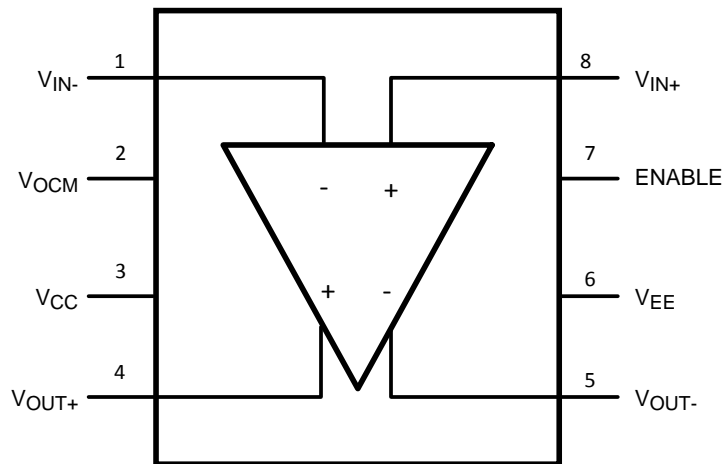


Figure 2. 8-Pin SO PowerPad  
See DDA0008B Package

**PIN DESCRIPTIONS**

Pin	Name	Pin Function	Type
1	V <sub>IN-</sub>	Input pin	Analog Input
2	V <sub>OCM</sub>	Sets the output DC voltage. Internally set by a resistor divider to the midpoint of the voltages on the V <sub>CC</sub> and V <sub>EE</sub> pins. Can be forced externally to a different voltage (50kΩ input impedance).	Analog Input
3	V <sub>CC</sub>	Positive power supply pin.	Power Supply
4	V <sub>OUT+</sub>	Output pin. Signal is inverted relative to V <sub>IN-</sub> where the feedback loop is connected.	Analog Output
5	V <sub>OUT-</sub>	Output pin. Signal is inverted relative to V <sub>IN+</sub> where the feedback loop is connected.	Analog Output
6	V <sub>EE</sub>	Negative power supply pin or ground for a single supply configuration.	Power Supply
7	ENABLE	Enables the LME49724 when the voltage is greater than 2.35V above the voltage on the V <sub>EE</sub> pin. Disable the LME49724 by connecting to the same voltage as on the V <sub>EE</sub> pin which will reduce current consumption to less than 0.3mA (typ).	Analog Input
8	V <sub>IN+</sub>	Input pin	Analog Input
Exposed Pad		Exposed pad for improved thermal performance. Connect to the same potential as the V <sub>EE</sub> pin or electrically isolate.	



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings** <sup>(1)(2)(3)</sup>

Power Supply Voltage	(V <sub>S</sub> = V <sub>CC</sub> +  V <sub>EE</sub>  )	38V
Storage Temperature		-65°C to 150°C
Input Voltage		(V <sub>EE</sub> ) - 0.7V to (V <sub>CC</sub> ) + 0.7V
Output Short Circuit		Continuous
Power Dissipation <sup>(4)</sup>		Internally Limited
ESD Rating <sup>(5)</sup>		2000V
ESD Rating <sup>(6)</sup>		200V
Junction Temperature (T <sub>JMAX</sub> )		150°C
Soldering Information	Vapor Phase (60sec.)	215°C
	Infrared (60sec.)	220°C
Thermal Resistance	θ <sub>JA</sub> (MR)	49.6°C/W

- (1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The *Electrical Characteristics* tables list specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T<sub>JMAX</sub>, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation is P<sub>DMAX</sub> = (T<sub>JMAX</sub> - T<sub>A</sub>) / θ<sub>JA</sub> or the number given in *Absolute Maximum Ratings*, whichever is lower.
- (5) Human body model, applicable std. JESD22-A114C.
- (6) Machine model, applicable std. JESD22-A115-A.

## Operating Ratings <sup>(1)(2)</sup>

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
Supply Voltage Range		$\pm 2.5\text{V} \leq V_S \leq \pm 18\text{V}$

- (1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The *Electrical Characteristics* tables list specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

## Electrical Characteristics <sup>(1)(2)</sup>

The following specifications apply for  $V_S = \pm 15\text{V}$ ,  $R_L = 2\text{k}\Omega$ ,  $f_{IN} = 1\text{kHz}$ , and  $T_A = 25^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	LME49724		Units (Limits)
			Typical <sup>(3)</sup>	Limit <sup>(4)</sup>	
<b>POWER SUPPLY</b>					
$V_S$	Operating Power Supply			$\pm 2.5\text{V}$ $\pm 18\text{V}$	V (min) V (max)
$I_{CCQ}$	Total Quiescent Current	$V_O = 0\text{V}$ , $I_O = 0\text{mA}$ Enable = GND Enable = $V_{EE}$	10 0.3	15 0.5	mA (max) mA (max)
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$ <sup>(5)</sup>	125	95	dB (min)
$V_{ENIH}$	Enable High Input Voltage	Device active, $T_A = 25^{\circ}\text{C}$ <sup>(6)</sup>	$V_{EE} + 2.35$		V
$V_{ENIL}$	Enable Low Input Voltage	Device disabled, $T_A = 25^{\circ}\text{C}$ <sup>(6)</sup>	$V_{EE} + 1.75$		V
<b>DYNAMIC PERFORMANCE</b>					
THD+N	Total Harmonic Distortion + Noise	$A_V = 1$ , $V_{OUT} = 3V_{RMS}$ $R_L = 2\text{k}\Omega$ $R_L = 600\Omega$	0.00003 0.00003	0.00009	% % (max)
IMD	Intermodulation Distortion	$A_V = 1$ , $V_{OUT} = 3V_{RMS}$ Two-tone, 60Hz & 7kHz 4:1	0.0005		%
GBWP	Gain Bandwidth Product		50	35	MHz (min)
FPBW	Full Power Bandwidth	$V_{OUT} = 1V_{P-P}$ , $-3\text{dB}$ referenced to output magnitude at $f = 1\text{kHz}$	13		MHz
SR	Slew Rate	$R_L = 2\text{k}\Omega$	$\pm 18$	$\pm 13$	V/ $\mu\text{s}$ (min)
$t_S$	Settling time	$A_V = -1$ , 10V step, $C_L = 100\text{pF}$ settling time to 0.1%	0.2		$\mu\text{s}$
$A_{VOL}$	Open-Loop Voltage Gain	$-10\text{V} < V_{OUT} < 10\text{V}$ , $R_L = 600\Omega$	125	100	dB (min)
		$-10\text{V} < V_{OUT} < 10\text{V}$ , $R_L = 2\text{k}\Omega$	125		dB
		$-10\text{V} < V_{OUT} < 10\text{V}$ , $R_L = 10\text{k}\Omega$	125		dB

- (1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The *Electrical Characteristics* tables list specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Typical values represent most likely parametric norms at  $T_A = +25^{\circ}\text{C}$ , and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
- (4) Datasheet min/max specification limits are specified by test or statistical analysis.
- (5) PSRR is measured as follows:  $V_{OS}$  is measured at two supply voltages,  $\pm 5\text{V}$  and  $\pm 15\text{V}$ .  $\text{PSRR} = |20\log(\Delta V_{OS}/\Delta V_S)|$ .
- (6) The ENABLE threshold voltage is determined by  $V_{BE}$  voltages and will therefore vary with temperature. The typical values represent the most likely parametric norms at  $T_A = +25^{\circ}\text{C}$ .

**Electrical Characteristics <sup>(1)(2)</sup> (continued)**

 The following specifications apply for  $V_S = \pm 15V$ ,  $R_L = 2k\Omega$ ,  $f_{IN} = 1kHz$ , and  $T_A = 25^\circ C$ , unless otherwise specified.

Symbol	Parameter	Conditions	LME49724		Units (Limits)
			Typical <sup>(3)</sup>	Limit <sup>(4)</sup>	
<b>NOISE</b>					
$e_N$	Equivalent Input Noise Voltage	$f_{BW} = 20Hz \text{ to } 20kHz$	0.30	0.64	$\mu V_{RMS} \text{ (max)}$
	Equivalent Input Noise Density	$f = 1kHz$ $f = 10Hz$	2.1 3.7		$nV/\sqrt{Hz} \text{ (max)}$
<b>INPUT CHARACTERISTICS</b>					
$V_{OS}$	Offset Voltage		$\pm 0.2$	$\pm 1$	mV (max)
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Voltage Drift vs Temperature	$-40^\circ C \leq T_A \leq 85^\circ C$	0.5		$\mu V/^\circ C$
$I_B$	Input Bias Current	$V_{CM} = 0V$	60	200	nA (max)
$I_{OS}$	Input Offset Current	$V_{CM} = 0V$	10	65	nA (max)
$\Delta I_{OS}/\Delta Temp$	Input Bias Current Drift vs Temperature	$-40^\circ C \leq T_A \leq 85^\circ C$	0.1		$nA/^\circ C$
$V_{IN-CM}$	Common-Mode Input Voltage Range		$\pm 14$	$V_{CC} - 1.5$ $V_{EE} + 1.5$	V (min) V (min)
CMRR	Common-Mode Rejection	$-10V < V_{CM} < 10V$	102	95	dB (min)
$Z_{IN}$	Differential Input Impedance		16		k $\Omega$
	Common-Mode Input Impedance	$-10V < V_{CM} < 10V$	500		M $\Omega$
<b>OUTPUT CHARACTERISTICS</b>					
$V_{OUTMAX}$	Maximum Output Voltage Swing	$R_L = 600\Omega$	52	50	$V_{P-P} \text{ (min)}$
		$R_L = 2k\Omega$	52		$V_{P-P}$
		$R_L = 10k\Omega$	53		$V_{P-P}$
$I_{OUT-CC}$	Instantaneous Short Circuit Current		80		mA
$R_{OUT}$	Output Impedance	$f_{IN} = 10kHz$ Closed-Loop	0.01		$\Omega$
		Open-Loop	23		$\Omega$
$C_{LOAD}$	Capacitive Load Drive Overshoot	$C_L = 100pF$	5		%

### Typical Performance Characteristics

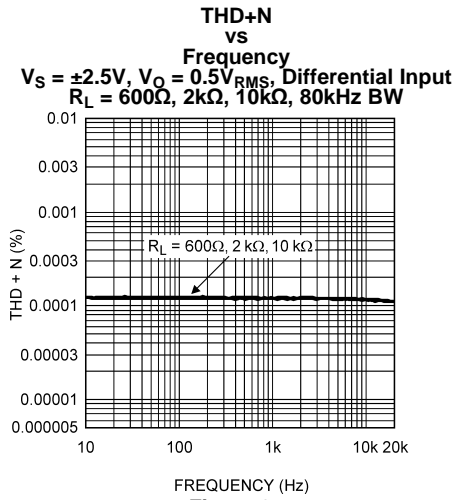


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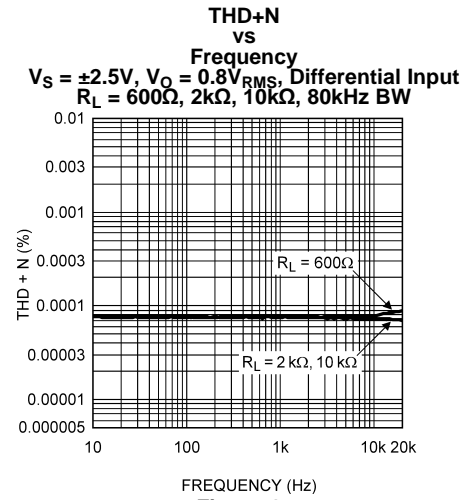


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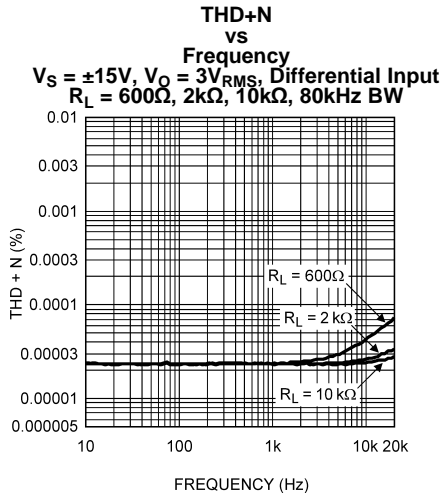


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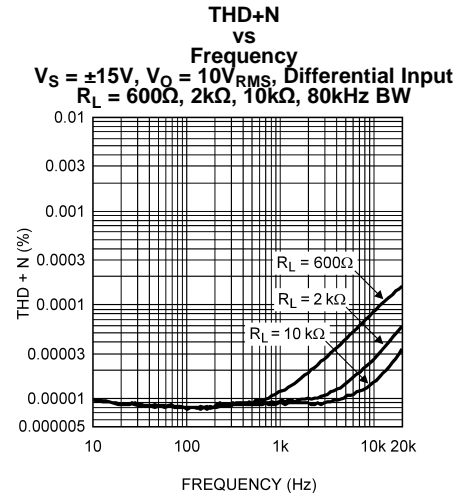


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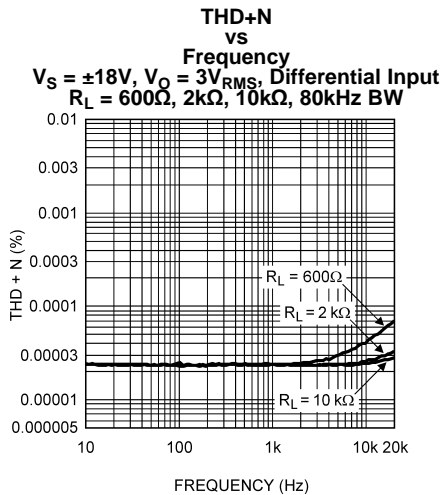


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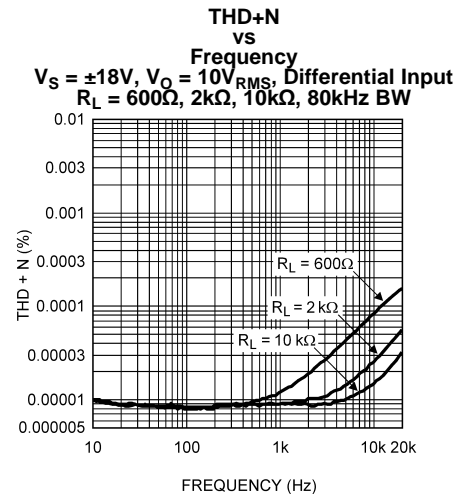


Figure 8.

Typical Performance Characteristics (continued)

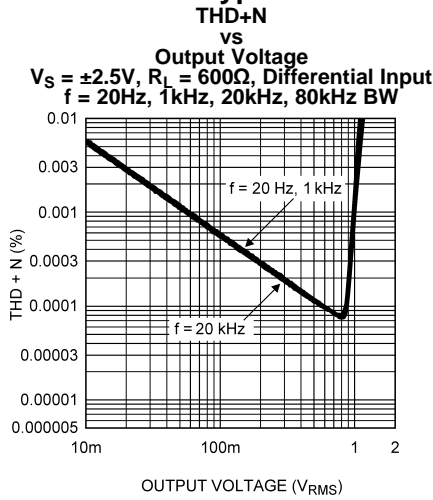


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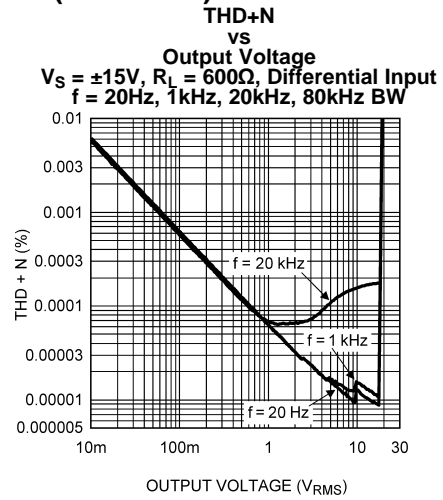


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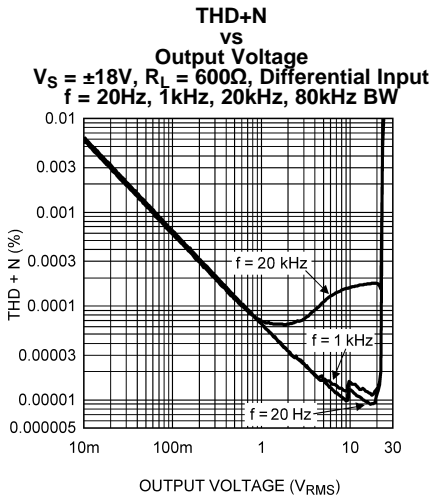


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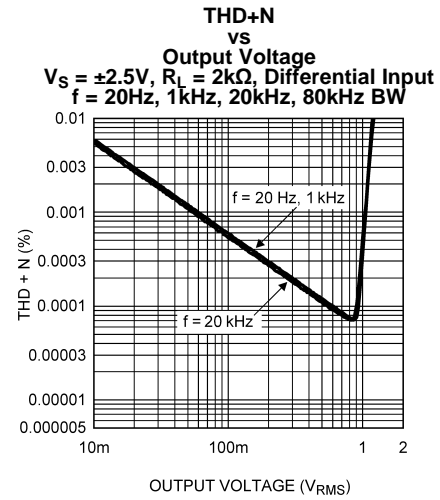


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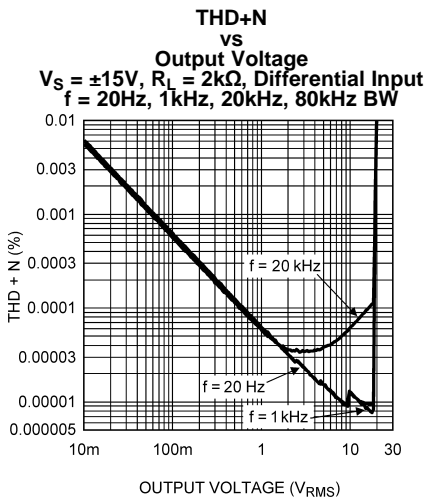


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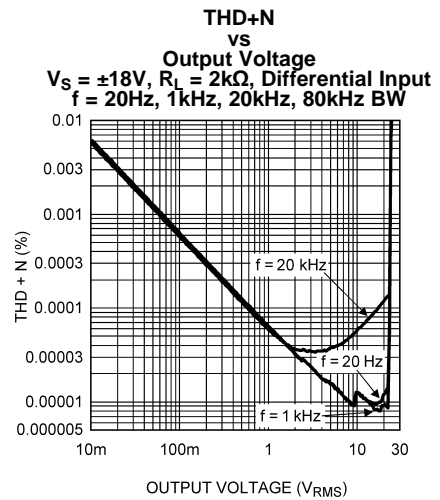


Figure 14.

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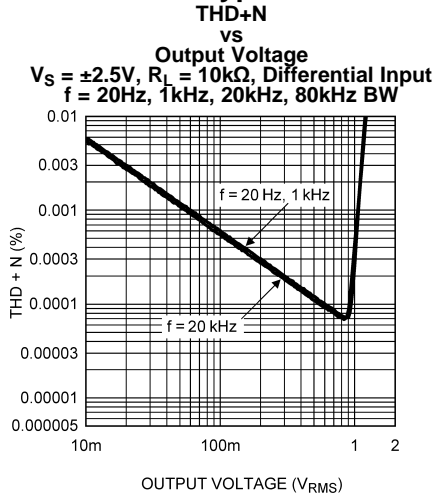


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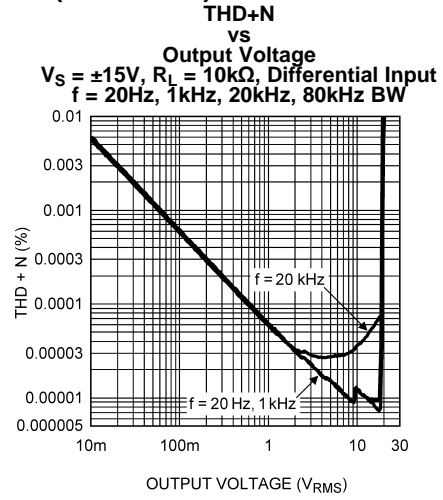


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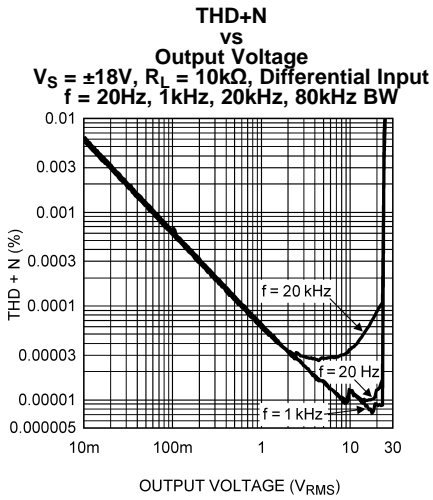


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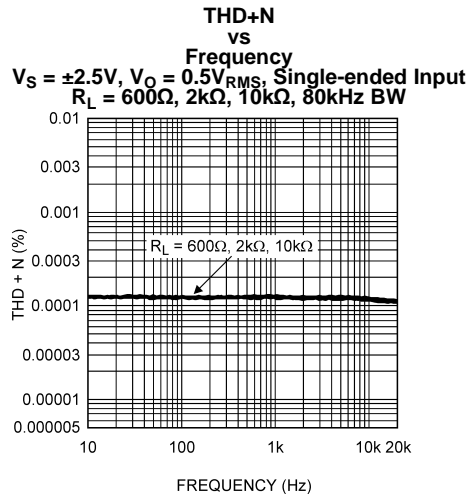


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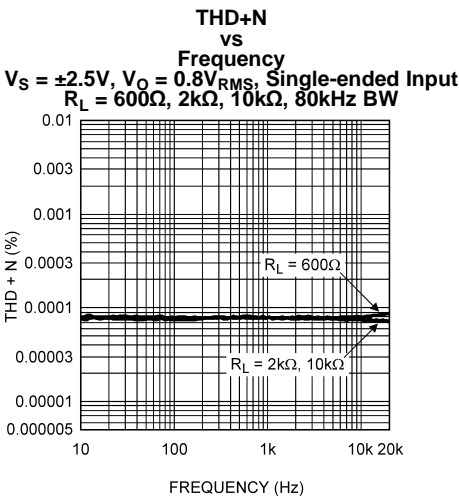


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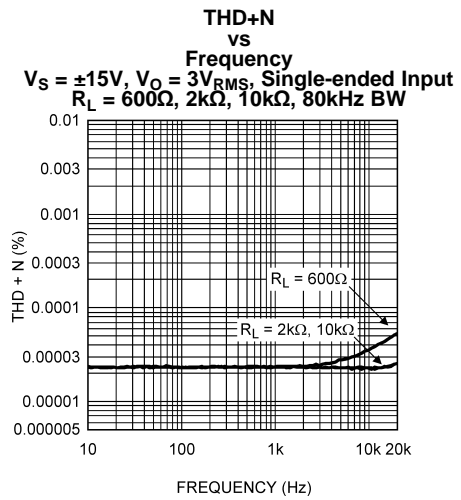


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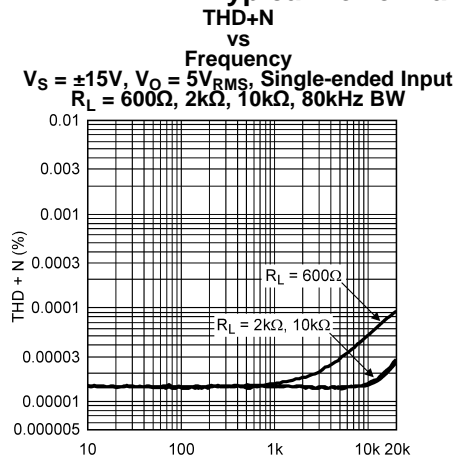


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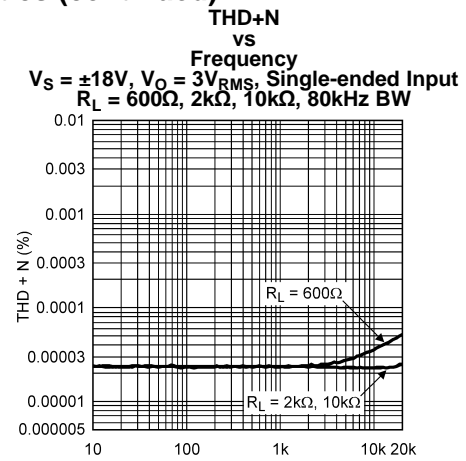


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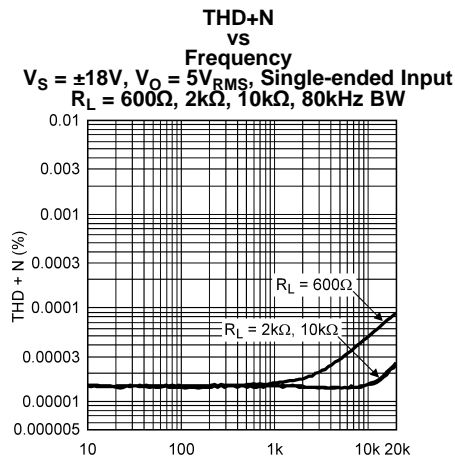


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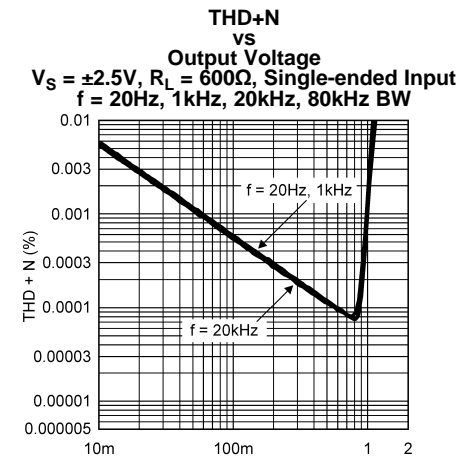


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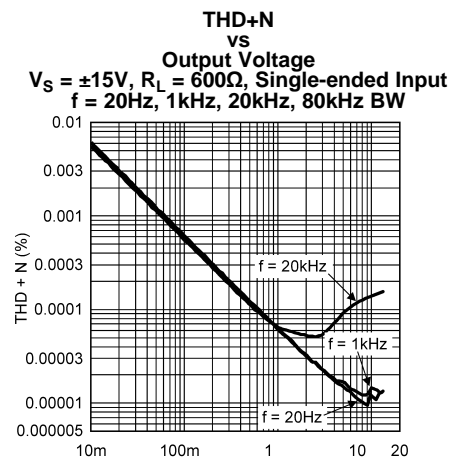


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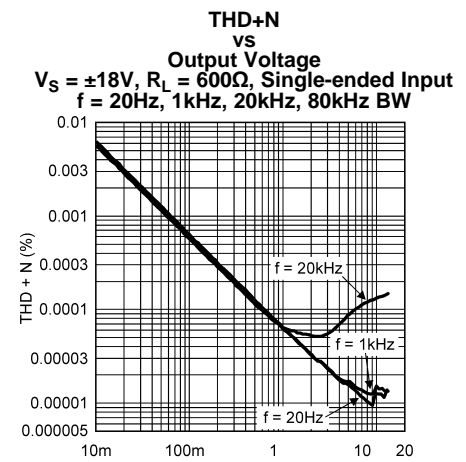


Figure 26.

**Typical Performance Characteristics (continued)**

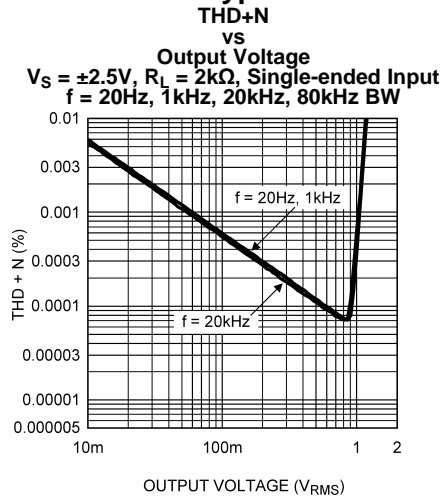


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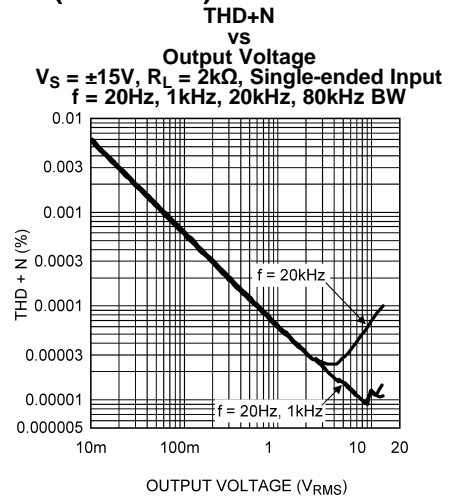


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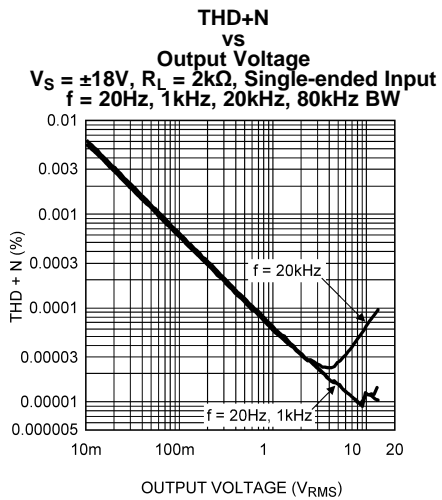


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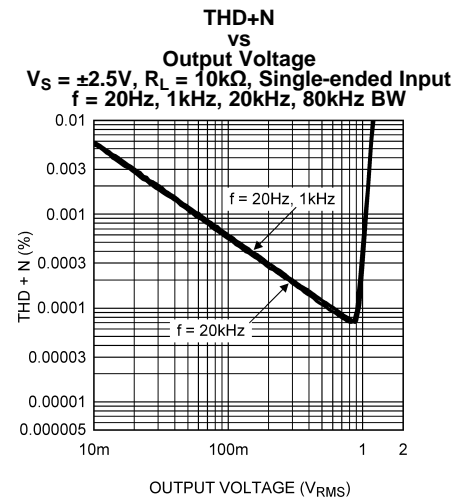


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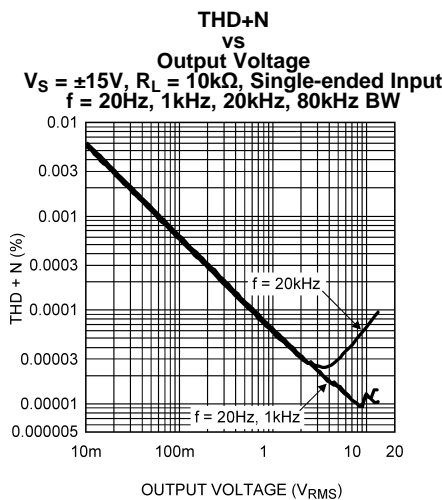


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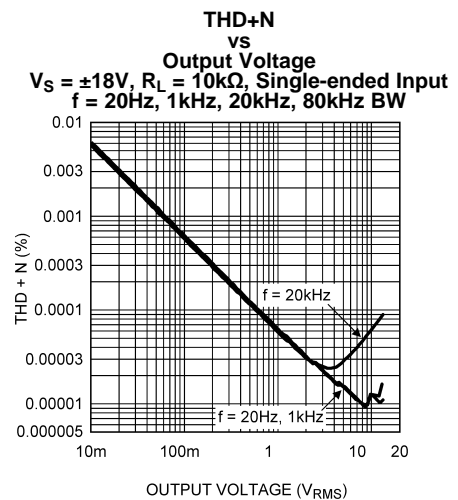


Figure 32.

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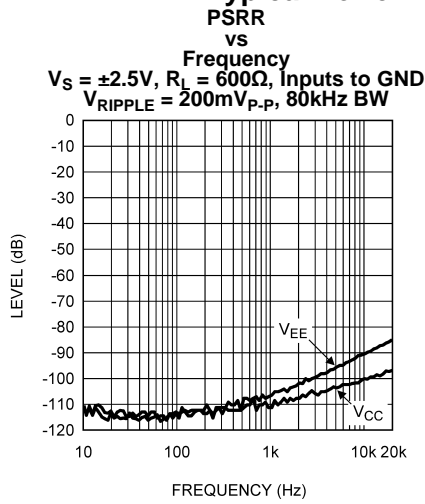


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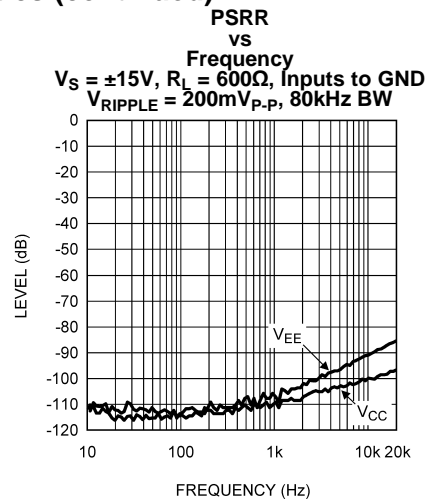


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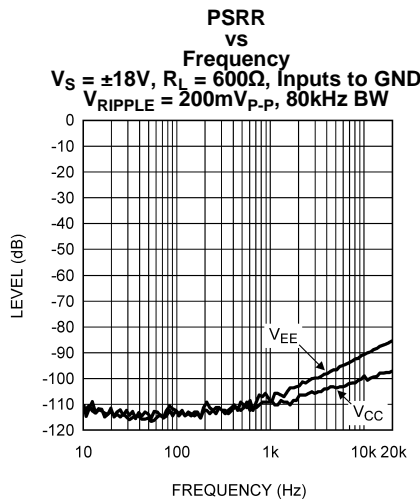


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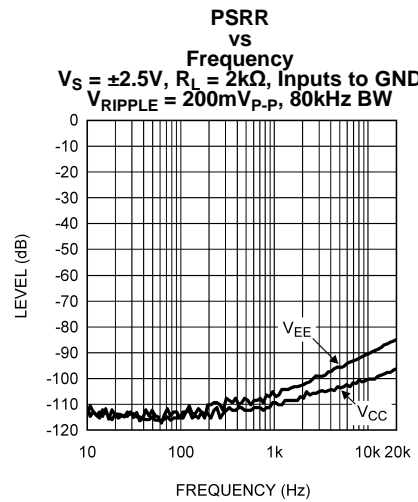


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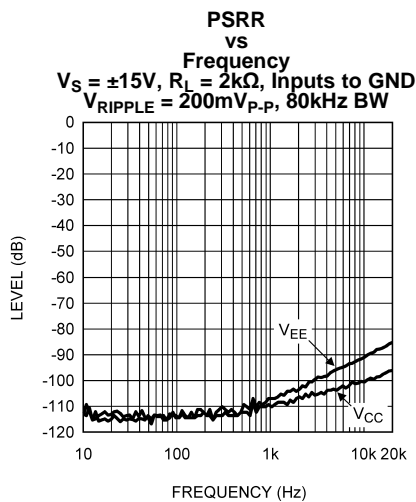


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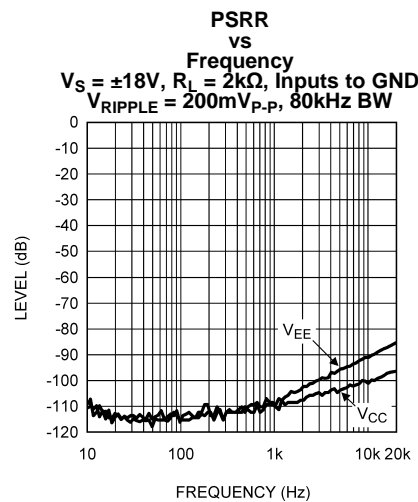


Figure 38.

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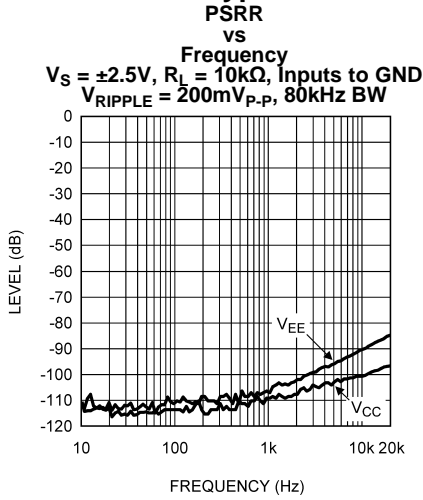


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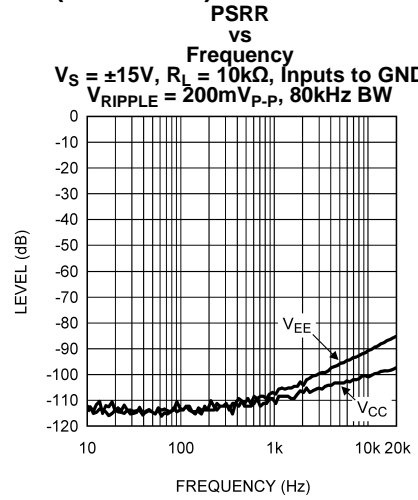


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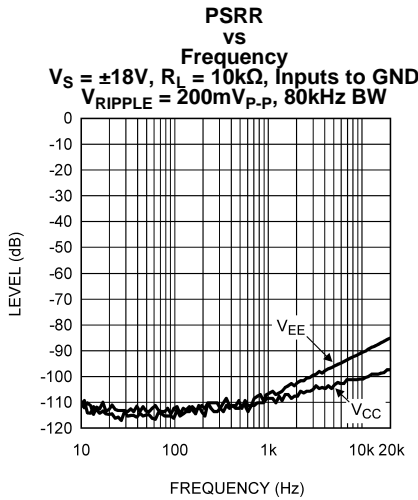


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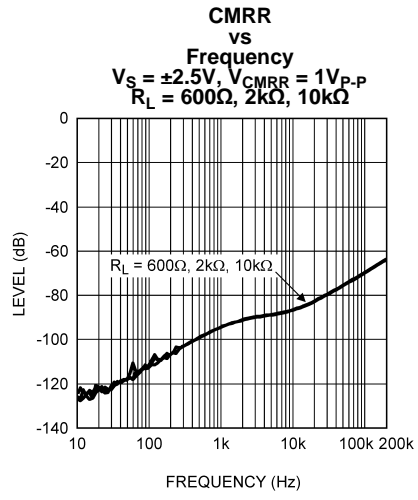


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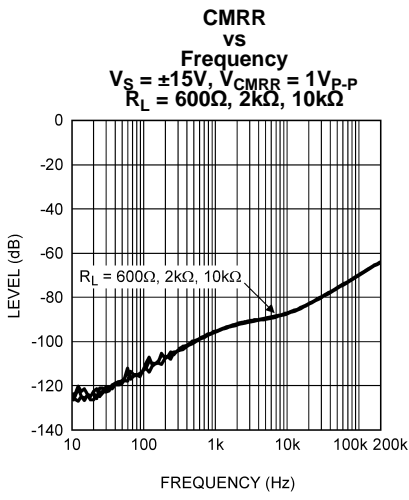


Figure 43.

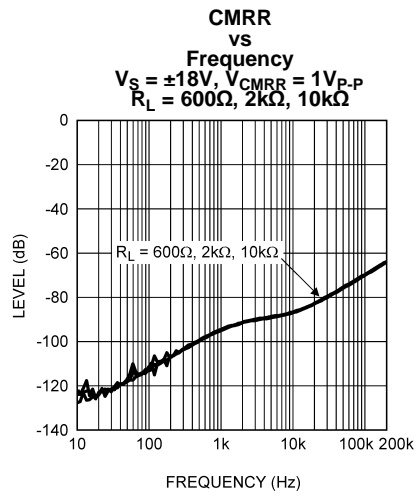


Figure 44.

**Typical Performance Characteristics (continued)**

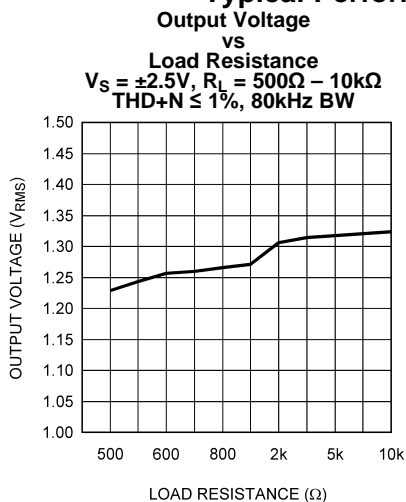


Figure 45.

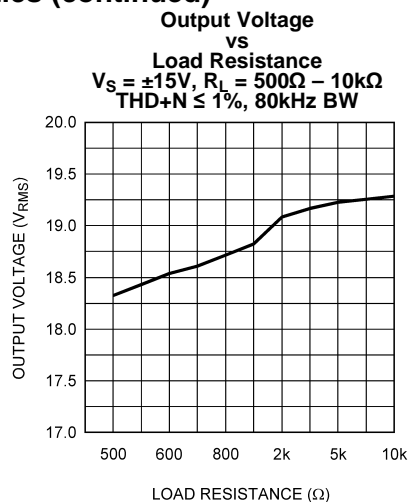


Figure 46.

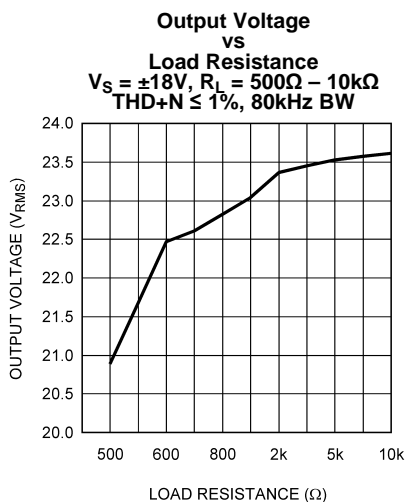


Figure 47.

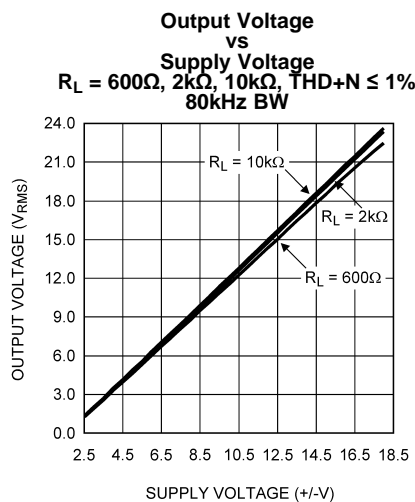


Figure 48.

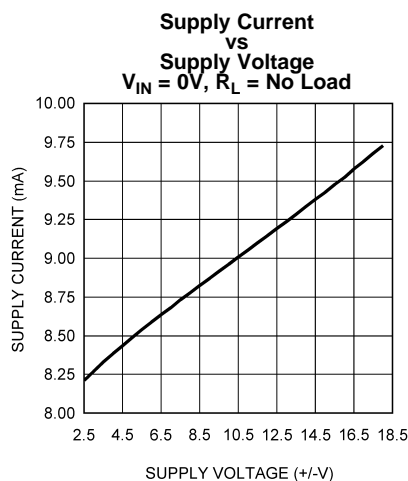


Figure 49.

## APPLICATION INFORMATION

### GENERAL OPERATION

The LME49724 is a fully differential amplifier with an integrated common-mode reference input ( $V_{OCM}$ ). Fully differential amplification provides increased noise immunity, high dynamic range, and reduced harmonic distortion products.

Differential amplifiers typically have high CMRR providing improved immunity from noise. When input, output, and supply line trace pairs are routed together, noise pick up is common and easily rejected by the LME49724. CMRR performance is directly proportional to the tolerance and matching of the gain configuring resistors. With 0.1% tolerance resistors the worst case CMRR performance will be about 60dB ( $20\text{LOG}(0.001)$ ).

A differential output has a higher dynamic range than a single-ended output because of the doubling of output voltage. The dynamic range is increased by 6dB as a result of the outputs being equal in magnitude but opposite in phase. As an example, a single-ended output with a  $1V_{PP}$  signal will be two  $1V_{PP}$  signals with a differential output. The increase is  $20\text{LOG}(2) = 6\text{dB}$ . Differential amplifiers are ideal for low voltage applications because of the increase in signal amplitude relative to a single-ended amplifier and the resulting improvement in SNR.

Differential amplifiers can also have reduced even order harmonics, all conditions equal, when compared to a single-ended amplifier. The differential output causes even harmonics to cancel between the two inverted outputs leaving only the odd harmonics. In practice even harmonics do not cancel completely, however there still is a reduction in total harmonic distortion.

### OUTPUT COMMON-MODE VOLTAGE ( $V_{OCM}$ pin)

The output common-mode voltage is the DC voltage on each output. The output common-mode voltage is set by the  $V_{OCM}$  pin. The  $V_{OCM}$  pin can be driven by a low impedance source. If no voltage is applied to the  $V_{OCM}$  pin, the DC common-mode output voltage will be set by the internal resistor divider to the midpoint of the voltages on the  $V_{CC}$  and  $V_{EE}$  pins. The input impedance of the  $V_{OCM}$  pin is  $50k\Omega$ . The  $V_{OCM}$  pin can be driven up to  $V_{CC} - 1.5V$  and  $V_{EE} + 1.5V$ . The  $V_{OCM}$  pin should be bypassed to ground with a  $0.1\mu F$  to  $1\mu F$  capacitor. The  $V_{OCM}$  pin should be connected to ground when the desired output common-mode voltage is ground reference. The value of the external capacitor has an effect on the PSRR performance of the LME49724. With the  $V_{OCM}$  pin only bypassed with a low value capacitor, the PSRR performance of the LME49724 will be reduced, especially at low audio frequencies. For best PSRR performance, the  $V_{OCM}$  pin should be connected to stable, clean reference. Increasing the value of the bypass capacitor on the  $V_{OCM}$  pin will also improve PSRR performance.

### ENABLE FUNCTION

The LME49724 can be placed into standby mode to reduce system current consumption by driving the ENABLE pin below  $V_{EE} + 1.75V$ . The LME49724 is active when the voltage on the ENABLE pin is above  $V_{EE} + 2.35V$ . The ENABLE pin should not be left floating. For best performance under all conditions, drive the ENABLE pin to the  $V_{EE}$  pin voltage to enter standby mode and to ground for active operation when operating from split supplies. When operating from a single supply, drive the ENABLE pin to ground for standby mode and to  $V_{CC}$  for active mode.

## FULLY DIFFERENTIAL OPERATION

The LME49724 performs best in a fully differential configuration. The circuit shown in Figure 50 is the typical fully differential configuration.

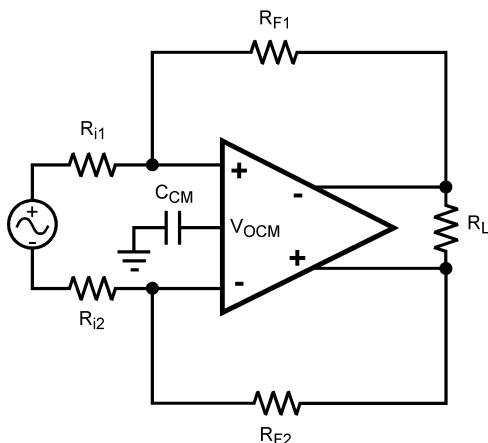


Figure 50. Fully Differential Configuration

The closed-loop gain is shown in Equation 1 below.

$$A_V = R_F / R_i \quad (V/V)$$

where

- $R_{F1} = R_{F2}$
  - $R_{i1} = R_{i2}$
  - Using low value resistors will give the lowest noise performance
- (1)

## SINGLE-ENDED TO DIFFERENTIAL CONVERSION

For many applications, it is required to convert a single-ended signal to a differential signal. The LME49724 can be used for a high performance, simple single-to-differential converter. Figure 51 shows the typical single-to-differential converter circuit configuration.

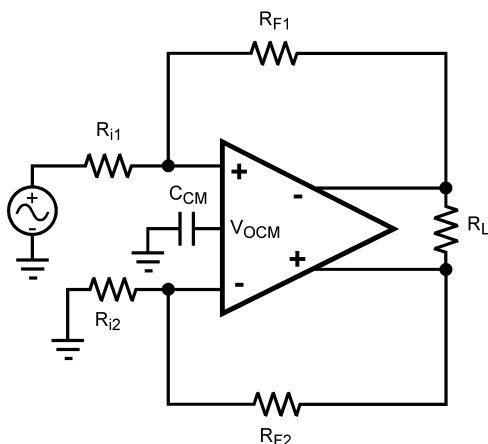


Figure 51. Single-Ended Input to Differential Output

## SINGLE SUPPLY OPERATION

The LME49724 can be operated from a single power supply, as shown in Figure 52. The supply voltage range is limited to a minimum of 5V and a maximum of 36V. The common-mode output DC voltage will be set to the midpoint of the supply voltage. The  $V_{OCM}$  pin can be used to adjust the common-mode output DC voltage on the outputs, as described previously, if the supply voltage midpoint is not the desired DC voltage.

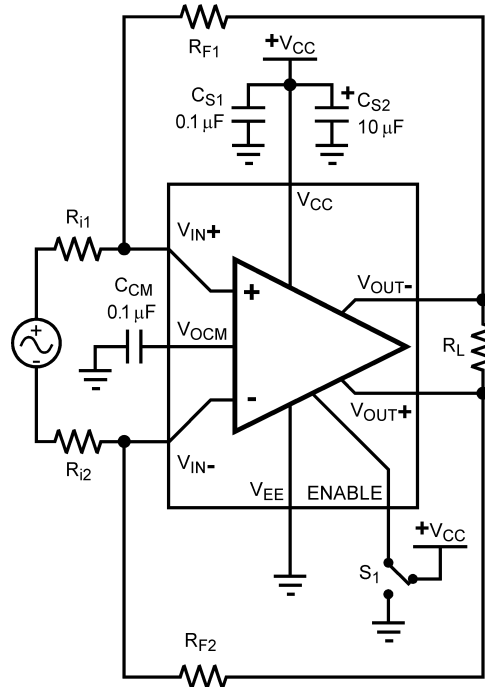


Figure 52. Single Supply Configuration

## DRIVING A CAPACITIVE LOAD

The LME49724 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

## THERMAL PCB DESIGN

The LME49724's high operating supply voltage along with its high output current capability can result in significant power dissipation. For this reason the LME49724 is provided in the exposed DAP SO PowerPad package for improved thermal dissipation performance compared to other surface mount packages. The exposed pad is designed to be soldered to a copper plane on the PCB which then acts as a heat sink. The thermal plane can be on any layer by using multiple thermal vias under and outside the IC package. The vias under the IC should have solder mask openings for the entire pad under the IC on the top layer but cover the vias on the bottom layer. This method prevents solder from being pulled away from the thermal vias during the reflow process resulting in optimum thermal conductivity.

Heat radiation from the PCB plane area is best accomplished when the thermal plane is on the top or bottom copper layers. The LME49724 should always be soldered down to a copper pad on the PCB for both optimum thermal performance as well as mechanical stability.

The exposed pad is for heat transfer and the thermal plane should either be electrically isolated or connected to the same potential as the  $V_{EE}$  pin. For high frequency applications ( $f > 1\text{MHz}$ ) or lower impedance loads, the pad should be connected to a plane that is connected to the  $V_{EE}$  potential.



## SUPPLY BYPASSING

The LME49724 should have its supply leads bypassed with low-inductance capacitors such as leadless surface mount (SMT) capacitors located as close as possible to the supply pins. It is recommended that a 10 $\mu$ F tantalum or electrolytic capacitor be placed in parallel with a 0.1 $\mu$ F ceramic or film type capacitor on each supply pin. These capacitors should be star routed with a dedicated ground return plane or large trace for best THD performance. Placing capacitors too far from the power supply pins, especially with thin connecting traces, can lead to excessive inductance, resulting in degraded high-frequency bypassing. Poor high-frequency bypassing can result in circuit instabilities. When using high bandwidth power supplies, the value and number of supply bypass capacitors should be reduced for optimal power supply performance.

## BALANCE CABLE DRIVER

With high peak-to-peak differential output voltage and plenty of low distortion drive current, the LME49724 makes an excellent balanced cable driver. Combining the single-to-differential configuration with a balanced cable driver results in a high performance single-ended input to balanced line driver solution.

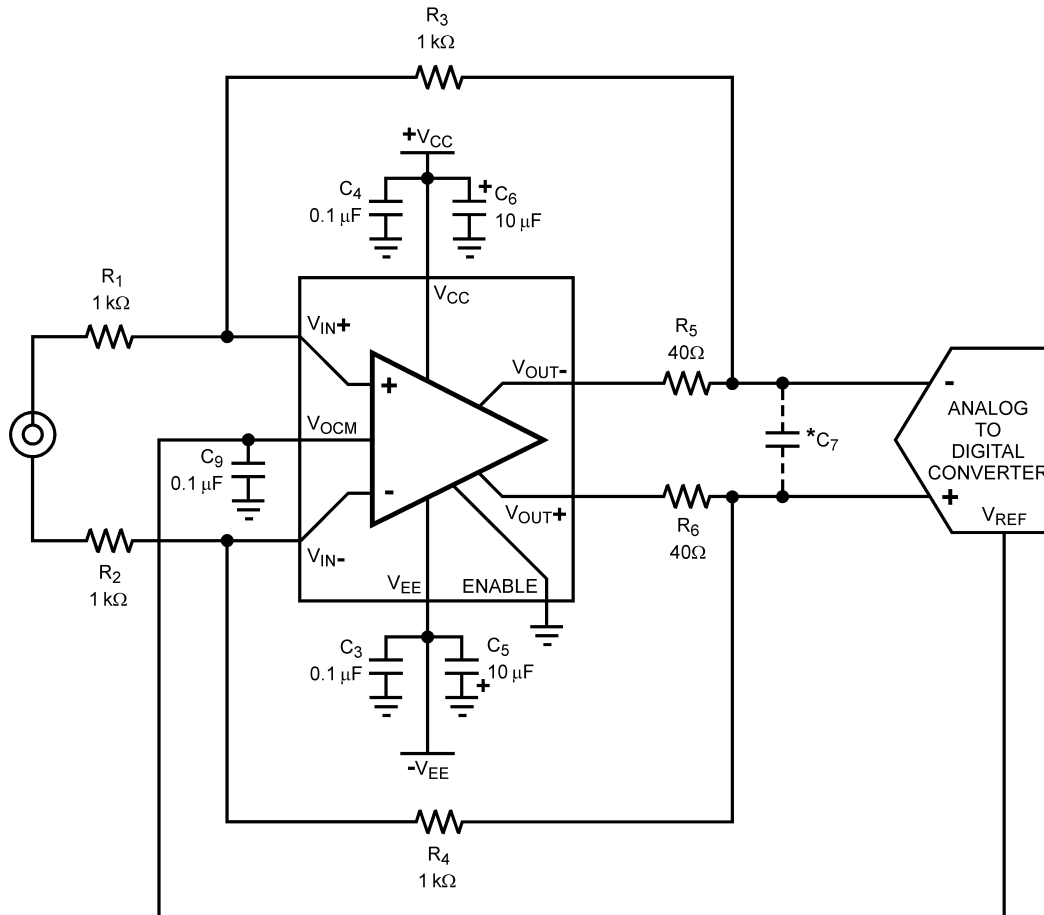
Although the LME49724 can drive capacitive loads up to 100pF, cable loads exceeding 100pF can cause instability. For such applications, series resistors are needed on the outputs before the capacitive load.

## ANALOG-TO-DIGITAL CONVERTER (ADC) APPLICATION

[Figure 53](#) is a typical fully differential application circuit for driving an analog-to-digital converter (ADC). The additional components of  $R_5$ ,  $R_6$ , and  $C_7$  are optional components and are for stability and proper ADC sampling. ADC's commonly use switched capacitor circuitry at the input. When the ADC samples the signal the current momentarily increases and may disturb the signal integrity at the sample point causing a signal glitch. Component  $C_7$  is significantly larger than the input capacitance of a typical ADC and acts as a charge reservoir greatly reducing the effect of the signal sample by the ADC. Resistors  $R_5$  and  $R_6$  decouple the capacitive load,  $C_7$ , for stability. The values shown are general values. Specific values should be optimized for the particular ADC loading requirements.

The output reference voltage from the ADC can be used to drive the  $V_{OCM}$  pin to set the common-mode DC voltage on the outputs of the LME49724. A buffer may be needed to drive the LME49724's  $V_{OCM}$  pin if the ADC cannot drive the 50k $\Omega$  input impedance of the  $V_{OCM}$  pin.

In order to minimize circuit distortion when using capacitors in the signal path, the capacitors should be comprised of either NPO ceramic, polystyrene, polypropylene or mica composition. Other types of capacitors may provide a reduced distortion performance but for a cost improvement, so capacitor selection is dependent upon design requirements. The performance/cost tradeoff for a specific application is left up to the user.



\* Value is application and converted dependent.

**Figure 53. Typical Analog-to-Digital Converter Circuit**

## DISTORTION MEASUREMENTS

The vanishing low residual distortion produced by the LME49724 is below the capabilities of commercially available equipment. This makes distortion measurements more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49724's low residual distortion is an input referred internal error. As shown in [Figure 54](#), adding a resistor connected between the amplifier's inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is increased. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced, which means that measurement resolution increases. To ensure minimum effects on distortion measurements, keep the value of  $R_5$  low. The distortion reading on the audio analyzer must be divided by a factor of  $(R_3 + R_4)/R_5$ , where  $R_1 = R_2$  and  $R_3 = R_4$ , to get the actual measured distortion of the device under test. The values used for the LME49724 measurements were  $R_1, R_2, R_3, R_4 = 1\text{ k}\Omega$  and  $R_5 = 20\Omega$ .

This technique is verified by duplicating the measurements with high closed-loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities.

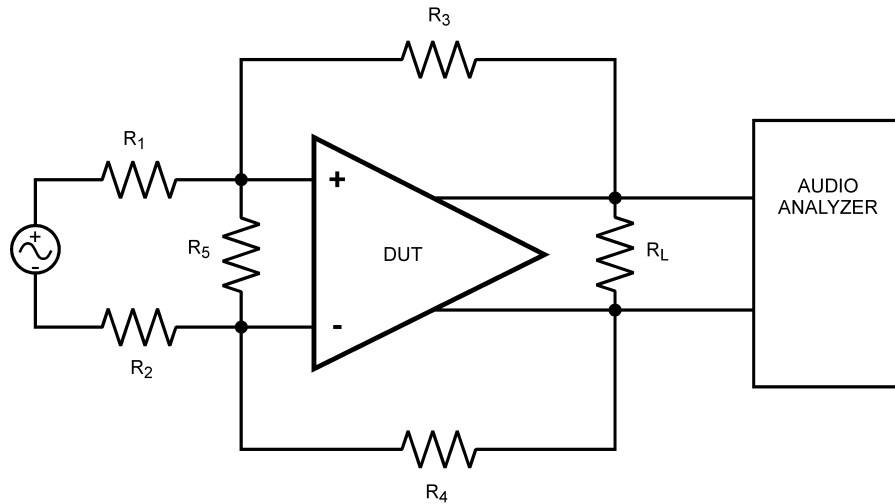


Figure 54. THD+N and IMD Distortion Test Circuit

### PERFORMANCE VARIATIONS

The LME49724 has excellent performance with little variation across different supply voltages, load impedances, and input configuration (single-ended or differential). Inspection of the THD+N vs Frequency and THD+N vs Output Voltage performance graphs (See [Typical Performance Characteristics](#) reveals only minimal differences with different load values. [Figure 55](#) and [Figure 56](#) below show the performance across different supply voltages with the same output signal level and load. [Figure 55](#) has plots at  $\pm 5V$ ,  $\pm 12V$ ,  $\pm 15V$ , and  $\pm 18V$  with a  $3V_{RMS}$  output while [Figure 56](#) has plots at  $\pm 12V$ ,  $\pm 15V$ , and  $\pm 18V$  with a  $10V_{RMS}$  output. Both figures use a  $600\Omega$  load. The performance for each different supply voltage under the same conditions is so similar it is nearly impossible to discern the different plots lines.

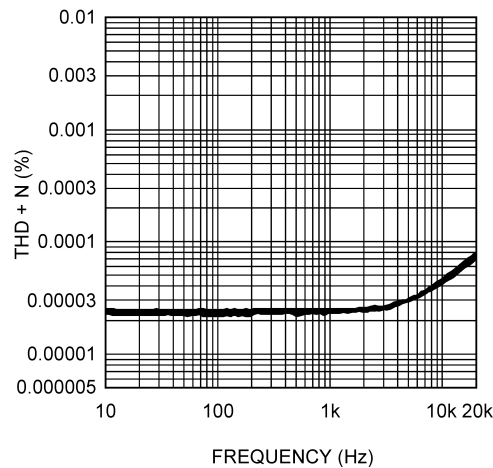
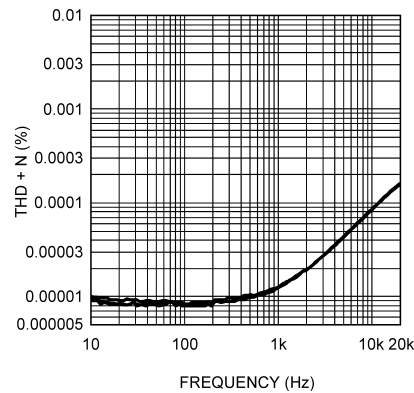
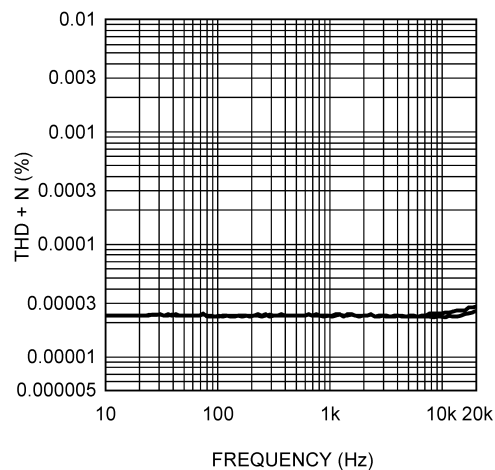


Figure 55. THD+N vs FREQUENCY with  $R_L = 600\Omega$   
 $V_{OUT} = 3V_{RMS}$ , Differential Input, 80kHz BW  
 $V_S = \pm 5V, \pm 12V, \pm 15V, \text{ and } \pm 18V$

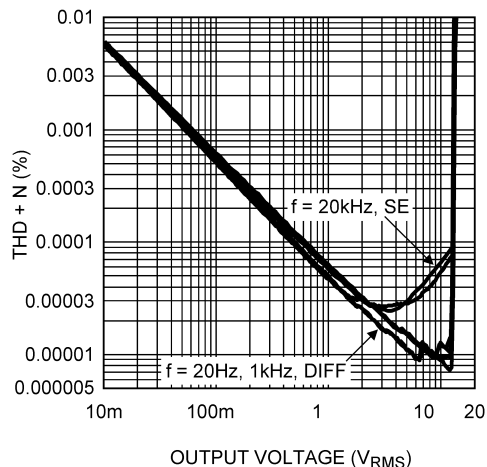


**Figure 56. THD+N vs FREQUENCY with  $R_L = 600\Omega$**   
 $V_{OUT} = 10V_{RMS}$ , Differential Input, 80kHz BW  
 $V_S = \pm 12V, \pm 15V, \text{ and } \pm 18V$

Whether the input configuration is single-ended or differential has only a minimal affect on THD+N performance at higher audio frequencies or higher signal levels. For easy comparison, [Figure 57](#) and [Figure 58](#) are a combination of the performance graphs found in [Typical Performance Characteristics](#).

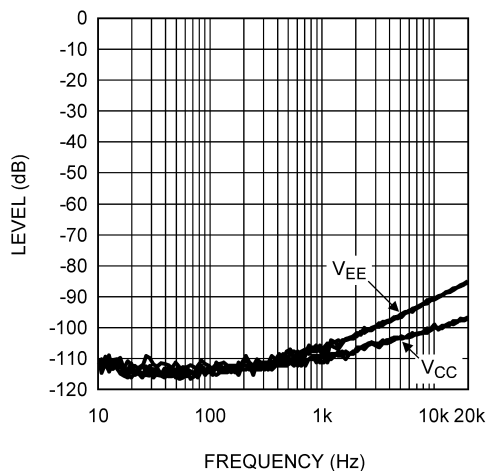


**Figure 57. THD+N vs FREQUENCY with  $R_L = 10k\Omega$**   
 $V_{OUT} = 3V_{RMS}$ ,  $V_S = \pm 15V$ , 80kHz BW  
 Single-ended and Differential Input

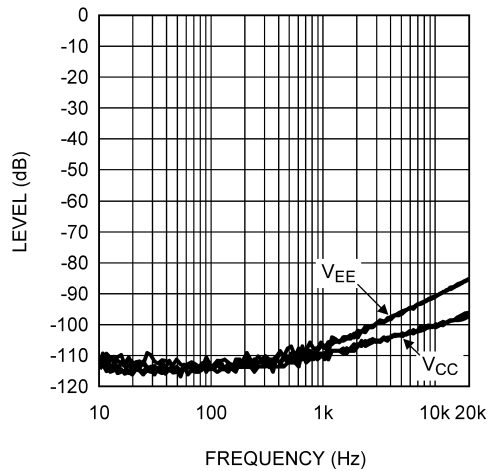


**Figure 58. THD+N vs OUTPUT VOLTAGE with  $R_L = 10k\Omega$   
 $f = 20\text{Hz}, 1\text{kHz}, 20\text{kHz}, V_S = \pm 15\text{V}, 80\text{kHz BW}$   
 Single-ended and Differential Input**

Power Supply Rejection Ratio does not vary with load value nor supply voltage. For easy comparison, [Figure 59](#) and [Figure 60](#) below are created by combining performance graphs found in [Typical Performance Characteristics](#).

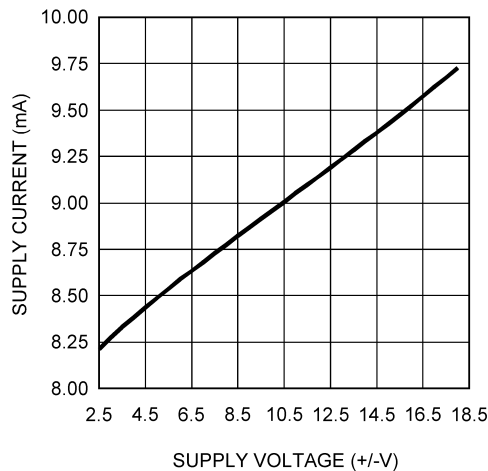


**Figure 59. PSRR vs FREQUENCY with  $R_L = 600\Omega$   
 $V_S = \pm 2.5\text{V}, \pm 15\text{V}, \text{ and } \pm 18\text{V}, 80\text{kHz BW}$**



**Figure 60. PSRR vs FREQUENCY with  $V_S = \pm 15V$   
 $R_L = 600\Omega, 2k\Omega, \text{ and } 10k\Omega, 80kHz \text{ BW}$**

Although supply current may not be a critical specification for many applications, there is also no real variation in supply current with no load or with a 600Ω load. This is a result of the extremely low offset voltage, typically less than 1mV. Figure 61 shows the supply current under the two conditions with no real difference discernable.



**Figure 61. Supply Current vs Supply Voltage  
 $R_L = \text{No Load and } 600\Omega$**

Demo Board Schematic

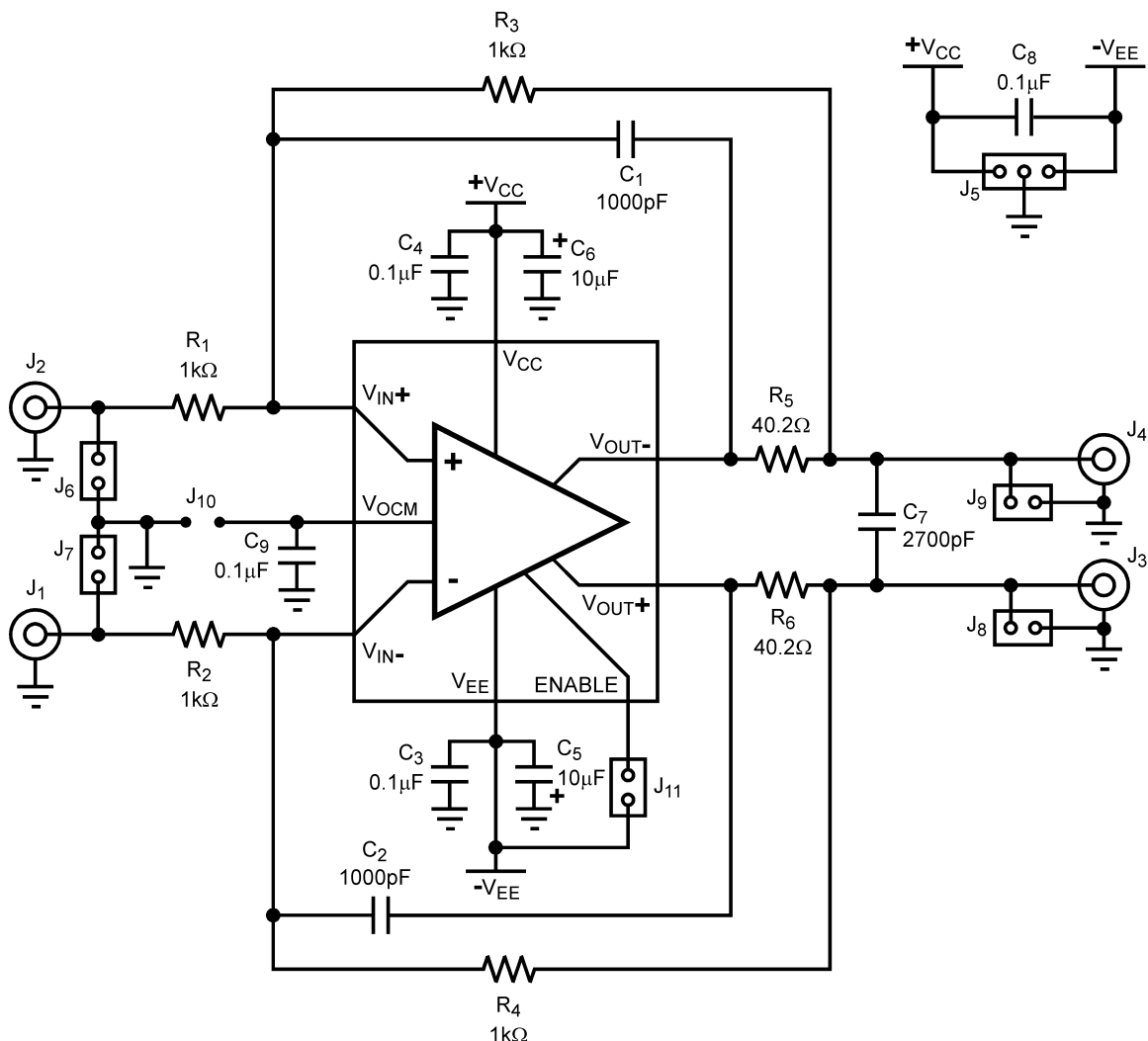


Figure 62. Demonstration Board Circuit

Build of Materials

Table 2. Reference Demo Board Bill of Materials

Designator	Value	Tolerance	Part Description	Comment
R <sub>1</sub> , R <sub>2</sub> , R <sub>3</sub> , R <sub>4</sub>	1kΩ	1%	1/8W, 0603 Resistor	
R <sub>5</sub> , R <sub>6</sub>	40.2Ω	1%	1/8W, 0603 Resistor	
C <sub>1</sub> , C <sub>2</sub>	1000pF	10%	0603, NPO Ceramic Capacitor, 50V	
C <sub>3</sub> , C <sub>4</sub> , C <sub>8</sub> , C <sub>9</sub>	0.1μF	-20%, +80%	0603, Y5V Ceramic Capacitor, 25V	
C <sub>5</sub> , C <sub>6</sub>	10μF	20%	Size C (6032), Tantalum Capacitor, 25V	
C <sub>7</sub>	2700pF	10%	0805, NPO Ceramic Capacitor, 50V	
U <sub>1</sub>			LME49724MR	
J <sub>1</sub> , J <sub>2</sub> , J <sub>3</sub> , J <sub>4</sub>			SMA coaxial connector	Inputs & Outputs
J <sub>5</sub>			0.100" 1x3 header, vertical mount	V <sub>DD</sub> , V <sub>EE</sub> , GND
J <sub>6</sub> , J <sub>7</sub> , J <sub>8</sub> , J <sub>9</sub> , J <sub>10</sub> , J <sub>11</sub>			0.100" 1x2 header, vertical mount	Inputs, Outputs, V <sub>OCM</sub> , Enable

### REVISION HISTORY

Rev	Date	Description
1.0	11/12/08	Initial release.
A	04/04/13	Changed layout of National Data Sheet to TI format.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49724MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L49724 MR	<a href="#">Samples</a>
LME49724MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L49724 MR	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49724MRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**





\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49724MRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49724MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L49724 MR	
LME49724MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L49724 MR	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

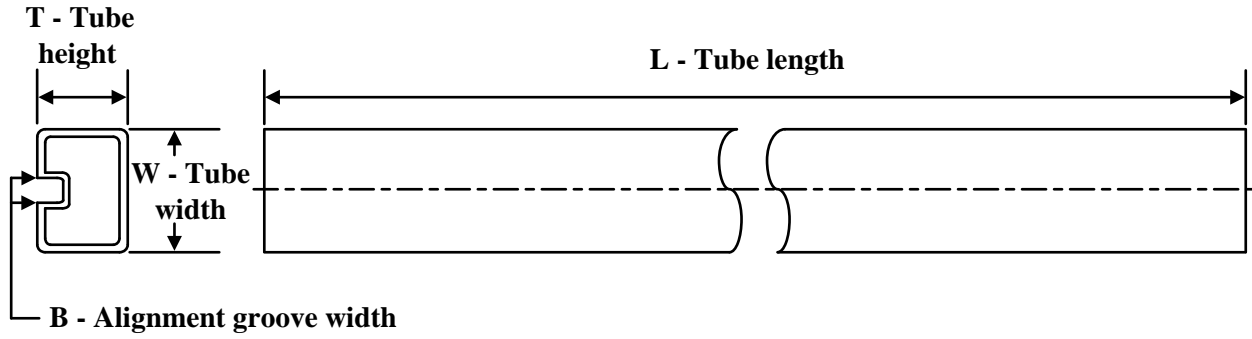
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49724MRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49724MRX/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LME49724MR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05

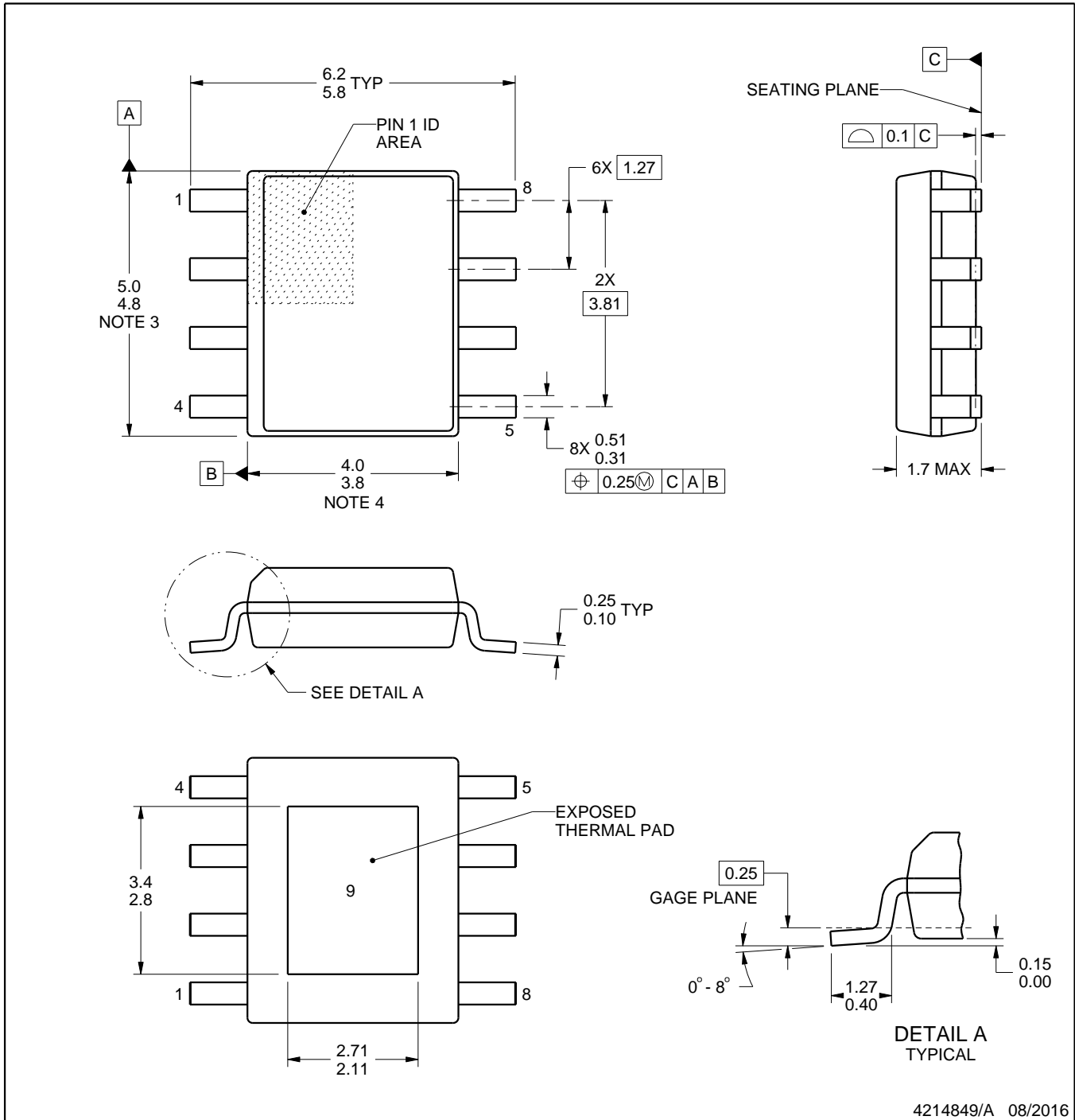
# DDA0008B



# PACKAGE OUTLINE

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



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**NOTES:**

PowerPAD is a trademark of Texas Instruments.

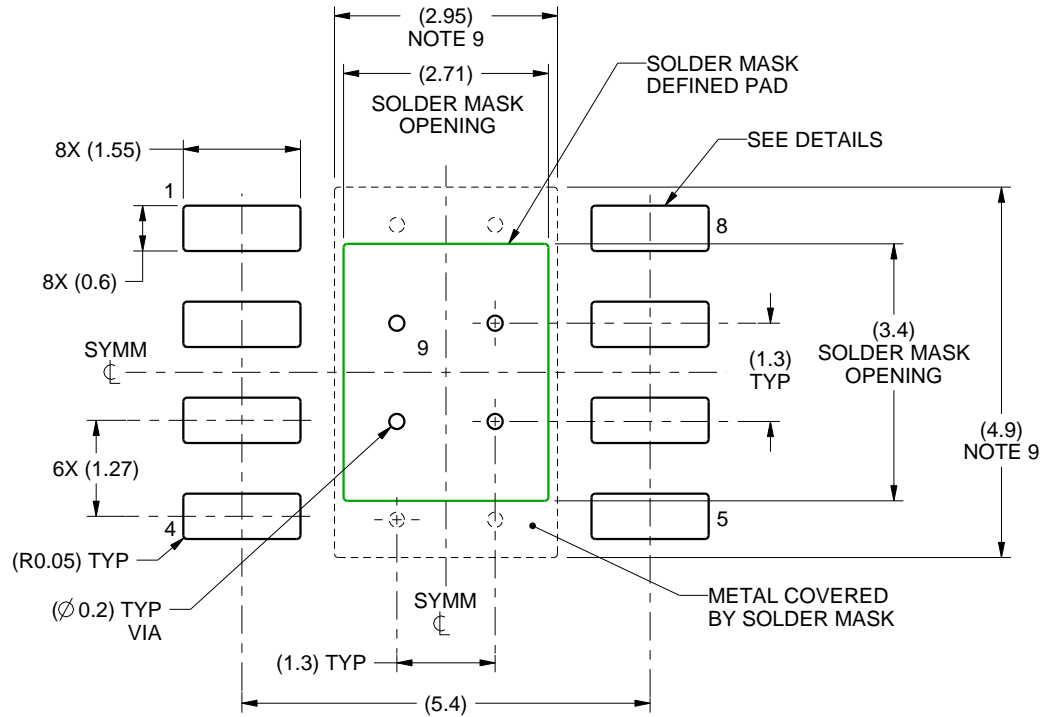
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

# EXAMPLE BOARD LAYOUT

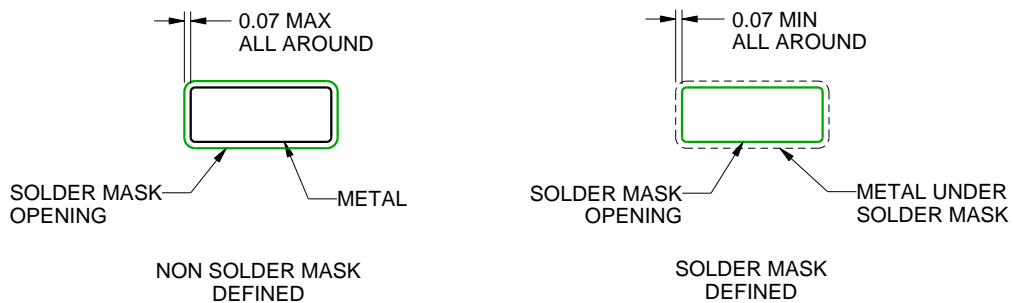
DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
PADS 1-8

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
 EXPOSED PAD  
 100% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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