

## LMH6321 具有可调节电流限制的 300 mA 高速缓冲器

### 1 特性

- 高压摆率 1800V/ $\mu$ s
- 高带宽 110MHz
- 持续输出电流  $\pm 300$ mA
- 输出电流限制容差  $\pm 5$ mA  $\pm 5$ %
- 宽电源电压范围 5V 至  $\pm 15$ V
- 宽温度范围  $-40^{\circ}\text{C}$  至  $+125^{\circ}\text{C}$
- 可调节电流限制
- 高容性负载驱动
- 热关断错误标志

### 2 应用

- 线路驱动器
- 引脚驱动器
- 声纳驱动器
- 电机控制

### 3 描述

LMH6321 是一种高速单位增益缓冲器，其压摆率为 1800V/ $\mu$ s，在驱动 50 $\Omega$  负载时具有 110MHz 的低信号带宽。它可以连续驱动  $\pm 300$ mA，在驱动大容性负载时不会振荡。

LMH6321 具有可调电流限制。电流限制可在 10mA 至 300mA 范围内以  $\pm 5$ mA  $\pm 5$ % 的精度连续调节。可使用电阻器调整外部基准电流，从而设置电流限制。通过将电阻器连接到 DAC 以形成基准电流，可以根据需要轻松、即时地调整电流。拉电流和灌电流具有共同的电流限制。

LMH6321 采用节省空间的 8 引脚 SO PowerPAD 或 7 引脚 DDPAK 电源封装。SO PowerPAD™ 封装在封装的底部具有裸焊盘以提高其散热能力。LMH6321 可用于运算放大器的反馈环路内以提高电流输出，或用作独立缓冲器。

表 3-1. 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 (标称值)
LMH6321	SO PowerPAD (8)	1.7 mm × 1.27 mm
	DDPAK (7)	4.65 mm × 1.27 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

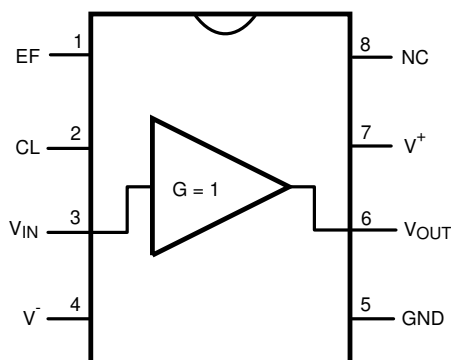
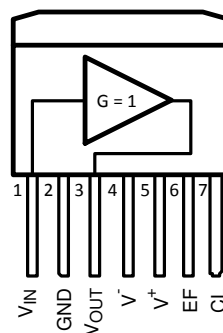


图 3-1. 连接图：8 引脚 SO PowerPAD



A. V<sup>-</sup> 引脚连接到每个封装背面的凸片上。

图 3-2. 连接图：7 引脚 DDPAK(A)



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision C (March 2013) to Revision D (September 2021)</b>	<b>Page</b>
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 添加了 <i>器件信息表</i> .....	1
• Removed the Thermal Resistance ( $\theta_{JA}$ ), ( $\theta_{JC}$ ), and SO PowerPAD Package details from the <i>Operating Ratings</i> table.....	3
• Added the <i>Thermal Information</i> section.....	3
• Added the <i>Device and Documentation Support</i> sections.....	26
• Added the <i>Mechanical, Packaging, and Orderable Information</i> section.....	26

<b>Changes from Revision B (March 2013) to Revision C (March 2013)</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format.....	24

## 5 Specifications

### 5.1 Absolute Maximum Ratings

See (1) (2)

ESD Tolerance (3)	Human Body Model	2.5 kV
	Machine Model	250 V
Supply Voltage		36 V (±18 V)
Input to Output Voltage (4)		±5 V
Input Voltage		±V <sub>SUPPLY</sub>
Output Short-Circuit to GND (5)		Continuous
Storage Temperature Range		-65°C to +150°C
Junction Temperature (T <sub>JMAX</sub> )		+150°C
Lead Temperature (Soldering, 10 seconds)		260°C
Power Dissipation		(6)
C <sub>L</sub> Pin to GND Voltage		±1.2 V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications and the test conditions, see the Electrical Characteristics Table.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0 Ω in series with 200 pF.
- (4) If the input-output voltage differential exceeds ±5 V, internal clamping diodes will turn on. The current through these diodes should be limited to 5 mA max. Thus for an input voltage of ±15 V and the output shorted to ground, a minimum of 2 kΩ should be placed in series with the input.
- (5) The maximum continuous current must be limited to 300 mA. See 节 6 for more details.
- (6) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. See 节 6.8 of 节 6.

### 5.2 Operating Ratings

Operating Temperature Range	-40°C to +125°C
Operating Supply Range	5 V to ±16 V

### 5.3 Thermal Information

THERMAL METRIC <sup>1</sup>		LMH6321		UNIT
		DDA SO Power Pad	DDAPAK	
		8 Pins	7 Pins	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	37.8	21.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	51.6	34.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	11.7	6.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.5	3.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	11.7	6.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.6	1.1	°C/W

## 5.4 ±15 V Electrical Characteristics

The following specifications apply for Supply Voltage = ±15 V,  $V_{CM} = 0$ ,  $R_L \geq 100 \text{ k}\Omega$  and  $R_S = 50 \text{ }\Omega$ ,  $C_L$  open, unless otherwise noted. *Italicized* limits apply for  $T_A = T_J = T_{MIN}$  to  $T_{MAX}$ ; all other limits  $T_A = T_J = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$A_V$	Voltage Gain	$R_L = 1 \text{ k}\Omega$ , $V_{IN} = \pm 10 \text{ V}$	0.99 <i>0.98</i>	0.995		V/V
		$R_L = 50 \text{ }\Omega$ , $V_{IN} = \pm 10 \text{ V}$	0.86 <i>0.84</i>	0.92		V/V
$V_{OS}$	Input Offset Voltage	$R_L = 1 \text{ k}\Omega$ , $R_S = 0 \text{ V}$		±4	±35 ±52	mV
$I_B$	Input Bias Current	$V_{IN} = 0 \text{ V}$ , $R_L = 1 \text{ k}\Omega$ , $R_S = 0 \text{ V}$		±2	±15 ±17	μA
$R_{IN}$	Input Resistance	$R_L = 50 \text{ }\Omega$		250		kΩ
$C_{IN}$	Input Capacitance			3.5		pF
$R_O$	Output Resistance	$I_O = \pm 10 \text{ mA}$		5		Ω
$I_S$	Power Supply Current	$R_L = \infty$ , $V_{IN} = 0$		11	14.5 16.5	mA
		750 μA into $C_L$ Pin		14.9	18.5 20.5	
$V_{O1}$	Positive Output Swing	$I_O = 300 \text{ mA}$ , $R_S = 0 \text{ V}$ , $V_{IN} = \pm V_S$	11.2 10.8	11.9		V
	Negative Output Swing	$I_O = 300 \text{ mA}$ , $R_S = 0 \text{ V}$ , $V_{IN} = \pm V_S$		-11.3	-10.3 -9.8	
$V_{O2}$	Positive Output Swing	$R_L = 1 \text{ k}\Omega$ , $R_S = 0 \text{ V}$ , $V_{IN} = \pm V_S$	13.1 12.9	13.4		V
	Negative Output Swing	$R_L = 1 \text{ k}\Omega$ , $R_S = 0 \text{ V}$ , $V_{IN} = \pm V_S$		-13.4	-12.9 -12.6	
$V_{O3}$	Positive Output Swing	$R_L = 50 \text{ }\Omega$ , $R_S = 0 \text{ V}$ , $V_{IN} = \pm V_S$	11.6 11.2	12.2		V
	Negative Output Swing	$R_L = 50 \text{ }\Omega$ , $R_S = 0 \text{ V}$ , $V_{IN} = \pm V_S$		-11.9	-10.9 -10.6	
$V_{EF}$	Error Flag Output Voltage	$R_L = \infty$ , $V_{IN} = 0$ , EF pulled up with 5 kΩ to +5 V	Normal	5.00		V
			During Thermal Shutdown	0.25		
$T_{SH}$	Thermal Shutdown Temperature	Measure Quantity is Die (Junction) Temperature		168		°C
		Hysteresis		10		
$I_{SH}$	Supply Current at Thermal Shutdown	EF pulled up with 5 kΩ to +5 V		3		mA
PSSR	Power Supply Rejection Ratio	$R_L = 1 \text{ k}\Omega$ , $V_{IN} = 0 \text{ V}$ , $V_S = \pm 5 \text{ V}$ to $\pm 15 \text{ V}$	Positive	58 54	66	dB
			Negative	58 54	64	
SR	Slew Rate	$V_{IN} = \pm 11 \text{ V}$ , $R_L = 1 \text{ k}\Omega$		2900		V/μs
		$V_{IN} = \pm 11 \text{ V}$ , $R_L = 50 \text{ }\Omega$		1800		
BW	-3 dB Bandwidth	$V_{IN} = \pm 20 \text{ mV}_{PP}$ , $R_L = 50 \text{ }\Omega$		110		MHz
LSBW	Large Signal Bandwidth	$V_{IN} = 2 \text{ V}_{PP}$ , $R_L = 50 \text{ }\Omega$		48		MHz

## 5.4 ±15 V Electrical Characteristics (continued)

The following specifications apply for Supply Voltage = ±15 V,  $V_{CM} = 0$ ,  $R_L \geq 100 \text{ k}\Omega$  and  $R_S = 50 \Omega$ ,  $C_L$  open, unless otherwise noted. *Italicized* limits apply for  $T_A = T_J = T_{MIN}$  to  $T_{MAX}$ ; all other limits  $T_A = T_J = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
HD2	2 <sup>nd</sup> Harmonic Distortion	$V_O = 2 V_{PP}$ , $f = 100 \text{ kHz}$	$R_L = 50 \Omega$	-59		dBc	
			$R_L = 100 \Omega$	-70			
		$V_O = 2 V_{PP}$ , $f = 1 \text{ MHz}$	$R_L = 50 \Omega$	-57			
			$R_L = 100 \Omega$	-68			
HD3	3rd Harmonic Distortion	$V_O = 2 V_{PP}$ , $f = 100 \text{ kHz}$	$R_L = 50 \Omega$	-59		dBc	
			$R_L = 100 \Omega$	-70			
		$V_O = 2 V_{PP}$ , $f = 1 \text{ MHz}$	$R_L = 50 \Omega$	-62			
			$R_L = 100 \Omega$	-73			
$e_n$	Input Voltage Noise	$f \geq 10 \text{ kHz}$		2.8		nV/√Hz	
$i_n$	Input Current Noise	$f \geq 10 \text{ kHz}$		2.4		pA/√Hz	
$I_{SC1}$	Output Short Circuit Current Source <sup>(1)</sup>	$V_O = 0 \text{ V}$ , Program Current into $C_L = 25 \mu\text{A}$	Sourcing $V_{IN} = +3 \text{ V}$	4.5 4.5	10	15.5 15.5	mA
			Sinking $V_{IN} = -3 \text{ V}$	4.5 4.5	10	15.5 15.5	
		$V_O = 0 \text{ V}$ Program Current into $C_L = 750 \mu\text{A}$	Sourcing $V_{IN} = +3 \text{ V}$	280 273	295	308 325	mA
			Sinking $V_{IN} = -3 \text{ V}$	280 275	295	310 325	
$I_{SC2}$	Output Short Circuit Current Source	$R_S = 0 \text{ V}$ , $V_{IN} = +3 \text{ V}$ <sup>(1) (2)</sup>	320 300	570	750 920	mA	
	Output Short Circuit Current Sink	$R_S = 0 \text{ V}$ , $V_{IN} = -3 \text{ V}$ <sup>(1) (2)</sup>	300 305	515	750 910		
<i>V/I Section</i>							
$CLV_{OS}$	Current Limit Input Offset Voltage	$R_L = 1 \text{ k}\Omega$ , $GND = 0 \text{ V}$		±0.5	±4.0 ±8.0	mV	
$CL_{IB}$	Current Limit Input Bias Current	$R_L = 1 \text{ k}\Omega$	-0.5 -0.8	-0.2		μA	
$CL_{CMRR}$	Current Limit Common Mode Rejection Ratio	$R_L = 1 \text{ k}\Omega$ , $GND = -13 \text{ to } +14 \text{ V}$	60 56	69		dB	

(1)  $V_{IN} = +$  or  $-4 \text{ V}$  at  $T_J = -40^\circ\text{C}$ .

(2) For the condition where the  $C_L$  pin is left open the output current should not be continuous, but instead, should be limited to low duty cycle pulse mode such that the RMS output current is less than or equal to 300 mA.

## 5.5 ±5 V Electrical Characteristics

The following specifications apply for Supply Voltage = ±5 V,  $V_{CM} = 0$ ,  $R_L \geq 100 \text{ k}\Omega$  and  $R_S = 50 \Omega$ ,  $C_L$  Open, unless otherwise noted. *Italicized* limits apply for  $T_A = T_J = T_{MIN}$  to  $T_{MAX}$ ; all other limits  $T_A = T_J = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$A_V$	Voltage Gain	$R_L = 1 \text{ k}\Omega$ , $V_{IN} = \pm 3 \text{ V}$	0.99 0.98	0.994		V/V
		$R_L = 50 \Omega$ , $V_{IN} = \pm 3 \text{ V}$	0.86 0.84	0.92		
$V_{OS}$	Offset Voltage	$R_L = 1 \text{ k}\Omega$ , $R_S = 0 \text{ V}$		±2.5	±35 ±50	mV
$I_B$	Input Bias Current	$V_{IN} = 0 \text{ V}$ , $R_L = 1 \text{ k}\Omega$ , $R_S = 0 \text{ V}$		±2	±15 ±17	μA
$R_{IN}$	Input Resistance	$R_L = 50 \Omega$		250		kΩ
$C_{IN}$	Input Capacitance			3.5		pF

## 5.5 $\pm 5$ V Electrical Characteristics (continued)

The following specifications apply for Supply Voltage =  $\pm 5$  V,  $V_{CM} = 0$ ,  $R_L \geq 100 \text{ k}\Omega$  and  $R_S = 50 \text{ }\Omega$ ,  $C_L$  Open, unless otherwise noted. *Italicized* limits apply for  $T_A = T_J = T_{MIN}$  to  $T_{MAX}$ ; all other limits  $T_A = T_J = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
$R_O$	Output Resistance	$I_{OUT} = \pm 10 \text{ mA}$		5		$\Omega$	
$I_S$	Power Supply Current	$R_L = \infty$ , $V_{IN} = 0 \text{ V}$		10	13.5 14.7	mA	
		750 $\mu\text{A}$ into CL Pin		14	17.5 19.5		
$V_{O1}$	Positive Output Swing	$I_O = 300 \text{ mA}$ , $R_S = 0 \text{ V}$ , $V_{IN} = \pm V_S$	1.3 0.9	1.9		V	
	Negative Output Swing	$I_O = 300 \text{ mA}$ , $R_S = 0 \text{ V}$ , $V_{IN} = \pm V_S$		-1.3	-0.5 -0.1		
$V_{O2}$	Positive Output Swing	$R_L = 1 \text{ k}\Omega$ , $R_S = 0 \text{ V}$ , $V_{IN} = \pm V_S$	3.2 2.9	3.5		V	
	Negative Output Swing	$R_L = 1 \text{ k}\Omega$ , $R_S = 0 \text{ V}$ , $V_{IN} = \pm V_S$		-3.5	-3.1 -2.9	V	
$V_{O3}$	Positive Output Swing	$R_L = 50 \text{ }\Omega$ , $R_S = 0 \text{ V}$ , $V_{IN} = \pm V_S$	2.8 2.5	3.1		V	
	Negative Output Swing	$R_L = 50 \text{ }\Omega$ , $R_S = 0 \text{ V}$ , $V_{IN} = \pm V_S$		-3.0	-2.6 -2.4	V	
PSSR	Power Supply Rejection Ratio	$R_L = 1 \text{ k}\Omega$ , $V_{IN} = 0$ , $V_S = \pm 5 \text{ V}$ to $\pm 15 \text{ V}$	Positive	58 54	66		dB
			Negative	58 54	64		
$I_{SC1}$	Output Short Circuit Current	$V_O = 0 \text{ V}$ , Program Current into $C_L = 25 \text{ }\mu\text{A}$	Sourcing $V_{IN} = +3 \text{ V}$	4.5 4.5	9	14.0 15.5	mA
			Sinking $V_{IN} = -3 \text{ V}$	4.5 4.5	9	14.0 15.5	
		$V_O = 0 \text{ V}$ , Program Current into $C_L = 750 \text{ }\mu\text{A}$	Sourcing $V_{IN} = +3 \text{ V}$	275 270	290	305 320	
			Sinking $V_{IN} = -3 \text{ V}$	275 270	290	310 320	
$I_{SC2}$	Output Short Circuit Current Source	$R_S = 0 \text{ V}$ , $V_{IN} = +3 \text{ V}$ 1 2	300	470		mA	
	Output Short Circuit Current Sink	$R_S = 0 \text{ V}$ , $V_{IN} = -3 \text{ V}$ 1 2	300	400			
SR	Slew Rate	$V_{IN} = \pm 2 V_{PP}$ , $R_L = 1 \text{ k}\Omega$		450		V/ $\mu\text{s}$	
		$V_{IN} = \pm 2 V_{PP}$ , $R_L = 50 \text{ }\Omega$		210			
BW	-3 dB Bandwidth	$V_{IN} = \pm 20 \text{ mV}_{PP}$ , $R_L = 50 \text{ }\Omega$		90		MHz	
LSBW	Large Signal Bandwidth	$V_{IN} = 2 V_{PP}$ , $R_L = 50 \text{ }\Omega$		39		MHz	
$T_{SD}$	Thermal Shutdown	Temperature		170		$^\circ\text{C}$	
		Hysteresis		10			
<i>V/I Section</i>							
$CLV_{OS}$	Current Limit Input Offset Voltage	$R_L = 1 \text{ k}\Omega$ , $GND = 0 \text{ V}$		2.7	+5 $\pm 5.0$	mV	
$CLI_B$	Current Limit Input Bias Current	$R_L = 1 \text{ k}\Omega$ , $C_L = 0 \text{ V}$	-0.5 -0.6	-0.2		$\mu\text{A}$	
CL CMRR	Current Limit Common Mode Rejection Ratio	$R_L = 1 \text{ k}\Omega$ , $GND = -3 \text{ V}$ to $+4 \text{ V}$	60 56	65		dB	

1.  $V_{IN} = +$  or  $-4 \text{ V}$  at  $T_J = -40^\circ\text{C}$ .

2. For the condition where the  $C_L$  pin is left open the output current should not be continuous, but instead, should be limited to low duty cycle pulse mode such that the RMS output current is less than or equal to 300 mA.

### 5.6 Typical Characteristics

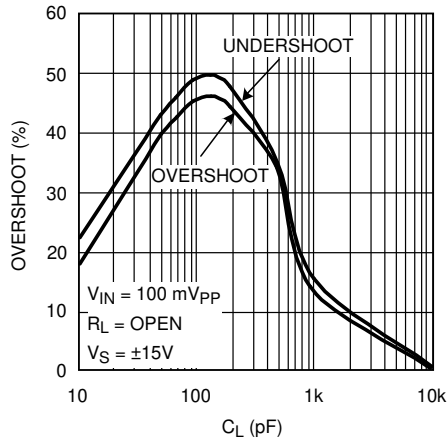


图 5-1. Overshoot vs. Capacitive Load

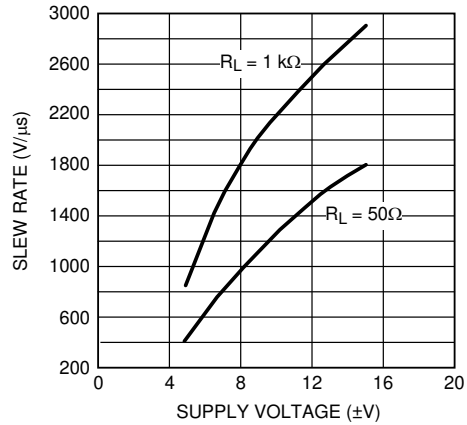


图 5-2. Slew Rate

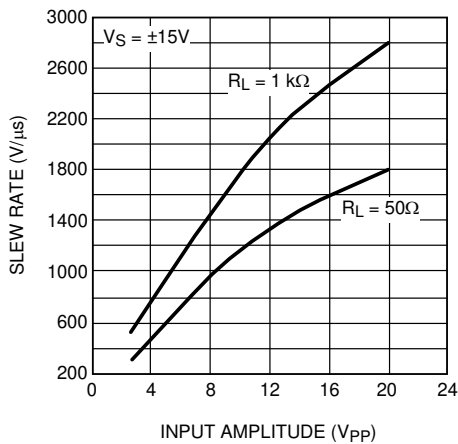


图 5-3. Slew Rate

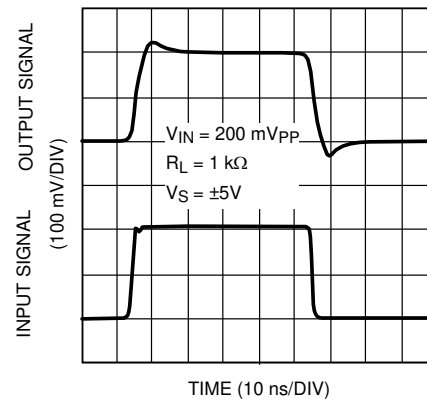


图 5-4. Small Signal Step Response

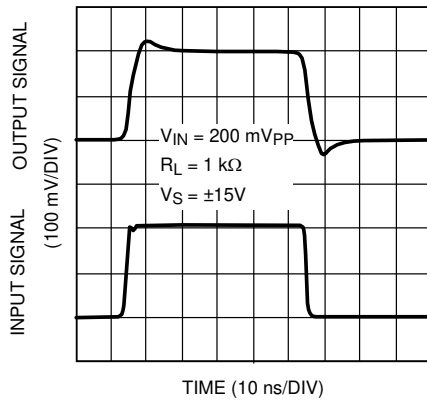


图 5-5. Small Signal Step Response

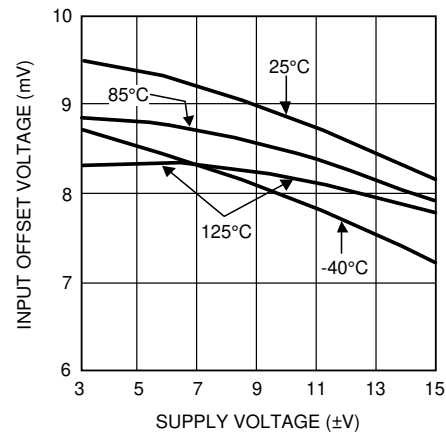


图 5-6. Input Offset Voltage of Amplifier vs. Supply Voltage



## 5.6 Typical Characteristics (continued)

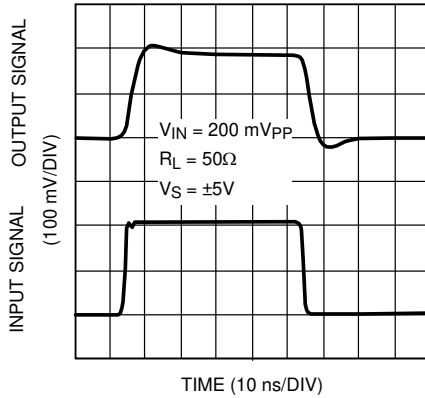


图 5-7. Small Signal Step Response

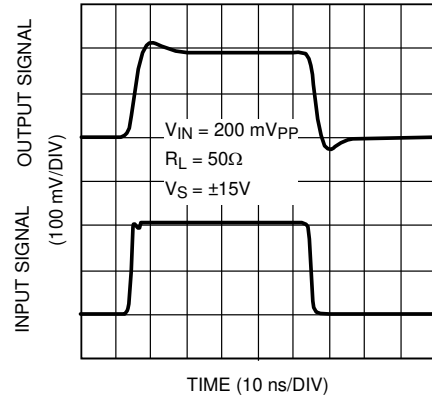


图 5-8. Small Signal Step Response

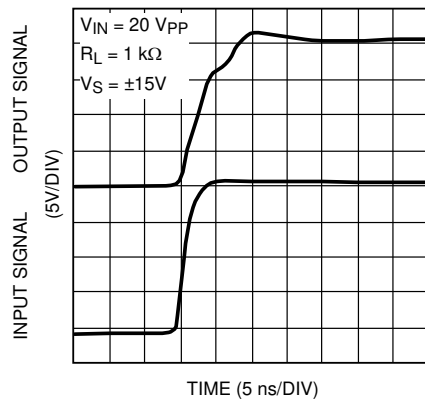


图 5-9. Large Signal Step Response—Leading Edge

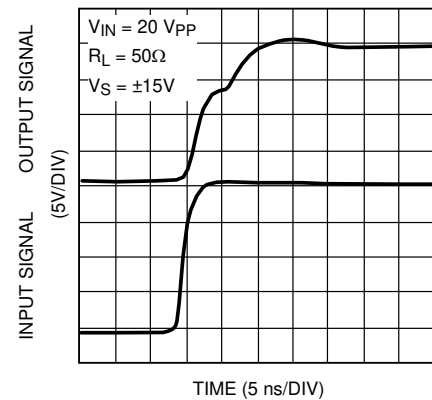


图 5-10. Large Signal Step Response — Leading Edge

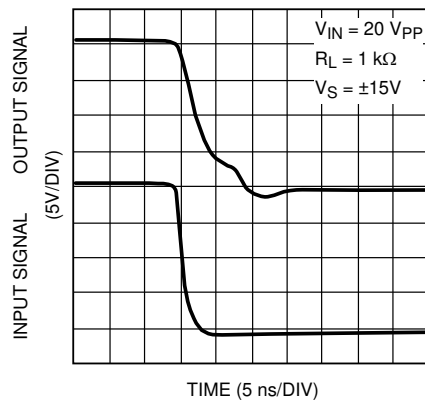


图 5-11. Large Signal Step Response — Trailing Edge

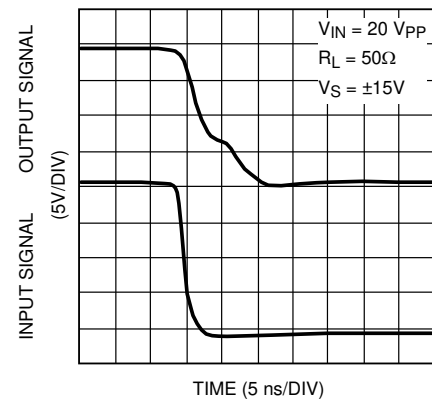


图 5-12. Large Signal Step Response — Trailing Edge

### 5.6 Typical Characteristics (continued)

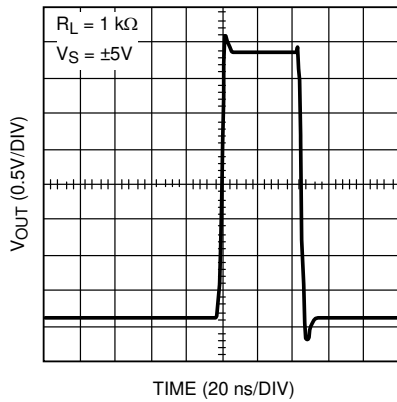


图 5-13. Large Signal Step Response

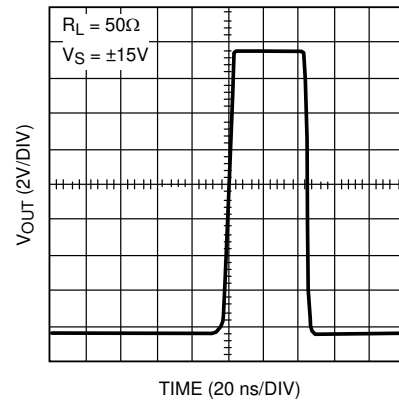


图 5-14. Large Signal Step Response

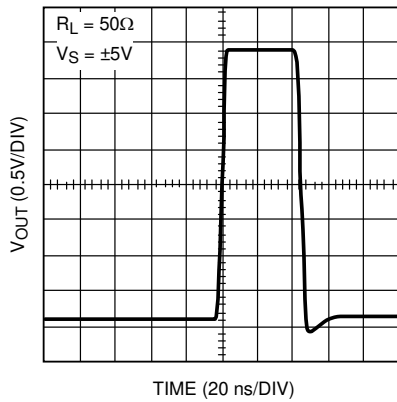


图 5-15. Large Signal Step Response

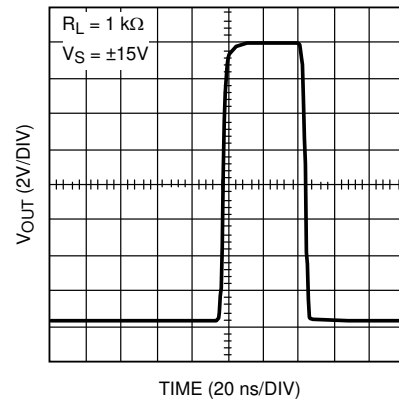


图 5-16. Large Signal Step Response

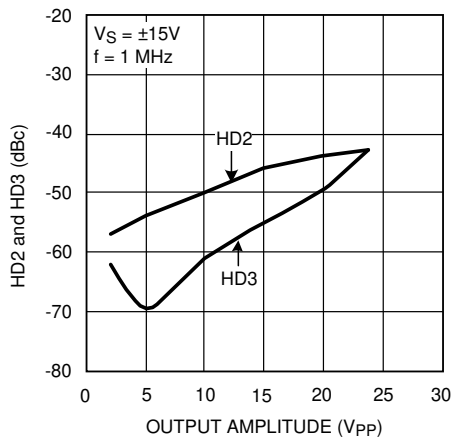


图 5-17. Harmonic Distortion with 50 Ω Load

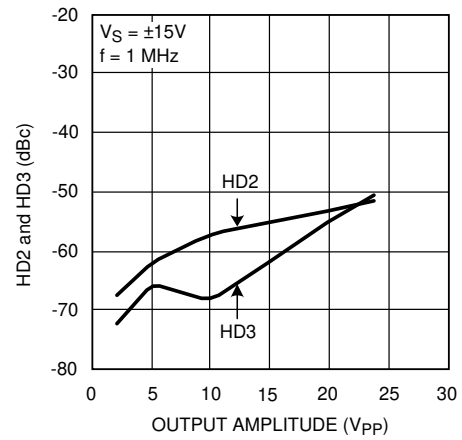


图 5-18. Harmonic Distortion with 100 Ω Load

### 5.6 Typical Characteristics (continued)

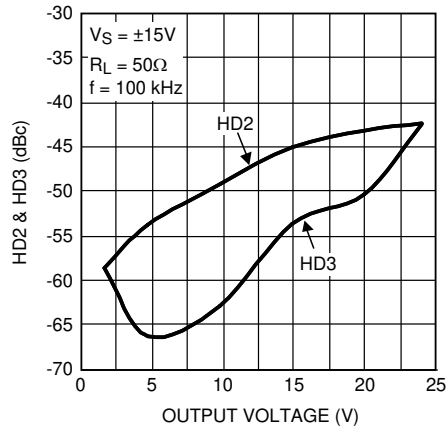


图 5-19. Harmonic Distortion with 50 Ω Load

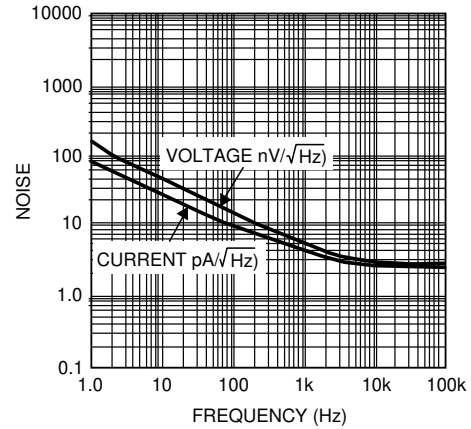


图 5-20. Noise vs. Frequency

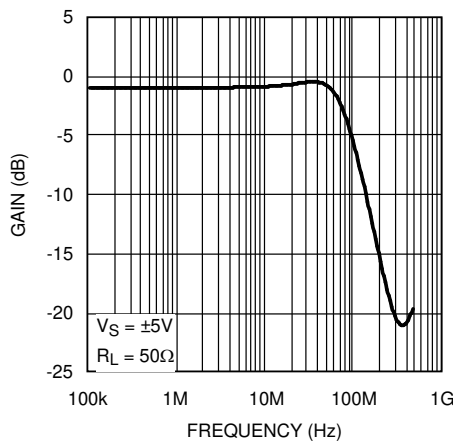


图 5-21. Gain vs. Frequency

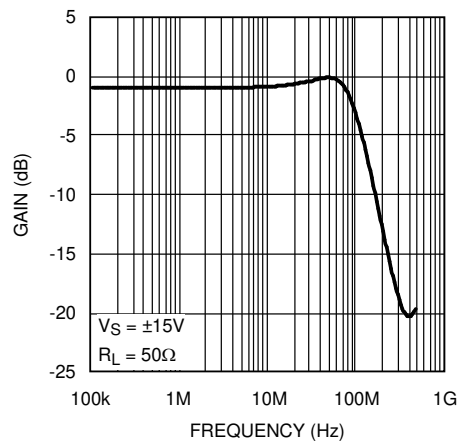


图 5-22. Gain vs. Frequency

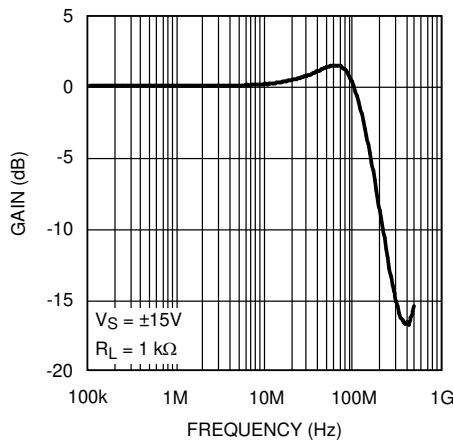


图 5-23. Gain vs. Frequency

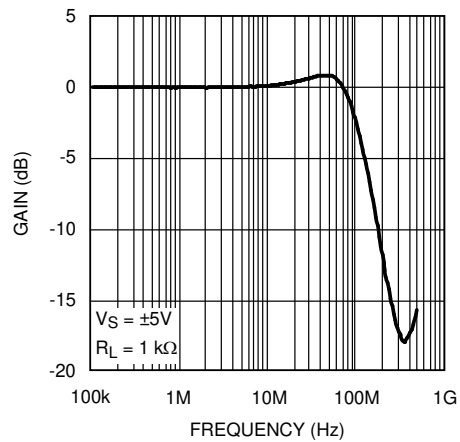


图 5-24. Gain vs. Frequency

### 5.6 Typical Characteristics (continued)

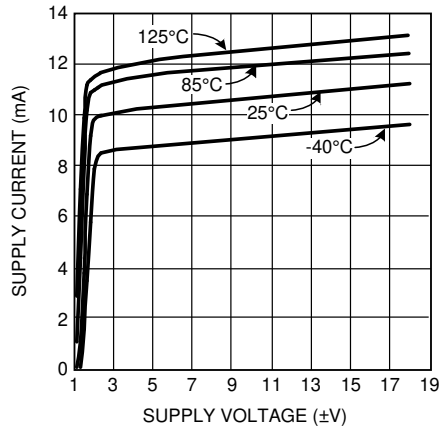


图 5-25. Supply Current vs. Supply Voltage

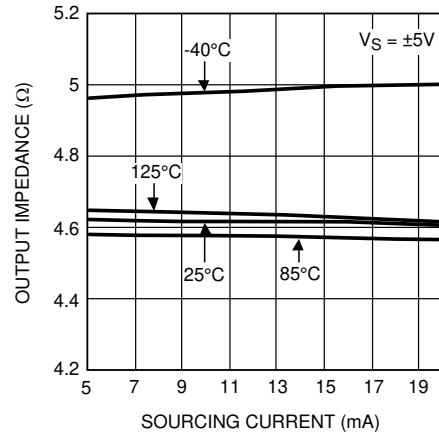


图 5-26. Output Impedance vs. Sourcing Current

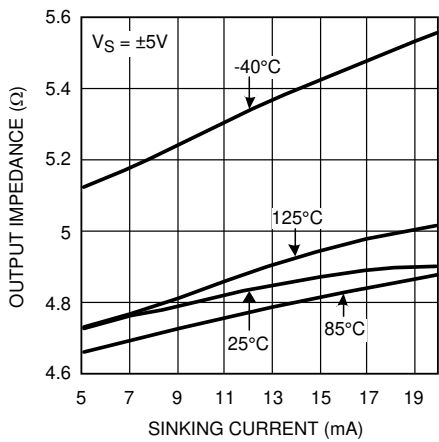


图 5-27. Output Impedance vs. Sinking Current

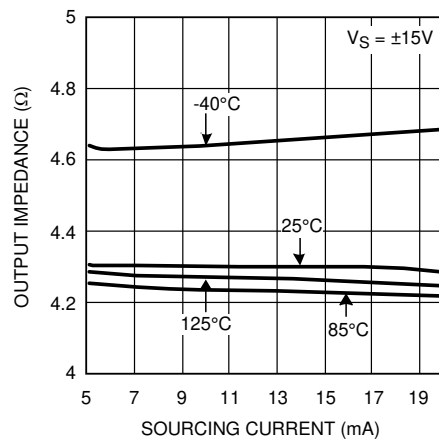


图 5-28. Output Impedance vs. Sourcing Current

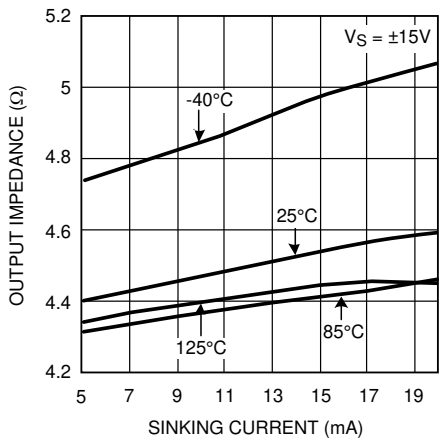


图 5-29. Output Impedance vs. Sinking Current

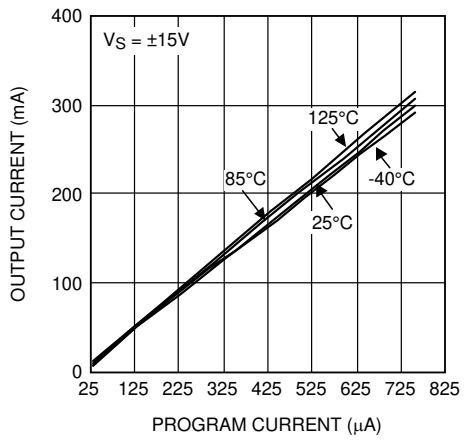


图 5-30. Output Short Circuit Current — Sourcing vs. Program Current

### 5.6 Typical Characteristics (continued)

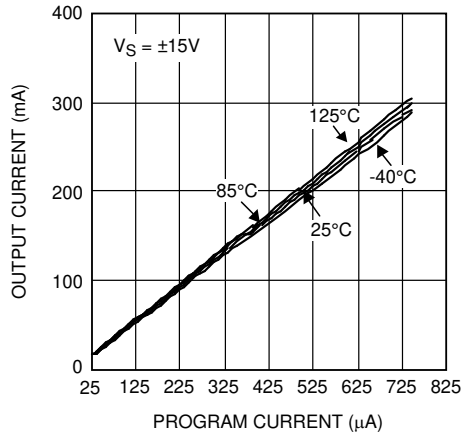


图 5-31. Output Short Circuit Current — Sinking vs. Program Current

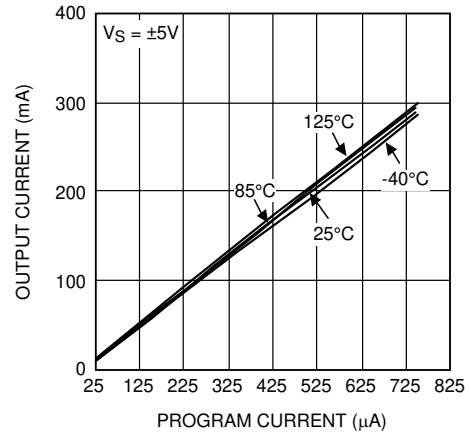


图 5-32. Output Short Circuit Current — Sourcing vs. Program Current

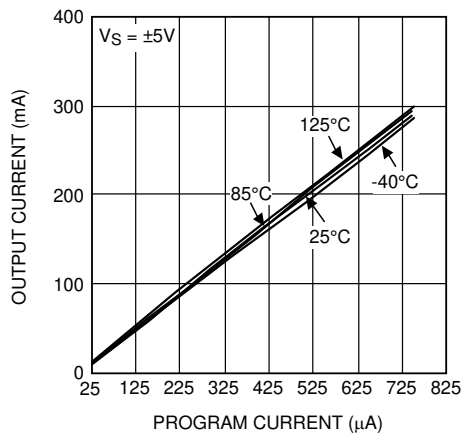


图 5-33. Output Short Circuit Current — Sinking vs. Program Current

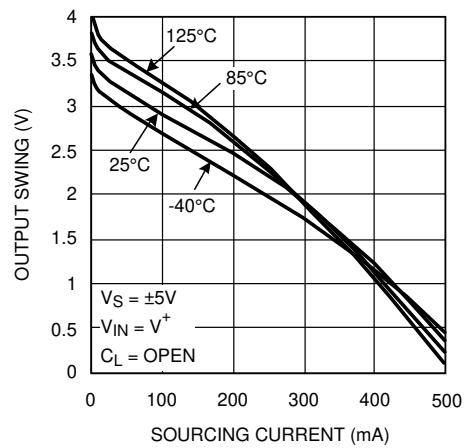


图 5-34. Positive Output Swing vs. Sourcing Current

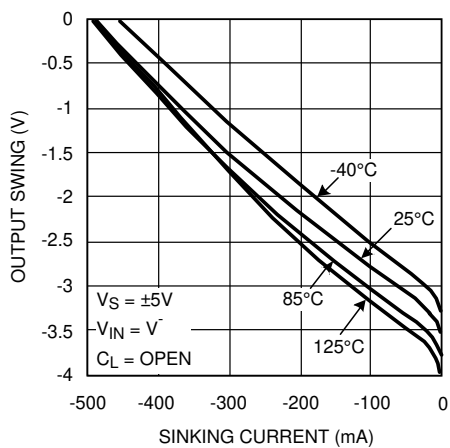


图 5-35. Negative Output Swing vs. Sinking Current

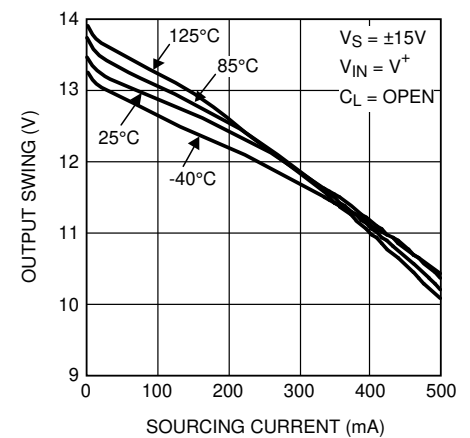


图 5-36. Positive Output Swing vs. Sourcing Current

### 5.6 Typical Characteristics (continued)

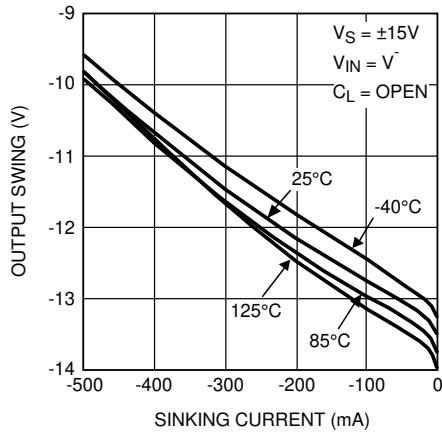


图 5-37. Negative Output Swing vs. Sinking Current

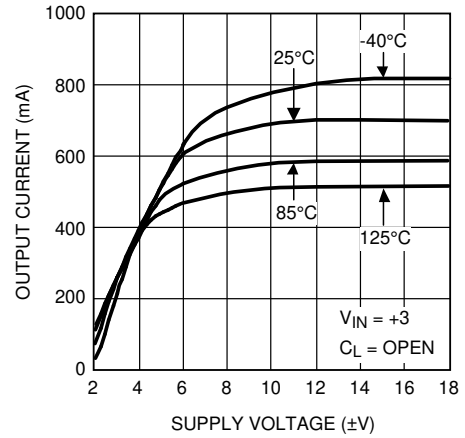


图 5-38. Output Short Circuit Current — Sourcing vs. Supply Voltage

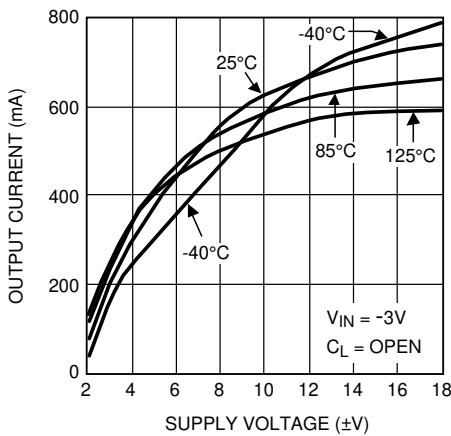


图 5-39. Output Short Circuit Current — Sinking vs. Supply Voltage

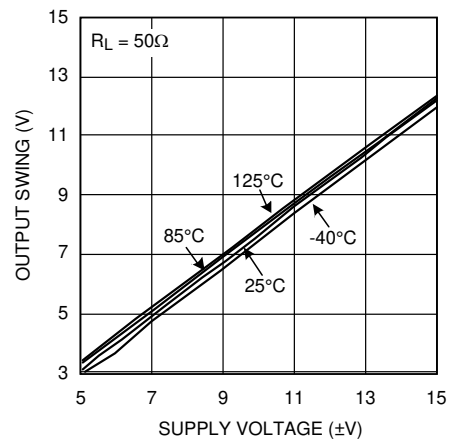


图 5-40. Positive Output Swing vs. Supply Voltage

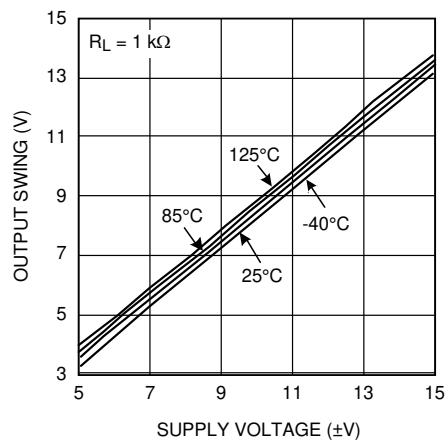


图 5-41. Positive Output Swing vs. Supply Voltage

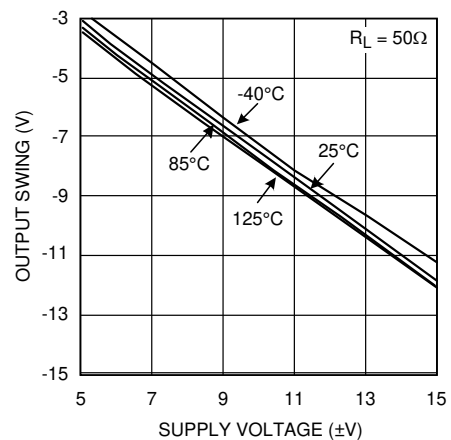


图 5-42. Negative Output Swing vs. Supply Voltage

5.6 Typical Characteristics (continued)

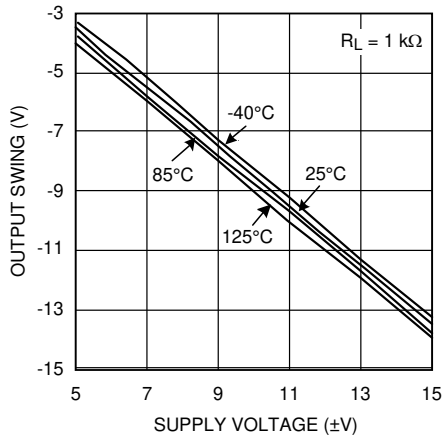


图 5-43. Negative Output Swing vs. Supply Voltage

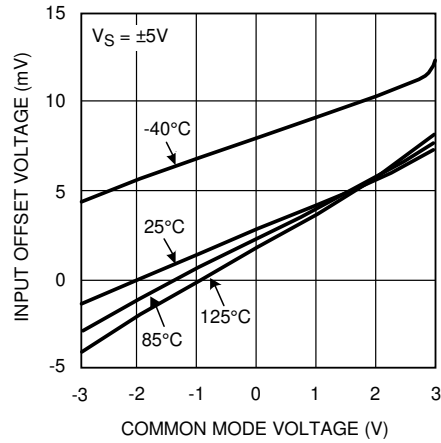


图 5-44. Input Offset Voltage of Amplifier vs. Common Mode Voltage

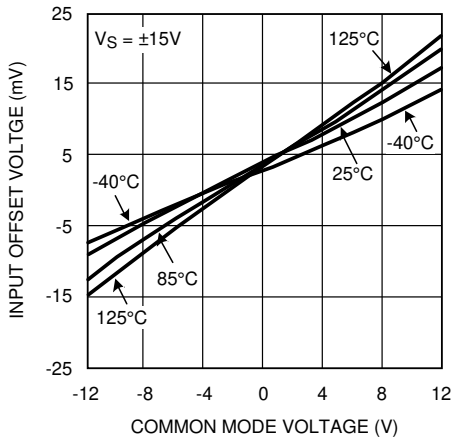


图 5-45. Input Offset Voltage of Amplifier vs. Common Mode Voltage

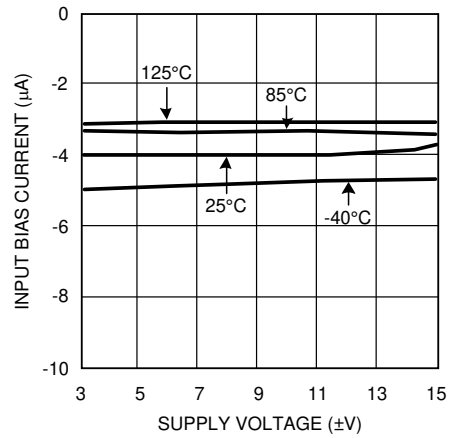


图 5-46. Input Bias Current of Amplifier vs. Supply Voltage

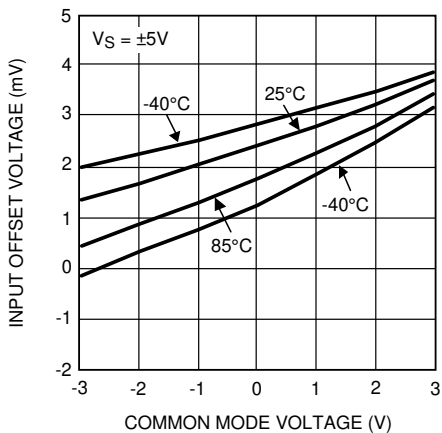


图 5-47. Input Offset Voltage of V/I Section vs. Common Mode Voltage

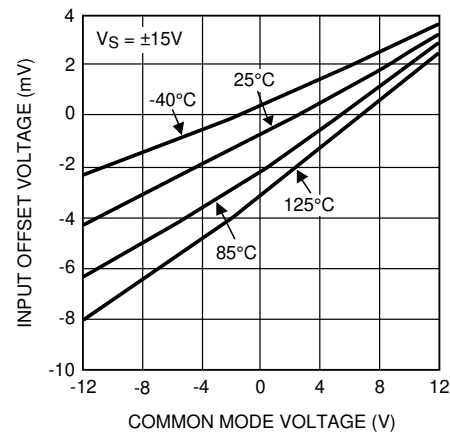


图 5-48. Input Offset Voltage of V/I Section vs. Common Mode Voltage

## 6 Application Hints

### 6.1 Buffers

Buffers are often called voltage followers because they have largely unity voltage gain, thus the name has generally come to mean a device that supplies current gain but no voltage gain. Buffers serve in applications requiring isolation of source and load, for example, high input impedance and low output impedance (high output current drive). In addition, they offer gain flatness and wide bandwidth.

Most operational amplifiers that meet the other given requirements in a particular application can be configured as buffers, though they are generally more complex and are, for the most part, not optimized for unity gain operation. The commercial buffer is a cost effective substitute for an op amp. Buffers serve several useful functions, either in tandem with op amps or in standalone applications. As mentioned, their primary function is to isolate a high impedance source from a low impedance load, since a high  $Z$  source cannot supply the needed current to the load. For example, in the case where the signal source to an analog to digital converter is a sensor, it is recommended that the sensor be isolated from the A/D converter. The use of a buffer ensures a low output impedance and delivery of a stable output to the converter. In A/D converter applications buffers need to drive varying and complex reactive loads.

Buffers come in two flavors: Open Loop and Closed Loop. While sacrificing the precision of some DC characteristics, and generally displaying poorer gain linearity, open loop buffers offer lower cost and increased bandwidth, along with less phase shift and propagation delay than do closed loop buffers. The LMH6321 is of the open loop variety.

图 6-1 shows a simplified diagram of the LMH6321 topology, revealing the open loop complementary follower design approach. 图 6-2 shows the LMH6321 in a typical application, in this case, a 50  $\Omega$  coaxial cable driver.

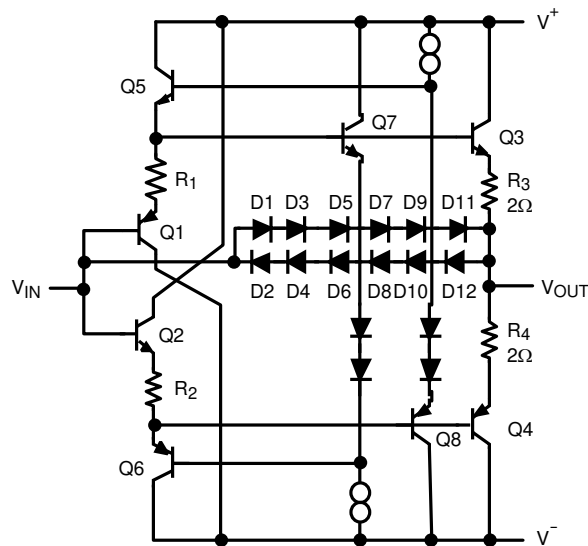


图 6-1. Simplified Schematic

### 6.2 Supply Bypassing

The method of supply bypassing is not critical for frequency stability of the buffer, and, for light loads, capacitor values in the neighborhood of 1 nF to 10 nF are adequate. However, under fast slewing and large loads, large transient currents are demanded of the power supplies, and when combined with any significant wiring inductance, these currents can produce voltage transients. For example, the LMH6321 can slew typically at 1000 V/ $\mu$ s. Therefore, under a 50  $\Omega$  load condition the load can demand current at a rate,  $di/dt$ , of 20 A/ $\mu$ s. This current flowing in an inductance of 50 nH (approximately 1.5" of 22 gauge wire) will produce a 1 V transient. Thus, it is recommended that solid tantalum capacitors of 5  $\mu$ F to 10  $\mu$ F, in parallel with a ceramic 0.1  $\mu$ F capacitor be added as close as possible to the device supply pins.



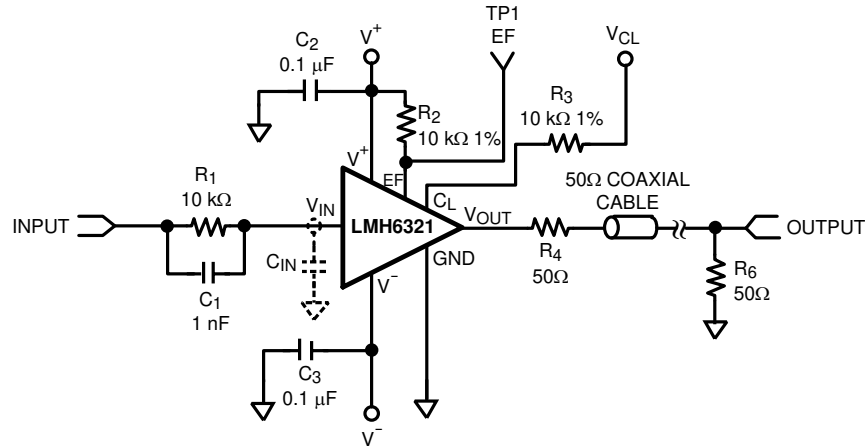


图 6-2. 50 Ω Coaxial Cable Driver with Dual Supplies

For values of capacitors in the 10  $\mu$ F to 100  $\mu$ F range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of their very low ESR (typically less than 10  $M\Omega$ ) and low ESL.

### 6.3 Load Impedance

The LMH6321 is stable under any capacitive load when driven by a 50  $\Omega$  source. As shown by 图 5-1 in 节 5.6, worst case overshoot is for a purely capacitive load of about 1 nF. Shunting the load capacitance with a resistor will reduce the overshoot.

### 6.4 Source Inductance

Like any high frequency buffer, the LMH6321 can oscillate with high values of source inductance. The worst case condition occurs with no input resistor, and a purely capacitive load of 50 pF, where up to 100 nH of source inductance can be tolerated. With a 50  $\Omega$  load, this goes up to 200 nH. However, a 100  $\Omega$  resistor placed in series with the buffer input will ensure stability with a source inductances up to 400 nH with any load.

### 6.5 Overvoltage Protection

(Refer to the simplified schematic in 图 6-1).

If the input-to-output differential voltage were allowed to exceed the Absolute Maximum Rating of 5 V, an internal diode clamp would turn on and divert the current around the compound emitter followers of Q1/Q3 (D1 - D11 for positive input), or around Q2/Q4 (D2 - D12 for negative inputs). Without this clamp, the input transistors Q1 - Q4 would zener, thereby damaging the buffer.

To limit the current through this clamp, a series resistor should be added to the buffer input (see  $R_1$  in 图 6-2). Although the allowed current in the clamp can be as high as 5 mA, which would suggest a 2 k $\Omega$  resistor from a 15 V source, it is recommended that the current be limited to about 1 mA, hence the 10 k $\Omega$  shown.

The reason for this larger resistor is explained in the following: One way that the input or output voltage differential can exceed the Absolute Maximum value is under a short circuit condition to ground while driving the input with up to  $\pm 15$  V. However, in the LMH6321 the maximum output current is set by the programmable Current Limit pin ( $C_L$ ). The value set by this pin is specified to be accurate to 5 mA  $\pm 5\%$ . If the input/output differential exceeds 5 V while the output is trying to supply the maximum set current to a shorted condition or to a very low resistance load, a portion of that current will flow through the clamp diodes, thus creating an error in the total load current. If the input resistor is too low, the error current can exceed the 5 mA  $\pm 5\%$  budget.

## 6.6 Bandwidth and Stability

As can be seen in the schematic of [图 6-2](#), a small capacitor is inserted in parallel with the series input resistors. The reason for this is to compensate for the natural band-limiting effect of the 1st order filter formed by this resistor and the input capacitance of the buffer. With a typical  $C_{IN}$  of 3.5 pF ([图 6-2](#)), a pole is created at

$$f_{p2} = 1/(2 \pi R_1 C_{IN}) = 4.5 \text{ MHz} \quad (1)$$

This will band-limit the buffer and produce further phase lag. If used in an op amp-loop application with an amplifier that has the same order of magnitude of unity gain crossing as  $f_{p2}$ , this additional phase lag will produce oscillation.

The solution is to add a small feed-forward capacitor (phase lead) around the input resistor, as shown in [图 6-2](#). The value of this capacitor is not critical but should be such that the time constant formed by it and the input resistor that it is in parallel with ( $R_{IN}$ ) be at least five times the time constant of  $R_{IN}C_{IN}$ . Therefore,

$$C_1 = (5R_{IN}/R_1)(C_{IN}) \quad (2)$$

from [节 5.4](#),  $R_{IN}$  is 250 k $\Omega$ .

In the case of the example in [图 6-2](#),  $R_{IN}C_{IN}$  produces a time-constant of 870 ns, so  $C_1$  should be chosen to be a minimum of 4.4  $\mu$ s, or 438 pF. The value of  $C_1$  (1000 pF) shown in [图 6-2](#) gives 10  $\mu$ s.

## 6.7 Output Current and Short Circuit Protection

The LMH6321 is designed to deliver a maximum continuous output current of 300 mA. However, the maximum available current, set by internal circuitry, is about 700 mA at room temperature. The output current is programmable up to 300 mA by a single external resistor and voltage source.

The LMH6321 is not designed to safely output 700 mA continuously and should not be used this way. However, the available maximum continuous current will likely be limited by the particular application and by the package type chosen, which together set the thermal conditions for the buffer (see [节 6.8](#)) and could require less than 300 mA.

The programming of both the sourcing and sinking currents into the load is accomplished with a single resistor. [Figure 6-3](#) shows a simplified diagram of the V to I converter and  $I_{SC}$  protection circuitry that, together, perform this task.

Referring to [Figure 6-3](#), the two simplified functional blocks, labeled V/I Converter and Short Circuit Protection, comprise the circuitry of the Current Limit Control.

The V/I converter consists of error amplifier A1 driving two PNP transistors in a Darlington configuration. The two input connections to this amplifier are  $V_{CL}$  (inverting input) and GND (non-inverting input). If GND is connected to zero volts, then the high open loop gain of A1, as well as the feedback through the Darlington, will force  $C_L$ , and thus one end  $R_{EXT}$  to be at zero volts also. Therefore, as shown in [方程式 3](#) a voltage applied to the other end of  $R_{EXT}$  will force a current into this pin.

$$I_{EXT} = V_{PROG}/R_{EXT} \quad (3)$$

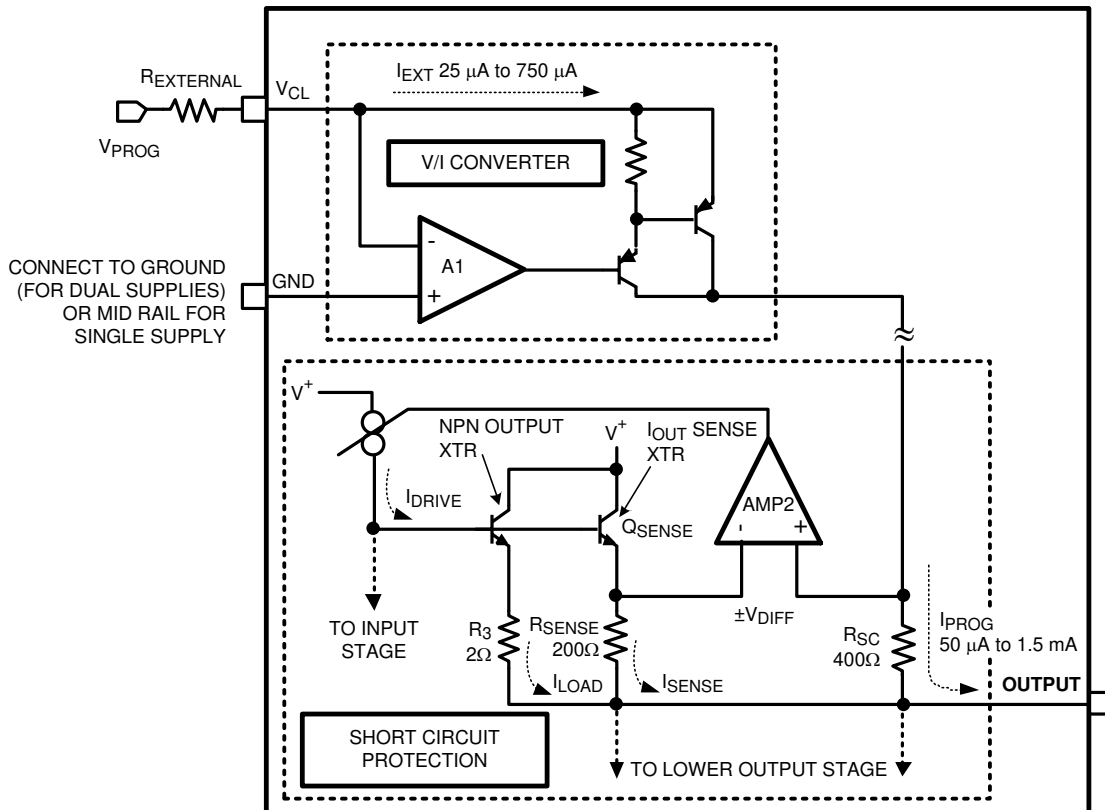
Through the  $V_{CL}$  pin,  $I_{OUT}$  is programmable from 10 mA to 300 mA by setting  $I_{EXT}$  from 25  $\mu$ A to 750  $\mu$ A by means of a fixed  $R_{EXT}$  of 10 k $\Omega$  and making  $V_{PROG}$  variable from 0.25 V to 7.5 V. Thus, an input voltage  $V_{PROG}$  is converted to a current  $I_{EXT}$ . This current is the output from the V/I converter. It is gained up by a factor of two and sent to the Short Circuit Protection block as  $I_{PROG}$ .  $I_{PROG}$  sets a voltage drop across  $R_{SC}$  which is applied to the non-inverting input of error amp A2. The other input is across  $R_{SENSE}$ . The current through  $R_{SENSE}$ , and hence the voltage drop across it, is proportional to the load current, through the current sense transistor  $Q_{SENSE}$ . The output of A2 controls the drive ( $I_{DRIVE}$ ) to the base of the NPN output transistor, Q3 which is, proportional to the amount and polarity of the voltage differential ( $V_{DIFF}$ ) between AMP2 inputs, that is, how much the voltage across  $R_{SENSE}$  is greater than or less than the voltage across  $R_{SC}$ . This loop gains  $I_{EXT}$  up by another 200, thus

$$I_{SC} = 2 \times 200 (I_{EXT}) = 400 I_{EXT} \quad (4)$$

Therefore, combining 方程式 3 and 方程式 4, and solving for  $R_{EXT}$ , we get

$$R_{EXT} = 400 V_{PROG}/I_{SC} \quad (5)$$

If the  $V_{CL}$  pin is left open, the output short circuit current will default to about 700 mA. At elevated temperatures this current will decrease.



Only the NPN output  $I_{SC}$  protection is shown. Depending on the polarity of  $V_{DIFF}$ , AMP2 will turn  $I_{DRIVE}$  either on or off.

图 6-3. Simplified Diagram of Current Limit Control

## 6.8 Thermal Management

### 6.8.1 Heatsinking

For some applications, a heat sink may be required with the LMH6321. This depends on the maximum power dissipation and maximum ambient temperature of the application. To accomplish heat sinking, the tabs on DDPACK and SO PowerPAD package may be soldered to the copper plane of a PCB for heatsinking (note that these tabs are electrically connected to the most negative point in the circuit, for example,  $V^-$ ).

Heat escapes from the device in all directions, mainly through the mechanisms of convection to the air above it and conduction to the circuit board below it and then from the board to the air. Natural convection depends on the amount of surface area that is in contact with the air. If a conductive plate serving as a heatsink is thick enough to ensure perfect thermal conduction (heat spreading) into the far recesses of the plate, the temperature rise would be simply inversely proportional to the total exposed area. PCB copper planes are, in that sense, an aid to convection, the difference being that they are not thick enough to ensure perfect conduction. Therefore, eventually we will reach a point of diminishing returns (as seen in 图 6-5). Very large increases in the copper area will produce smaller and smaller improvement in thermal resistance. This occurs, roughly, for a 1 inch square of 1 oz copper board. Some improvement continues until about 3 square inches, especially for 2 oz

boards and better, but beyond that, external heatsinks are required. Ultimately, a reasonable practical value attainable for the junction to ambient thermal resistance is about 30 °C/W under zero air flow.

A copper plane of appropriate size may be placed directly beneath the tab or on the other side of the board. If the conductive plane is placed on the back side of the PCB, it is recommended that thermal vias be used per JEDEC Standard JESD51-5.

### 6.8.2 Determining Copper Area

One can determine the required copper area by following a few basic guidelines:

1. Determine the value of the circuit's power dissipation,  $P_D$
2. Specify a maximum operating ambient temperature,  $T_{A(MAX)}$ . Note that when specifying this parameter, it must be kept in mind that, because of internal temperature rise due to power dissipation, the die temperature,  $T_J$ , will be higher than  $T_A$  by an amount that is dependent on the thermal resistance from junction to ambient,  $\theta_{JA}$ . Therefore,  $T_A$  must be specified such that  $T_J$  does not exceed the absolute maximum die temperature of 150°C.
3. Specify a maximum allowable junction temperature,  $T_{J(MAX)}$ , which is the temperature of the chip at maximum operating current. Although no strict rules exist, typically one should design for a maximum continuous junction temperature of 100°C to 130°C, but no higher than 150°C which is the absolute maximum rating for the part.
4. Calculate the value of junction to ambient thermal resistance,  $\theta_{JA}$
5. Choose a copper area that will ensure the specified  $T_{J(MAX)}$  for the calculated  $\theta_{JA}$ .  $\theta_{JA}$  as a function of copper area in square inches is shown in [Figure 6-4](#).

The maximum value of thermal resistance, junction to ambient  $\theta_{JA}$ , is defined as:

$$\theta_{JA} = (T_{J(MAX)} - T_{A(MAX)}) / P_{D(MAX)} \quad (6)$$

where

- $T_{J(MAX)}$  = the maximum recommended junction temperature
- $T_{A(MAX)}$  = the maximum ambient temperature in the user's environment
- $P_{D(MAX)}$  = the maximum recommended power dissipation

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#### Note

The allowable thermal resistance is determined by the maximum allowable heat rise,  $T_{RISE} = T_{J(MAX)} - T_{A(MAX)} = (\theta_{JA}) (P_{D(MAX)})$ . Thus, if ambient temperature extremes force  $T_{RISE}$  to exceed the design maximum, the part must be de-rated by either decreasing  $P_D$  to a safe level, reducing  $\theta_{JA}$ , further, or, if available, using a larger copper area.

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### 6.8.3 Procedure

1. First determine the maximum power dissipated by the buffer,  $P_{D(MAX)}$ . For the simple case of the buffer driving a resistive load, and assuming equal supplies,  $P_{D(MAX)}$  is given by:

$$P_{D(MAX)} = I_S (2V^+) + V^{+2}/4R_L \quad (7)$$

where

- $I_S$  = quiescent supply current
2. Determine the maximum allowable die temperature rise,

$$T_{R(MAX)} = T_{J(MAX)} - T_{A(MAX)} = P_{D(MAX)} \theta_{JA} \quad (8)$$

3. Using the calculated value of  $T_{R(MAX)}$  and  $P_{D(MAX)}$  the required value for junction to ambient thermal resistance can be found:

$$\theta_{JA} = T_{R(MAX)} / P_{D(MAX)} \quad (9)$$

4. Finally, using this value for  $\theta_{JA}$  choose the minimum value of copper area from [Figure 6-4](#).

### 6.8.4 Example

Assume the following conditions:

$$V^+ = V^- = 15 \text{ V}, R_L = 50 \ \Omega, I_S = 15 \text{ mA } T_{J(\text{MAX})} = 125^\circ\text{C}, T_{A(\text{MAX})} = 85^\circ\text{C}.$$

1. From 方程式 7

$$\bullet P_{D(\text{MAX})} = I_S (2 V^+) + V^{+2}/4R_L = (15 \text{ mA})(30 \text{ V}) + 15 \text{ V}^2/200 \ \Omega = 1.58 \text{ W}$$

2. From 方程式 8

$$\bullet T_{R(\text{MAX})} = 125^\circ\text{C} - 85^\circ\text{C} = 40^\circ\text{C}$$

3. From 方程式 9

$$\bullet \theta_{JA} = 40^\circ\text{C}/1.58 \text{ W} = 25.3^\circ\text{C}/\text{W}$$

Examining 图 6-4, we see that we cannot attain this low of a thermal resistance for one layer of 1 oz copper. It will be necessary to derate the part by decreasing either the ambient temperature or the power dissipation. Other solutions are to use two layers of 1 oz foil, or use 2 oz copper (see 表 6-1), or to provide forced air flow. One should allow about an extra 15% heat sinking capability for safety margin.

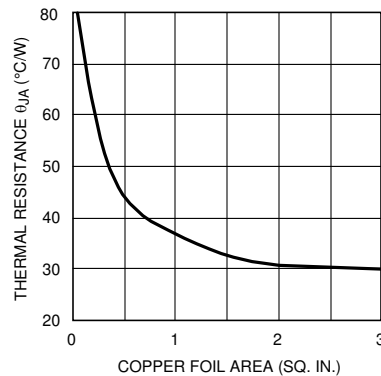


图 6-4. Thermal Resistance (Typical) for 7-L DDPACK Package Mounted on 1 oz. (0.036 mm) PC Board Foil

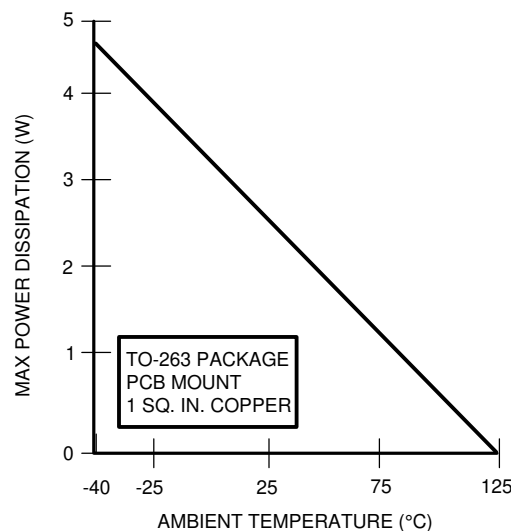


图 6-5. Derating Curve for DDPACK package. No Air Flow

**表 6-1.  $\theta_{JA}$  vs. Copper Area and  $P_D$  for DDPAK. 1.0 oz cu Board. No Air Flow. Ambient Temperature = 24°C**

Copper Area	$\theta_{JA}$ at 1.0W (°C/W)	$\theta_{JA}$ at 2.0W (°C/W)
1 Layer = 1" x2" cu Bottom	62.4	54.7
2 Layer = 1" x2" cu Top and Bottom	36.4	32.1
2 Layer = 2" x2" cu Top and Bottom	23.5	22.0
2 Layer = 2" x4" cu Top and Bottom	19.8	17.2

As seen in the previous example, buffer dissipation in DC circuit applications is easily computed. However, in AC circuits, signal wave shapes and the nature of the load (reactive, non-reactive) determine dissipation. Peak dissipation can be several times the average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

A selection of thermal data for the SO PowerPAD package is shown in 表 6-2. The table summarizes  $\theta_{JA}$  for both 0.5 watts and 0.75 watts. Note that the thermal resistance, for both the DDPAK and the SO PowerPAD package is lower for the higher power dissipation levels. This phenomenon is a result of the principle of Newtons Law of Cooling. Restated in term of heatsink cooling, this principle says that the rate of cooling and hence the thermal conduction, is proportional to the temperature difference between the junction and the outside environment (ambient). This difference increases with increasing power levels, thereby producing higher die temperatures with more rapid cooling.

**表 6-2.  $\theta_{JA}$  vs. Copper Area and  $P_D$  for SO PowerPAD. 1.0 oz cu Board. No Airflow. Ambient Temperature = 22°C**

Copper Area/Vias	$\theta_{JA}$ at 0.5W (°C/W)	$\theta_{JA}$ at 0.75W (°C/W)
1 Layer = 0.05 sq. in. (Bottom) + 3 Via Pads	141.4	138.2
1 Layer = 0.1 sq. in. (Bottom) + 3 Via Pads	134.4	131.2
1 Layer = 0.25 sq. in. (Bottom) + 3 Via Pads	115.4	113.9
1 Layer = 0.5 sq. in. (Bottom) + 3 Via Pads	105.4	104.7
1 Layer = 1.0 sq. in. (Bottom) + 3 Via Pads	100.5	100.2
2 Layer = 0.5 sq. in. (Top)/ 0.5 sq. in. (Bottom) + 33 Via Pads	93.7	92.5
2 Layer = 1.0 sq. in. (Top)/ 1.0 sq. in. (Bottom) + 53 Via Pads	82.7	82.2

## 6.9 Error Flag Operation

The LMH6321 provides an open collector output at the EF pin that produces a low voltage when the Thermal Shutdown Protection is engaged, due to a fault condition. Under normal operation, the Error Flag pin is pulled up to  $V^+$  by an external resistor. When a fault occurs, the EF pin drops to a low voltage and then returns to  $V^+$  when the fault disappears. This voltage change can be used as a diagnostic signal to alert a microprocessor of a system fault condition. If the function is not used, the EF pin can be either tied to ground or left open. If this function is used, a 10 k $\Omega$ , or larger, pull-up resistor ( $R_2$  in 图 6-2) is recommended. The larger the resistor the lower the voltage will be at this pin under thermal shutdown. 表 6-3 shows some typical values of  $V_{EF}$  for 10 k $\Omega$  and 100 k $\Omega$ .

**表 6-3.  $V_{EF}$  vs.  $R_2$**

$R_2$ (in 图 6-2)	At $V^+ = 5 V$	At $V^+ = 15 V$
10 k $\Omega$	0.24 V	0.55 V
100 K $\Omega$	0.036 V	0.072 V

## 6.10 Single Supply Operation

If dual supplies are used, then the GND pin can be connected to a hard ground (0 V) (as shown in 图 6-2). However, if only a single supply is used, this pin must be set to a voltage of one  $V_{BE}$  ( $\approx 0.7$  V) or greater, or more commonly, mid rail, by a stiff, low impedance source. This precludes applying a resistive voltage divider to the GND pin for this purpose. 图 6-6 shows one way that this can be done.

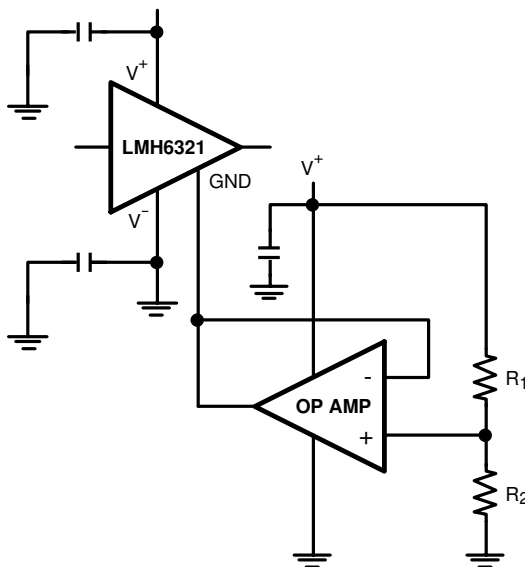


图 6-6. Using an Op Amp to Bias the GND Pin to  $\frac{1}{2} V^+$  for Single Supply Operation

In 图 6-6, the op amp circuit pre-biases the GND pin of the buffer for single supply operation.

The GND pin can be driven by an op amp configured as a constant voltage source, with the output voltage set by the resistor voltage divider,  $R_1$  and  $R_2$ . It is recommended that These resistors be chosen so as to set the GND pin to  $V^+/2$ , for maximum common mode range.

## 6.11 Slew Rate

Slew rate is the rate of change of output voltage for large-signal step input changes. For resistive load, slew rate is limited by internal circuit capacitance and operating current (in general, the higher the operating current for a given internal capacitance, the faster is the slew rate). 图 6-7 shows the slew capabilities of the LMH6321 under large signal input conditions, using a resistive load.

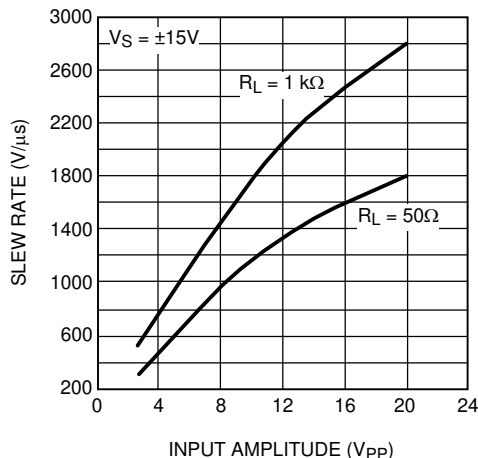


图 6-7. Slew Rate vs. Peak-to-Peak Input Voltage

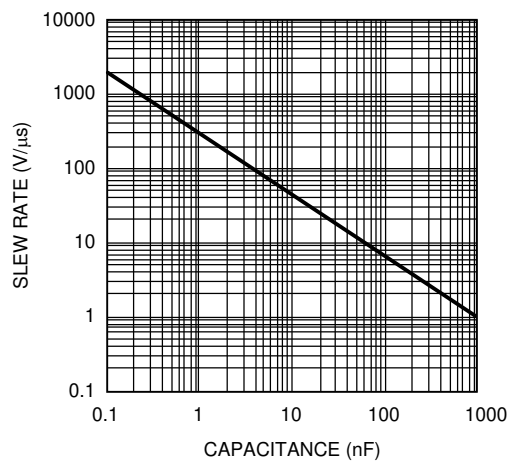


However, when driving capacitive loads, the slew rate may be limited by the available peak output current according to the following expression.

$$dv/dt = I_{PK}/C_L \tag{10}$$

and rapidly changing output voltages will require large output load currents. For example if the part is required to slew at 1000 V/μs with a load capacitance of 1 nF the current demand from the LMH6321 would be 1A. Therefore, fast slew rate is incompatible with large C<sub>L</sub>. Also, since C<sub>L</sub> is in parallel with the load, the peak current available to the load decreases as C<sub>L</sub> increases.

图 6-8 illustrates the effect of the load capacitance on slew rate. Slew rate tests are specified for resistive loads and/or very small capacitive loads, otherwise the slew rate test would be a measure of the available output current. For the highest slew rate, it is obvious that stray load capacitance should be minimized. Peak output current should be kept below 500 mA. This translates to a maximum stray capacitance of 500 pF for a slew rate of 1000 V/μs.



**图 6-8. Slew Rate vs. Load Capacitance**

## 7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 7.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

## 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6321MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMH63 21MR	<a href="#">Samples</a>
LMH6321MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMH63 21MR	<a href="#">Samples</a>
LMH6321TS/NOPB	ACTIVE	DDPAK/ TO-263	KTW	7	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LMH6321TS	<a href="#">Samples</a>
LMH6321TSX/NOPB	ACTIVE	DDPAK/ TO-263	KTW	7	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LMH6321TS	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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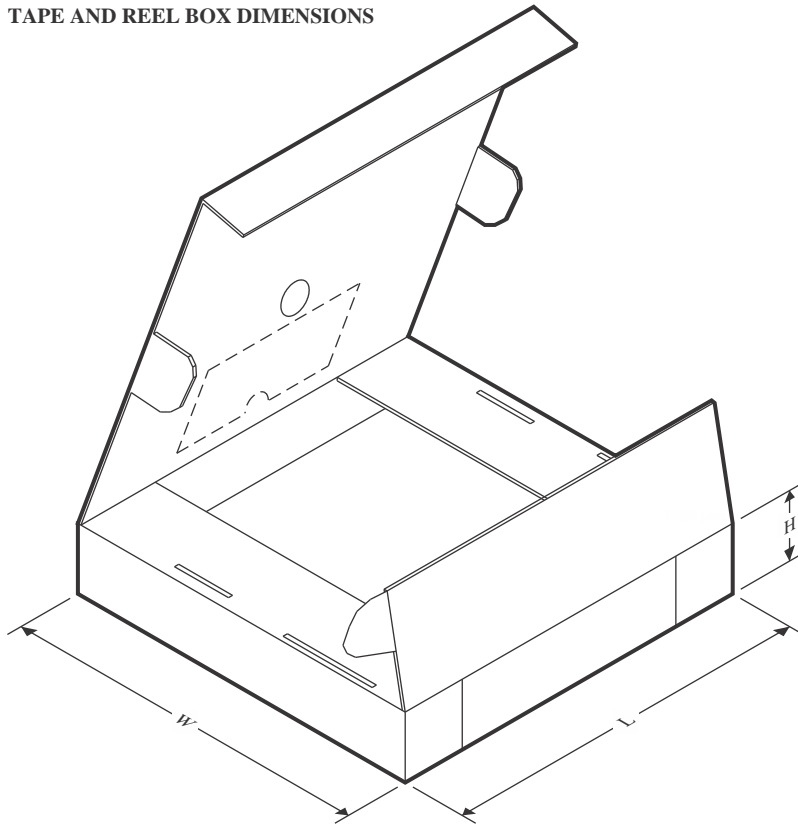
**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

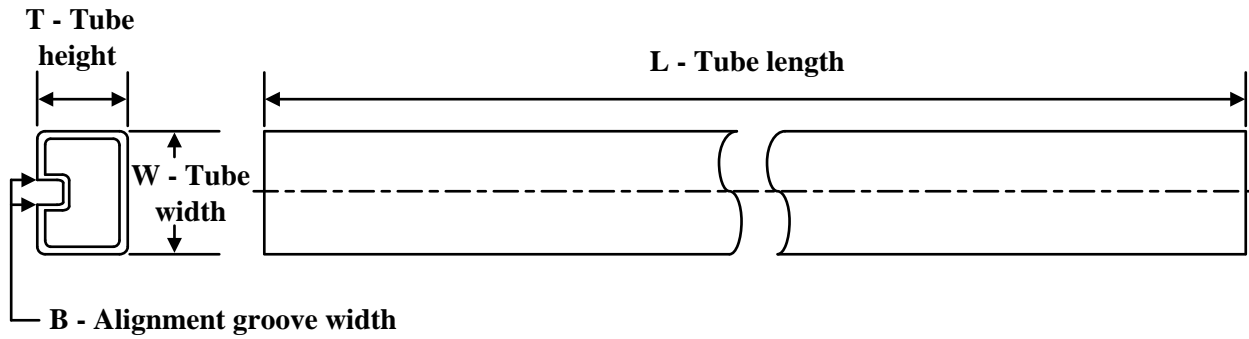
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6321MRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6321TSX/NOPB	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6321MRX/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	35.0
LMH6321TSX/NOPB	DDPAK/TO-263	KTW	7	500	367.0	367.0	45.0

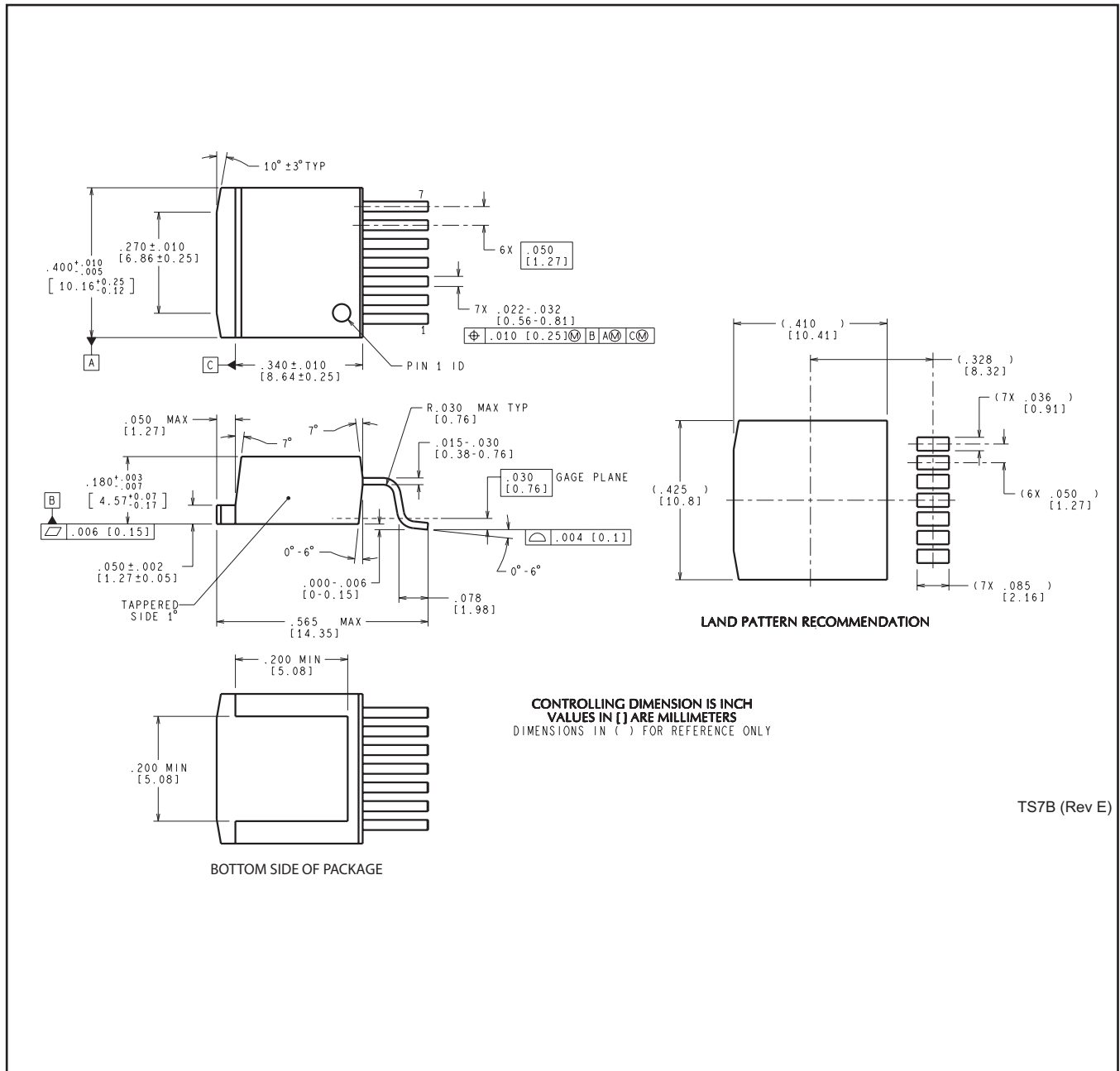
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LMH6321MR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LMH6321TS/NOPB	KTW	TO-263	7	45	502	25	8204.2	9.19

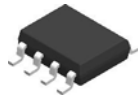


KTW0007B



TS7B (Rev E)

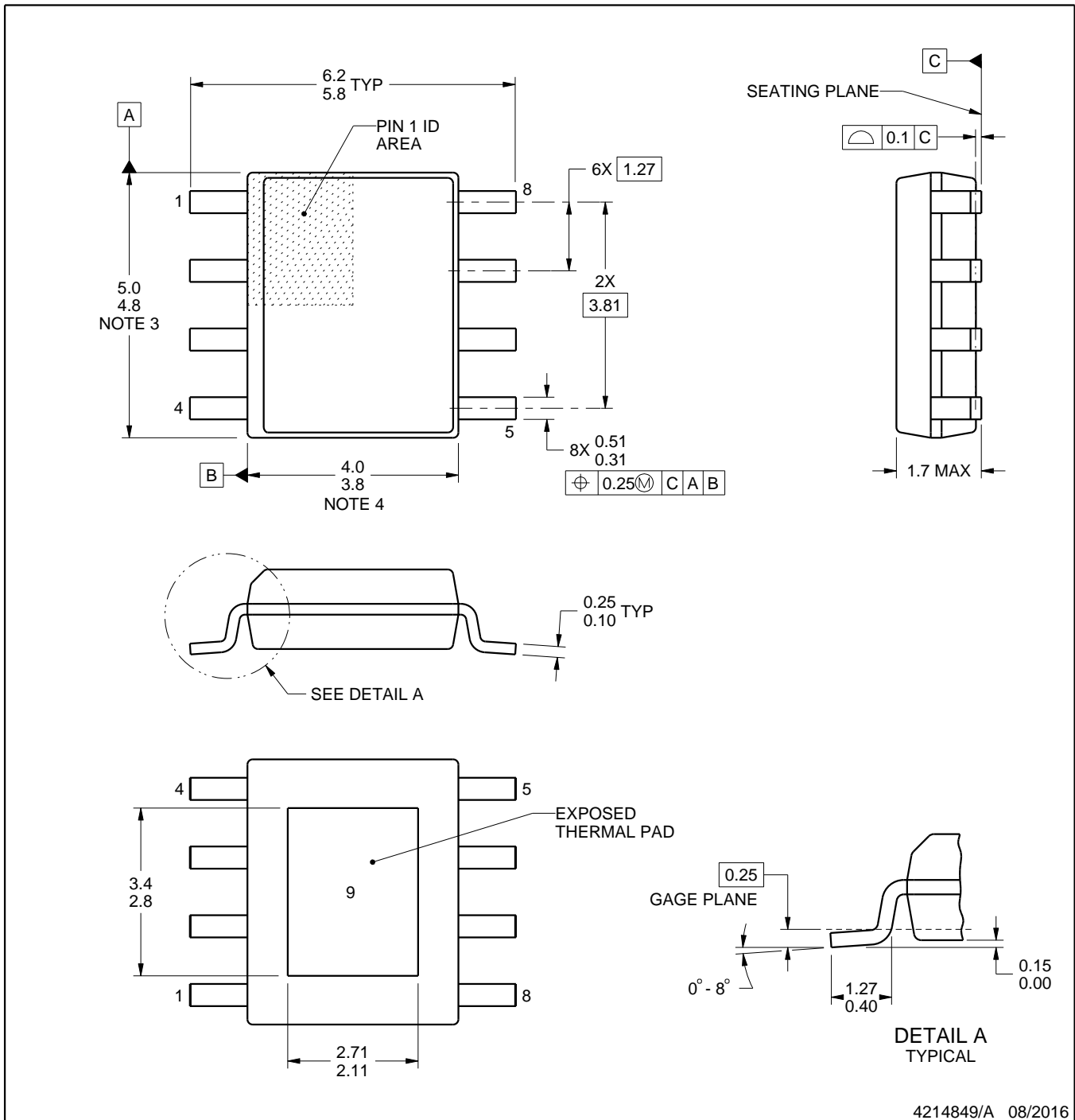
# DDA0008B



# PACKAGE OUTLINE

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



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### NOTES:

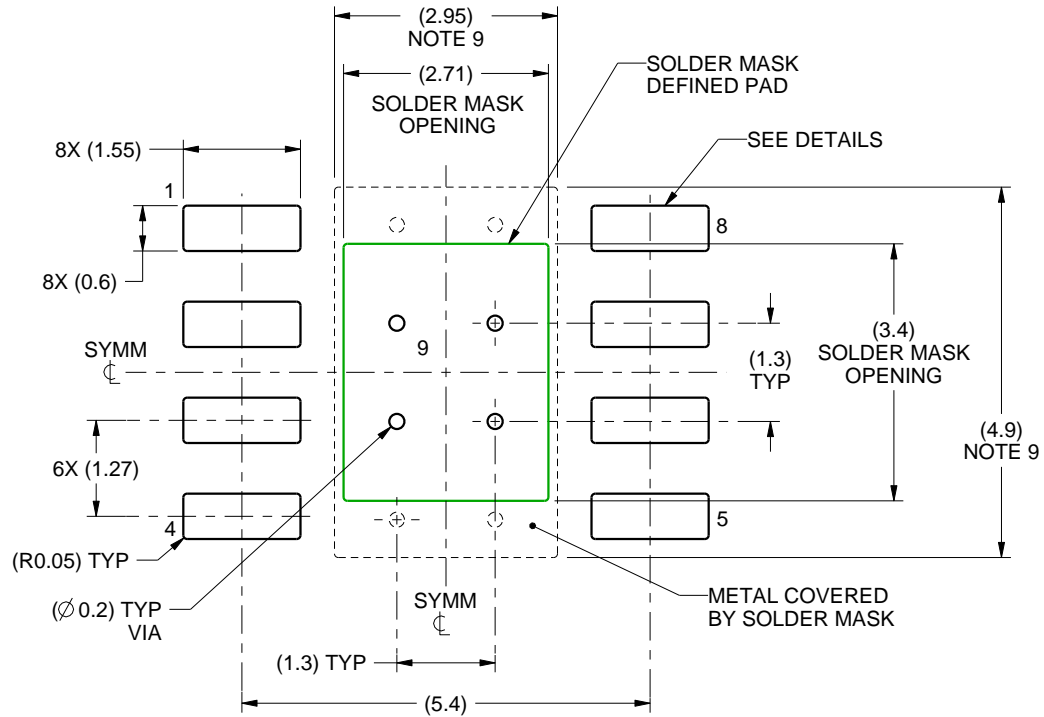
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

# EXAMPLE BOARD LAYOUT

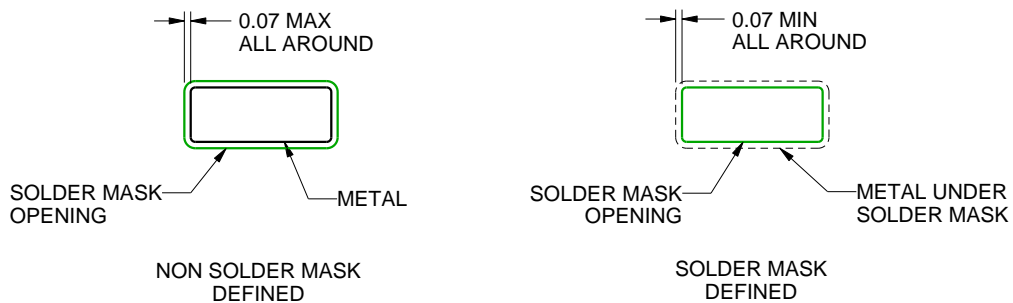
DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
PADS 1-8

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NOTES: (continued)

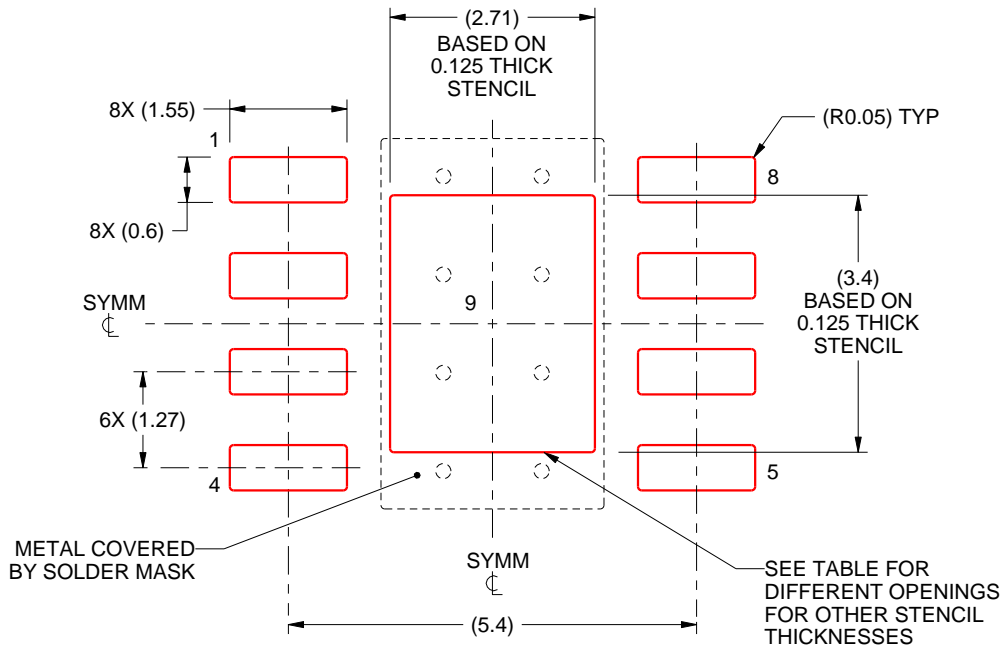
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
 EXPOSED PAD  
 100% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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