具有内部 EEPROM 的 LMK61E2 超低抖动可编程振荡器

1 特性

- 超低噪声、高性能
  - 抖动：f_{OUT} > 100MHz 时的典型值为 90fs RMS
  - PSRR：–70dBc，强大的电源抗噪性
- 灵活的输出格式；用户可选择
  - 低电压正射极耦合逻辑 (LVPECL) 高达 1GHz
  - 低压差分信令 (LVDS) 高达 900MHz
  - 高速收发器逻辑 (HSTL) 高达 400MHz
- 总频率容差：±50ppm
- 系统级 特性
  - 频率裕量：精调和粗调
  - 内部 EEPROM：用户可配置默认设置
- 其他 特性
  - 器件控制：I^2C
  - 3.3V 工作电压
  - 工业温度范围（-40ºC 至 +85ºC）
  - 7mm × 5mm 8 引脚封装
  - 使用 LMK61E2 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 晶体振荡器、SAW 振荡器或芯片振荡器的高性能替代产品
- 开关、路由器、网卡、基带装置 (BBU)、服务器、存储/SAN
- 测试和测量
- 医疗成像
- 现场可编程门阵列 (FPGA)，处理器连接

3 说明

LMK61E2 是一款超低抖动 PLLatinum™可编程振荡器，具有分数 N 频率合成器（带可生成常用基准时钟的集成 VCO）。输出可配置为 LVPECL、LVDS 或 HCSL。

该器件 支持 从片上 EEPROM 自启动，该片上 EEPROM 出厂时编程为生成 156.25MHz 的 LVPECL 输出。器件寄存器和 EEPROM 设置可通过 I^2C 串行接口在系统内实现完全编程。内部电源调节功能提供出色的电源纹波抑制 (PSRR)，降低了供电网络的成本和复杂性。该器件由单个 3.3V ± 5% 电源供电。

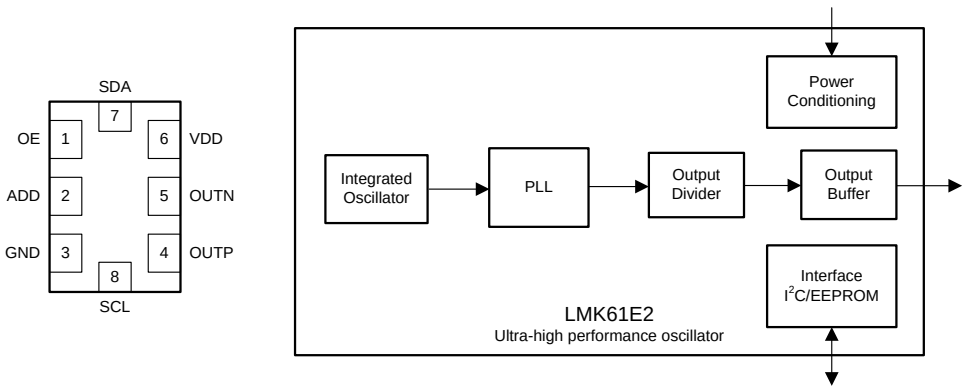
该器件支持通过 I^2C 串行接口进行频率精调和粗调，从而支持系统设计验证测试 (DVT)，例如标准合规性和系统时序裕量测试。

器件信息(1)

器件型号	默认输出频率 (MHz) 和格式	封装和封装尺寸（标称值）
LMK61E2	156.25 LVPECL	8 引脚 QFM (SIA)，7.00mm x 5.00mm
LMK61E2BAA	156.25 LVDS	
LMK61E2BBA	125 LVDS	

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

引脚分布和简化框图



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4 修订历史记录

Changes from Revision A (September 2015) to Revision B **Page**

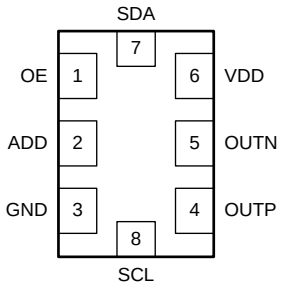
- 添加了用于定制设计的 WEBENCH 链接和信息 ... 1
- 发布了新的 LMK61E2BAA、LMK61E2BBA ... 1
- 将数据表文本更新为最新的文档和转换标准 ... 1
- Moved Figure 34 to *Layout Example* ... 45

Changes from Original (September 2015) to Revision A **Page**

- Moved conditions from figure title to table under each graphic ... 9
- Updated Figure 26 ... 18
- 添加了“相关文档”部分。 ... 46

5 Pin Configuration and Functions

SIA Package
8-Pin QFM
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
POWER			
GND	3	Ground	Device Ground.
VDD	6	Analog	3.3-V Power Supply.
OUTPUT BLOCK			
OUTP, OUTN	4, 5	Universal	Differential Output Pair (LVPECL, LVDS or HCSL).
DIGITAL CONTROL / INTERFACES			
ADD	2	LVCMOS	When left open, LSB of I^2C slave address is set to 01. When tied to VDD, LSB of I^2C slave address is set to 10. When tied to GND, LSB of I^2C slave address is set to 00.
OE	1	LVCMOS	Output Enable (internal pullup). When set to low, output pair is disabled and set at high impedance.
SCL	8	LVCMOS	I^2C Serial Clock (open-drain). Requires an external pullup resistor to VDD.
SDA	7	LVCMOS	I^2C Serial Data (bidirectional, open-drain). Requires an external pullup resistor to VDD.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD	Device supply voltage	–0.3	3.6	V
V_{IN}	Output voltage for logic inputs	–0.3	VDD + 0.3	V
V_{OUT}	Output voltage for clock outputs	–0.3	VDD + 0.3	V
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device supply voltage	3.135	3.3	3.465	V
T_A	Ambient temperature	–40	25	85	°C
T_J	Junction temperature			125	°C
t_{RAMP}	VDD power-up ramp time	0.1		100	ms

6.4 Thermal Information

THERMAL METRIC(1)		LMK61E2 (2) (3) (4) QFM (SIA) 8 PINS			UNIT
		AIRFLOW (LFM) 0	AIRFLOW (LFM) 200	AIRFLOW (LFM) 400	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54	44	41.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34	n/a	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.7	n/a	n/a	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.2	16.9	21.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.7	37.8	38.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal resistance is calculated on a 4-layer JEDEC board.
(3) Connected to GND with 3 thermal vias (0.3-mm diameter).
(4) ψ_{JB} (junction-to-board) is used when the main heat flow is from the junction to the GND pad. See the *Layout* section for more information on ensuring good system reliability and quality.

6.5 Electrical Characteristics - Power Supply(1)

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Device current consumption	LVPECL (2)		162	208	mA
		LVDS		152	196	
		HCSL		155	196	
IDD-PD	Device current consumption when output is disabled	OE = GND		136		mA

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) On-chip power dissipation should exclude 40 mW, dissipated in the 150-Ω termination resistors, from total power dissipation.

6.6 LVPECL Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency(2)		10		1000	MHz
V_{OD}	Output voltage swing (V_{OH} – V_{OL})(2)		700	800	1200	mV
$V_{OUT, DIFF, PP}$	Differential output peak-to-peak swing			2 × $\|V_{OD}\|$		V
V_{OS}	Output common-mode voltage			VDD – 1.55		V
t_R / t_F	Output rise/fall time (20% to 80%)(3)			120	200	ps
PN-Floor	Output phase noise floor (f_{OFFSET} > 10 MHz)	156.25 MHz		–165		dBc/Hz
ODC	Output duty cycle(3)		45%		55%	

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(3) Ensured by characterization.

6.7 LVDS Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency(1)		10		900	MHz
V_{OD}	Output voltage swing (V_{OH} – V_{OL})(1)		300	390	480	mV
$V_{OUT, DIFF, PP}$	Differential output peak-to-peak swing			2 × $\|V_{OD}\|$		V
V_{OS}	Output common-mode voltage			1.2		V
t_R / t_F	Output rise/fall time (20% to 80%)(2)			150	250	ps
PN-Floor	Output phase noise floor (f_{OFFSET} > 10 MHz)	156.25 MHz		–162		dBc/Hz
ODC	Output duty cycle(2)		45%		55%	
R_{OUT}	Differential output impedance			125		Ω

(1) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(2) Ensured by characterization.

6.8 HCSL Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency		10		400	MHz
V_{OH}	Output high voltage		600		850	mV
V_{OL}	Output low voltage		–100		100	mV
V_{CROSS}	Absolute crossing voltage(2)(3)		250		475	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS}(2)(3)		0		140	mV
dV/dt	Slew rate(4)		0.8		2	V/ns
PN-Floor	Output phase noise floor (f_{OFFSET} > 10 MHz)	100 MHz		–164		dBc/Hz
ODC	Output duty cycle(4)		45%		55%	

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Measured from –150 mV to +150 mV on the differential waveform with the 300-mVpp measurement window centered on the differential zero crossing.
(3) Ensured by design.
(4) Ensured by characterization.

6.9 OE Input Characteristics

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		1.4			V
V_{IL}	Input low voltage				0.6	V
I_{IH}	Input high current	V_{IH} = VDD	–40		40	µA
I_{IL}	Input low current	V_{IL} = GND	–40		40	µA
C_{IN}	Input capacitance			2		pF

6.10 ADD Input Characteristics

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		1.4			V
V_{IL}	Input low voltage				0.4	V
I_{IH}	Input high current	V_{IH} = VDD	–40		40	µA
I_{IL}	Input low current	V_{IL} = GND	–40		40	µA
C_{IN}	Input capacitance			2		pF

6.11 Frequency Tolerance Characteristics(1)

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_T	Total frequency tolerance	All output formats, frequency bands and device junction temperature up to 125°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and aging (10 years)	–50		50	ppm

(1) Ensured by characterization.

6.12 Power-On/Reset Characteristics (VDD)

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{THRESH}	Threshold voltage(1)		2.72		2.95	V
V_{DROOP}	Allowable voltage droop(2)				0.1	V
$t_{STARTUP}$	Start-up time (1)	Time elapsed from VDD at 3.135 V to output enabled			10	ms
t_{OE-EN}	Output enable time(2)	Time elapsed from OE at V_{IH} to output enabled			50	µs
t_{OE-DIS}	Output disable time(2)	Time elapsed from OE at V_{IL} to output disabled			50	µs

(1) Ensured by characterization.
(2) Ensured by design.

6.13 I²C-Compatible Interface Characteristics (SDA, SCL)(1)(2)

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.6	V
I_{IH}	Input leakage		–40		40	µA
C_{IN}	Input capacitance			2		pF
C_{OUT}	Input capacitance				400	pF
V_{OL}	Output low voltage	I_{OL} = 3 mA			0.6	V

(1) Total capacitive load for each bus line ≤ 400 pF.
(2) Ensured by design.

I²C-Compatible Interface Characteristics (SDA, SCL)(1)(2) (continued)

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	I²C clock rate		100		400	kHz
t_{SU_STA}	START condition setup time	SCL high before SDA low	0.6			µs
t_{H_STA}	START condition hold time	SCL low after SDA low	0.6			µs
t_{PH_SCL}	SCL pulse width high		0.6			µs
t_{PL_SCL}	SCL pulse width low		1.3			µs
t_{H_SDA}	SDA hold time	SDA valid after SCL low	0		0.9	µs
t_{SU_SDA}	SDA setup time		115			ns
t_{R_IN} / t_{F_IN}	SCL/SDA input rise and fall time				300	ns
t_{F_OUT}	SDA output fall time	C_{BUS} = 10 pF to 400 pF			250	ns
t_{SU_STOP}	STOP condition setup time		0.6			µs
t_{BUS}	Bus free time between STOP and START		1.3			µs

6.14 PSRR Characteristics(1)

VDD = 3.3 V, T_A = 25°C, PLL bandwidth = 400 kHz, VCO Frequency = 5 GHz (Integer-N PLL), Output Divider = 32, Output Type = LVPECL/LVDS/HCSL

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Spurs induced by 50-mV power supply ripple(2)(3) at 156.25-MHz output, all output types	Sine wave at 50 kHz		–70		dBc
		Sine wave at 100 kHz		–70		
		Sine wave at 500 kHz		–70		
		Sine wave at 1 MHz		–70		

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Measured maximum spur level with 50-mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD pin
(3) DJ_{SPUR} (ps, pk-pk) = [2 × 10(SPUR/20) / (π × f_{OUT})] × 1e6, where PSRR or SPUR in dBc and f_{OUT} in MHz.

6.15 Other Characteristics

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VCO}	VCO frequency range		4.6		5.6	GHz

6.16 PLL Clock Output Jitter Characteristics(1)(2)

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ	RMS phase jitter(3) (12 kHz – 20 MHz) (1 kHz – 5 MHz)	f_{OUT} ≥ 100 MHz, Integer-N PLL, All output types		100	200	fs RMS
RJ	RMS phase jitter(3) (12 kHz – 20 MHz) (1 kHz – 5 MHz)	f_{OUT} ≥ 100 MHz, Fractional-N PLL, All output types		150	300	fs RMS

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).
(3) Ensured by characterization.

6.17 Typical 156.25-MHz Output Phase Noise Characteristics(1)(2)

VDD = 3.3 V, T_A = 25°C, PLL bandwidth = 400 kHz, VCO Frequency = 5 GHz, Integer-N PLL, Output Divider = 32, Output Type = LVPECL/LVDS/HCSL

PARAMETER		OUTPUT TYPE			UNIT
		LVPECL	LVDS	HCSL	
phn_{10k}	Phase noise at 10-kHz offset	–143	–143	–143	dBc/Hz
Phn_{20k}	Phase noise at 20-kHz offset	–143	–143	–143	dBc/Hz
phn_{100k}	Phase noise at 100-kHz offset	–144	–144	–144	dBc/Hz
Phn_{200k}	Phase noise at 200-kHz offset	–145	–145	–145	dBc/Hz
phn_{1M}	Phase noise at 1-MHz offset	–150	–150	–150	dBc/Hz
phn_{2M}	Phase noise at 2-MHz offset	–154	–154	–154	dBc/Hz
phn_{10M}	Phase noise at 10-MHz offset	–165	–162	–164	dBc/Hz
phn_{20M}	Phase noise at 20-MHz offset	–165	–162	–164	dBc/Hz

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).

6.18 Typical 161.1328125 MHz Output Phase Noise Characteristics(1)(2)

VDD = 3.3 V, T_A = 25°C, PLL bandwidth = 400 kHz, VCO Frequency = 5.15625 GHz, Fractional-N PLL, Output Divider = 32, Output Type = LVPECL/LVDS/HCSL

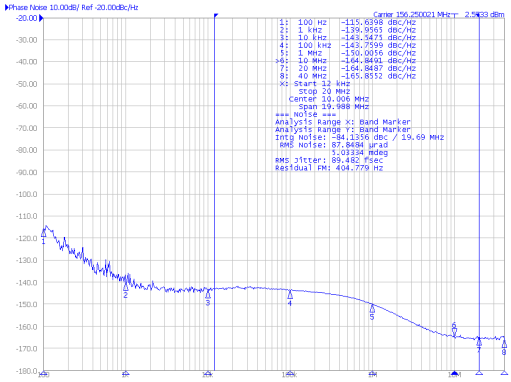
PARAMETER		OUTPUT TYPE			UNIT
		LVPECL	LVDS	HCSL	
phn_{10k}	Phase noise at 10-kHz offset	–136	–136	–136	dBc/Hz
phn_{20k}	Phase noise at 20-kHz offset	–136	–136	–136	dBc/Hz
phn_{100k}	Phase noise at 100-kHz offset	–140	–140	–140	dBc/Hz
phn_{200k}	Phase noise at 200-kHz offset	–141	–141	–141	dBc/Hz
phn_{1M}	Phase noise at 1-MHz offset	–148	–148	–148	dBc/Hz
phn_{2M}	Phase noise at 2-MHz offset	–156	–156	–156	dBc/Hz
phn_{10M}	Phase noise at 10-MHz offset	–161	–159	–160	dBc/Hz
phn_{20M}	Phase noise at 20-MHz offset	–162	–160	–161	dBc/Hz

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).

6.19 Additional Reliability and Qualification

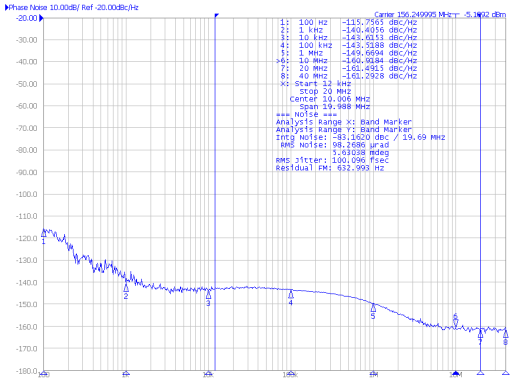
PARAMETER	CONDITION / TEST METHOD
Mechanical Shock	MIL-STD-202, Method 213
Mechanical Vibration	MIL-STD-202, Method 204
Moisture Sensitivity Level	J-STD-020, MSL3

6.20 Typical Characteristics



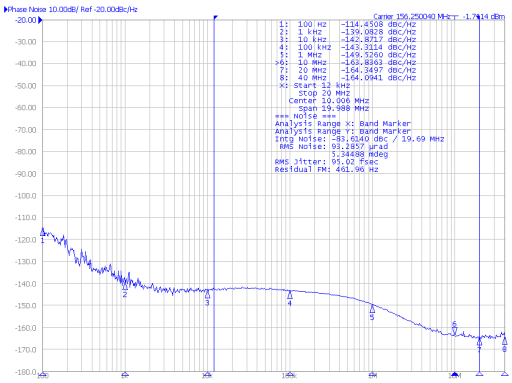
PLL Bandwidth = 400 kHz VCO Frequency = 5 GHz
Integer-N PLL Output Divider = 32

Figure 1. Closed-Loop Phase Noise of LVPECL Differential Output at 156.25 MHz



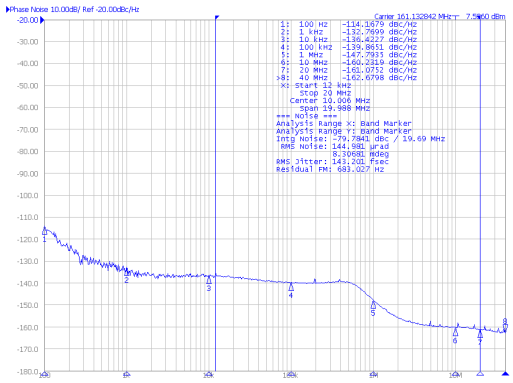
PLL Bandwidth = 400 kHz VCO Frequency = 5 GHz
Integer-N PLL Output Divider = 32

Figure 2. Closed-Loop Phase Noise of LVDS Differential Output at 156.25 MHz



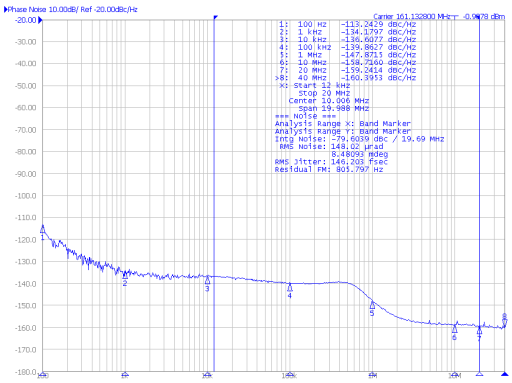
PLL Bandwidth = 400 kHz VCO Frequency = 5 GHz
Integer-N PLL Output Divider = 32

Figure 3. Closed-Loop Phase Noise of HCSL Differential Output at 156.25 MHz



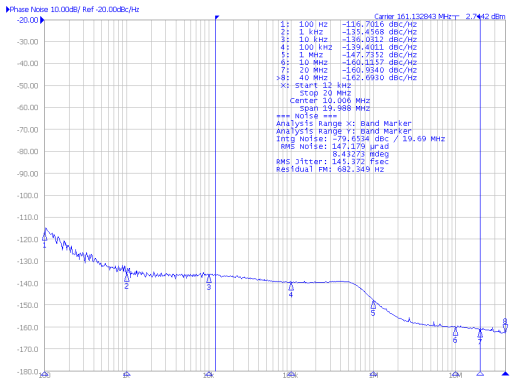
PLL Bandwidth = 400 kHz VCO Frequency = 5.15625 GHz
Fractional-N PLL Output Divider = 32

Figure 4. Closed-Loop Phase Noise of LVPECL Differential Output at 161.1328125 MHz



PLL Bandwidth = 400 kHz VCO Frequency = 5.15625 GHz
Fractional-N PLL Output Divider = 32

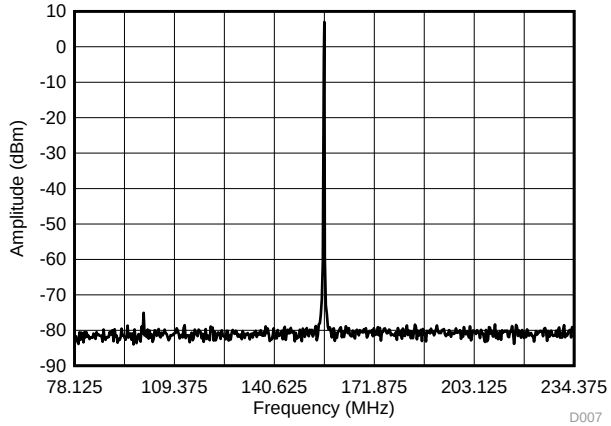
Figure 5. Closed-Loop Phase Noise of LVDS Differential Output at 161.1328125 MHz



PLL Bandwidth = 400 kHz VCO Frequency = 5.15625 GHz
Fractional-N PLL Output Divider = 32

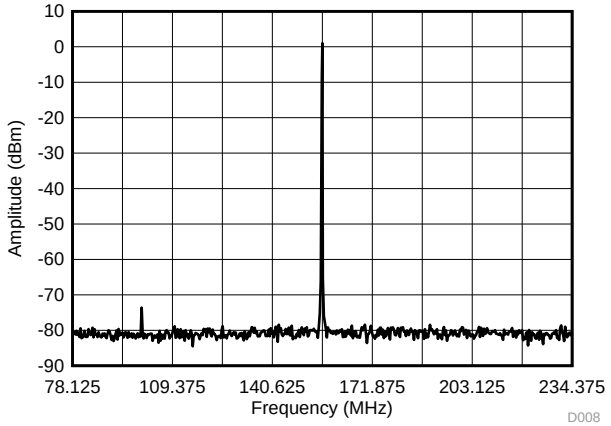
Figure 6. Closed-Loop Phase Noise of HCSL Differential Output at 161.1328125 MHz

Typical Characteristics (continued)



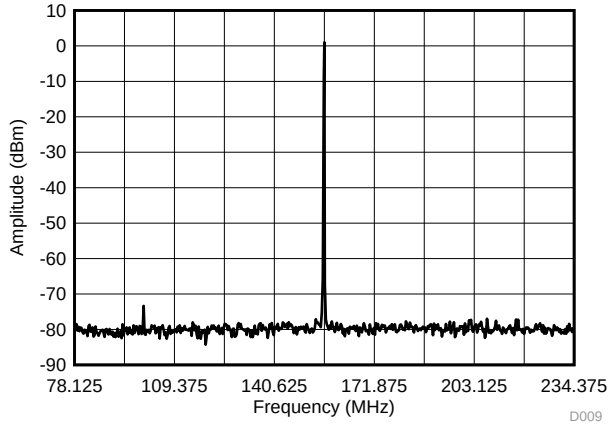
PLL Bandwidth = 400 kHz
Integer-N PLL
VCO Frequency = 5 GHz
Output Divider = 32

Figure 7. 156.25 ± 78.125-MHz LVPECL Differential Output Spectrum



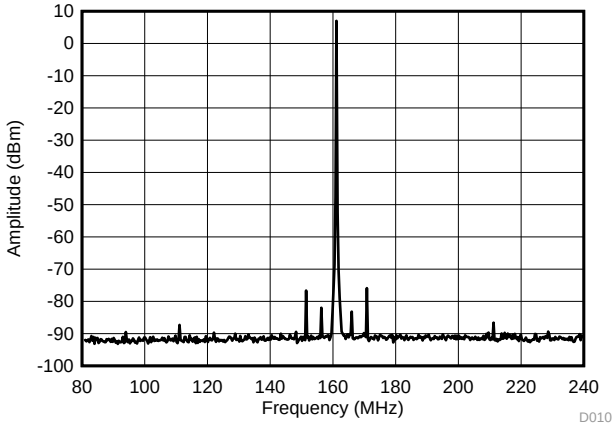
PLL Bandwidth = 400 kHz
Integer-N PLL
VCO Frequency = 5 GHz
Output Divider = 32

Figure 8. 156.25 ± 78.125-MHz LVDS Differential Output Spectrum



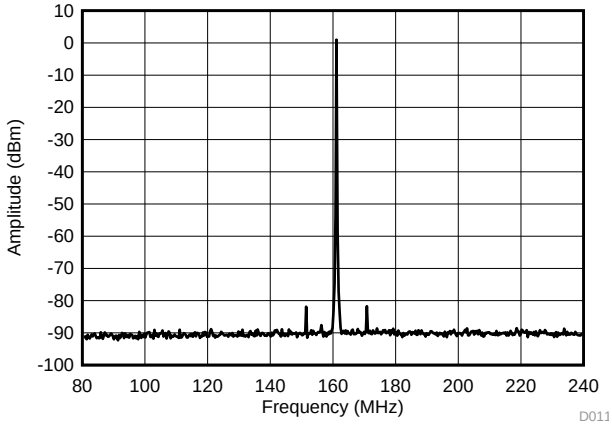
PLL Bandwidth = 400 kHz
Integer-N PLL
VCO Frequency = 5 GHz
Output Divider = 32

Figure 9. 156.25 ± 78.125-MHz HCSL Differential Output Spectrum



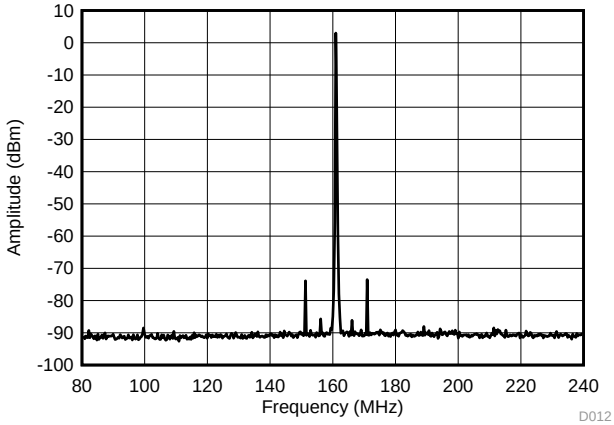
PLL Bandwidth = 400 kHz
Fractional-N PLL
VCO Frequency = 5.15625 GHz
Output Divider = 32

Figure 10. 161.1328125 ± 80.56640625-MHz LVPECL Differential Output Spectrum



PLL Bandwidth = 400 kHz
Fractional-N PLL
VCO Frequency = 5.15625 GHz
Output Divider = 32

Figure 11. 161.1328125 ± 80.56640625-MHz LVDS Output Spectrum



PLL Bandwidth = 400 kHz
Fractional-N PLL
VCO Frequency = 5.15625 GHz
Output Divider = 32

Figure 12. 161.1328125 ± 80.56640625-MHz HCSL Output Spectrum

Typical Characteristics (continued)

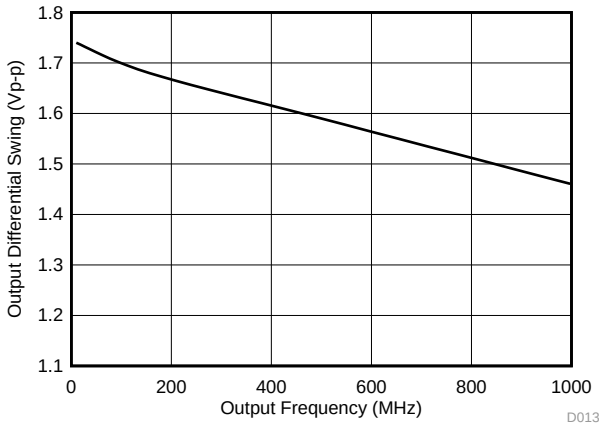


Figure 13. LVPECL Differential Output Swing vs Frequency

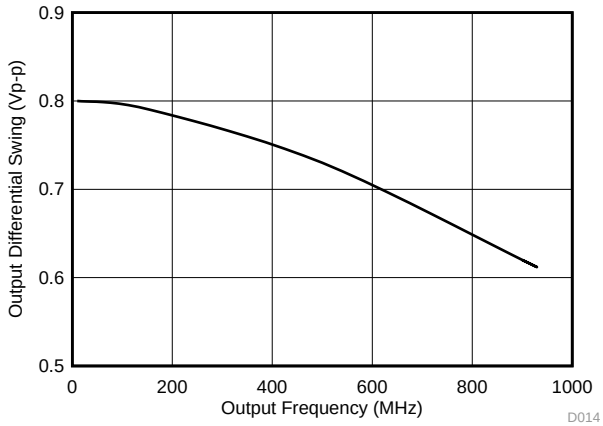


Figure 14. LVDS Differential Output Swing vs Frequency

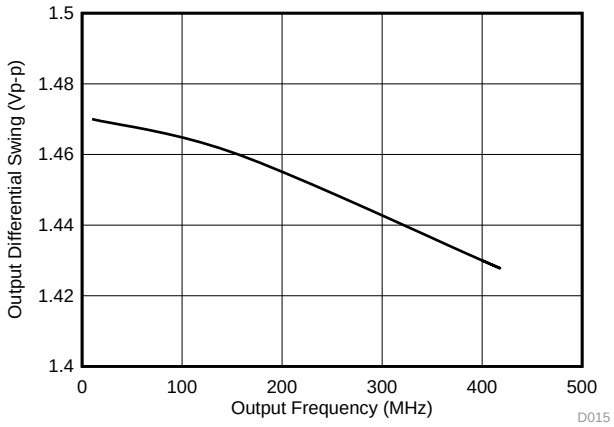


Figure 15. HCSL Differential Output Swing vs Frequency

7 Parameter Measurement Information

7.1 Device Output Configurations

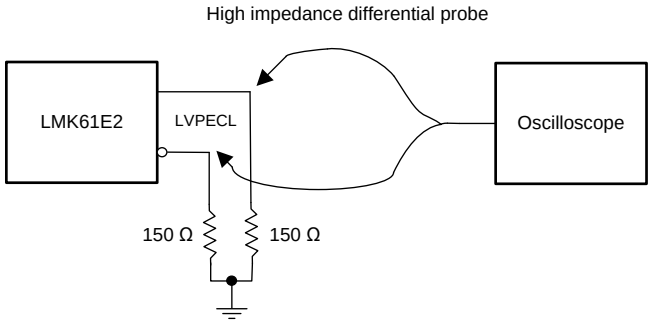


Figure 16. LVPECL Output DC Configuration During Device Test

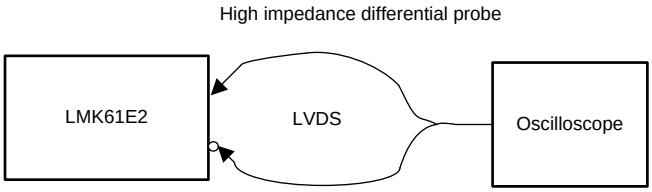


Figure 17. LVDS Output DC Configuration During Device Test

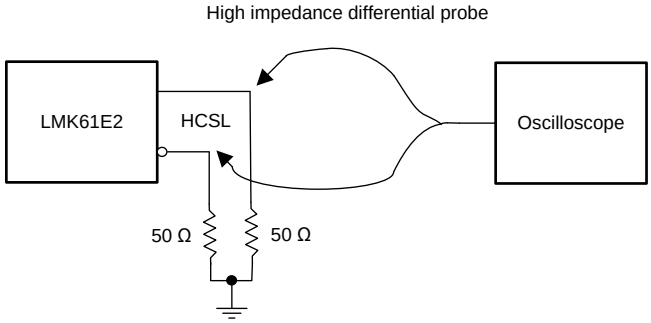


Figure 18. HCSL Output DC Configuration During Device Test

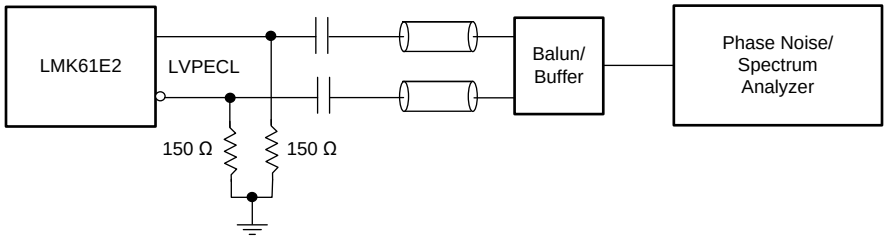


Figure 19. LVPECL Output AC Configuration During Device Test

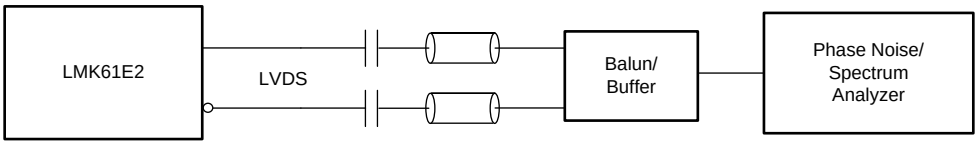


Figure 20. LVDS Output AC Configuration During Device Test

Device Output Configurations (continued)

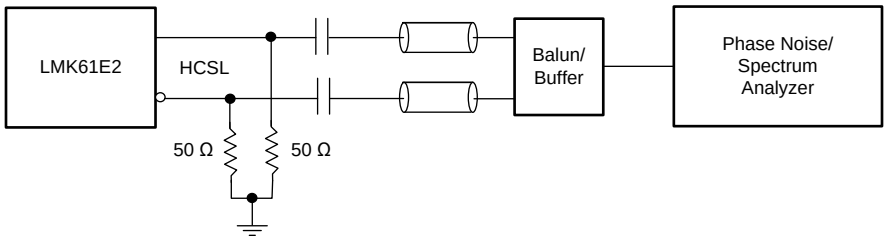


Figure 21. HCSL Output AC Configuration During Device Test

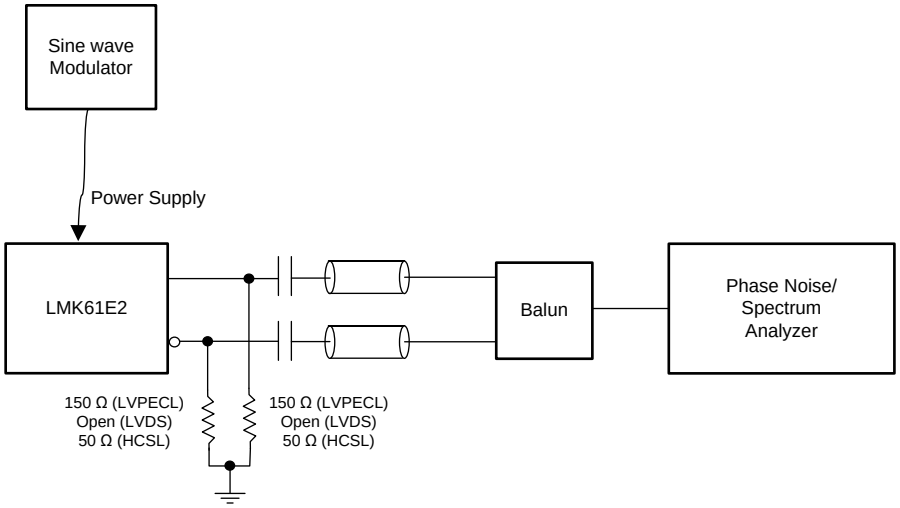


Figure 22. PSRR Test Setup

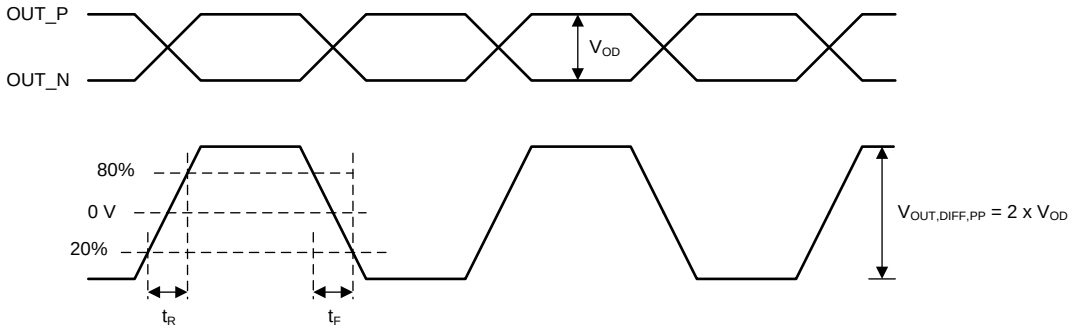


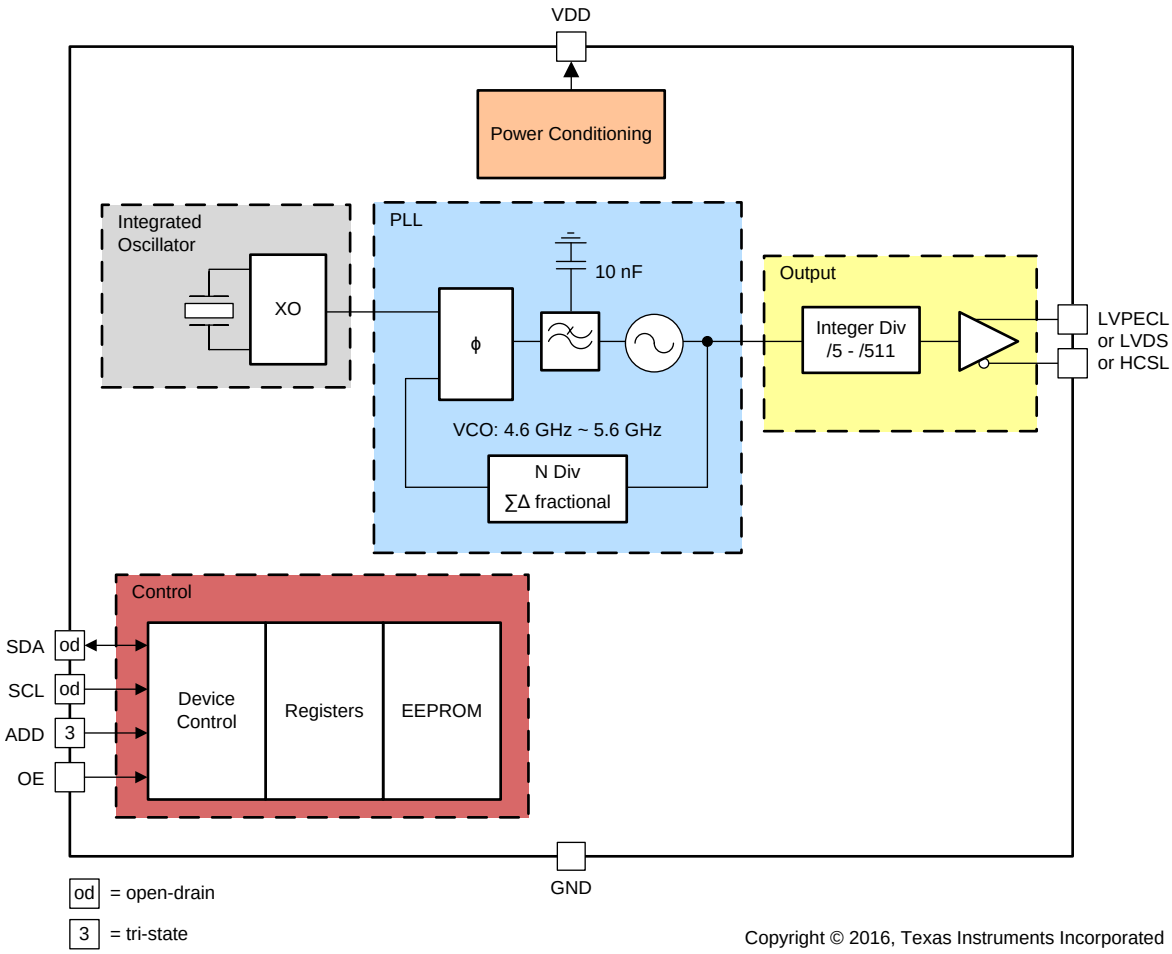
Figure 23. Differential Output Voltage and Rise/Fall Time

8 Detailed Description

8.1 Overview

The LMK61E2 is a programmable oscillator that generates commonly used reference clocks with less than 200-fs RMS maximum random jitter in integer PLL mode and less than 300-fs RMS maximum random jitter in fractional PLL mode.

8.2 Functional Block Diagram



NOTE

Control blocks are compatible with 1.8, 2.5, or 3.3-V I/O voltage levels.

8.3 Feature Description

8.3.1 Device Block-Level Description

The LMK61E2 comprises of an integrated oscillator that includes a 50-MHz crystal, a fractional PLL with integrated VCO that supports a frequency range of 4.6 GHz to 5.6 GHz. The PLL block consists of a phase frequency detector (PFD), charge pump, integrated passive loop filter, a feedback divider that can support both integer and fractional values and a delta-sigma engine for noise suppression in fractional PLL mode. Completing the device is the combination of an integer output divider and a universal differential output buffer. The PLL is powered by on-chip low dropout (LDO) linear voltage regulators and the regulated supply network is partitioned

Feature Description (continued)

such that the sensitive analog supplies are running from separate LDOs than the digital supplies which use their own LDO. The LDOs provide isolation to the PLL from any noise in the external power supply rail with a PSRR of better than –70 dBc at 50-kHz to 1-MHz ripple frequencies at 3.3-V device supply. The device supports fine and coarse frequency margining by changing the settings of the integrated oscillator and the output divider respectively.

8.3.2 Device Configuration Control

The LMK61E2 supports I^2C programming interface where an I^2C host can update any device configuration after the device enables the host interface and the host writes a sequence that updates the device registers. Once the device configuration is set, the host can also write to the on-chip EEPROM for a new set of power-up defaults based on the configuration pin settings in the soft pin configuration mode.

8.3.3 Register File Reference Convention

Figure 24 shows the method that this document employs to refer to an individual register bit or a grouping of register bits. If a drawing or text references an individual bit the format is to specify the register number first and the bit number second. The LMK61E2 contains 38 registers that are 8 bits wide. The register addresses and the bit positions both begin with the number zero (0). A period separates the register address and bit address. The first bit in the register file is address 'R0.0' meaning that it is located in Register 0 and is bit position 0. The last bit in the register file is address 'R72.7' referring to the 8th bit of register address 72 (the 73rd register in the device). Figure 24 also lists specific bit positions as a number contained within a box. A box with the register address encloses the group of boxes that represent the bits relevant to the specific device circuitry in context.

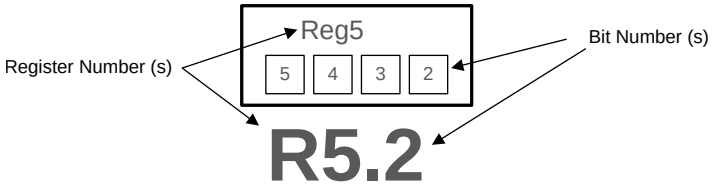


Figure 24. LMK61E2 Register Reference Format

8.3.4 Configuring the PLL

The PLL in LMK61E2 can be configured to accommodate various output frequencies either through I^2C programming interface or in the absence of programming, the PLL defaults stored in EEPROM is loaded on power up. The PLL can be configured by setting the Reference Doubler, Integrated PLL Loop Filter, Feedback Divider, and Output Divider.

For the PLL to operate in closed-loop mode, the following condition in Equation 1 has to be met.

$$F_{VCO} = F_{REF} \times D \times [(INT + NUM/DEN)] \quad (1)$$

where

- F_{VCO}: PLL/VCO Frequency (4.6 GHz to 5.6 GHz)
- F_{REF}: 50-MHz reference input
- D: PLL input frequency doubler, 1=Disabled, 2=Enabled
- INT: PLL feedback divider integer value (12 bits, 1 to 4095)
- NUM: PLL feedback divider fractional numerator value (22 bits, 0 to 4194303)
- DEN: PLL feedback divider fractional denominator value (22 bits, 1 to 4194303)

The output frequency is related to the VCO frequency as given in Equation 2.

$$F_{OUT} = F_{VCO} / OUTDIV \quad (2)$$

where

- OUTDIV: Output divider value (9 bits, 5 to 511)

Feature Description (continued)

8.3.5 Integrated Oscillator

The integrated oscillator in LMK61E2 features programmable load capacitances that can be set to either operate at exactly its nominal oscillation frequency or operate at a fixed frequency offset from its nominal oscillation frequency. This is done by programming R16 and R17. More details on frequency margining are provided in *Fine Frequency Margining*.

8.3.6 Reference Doubler

The reference path has a frequency doubler that can be enabled by programming R34.5 = 1. Enabling the doubler allows a higher comparison frequency for the PLL and would result in a 3-dB reduction in the in-band phase noise at the output of the LMK61E2. Enabling the doubler also results in higher reference and phase detector spurs which will be minimized by enabling the higher order components (R3, C3) of the loop filter and programmed to appropriate values. Disabling the doubler would result in higher in-band phase noise on the device output than when the doubler is enabled but the reference and phase detector spurs would be lower on the device output than when the doubler is enabled.

8.3.7 Phase Frequency Detector

The Phase Frequency Detector (PFD) of the PLL takes inputs from the reference path and the feedback divider output and produces an output that is dependent on the phase and frequency difference between the two inputs. The input frequency of the PFD is 50 MHz when reference doubler is disabled, or 100 MHz when reference doubler is enabled.

8.3.8 Feedback Divider (N)

The N divider of the PLL includes fractional compensation and can achieve any fractional denominator (DEN) from 1 to 4,194,303. The integer portion, INT, is the whole part of the N divider value and the fractional portion, NUM / DEN, is the remaining fraction. INT, NUM, and DEN are programmed in R25, R26, R27, R28, R29, R30, R31, and R32. The total programmed N divider value, N, is determined by: N = INT + NUM / DEN. The output of the N divider sets the PFD frequency to the PLL and should equal 50 MHz, when reference doubler is disabled, or 100 MHz, when reference doubler is enabled.

8.3.9 Fractional Circuitry

The delta signal modulator is a key component of the fractional circuitry and is involved in noise shaping for better phase noise and spurs in the band of interest. The order of the delta sigma modulator is selectable between integer mode and third order, for fractional PLL mode, and can be programmed in R33[1-0]. Dithering can be programmed in R33[3-2] and should be disabled for integer PLL mode and set to weak for fractional PLL mode.

8.3.10 Charge Pump

The PLL has charge pump slices of 1.6 mA, to be used when PLL is set to fractional mode, or 6.4 mA, to be used when PLL is set to integer mode. These slices can be selected by programming R34[3-0]. When PLL is set to fractional mode, a phase shift needs to be introduced to maintain a linear response and ensure consistent performance across operating conditions and a value of 0x2 should be programmed in R35[6-4]. When PLL is set to integer mode, a value of 0x0 should be programmed in R35[6-4].

8.3.11 Loop Filter

The LMK61E2 features a fully integrated loop filter for the PLL and supports programmable loop bandwidth from 100 kHz to 1 MHz. The loop filter components, R2, C1, R3, and C3 can be configured by programming R36, R37, R38, and R39 respectively. The LMK61E2 features a fixed value of C2 of 10 nF. When PLL is configured in the fractional mode, R35.2 should be set to 1. When reference doubler is disabled for integer mode PLL, R35.2 should be set to 0 and R38[6-0] should be set to 0x00. When reference doubler is enabled for integer mode PLL, R35.2 should be set to 1 and R38 and R39 are written with the appropriate values. Figure 25 shows the loop filter structure of the PLL. It is important to set the PLL to best possible bandwidth to minimize output jitter. TI provides the WEBENCH® Clock Architect Tool that makes it easy to select the right loop filter components.

Feature Description (continued)

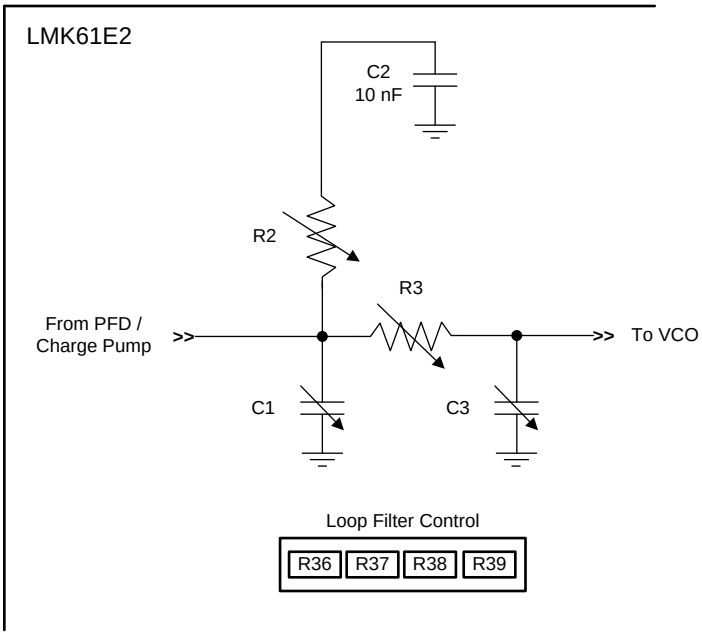


Figure 25. Loop Filter Structure of PLL

8.3.12 VCO Calibration

The PLL in LMK61E2 is made of LC VCO that is designed using high-Q monolithic inductors to oscillate between 4.6 GHz and 5.6 GHz and has low-phase noise characteristics. The VCO must be calibrated to ensure that the clock outputs deliver optimal phase noise performance. Fundamentally, a VCO calibration establishes an optimal operating point within the tuning range of the VCO. Setting R72.1 to 1 causes a VCO recalibration and is necessary after device reconfiguration. VCO calibration automatically occurs on device power up.

8.3.13 High-Speed Output Divider

The high-speed output divider supports divide values of 5 to 511 and are programmed in R22 and R23. The output divider also supports coarse frequency margining that can initiate as low as a 5% change in the output frequency.

8.3.14 High-Speed Clock Output

The clock output can be configured as LVPECL, LVDS, or HCSL by programming R21[1-0]. Interfacing to LVPECL, LVDS, or HCSL receivers are done either with direct coupling or with AC-coupling capacitor as shown in Figure 16 – Figure 21.

The LVDS output structure has integrated 125-Ω termination between each side (P and N) of the differential pair. The HCSL output structure is open drain and can be DC or AC coupled to HCSL receivers with appropriate termination scheme. The LVPECL output structure is an emitter follower requiring external termination.

8.3.15 Device Status

The PLL loss of lock and PLL calibration status can be monitored by reading R66[1-0]. These bits represent a logic-high interrupt output and are self-cleared once the readback is complete.

8.3.15.1 Loss of Lock

The PLL loss of lock detection circuit is a digital circuit that detects any frequency error, even a single cycle slip. Loss of lock may occur when an incorrect PLL configuration is programmed or the VCO has not been recalibrated.

8.4 Device Functional Modes

8.4.1 Interface and Control

The host (DSP, Microcontroller, FPGA, and so forth) configures and monitors the LMK61E2 through the I^2C port. The host reads and writes to a collection of control and status bits called the register map. The device blocks can be controlled and monitored through a specific grouping of bits located within the register file. The host controls and monitors certain device Wide critical parameters directly through register control and status bits. In the absence of the host, the LMK61E2 can be configured to operate from its on-chip EEPROM. The EEPROM array is automatically copied to the device registers upon power up. The user has the flexibility to rewrite the contents of EEPROM from the SRAM up to a 100 times.

Within the device registers, there are certain bits that have read or write access. Other bits are read-only (an attempt to write to a read-only bit does not change the state of the bit). Certain device registers and bits are reserved, meaning that they must not be changed from their default reset state. Figure 26 shows interface and control blocks within LMK61E2 and the arrows refer to read access from and write access to the different embedded memories (EEPROM, SRAM).

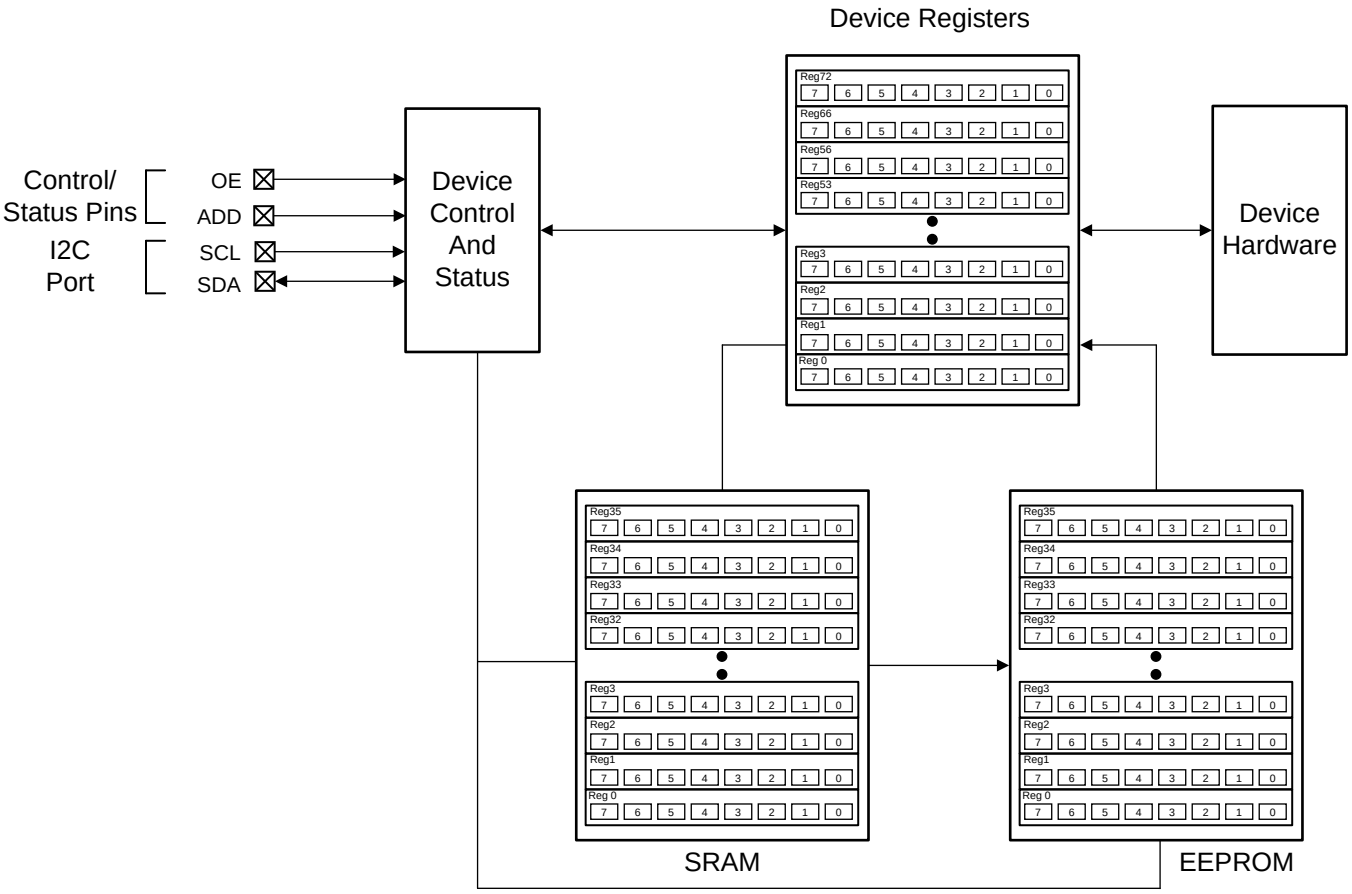


Figure 26. LMK61E2 Interface and Control Block

8.5 Programming

8.5.1 I²C Serial Interface

The I²C port on the LMK61E2 works as a slave device and supports both the 100-kHz standard mode and 400-kHz fast mode operations. Fast mode imposes a glitch tolerance requirement on the control signals. Therefore, the input receivers ignore pulses of less than 50 ns duration. The I²C timing is given in *I²C-Compatible Interface Characteristics (SDA, SCL)*(1)(2). The timing diagram is given in Figure 27.

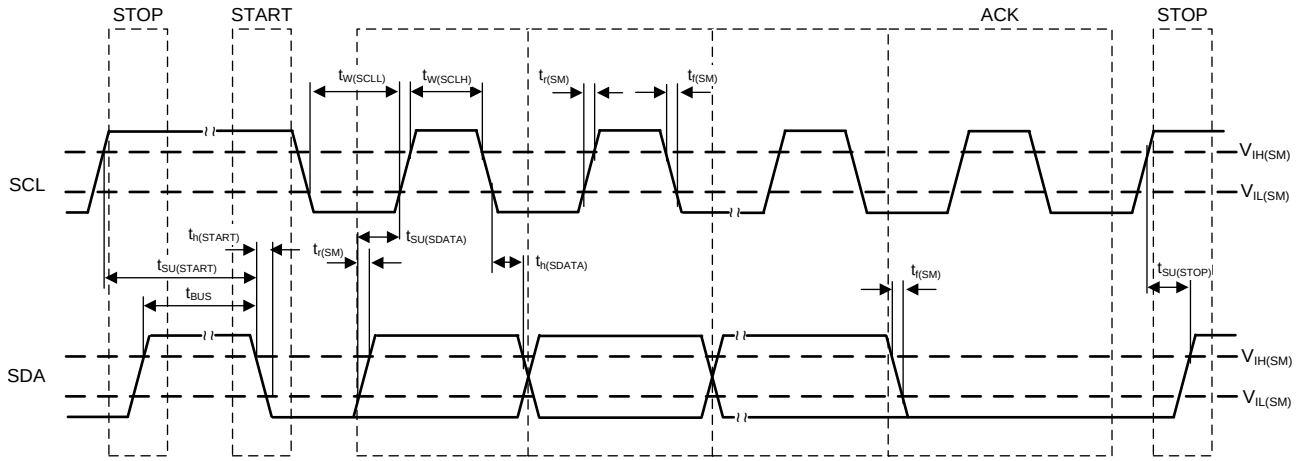


Figure 27. I²C Timing Diagram

In an I²C bus system, the LMK61E2 acts as a slave device and is connected to the serial bus (data bus SDA and lock bus SCL). These are accessed via a 7-bit slave address transmitted as part of an I²C packet. Only the device with a matching slave address responds to subsequent I²C commands. In soft pin mode, the LMK61E2 allows up to three unique slave devices to occupy the I²C bus based on the pin strapping of ADD (tied to VDD, GND, or left open). The device slave address is 10110xx (the two LSBs are determined by the ADD pin).

During the data transfer through the I²C interface, one clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low. The start data transfer condition is characterized by a high-to-low transition on the SDA line while SCL is high. The stop data transfer condition is characterized by a low-to-high transition on the SDA line while SCL is high. The start and stop conditions are always initiated by the master. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit and bytes are sent MSB first. The I²C register structure of the LMK61E2 is shown in Figure 28.

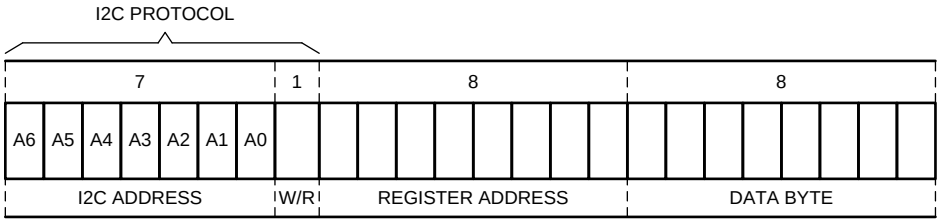


Figure 28. I²C Register Structure

The acknowledge bit (A) or non-acknowledge bit (A') is the 9th bit attached to any 8-bit data byte and is always generated by the receiver to inform the transmitter that the byte has been received (when A = 0) or not (when A' = 0). A = 0 is done by pulling the SDA line low during the 9th clock pulse and A' = 0 is done by leaving the SDA line high during the 9th clock pulse.

(1) Total capacitive load for each bus line ≤ 400 pF.
(2) Ensured by design.

Programming (continued)

The I^{2}C master initiates the data transfer by asserting a start condition which initiates a response from all slave devices connected to the serial bus. Based on the 8-bit address byte sent by the master over the SDA line (consisting of the 7-bit slave address (MSB first) and an R/W' bit), the device whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data transfer with the master.

After the data transfer has occurred, stop conditions are established. In write mode, the master asserts a stop condition to end data transfer during the 10th clock pulse following the acknowledge bit for the last data byte from the slave. In read mode, the master receives the last data byte from the slave but does not pull SDA low during the 9th clock pulse. This is known as a non-acknowledge bit. By receiving the non-acknowledge bit, the slave knows the data transfer is finished and enters the idle mode. The master then takes the data line low during the low period before the 10th clock pulse, and high during the 10th clock pulse to assert a stop condition. A generic transaction is shown in Figure 29.

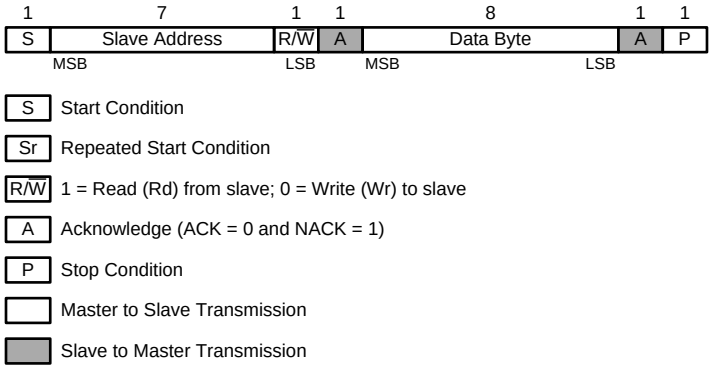


Figure 29. Generic Programming Sequence

The LMK61E2 I^{2}C interface supports *Block Register Write/Read*, *Read/Write SRAM*, and *Read/Write EEPROM* operations. For *Block Register Write/Read* operations, the I^{2}C master can individually access addressed registers that are made of an 8-bit data byte. The offset of the indexed register is encoded in the register address, as described in Table 1.

Table 1. Slave Address Byte

DEVICE	A6	A5	A4	A3	A2	ADD pin	R/$\overline{W}$
LMK61E2	1	0	1	1	0	0x0, 0x1 or 0x3	1/0

8.5.2 Block Register Write

The I^{2}C *Block Register Write* transaction is illustrated in Figure 30 and consists of the following sequence.

1. Master issues a Start Condition.
2. Master writes the 7-bit Slave Address following by a Write bit.
3. Master writes the 8-bit Register address as the CommandCode of the programming sequence.
4. Master writes one or more data bytes each of which should be acknowledged by the slave. The slave increments the internal register address after each byte.
5. Master issues a Stop Condition to terminate the transaction.

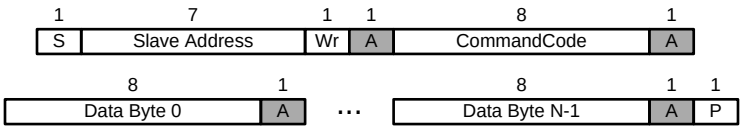


Figure 30. Block Register Write Programming Sequence

8.5.3 Block Register Read

The I^{2}C *Block Register Read* transaction is illustrated in Figure 31 and consists of the following sequence.

1. Master issues a Start Condition.
2. Master writes the 7-bit Slave Address followed by a Write bit.
3. Master writes the 8-bit Register address as the CommandCode of the programming sequence.
4. Master issues a Repeated Start Condition.
5. Master writes the 7-bit Slave Address following by a Read bit.
6. Slave returns one or more data bytes as long as the Master continues to acknowledge them. The slave increments the internal register address after each byte.
7. Master issues a Stop Condition to terminate the transaction.

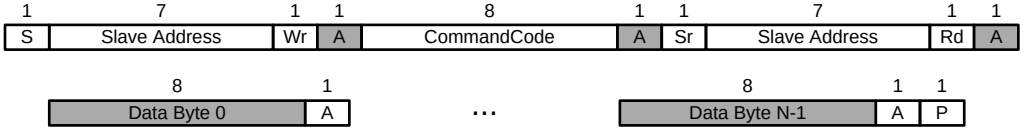


Figure 31. Block Register Read Programming Sequence

8.5.4 Write SRAM

The on-chip SRAM is a volatile, shadow memory array used to temporarily store register data, and is intended only for programming the non-Volatile EEPROM. The SRAM has the identical data format as the EEPROM map. The register configuration data can be transferred to the SRAM array through special memory access registers in the register map. To successfully program the SRAM, the complete base array and at least one page should be written. The following details the programming sequence to transfer the device registers into the SRAM.

1. Program the device registers to match a desired setting.
2. Write a 1 to R49.6. This ensures that the device registers are copied to the SRAM.

The SRAM can also be written with particular values according to the following programming sequence.

1. Write the SRAM address in R51.
2. Write the desired data byte in R53 in the same I^{2}C transaction and this data byte will be written to the address specified in the step above. Any additional access that is part of the same transaction will cause the SRAM address to be incremented and a write will take place to the next SRAM address. Access to SRAM will terminate at the end of current I^{2}C transaction.

NOTE

It is possible to increment SRAM address incorrectly when 2 successive accesses are made to R51.

8.5.5 Write EEPROM

The on-chip EEPROM is a non-Volatile memory array used to permanently store register data for a custom device start-up configuration setting to initialize registers upon power up or POR. The EEPROM is comprised of bits shown in the EEPROM Map. The transfer must first happen to the SRAM and then to the EEPROM. During *EEPROM write*, R49.2 is a 1 and the EEPROM contents cannot be accessed. The following details the programming sequence to transfer the entire contents of SRAM to EEPROM.

1. Make sure the *Write SRAM* procedure (Write SRAM) was done to commit the register settings to the SRAM with start-up configurations intended for programming to the EEPROM.
2. Write 0xBE to R56. This provides basic protection from inadvertent programming of EEPROM.
3. Write a 1 to R49.0. This programs the entire SRAM contents to EEPROM. Once completed, the contents in R48 will increment by 1. R48 contains the total number of EEPROM programming cycles that are successfully completed.
4. Write 0x00 to R56 to protect against inadvertent programming of EEPROM.

8.5.6 Read SRAM

The contents of the SRAM can be read out, one word at a time, starting with that of the requested address. Following details the programming sequence for an SRAM read by address.

1. Write the SRAM address in R51.
2. The SRAM data located at the address specified in the step above can be obtained by reading R53 in the same I^2C transaction. Any additional access that is part of the same transaction will cause the SRAM address to be incremented and a read will take place of the next SRAM address. Access to SRAM will terminate at the end of current I^2C transaction.

NOTE

It is possible to increment SRAM address incorrectly when 2 successive accesses are made to R51.

8.5.7 Read EEPROM

The contents of the EEPROM can be read out, one word at a time, starting with that of the requested address. Following details the programming sequence for an EEPROM read by address.

1. Write the EEPROM address in R51.
2. The EEPROM data located at the address specified in the step above can be obtained by reading R52 in the same I^2C transaction. Any additional access that is part of the same transaction will cause the EEPROM address to be incremented and a read will take place of the next EEPROM address. Access to EEPROM will terminate at the end of current I^2C transaction.

NOTE

It is possible to increment EEPROM address incorrectly when 2 successive accesses are made to R51.

8.6 EEPROM Map

Any bit that is labeled as RESERVED should be written with a 0.

Byte #	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
1	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
2	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
3	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
4	NVMSCRC[7]	NVMSCRC[6]	NVMSCRC[5]	NVMSCRC[4]	NVMSCRC[3]	NVMSCRC[2]	NVMSCRC[1]	NVMSCRC[0]
5	NVMCNT[7]	NVMCNT[6]	NVMCNT[5]	NVMCNT[4]	NVMCNT[3]	NVMCNT[2]	NVMCNT[1]	NVMCNT[0]
6	1	RESERVED	RESERVED	RESERVED	RESERVED	1	RESERVED	RESERVED
7	RESERVED	RESERVED	1	RESERVED	RESERVED	RESERVED	RESERVED	1
8	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
9	SLAVEADR[7]	SLAVEADR[6]	SLAVEADR[5]	SLAVEADR[4]	SLAVEADR[3]	RESERVED	RESERVED	RESERVED
10	EEREV[7]	EEREV[6]	EEREV[5]	EEREV[4]	EEREV[3]	EEREV[2]	EEREV[1]	EEREV[0]
11	RESERVED	PLL_PDN	RESERVED	RESERVED	RESERVED	RESERVED	AUTOSTRT	RESERVED
14	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	1	RESERVED	1
15	RESERVED	XO_CAPCTRL[1]	XO_CAPCTRL[0]	XO_CAPCTRL[9]	XO_CAPCTRL[8]	XO_CAPCTRL[7]	XO_CAPCTRL[6]	XO_CAPCTRL[5]
16	XO_CAPCTRL[4]	XO_CAPCTRL[3]	XO_CAPCTRL[2]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
19	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OUT_SEL[2]
20	OUT_SEL[1]	OUT_SEL[0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
21	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
22	PLL_NDIV[11]	PLL_NDIV[10]	PLL_NDIV[9]	PLL_NDIV[8]	PLL_NDIV[7]	PLL_NDIV[6]	PLL_NDIV[5]	PLL_NDIV[4]
23	PLL_NDIV[3]	PLL_NDIV[2]	PLL_NDIV[1]	PLL_NDIV[0]	PLL_NUM[21]	PLL_NUM[20]	PLL_NUM[19]	PLL_NUM[18]
24	PLL_NUM[17]	PLL_NUM[16]	PLL_NUM[15]	PLL_NUM[14]	PLL_NUM[13]	PLL_NUM[12]	PLL_NUM[11]	PLL_NUM[10]
25	PLL_NUM[9]	PLL_NUM[8]	PLL_NUM[7]	PLL_NUM[6]	PLL_NUM[5]	PLL_NUM[4]	PLL_NUM[3]	PLL_NUM[2]
26	PLL_NUM[1]	PLL_NUM[0]	PLL_DEN[21]	PLL_DEN[20]	PLL_DEN[19]	PLL_DEN[18]	PLL_DEN[17]	PLL_DEN[16]
27	PLL_DEN[15]	PLL_DEN[14]	PLL_DEN[13]	PLL_DEN[12]	PLL_DEN[11]	PLL_DEN[10]	PLL_DEN[9]	PLL_DEN[8]
28	PLL_DEN[7]	PLL_DEN[6]	PLL_DEN[5]	PLL_DEN[4]	PLL_DEN[3]	PLL_DEN[2]	PLL_DEN[1]	PLL_DEN[0]
29	PLL_ DTHRMODE[1]	PLL_DTHRMODE[0]	PLL_ORDER[1]	PLL_ORDER[0]	RESERVED	RESERVED	PLL_D	PLL_CP[3]
30	PLL_CP[2]	PLL_CP[1]	PLL_CP[0]	PLL_CP_PHASE_ SHIFT[2]	PLL_CP_PHASE_ SHIFT[1]	PLL_CP_PHASE_ SHIFT[0]	PLL_ENABLE_ C3[2]	PLL_ENABLE_ C3[1]
31	PLL_ENABLE_ C3[0]	PLL_LF_R2[7]	PLL_LF_R2[6]	PLL_LF_R2[5]	PLL_LF_R2[4]	PLL_LF_R2[3]	PLL_LF_R2[2]	PLL_LF_R2[1]
32	PLL_LF_R2[0]	PLL_LF_C1[2]	PLL_LF_C1[1]	PLL_LF_C1[0]	PLL_LF_R3[6]	PLL_LF_R3[5]	PLL_LF_R3[4]	PLL_LF_R3[3]
33	PLL_LF_R3[2]	PLL_LF_R3[1]	PLL_LF_R3[0]	PLL_LF_C3[2]	PLL_LF_C3[1]	PLL_LF_C3[0]	RESERVED	RESERVED

EEPROM Map (continued)

Byte #	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
34	RESERVED	OUT_DIV[8]	OUT_DIV[7]	OUT_DIV[6]	OUT_DIV[5]	OUT_DIV[4]	OUT_DIV[3]	OUT_DIV[2]
35	OUT_DIV[1]	OUT_DIV[0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

8.7 Register Map

The default/reset values for each register is specified for LMK61E2-I3.

Name	Addr	Reset	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VNDRID_BY1	0	0x10	VNDRID[15:8]							
VNDRID_BY0	1	0x0B	VNDRID[7:0]							
PRODID	2	0x33	PRODID[7:0]							
REVID	3	0x00	REVID[7:0]							
SLAVEADR	8	0xB0	SLAVEADR[7:1]							RESERVED
EEREV	9	0x00	EEREV[7:0]							
DEV_CTL	10	0x01	RESERVED	PLL_PDN	RESERVED				ENCAL	AUTOSTRT
XO_CAPCTRL_BY1	16	0x00	RESERVED						XO_CAPCTRL[1:0]	
XO_CAPCTRL_BY0	17	0x00	XO_CAPCTRL[9:2]							
DIFFCTL	21	0x01	DIFF_OUT_PD	RESERVED					OUT_SEL[1:0]	
OUTDIV_BY1	22	0x00	RESERVED							OUT_DIV[8]
OUTDIV_BY0	23	0x20	OUT_DIV[7:0]							
PLL_NDIV_BY1	25	0x00	RESERVED				PLL_NDIV[11:8]			
PLL_NDIV_BY0	26	0x64	PLL_NDIV[7:0]							
PLL_FRACNUM_BY2	27	0x00	RESERVED		PLL_NUM[21:16]					
PLL_FRACNUM_BY1	28	0x00	PLL_NUM[15:8]							
PLL_FRACNUM_BY0	29	0x00	PLL_NUM[7:0]							
PLL_FRACDEN_BY2	30	0x00	RESERVED		PLL_DEN[21:16]					
PLL_FRACDEN_BY1	31	0x00	PLL_DEN[15:8]							
PLL_FRACDEN_BY0	32	0x00	PLL_DEN[7:0]							
PLL_MASHCTRL	33	0x0C	RESERVED				PLL_DTHRMODE[1:0]		PLL_ORDER[1:0]	
PLL_CTRL0	34	0x24	RESERVED		PLL_D	RESERVED	PLL_CP[3:0]			
PLL_CTRL1	35	0x03	RESERVED	PLL_CP_PHASE_SHIFT[2:0]			RESERVED	PLL_ENABLE_C3[2:0]		
PLL_LF_R2	36	0x28	PLL_LF_R2[7:0]							
PLL_LF_C1	37	0x00	RESERVED					PLL_LF_C1[2:0]		
PLL_LF_R3	38	0x00	RESERVED	PLL_LF_R3[6:0]						

Register Map (continued)

Name	Addr	Reset	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PLL_LF_C3	39	0x00	RESERVED					PLL_LF_C3[2:0]		
PLL_CALCTRL	42	0x00	RESERVED				PLL_CLSDWAIT[1:0]		PLL_VCOWAIT[1:0]	
NVMSCRC	47	0x00	NVMSCRC[7:0]							
NVMCNT	48	0x00	NVMCNT[7:0]							
NVMCTL	49	0x10	RESERVED	REGCOMMIT	NVMCRCERR	NVMAUTOCRC	NVMCOMMIT	NVMBUSY	NVMERASE	NVMPROG
NVMLCRC	50	0x00	NVMLCRC[7:0]							
MEMADR	51	0x00	RESERVED	MEMADR[6:0]						
NVMDAT	52	0x00	NVMDAT[7:0]							
RAMDAT	53	0x00	RAMDAT[7:0]							
NVMUNLK	56	0x00	NVMUNLK[7:0]							
INT_LIVE	66	0x00	RESERVED						LOL	CAL
SWRST	72	0x00	RESERVED						SWR2PLL	RESERVED

8.7.1 Register Descriptions

8.7.1.1 VNDRID_BY1 Register; R0

VNDRID_BY1 and VNDRID_BY0 registers are used to store the unique 16-bit Vendor Identification number assigned to I^2C vendors.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	VNDRID[15:8]	R	0x10	N	Vendor Identification Number Byte 1.

8.7.1.2 VNDRID_BY0 Register; R1

VNDRID_BY1 and VNDRID_BY0 registers are used to store the unique 16-bit Vendor Identification number assigned to I^2C vendors.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	VNDRID[7:0]	R	0x0B	N	Vendor Identification Number Byte 0.

8.7.1.3 PRODID Register; R2

The Product Identification Number is a unique 8-bit identification number used to identify the LMK61E2.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	PRODID[7:0]	R	0x33	N	Product Identification Number.

8.7.1.4 REVID Register; R3

The REVID register is used to identify the LMK61E2 mask revision.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	REVID[7:0]	R	0x00	N	Device Revision Number. The Device Revision Number is used to identify the LMK61E2 mask-set revision used to fabricate this device.

8.7.1.5 SLAVEADR Register; R8

The SLAVEADR register reflects the 7-bit I^2C Slave Address value initialized from from on-chip EEPROM.

Bit #	Field	Type	Reset	EEPROM	Description	
[7:1]	SLAVEADR[7:1]	R	0x58	Y	I^2C Slave Address. This field holds the 7-bit Slave Address used to identify this device during I^2C transactions. The two least significant bits of the address can be configured using ADD pin as shown.	
					SLAVEADR[2:1]	**ADD pin**
					0 (0x0)	0
					1 (0x1)	Float
					3 (0x3)	1
[0]	RESERVED	-	-	N	Reserved.	

8.7.1.6 EEREV Register; R9

The EEREV register provides an EEPROM image revision record. EEPROM Image Revision is automatically retrieved from EEPROM and stored in the EEREV register after a reset or after a EEPROM commit operation.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	EEREV[7:0]	R	0x00	Y	EEPROM Image Revision ID

8.7.1.7 DEV_CTL Register; R10

The DEV_CTL register holds the control functions described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description
[7]	RESERVED	-	0	Y	Reserved.
[6]	PLL_PDN	RW	0	Y	PLL Powerdown. The PLL_PDN bit determines whether PLL is automatically enabled and calibrated after a hardware reset. If the PLL_PDN bit is set to 1 during normal operation then PLL is disabled and the calibration circuit is reset. When PLL_PDN is then cleared to 0 PLL is re-enabled and the calibration sequence is automatically restarted.
					PLL_PDN / **Value**: 0 / PLL Enabled; 1 / PLL Disabled
[5:2]	RESERVED[5:2]	RW	0	Y	Reserved.
[1]	ENCAL	RWSC	0	N	Enable Frequency Calibration. Triggers PLL/VCO calibration on both PLLs in parallel on 0 –> 1 transition of ENCAL. This bit is self-clearing and set to a 0 after PLL/VCO calibration is complete. In powerup or software rest mode, AUTOSTRT takes precedence.
[0]	AUTOSTRT	RW	1	Y	Autostart. If AUTOSTRT is set to 1 the device will automatically attempt to achieve lock and enable outputs after a device reset. A device reset can be triggered by the power-on-reset, RESETn pin or by writing to the RESETN_SW bit. If AUTOSTRT is 0 then the device will halt after the configuration phase, a subsequent write to set the AUTOSTRT bit to 1 will trigger the PLL Lock sequence.

8.7.1.8 XO_CAPCTRL_BY1 Register; R16

XO Margining Offset Value bits[9:8]

Bit #	Field	Type	Reset	EEPROM	Description
[7:2]	RESERVED[5:0]	-	-	N	Reserved.
[1:0]	XO_CAPCTRL [1:0]	RW	0x0	Y	XO Offset Value bits [1:0]

8.7.1.9 XO_CAPCTRL_BY0 Register; R17

XO margining Offset Value bits[7:0]

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	XO_CAPCTRL [9:2]	RW	0x80	Y	XO Offset Value bits[9:2]

8.7.1.10 DIFFCTL Register; R21

The DIFFCTL register provides control over Output.

Bit #	Field	Type	Reset	EEPROM	Description	
[7]	DIFF_OUT_PD	RW	0	N	Power down differential output buffer.	
[6:2]	RESERVED	-	-	N	Reserved.	
[1:0]	OUT_SEL[1:0]	RW	0x1	Y	Channel Output Driver Format Select. The OUT_SEL field controls the Channel Output Driver as shown below.	
					OUT_SEL	**OUTPUT OPERATION**
					0 (0x0)	Tri-State
					1 (0x1)	LVPECL
					2 (0x2)	LVDS
					3 (0x3)	HCSL

8.7.1.11 OUTDIV_BY1 Register; R22

The 9-bit output integer divider value is set by the OUTDIV_BY1 and OUTDIV_BY0 registers.

Bit #	Field	Type	Reset	EEPROM	Description	
[7:1]	RESERVED	RW	0x00	Y	Reserved.	
[0]	OUT_DIV[8]	RW	0	Y	Channel's Output Divider Byte 1 (Bit 8). The Channel Divider, OUT_DIV, is a 9-bit divider. The valid values for OUT_DIV range from 5 to 511 as shown below.	
					OUT_DIV	**DIVIDE RATIO**
					0-4	RESERVED
					5 (0x005)	5
					6 (0x006)	6
					7 (0x007)	7
					255 (0x0FF)	255
					256 (0x100)	256
					257 (0x101)	257
					...	...
					511 (0x1FF)	511

8.7.1.12 OUTDIV_BY0 Register; R23

The 9-bit output integer divider value is set by the OUTDIV_BY1 and OUTDIV_BY0 registers.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	OUT_DIV[7:0]	RW	0x20	Y	Channel's Output Divider Byte 0 (Bits 7-0).

8.7.1.13 PLL_NDIV_BY1 Register; R25

The 12-bit N integer divider value for PLL is set by the PLL_NDIV_BY1 and PLL_NDIV_BY0 registers.

Bit #	Field	Type	Reset	EEPROM	Description
[7:4]	RESERVED	-	-	N	Reserved.
[3:0]	PLL_NDIV[11:8]	RW	0x0	Y	PLL N Divider Byte 1. PLL Integer N Divider bits [11:8].

8.7.1.14 PLL_NDIV_BY0 Register; R26

The PLL_NDIV_BY0 register is described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	PLL_NDIV[7:0]	RW	0x32	Y	PLL N Divider Byte 0. PLL Integer N Divider bits [7:0].

8.7.1.15 PLL_FRACNUM_BY2 Register; R27

The 22-bit Fractional Divider Numerator value for PLL is set by registers PLL_FRACNUM_BY2, PLL_FRACNUM_BY1 and PLL_FRACNUM_BY0.

Bit #	Field	Type	Reset	EEPROM	Description
[7:6]	RESERVED	-	-	N	Reserved.
[5:0]	PLL_NUM[21:16]	RW	0x00	Y	PLL Fractional Divider Numerator Byte 2. Bits [21:16]

8.7.1.16 PLL_FRACNUM_BY1 Register; R28

The PLL_FRACNUM_BY1 register is described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	PLL_NUM[15:8]	RW	0x00	Y	PLL Fractional Divider Numerator Byte 1. Bits [15:8].

8.7.1.17 PLL_FRACNUM_BY0 Register; R29

The PLL_FRACNUM_BY0 register is described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	PLL_NUM[7:0]	RW	0x00	Y	PLL Fractional Divider Numerator Byte 0. Bits [7:0].

8.7.1.18 PLL_FRACDEN_BY2 Register; R30

The 22-bit Fractional Divider Denominator value for PLL is set by registers PLL_FRACDEN_BY2, PLL_FRACDEN_BY1 and PLL_FRACDEN_BY0.

Bit #	Field	Type	Reset	EEPROM	Description
[7:6]	RESERVED	-	-	N	Reserved.
[5:0]	PLL_DEN[21:16]	RW	0x00	Y	PLL Fractional Divider Denominator Byte 2. Bits [21:16].

8.7.1.19 PLL_FRACDEN_BY1 Register; R31

The PLL_FRACDEN_BY1 register is described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	PLL_DEN[15:8]	RW	0x00	Y	PLL Fractional Divider Denominator Byte 1. Bits [15:8].

8.7.1.20 PLL_FRACDEN_BY0 Register; R32

The PLL_FRACDEN_BY0 register is described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	PLL_DEN[7:0]	RW	0x00	Y	PLL Fractional Divider Denominator Byte 0. Bits [7:0].

8.7.1.21 PLL_MASHCTRL Register; R33

The PLL_MASHCTRL register provides control of the fractional divider for PLL.

Bit #	Field	Type	Reset	EEPROM	Description	
[7:4]	RESERVED	-	-	N	Reserved.	
[3:2]	PLL_DTHRMODE[1:0]	RW	0x3	Y	Mash Engine dither mode control.	
					DITHERMODE	**Dither Configuration**
					0 (0x0)	Weak
					1 (0x1)	Reserved
					2 (0x2)	Reserved
					3 (0x3)	Dither Disabled
[1:0]	PLL_ORDER[1:0]	RW	0x0	Y	Mash Engine Order.	
					ORDER	**Order Configuration**
					0 (0x0)	Integer Mode Divider
					1 (0x1)	Reserved
					2 (0x2)	Reserved
					3 (0x3)	3rd order

8.7.1.22 PLL_CTRL0 Register; R34

The PLL_CTRL1 register provides control of PLL. The PLL_CTRL1 register fields are described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description	
[7:6]	RESERVED	RW	0x0	Y	Reserved.	
[5]	PLL_D	RW	1	Y	PLL R Divider Frequency Doubler Enable. If PLL_D is 1 the R Divider Frequency Doubler is enabled.	
[4]	RESERVED	-	-	N	Reserved.	
[3:0]	PLL_CP[3:0]	RW	0x8	Y	PLL Charge Pump Current. Other combinations of PLL_CP[3:0] not in table below are reserved and not supported.	
					PLL_CP[3:0]	PLL Charge Pump Current
					4 (0x4)	1.6 mA
					8 (0x8)	6.4 mA

8.7.1.23 PLL_CTRL1 Register; R35

The PLL_CTRL3 register provides control of PLL. The PLL_CTRL3 register fields are described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description	
[7]	RESERVED	-	-	N	Reserved.	
[6:4]	PLL_CP_PHASE_SHIFT [2:0]	RW	0x0	Y	Program Charge Pump Phase Shift.	
					PLL_CP_PHASE_SHIFT[2:0]	**Phase Shift**
					0 (0x0)	No delay
					1 (0x1)	1.3 ns for 100 MHz f_{PD}
					2 (0x2)	1 ns for 100 MHz f_{PD}
					3 (0x3)	0.9 ns for 100 MHz f_{PD}
					4 (0x4)	1.3 ns for 50 MHz f_{PD}
					5 (0x5)	1 ns for 50 MHz f_{PD}
					6 (0x6)	0.9 ns for 50 MHz f_{PD}
					7 (0x7)	0.7 ns for 50 MHz f_{PD}
[3]	RESERVED	-	-	N	Reserved.	
[2]	PLL_ENABLE_C3	RW	0	Y	Disable third order capacitor in the low pass filter.	
					PLL_ENABLE_C3	**MODE**
					0	2nd order loop filter recommended setting
					1	Enables C3, 3rd order loop filter enabled
[1:0]	RESERVED	-	0x3	Y	Reserved.	

8.7.1.24 PLL_LF_R2 Register; R36

The PLL_LF_R2 register controls the value of the PLL Loop Filter R2.

Bit #	Field	Type	Reset	EEPROM	Description	
[7:0]	PLL_LF_R2[7:0]	RW	0x08	Y	PLL Loop Filter R2. NOTE: Table below lists commonly used R2 values but more selections are available.	
					PLL_LF_R2[7:0]	**R2 (Ω)**
					1 (0x01)	200
					4 (0x04)	500
					8 (0x08)	700
					32 (0x20)	1600
					48 (0x30)	2400
					64 (0x40)	3200

8.7.1.25 PLL_LF_C1 Register; R37

The PLL_LF_C1 register controls the value of the PLL Loop Filter C1.

Bit #	Field	Type	Reset	EEPROM	Description
[7:3]	RESERVED	-	-	N	Reserved.
[2:0]	PLL_LF_C1[2:0]	RW	0x0	Y	PLL Loop Filter C1. The value in pF is given by 5 + 50 * PLL_LF_C1 (in decimal).

8.7.1.26 PLL_LF_R3 Register; R38

The PLL_LF_R3 register controls the value of the PLL Loop Filter R3.

Bit #	Field	Type	Reset	EEPROM	Description	
[7]	RESERVED	-	-	N	Reserved.	
[6:0]	PLL_LF_R3[6:0]	RW	0x00	Y	PLL Loop Filter R3. NOTE: Table below lists commonly used R3 values but more selections are available.	
					PLL_LF_R3[6:0]	**R3 (Ω)**
					0 (0x00)	18
					3 (0x03)	205
					8 (0x08)	854
					9 (0x09)	1136
					12 (0x0C)	1535
					17 (0x11)	1936
					20 (0x14)	2335

8.7.1.27 PLL_LF_C3 Register; R39

The PLL_LF_C3 register controls the value of the PLL Loop Filter C3.

Bit #	Field	Type	Reset	EEPROM	Description
[7:3]	RESERVED	-	-	N	Reserved.
[2:0]	PLL_LF_C3[2:0]	RW	0x0	Y	PLL Loop Filter C3. The value in pF is given by 5 * PLL_LF_C3 (in decimal).

8.7.1.28 PLL_CALCTRL Register; R42

The PLL_CALCTRL register is described in the following table.

Bit #	Field	Type	Reset	EEPROM	Description	
[7:4]	RESERVED	-	-	N	Reserved.	
[3:2]	PLL_CLSDWAIT[1:0]	RW	0x2	Y	Closed Loop Wait Period. The CLSDWAIT field sets the closed loop wait period. Recommended value is 0x2.	
					CLSDWAIT	**Anlog closed loop VCO stabilization time**
					0 (0x0)	150 µs
					1 (0x1)	300 µs
					2 (0x2)	500 µs
					3 (0x3)	2000 µs
[1:0]	PLL_VCOWAIT[1:0]	RW	0x1	Y	VCO Wait Period. Recommended value is 0x1.	
					VCOWAIT	**VCO stabilization time**
					0 (0x0)	20 µs
					1 (0x1)	400 µs
					2 (0x2)	4000 µs
					3 (0x3)	10000 µs

8.7.1.29 NVMSCRC Register; R47

The NVMSCRC register holds the Stored CRC (Cyclic Redundancy Check) byte that has been retreived from on-chip EEPROM.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	NVMSCRC[7:0]	R	0x00	Y	EEPROM Stored CRC.

8.7.1.30 NVMCNT Register; R48

The NVMCNT register is intended to reflect the number of on-chip EEPROM Erase/Program cycles that have taken place in EEPROM. The count is automatically incremented by hardware and stored in EEPROM.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	NVMCNT[7:0]	R	0x00	Y	EEPROM Program Count. The NVMCNT increments automatically after every EEPROM Erase/Program Cycle. The NVMCNT value is retreived automatically after reset, after a EEPROM Commit operation or after a Erase/Program cycle. The NVMCNT register will increment until it reaches its maximum value of 255 after which no further increments will take place.

8.7.1.31 NVMCTL Register; R49

The NVMCTL register allows control of the on-chip EEPROM Memories.

Bit #	Field	Type	Reset	EEPROM	Description
[7]	RESERVED	-	-	N	Reserved.
[6]	REGCOMMIT	RWSC	0	N	REG Commit to EEPROM SRAM Array. The REGCOMMIT bit is used to initiate a transfer from the on-chip registers back to the corresponding location in the EEPROM SRAM Array. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete.
[5]	NVMCRCERR	R	0	N	EEPROM CRC Error Indication. The NVMCRCERR bit is set to 1 if a CRC Error has been detected when reading back from on-chip EEPROM during device configuration.
[4]	NVMAUTOCRC	RW	1	N	EEPROM Automatic CRC. When NVMAUTOCRC is 1 then the EEPROM Stored CRC byte is automatically calculated whenever a EEPROM program takes place.
[3]	NVMCOMMIT	RWSC	0	N	EEPROM Commit to Registers. The NVMCOMMIT bit is used to initiate a transfer of the on-chip EEPROM contents to internal registers. The transfer happens automatically after reset or when NVMCOMMIT is set to 1. The NVMCOMMIT bit is automatically cleared to 0. The I^2C registers cannot be read while a EEPROM Commit operation is taking place.
[2]	NVMBUSY	R	0	N	EEPROM Program Busy Indication. The NVMBUSY bit is 1 during an on-chip EEPROM Erase/Program cycle. While NVMBUSY is 1 the on-chip EEPROM cannot be accessed.
[1]	NVMERASE	RWSC	0	N	EEPROM Erase Start. The NVMERASE bit is used to begin an on-chip EEPROM Erase cycle. The Erase cycle is only initiated if the immediately preceding I^2C transaction was a write to the NVMUNLK register with the appropriate code. The NVMERASE bit is automatically cleared to 0. The EEPROM Erase operation takes around 115ms.
[0]	NVMPROG	RWSC	0	N	EEPROM Program Start. The NVMPROG bit is used to begin an on-chip EEPROM Program cycle. The Program cycle is only initiated if the immediately preceding I^2C transaction was a write to the NVMUNLK register with the appropriate code. The NVMPROG bit is automatically cleared to 0. If the NVMERASE and NVMPROG bits are set simultaneously then an ERASE/PROGRAM cycle will be executed The EEPROM Program operation takes around 115ms.

8.7.1.32 MEMADR Register; R51

The MEMADR register holds 7-bits of the starting address for on-chip SRAM or EEPROM access.

Bit #	Field	Type	Reset	EEPROM	Description
[7]	RESERVED	-	-	N	Reserved.
[6:0]	MEMADR[6:0]	RW	0x00	N	Memory Address. The MEMADR value determines the starting address for on-chip SRAM read/write access or on-chip EEPROM access. The internal address to access SRAM or EEPROM is automatically incremented; however the MEMADR register does not reflect the internal address in this way. When the SRAM or EEPROM arrays are accessed using the I^2C interface only bits [4:0] of MEMADR are used to form the byte Wise address.

8.7.1.33 NVMDAT Register; R52

The NVMDAT register returns the on-chip EEPROM contents from the starting address specified by the MEMADR register.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	NVMDAT[7:0]	R	0x00	N	EEPROM Read Data. The first time an I^2C read transaction accesses the NVMDAT register address, either because it was explicitly targeted or because the address was auto-incremented, the read transaction will return the EEPROM data located at the address specified by the MEMADR register. Any additional read's which are part of the same transaction will cause the EEPROM address to be incremented and the next EEPROM data byte will be returned. The I^2C address will no longer be auto-incremented, i.e the I^2C address will be locked to the NVMDAT register after the first access. Access to the NVMDAT register will terminate at the end of the current I^2C transaction.

8.7.1.34 RAMDAT Register; R53

The RAMDAT register provides read and write access to the SRAM that forms part of the on-chip EEPROM module.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	RAMDAT[7:0]	RW	0x00	N	RAM Read/Write Data. The first time an I^2C read or write transaction accesses the RAMDAT register address, either because it was explicitly targeted or because the address was auto-incremented, a read transaction will return the RAM data located at the address specified by the MEMADR register and a write transaction will cause the current I^2C data to be written to the address specified by the MEMADR register. Any additional accesses which are part of the same transaction will cause the RAM address to be incremented and a read or write access will take place to the next SRAM address. The I^2C address will no longer be auto-incremented, i.e the I^2C address will be locked to the RAMDAT register after the first access. Access to the RAMDAT register will terminate at the end of the current I^2C transaction.

8.7.1.35 NVMUNLK Register; R56

The NVMUNLK register provides a rudimentary level of protection to prevent inadvertent programming of the on-chip EEPROM.

Bit #	Field	Type	Reset	EEPROM	Description
[7:0]	NVMUNLK[7:0]	RW	0x00	N	EEPROM Prog Unlock. The NVMUNLK register must be written immediately prior to setting the NVMPROG bit of register NVMCTL, otherwise the Erase/Program cycle will not be triggered. NVMUNLK must be written with a value of 0xBE.

8.7.1.36 INT_LIVE Register; R66

The INT_LIVE register reflects the current status of the interrupt sources.

Bit #	Field	Type	Reset	EEPROM	Description
[7:2]	RESERVED	-	-	N	Reserved.
[1]	LOL	R	0	N	Loss of Lock PLL.
[0]	CAL	R	0	N	Calibration Active PLL.

8.7.1.37 SWRST Register; R72

The SWRST1 register provides software reset control for specific on-chip modules. Each bit in this register is individually self cleared after a write operation. The SWRST1 register will always return 0x00 in a read transaction.

Bit #	Field	Type	Reset	EEPROM	Description
[7:2]	RESERVED	-	-	N	Reserved.
[1]	SWR2PLL	RWSC	0	N	Software Reset PLL. Setting SWR2PLL to 1 resets the PLL calibrator and clock dividers. This bit is automatically cleared to 0.
[0]	RESERVED	-	-	N	Reserved.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMK61E2 is an ultra-low jitter programmable oscillator that can be used to provide reference clocks for high-speed serial links resulting in improved system performance. The LMK61E2 also supports a variety of features that aids the hardware designer during the system debug and validation phase.

9.2 Typical Applications

9.2.1 Jitter Considerations in Serdes Systems

Jitter-sensitive applications such as 10-Gbps or 100-Gbps Ethernet, deploy a serial link using a Serializer in the transmit section (TX) and a De-serializer in the receive section (RX). These SERDES blocks are typically embedded in an ASIC or FPGA. Estimating the clock jitter impact on the link budget requires understanding of the TX PLL bandwidth and the RX CDR bandwidth.

As can be seen in Figure 32, the pass band region between the TX low-pass cutoff and RX high-pass cutoff frequencies is the range over which the reference clock jitter adds without any attenuation to the jitter budget of the link. Outside of these frequencies, the SERDES link will attenuate the reference clock jitter with a 20 dB/dec or even steeper roll-off. Modern ASIC or FPGA designs have some flexibility on deciding the optimal RX CDR bandwidth and TX PLL bandwidth. These bandwidths are typically set based on what is achievable in the ASIC or FPGA process node, without increasing design complexity, and on any jitter tolerance or wander specification that needs to be met, as related to the RX CDR bandwidth.

The overall allowable jitter in a serial link is dictated by IEEE or other relevant standards. For example, IEEE802.3ba states that the maximum transmit jitter (peak-peak) for 10-Gbps Ethernet should be no more than 0.28 × UI and this equates to a 27.1516 ps, p-p for the overall allowable transmit jitter.

The jitter contributing elements are made up of the reference clock, generated potentially from a device like LMK61E2, the transmit medium, transmit driver, and so forth. Only a portion of the overall allowable transmit jitter is allocated to the reference clock, typically 20% or lower. Therefore, the allowable reference clock jitter, for a 20% clock jitter budget, is 5.43 ps, p-p.

Jitter in a reference clock is made up of deterministic jitter (arising from spurious signals due to supply noise or mixing from other outputs or from the reference input) and random jitter (usually due to thermal noise and other uncorrelated noise sources). A typical clock tree in a serial link system consists of clock generators and fanout buffers. The allowable reference clock jitter of 5.43 ps, p-p is needed at the output of the fanout buffer. Modern fanout buffers have low-additive random jitter (less than 100 fs RMS) with no substantial contribution to the deterministic jitter. Therefore, the clock generator and fanout buffer contribute to the random jitter while the primary contributor to the deterministic jitter is the clock generator. Rule of thumb, for modern clock generators, is to allocate 25% of allowable reference clock jitter to the deterministic jitter and 75% to the random jitter. This amounts to an allowable deterministic jitter of 1.36 ps, p-p and an allowable random jitter of 4.07 ps, p-p. For serial link systems that need to meet a bit error rate (BER) of 10^{-12}, the allowable random jitter in root-mean-square is 0.29 ps RMS. This is calculated by dividing the p-p jitter by 14 for a BER of 10^{-12}. Accounting for random jitter from the fanout buffer, the random jitter needed from the clock generator is 0.27 ps RMS. This is calculated by the root-mean-square subtraction from the desired jitter at the fanout buffer's output assuming 100 fs RMS of additive jitter from the fanout buffer.

With careful frequency planning techniques, like spur optimization (covered in *Spur Mitigation Techniques*) and on-chip LDOs to suppress supply noise, the LMK61E2 is able to generate clock outputs with deterministic jitter that is below 1 ps, p-p and random jitter that is below 0.2 ps RMS. This gives the serial link system with additional margin on the allowable transmit jitter resulting in a BER better than 10^{-12}.

Typical Applications (continued)

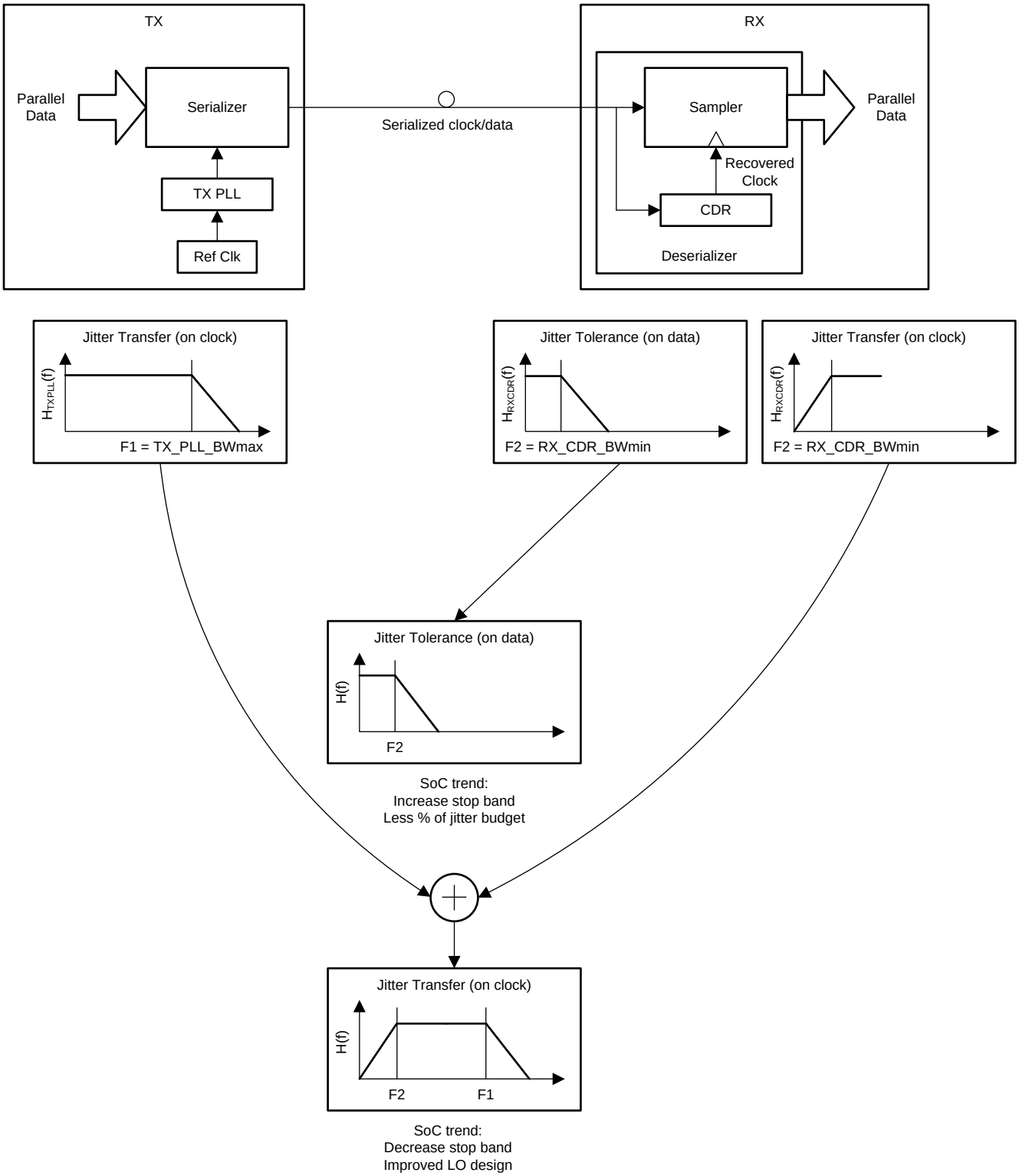


Figure 32. Dependence of Clock Jitter in Serial Links

Typical Applications (continued)

9.2.2 Frequency Margining

9.2.2.1 Fine Frequency Margining

IEEE802.3 dictates that Ethernet frames stay compliant to the standard specifications when clocked with a reference clock that is within ±100 ppm of its nominal frequency. In the worst case, an RX node with its local reference clock at –100 ppm from its nominal frequency should be able to work seamlessly with a TX node that has its own local reference clock at +100 ppm from its nominal frequency. Without any clock compensation on the RX node, the read pointer will severely lag behind the write pointer and cause FIFO overflow errors. On the contrary, when the RX node's local clock operates at +100 ppm from its nominal frequency and the TX node's local clock operates at –100 ppm from its nominal frequency, FIFO underflow errors occur without any clock compensation.

To prevent such overflow and underflow errors from occurring, modern ASICs and FGPAs include a clock compensation scheme that introduces elastic buffers. Such a system, shown in Figure 33, is validated thoroughly during the validation phase by interfacing slower nodes with faster ones and ensuring compliance to IEEE802.3. The LMK61E2 provides the ability to fine tune the frequency of its outputs based on changing its load capacitance for the integrated oscillator. This fine tuning can be done through I^2C as described in *Integrated Oscillator*. The change in load capacitance is implemented in a manner such that the output of LMK61E2 undergoes a smooth monotonic change in frequency.

9.2.2.2 Coarse Frequency Margining

Certain systems require the processors to be tested at clock frequencies that are slower or faster by 5% or 10%. The LMK61E2 offers the ability to change its output divider for the desired change from its nominal output frequency as explained in the *High-Speed Output Divider* section.

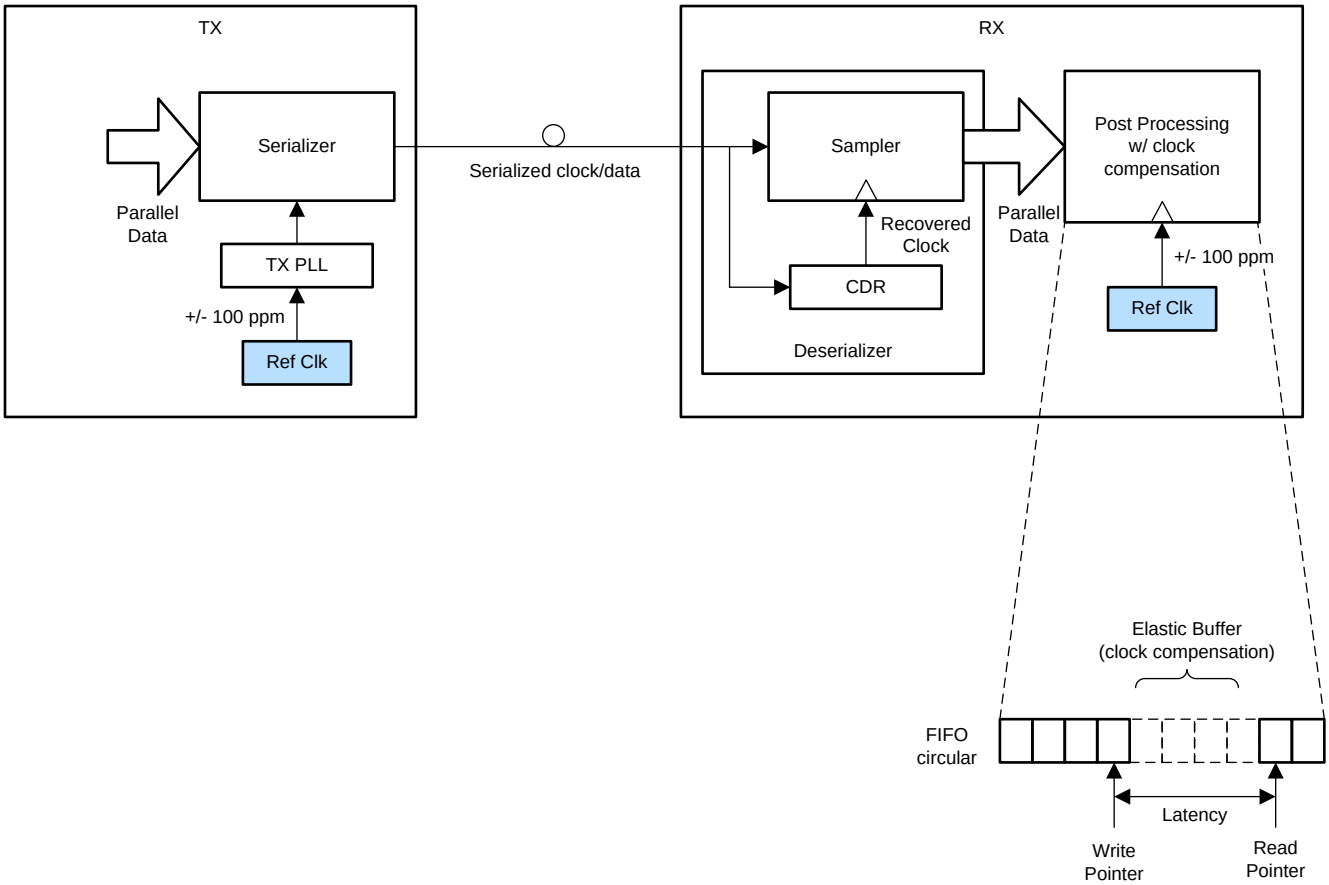


Figure 33. System Implementation With Clock Compensation for Standards Compliance

Typical Applications (continued)

9.2.3 Design Requirements

Consider a typical wired communications application, like a top-of-rack switch, which needs to clock high data rate 10-Gbps or 100-Gbps Ethernet PHYs. In such systems, the clock is expected to be available upon power up without the need for any device-level programming. An example of such a clock frequency would be a 156.25 MHz in LVPECL output format.

The *Detailed Design Procedure* below describes the detailed design procedure to generate the required output frequencies for the above scenario using LMK61E2.

9.2.3.1 Detailed Design Procedure

Design of all aspects of the LMK61E2 is simplified with software support that assists in part selection, part programming, loop filter design, and phase noise simulation. This design procedure will give a quick outline of the process.

1. Device Selection
   - The first step to calculate the specified VCO frequency given required output frequency. The device must be able to produce the VCO frequency that can be divided down to the required output frequency.
   - The WEBENCH Clock Architect Tool from TI will aid in the selection of the right device that meets the customer's output frequency and format requirements.
2. Device Configuration
   - There are many device configurations to achieve the desired output frequency from a device. However, the user should consider some optimizations and trade-offs.
   - The WEBENCH Clock Architect Tool attempts to maximize the phase detector frequency, use smallest dividers, and maximizes PLL charge pump current.
   - These guidelines below may be followed when configuring PLL related dividers or other related registers:
     - For lowest possible in-band PLL flat noise, maximize phase detector frequency to minimize N divide value.
     - For lowest possible in-band PLL flat noise, maximize charge pump current. The highest value charge pump currents often have similar performance due to diminishing returns.
     - For fractional divider values, keep the denominator at highest value possible in order to minimize spurs. It is also best to use higher order modulator wherever possible for the same reason.
     - As a rule of thumb, keeping the phase detector frequency approximately between 10 × PLL loop bandwidth and 100 × PLL loop bandwidth. A phase detector frequency less than 5 × PLL bandwidth may be unstable and a phase.
3. PLL Loop Filter Design
   - It is recommended to use the WEBENCH Clock Architect Tool to design your loop filter.
   - Optimal loop filter design and simulation can be achieved when custom reference phase noise profiles are loaded into the software tool.
   - While designing the loop filter, adjusting the charge pump current or N value can help with loop filter component selection. Lower charge pump currents and larger N values result in smaller component values but may increase impacts of leakage and reduce PLL phase noise performance.
   - For a more detailed understanding of loop filter design can be found in *PLL Performance, Simulation, and Design* (SNAA106).
4. Device Programming
   - The EVM programming software tool CodeLoader can be used to program the device with the desired configuration.

Typical Applications (continued)

9.2.3.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMK61E2 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.3.1.2 Device Selection

Use the WEBENCH Clock Architect Tool. Enter the required output frequencies and formats into the tool. To use this device, find a solution using the LMK61E2.

9.2.3.1.3 VCO Frequency Calculation

In this example, the VCO frequency of the LMK61E2 to generate 156.25 MHz can be calculated as 5 GHz.

9.2.3.1.4 Device Configuration

For this example, enter the desired output frequency and click on *Generate Solutions*. Select LMK61E2 from the solution list. From the simulation page of the WEBENCH Clock Architect Tool, it can be seen that to maximize phase detector frequency, PLL R divider is set to 1, doubler is enabled and N divider is set to 50 for a PFD frequency of 100 MHz. This results in a VCO frequency of 5 GHz. At this point the design meets the output frequency requirements and it is possible to design a loop filter for system and simulate performance on the clock output.

9.2.3.1.5 PLL Loop Filter Design

In the WEBENCH Clock Architect Tool simulator, click on the PLL loop filter design button, then press recommend design. For the PLL loop filter, maximum phase detector frequency and maximum charge pump current are typically used. The tool recommends a loop filter that is designed to minimize jitter. The integrated loop filter's components are minimized with this recommendation as to allow maximum flexibility in achieving wide loop bandwidths for low PLL noise. With the recommended loop filter calculated, this loop filter is ready to be simulated.

The PLL loop filter's bode plot can additionally be viewed and adjustments can be made to the integrated components. The effective loop bandwidth and phase margin with the updated values is then calculated. The integrated loop filter components are good to use when attempting to eliminate certain spurs. The recommended procedure is to increase C3 capacitance, then R3 resistance. Large R3 resistance can result in degraded VCO phase noise performance.

9.2.3.1.6 Spur Mitigation Techniques

The LMK61E2 offers several programmable features for optimizing fractional spurs. In order to get the best out of these features, it makes sense to understand the different kinds of spurs as well as their behaviors, causes, and remedies. Although optimizing spurs may involve some trial and error, there are ways to make this process more systematic. TI offers the *Clock Design Tool* for more information and estimation of fractional spurs.

Typical Applications (continued)

9.2.3.1.6.1 Phase Detection Spur

The phase detector spur occurs at an offset from the carrier equal to the phase detector frequency, f_{PD}. To minimize this spur, a lower phase detector frequency should be considered. In some cases where the loop bandwidth is very wide relative to the phase detector frequency, some benefit might be gained from using a narrower loop bandwidth or adding poles to the loop filter by using R3 and C3 if previously unused, but otherwise the loop filter has minimal impact. Bypassing at the supply pins and board layout can also have an impact on this spur, especially at higher phase detector frequencies.

9.2.3.1.6.2 Integer Boundary Fractional Spur

This spur occurs at an offset equal to the difference between the VCO frequency and the closest integer channel for the VCO. For instance, if the phase detector frequency is 100 MHz and the VCO frequency is 5003 MHz, then the integer boundary spur would be at 3-MHz offset. This spur can be either PLL or VCO dominated. If it is PLL dominated, decreasing the loop bandwidth and some of the programmable fractional words may impact this spur. If the spur is VCO dominated, then reducing the loop filter will not help, but rather reducing the phase detector and having good slew rate and signal integrity at the selected reference input will help.

9.2.3.1.6.3 Primary Fractional Spur

These spurs occur at multiples of f_{PD}/DEN and are not the integer boundary spur. For instance, if the phase detector frequency is 100 MHz and the fraction is 3/100, the primary fractional spurs would be at 1 MHz, 2 MHz, 4 MHz, 5 MHz, 6 MHz, and so forth. These are impacted by the loop filter bandwidth and modulator order. If a small frequency error is acceptable, then a larger equivalent fraction may improve these spurs. This larger unequivalent fraction pushes the fractional spur energy to much lower frequencies that where they are not impactful to the system performance.

9.2.3.1.6.4 Sub-Fractional Spur

These spurs appear at a fraction of f_{PD}/DEN and depend on modulator order. With the first order modulator, there are no sub-fractional spurs. The second order modulator can produce 1/2 sub-fractional spurs if the denominator is even. A third order modulator can produce sub-fractional spurs at 1/2, 1/3, or 1/6 of the offset, depending if it is divisible by 2 or 3. For instance, if the phase detector frequency is 100 MHz and the fraction is 3/100, no sub-fractional spurs for a first order modulator or sub-fractional spurs at multiples of 1.5 MHz for a second or third order modulator would be expected. Aside from strategically choosing the fractional denominator and using a lower order modulator, another tactic to eliminate these spurs is to use dithering and express the fraction in larger equivalent terms. Because dithering also adds phase noise, its level needs to be managed to achieve acceptable phase noise and spurious performance.

Typical Applications (continued)

Table 2 summarizes spur and mitigation techniques.

Table 2. Spur and Mitigation Techniques

SPUR TYPE	OFFSET	WAYS TO REDUCE	TRADE-OFFS
Phase Detector	f_{PD}	Reduce Phase Detector Frequency.	Although reducing the phase detector frequency does improve this spur, it also degrades phase noise.
Integer Boundary	f_{VCO} mod f_{PD}	**Methods for PLL Dominated Spurs**	Reducing the loop bandwidth may degrade the total integrated noise if the bandwidth is too narrow.
		- Avoid the worst case VCO frequencies if possible.	
		- Ensure good slew rate and signal integrity at reference input.	
		- Reduce loop bandwidth or add more filter poles to suppress out of band spurs.	
		Methods for VCO Dominated Spurs	Reducing the phase detector may degrade the phase noise.
		- Avoid the worst case VCO frequencies if possible.	
		- Reduce Phase Detector Frequency.	
		- Ensure good slew rate and signal integrity at reference input.	
Primary Fractional	f_{PD}/DEN	- Decrease Loop Bandwidth.	Decreasing the loop bandwidth may degrade in-band phase noise. Also, larger unequivalent fractions don't always reduce spurs.
		- Change Modulator Order.	
		- Use Larger Unequivalent Fractions.	
Sub-Fractional	f_{PD}/DEN/k k=2,3, or 6	- Use Dithering.	Dithering and larger fractions may increase phase noise.
		- Use Larger Equivalent Fractions.	
		- Use Larger Unequivalent Fractions.	
		- Reduce Modulator Order.	
		- Eliminate factors of 2 or 3 in denominator.	

10 Power Supply Recommendations

For best electrical performance of the LMK61E2 device, it is preferred to use a combination of 10 µF, 1 µF, and 0.1 µF on its power supply bypass network. ITI also recommends using component side mounting of the power supply bypass capacitors and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. Figure 34 shows the layout recommendation for power supply decoupling of LMK61E2.

11 Layout

11.1 Layout Guidelines

Ensured Thermal Reliability, *Best Practices for Signal Integrity* and *Recommended Solder Reflow Profile* provide recommendations for board layout, solder reflow profile and power supply bypassing when using LMK61E2 to ensure good thermal / electrical performance and overall signal integrity of entire system.

11.1.1 Ensured Thermal Reliability

The LMK61E2 is a high performance device. Therefore careful attention must be paid to device configuration and printed circuit board (PCB) layout with respect to power consumption. The ground pin needs to be connected to the ground plane of the PCB through three vias or more, as shown in Figure 34, to maximize thermal dissipation out of the package.

Equation 3 describes the relationship between the PCB temperature around the LMK61E2 and its junction temperature.

$$T_B = T_J – \Psi_{JB} * P \quad (3)$$

where

- T_B: PCB temperature around the LMK61E2
- T_J: Junction temperature of LMK61E2
- Ψ_{JB}: Junction-to-board thermal resistance parameter of LMK61E2 (36.7°C/W without airflow)
- P: On-chip power dissipation of LMK61E2

In order to ensure that the maximum junction temperature of LMK61E2 is below 125°C, it can be calculated that the maximum PCB temperature without airflow should be at 100°C or below when the device is optimized for best performance resulting in maximum on-chip power dissipation of 0.68 W.

11.1.2 Best Practices for Signal Integrity

For best electrical performance and signal integrity of entire system with LMK61E2, it is recommended to route vias into decoupling capacitors and then into the LMK61E2. It is also recommended to increase the via count and width of the traces wherever possible. These steps ensure lowest impedance and shortest path for high frequency current flow. Figure 34 shows the layout recommendation for LMK61E2.

11.1.3 Recommended Solder Reflow Profile

It is recommended to follow the solder paste supplier's recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. It is preferable for the LMK61E2 to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well solder manufactures recommended profile, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

11.2 Layout Example

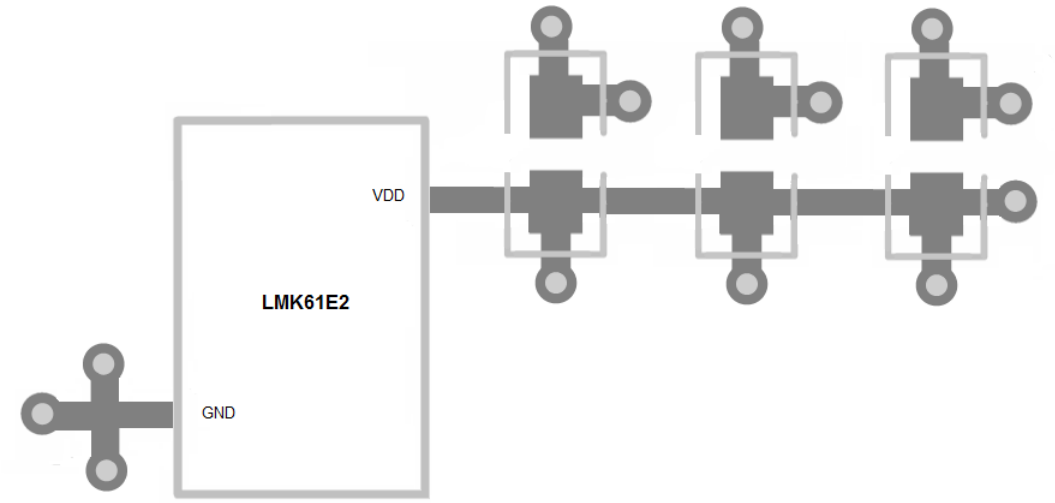


Figure 34. LMK61E2 Layout Recommendation for Power Supply and Ground

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

相关开发支持，请参见以下文档：

- WEBENCH 时钟架构工具
- CodeLoader

12.1.1.1 使用 WEBENCH® 工具定制设计方案

请单击此处，使用 LMK61E2 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 在开始阶段键入输出电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

12.2 文档支持

12.2.1 相关文档

相关文档如下：

- *《时钟设计工具》*(SNAU082)
- *《PLL 性能、仿真和设计》*(SNAA106)
- *《半导体和 IC 封装热指标》*(SPRA953)

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

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WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK61E2-SIAR	ACTIVE	QFM	SIA	8	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2	Samples
LMK61E2-SIAT	ACTIVE	QFM	SIA	8	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2	Samples
LMK61E2BAA-SIAR	ACTIVE	QFM	SIA	8	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 BAA	Samples
LMK61E2BAA-SIAT	ACTIVE	QFM	SIA	8	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 BAA	Samples
LMK61E2BBA-SIAR	ACTIVE	QFM	SIA	8	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E2 BBA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

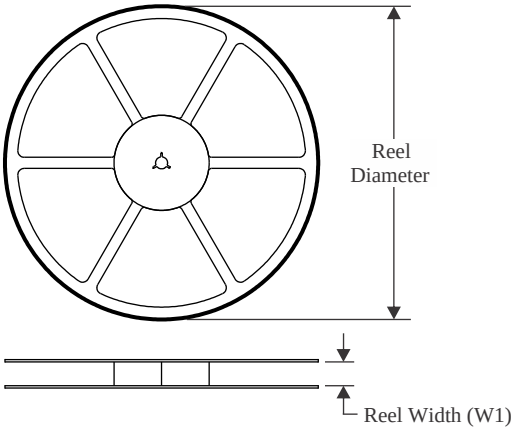
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

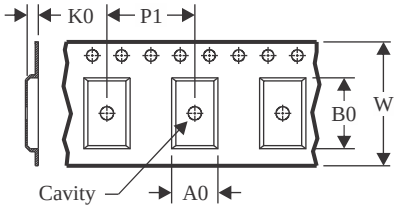
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

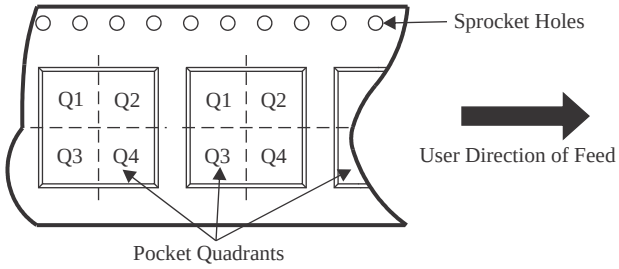


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

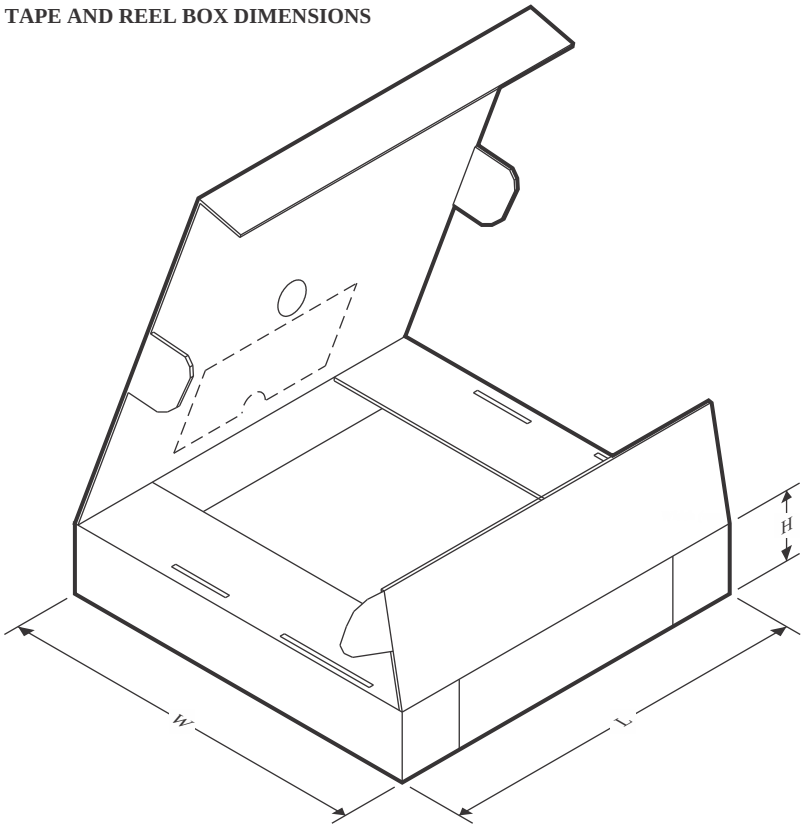
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK61E2-SIAR	QFM	SIA	8	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2-SIAT	QFM	SIA	8	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2BAA-SIAR	QFM	SIA	8	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2BAA-SIAT	QFM	SIA	8	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK61E2BBA-SIAR	QFM	SIA	8	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

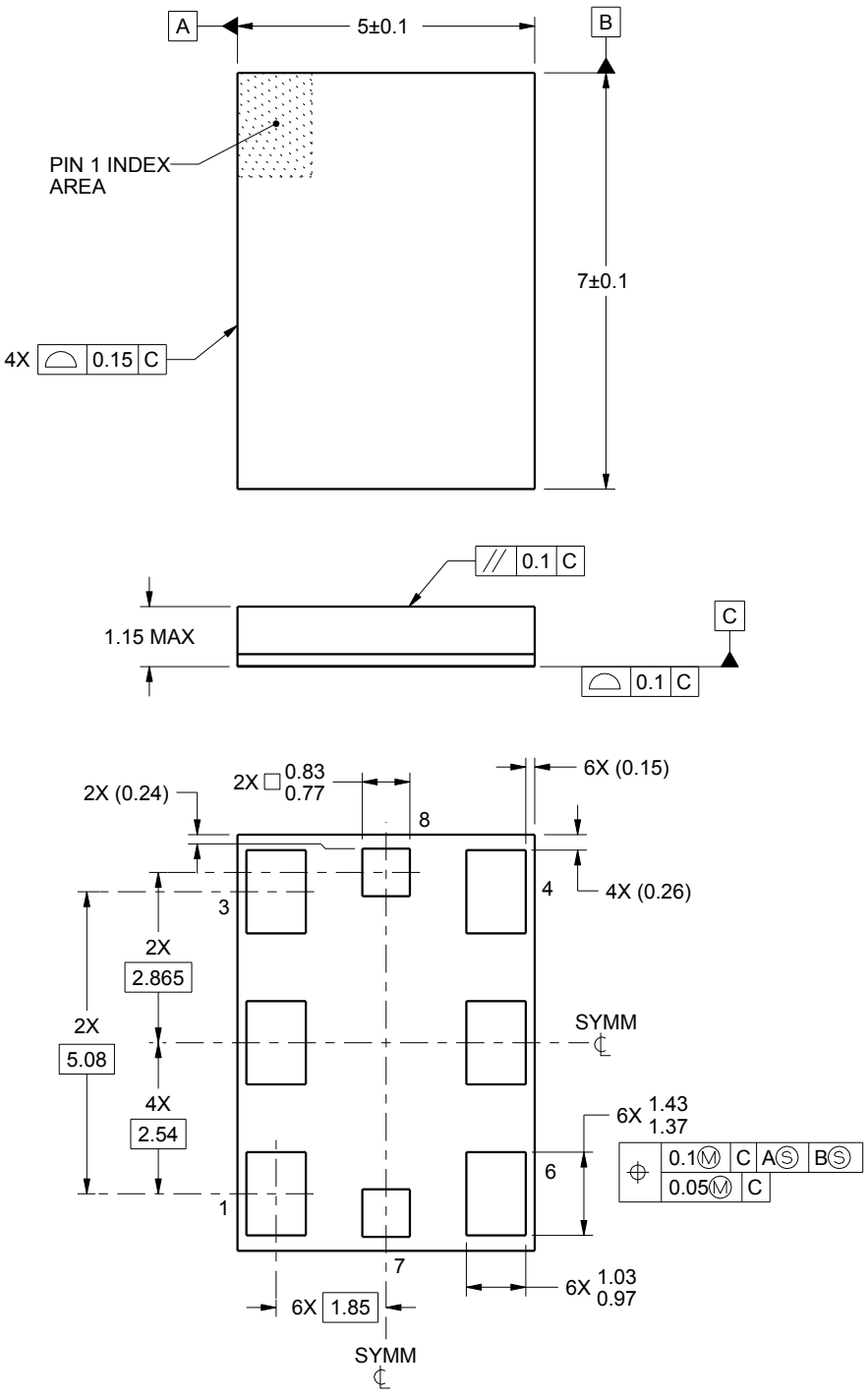
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK61E2-SIAR	QFM	SIA	8	2500	356.0	356.0	35.0
LMK61E2-SIAT	QFM	SIA	8	250	208.0	191.0	35.0
LMK61E2BAA-SIAR	QFM	SIA	8	2500	356.0	356.0	35.0
LMK61E2BAA-SIAT	QFM	SIA	8	250	213.0	191.0	55.0
LMK61E2BBA-SIAR	QFM	SIA	8	2500	356.0	356.0	35.0

PACKAGE OUTLINE

SIA0008B

QFM - 1.15 mm max height

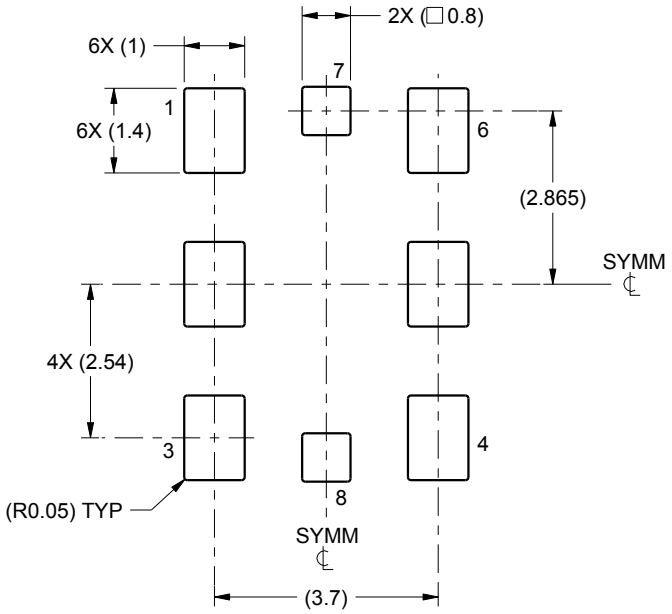
QUAD FLAT MODULE



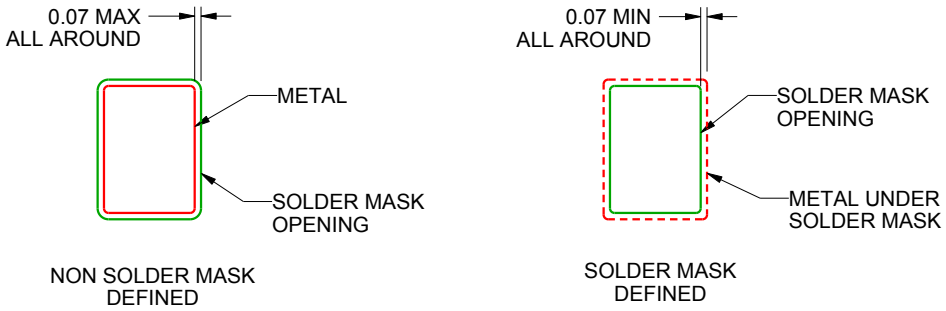
4221443/B 09/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PACKAGE SOLDER PADS
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

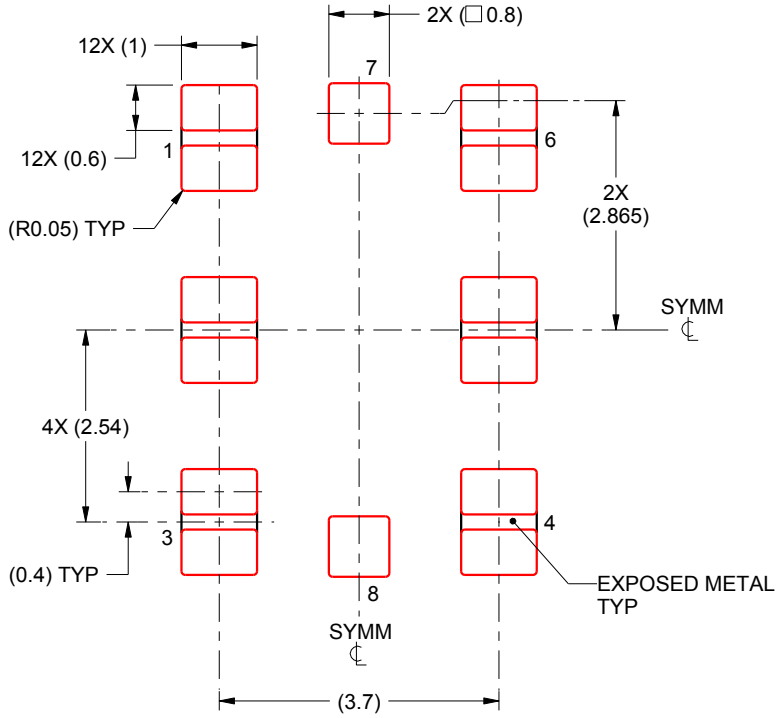
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIA0008B

QFM - 1.15 mm max height

QUAD FLAT MODULE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
PADS 1-3 & 4-6: 86%
SCALE:10X

4221443/B 09/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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