LMX2492/LMX2492-Q1 14GHz 低噪声分数 N 分频锁相环 (PLL)，具有斜坡/超宽带信号源发生功能

1 特性

- -227dBc/Hz 标称 PLL 噪声
- 500MHz - 14GHz 宽频带 PLL
- 3.15 -5.25V 电荷泵 PLL 电源
- 多用途斜坡/超宽带信号源发生
- 最大相位检测器频率 200MHz
- 频移键控/相移键控 (FSK/PSK) 调制引脚
- 数字锁检测
- 单个 3.3V 电源
- 汽车用 125°C Q100 1 级认证
- 非汽车用 (LMX2492) 选项

2 应用范围

- 汽车用调频连续波 (FMCW) 雷达
- 军用雷达
- 微波回程
- 测试和测量
- 卫星通信
- 无线基础设施
- 针对高速模数转换器 (ADC) / 数模转换器 (DAC) 的采样时钟

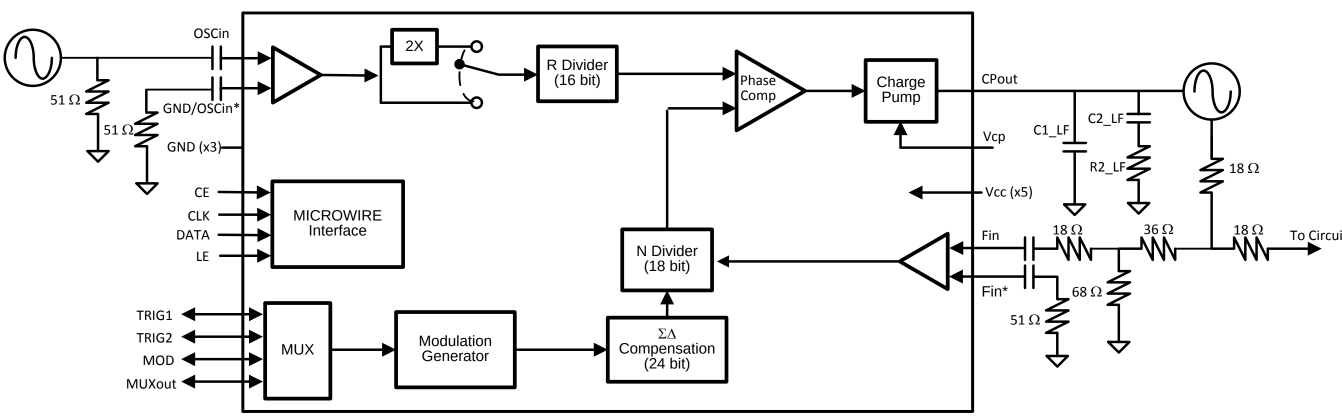
3 说明

LMX2492/92-Q1 是一款具有斜坡和超宽带信号源发生功能的 14GHz 宽频带三角积分分数 N 分频 PLL。 它由一个相位频率检测器、可编程电荷泵以及用于外部 VCO 的高频输入组成。 LMX2492/92-Q1 支持宽范围且灵活的斜升功能类 (class of ramping capabilities)，其中包括 FSK，PSK 和高达 8 个段的可配置分段线性 FM 调制系统配置。 它还支持精细的 PLL 分辨率以及相位检测器速率高达 200MHz 的快速斜坡。 LMX2492/92-Q1 的任何一个寄存器均可被回读。 LMX2492/92-Q1 可由单个 3.3V 电源供电运行。 而且，对于电压高达 5.25V 的电荷泵的支持能够免除对于外部放大器的需要，从而获得一个具有更佳相位噪声性能的更简单解决方案。

器件信息

订货编号	封装	封装尺寸
LMX2492-Q1RTW	超薄四方扁平无引线 (WQFN) (24)	4mm x 4mm
LMX2492RTW		

4 简化电路原理图



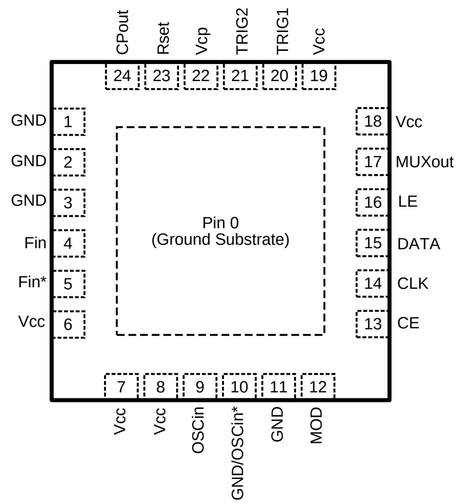
目录

5 修订历史记录

日期	修订版本	注释
2014 年 3 月	*	最初发布版本。

6 Terminal Configuration and Functions

WQFN (RTW)
24 Terminal
(Top View)



Terminal Functions

TERMINAL		TYPE	DESCRIPTION
NUMBER	NAME		
0	DAP	GND	Die Attach Pad. Connect to PCB ground plane.
1	GND	GND	Ground for charge pump.
2,3	GND	GND	Ground for Fin Buffer
4,5	Fin Fin*	Input	Complimentary high frequency input pins. Should be AC coupled. If driving single-ended, impedance as seen from Fin and Fin* pins looking outwards from the part should be roughly the same.
6	Vcc	Supply	Power Supply for Fin Buffer
7	Vcc	Supply	Supply for On-chip LDOs
8	Vcc	Supply	Supply for OSCin Buffer
9	OSCin	Input	Reference Frequency Input
10	GND/ OSCin*	GND/Input	Complimentary input for OSCin. If not used, it is recommended to match the termination as seen from the OSCin terminal looking outwards. However, this may also be grounded as well.
11	GND	GND	Ground for OSCin Buffer
12	MOD	Input/Output	Multiplexed Input/Output Pins for Ramp Triggers, FSK/PSK Modulation, FastLock, and Diagnostics
13	CE	Input	Chip Enable
14	CLK	GND	Serial Programming Clock.
15	DATA	GND	Serial Programming Data
16	LE	Input	Serial Programming Latch Enable
17	MUXout	Input/Output	Multiplexed Input/Output Pins for Ramp Triggers, FSK/PSK Modulation, FastLock, and Diagnostics
18	Vcc	Supply	Supply for delta sigma engine.
19	Vcc	Supply	Supply for general circuitry.
20	TRIG1	Input/Output	Multiplexed Input/Output Pins for Ramp Triggers, FSK/PSK Modulation, FastLock, and Diagnostics
21	TRIG2	Input/Output	Multiplexed Input/Output Pins for Ramp Triggers, FSK/PSK Modulation, FastLock, and Diagnostics
22	Vcp	Supply	Power Supply for the charge pump.
23	Rset	NC	No connect.
24	CPout	Output	Charge Pump Output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Vcp	Supply Voltage for Charge Pump	Vcc	5.5	V
CPout	Charge Pump Output Pin	-0.3	Vcp	V
Vcc	All Vcc Pins	-0.3	3.6	V
Others	All Other I/O Pins	-0.3	Vcc + 0.3	V
T_{Solder}	Lead Temperature (solder 4 seconds)		260	°C
$T_{Junction}$	Junction Temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{STG}	Storage Temperature Range	-65	150	°C
MSL	Moisture Sensitivity Level		3	n/a
V_{ESD} (1)	Human body model (HBM) ESD stress voltage (2)		2500	V
	Charged device model (CDM) ESD stress voltage (3)		1500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	DEVICE	MIN	TYP	MAX	UNIT
Vcc	PLL Supply Voltage		3.15	3.3	3.45	V
Vcp	Charge Pump Supply Voltage		Vcc		5.25	V
T_A	Ambient Temperature	LMX2492	-40		85	°C
		LMX2492-Q1	-40		125	
T_J	Junction Temperature	LMX2492	-40		125	°C
		LMX2492-Q1	-40		135	

7.4 Thermal Information

	THERMAL METRIC (1)	Temperature	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.4	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	7.1	
ψ_{JB}	Junction-to-board characterization parameter	20	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

(3.15 V ≤ Vcc ≤ 3.45 V. Vcc ≤Vcp ≤5.25 V. Typical values are at Vcc = Vcp = 3.3 V, 25 °C. -40°C ≤ T_A ≤ 85 °C for the LMX2492 and -40°C ≤ T_A ≤ 125 °C for the LMX2492-Q1 ; except as specified.)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Icc	Current Consumption	All Vcc Pins	Fpd = 10 MHz		45		mA
			Fpd = 100 MHz		50		
			Fpd = 200 MHz		55		
		Vcp Pin	Kpd = 0.1 mA		2		
			Kpd = 1.6 mA		10		
			Kpd = 3.1 mA		19		
IccPD	Current	POWERDOWN			3		
f_{OSCin}	Frequency for OSCin terminal	OSC_DIFFR=0, Doubler Disabled		10		600	MHz
		OSC_DIFFR=0, Doubler Enabled		10		300	
		OSC_DIFFR=1, Doubler Disabled		10		1200	
		OSC_DIFFR=1, Doubler Enabled		10		600	
v_{OSCin}	Voltage for OSCin Pin(1)			0.5		Vcc-0.5	Vpp
f_{Fin}	Frequency for FinPin(2)			500		14000	MHz
p_{Fin}	Power for Fin Pin	Single-Ended Operation		-5		5	dBm
f_{PD}	Phase Detector Frequency					200	MHz
PN1Hz	PLL Figure of Merit(3)				-227		dBc/Hz
PN10kHz	Normalized PLL 1/f Noise(3)	Normalized to 10 kHz offset for a 1 GHz carrier.			-120		dBc/Hz
I_{CPout}TRI	Charge Pump Leakage Tri-state Leakage					10	nA
I_{CPout}MM	Charge Pump Mismatch(4)	V_{CPout} = Vcp / 2			5 %		
I_{CPout}	Charge Pump Current	V_{CPout} = Vcp / 2	CPG=1X		0.1		mA
			…				
			CPG=31X		3.1		

(1) For optimal phase noise performance, higher input voltage and a slew rate of at least 3 V/ns is recommended
(2) Tested to 13.5 GHz, Guaranteed to 14 GHz by characterization
(3) PLL Noise Metrics are measured with a clean OSCin signal with a high slew rate using a wide loop bandwidth. The noise metrics model the PLL noise for an infinite loop bandwidth as:
$PLL\_Total = 10\times\log(10^{PLL\_Flat/10} + 10^{PLL\_Flicker(Offset)/10})$
$PLL\_Flat = PN1Hz + 20\times\log(N) + 10\times\log(Fpd/1Hz)$
$PLL\_Flicker = PN10kHz - 10\times\log(Offset/10kHz) + 20\times\log(Fvco/1GHz)$
(4) Charge pump mismatch varies as a function of charge pump voltage. Consult typical performance characteristics to see this variation.

Electrical Characteristics (continued)

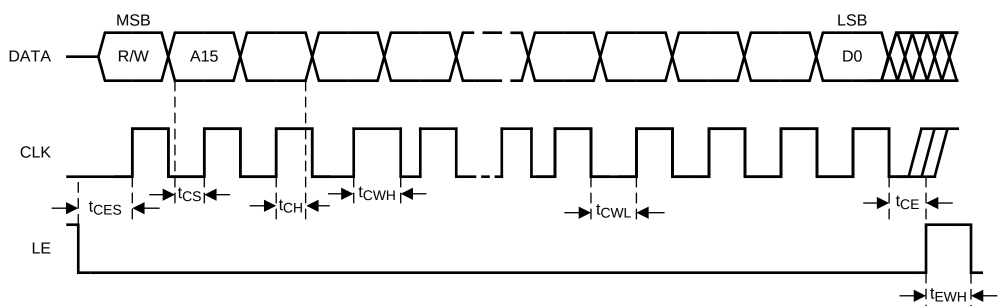
(3.15 V ≤ Vcc ≤ 3.45 V. Vcc ≤Vcp ≤5.25 V. Typical values are at Vcc = Vcp = 3.3 V, 25 °C.
-40°C ≤ T_A ≤ 85 °C for the LMX2492 and -40°C ≤ T_A ≤ 125 °C for the LMX2492-Q1 ; except as specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC OUTPUT TERMINALS (MUXout,TRIG1,TRIG2,MOD)						
V_{OH}	Output High Voltage		0.8 x Vcc	Vcc		V
V_{OL}	Output Low Voltage			0	0.2 x Vcc	V
LOGIC INPUT TERMINALS (CE,CLK,DATA,LE,MUXout,TRIG1,TRIG2,MOD)						
V_{IH}	Input High Voltage		1.4		Vcc	V
V_{IL}	Input Low Voltage		0		0.6	V
I_{IH}	Input Leakage		-5	1	5	uA
T_{CE}LOW	Chip enable Low Time		5			us
T_{CE}HIGH	Chip enable High Time		5			us

7.6 Timing Requirements, Programming Interface (CLK, DATA, LE)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_{CE}	Clock To LE Low Time	35			ns
T_{CS}	Data to Clock Setup Time	10			ns
T_{CH}	Data to Clock Hold Time	10			ns
T_{CWH}	Clock Pulse Width High	25			ns
T_{CWL}	Clock Pulse Width Low	25			ns
T_{CES}	Enable to Clock Setup Time	10			ns
T_{EWH}	Enable Pulse Width High	10			ns

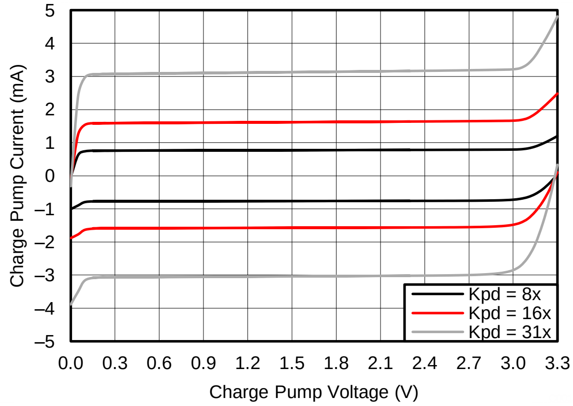
7.7 Serial Data Input Timing



There are several other considerations for programming:

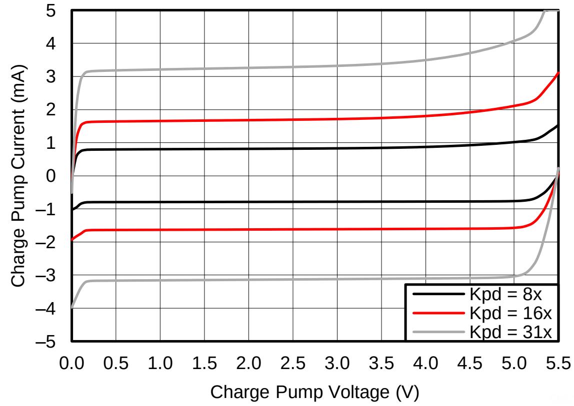
- The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the LE signal, the data is sent from the shift register to an actual counter.
- If no LE signal is given after the last data bit and the clock is kept toggling, then these bits will be read into the next lower register. This eliminates the need to send the address each time.
- A slew rate of at least 30 V/us is recommended for the CLK, DATA, and LE signals
- Timing specs also apply to readback. Readback can be done through the MUXout, TRIG1, TRIG2, or MOD terminals.

7.8 Typical Characteristics



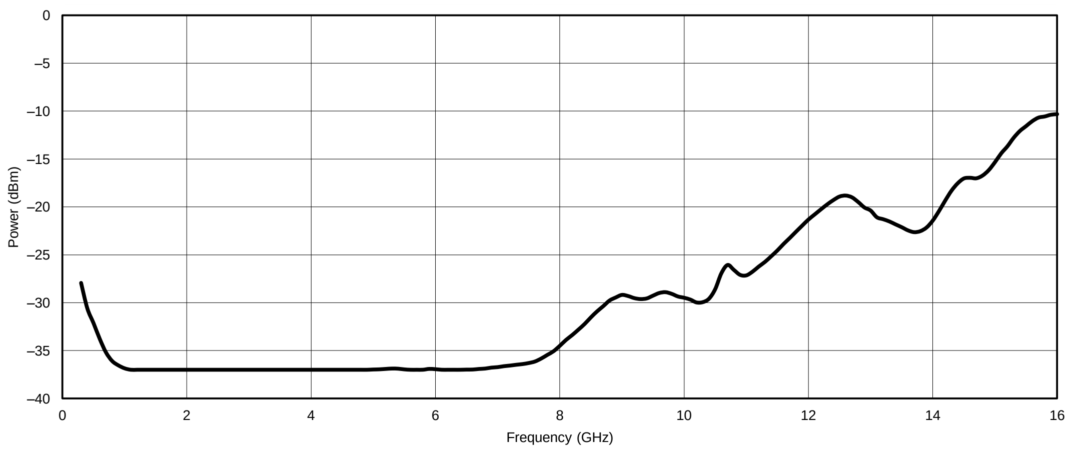
For a charge pump supply of 3.3 V, optimal performance is for a typical charge pump output voltage between 0.5 and 2.8 volts.

Figure 1. Charge Pump Current for Vcp = 3.3 V



For a charge pump supply voltage of 5 volts or higher, optimal performance is typically for a charge pump output voltage between 0.5 and 4.5 volts.

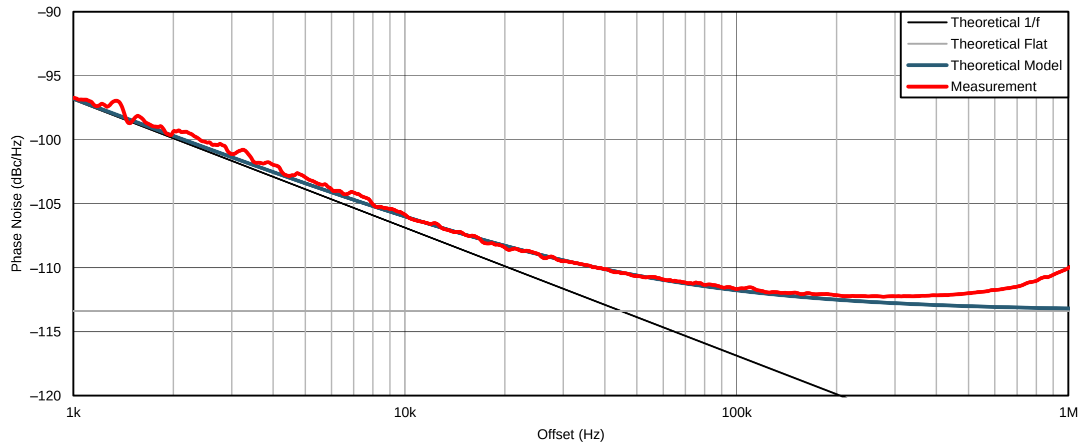
Figure 2. Charge Pump Current for Vcp = 5.5 V



Typical value of lowest power level as a function of frequency. Design to electrical specifications for input sensitivity, not typical performance graphs.

Figure 3. Fin Input Sensitivity

Typical Characteristics (continued)



This plot is for a phase detector of 100 MHz, 2 MHz loop bandwidth, and VCO at 9600 MHz. However, the plot shown is the divide by 2 port at 4800 MHz. The input was a 100 MHz Wenzel Oscillator. The model shows this phase noise has a figure of merit of -227 dBc/Hz and a normalized 1/f noise of -120.5 dBc/Hz. The charge pump supply was 5 V and the charge pump output voltage was 1.34 V.

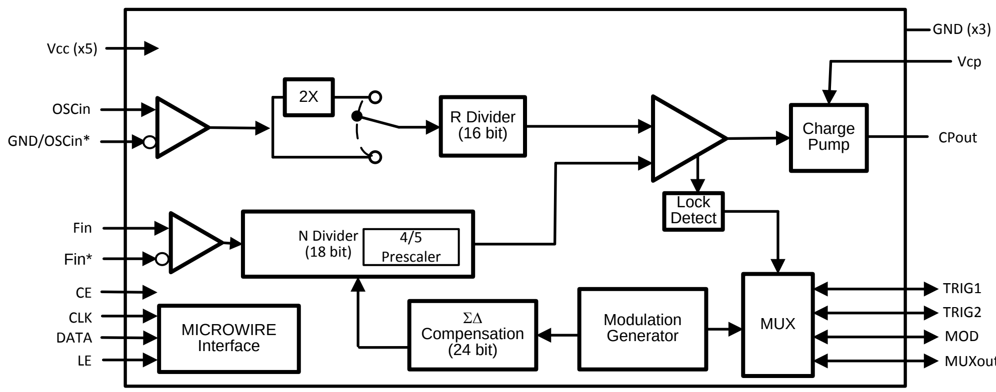
Figure 4. LMX2492/92-Q1 Phase Noise for Fpd =100 MHz, Fvco = 9600 MHz/2

8 Detailed Description

8.1 Overview

The LMX2492/92-Q1 is a microwave PLL, consisting of a reference input and divider, high frequency input and divider, charge pump, ramp generator, and other digital logic. The Vcc power supply pins run at a nominal 3.3 volts, while the charge pump supply pin, Vcp, operates anywhere from Vcc to 5 volts. The device is designed to operate with an external loop filter and VCO. Modulation is achieved by manipulating the MASH engine.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 OSCin Input

The reference can be applied in several ways. If using a differential input, this should be terminated differentially with a 100 ohm resistance and AC coupled to the OSCin and GND/OSCin* terminals. If driving this single-ended, then the GND/OSCin* terminal may be grounded, although better performance is attained by connecting the GND/OSCin* terminal through a series resistance and capacitance to ground to match the OSCin terminal impedance.

8.3.2 OSCin Doubler

The OSCin doubler allows the input signal to the OSCin to be doubled in order to have higher phase detector frequencies. This works by clocking on both the rising and falling edges of the input signal, so it therefore requires a 50% input duty cycle.

8.3.3 R Divider

The R counter is 16 bits divides the OSCin signal from 1 to 65535. If DIFF_R = 0, then any value can be chosen in this range. If DIFF_R=1, then the divide is restricted to 2,4,8, and 16, but allows for higher OSCin frequencies.

8.3.4 PLL N Divider

The 16 bit N divider divides the signal at the Fin terminal down to the phase detector frequency. It contains a 4/5 prescaler that creates minimum divide restrictions, but allows the N value to increment in values of one.

Modulator Order	Minimum N Divide
Integer Mode, 1st Order Modulator	16
2nd Order Modulator	17
3rd Order Modulator	19
4th Order Modulator	25

8.3.5 Fractional Circuitry

The fractional circuitry controls the N divider with delta sigma modulation that supports a programmable first, second, third, and fourth order modulator. The fractional denominator is a fully programmable 24-bit denominator that can support any value from 1,2,..., 2^{24}, with the exception when the device is running one of the ramps, and in this case it is a fixed size of 2^{24}.

8.3.6 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the R and N dividers and generates a correction voltage corresponding to the phase error. This voltage is converted to a correction current by the charge pump. The phase detector frequency, f_{PD}, can be calculated as follows: $f_{PD} = f_{OSCin} \times OSC\_2X / R$.

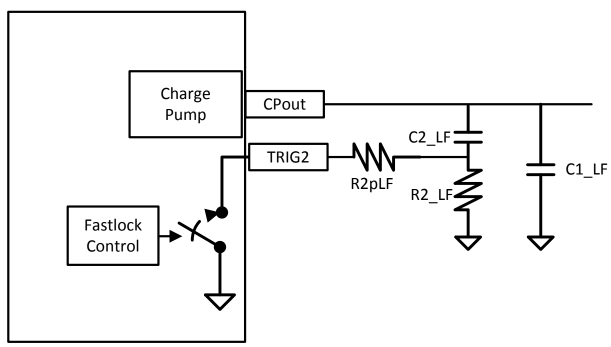
The charge pump supply voltage on this device, Vcp, can be either run at the Vcc voltage, or up to 5.25 volts in order to get higher tuning voltages to present to the VCO.

8.3.7 External Loop Filter

The loop filter is external to the device and is application specific. Texas Instruments website has details on this at www.ti.com.

8.3.8 Fastlock and Cycle Slip Reduction

The Fastlock™ and Cycle Slip Reduction features can be used to improved lock time. When the frequency is changed, a timeout counter can be used to engage these features for a prescribed number of phase detector cycles. During this time that the timeout counter is counting down, the device can be used to pull a terminal from high impedance to ground switch in an extra resistor (R2pLF), change the charge pump current (FL_CPG), or change the phase detector frequency. TRIG2 is recommended for switching the resistor with a setting of TRIG2_MUX = Fastlock (2) and TRIG2_PIN = Inverted/Open Drain (5).



Parameter	Normal Operation	Fastlock Operation
Charge Pump Gain	CPG	FL_CPG
Device Pin (TRIG1, TRIG2, MOD, or MUXout)	High Impedance	Grounded

The resistor and the charge pump current are changed simultaneously so that the phase margin remains the same while the loop bandwidth is by a factor of K as shown in the following table:

Parameter	Symbol	Calculation
Charge Pump Gain in Fastlock	FL_CPG	Typically use the highest value.
Loop Bandwidth Multiplier	K	K=sqrt(FL_CPG/CPG)
External Resistor	R2pLF	R2 / (K-1)

Cycle slip reduction is another method that can also be used to speed up lock time by reducing cycle slipping. Cycle slipping typically occurs when the phase detector frequency exceeds about 100x the loop bandwidth of the PLL. Cycle slip reduction works in a different way than fastlock. To use this, the phase detector frequency is decreased while the charge pump current is simultaneously increased by the same factor. Although the loop bandwidth is unchanged, the ratio of the phase detector frequency to the loop bandwidth is, and this is helpful for cases when the phase detector frequency is high. Because cycle slip reduction changes the phase detector rate, it also impacts other things that are based on the phase detector rate, such as the fastlock timeout-counter and ramping controls.

8.3.9 Lock Detect and Charge Pump Voltage Monitor

The LMX2492/92-Q1 offers two methods to determine if the PLL is in lock, charge pump voltage monitoring and digital lock detect. These features can be used individually or in conjunction to give a reliable indication of when the PLL is in lock. The output of this detection can be routed to the TRIG1, TRIG2, MOD, or MUXout terminals.

8.3.9.1 Charge Pump Voltage Monitor

The charge pump voltage monitor allows the user to set low (CMP_THR_LOW) and high (CMP_THR_HIGH) thresholds for a comparator that monitors the charge pump output voltage.

Vcp	Threshold	Suggested Level
3.3 V	CPM_THR_LOW = (Vthresh + 0.08) / 0.085	6 for 0.5V limit
	CPM_THR_HIGH = (Vthresh - 0.96) / 0.044	42 for 2.8V limit
5.0 V	CPM_THR_LOW = (Vthresh + 0.056) / 0.137	4 for 0.5V limit
	CPM_THR_HIGH = (Vthresh -1.23) / 0.071	46 for 4.5V limit

8.3.9.2 Digital Lock Detect

Digital lock detect works by comparing the phase error as presented to the phase detector. If the phase error plus the delay as specified by the PFD_DLY bit is outside the tolerance as specified by DLD_TOL, then this comparison would be considered to be an error, otherwise passing. The DLD_ERR_CNT specifies how may errors are necessary to cause the circuit to consider the PLL to be unlocked. The DLD_PASS_CNT specifies how many passing comparisons are necessary to cause the PLL to be considered to be locked and also resets the count for the errors. The DLD_TOL value should be set to no more than half of a phase detector period plus the PFD_DLY value. The DLD_ERR_CNT and DLD_PASS_CNT values can be decreased to make the circuit more sensitive. If the circuit is too sensitive, then chattering can occur and the DLD_ERR_CNT, DLD_PASS_CNT, or DLD_TOL values should be increased.

Note that if the OSCin signal goes away and there is no noise or self-oscillation at the OSCin pin, then it is possible for the digital lock detect to indicate a locked state when the PLL really is not in lock. If this is a concern, then digital lock detect can be combined with charge pump voltage monitor to detect this situation..

8.3.10 FSK/PSK Modulation

Two level FSK or PSK modulation can be created whenever a trigger event, as defined by the FSK_TRIG field is detected. This trigger can be defined as a transition on a terminal (TRIG1, TRIG2, MOD, or MUXout) or done purely in software. The RAMP_PM_EN bit defines the modulation to be either FSK or PSK and the FSK_DEV register determines the amount of the deviation. Remember that the FSK_DEV[32:0] field is programmed as the 2's complement of the actual desired FSK_DEV value. This modulation can be added to the modulation created from the ramping functions as well.

RAMP_PM_EN	Modulation Type	Deviation
0	2 Level FSK	Fpd × FSK_DEV / 2^{24}
1	2 Level PSK	360° × FSK_DEV / 2^{24}

8.3.11 Ramping Functions

The LMX2492/92-Q1 supports a broad and flexible class of FMCW modulation formed by up to 8 linear ramps. When the ramping function is running, the denominator is fixed to a forced value of 2^{24} = 16777216. The waveform always starts at RAMP0 when the LSB of the PLL_N (R16) is written to. After it is set up, it will start at the initial frequency and have piecewise linear frequency modulation that deviates from this initial frequency as specified by the modulation. Each of the eight ramps can be individually programmed. Various settings are as follows

Ramp Characteristic	Programming Field Name	Description
Ramp Length	RAMPx_LEN RAMPx_DLY	The user programs the length of the ramp in phase detector cycles. If RAMPx_DLY=1, then each count of RAMPx_LEN is actually two phase detector cycles.
Ramp Slope	RAMPx_LEN RAMPx_DLY RAMPx_INC	The user does not directly program slope of the line, but rather this is done by defining how long the ramp is and how much the fractional numerator is increased per phase detector cycle. The value for RAMPx_INC is calculated by taking the total expected increase in the frequency, expressed in terms of how much the fractional numerator increases, and dividing it by RAMPx_LEN. The value programmed into RAMPx_INC is actually the two's complement of the desired mathematical value.
Trigger for Next Ramp	RAMPx_NEXT_TRIG	The event that triggers the next ramp can be defined to be the ramp finishing or can wait for a trigger as defined by TRIG A, TRIG B, or TRIG C.
Next Ramp	RAMPx_NEXT	This sets the ramp that follows. Waveforms are constructed by defining a chain ramp segments. To make the waveform repeat, make RAMPx_NEXT point to the first ramp in the pattern.
Ramp Fastlock	RAMPx_FL	This allows the ramp to use a different charge pump current or use Fastlock
Ramp Flags	RAMPx_FLAG	This allows the ramp to set a flag that can be routed to external terminals to trigger other devices.

8.3.11.1 Ramp Count

If it is desired that the ramping waveform keep repeating, then all that is needed is to make the RAMPx_NEXT of the final ramp equal to the first ramp. This will run until the RAMP_EN bit is set to zero. If this is not desired, then one can use the RAMP_COUNT to specify how may times the specified pattern is to repeat.

8.3.11.2 Ramp Comparators and Ramp Limits

The ramp comparators and ramp limits use programable thresholds to allow the device to detect whenever the modulated waveform frequency crosses a limit as set by the user. The difference between these is that comparators set a flag to alert the user while a ramp limits prevent the frequency from going beyond the prescribed threshold. In either case, these thresholds are expressed by programming the Extended_Fractional_Numerator.

$$\text{Extended\_Fractional\_Numerator} = \text{Fractional\_Numerator} + (N-N^*) \times 2^{24}$$

In the above, N is the PLL feedback value without ramping and N* is the instantaneous value during ramping. The actual value programmed is the 2's complement of Extended_Fractional_Numerator.

Type	Programming Bit	Threshold
Ramp Limits	RAMP_LIMIT_LOW	Lower Limit
	RAMP_LIMIT_HIGH	Upper Limit
Ramp Comparators	RAMP_CMP0 RAMP_CMP1	For the ramp comparators, if the ramp is increasing and exceeds the value as specified by RAMP_CMPx, then the flag will go high, otherwise it is low. If the ramp is decreasing and goes below the value as specified by RAMP_CMPx, then the flag will go high, otherwise it will be low.

8.3.12 Power on Reset (POR)

The power on reset circuitry sets all the registers to a default state when the device is powered up. This same reset can be done by programming SWRST=1. In the programming section, the power on reset state is given for all the programmable fields.

8.4 Device Functional Modes

The two primary ways to use the LMX2492/92-Q1 are to run it to generate a set of frequencies

8.4.1 Continuous Frequency Generator

In this mode, the LMX2492/92-Q1 generates a single frequency that only changes when the N divider is programmed to a new value. In this mode, the RAMP_EN bit is set to 0 and the ramping controls are not used. The fractional denominator can be programmed to any value from 1 to 16777216. In this kind of application, the PLL is tuned to different channels, but at each channel, the goal is to generate a stable fixed frequency.

8.4.1.1 Integer Mode Operation

In integer mode operation, the VCO frequency needs to be an integer multiple of the phase detector frequency. This can be the case when the output frequency or frequencies are nicely related to the input frequency. As a rule of thumb, if this an be done with a phase detector of as high as the lesser of 10 MHz or the OSCin frequency, then this makes sense. To operate the device in integer mode, disable the fractional circuitry by programming the fractional order (FRAC_ORDER) , dithering (FRAC_DITH), and numerator (FRAC_NUM) to zero.

8.4.1.2 Fractional Mode Operation

In fractional mode, the output frequency does not need to be an integer multiple of the phase detector frequency. This makes sense when the channel spacing is more narrow or the input and output frequencies are not nicely related. There are several programmable controls for this such as the modulator order, fractional dithering, fractional numerator, and fractional denominator. There are many trade-offs with choosing these, but here are some guidelines

Parameter	Field Name	How to Choose
Fractional Numerator and Denominator	FRAC_NUM FRAC_DEN	The first step is to find the fractional denominator. To do this, find the frequency that divides the phase detector frequency by the channel spacing. For instance, if the output ranges from 5000 to 5050 in 5 MHz steps and the phase detector is 100 MHz, then the fractional denominator is 100 MHz/5 = 20. So for a an output of 5015 MHz, the N divider would be 50 + 3/20. In this case, the fractional numerator is 3 and the fractional denominator is 20. Sometimes when dithering is used, it makes sense to express this as a larger equivalent fraction. Note that if ramping is active, the fractional denominator is forced to 2^{24}.
Fractional Order	FRAC_ORDER	There are many trade-offs, but in general try either the 2nd or 3rd order modulator as starting points. The 3rd order modulator may give lower main spurs, but may generate others. Also if dithering is involved, it can generate phase noise.
Dithering	FRAC_DITH	Dithering can reduce some fractional spurs, but add noise. Consult application note AN-1879 for more details on this.

8.4.2 Modulated Waveform Generator

In this mode, the device can generate a broad class of frequency sweeping waveforms. The user can specify up to 8 linear segments in order to generate these waveforms. When the ramping function is running, the denominator is fixed to a forced value of 2^{24} = 16777216

In addition to the ramping functions, there is also the capability to use a terminal to add phase or frequency modulation that can be done by itself or added on top of the waveforms created by the ramp generation functions.

8.5 Programming

8.5.1 Loading Registers

The device is programmed using several 24 bit registers. The first 16 bits of the register are the address, followed by the next 8 bits of data. The user has the option to pull the LE terminal high after this data, or keep sending data and it will apply this data to the next lower register. So instead of sending three registers of 24 bits each, one could send a single 40 bit register with the 16 bits of address and 24 bits of data. For that matter, the entire device could be programmed as a single register if desired.

8.6 Register Map

Registers are programmed in REVERSE order from highest to lowest. Registers NOT shown in this table or marked as reserved can be written as all 0's unless otherwise stated. The POR value is the power on reset value that is assigned when the device is powered up or the SWRST bit is asserted.

Table 1. Register Map

Register		D7	D6	D5	D4	D3	D2	D1	D0	POR
0	0	0	0	0	1	1	0	0	0	0x18
1	0x1	Reserved								0x00
2	0x2	0	0	0	0	0	SWRST	POWERDOWN[1:0]		0x00
3-15	0x3 - 0xF	Reserved								-
16	0x10	PLL_N[7:0]								0x64
17	0x11	PLL_N[15:8]								0x00
18	0x12	0	FRAC_ORDER[2:0]			FRAC_DITHER[1:0]		PLL_N[17:16]		0x00
19	0x13	FRAC_NUM[7:0]								0x00
20	0x14	FRAC_NUM[15:8]								0x00
21	0x15	FRAC_NUM[23:16]								0x00
22	0x16	FRAC_DEN[7:0]								0x00
23	0x17	FRAC_DEN[15:8]								0x00
24	0x18	FRAC_DEN[23:16]								0x00
25	0x19	PLL_R[7:0]								0x04
26	0x1A	PLL_R[15:8]								0x00
27	0x1B	0	FL_CSR[1:0]		PFD_DLY[1:0]		PLL_R_ DIFF	0	OSC_2X	0x08
28	0x1C	0	0	CPPOL	CPG[4:0]					0x00
29	0x1D	FL_TOC[10:8]			FL_CPG[4:0]					0x00
30	0x1E	0	CPM_ FLAGL	CPM_THR_LOW[5:0]						0x0a
31	0x1F	0	CPM_ FLAGH	CPM_THR_HIGH[5:0]						0x32
32	0x20	FL_TOC[7:0]								0x00
33	0x21	DLD_PASS_CNT[7:0]								0x0f
34	0x22	DLD_TOL[2:0]			DLD_ERR_CNTR[4:0]					0x00
35	0x23	MOD_ MUX[5]	1	MUXout _MUX[5]	TRIG2 _MUX[5]	TRIG1 _MUX[5]	0	0	1	0x41
36	0x24	TRIG1_MUX[4:0]					TRIG1_PIN[2:0]			0x08
37	0x25	TRIG2_MUX[4:0]					TRIG2_PIN[2:0]			0x10
38	0x26	MOD_MUX[4:0]					MOD_PIN[2:0]			0x18
39	0x27	MUXout_MUX[4:0]					MUXout_PIN[2:0]			0x38
40-57	0x28-0x39	Reserved								-

Register Map (continued)

Table 1. Register Map (continued)

Register		D7	D6	D5	D4	D3	D2	D1	D0	POR
58	0x3A	RAMP_TRIG_A[3:0]				0	RAMP_ PM_EN	RAMP_ CLK	RAMP_EN	0x00
59	0x3B	RAMP_TRIG_C[3:0]				RAMP_TRIG_B[3:0]				0x00
60	0x3C	RAMP_CMP0[7:0]								0x00
61	0x3D	RAMP_CMP0[15:8]								0x00
62	0x3E	RAMP_CMP0[23:16]								0x00
63	0x3F	RAMP_CMP0[31:24]								0x00
64	0x40	RAMP_CMP0_EN[7:0]								0x00
65	0x41	RAMP_CMP1[7:0]								0x00
66	0x42	RAMP_CMP1[15:8]								0x00
67	0x43	RAMP_CMP1[23:16]								0x00
68	0x44	RAMP_CMP1[31:24]								0x00
69	0x45	RAMP_CMP1_EN[7:0]								0x00
70	0x46	0	FSK_TRIG[1:0]		RAMP_ LIMH[32]	RAMP_ LIML[32]	FSK_ DEV[32]	RAMP_ CMP1[32]	RAMP_ CMP0[32]	0x08
71	0x47	FSK_DEV[7:0]								0x00
72	0x48	FSK_DEV[15:8]								0x00
73	0x49	FSK_DEV[23:16]								0x00
74	0x4A	FSK_DEV[31:24]								0x00
75	0x4B	RAMP_LIMIT_LOW[7:0]								0x00
76	0x4C	RAMP_LIMIT_LOW[15:8]								0x00
77	0x4D	RAMP_LIMIT_LOW[23:16]								0x00
78	0x4E	RAMP_LIMIT_LOW[31:24]								0x00
79	0x4F	RAMP_LIMIT_HIGH[7:0]								0xff
80	0x50	RAMP_LIMIT_HIGH[15:8]								0xff
81	0x51	RAMP_LIMIT_HIGH[23:16]								0xff
82	0x52	RAMP_LIMIT_HIGH[31:24]								0xff
83	0x53	RAMP_COUNT[7:0]								0x00
84	0x54	RAMP_TRIG_INC[1:0]		RAMP_ AUTO	RAMP_COUNT[12:8]					0x00
85	0x55	Reserved								0x00

Register Map (continued)

Table 1. Register Map (continued)

Register		D7	D6	D5	D4	D3	D2	D1	D0	POR
86	0x56	RAMP0_INC[7:0]								0x00
87	0x57	RAMP0_INC[15:8]								0x00
88	0x58	RAMP0_INC[23:16]								0x00
89	0x59	RAMP0_ DLY	RAMP0_ FL	RAMP0_INC[29:24]						0x00
90	0x5A	RAMP0_LEN[7:0]								0x00
91	0x5B	RAMP0_LEN[15:8]								0x00
92	0x5C	RAMP0_NEXT[2:0]			RAMP0_ NEXT_TRIG[1:0]		RAMP0_ RST	RAMP0_FLAG[1:0]		0x00
93	0x5D	RAMP1_INC[7:0]								0x00
94	0x5E	RAMP1_INC[15:8]								0x00
95	0x5F	RAMP1_INC[23:16]								0x00
96	0x60	RAMP1_ DLY	RAMP1_ FL	RAMP1_INC[29:24]						0x00
97	0x61	RAMP1_LEN[7:0]								0x00
98	0x62	RAMP1_LEN[15:8]								0x00
99	0x63	RAMP1_NEXT[2:0]			RAMP1_ NEXT_TRIG[1:0]		RAMP1_ RST	RAMP1_FLAG[1:0]		0x00
100	0x64	RAMP2_INC[7:0]								0x00
101	0x65	RAMP2_INC[15:8]								0x00
102	0x66	RAMP2_INC[23:16]								0x00
103	0x67	RAMP2 DLY	RAMP2_ FL	RAMP2_INC[29:24]						0x00
104	0x68	RAMP2_LEN[7:0]								0x00
105	0x69	RAMP2_LEN[15:8]								0x00
106	0x6A	RAMP2_NEXT[2:0]			RAMP2_ NEXT_TRIG[1:0]		RAMP2_ RST	RAMP2_FLAG[1:0]		0x00
107	0x6B	RAMP3_INC[7:0]								0x00
108	0x6C	RAMP3_INC[15:8]								0x00
109	0x6D	RAMP3_INC[23:16]								0x00
110	0x6E	RAMP3_ DLY	RAMP3_ FL	RAMP3_INC[29:24]						0x00
111	0x6F	RAMP3_LEN[7:0]								0x00
112	0x70	RAMP3_LEN[15:8]								0x00
113	0x71	RAMP3_NEXT[2:0]			RAMP3_ NEXT_TRIG[1:0]		RAMP3_ RST	RAMP3_FLAG[1:0]		0x00

Register Map (continued)

Table 1. Register Map (continued)

Register		D7	D6	D5	D4	D3	D2	D1	D0	POR
114	0x72	RAMP4_INC[7:0]								0x00
115	0x73	RAMP4_INC[15:8]								0x00
116	0x74	RAMP4_INC[23:16]								0x00
117	0x75	RAMP4_ DLY	RAMP4_ FL	RAMP4_INC[29:24]						0x00
118	0x76	RAMP4_LEN[7:0]								0x00
119	0x77	RAMP4_LEN[15:8]								0x00
120	0x78	RAMP4_NEXT[2:0]			RAMP4_ NEXT_TRIG[1:0]		RAMP4_ RST	RAMP4_FLAG[1:0]		0x00
121	0x79	RAMP5_INC[7:0]								0x00
122	0x7A	RAMP5_INC[15:8]								0x00
123	0x7B	RAMP5_INC[23:16]								0x00
124	0x7C	RAMP5_ DLY	RAMP5_ FL	RAMP5_INC[29:24]						0x00
125	0x7D	RAMP5_LEN[7:0]								0x00
126	0x7E	RAMP5_LEN[15:8]								0x00
127	0x7F	RAMP5_NEXT[2:0]			RAMP5_ NEXT_TRIG[1:0]		RAMP5_ RST	RAMP5_FLAG[1:0]		0x00
128	0x80	RAMP6_INC[7:0]								0x00
129	0x81	RAMP6_INC[15:8]								0x00
130	0x82	RAMP6_INC[23:16]								0x00
131	0x83	RAMP6_ DLY	RAMP6_ FL	RAMP6_INC[29:24]						0x00
132	0x84	RAMP6_LEN[7:0]								0x00
133	0x85	RAMP6_LEN[15:8]								0x00
134	0x86	RAMP6_NEXT[2:0]			RAMP6_ NEXT_TRIG[1:0]		RAMP6_ RST	RAMP6_FLAG[1:0]		0x00
135	0x87	RAMP7_INC[7:0]								0x00
136	0x88	RAMP7_INC[15:8]								0x00
137	0x89	RAMP7_INC[23:16]								0x00
138	0x8A	RAMP7_ DLY	RAMP7_ FL	RAMP7_INC[29:24]						0x00
139	0x8B	RAMP7_LEN[7:0]								0x00
140	0x8C	RAMP7_LEN[15:8]								0x00
141	0x8D	RAMP7_NEXT[2:0]			RAMP7_ NEXT_TRIG[1:0]		RAMP7_ RST	RAMP7_FLAG[1:0]		0x00
142-32767	0x8E- 0x7fff	Reserved								0x00

8.7 Register Field Descriptions

The following sections go through all the programmable fields and their states. Additional information is also available in the applications and feature descriptions sections as well. The POR column is the power on reset state that this field assumes if not programmed.

8.7.1 POWERDOWN and Reset Fields

Table 2. POWERDOWN and Reset Fields

<table>
<tr><th>Field</th><th>Location</th><th>POR</th><th colspan="3">Description and States</th></tr>
<tr><td rowspan="5">POWERDOWN [1:0]</td><td rowspan="5">R2[1:0]</td><td rowspan="5">0</td><td rowspan="5">POWERDOWN Control</td><td>Value</td><td>POWERDOWN State</td></tr>
<tr><td>0</td><td>POWERDOWN, ignore CE</td></tr>
<tr><td>1</td><td>Power Up, ignore CE</td></tr>
<tr><td>2</td><td>Power State Defined by CE terminal state</td></tr>
<tr><td>3</td><td>Reserved</td></tr>
<tr><td rowspan="3">SWRST</td><td rowspan="3">R2[2]</td><td rowspan="3">0</td><td rowspan="3">Software Reset. Setting this bit sets all registers to their POR default values.</td><td>Value</td><td>Reset State</td></tr>
<tr><td>0</td><td>Normal Operation</td></tr>
<tr><td>1</td><td>Register Reset</td></tr>
</table>

8.7.2 Dividers and Fractional Controls

Table 3. Dividers and Fractional Controls

Field	Location	POR	Description and States		
PLL_N [17:0]	R18[1] to R16[0]	16	Feedback N counter Divide value. Minimum count is 16. Maximum is 262132. Writing of the register R16 begins any ramp execution when RAMP_EN=1.		
FRAC_ DITHER [1:0]	R18[3:2]	0	Dither used by the fractional modulator	**Value**	**Dither**
				0	Weak
				1	Medium
				2	Strong
				3	Disabled
FRAC_ ORDER [2:0]	R18[6:4]	0	Fractional Modulator order	**Value**	**Modulator Order**
				0	Integer Mode
				1	1st Order Modulator
				2	2nd Order Modulator
				3	3rd Order Modulator
				4	4th Order Modulator
				5-7	Reserved
FRAC_NUM [23:0]	R21[7] to R19[0]	0	Fractional Numerator. This value should be less than or equal to the fractional denominator.		
FRAC_DEN [23:0]	R24[7] to R22[0]	0	Fractional Denominator. If the RAMP_EN=1, this field is ignored and the denominator is fixed to 2^{24}.		
PLL_R [15:0]	R26[7] to R25[0]	1	Reference Divider value. Selecting 1 will bypass counter.		
OSC_2X	R27[0]	0	Enables the Doubler before the Reference divider	**Value**	**Doubler**
				0	Disabled
				1	Enabled
PLL_R _DIFF	R27[2]	0	Enables the Differential R counter. This allows for higher OSCin frequencies, but restricts PLL_R to divides of 2,4,8 or 16.	**Value**	**R Divider**
				0	Single-Ended
				1	Differential
PFD_DLY [1:0]	R27[4:3]	1	Sets the charge pump minimum pulse width. This could potentially be a trade-off between fractional spurs and phase noise. Setting 1 is recommended for general use.	**Value**	**Pulse Width**
				0	Reserved
				1	860 ps
				2	1200 ps
				3	1500 ps
CPG [4:0]	R28[4:0]	0	Charge pump gain	**Value**	**Charge Pump State**
				0	Tri-State
				1	100 uA
				2	200 uA
				…	…
				31	3100 uA
CPPOL	R28[5]	0	Charge Pump Polarity Positive is for a positive slope VCO characteristic, negative otherwise.	**Value**	**Charge Pump Polarity**
				0	Negative
				1	Positive

8.7.2.1 Speed Up Controls (Cycle Slip Reduction and Fastlock)

Table 4. FastLock and Cycle Slip Reduction

Field	Location	POR	Description and States		
FL_ CSR [1:0]	R27[6:5]	0	Cycle Slip Reduction (CSR) reduces the phase detector frequency by multiplying both the R and N counters by the CSR value while either the FastLock Timer is counting or the RAMPx_FL=1 and the part is ramping. Care must be taken that the R and N divides remain inside the range of the counters. Cycle slip reduction is generally not recommended during ramping.	**Value**	**CSR Value**
				0	Disabled
				1	x 2
				2	x 4.
				3	Reserved
FL_ CPG [4:0]	R29[4:0]	0	Charge pump gain only when Fast Lock Timer is counting down or a ramp is running with RAMPx_FL=1	**Value**	**Fastlock Charge Pump Gain**
				0	Tri-State
				1	100 uA
				2	200 uA
				…	…
				31	3100 uA
FL_ TOC [10:0]	R29[7:5] and R32[7:0]	0	Fast Lock Timer. This counter starts counting when the user writes the PLL_N(Register R16). During this time the FL_CPG gain is sent to the charge pump, and the FL_CSR shifts the R and N counters if enabled. When the counter terminates, the normal CPG is presented and the CSR undo's the shifts to give a normal PFD frequency.	**Value**	**Fastlock Timer Value**
				0	Disabled
				1	1 x 32 = 32
				...	
				2047	2047 x 32 = 65504

8.8 Lock Detect and Charge Pump Monitoring

Table 5. Lock Detect and Charge Pump Monitor

Field	Location	POR	Description and States		
CPM_THR _LOW [5:0]	R30[5:0]	0x0A	Charge pump voltage low threshold value. When the charge pump voltage is below this threshold, the LD goes low.	**Value**	**Threshold**
				0	Lowest
				…	…
				63	Highest
CPM_FLAGL	R30[6]	-	This is a read only bit. Low indicates the charge pump voltage is below the minimum threshold.	**Value**	**Flag Indication**
				0	Charge pump is below CPM_THR_LOW threshold
				1	Charge pump is above CPM_THR_LOW threshold
CPM_THR _HIGH [5:0]	R31[5:0]	0x32	Charge pump voltage high threshold value. When the charge pump voltage is above this threshold, the LD goes low.	**Value**	**Threshold**
				0	Lowest
				…	…
				63	Highest
CPM_FLAGH	R31[6]	-	This is a read only bit. Charge pump voltage high comparator reading. High indicates the charge pump voltage is above the maximum threshold.	**Value**	**Threshold**
				0	Charge pump is below CPM_THR_HIGH threshold
				1	Charge pump is above CPM_THR_HIGH threshold
DLD_ PASS_CNT [7:0]	R33[7:0]	0xff	Digital Lock Detect Filter amount. There must be at least DLD_PASS_CNT good edges and less than DLD_ERR edges before the DLD is considered in lock. Making this number smaller will speed the detection of lock, but also will allow a higher chance of DLD chatter.		
DLD_ ERR_CNT [4:0]	R34[4:0]	0	Digital Lock Detect error count. This is the maximum number of errors greater than DLD_TOL that are allowed before DLD is de-asserted. Although the default is 0, the recommended value is 4.		
DLD _TOL [2:0]	R34[7:5]	0	Digital Lock detect edge window. If both N and R edges are within this window, it is considered a “good” edge. Edges that are farther apart in time are considered “error” edges. Window choice depends on phase detector frequency, charge pump minimum pulse width, fractional modulator order and the users desired margin.	**Value**	**Window and Fpd Frequency**
				0	1 ns (Fpd > 130 MHz)
				1	1.7 ns (80 MHz , Fpd ≤ 130 MHz)
				2	3 ns (60 MHz , Fpd ≤ 80 MHz)
				3	6 ns (45 MHz , Fpd ≤ 60 MHz)
				4	10 ns (30 MHz < Fpd ≤ 45 MHz)
				5	18 ns (Fpd ≤ 30 MHz)
				6 and 7	Reserved

8.9 TRIG1,TRIG2,MOD, and MUXout Pins

Table 6. TRIG1, TRIG2, MOD, and MUXout Terminal States

<table>
<tr><th>Field</th><th>Location</th><th>POR</th><th colspan="3">Description and States</th></tr>
<tr><td rowspan="4">TRIG1 _PIN [2:0]</td><td rowspan="4">R36[2:0]</td><td rowspan="4">0</td><td rowspan="9">This is the terminal drive state for the TRIG1, TRIG2, MOD, and MUXout Pins</td><td>Value</td><td>Pin Drive State</td></tr>
<tr><td>0</td><td>TRISTATE (default)</td></tr>
<tr><td>1</td><td>Open Drain Output</td></tr>
<tr><td>2</td><td>Pullup / Pulldown Output</td></tr>
<tr><td>TRIG2 _PIN [2:0]</td><td>R37[2:0]</td><td>0</td><td>3</td><td>Reserved</td></tr>
<tr><td>MOD_ _PIN [2:0]</td><td>R38[2:0]</td><td>0</td><td>4</td><td>GND</td></tr>
<tr><td rowspan="3">MUXout_ _PIN [2:0]</td><td rowspan="3">R39[2:0]</td><td rowspan="3">0</td><td>5</td><td>Inverted Open Drain Output</td></tr>
<tr><td>6</td><td>Inverted Pullup / Pulldown Output</td></tr>
<tr><td>7</td><td>Input</td></tr>
</table>

Table 7. TRIG1, TRIG2, MOD, and MUXout Selections

Field	Location	POR	Description and States		
				Value	**MUX State**
TRIG1_MUX [5:0] TRIG2_MUX [5:0] MOD_MUX [5:0] MUXout_MUX [5:0]	R36[7:3], R37.3 R36[7:3], R35.3 R37[7:3], R35.4 R38[7:3], R35.7	1 2 3 7	These fields control what signal is muxed to or from the TRIG1,TRIG2, MOD, and MUXout pins. Some of the abbreviations used are: COMP0, COMP1: Comparators 0 and 1 LD, DLD: Lock Detect, Digital Lock Detect CPM: Charge Pump Monitor CPG: Charge Pump Gain CPUP: Charge Pump Up Pulse CPDN: Charge Pump Down Pulse	0	GND
				1	Input TRIG1
				2	Input TRIG2
				3	Input MOD
				4	Output TRIG1 after synchronizer
				5	Output TRIG2 after synchronizer
				6	Output MOD after synchronizer
				7	Output Read back
				8	Output CMP0
				9	Output CMP1
				10	Output LD (DLD good AND CPM good)
				11	Output DLD
				12	Output CPMON good
				13	Output CPMON too High
				14	Output CPMON too low
				15	Output RAMP LIMIT EXCEEDED
				16	Output R Divide/2
				17	Output R Divide/4
				18	Output N Divide/2
				19	Output N Divide/4
				20	Reserved
				21	Reserved
				22	Output CMP0RAMP
				23	Output CMP1RAMP
				24	Reserved
				25	Reserved
				26	Reserved
				27	Reserved
				28	Output Faslock
				29	Output CPG from RAMP
				30	Output Flag0 from RAMP
				31	Output Flag1 from RAMP
				32	Output TRIGA
				33	Output TRIGB
				34	Output TRIGC
				35	Output R Divide
				36	Output CPUP
				37	Output CPDN
				38	Output RAMP_CNT Finished
				39 to 63	Reserved

8.10 Ramping Functions

Table 8. Ramping Functions

Field	Location	POR	Description and States	Value	State
RAMP_EN	R58[0]	0	Enables the RAMP functions. When this bit is set, the Fractional Denominator is fixed to 2^{24}. RAMP execution begins at RAMP0 upon the PLL_N[7:0] write. The Ramp should be set up before RAMP_EN is set.	**Value**	**Ramp**
				0	Disabled
				1	Enabled
RAMP_CLK	R58[1]	0	RAMP clock input source. The ramp can be clocked by either the phase detector clock or the MOD terminal based on this selection.	**Value**	**Source**
				0	Phase Detector
				1	MOD Terminal
RAMP_PM_EN	R58[2]	0	Phase modulation enable.	**Value**	**Modulation Type**
				0	Frequency Modulation
				1	Phase Modulation
RAMP_TRIGA [3:0] RAMP_TRIGB [3:0] RAMP_TRIGC [3:0]	R58[7:4] R59[3:0] R59[7:4]	0	Trigger A,B, and C Sources	**Value**	**Source**
				0	Never Triggers (default)
				1	TRIG1 terminal rising edge
				2	TRIG2 terminal rising edge
				3	MOD terminal rising edge
				4	DLD Rising Edge
				5	CMP0 detected (level)
				6	RAMPx_CPG Rising edge
				7	RAMPx_FLAG0 Rising edge
				8	Always Triggered (level)
				9	TRIG1 terminal falling edge
				10	TRIG2 terminal falling edge
				11	MOD terminal falling edge
				12	DLD Falling Edge
				13	CMP1 detected (level)
				14	RAMPx_CPG Falling edge
				15	RAMPx_FLAG0 Falling edge
RAMP_CMP0 [32:0]	R70[0], R63[7] to R60[0]	0	Twos compliment of Ramp Comparator 0 value. Be aware of that the MSB is in Register R70.		
RAMP_CMP0_EN [7:0]	R64[7:0]	0	Comparator 0 is active during each RAMP corresponding to the bit. Place a 1 for ramps it is active in and 0 for ramps it should be ignored. RAMP0 corresponds to R64[0], RAMP7 corresponds to R64[7]		
RAMP_CMP1 [32:0]	R70[1], R68[7] to R65[0]	0	Twos compliment of Ramp Comparator 1 value. Be aware of that the MSB is in Register R70.		
RAMP_CMP1_EN [7:0]	R69[7:0]	0	Comparator 1 is active during each RAMP corresponding to the bit. Place a 1 for ramps it is active in and 0 for ramps it should be ignored. RAMP0 corresponds to R64[0], RAMP7 corresponds to R64[7].		
FSK_TRIG [1:0]	R76[4] to R75[3]	0	Deviation trigger source. When this trigger source specified is active, the FSK_DEV value is applied.	**Value**	**Trigger**
				0	Always Triggered
				1	Trigger A
				2	Trigger B
				3	Trigger C
FSK_DEV [32:0]	R70[2], R74[7] to R71[0]	0	Twos compliment of the deviation value for frequency modulation and phase modulation. This value should be written with 0 when not used. Be aware that the MSB is in Register R70.		

Ramping Functions (continued)

Table 8. Ramping Functions (continued)

<table>
<tr><th>Field</th><th>Location</th><th>POR</th><th colspan="3">Description and States</th></tr>
<tr><td>RAMP_LIMIT_LOW [32:0]</td><td>R70[3], R78[7] to 75[0]</td><td>0x000 00000</td><td colspan="3">Twos compliment of the ramp lower limit that the ramp can not go below . The ramp limit occurs before any deviation values are included. Care must be taken if the deviation is used and the ramp limit must be set appropriately. Be aware that the MSB is in Register R70.</td></tr>
<tr><td>RAMP_LIMIT_HIGH [32:0]</td><td>R70[4], R82[7] to 79.0[0]</td><td>0xfffffff f</td><td colspan="3">Twos compliment of the ramp higher limit that the ramp can not go above. The ramp limit occurs before any deviation values are included. Care must be taken if the deviation is used and the ramp limit must be set appropriately. Be aware that the MSB is in Register R70.</td></tr>
<tr><td>RAMP_COUNT [12:0]</td><td>R84[4] to R83[0]</td><td>0</td><td colspan="3">Number of RAMPs that will be executed before a trigger or ramp enable is brought down. Load zero if this feature is not used. Counter is automatically reset when RAMP_EN goes from 0 to 1.</td></tr>
<tr><td rowspan="3">RAMP_AUTO</td><td rowspan="3">R84[5]</td><td rowspan="3">0</td><td rowspan="3">Automatically clear RAMP_EN when RAMP Count hits terminal count.</td><th>Value</th><th>Ramp</th></tr>
<tr><td>0</td><td>RAMP_EN unaffected by ramp counter (default)</td></tr>
<tr><td>1</td><td>RAMP_EN automatically brought low when ramp counter terminal counts</td></tr>
<tr><td rowspan="5">RAMP_TRIG_INC [1:0]</td><td rowspan="5">R84[7:6]</td><td rowspan="5">0</td><td rowspan="5">Increment Trigger source for RAMP Counter. To disable ramp counter, load a count value of 0.</td><th>Value</th><th>Source</th></tr>
<tr><td>0</td><td>Increments occur on each ramp transition</td></tr>
<tr><td>1</td><td>Increment occurs on trigA</td></tr>
<tr><td>2</td><td>Increment occurs on trigB</td></tr>
<tr><td>3</td><td>Increment occurs on trigC</td></tr>
</table>

8.11 Individual Ramp Controls

These bits apply for all eight ramps. For the field names, x can be 0,1,2,3,4,5,6, or 7.

Table 9. Individual Ramp Controls

<table>
<tr><th>Field</th><th>Location</th><th>POR</th><th colspan="3">Description and States</th></tr>
<tr><td>RAMPx _INC[29:0]</td><td>Varies</td><td>0</td><td colspan="3">Signed ramp increment.</td></tr>
<tr><td rowspan="3">RAMPx _FL</td><td rowspan="3">Varies</td><td rowspan="3">0</td><td rowspan="3">This enables fastlock and cycle slip reduction for ramp x.</td><td>Value</td><td>CPG</td></tr>
<tr><td>0</td><td>Disabled</td></tr>
<tr><td>1</td><td>Enabled</td></tr>
<tr><td rowspan="3">RAMPx _DLY</td><td rowspan="3">Varies</td><td rowspan="3">0</td><td rowspan="3">During this ramp, each increment takes 2 PFD cycles per LEN clock instead of the normal 1 PFD cycle. Slows the ramp by a factor of 2.</td><td>Value</td><td>Clocks</td></tr>
<tr><td>0</td><td>1 PFD clock per RAMP tick.(default)</td></tr>
<tr><td>1</td><td>2 PFD clocks per RAMP tick.</td></tr>
<tr><td>RAMPx _LEN</td><td>Varies</td><td>0</td><td colspan="3">Number of PFD clocks (if DLY is 0) to continue to increment RAMP. 1=>1 cycle, 2=>2 etc. Maximum of 65536 cycles.</td></tr>
<tr><td rowspan="5">RAMPx _FLAG[1:0]</td><td rowspan="5">Varies</td><td rowspan="5">0</td><td rowspan="5">General purpose FLAGS sent out of RAMP.</td><td>Value</td><td>Flag</td></tr>
<tr><td>0</td><td>Both FLAG1 and FLAG0 are zero. (default)</td></tr>
<tr><td>1</td><td>FLAG0 is set, FLAG1 is clear</td></tr>
<tr><td>2</td><td>FLAG0 is clear, FLAG1 is set</td></tr>
<tr><td>3</td><td>Both FLAG0 and FLAG1 are set.</td></tr>
<tr><td rowspan="3">RAMP0 _RST</td><td rowspan="3">Varies</td><td rowspan="3">0</td><td rowspan="3">Forces a clear of the ramp accumulator. This is used to erase any accumulator creep that can occur depending on how the ramps are defined. Should be done at the start of a ramp pattern.</td><td>Value</td><td>Reset</td></tr>
<tr><td>0</td><td>Disabled</td></tr>
<tr><td>1</td><td>Enabled</td></tr>
<tr><td rowspan="5">RAMPx_ NEXT _TRIG [1:0]</td><td rowspan="5">Varies</td><td rowspan="5">0</td><td rowspan="5">Determines what event is necessary to cause the state machine to go to the next ramp. It can be set to when the RAMPx_LEN counter reaches zero or one of the events for Triggers A,B, or C.</td><td>Value</td><td>Operation</td></tr>
<tr><td>0</td><td>RAMPx_LEN</td></tr>
<tr><td>1</td><td>TRIG_A</td></tr>
<tr><td>2</td><td>TRIG_B</td></tr>
<tr><td>3</td><td>TRIG_C</td></tr>
<tr><td>RAMP0 _NEXT[2:0]</td><td>Varies</td><td>0</td><td colspan="3">The next RAMP to execute when the length counter times out</td></tr>
</table>

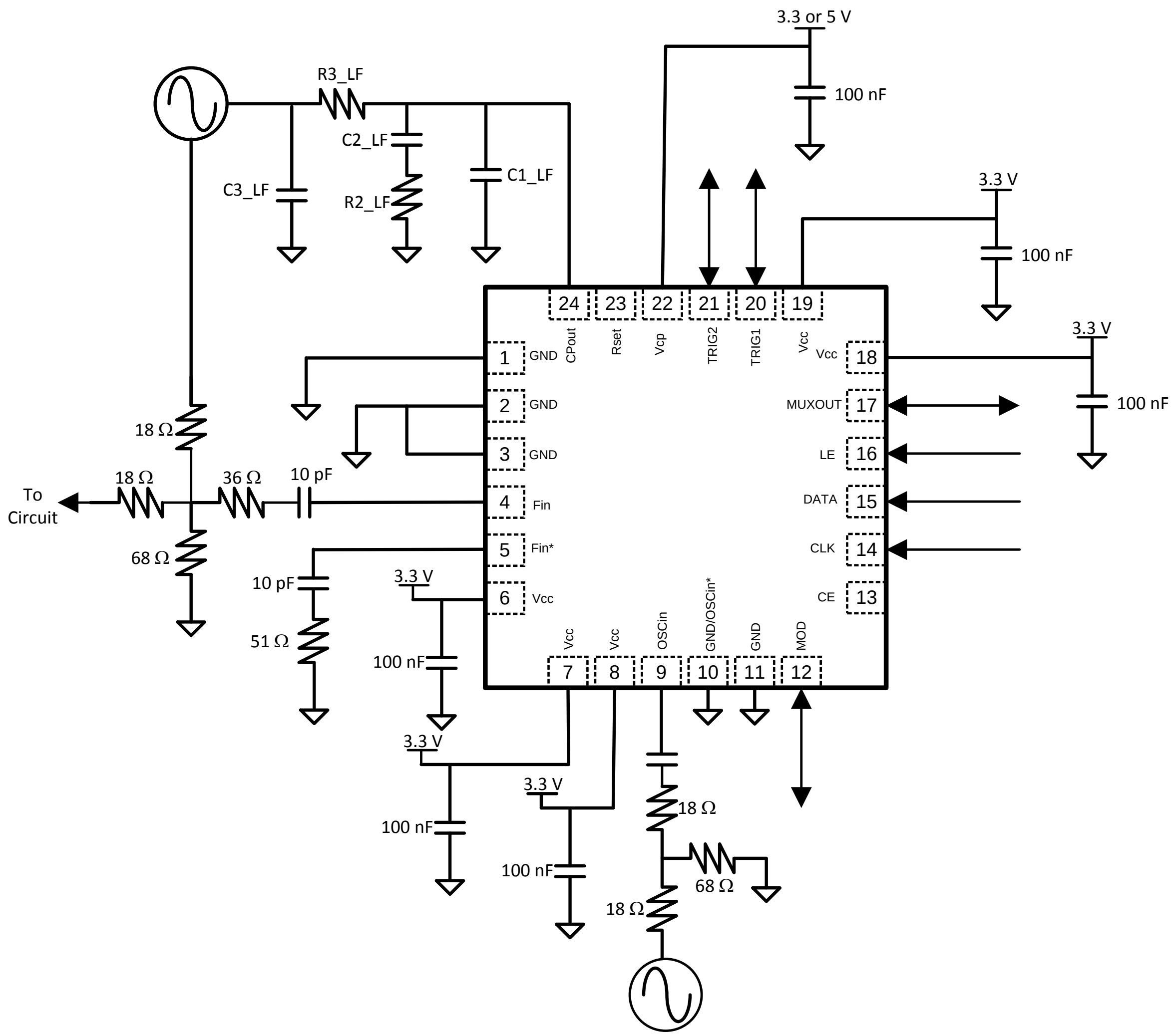
9 Applications and Implementation

9.1 Application Information

The LMX2492/92-Q1 can be used in a broad class of applications such as generating a single frequency for a high frequency clock, generating a tunable range of frequencies, or generating swept waveforms that can be used in applications such as radar.

9.2 Typical Applications

The following schematic is an example of hat could be used in a typical application.



9.2.1 Design Requirements

For these examples, it will be assumed that there is a 100 MHz input signal and the output frequency is between 9400 and 9800 MHz with various modulated waveforms.

Parameter	Symbol	Value	Comments
Input Frequency	OSCin	100 MHz	
Phase Detector Frequency	Fpd	100 MHz	There are many possibilities, but this choice gives good performance and saves a little current (as shown in the electrical specifications).

Typical Applications (continued)

Parameter	Symbol	Value	Comments
VCO Frequency	Fvco	9400 - 9800 MHz (Simple Chirp)	In the different examples, the VCO frequency is actually changing. However, the same loop filter design can be used for all three.
		9400 - 9800 (Flattened Ramp)	
		9500 - 9625 MHz (Complex Triggered Ramp	
VCO Gain	Kvco	200 MHz/V	This parameter has nothing to do with the LMX2492/92-Q1, but is rather set by the external VCO choice.

9.2.2 Detailed Design Procedure

The first step is to calculate the reference divider (PLL_R) and feedback divider (PLL_N) values as shown in the table that follows.

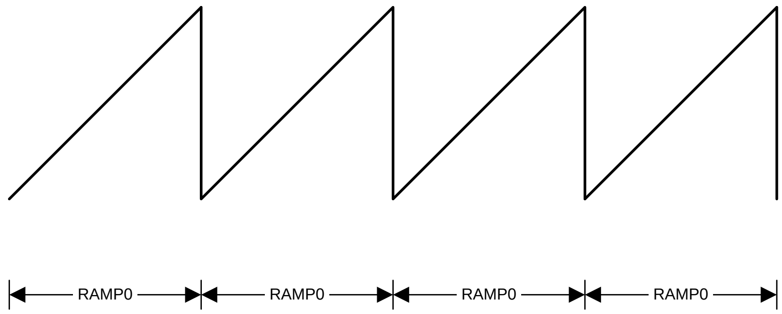
Parameter	Symbol and Calculations	Value	Comments
Average VCO Frequency	$Fvco_{Avg}$ = $(Fvco_{Max} + Fvco_{Min})/2$	9600 MHz	To design a loop filter, one designs for a fixed VCO value, although it is understood that the VCO will tune around. This typical value is usually chosen as the average VCO frequency.
VCO Gain	Kvco	200 MHz/V	This parameter has nothing to do with the LMX2492/92-Q1, but is rather set by the external VCO choice. In this case, it was the RFMD1843 VCO.
PLL Loop Bandwidth	BW	380 kHz	This bandwidth is very wide to allow the VCO frequency to be modulated.
Charge Pump Gain	CPG	3.1 mA	Using the larger gain allows a wider loop bandwidth and gives good phase performance.
R Divider	PLL_R = OSCin / Fpd	1	This value is calculated from previous values.
N Divider	PLL_N = Fvco / Fpd	96	This value is calculated from previous values.
Loop Filter Components	C1_LF	68 pF	These were calculated by TI design tools.
	C2_LF	3.9 nF	
	C3_LF	150 pF	
	R2_LF	390 ohm	
	R3_LF	390 ohm	

Once a loop filter bandwidth is chosen, the external loop filter components of C1_LF, C2_LF, C3_LF, R2_LF, and R3_LF can be calculated with a tool such as the Clock Architect tool available at www.ti.com. It is also highly recommended to look at the EVM instructions. The CodeLoader software is an excellent starting point and example to see how to program this device.

9.2.3 Application Performance Plot - Sawtooth Waveform Example

Using the above design, it can be programmed to generate a sawtooth waveform with the following paramters.

Parameter	Symbol	Value
Ramp Duration	ΔT	100 uS
VCO Frequency	Fvco	9400 - 9800 MHz
Range	ΔF	9400 - 9800 MHz = 400 MHz Change



Because we want the ramp length to be 100 us, this works out to 10,000 phase detector cycles which means that RAMP0_LEN=10000. To change 400 MHz, we know that each one of the 10000 steps is 40 kHz. Given the fractional denominator is 2^{24} = 16777216 and the phase detector frequency is 100 MHz, this implies that the fractional numerator at the end of the ramp will be 6711. However, since this 6711 number is not exact (closer to 6718.8864), the ramp will creep if we do not reset it. Therefore, we set reset the ramp. After the ramp finishes, we want to start with the same ramp, so RAMP0_NEXT is RAMP0. The results of this analysis are in the table below:

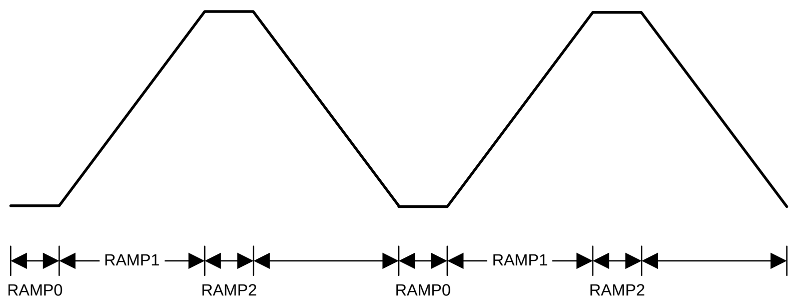
RAMP	RAMP0_LEN	RAMP0_INC	RAMP0_NEXT	RAMP0_RST
RAMP0	ΔT × Fpd = 100 us / 100 MHz = 10000	(ΔF / Fpd) /RAMP0_LEN × 2^{24} = (400/100)/10000 ×16777216 = 6711	0	1

The actual measured waveform for this is shown in the following figure. Note that the frequency that was actually measured was from the divide by two output of the VCO and therefore the measured frequency was half of the actual frequency presented to the PLL. This ramping waveform does show some undershoot as the frequency rapidly returns from 9800 MHz (4900 MHz on the plot) to 9400 MHz (4700 MHz on the plot). This undershoot can be mitigated by adding additional ramps.

9.2.4 Application Performance Plot - Flat Top Triangle Waveform

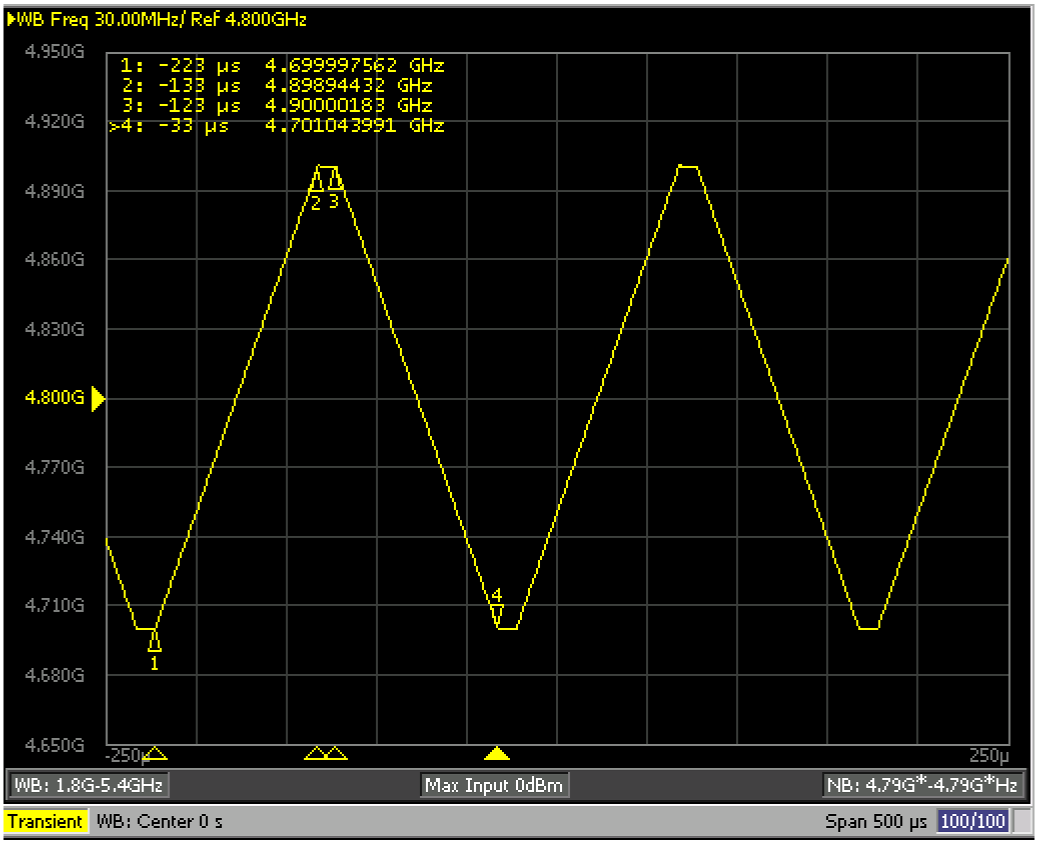
Now consider pattern as shown below. The ramp is sometimes used because it can better account for Doppler Shift. The purpose for making the top and bottom portions flat is to help reduce the impact of the PLL overshooting and undershooting in order to make the sloped ramped portions more linear.

Parameter	Symbol	Value
Ramp Duration	ΔT0	10 uS
	ΔT1	90 uS
	ΔT2	10 uS
	ΔT3	90 uS
Range	ΔF0	0
	ΔF1	400 MHz
	ΔF2	0
	ΔF3	-400 MHz



RAMP	RAMPx_LEN	RAMPx_INC	RAMPx_NEXT	RAMPx_RST
RAMP0	10 us/ 100 MHz =1000	0	1	1
RAMP1	90 us / 100 MHz =9000	(ΔF / Fpd) /RAMP1_LEN × 2^{24} = (400/100)/9000 ×16777216 = 7457	2	0
RAMP2	10 us/ 100 MHz =1000	0	3	0
RAMP3	90 us / 100 MHz =9000	(ΔF / Fpd) /RAMP1_LEN × 2^{24} = (-400/100)/9000 ×16777216 = -7457 Program in 2's complement of -7457 = 2^{30}-7457 = 1073734367	0	0

The actual measured waveform for this is shown in the following figure. Note that the frequency that was actually measured was from the divide by two output of the VCO and therefore the measured frequency was half of the actual frequency presented to the PLL. The flattened top and bottom of this triangle wave help mitigate the overshoot and undersoot in the frequency.



The actual measured waveform for this is shown in the following figure. Note that the frequency that was actually measured was from the divide by two output of the VCO and therefore the measured frequency was half of the actual frequency presented to the PLL. The flattened top and bottom of this triangle wave help mitigate the overshoot and undersoot in the frequency.

9.2.5 Applications Performance Plot -- Complex Triggered Ramp

In this example, the modulation is not started until a trigger pulse from the MOD terminal goes high. Assume a phase detector frequency of 100 MHz and we RAMP1 to be 60 us and ramps 2,3,and 4 to be 12 us each. We set the next trigger for RAMP0 to be trigger A and define trigger A to be the MOD terminal. Then we configure as follows:

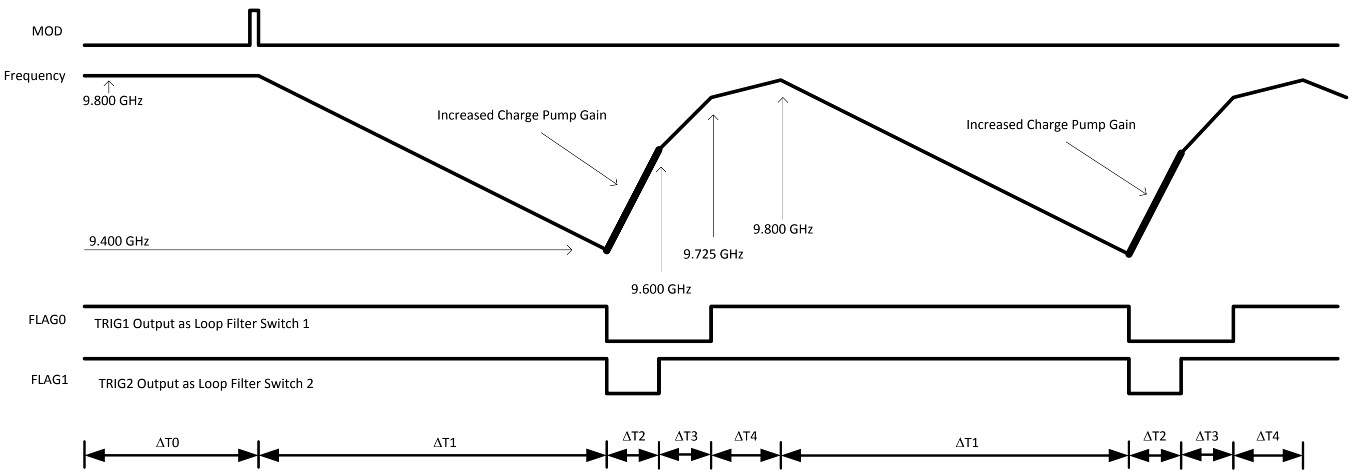


Figure 5. Complex Triggered Ramp Example

RAMP	RAMPx _LEN	RAMPx_ INC	RAMPx_FL	RAMPx _NEXT	RAMPx_FLAG	RAMPx_ NEXT_TRIG	RAMPx_RST
RAMP0	1	0	0	1	FLAG0 and FLAG1	TRIG A	1
RAMP1	6000	1073730639	0	2	FLAG0 and FLAG1	TOC Timeout	1
RAMP2	1200	27963	1	3	Disabled	TOC Timeout	0
RAMP3	1200	17476	0	4	FLAG1	TOC Timeout	0
RAMP4	1200	10486	0	1	FLAG0 and FLAG1	TOC Timeout	0

The actual measured waveform for this is shown in the following figure. Note that the frequency that was actually measured was from the divide by two output of the VCO and therefore the measured frequency was half of the actual frequency presented to the PLL. The flattened top and bottom of this triangle wave help mitigate the overshoot and undersoot in the frequency.

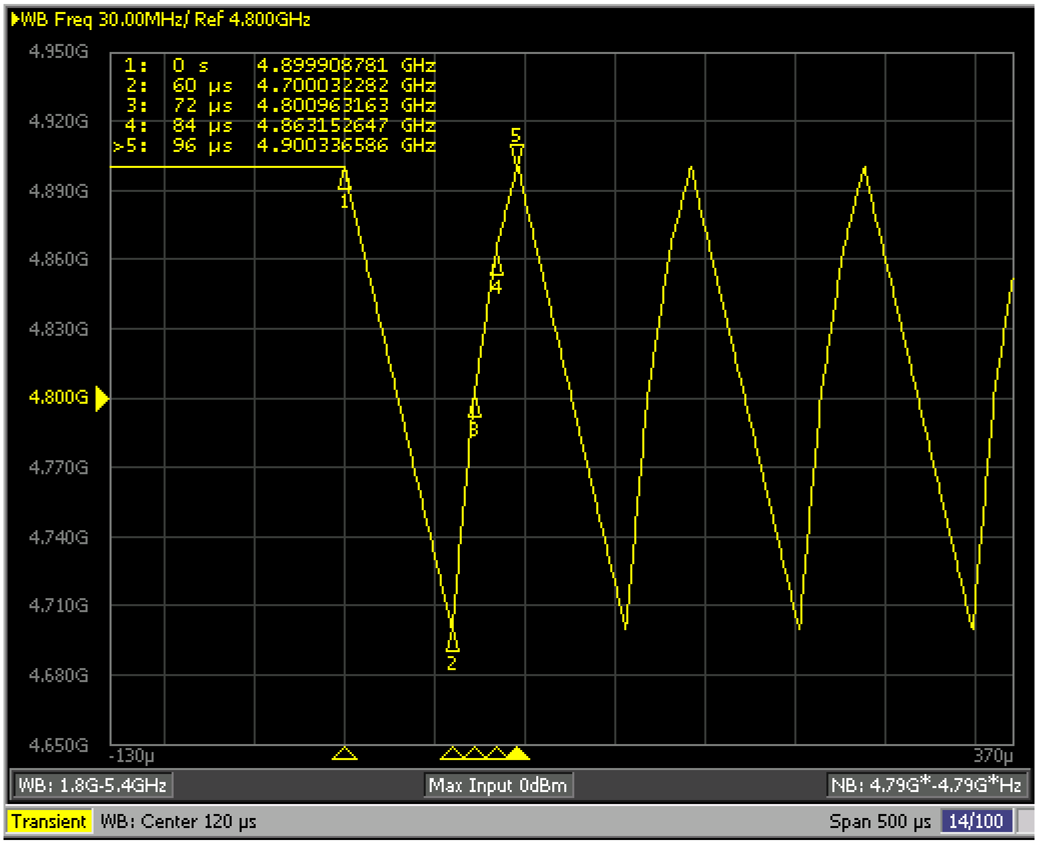


Figure 6. Actual Measurement for Complex Triggered Ramp

10 Power Supply Recommendations

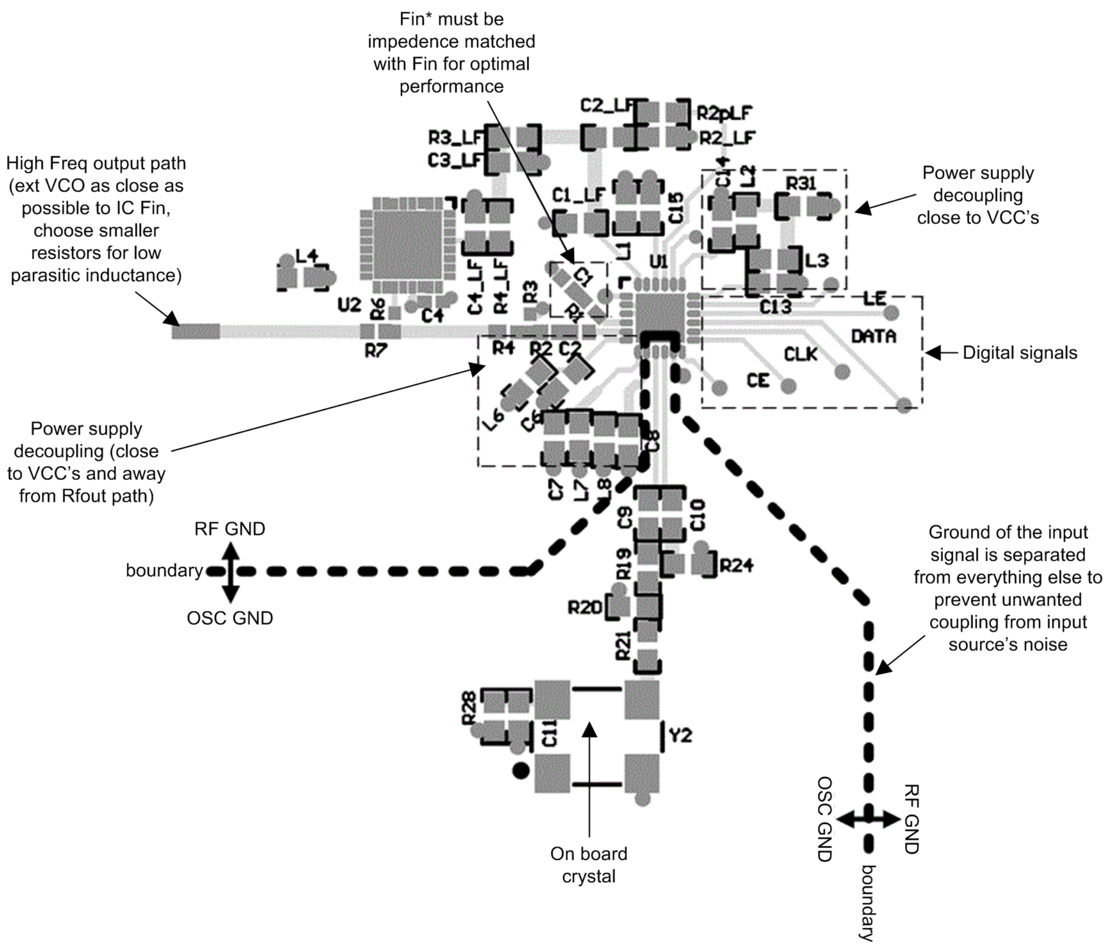
For power supplies, it is recommended to place 100 nF close to each of the power supply pins. If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins can reduce spurs to a small degree.

11 Layout

11.1 Layout Guidelines

For layout examples, the EVM instructions are the most comprehensive document. In general, the layout guidelines are similar to most other PLL devices. For the high frequency Fin pin, it is recommended to use 0402 components and match the trace width to these pad sizes. Also the same needs to be done on the Fin* pin. If layout is easier to route the signal to Fin* instead of Fin, then this is acceptable as well.

11.2 Layout Example



12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

Texas Instruments has several software tools to aid in the development process including CodeLoder for programming, Clock Design Tool for Loop filter design and phase noise/spur simulation, and the Clock Architect. All these tools are available at www.ti.com.

12.2 Documentation Support

12.2.1 Related Documentation

For the avid reader, the following resources are available at www.ti.com.

Application Note 1879 -- Fractional N Frequency Synthesis

PLL Performance, Simulation, and Design -- by Dean Banerjee

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10. Related Links

PARTS	PRODUCT FOLDER	SAMPLE and BUY	TECHNICAL DOCUMENTS	TOOLS and SOFTWARE	SUPPORT and COMMUNITY
LMX2492	Click here	Click here	Click here	Click here	Click here
LMX2492-Q1	Click here	Click here	Click here	Click here	Click here

12.4 Trademarks

All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 要获得这份数据表的浏览器版本，请查阅左侧导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMX2492QRTWRQ1	ACTIVE	WQFN	RTW	24	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	X2492Q	Samples
LMX2492QRTWTQ1	ACTIVE	WQFN	RTW	24	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	X2492Q	Samples
LMX2492RTWR	ACTIVE	WQFN	RTW	24	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	X2492	Samples
LMX2492RTWT	ACTIVE	WQFN	RTW	24	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	X2492	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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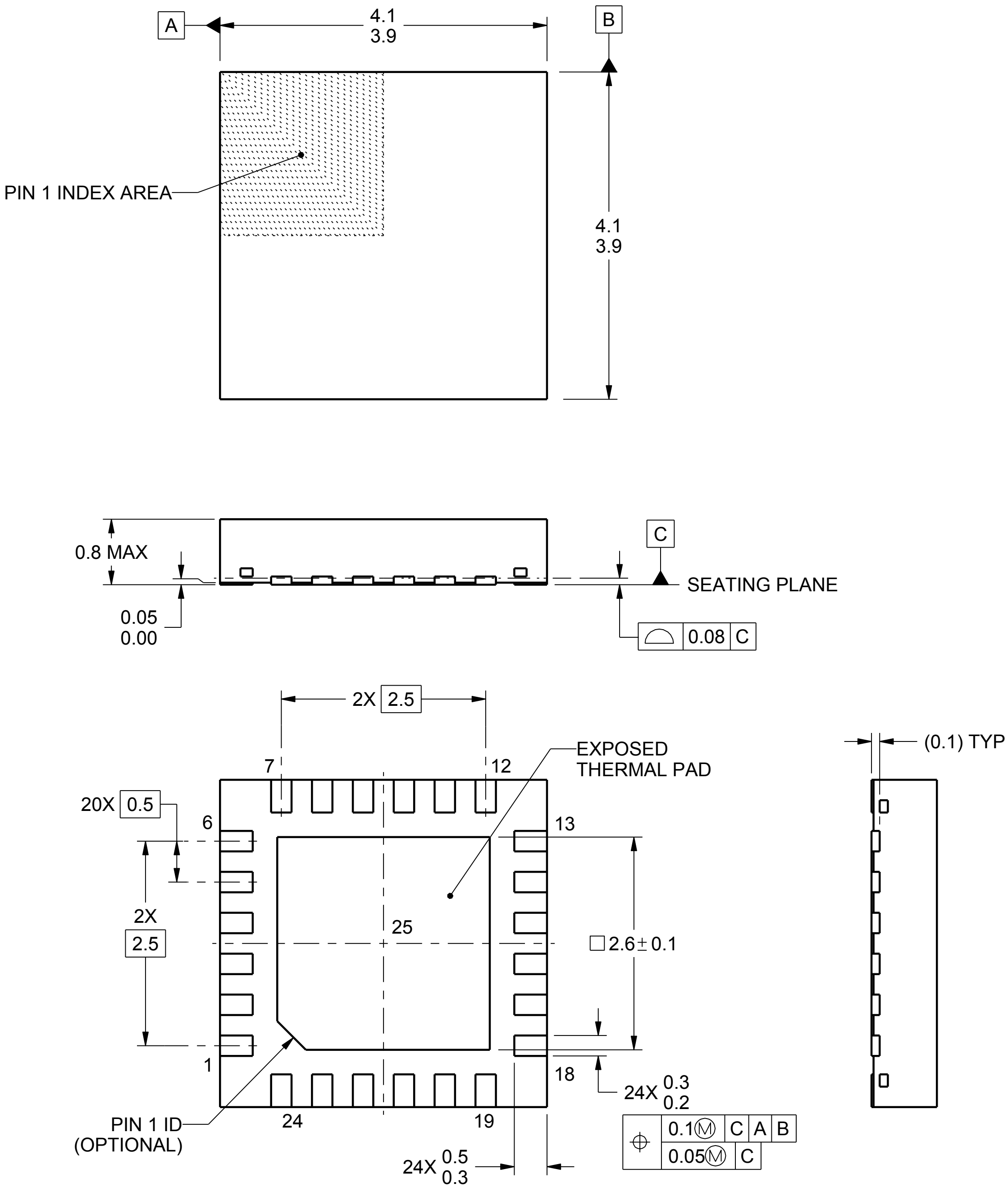
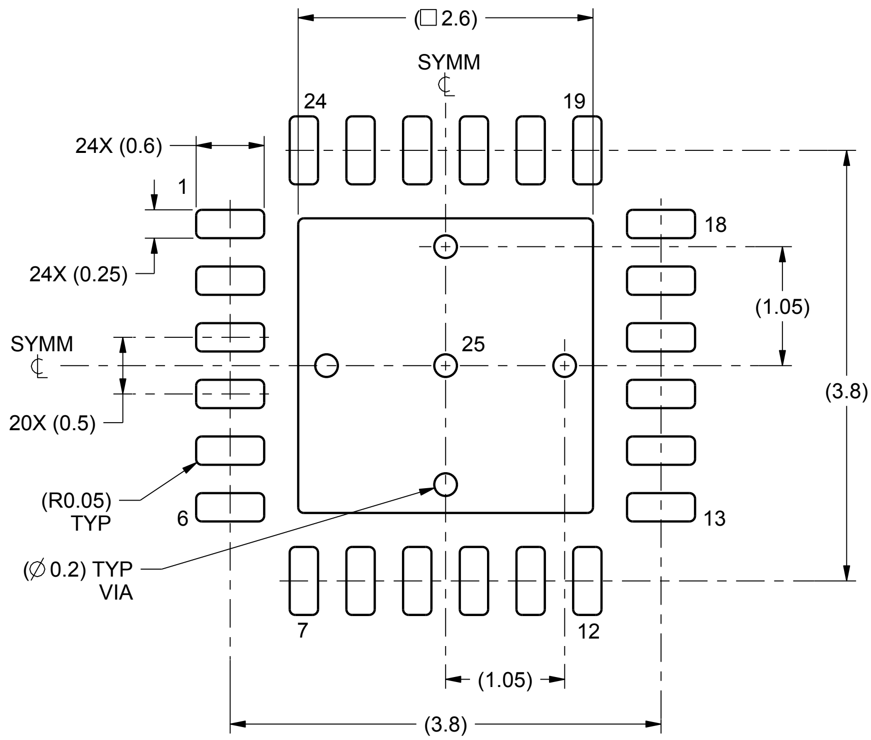


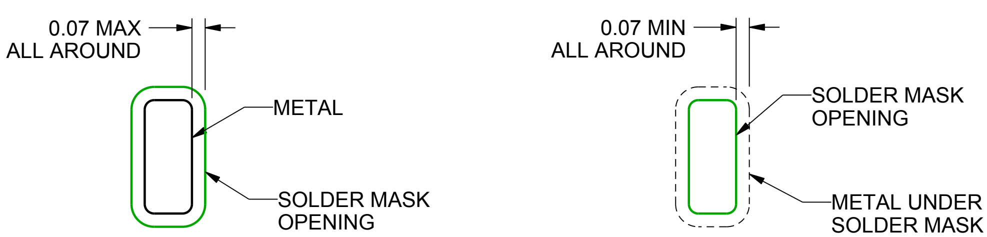
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

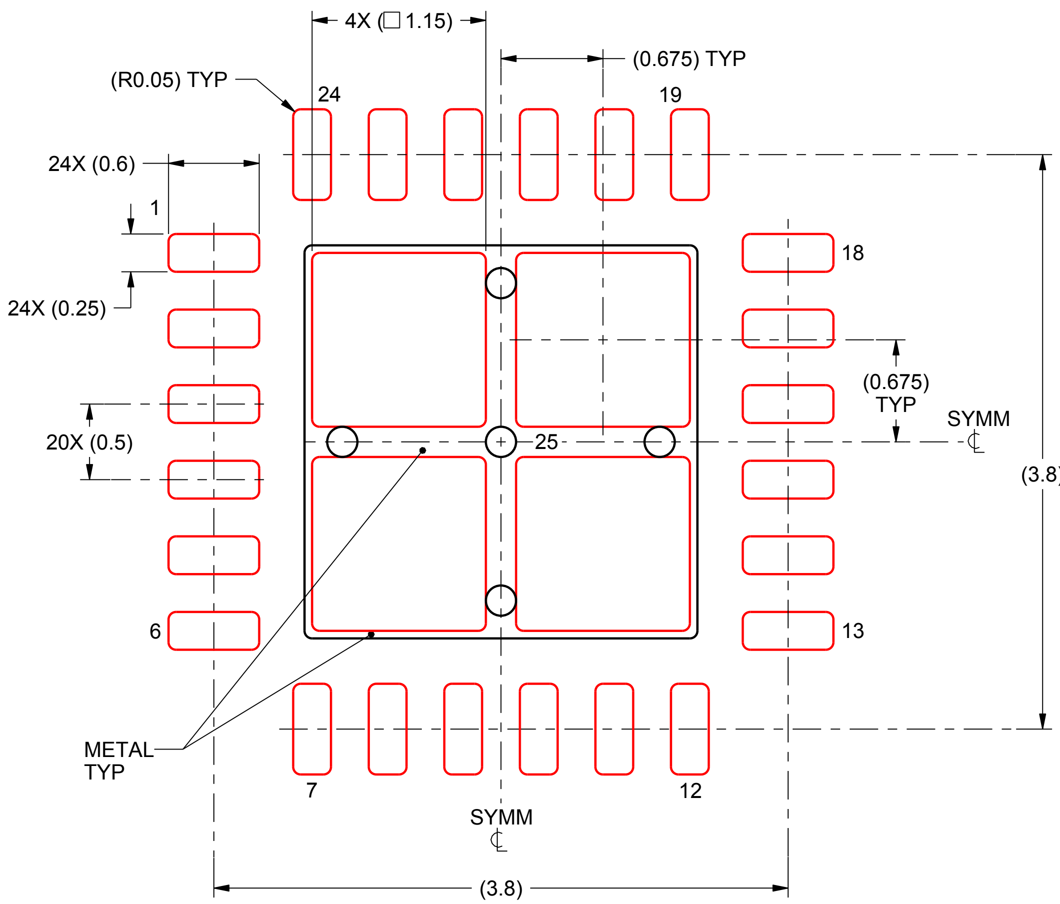
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222815/A 03/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222815/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265