

MSPM0L130x Mixed-Signal Microcontrollers

1 Features

• Core

- Arm® 32-bit Cortex®-M0+ CPU, frequency up to 32 MHz

• Operating characteristics

- Extended temperature: –40°C to 125°C
- Wide supply voltage range: 1.62 V to 3.6 V

• Memories

- Up to 64KB of flash
- Up to 4KB of SRAM

• High-performance analog peripherals

- One 12-bit 1.68-Msps analog-to-digital converter (ADC) with up to 10 total external channels
- Configurable 1.4-V or 2.5-V internal ADC voltage reference (VREF)
- Two zero-drift, zero-crossover chopper operational amplifiers (OPA)
 - 0.5- μ V/°C drift with chopping
 - 6-pA input bias current ¹
 - Integrated programmable gain stage (1-32x)
- One general-purpose amplifier (GPAMP)
- One high-speed comparator (COMP) with 8-bit reference DAC
 - 32-ns propagation delay
 - Low power mode down to <1- μ A
- Programmable analog connections between ADC, OPAs, COMP, and DAC
- Integrated temperature sensor

• Optimized low-power modes

- RUN: 71 μ A/MHz (CoreMark)
- STOP: 151 μ A at 4 MHz and 44 μ A at 32 kHz
- STANDBY: 1.0 μ A with 32-kHz 16-bit timer running, SRAM/registers fully retained, and 32MHz clock wakeup in 3.2 μ s
- SHUTDOWN: 61 nA with IO wakeup capability

• Intelligent digital peripherals

- 3-channel DMA controller
- 3-channel event fabric signaling system
- Four 16-bit general-purpose timers, each with two capture/compare registers supporting low-power operation in STANDBY mode, supporting a total of 8 PWM channels
- Windowed watchdog timer

• Enhanced communication interfaces

- Two UART interfaces; one supporting LIN, IrDA, DALI, Smart Card, Manchester and both supporting low-power operation in STANDBY

- Two I²C interfaces; one supporting FM+ (1 Mbit/s) and both supporting SMBus, PMBus, and wakeup from STOP
- One SPI supporting up to 16 Mbit/s

• Clock system

- Internal 4- to 32-MHz oscillator with $\pm 1.2\%$ accuracy (SYSOSC)
- Internal 32-kHz low-frequency oscillator with $\pm 3\%$ accuracy (LFOSC)

• Data integrity

- Cyclic redundancy checker (CRC-16 or CRC-32)

• Flexible I/O features

- Up to 28 GPIOs
- Two 5-V-tolerant open-drain IOs with fail-safe protection

• Development support

- 2-pin serial wire debug (SWD)

• Package options

- 32-pin VQFN (RHB)
- 32-pin VSSOP (DGS)
- 28-pin VSSOP (DGS)
- 24-pin VQFN (RGE)
- 20-pin VSSOP (DGS)
- 16-pin SOT(DYY)
- 16-pin WQFN (RTR)

• Family members (also see [Device Comparison](#))

- MSPM0L13x3: 8KB of flash, 2KB of RAM
- MSPM0L13x4: 16KB of flash, 2KB of RAM
- MSPM0L13x5: 32KB of flash, 4KB of RAM
- MSPM0L13x6: 64KB of flash, 4KB of RAM

• Development kits and software (also see [Tools and Software](#))

- LP-MSPM0L1306 LaunchPad™ development kit
- MSP Software Development Kit (SDK)

2 Applications

- [Battery charging and management](#)
- [Power supplies and power delivery](#)
- [Personal electronics](#)
- [Building security and fire safety](#)
- [Connected peripherals and printers](#)
- [Grid infrastructure](#)
- [Smart metering](#)
- [Communication modules](#)
- [Medical and healthcare](#)
- [Lighting](#)

¹ MSPM0L134x only



3 Description

MSPM0L134x and MSPM0L130x microcontrollers (MCUs) are part of the MSP highly-integrated, ultra-low-power [32-bit MSPM0 MCU family](#) based on the enhanced Arm® Cortex®-M0+ core platform operating at up to 32-MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages ranging from 1.62 V to 3.6 V.

The MSPM0L134x and MSPM0L130x devices provide up to 64KB embedded flash program memory with up to 4KB SRAM. These MCUs incorporate a high-speed on-chip oscillator with an accuracy up to $\pm 1.2\%$, eliminating the need for an external crystal. Additional features include a 3-channel DMA, 16- and 32-bit CRC accelerator, and a variety of high-performance analog peripherals such as one 12-bit 1.68-MSPS ADC with configurable internal voltage reference, one high-speed comparator with built-in reference DAC, two zero-drift zero-crossover operational amplifiers with programmable gain, one general-purpose amplifier, and an on-chip temperature sensor. These devices also offer intelligent digital peripherals such as four 16-bit general purpose timers, one windowed watchdog timer, and a variety of communication peripherals including two UARTs, one SPI, and two I²Cs. These communication peripherals offer protocol support for LIN, IrDA, DALI, Manchester, Smart Card, SMBus, and PMBus.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers find the MCU that meets their project's needs. The architecture combined with extensive low-power modes are optimized to achieve extended battery life in portable measurement applications.

MSPM0L134x and MSPM0L130x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad™ development kit available for purchase and design files for a target-socket board. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of [Code Composer Studio™ IDE](#) desktop and cloud version within the [TI Resource Explorer](#). MSPM0 MCUs are also supported by extensive online collateral, training with [MSP Academy](#), and online support through the [TI E2E™ support forums](#).

For complete module descriptions, see the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See [MSP430™ System-Level ESD Considerations](#) for more information; the principles in this application note are applicable to MSPM0 MCUs.

4 Functional Block Diagram

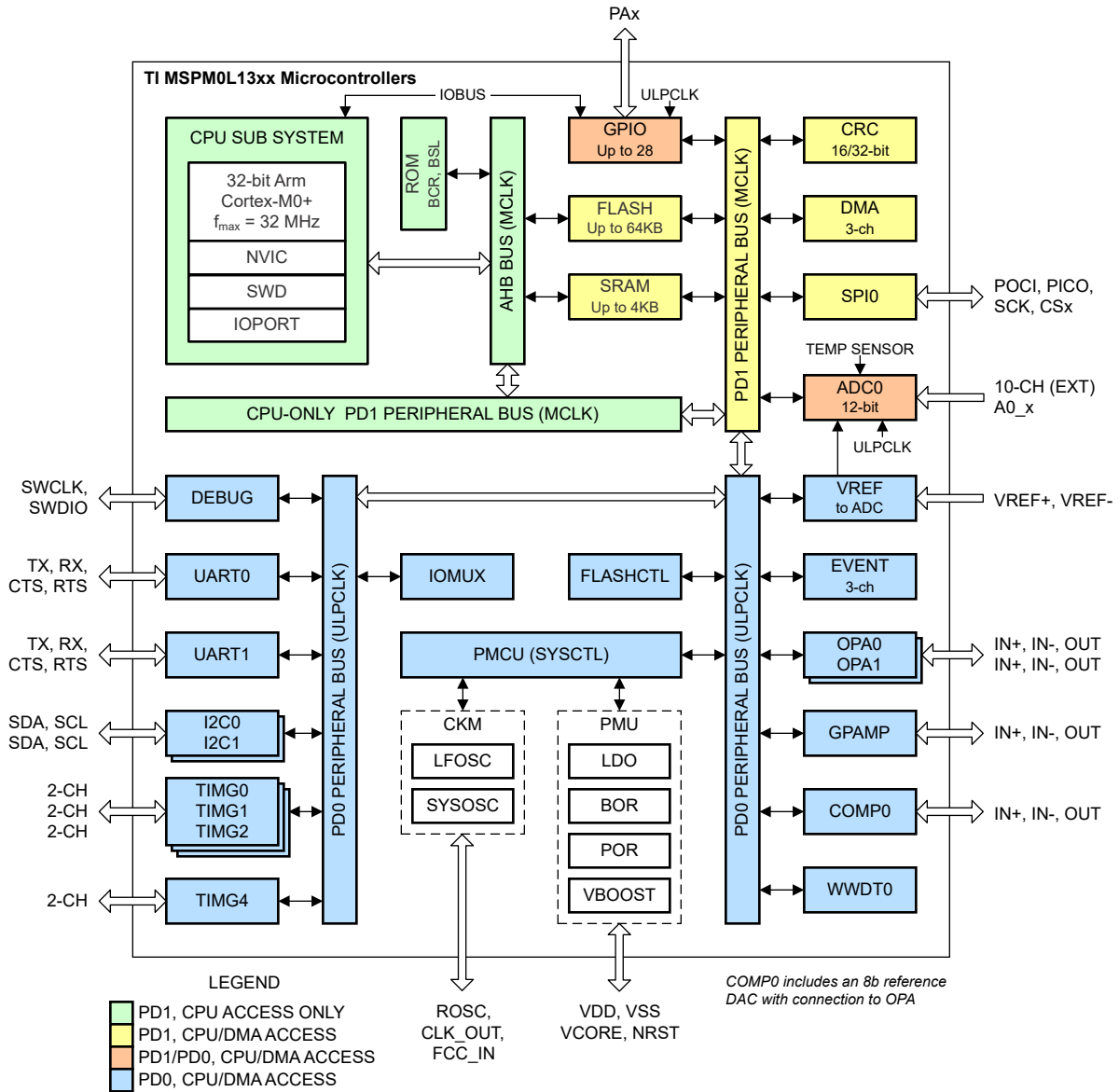


Figure 4-1. MSPM0L134x, MSPM0L130x Functional Block Diagram

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5 Device Comparison

Table 5-1. Device Comparison

| DEVICE NAME ^{(1) (2)} | FLASH / SRAM (KB) | QUAL ⁽³⁾ | ADC CH. | COMP | OPA | GPAMP | UART/I2C/SPI | TIMG | GPIOs | 5-V TOL. IO | PACKAGE [PACKAGE SIZE] ⁽⁴⁾ |
|--------------------------------|-------------------|---------------------|---------|------|-----|-------|--------------|------|-------|-------------|---------------------------------------|
| MSPM0L1306xRHB | 64 / 4 | T/S | 10 | 1 | 2 | 1 | 2 / 2 / 1 | 4 | 28 | 2 | 32 VQFN [5 mm × 5 mm] |
| MSPM0L1305xRHB | 32 / 4 | | | | | | | | | | |
| MSPM0L1304xRHB | 16 / 2 | | | | | | | | | | |
| MSPM0L1306xDGS28 | 64 / 4 | T/S | 10 | 1 | 2 | 1 | 2 / 2 / 1 | 4 | 24 | 2 | 28 VSSOP [7.1 mm × 4.9 mm] |
| MSPM0L1305xDGS28 | 32 / 4 | | | | | | | | | | |
| MSPM0L1304xDGS28 | 16 / 2 | | | | | | | | | | |
| MSPM0L1346xDGS28 | 64 / 4 | T | 9 | | | | | | 22 | | |
| MSPM0L1345xDGS28 | 32 / 4 | | | | | | | | | | |
| MSPM0L1306xRGE | 64 / 4 | T/S | 9 | 1 | 2 | 1 | 2 / 2 / 1 | 4 | 20 | 2 | 24 VQFN [4 mm × 4 mm] |
| MSPM0L1305xRGE | 32 / 4 | | | | | | | | | | |
| MSPM0L1304xRGE | 16 / 2 | | | | | | | | | | |
| MSPM0L1303xRGE | 8 / 2 | | | | | | | | | | |
| MSPM0L1306xDGS20 | 64 / 4 | T/S | 8 | 1 | 2 | 1 | 2 / 2 / 1 | 4 | 17 | 2 | 20 VSSOP [5.1 mm × 4.9 mm] |
| MSPM0L1305xDGS20 | 32 / 4 | | | | | | | | | | |
| MSPM0L1304xDGS20 | 16 / 2 | | | | | | | | | | |
| MSPM0L1344xDGS20 | 16 / 2 | T | 7 | | | | | | 15 | | |
| MSPM0L1343xDGS20 | 8 / 2 | | | | | | | | | | |
| MSPM0L1306xRTR | 64 / 4 | T/S | 6 | 1 | 2 | 1 | 2 / 2 / 1 | 4 | 13 | 2 | 16 WQFN [3 mm × 2 mm] |
| MSPM0L1305xRTR | 32 / 4 | | | | | | | | | | |
| MSPM0L1304xRTR | 16 / 2 | | | | | | | | | | |
| MSPM0L1306xDYY | 64 / 4 | T/S | 6 | 1 | 2 | 1 | 2 / 2 / 1 | 4 | 13 | 2 | 16 SOT [4.2 mm × 2 mm] |
| MSPM0L1305xDYY | 32 / 4 | | | | | | | | | | |
| MSPM0L1304xDYY | 16 / 2 | | | | | | | | | | |

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in [Section 12](#), or see the [TI website](#).

(2) For more information about the device name, see [Section 10.1](#).

(3) Device qualifications:

- T = -40°C to 105°C
- S = -40°C to 125°C

(4) The package size (length × width) is a nominal value and includes pins, where applicable. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 12](#).

6 Pin Configuration and Functions

6.1 Pin Diagrams

- Power
- Reset
- High-Speed I/O (HSIO)
- 5-V Tolerant Open-Drain I/O (ODIO)

Figure 6-1. Pin Diagram Color Coding

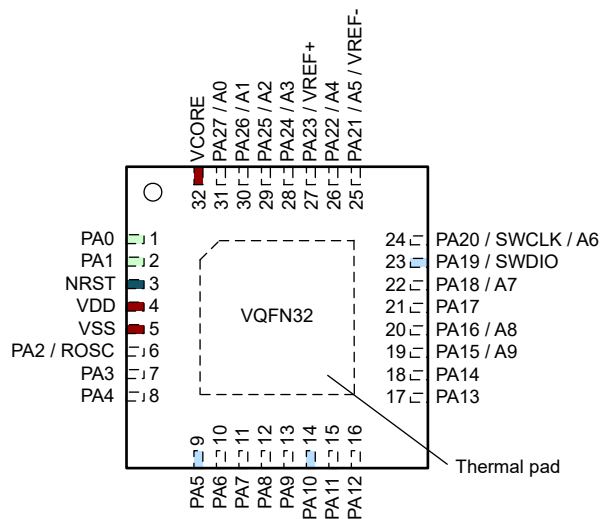


Figure 6-2. 32-Pin RHB (VQFN) (Top View) - MSPM0L130x

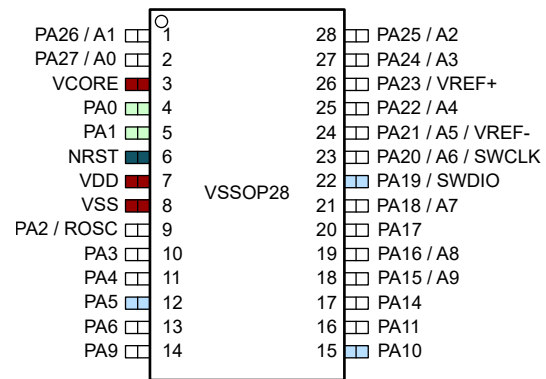


Figure 6-3. 28-Pin DGS28 (VSSOP) (Top View) - MSPM0L130x

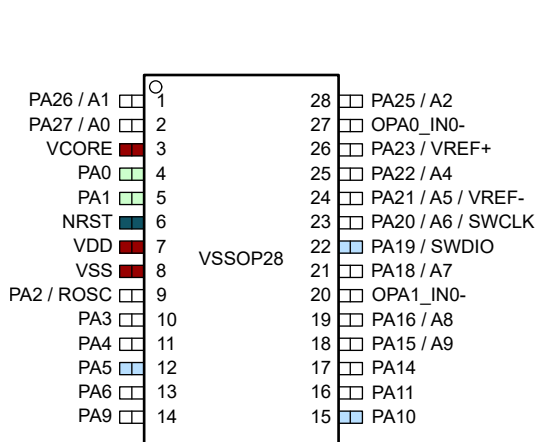


Figure 6-4. 28-Pin DGS28 (VSSOP) (Top View) - MSPM0L134x

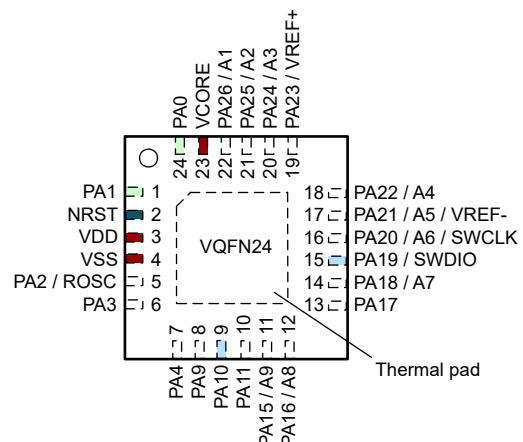


Figure 6-5. 24-Pin RGE (VQFN) (Top View) - MSPM0L130x

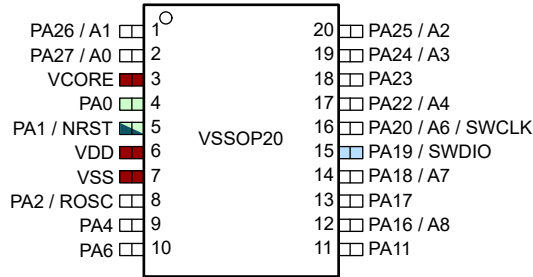


Figure 6-6. 20-Pin DGS20 (VSSOP) (Top View) - MSPM0L130x

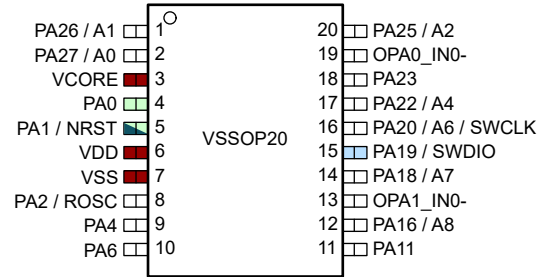


Figure 6-7. 20-Pin DGS20 (VSSOP) (Top View) - MSPM0L134x

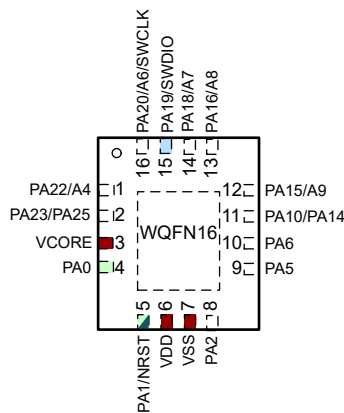


Figure 6-8. 16-Pin RTR (WQFN) (Top View) - MSPM0L130x

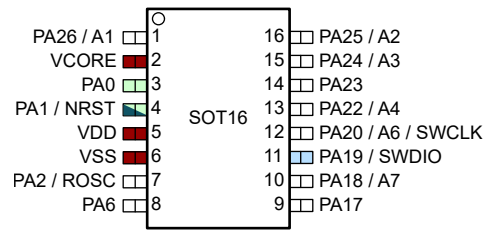


Figure 6-9. 16-Pin DYY (SOT) (Top View) - MSPM0L130x

6.2 Pin Attributes

The following table describes the functions available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which allows users to configure the desired *Pin Function* using the PINCM.PF control bits.

Table 6-1. Pin Attributes

| PINCMx | PIN NAME | PIN FUNCTION | | PIN NUMBER | | | | | | | I/O STRUCTURE |
|--------|----------|--------------|--|------------|-------------------------|-------------------------|---------|----------|---------|--------|-------------------------|
| | | ANALOG | DIGITAL ⁽¹⁾ | 32 VQFN | 28 VSSOP ⁽²⁾ | 28 VSSOP ⁽³⁾ | 24 VQFN | 20 VSSOP | 16 WQFN | 16 SOT | |
| N/A | N/A | VDD | | 4 | 7 | 7 | 3 | 6 | 6 | 5 | Power |
| N/A | N/A | VSS | | 5 | 8 | 8 | 4 | 7 | 7 | 6 | Power |
| N/A | N/A | VCORE | | 32 | 3 | 3 | 23 | 3 | 3 | 2 | Power |
| 1 | PA0 | | UART1_TX [2] / I2C0_SDA [3] / TIMG1_C0 [4] / SPI0_CS1 [5](Default BSL I2C_SDA) | 1 | 4 | 4 | 24 | 4 | 4 | 3 | 5-V tolerant Open-Drain |

Table 6-1. Pin Attributes (continued)

| PINCM x | PIN NAME | PIN FUNCTION | | PIN NUMBER | | | | | | | I/O STRUCT URE |
|------------|-------------|----------------------------|---|------------|-------------------------|-------------------------|---------|-------------------|---------|--------|-------------------------|
| | | ANALOG | DIGITAL ⁽¹⁾ | 32 VQFN | 28 VSSOP ⁽²⁾ | 28 VSSOP ⁽³⁾ | 24 VQFN | 20 VSSOP | 16 WQFN | 16 SOT | |
| 2 | PA1 | | UART1_RX [2] / I2C0_SCL [3] / TIMG1_C1 [4](Default BSL I2C_SCL) | 2 | 5 | 5 | 1 | 5 | 5 | 4 | 5-V tolerant Open-Drain |
| N/A | N/A | NRST | | 3 | 6 | 6 | 2 | | | | Reset ⁽⁴⁾ |
| 3 | PA2 | ROSC | TIMG1_C1 [2] / SPI0_CS0 [3] | 6 | 9 | 9 | 5 | 8 | 8 | 7 | Standard |
| 4 | PA3 | | TIMG2_C0 [2] / SPI0_CS1 [3] / UART1_CTS [4] / COMP0_OUT [5] | 7 | 10 | 10 | 6 | – | – | – | Standard |
| 5 | PA4 | | TIMG2_C1 [2] / SPI0_POCI [3] / UART1_RTS [4] | 8 | 11 | 11 | 7 | 9 | – | – | Standard |
| 6 | PA5 | | TIMG0_C0 [2] / SPI0_PICO [3]/FCC_IN[4] | 9 | 12 | 12 | – | – | 9 | – | High-Speed |
| 7 | PA6 | | TIMG0_C1 [2] / SPI0_SCK [3] | 10 | 13 | 13 | – | 10 | 10 | 8 | Standard |
| 8 | PA7 | | COMP0_OUT [2] / CLK_OUT [3] / TIMG1_C0 [4] | 11 | – | – | – | – | – | – | Standard |
| 9 | PA8 | | UART0_TX [2] / SPI0_CS0 [3] / UART1_RTS [4] / TIMG2_C0 [5] | 12 | – | – | – | – | – | – | Standard |
| 10 | PA9 | | UART0_RX [2] / SPI0_PICO [3] / UART1_CTS [4] / TIMG2_C1 [5]/CLK_OUT[6] | 13 | 14 | 14 | 8 | – | – | – | Standard |
| 11 | PA10 | | UART1_TX [2] / SPI0_POCI [3] / I2C0_SDA [4] / TIMG4_C0 [5]/CLK_OUT[6] | 14 | 15 | 15 | 9 | – | 11 | – | High-Speed |
| 12 | PA11 | | UART1_RX [2] / SPI0_SCK [3] / I2C0_SCL [4] / TIMG4_C1 [5] / COMP0_OUT [6] | 15 | 16 | 16 | 10 | 11 | – | – | Standard |
| 13 | PA12 | | UART0_CTS [2] / TIMG0_C0 [3]/FCC_IN[4] | 16 | – | – | – | – | – | – | Standard |
| 14 | PA13 | | UART0_RTS [2] / TIMG0_C1 [3] / UART1_RX [4] | 17 | – | – | – | – | – | – | Standard |
| 15 | PA14 | | UART1_CTS [2] / CLK_OUT [3] / UART1_TX [4] / TIMG1_C0 [5] | 18 | 17 | 17 | – | – | – | – | Standard |
| 16 | PA15 | A9 | UART1_RTS [2] / I2C1_SCL [3] / SPI0_CS2 [4] / TIMG4_C1 [5] | 19 | 18 | 18 | 11 | – | 12 | – | Standard |
| 17 | PA16 | A8 / OPA1_OUT | COMP0_OUT [2] / I2C1_SDA [3] / SPI0_POCI [4] / TIMG0_C0 [5]/FCC_IN[6] | 20 | 19 | 19 | 12 | 12 | 13 | – | Standard |
| 18 | PA17 | OPA1_IN1- | UART0_TX [2] / I2C1_SCL [3] / SPI0_SCK [4] / TIMG4_C0 [5] / SPI0_CS1 [6] | 21 | 20 | – | 13 | 13 ⁽²⁾ | – | 9 | Standard with wake |
| | N/A | OPA1_IN0- | | | | | | | | | |
| N/A | N/A | OPA1_IN0- | | – | – | 20 | – | 13 ⁽³⁾ | – | – | Analog |
| 19 | PA18 | A7 / OPA1_IN0+ / GPAMP_IN- | UART0_RX [2] / SPI0_PICO [3] / I2C1_SDA [4] / TIMG4_C1 [5](BSL Invoke) | 22 | 21 | 21 | 14 | 14 | 14 | 10 | Standard with wake |
| 20 | PA19 | | SWDIO [2] / I2C1_SDA [3] / SPI0_POCI [4] | 23 | 22 | 22 | 15 | 15 | | | |
| 21 | PA20 | A6 / COMP0_IN1+ | SWCLK [2] / I2C1_SCL [3] / TIMG4_C0 [4] | 24 | 23 | 23 | 16 | 16 | 16 | 12 | Standard |
| 22 | PA21 | A5 / VREF- | TIMG2_C0 [2] / UART0_CTS [3] / UART0_TX [4] | 25 | 24 | 24 | 17 | – | – | – | Standard |
| 23 | PA22 | A4 / GPAMP_OUT / OPA0_OUT | UART0_RX [2] / TIMG2_C1 [3] / UART0_RTS [4] / CLK_OUT [5] / UART1_RX [6](Default BSL UART_RX) | 26 | 25 | 25 | 18 | 17 | 1 | 13 | Standard |

Table 6-1. Pin Attributes (continued)

| PINCM x | PIN NAME | PIN FUNCTION | | PIN NUMBER | | | | | | I/O STRUCTURE | |
|------------|-------------|-----------------------------------|--|------------|-------------------------|-------------------------|---------|-------------------|---------|------------------|----------|
| | | ANALOG | DIGITAL ⁽¹⁾ | 32 VQFN | 28 VSSOP ⁽²⁾ | 28 VSSOP ⁽³⁾ | 24 VQFN | 20 VSSOP | 16 WQFN | | 16 SOT |
| 24 | PA23 | VREF+ / COMP0_IN1- | UART0_TX [2] / SPI0_CS3 [3] / TIMG0_C0 [4] / UART0_CTS [5] / UART1_TX [6](Default BSL UART_TX) | 27 | 26 | 26 | 19 | 18 | 2 | 14 | Standard |
| 25 | PA24 | A3 / OPA0_IN1- / OPA0_IN0- | SPI0_CS2 [2] / TIMG0_C1 [3] / UART0_RTS [4] | 28 | 27 | – | 20 | 19 ⁽²⁾ | – | 15 | Standard |
| N/A | N/A | OPA0_IN0- | | – | – | 27 | – | 19 ⁽³⁾ | – | – | Analog |
| 26 | PA25 | A2 / OPA0_IN0+ | TIMG4_C1 [2] / UART0_TX [3] / SPI0_PICO [4] | 29 | 28 | 28 | 21 | 20 | 2 | 16 | Standard |
| 27 | PA26 | A1 / GPAMP_IN+ / COMP0_IN0+ | TIMG1_C0 [2] / UART0_RX [3] / SPI0_POCI [4] | 30 | 1 | 1 | 22 | 1 | – | 1 | Standard |
| 28 | PA27 | A0 / COMP0_IN0- | TIMG1_C1 [2] / SPI0_CS3 [3] | 31 | 2 | 2 | – | 2 | – | – | Standard |

- (1) PINCM.PF and PINCM.PC in [IOMUX](#) must be set to 0 for analog functions (for example, OPA inputs or outputs or COMP inputs). Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which lets software configure the desired *Pin Function* using the PINCM.PF control bits.
- (2) MSPM0L130x only
- (3) MSPM0L134x only
- (4) Reset PIN is muxed with PA1 for 16-pin and 20-pin devices.

Table 6-2. Digital IO Features by IO Type

| IO STRUCTURE | INVERSION CONTROL | DRIVE STRENGTH CONTROL | HYSTERESIS CONTROL | PULLUP RESISTOR | PULLDOWN RESISTOR | WAKEUP LOGIC |
|--------------------------|-------------------|------------------------|--------------------|-----------------|-------------------|--------------|
| Standard drive | Y | | | Y | Y | |
| Standard drive with wake | Y | | | Y | Y | Y |
| High speed | Y | Y | | Y | Y | |
| 5-V tolerant open drain | Y | | Y | | Y | Y |

6.3 Signal Descriptions

Table 6-3. Signal Descriptions

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|---------------------------|-------------|------------------------|-------------------------|-------------------------|---------|-------------------|---------|--------|-------------------------|--|
| | | 32 VQFN | 28 VSSOP ⁽³⁾ | 28 VSSOP ⁽⁴⁾ | 24 VQFN | 20 VSSOP | 16 WQFN | 16 SOT | | |
| ADC | A0 | 31 | 2 | 2 | – | 2 | – | – | I | ADC0 analog input 0 |
| | A1 | 30 | 1 | 1 | 22 | 1 | – | 1 | I | ADC0 analog input 1 |
| | A2 | 29 | 28 | 28 | 21 | 20 | 2 | 16 | I | ADC0 analog input 2 |
| | A3 | 28 | 27 | – | 20 | 19 ⁽³⁾ | – | 15 | I | ADC0 analog input 3 |
| | A4 | 26 | 25 | 25 | 18 | 17 | 1 | 13 | I | ADC0 analog input 4 |
| | A5 | 25 | 24 | 24 | 17 | – | – | – | I | ADC0 analog input 5 |
| | A6 | 24 | 23 | 23 | 16 | 16 | 16 | 12 | I | ADC0 analog input 6 |
| | A7 | 22 | 21 | 21 | 14 | 14 | 14 | 10 | I | ADC0 analog input 7 |
| | A8 | 20 | 19 | 18 | 12 | 12 | 13 | – | I | ADC0 analog input 8 |
| | A9 | 19 | 18 | 17 | 11 | – | 12 | – | I | ADC0 analog input 9 |
| BSL | BSL_invoke | 22 | 21 | 21 | 14 | 14 | 14 | 10 | I | Input pin used to invoke bootloader |
| BSL (I ² C) | BSLSCL | 2 | 5 | 5 | 1 | 5 | 5 | 4 | I/O | Default I ² C BSL clock |
| | BSLSDA | 1 | 4 | 4 | 24 | 4 | 4 | 3 | I/O | Default I ² C BSL data |
| BSL (UART) | BSLRX | 26 | 25 | 25 | 18 | 17 | 1 | 13 | I | Default UART BSL receive |
| | BSLTX | 27 | 26 | 26 | 19 | 18 | 2 | 14 | O | Default UART BSL transmit |
| Clock | CLK_OUT | 11 18 26 | 17 25 | 16 25 | 18 | 17 | 1 11 | 13 | O | Configurable clock output |
| | ROSC | 6 | 9 | 9 | 5 | 8 | 8 | 7 | I | External resistor used for improving oscillator accuracy |
| Comparator | COMP0_IN0- | 31 | 2 | 2 | – | 2 | – | – | I | Comparator 0 inverting input 0 |
| | COMP0_IN0+ | 30 | 1 | 1 | 22 | 1 | – | 1 | I | Comparator 0 non-inverting input 0 |
| | COMP0_IN1- | 27 | 26 | 26 | 19 | 18 | 2 | 14 | I | Comparator 0 inverting input 1 |
| | COMP0_IN1+ | 24 | 23 | 23 | 16 | 16 | 16 | 12 | I | Comparator 0 non-inverting input 1 |
| | COMP0_OUT | 7 11 15 20 | 10 16 18 | 10 18 | 6 12 | 11 12 | 13 | – | O | Comparator 0 output |
| Debug | SWCLK | 24 | 23 | 23 | 16 | 16 | 16 | 12 | I | Serial wire debug input clock |
| | SWDIO | 23 | 22 | 22 | 15 | 15 | 15 | 11 | I/O | Serial wire debug data input/output |
| General-Purpose Amplifier | GPAMP_IN+ | 30 | 1 | 1 | 22 | 1 | – | 1 | I | GPAMP non-inverting terminal input |
| | GPAMP_OUT | 26 | 25 | 25 | 18 | 17 | 1 | 13 | O | GPAMP output |
| | GPAMP_IN- | 22 | 21 | 21 | 14 | 14 | 14 | 10 | I | GPAMP inverting terminal input |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|------------------|-------------|------------------------|-------------------------|-------------------------|----------------|----------------------------|----------------|----------|-----------------------------|--|
| | | 32 VQFN | 28 VSSOP ⁽³⁾ | 28 VSSOP ⁽⁴⁾ | 24 VQFN | 20 VSSOP | 16 WQFN | 16 SOT | | |
| GPIO | PA0 | 1 | 4 | 4 | 24 | 4 | 4 | 3 | I/O | General-purpose digital I/O with wake up from SHUTDOWN |
| | PA1 | 2 | 5 | 5 | 1 | 5 | 5 | 4 | I/O | General-purpose digital I/O with wake up from SHUTDOWN |
| | PA2 | 6 | 9 | 9 | 5 | 8 | 8 | 7 | I/O | General-purpose digital I/O |
| | PA3 | 7 | 10 | 10 | 6 | – | – | – | I/O | General-purpose digital I/O |
| | PA4 | 8 | 11 | 11 | 7 | 9 | – | – | I/O | General-purpose digital I/O |
| | PA5 | 9 | 12 | 12 | – | – | 9 | – | I/O | General-purpose digital I/O |
| | PA6 | 10 | 13 | 13 | – | 10 | 10 | 8 | I/O | General-purpose digital I/O |
| | PA7 | 11 | – | – | – | – | – | – | I/O | General-purpose digital I/O |
| | PA8 | 12 | – | – | – | – | – | – | I/O | General-purpose digital I/O |
| | PA9 | 13 | 14 | 14 | 8 | – | – | – | I/O | General-purpose digital I/O |
| | PA10 | 14 | 15 | – | 9 | – | 11 | – | I/O | General-purpose digital I/O |
| | PA11 | 15 | 16 | – | 10 | 11 | – | – | I/O | General-purpose digital I/O |
| | PA12 | 16 | – | – | – | – | – | – | I/O | General-purpose digital I/O |
| | PA13 | 17 | – | 15 | – | – | – | – | I/O | General-purpose digital I/O |
| | PA14 | 18 | 17 | 16 | – | – | 11 | – | I/O | General-purpose digital I/O |
| | PA15 | 19 | 18 | 17 | 11 | – | 12 | – | I/O | General-purpose digital I/O |
| | PA16 | 20 | 19 | 18 | 12 | 12 | 13 | – | I/O | General-purpose digital I/O |
| | PA17 | 21 | 20 | 19 | 13 | 13 ⁽³⁾ | 14 | 9 | I/O | General-purpose digital I/O with wake up from SHUTDOWN |
| | PA18 | 22 | 21 | 21 | 14 | 14 | 14 | 10 | I/O | General-purpose digital I/O with wake up from SHUTDOWN |
| | PA19 | 23 | 22 | 22 | 15 | 15 | 15 | 11 | I/O | General-purpose digital I/O |
| | PA20 | 24 | 23 | 23 | 16 | 16 | 16 | 12 | I/O | General-purpose digital I/O |
| | PA21 | 25 | 24 | 24 | 17 | – | – | – | I/O | General-purpose digital I/O |
| | PA22 | 26 | 25 | 25 | 18 | 17 | 1 | 13 | I/O | General-purpose digital I/O |
| | PA23 | 27 | 26 | 26 | 19 | 18 | 2 | 14 | I/O | General-purpose digital I/O |
| | PA24 | 28 | 27 | – | 20 | 19 ⁽³⁾ | – | 15 | I/O | General-purpose digital I/O |
| | PA25 | 29 | 28 | 28 | 21 | 20 | 2 | 16 | I/O | General-purpose digital I/O |
| | PA26 | 30 | 1 | 1 | 22 | 1 | – | 1 | I/O | General-purpose digital I/O |
| PA27 | 31 | 2 | 2 | – | 2 | – | – | I/O | General-purpose digital I/O | |
| I ² C | I2C0_SCL | 2 15 | 5 16 | 5 | 1 10 | 5 11 | 5 | 4 | I/O | I2C0 serial clock |
| | I2C0_SDA | 1 14 | 4 15 | 4 | 24 9 | 4 | 4 11 | 3 | I/O | I2C0 serial data |
| | I2C1_SCL | 19 21 24 | 18 20 23 | 17 19 23 | 11 13 16 | 13 ⁽³⁾ 16 | 12 16 | 9 12 | I/O | I2C1 serial clock |
| | I2C1_SDA | 20 22 23 | 19 21 22 | 18 21 22 | 12 14 15 | 12 14 15 | 13 14 15 | 10 11 | I/O | I2C1 serial data |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|---|-------------|---------------------------|---------------------------|-------------------------|--------------------------|----------------------------------|----------------|----------|-------------------------|--|
| | | 32 VQFN | 28 VSSOP ⁽³⁾ | 28 VSSOP ⁽⁴⁾ | 24 VQFN | 20 VSSOP | 16 WQFN | 16 SOT | | |
| Operational Amplifier with Chopping (Zero-Drift Op-Amp) | OPA0_IN0+ | 29 | 28 | 28 | 21 | 20 | 2 | 16 | I | OPA0 non-inverting terminal input 0 |
| | OPA0_IN0- | 28 | 27 | 27 | 20 | 19 | – | 15 | I | OPA0 inverting terminal input 0 |
| | OPA0_IN1- | 28 | 27 | – | 20 | 19 ⁽³⁾ | – | 15 | I | OPA0 inverting terminal input 1 |
| | OPA0_OUT | 26 | 25 | 25 | 18 | 17 | 1 | 13 | O | OPA0 output |
| | OPA1_IN0+ | 22 | 21 | 21 | 14 | 14 | 14 | 10 | I | OPA1 non-inverting terminal input 0 |
| | OPA1_IN0- | 21 | 20 | 20 | 13 | 13 | 14 | 9 | I | OPA1 inverting terminal input 0 |
| | OPA1_IN1- | 21 | 20 | 19 | 13 | 13 ⁽³⁾ | – | 9 | I | OPA1 inverting terminal input 1 |
| | OPA1_OUT | 20 | 19 | 18 | 12 | 12 | 13 | – | O | OPA1 output |
| Power | VSS | 5 | 8 | 8 | 4 | 7 | 7 | 6 | P | Ground supply |
| | VDD | 4 | 7 | 7 | 3 | 6 | 6 | 5 | P | Power supply |
| | VCORE | 32 | 3 | 3 | 23 | 3 | 3 | 2 | P | Regulated core power supply output |
| | QFN Pad | Pad | – | – | Pad | – | Pad | – | P | QFN package exposed thermal pad. TI recommends connection to V _{SS} . |
| SPI | SPI0_CS0 | 6 12 | 9 | 9 | 5 | 8 | 8 | 7 | I/O | SPI0 chip-select 0 |
| | SPI0_CS1 | 1 7 21 | 4 10 20 | 4 10 19 | 6 13 24 | 4 13 ⁽³⁾ | 4 | 3 9 | I/O | SPI0 chip-select 1 |
| | SPI0_CS2 | 19 28 | 18 27 | 17 | 11 20 | 19 ⁽³⁾ | 12 | 15 | I/O | SPI0 chip-select 2 |
| | SPI0_CS3 | 27 31 | 2 26 | 2 26 | 19 | 2 18 | 2 | 14 | I/O | SPI0 chip-select 3 |
| | SPI0_SCK | 10 15 21 | 13 16 20 | 13 19 | 10 13 | 10 11 13 ⁽³⁾ | 10 | 8 9 | I/O | SPI0 clock signal input – SPI peripheral mode Clock signal output – SPI controller mode |
| | SPI0_POCI | 8 14 20 23 30 | 1 11 15 19 22 | 1 11 18 22 | 7 9 12 15 22 | 1 9 12 15 | 11 13 15 | 1 11 | I/O | SPI0 controller in/peripheral out |
| | SPI0_PICO | 9 13 22 29 | 12 14 21 28 | 12 14 21 28 | 8 14 21 | 14 20 | 2 9 14 | 10 16 | I/O | SPI0 controller out/peripheral in |
| System | NRST | 3 | 6 | 6 | 2 | 5 | 5 | 4 | I | Reset input active low |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|----------|-------------|------------------------|-------------------------|-------------------------|----------------------|----------------------------|---------------|----------|-------------------------|---|
| | | 32 VQFN | 28 VSSOP ⁽³⁾ | 28 VSSOP ⁽⁴⁾ | 24 VQFN | 20 VSSOP | 16 WQFN | 16 SOT | | |
| Timer | TIMG0_C0 | 9 16 20 27 | 12 19 26 | 12 18 26 | 12 19 | 12 18 | 2 9 13 | 14 | I/O | General purpose timer 0 CCR0 capture input/ compare output |
| | TIMG0_C1 | 10 17 28 | 13 27 | 13 15 | 20 | 10 19 ⁽³⁾ | 10 | 8 15 | I/O | General purpose timer 0 CCR1 capture input/ compare output |
| | TIMG1_C0 | 1 11 18 30 | 1 4 17 | 1 4 16 | 22 24 | 1 4 | 4 11 | 1 3 | I/O | General purpose timer 1 CCR0 capture input/ compare output |
| | TIMG1_C1 | 2 6 31 | 2 5 9 | 2 5 9 | 1 5 | 2 5 8 | 5 8 | 4 7 | I/O | General purpose timer 1 CCR1 capture input/ compare output |
| | TIMG2_C0 | 7 12 25 | 10 24 | 10 24 | 6 17 | – | – | – | I/O | General purpose timer 2 CCR0 capture input/ compare output |
| | TIMG2_C1 | 8 13 26 | 11 14 25 | 11 14 25 | 7 8 18 | 9 17 | 1 | 13 | I/O | General purpose timer 2 CCR1 capture input/ compare output |
| | TIMG4_C0 | 14 21 24 | 15 20 23 | 19 23 | 9 13 16 | 13 ⁽³⁾ 16 | 11 16 | 9 12 | I/O | General purpose timer 4 CCR0 capture input/ compare output |
| | TIMG4_C1 | 15 19 22 29 | 16 18 21 28 | 17 21 28 | 10 11 14 21 | 11 11 14 20 | 2 12 14 | 10 16 | I/O | General purpose timer 4 CCR1 capture input/ compare output |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|----------------------------------|-------------|----------------------------|-------------------------|-------------------------|----------------------|----------------------------------|--------------|---------------|-------------------------|--|
| | | 32 VQFN | 28 VSSOP ⁽³⁾ | 28 VSSOP ⁽⁴⁾ | 24 VQFN | 20 VSSOP | 16 WQFN | 16 SOT | | |
| UART | UART0_TX | 12 21 25 27 29 | 20 24 26 28 | 19 24 26 28 | 13 17 19 21 | 13 ⁽³⁾ 18 20 | 2 | 9 14 16 | O | UART0 transmit data |
| | UART0_RX | 13 22 26 30 | 1 14 21 25 | 1 14 21 25 | 8 14 18 22 | 1 14 17 | 1 14 | 1 10 13 | I | UART0 receive data |
| | UART0_CTS | 16 25 27 | 24 26 | 24 26 | 17 19 | 18 | 2 | 14 | I | UART0 "clear to send" flow control input |
| | UART0_RTS | 17 26 28 | 25 27 | 15 25 | 18 20 | 17 19 ⁽³⁾ | 1 | 13 15 | O | UART0 "request to send" flow control output |
| | UART1_TX | 1 14 18 27 | 4 15 17 26 | 4 16 26 | 9 19 24 | 4 18 | 2 4 11 | 3 14 | O | UART1 transmit data |
| | UART1_RX | 2 15 17 26 | 5 16 25 | 5 15 25 | 1 10 18 | 5 11 17 | 1 5 | 4 13 | I | UART1 receive data |
| | UART1_CTS | 7 13 18 | 10 14 17 | 10 14 16 | 6 8 | – | 11 | – | I | UART1 "clear to send" flow control input |
| | UART1_RTS | 8 12 19 | 11 18 | 11 17 | 7 11 | 9 | 12 | – | O | UART1 "request to send" flow control output |
| Voltage Reference ⁽⁵⁾ | VREF+ | 27 | 26 | 26 | 19 | 18 | 2 | 14 | I | Voltage reference power supply - external reference input |
| | VREF- | 25 | 24 | 24 | 17 | – | – | – | I | Voltage reference ground supply - external reference input |

- (1) – = not available
- (2) I = input, O = output, I/O = input or output, P = power
- (3) MSPM0L130x only
- (4) MSPM0L134x only
- (5) When using VREF+ and VREF- to bring in an external voltage reference for analog peripherals such as the ADC, a decoupling capacitor must be placed on VREF+ to VREF-/GND with a capacitance based on the external reference source

6.4 Connections for Unused Pins

Table 6-4 lists the correct termination of unused pins.

Table 6-4. Connection of Unused Pins

| PIN ⁽¹⁾ | POTENTIAL | COMMENT |
|------------------------|-----------|---|
| PAx | Open | Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup or pulldown resistor. |
| OPA _x _IN0- | Open | This pin is high-impedance |

Table 6-4. Connection of Unused Pins (continued)

| PIN ⁽¹⁾ | POTENTIAL | COMMENT |
|--------------------|-----------|--|
| NRST | VCC | NRST is an active-low reset signal; the pin must be pulled high to VCC or the device cannot start. For more information, see Section 9.1 . |

(1) Any unused pin with a function that is shared with general-purpose I/O must follow the "PAX" unused pin connection guidelines.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------------|------------------------------------|---|------|------------------------------------|------|
| VDD | Supply voltage | At VDD pin, with respect to VSS | -0.3 | 4.1 | V |
| V _I | Input voltage | Applied to any 5-V tolerant open-drain pins | -0.3 | 5.5 | V |
| V _I | Input voltage | Applied to any common tolerance pins | -0.3 | V _{DD} + 0.3 (4.1 MAX) | V |
| I _{VDD} | Current into VDD pin (source) | -40°C ≤ T _j ≤ 130°C | | 80 | mA |
| | | -40°C ≤ T _j ≤ 85°C | | 100 | mA |
| I _{VSS} | Current out of VSS pin (sink) | -40°C ≤ T _j ≤ 130°C | | 80 | mA |
| | | -40°C ≤ T _j ≤ 85°C | | 100 | mA |
| I _{IO} | Current for SDIO pin | Current sunk or sourced by SDIO pin | | 6 | mA |
| | Current for HSIO pin | Current sunk or sourced by HSIO pin | | 6 | mA |
| | Current for ODIO pin | Current sunk by ODIO pin | | 20 | mA |
| I _D | Supported diode current | Diode current at any device pin | | ±2 | mA |
| T _j | Junction temperature | | -40 | 130 | °C |
| T _{stg} | Storage temperature ⁽²⁾ | | -40 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Higher temperatures may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

7.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--------------------|--|---------------------|------|-----|------|
| VDD | Supply voltage ⁽⁴⁾ | 1.62 ⁽⁵⁾ | | 3.6 | V |
| VCORE | Voltage on VCORE pin ⁽²⁾ | | 1.35 | | V |
| C _{VDD} | Capacitor placed between VDD and VSS ⁽¹⁾ | | 10 | | uF |
| C _{VCORE} | Capacitor placed between VCORE and VSS ^{(1) (2)} | | 470 | | nF |
| T _A | Ambient temperature, T version | -40 | | 105 | °C |
| | Ambient temperature, S version | -40 | | 125 | |
| T _J | Max junction temperature, T version | | | 125 | °C |
| T _J | Max junction temperature, S version | | | 130 | °C |
| f _{MCLK} | MCLK, CPUCLK, ULPCLK frequency with 1 flash wait state ⁽³⁾ | | | 32 | MHz |
| | MCLK, CPUCLK, ULPCLK frequency with 0 flash wait states ⁽³⁾ | | | 24 | |

- (1) Connect C_{VDD} and C_{VCORE} between VDD/VSS and VCORE/VSS, respectively, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD} and C_{VCORE}.

- (2) The V_{CORE} pin must only be connected to C_{V_{CORE}}. Do not supply any voltage or apply any external load to the V_{CORE} pin.
- (3) Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software.
- (4) There is no dependency on MCLK frequency with respect to V_{DD} recommended operating range.
- (5) Functionality is guaranteed down to V_{BOR0-(min)}.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | PACKAGE | VALUE | UNIT |
|-------------------------------|--|------------------|-------|------|
| R _{θJA} | Junction-to-ambient thermal resistance | VQFN-32 (RHB) | 36.3 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | | 28.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | | 17.2 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | | 0.8 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | | 17.2 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | | 6.9 | °C/W |
| R _{θJA} | Junction-to-ambient thermal resistance | VSSOP-28 (DGS28) | 78.9 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | | 38.6 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | | 41.3 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | | 3.4 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | | 41.0 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | | N/A | °C/W |
| R _{θJA} | Junction-to-ambient thermal resistance | VQFN-24 (RGE) | 44.7 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | | 38.1 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | | 21.9 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | | 1.1 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | | 21.9 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | | 7.1 | °C/W |
| R _{θJA} | Junction-to-ambient thermal resistance | VSSOP-20 (DGS20) | 91.3 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | | 29.3 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | | 48.3 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | | 0.7 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | | 47.9 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | | N/A | °C/W |
| R _{θJA} | Junction-to-ambient thermal resistance | WQFN-16 (RTR) | 100.1 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | | 43.2 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | | 47.4 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | | 2.1 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | | 47.2 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | | N/A | °C/W |
| R _{θJA} | Junction-to-ambient thermal resistance | SOT-16 (DYY) | 86.6 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | | 39.3 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | | 27.8 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | | 1.1 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | | 27.8 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Supply Current Characteristics

7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

| PARAMETER | | MCLK | -40°C | | 25°C | | 85°C | | 105°C | | 125°C | | UNIT |
|------------------------------|---|-------|-------|------|------|------|------|------|-------|------|-------|------|--------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| RUN Mode | | | | | | | | | | | | | |
| IDD _{RUN} | MCLK=SYSOSC, CoreMark, execute from flash | 32MHz | 2.3 | | 2.3 | | 2.3 | | 2.3 | | 2.4 | | mA |
| | | 4MHz | 0.52 | | 0.52 | | 0.54 | | 0.56 | | 0.60 | | |
| IDD _{RUN} , per MHz | MCLK=SYSOSC, While(1), execute from flash | 32MHz | 40 | 48 | 40 | 50 | 41 | 50 | 42 | 51 | 43 | 56 | uA/MHz |
| | MCLK=SYSOSC, CoreMark, execute from flash | 32MHz | 72 | | 72 | | 72 | | 73 | | 74 | | |
| | MCLK=SYSOSC, CoreMark, execute from flash | 4MHz | 130 | | 130 | | 135 | | 140 | | 150 | | |
| SLEEP Mode | | | | | | | | | | | | | |
| IDD _{SLEEP} | MCLK=SYSOSC, CPU is halted | 32MHz | 967 | 1047 | 978 | 1066 | 1002 | 1192 | 1024 | 1301 | 1070 | 1416 | uA |
| | | 4MHz | 356 | 416 | 363 | 441 | 389 | 577 | 411 | 689 | 458 | 809 | |

7.5.2 STOP/STANDBY Modes

VDD=3.3V unless otherwise noted. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

| PARAMETER | | ULPCLK | -40°C | | 25°C | | 85°C | | 105°C | | 125°C | | UNIT |
|----------------------|--|--------|-------|-----|------|-----|------|-----|-------|-----|-------|-----|------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| STOP Mode | | | | | | | | | | | | | |
| IDD _{STOP0} | SYSOSC=32MHz, USE4MHZSTOP=0, DISABLESTOP=0 | 4MHz | 316 | 342 | 320 | 344 | 323 | 347 | 327 | 352 | 334 | 361 | uA |
| IDD _{STOP1} | SYSOSC=4MHz, USE4MHZSTOP=1, DISABLESTOP=0 | 4MHz | 146 | 167 | 151 | 171 | 155 | 176 | 158 | 182 | 166 | 192 | |
| IDD _{STOP2} | SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK | 32kHz | 42 | 51 | 44 | 54 | 47 | 58 | 50 | 64 | 56 | 76 | |
| STANDBY Mode | | | | | | | | | | | | | |
| IDD _{STBY0} | STOPCLKSTBY=0, TIMG0 enabled | 32kHz | 1.2 | 1.3 | 1.3 | 1.7 | 2.7 | 6.2 | 4.7 | 12 | 11 | 25 | uA |
| IDD _{STBY1} | STOPCLKSTBY=1, TIMG0 enabled | | 0.9 | 1.0 | 1.0 | 1.4 | 2.4 | 5.9 | 4.4 | 12 | 11 | 25 | |
| | STOPCLKSTBY=1, GPIOA enabled | | 0.9 | 1.0 | 1.0 | 1.4 | 2.4 | 5.9 | 4.4 | 12 | 10 | 25 | |

7.5.3 SHUTDOWN Mode

All inputs tied to 0V or VDD. Outputs do not source or sink any current. Core regulator is powered down.

| PARAMETER | | VDD | -40°C | | 25°C | | 85°C | | 105°C | | 125°C | | UNIT |
|---------------------|---------------------------------|------|-------|-----|------|-----|------|-----|-------|-----|-------|-----|------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| IDD _{SHDN} | Supply current in SHUTDOWN mode | 3.3V | 47 | | 61 | | 352 | | 793 | | 2020 | nA | |

7.6 Power Supply Sequencing

7.6.1 POR and BOR

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|---|------------------------|------|------|------|------|
| dVDD/dt | VDD (supply voltage) slew rate | Rising | | | 1 | V/us |
| | | Falling (2) | | | 0.01 | |
| | | Falling, STANDBY | | | 0.1 | V/ms |
| V _{POR+} | Power-on reset voltage level | Rising (1) | 0.95 | 1.30 | 1.51 | V |
| V _{POR-} | | Falling (1) | 0.9 | 1.25 | 1.48 | V |
| V _{HYS, POR} | POR hysteresis | (1) | 30 | 45 | 60 | mV |
| V _{BOR0+, COLD} | Brown-out reset voltage level 0 (default level) | Cold start, rising (1) | 1.48 | 1.54 | 1.61 | V |
| V _{BOR0+} | | Rising (1) (2) | 1.55 | 1.59 | 1.62 | |
| V _{BOR0-} | | Falling (1) (2) | 1.54 | 1.58 | 1.61 | |
| V _{BOR0, STBY} | | STANDBY mode (1) | 1.51 | 1.57 | 1.61 | |
| V _{BOR1+} | Brown-out-reset voltage level 1 | Rising (1) (2) | 2.13 | 2.18 | 2.23 | V |
| V _{BOR1-} | | Falling (1) (2) | 2.10 | 2.15 | 2.19 | |
| V _{BOR2+} | Brown-out-reset voltage level 2 | Rising (1) (2) | 2.72 | 2.77 | 2.82 | V |
| V _{BOR2-} | | Falling (1) (2) | 2.69 | 2.74 | 2.79 | |
| V _{BOR3+} | Brown-out-reset voltage level 3 | Rising (1) (2) | 2.88 | 2.97 | 3.04 | V |
| V _{BOR3-} | | Falling (1) (2) | 2.85 | 2.94 | 3.01 | |
| V _{HYS, BOR} | Brown-out reset hysteresis | Level 0 (1) | | 15 | 21 | mV |
| | | Levels 1-3 (1) | | 34 | 40 | |
| T _{PD, BOR} | BOR propagation delay | RUN/SLEEP/STOP mode | | | 10 | us |
| | | STANDBY mode | | | 100 | us |

(1) |dVDD/dt| ≤ 3V/s

(2) Device operating in RUN, SLEEP, or STOP mode.

7.6.2 Power Supply Ramp

Figure 7-1 shows the relationships of POR-, POR+, BOR0-, and BOR0+ during powerup and powerdown.

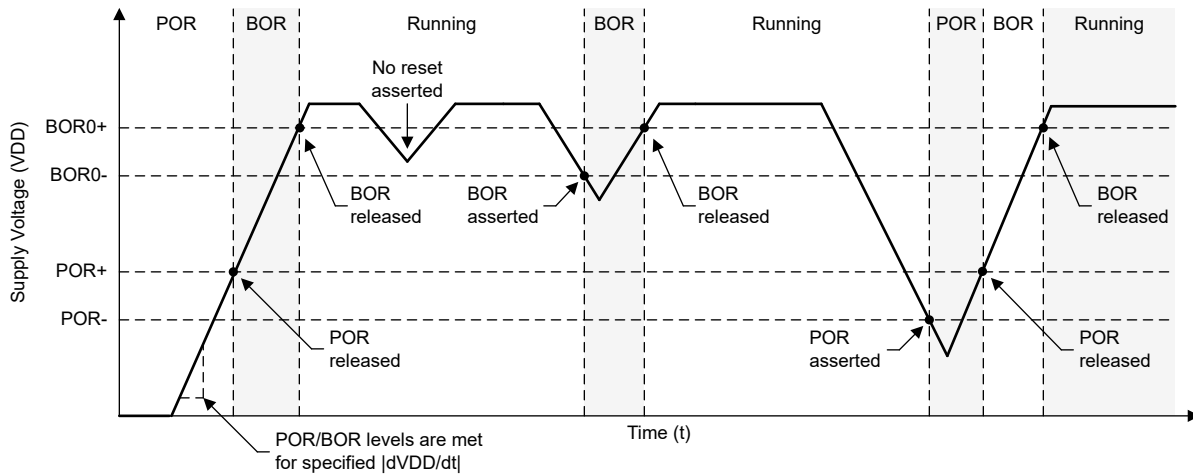


Figure 7-1. Power Cycle POR and BOR Conditions

7.7 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|---|--|------|-----|-----|--------------------|
| Supply | | | | | | |
| VDD _{PGM/ERASE} | Program and erase supply voltage | | 1.62 | | 3.6 | V |
| IDDERASE | Supply current from VDD during erase operation | Supply current delta | | 2 | | mA |
| IDDPGM | Supply current from VDD during program operation | Supply current delta | | 2.5 | | mA |
| Endurance | | | | | | |
| NWEC _(LOWER) | Erase/program cycle endurance (lower 32kB flash) ⁽¹⁾ | | 100 | | | k cycles |
| NWEC _(UPPER) | Erase/program cycle endurance (remaining flash) ⁽¹⁾ | | 10 | | | k cycles |
| NE _(MAX) | Total erase operations before failure ⁽²⁾ | | 802 | | | k erase operations |
| NW _(MAX) | Write operations per word line before sector erase ⁽³⁾ | | | | 83 | write operations |
| Retention | | | | | | |
| t _{RET_85} | Flash memory data retention | -40°C ≤ T _J ≤ 85°C | 60 | | | years |
| t _{RET_105} | Flash memory data retention | -40°C ≤ T _J ≤ 105°C | 11.4 | | | years |
| Program and Erase Timing | | | | | | |
| t _{PROG (WORD, 64)} | Program time for flash word ⁽⁴⁾ ⁽⁶⁾ | | | 50 | 275 | µs |
| t _{PROG (SEC, 64)} | Program time for 1kB sector ⁽⁵⁾ ⁽⁶⁾ | | | 6.4 | | ms |
| t _{ERASE (SEC)} | Sector erase time | ≤2k erase/program cycles, T _J ≥ 25°C | | 4 | 20 | ms |
| t _{ERASE (SEC)} | Sector erase time | ≤10k erase/program cycles, T _J ≥ 25°C | | 20 | 150 | ms |
| t _{ERASE (SEC)} | Sector erase time | ≤10k erase/program cycles | | 20 | 200 | ms |
| t _{ERASE (BANK)} | Bank erase time | ≤10k erase/program cycles | | 22 | 220 | ms |

- (1) The lower 32kB flash address space supports higher erase/program endurance to enable EEPROM emulation applications. On devices with ≤32kB flash memory, the entire flash memory supports NWEC_(LOWER) erase/program cycles.
- (2) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.
- (3) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.
- (4) Program time is defined as the time from when the program command is triggered until the command completion interrupt flag is set in the flash controller.
- (5) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.
- (6) Flash word size is 64 data bits (8 bytes). On devices with ECC, the total flash word size is 72 bits (64 data bits plus 8 ECC bits).

7.8 Timing Characteristics

VDD=3.3V, T_a=25 °C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|--|-----------------|-----|-----|-----|--------|
| Wakeup Timing | | | | | | |
| t _{WAKE, SLEEP} | Wakeup time from SLEEP to RUN ⁽¹⁾ | | | 2 | | cycles |
| t _{WAKE, STOP} | Wakeup time from STOP1 to RUN (SYSOSC enabled) ⁽¹⁾ | | | 14 | | µs |
| | Wakeup time from STOP2 to RUN (SYSOSC disabled) ⁽¹⁾ | | | 13 | | µs |

7.8 Timing Characteristics (continued)

VDD=3.3V, T_a=25 °C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|--------------------|-----|-----|-----|------|
| t _{WAKE, STBY} | Wakeup time from STANDBY to RUN (1) | | | 15 | | us |
| t _{WAKE, SHDN} | Wakeup time from SHUTDOWN to RUN | Fast boot enabled | | 214 | | us |
| t _{WAKE, SHDN} | Wakeup time from SHUTDOWN to RUN | Fast boot disabled | | 230 | | us |
| Asynchronous Fast Clock Request Timing | | | | | | |
| t _{DELAY} | Delay time from edge of asynchronous request to first 32MHz MCLK edge | Mode is SLEEP2 | | 0.9 | | us |
| | | Mode is STOP1 | | 2.4 | | us |
| | | Mode is STOP2 | | 0.9 | | us |
| | | Mode is STANDBY1 | | 3.2 | | us |
| Startup Timing | | | | | | |
| t _{START, RESET} | Device cold start-up time from reset/power-up (2) | Fast boot enabled | | 241 | | us |
| | | Fast boot disabled | | 284 | | us |
| NRST Timing | | | | | | |
| t _{RST, BOOTRST} | Minimum pulse length on NRST pin to generate BOOTRST | ULPCLK≥4MHz | | 2 | | us |
| | | ULPCLK=32kHz | | 100 | | us |
| t _{RST, POR} | Minimum pulse length on NRST pin to generate POR | | | 1 | | s |

- (1) The wake-up time is measured from the edge of an external signal (GPIO wake-up event) to the time that the first CPU instruction is executed, with the GPIO glitch filter disabled (FILTEREN=0x0) and fast wake enabled (FASTWAKEONLY=1)
- (2) The start-up time is measured from the time that VDD crosses VBOR0+ (cold start-up) to the time that the first instruction of the user program is executed.

7.9 Clock Specifications

7.9.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|--|---|------|-------|-----|------|---|
| f _{SYSOSC} | Factory trimmed SYSOSC frequency | SYSOSCCFG.FREQ=00 (BASE) | | 32 | | MHz | |
| | | SYSOSCCFG.FREQ=01 | | 4 | | | |
| | User trimmed SYSOSC frequency | SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=10 | | 24 | | | |
| | | SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=01 | | 16 | | | |
| | SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled and an ideal ROSC resistor is assumed ⁽¹⁾ ⁽²⁾ | SETUSEFCL=1, T _a = 25 °C | | -0.41 | | 0.58 | % |
| | | SETUSEFCL=1, -40 °C ≤ T _a ≤ 85 °C | | -0.80 | | 0.93 | |
| | | SETUSEFCL=1, -40 °C ≤ T _a ≤ 105 °C | | -0.80 | | 1.09 | |
| | | SETUSEFCL=1, -40 °C ≤ T _a ≤ 125 °C | | -0.80 | | 1.30 | |
| | SYSOSC accuracy when frequency correction loop (FCL) is enabled with R _{OSC} resistor put at R _{OSC} pin, for factory trimmed frequencies ⁽¹⁾ | SETUSEFCL=1, T _a = 25 °C, ±0.1% ±25ppm R _{OSC} | | -0.5 | | 0.7 | % |
| | | SETUSEFCL=1, -40 °C ≤ T _a ≤ 85 °C, ±0.1% ±25ppm R _{OSC} | | -1.1 | | 1.2 | |
| SETUSEFCL=1, -40 °C ≤ T _a ≤ 105 °C, ±0.1% ±25ppm R _{OSC} | | | -1.1 | | 1.4 | | |
| SETUSEFCL=1, -40 °C ≤ T _a ≤ 125 °C, ±0.1% ±25ppm R _{OSC} | | | -1.1 | | 1.7 | | |
| SYSOSC accuracy when frequency correction loop (FCL) is disabled, 32MHz | SETUSEFCL=0, SYSOSCCFG.FREQ=00, -40 °C ≤ T _a ≤ 125 °C | | -2.6 | | 1.8 | % | |
| f _{SYSOSC} | SYSOSC accuracy when frequency correction loop (FCL) is disabled, for factory trimmed frequencies, 4MHz | SETUSEFCL=0, SYSOSCCFG.FREQ=01, -40 °C ≤ T _a ≤ 125 °C | | -2.7 | | 2.3 | % |
| R _{OSC} | External resistor put between ROSC pin and VSS ⁽¹⁾ | SETUSEFCL=1 | | 100 | | kΩ | |
| t _{settle, SYSOSC} | Settling time to target accuracy ⁽³⁾ | SETUSEFCL=1, ±0.1% 25ppm R _{OSC} ⁽¹⁾ | | | 30 | us | |
| f _{settle, SYSOSC} | f _{SYSOSC} additional undershoot accuracy during t _{settle} ⁽³⁾ | SETUSEFCL=1, ±0.1% 25ppm R _{OSC} ⁽¹⁾ | | -11 | | % | |

- (1) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an external reference resistor (R_{OSC}) which must be connected between the device ROSC pin and VSS when using the FCL. Accuracies are shown for a ±0.1% ±25ppm R_{OSC}; relaxed tolerance resistors may also be used (with reduced SYSOSC accuracy). See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy for various R_{OSC} accuracies. R_{OSC} does not need to be populated if the FCL is not enabled.
- (2) Represents the device accuracy only. The tolerance and temperature drift of the ROSC resistor used must be combined with this spec to determine final accuracy. Performance for a ±0.1% ±25ppm R_{OSC} is given as a reference point.
- (3) When SYSOSC is waking up (for example, when exiting a low power mode) and FCL is enabled, the SYSOSC will initially undershoot the target frequency f_{SYSOSC} by an additional error of up to f_{settle, SYSOSC} for the time t_{settle, SYSOSC}, after which the target accuracy is achieved.

7.9.2 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--------------------|-----------------|----------------------------------|-----|-------|-----|------|---|
| f _{LFOSC} | LFOSC frequency | | | 32768 | | Hz | |
| | LFOSC accuracy | -40 °C ≤ T _a ≤ 125 °C | | -5 | | 5 | % |
| | | -40 °C ≤ T _a ≤ 85 °C | | -3 | | 3 | % |

7.9.2 Low Frequency Oscillator (LFOSC) (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|---------------------|-----------------|-----|-----|-----|------|
| t_{start} , LFOSC | LFOSC start-up time | | | 1.7 | | ms |

7.10 Digital IO

7.10.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---------------------------|-----------------------------|--|----------|-------------------------|------------|
| V_{IH} | High level input voltage | ODIO ⁽¹⁾ | VDD \geq 1.62V | 0.7*VDD | 5.5 | V |
| | | | VDD \geq 2.7V | 2 | 5.5 | V |
| | | All I/O except ODIO & Reset | VDD \geq 1.62V | 0.7*VDD | VDD+0.3 | V |
| V_{IL} | Low level input voltage | ODIO | VDD \geq 1.62V | -0.3 | 0.3*VDD | V |
| | | | VDD \geq 2.7V | -0.3 | 0.8 | V |
| | | All I/O except ODIO & Reset | VDD \geq 1.62V | -0.3 | 0.3*VDD | V |
| V_{HYS} | Hysteresis | ODIO | | 0.05*VDD | | V |
| | | All I/O except ODIO | | 0.1*VDD | | V |
| I_{Ikg} | High-Z leakage current | SDIO ^{(2) (3)} | | | ± 50 ⁽⁴⁾ | nA |
| R_{PU} | Pull up resistance | All I/O except ODIO | | 40 | | k Ω |
| R_{PD} | Pull down resistance | | | 40 | | k Ω |
| C_{I} | Input capacitance | | | 5 | | pF |
| V_{OH} | High level output voltage | SDIO | VDD \geq 2.7V, $ I_{\text{IOI,max}} =6\text{mA}$ VDD \geq 1.71V, $ I_{\text{IOI,max}} =2\text{mA}$ VDD \geq 1.62V, $ I_{\text{IOI,max}} =1.5\text{mA}$ -40 °C $\leq T_{\text{J}} \leq 25$ °C | VDD-0.4 | | V |
| | | | VDD \geq 2.7V, $ I_{\text{IOI,max}} =6\text{mA}$ VDD \geq 1.71V, $ I_{\text{IOI,max}} =2\text{mA}$ VDD \geq 1.62V, $ I_{\text{IOI,max}} =1.5\text{mA}$ -40 °C $\leq T_{\text{J}} \leq 130$ °C | VDD-0.45 | | |
| | | HSIO | VDD \geq 2.7V, DRV=1, $ I_{\text{IOI,max}} =6\text{mA}$ VDD \geq 1.71V, DRV=1, $ I_{\text{IOI,max}} =3\text{mA}$ VDD \geq 1.62V, DRV=1, $ I_{\text{IOI,max}} =2\text{mA}$ -40 °C $\leq T_{\text{J}} \leq 25$ °C | VDD-0.4 | | |
| | | | VDD \geq 2.7V, DRV=1, $ I_{\text{IOI,max}} =6\text{mA}$ VDD \geq 1.71V, DRV=1, $ I_{\text{IOI,max}} =3\text{mA}$ VDD \geq 1.62V, DRV=1, $ I_{\text{IOI,max}} =2\text{mA}$ -40 °C $\leq T_{\text{J}} \leq 130$ °C | VDD-0.4 | | |
| | | | VDD \geq 2.7V, DRV=0, $ I_{\text{IOI,max}} =4\text{mA}$ VDD \geq 1.71V, DRV=0, $ I_{\text{IOI,max}} =2\text{mA}$ VDD \geq 1.62V, DRV=0, $ I_{\text{IOI,max}} =1.5\text{mA}$ -40 °C $\leq T_{\text{J}} \leq 25$ °C | VDD-0.45 | | |
| | | | VDD \geq 2.7V, DRV=0, $ I_{\text{IOI,max}} =4\text{mA}$ VDD \geq 1.71V, DRV=0, $ I_{\text{IOI,max}} =2\text{mA}$ VDD \geq 1.62V, $ I_{\text{IOI,max}} =1.5\text{mA}$ -40 °C $\leq T_{\text{J}} \leq 130$ °C | VDD-0.45 | | |

7.10.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------|-----------------|--|-----|-----|------|------|
| V _{OL} | Low level output voltage | SDIO | VDD ≥ 2.7V, I _{IO} _{max} = 6mA VDD ≥ 1.71V, I _{IO} _{max} = 2mA VDD ≥ 1.62V, I _{IO} _{max} = 1.5mA -40 °C ≤ T _j ≤ 25 °C | | | 0.4 | V |
| | | | VDD ≥ 2.7V, I _{IO} _{max} = 6mA VDD ≥ 1.71V, I _{IO} _{max} = 2mA VDD ≥ 1.62V, I _{IO} _{max} = 1.5mA -40 °C ≤ T _j ≤ 130 °C | | | 0.45 | |
| | | HSIO | VDD ≥ 2.7V, DRV = 1, I _{IO} _{max} = 6mA VDD ≥ 1.71V, DRV = 1, I _{IO} _{max} = 3mA VDD ≥ 1.62V, DRV = 1, I _{IO} _{max} = 2mA T _j ≤ 85 °C | | | 0.4 | |
| | | | VDD ≥ 2.7V, DRV = 1, I _{IO} _{max} = 6mA VDD ≥ 1.71V, DRV = 1, I _{IO} _{max} = 3mA VDD ≥ 1.62V, DRV = 1, I _{IO} _{max} = 2mA -40 °C ≤ T _j ≤ 130 °C | | | 0.45 | |
| | | | VDD ≥ 2.7V, DRV = 0, I _{IO} _{max} = 4mA VDD ≥ 1.71V, DRV = 0, I _{IO} _{max} = 2mA VDD ≥ 1.62V, DRV = 0, I _{IO} _{max} = 1.5mA T _j ≤ 85 °C | | | 0.4 | |
| | | | VDD ≥ 2.7V, DRV = 0, I _{IO} _{max} = 4mA VDD ≥ 1.71V, DRV = 0, I _{IO} _{max} = 2mA VDD ≥ 1.62V, DRV = 0, I _{IO} _{max} = 1.5mA -40 °C ≤ T _j ≤ 130 °C | | | 0.45 | |
| | | ODIO | VDD ≥ 2.7V, I _{OL,max} = 8mA VDD ≥ 1.71V, I _{OL,max} = 4mA -40 °C ≤ T _j ≤ 25 °C | | | 0.4 | |
| | | | VDD ≥ 2.7V, I _{OL,max} = 8mA VDD ≥ 1.71V, I _{OL,max} = 4mA -40 °C ≤ T _j ≤ 130 °C | | | 0.45 | |

- (1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed
- (2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
- (3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
- (4) This value is for SDIO not muxed with any analog inputs. If the SDIO is muxed with analog inputs then the leakage can be as high as 100nA.

7.10.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---------------------------------|-----------------------|------------------------------|--|------------|-----|----------------------|------|
| f _{max} | Port output frequency | SDIO (1) | VDD ≥ 1.71V, C _L = 20pF | | | 16 | MHz |
| | | | VDD ≥ 2.7V, C _L = 20pF | | | 32 | |
| | | HSIO | VDD ≥ 1.71V, DRV = 0, C _L = 20pF | | | 16 | |
| | | | VDD ≥ 1.71V, DRV = 1, C _L = 20pF | | | 24 | |
| | | | VDD ≥ 2.7V, DRV = 0, C _L = 20pF | | | 32 | |
| | | ODIO | VDD ≥ 1.71V, FM ⁺ , C _L = 20pF - 100pF | | | 1 | |
| t _r , t _f | Output rise/fall time | All output ports except ODIO | VDD ≥ 1.71V | | | 0.3*f _{max} | s |
| t _f | Output fall time | ODIO | VDD ≥ 1.71V, FM ⁺ , C _L = 20pF-100pF | 20*VDD/5.5 | | 120 | ns |

- (1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed

7.11 Analog Mux VBOOST

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|----------------------|--|-----|-----|-----|------|
| I _{VBST} | VBOOST current adder | MCLK/ULPCLK is LFCLK | | 0.8 | | uA |
| | | MCLK/ULPCLK is not LFCLK, SYSOSC frequency is 4MHz | | 8.5 | | |
| t _{START,VBST} | VBOOST startup time | | | 12 | | us |

7.12 ADC

7.12.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|--|---|------|------|------|------|
| V _{IN(ADC)} | Analog input voltage range ⁽¹⁾ | Applies to all ADC analog input pins | 0 | | VDD | V |
| V _{R+} | Positive ADC reference voltage | V _{R+} sourced from VDD | | VDD | | V |
| | | V _{R+} sourced from external reference pin (VREF+) | 1.4 | | VDD | V |
| | | V _{R+} sourced from internal reference (VREF) | | VREF | | V |
| V _{R-} | Negative ADC reference voltage | | 0 | | | V |
| F _S | ADC sampling frequency | RES = 0x0 (12-bit mode), External Reference | | | 1.68 | Msps |
| I _(ADC) ⁽²⁾ | Operating supply current into VDD terminal | F _S = 1MSPS, Internal reference OFF, V _{R+} = VDD | | 454 | 600 | μA |
| | | F _S = 200ksps, Internal reference ON, V _{R+} = VREF = 2.5V | | 300 | 435 | |
| C _{S/H} | ADC sample-and-hold capacitance | | | 3.3 | 7 | pF |
| R _{in} | ADC sampling switch resistance | | | 0.5 | 1 | kΩ |
| ENOB | Effective number of bits | Internal reference, V _{R+} = VREF = 2.5V, F _{in} = 10KHz | 10 | 10.2 | | bit |
| | | External reference, F _{in} = 10KHz ⁽³⁾ | 11 | 11.1 | | |
| SNR | Signal-to-noise ratio | External reference ⁽³⁾ | 68 | 71 | | dB |
| | | Internal reference, V _{R+} = VREF = 2.5V | 63 | 65 | | |
| PSRR _{DC} | Power supply rejection ratio, DC | External reference ⁽³⁾ , VDD = VDD _(min) to VDD _(max) | 63 | 68 | | dB |
| | | VDD = VDD _(min) to VDD _(max) Internal reference, V _{R+} = VREF = 2.5V | 49 | 55 | | |
| PSRR _{AC} | Power supply rejection ratio, AC | External reference ⁽³⁾ , ΔVDD = 0.1 V at 1 kHz | | 61 | | dB |
| | | ΔVDD = 0.1 V at 1 kHz Internal reference, V _{R+} = VREF = 2.5V | | 49 | | |
| T _{wakeup} | ADC Wakeup Time | Assumes internal reference is active | | 1 | | us |
| V _{SupplyMon} | Supply Monitor voltage divider (VDD/3) accuracy | ADC input channel: Supply Monitor ⁽⁴⁾ | -1.5 | | +1.5 | % |
| I _{SupplyMon} | Supply Monitor voltage divider current consumption | ADC input channel: Supply Monitor | | 10 | | uA |

(1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.

(2) The internal reference (VREF) supply current is not included in current consumption parameter I_(ADC).

(3) All external reference specifications are measured with V_{R+} = VREF+ = VDD = 3.3V and V_{R-} = VREF- = VSS = 0V and external 1uF cap on VREF+ pin

(4) Analog power supply monitor. Analog input on channel 15 is disconnected and is internally connected to the voltage divider which is VDD/3.

7.12.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|--------------------------------|-----------------|-----|-----|-----|---------------|
| f _{ADCCLK} | ADC clock frequency | | 4 | | 32 | MHz |
| t _{ADC trigger} | Software trigger minimum width | | 3 | | | ADCCLK cycles |

7.12.2 Switching Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------------------|---|---|---------------------------|------|-----|-----|---------------|
| t_{Sample} | Sampling time without OPA | 12-bit mode, $R_S = 50\Omega$, $C_{\text{pext}} = 10\text{pF}$ | | 156 | | | ns |
| $t_{\text{Sample_PGA}}$ | Sampling time with OPA ⁽¹⁾ | 12-bit mode | GBW = 0x1, PGA gain = x1 | 0.31 | | | μs |
| | | | GBW = 0x1, PGA gain = x32 | 1.5 | | | μs |
| $t_{\text{Sample_GPAMP}}$ | Sampling time with GPAMP | 12-bit mode | | 2.5 | | | μs |
| $t_{\text{Sample_SupplyMon}}$ | Sample time with Supply Monitor (VDD/3) | 12-bit mode | | 3 | | | μs |

(1) Only applies for devices with OPA

7.12.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) ⁽¹⁾

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------|---|---|--|------|-----|------|------|
| E_I | Integral linearity error (INL) | External reference ⁽²⁾ | | -2.0 | | +2.0 | LSB |
| E_D | Differential linearity error (DNL) Guaranteed no missing codes | External reference ⁽²⁾ | | -1.0 | | +1.0 | LSB |
| E_O | Offset error | External reference ⁽²⁾ | | -3 | | 3 | mV |
| | | Internal reference, $V_{R+} = V_{\text{REF}} = 2.5\text{V}$ | | -3 | | 3 | mV |
| E_G | Gain error | External reference ⁽²⁾ | | -3 | | 3 | LSB |

(1) Total Unadjusted Error (TUE) can be calculated from E_I , E_O , and E_G using the following formula: $TUE = \sqrt{(E_I)^2 + |E_O|^2 + E_G^2}$

Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate

(2) All external reference specifications are measured with $V_{R+} = V_{\text{REF}+} = V_{\text{DD}} = 3.3\text{V}$ and $V_{R-} = V_{\text{REF}-} = V_{\text{SS}} = 0\text{V}$ and external 1 μF cap on $V_{\text{REF}+}$ pin

7.12.4 Typical Connection Diagram

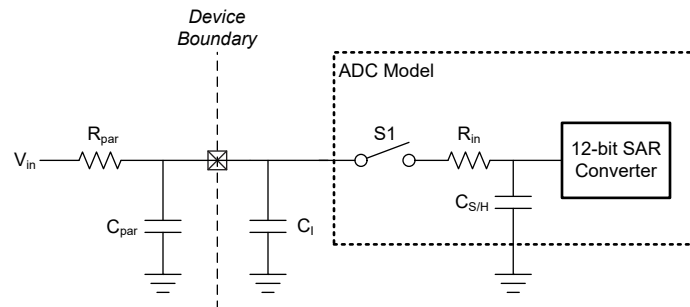


Figure 7-2. ADC Input Network

1. Refer to [ADC Electrical Characteristics](#) for the values of R_{in} and $C_{\text{S/H}}$
2. Refer to [Digital IO Electrical Characteristics](#) for the value of C_I
3. C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1. $\text{Tau} = (R_{\text{par}} + R_{\text{in}}) \times C_{\text{S/H}} + R_{\text{par}} \times (C_{\text{par}} + C_I)$
2. $K = \ln(2^n / \text{Settling error}) - \ln((C_{\text{par}} + C_I) / C_{\text{S/H}})$
3. T (Min sampling time) = $K \times \text{Tau}$

7.13 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|--|-------|-------|-------|-------|
| T _{TRIM} | Factory trim temperature ⁽¹⁾ | ADC and VREF configuration: RES=0 (12-bit mode), VRSEL=2h (internal VREF), BUFCONFIG=1h (1.4V VREF), ADC t _{sample} =12.5μs | 27 | 30 | 33 | °C |
| TS _c | Temperature coefficient | | -1.84 | -1.75 | -1.66 | mV/°C |
| t _{SET, TS} | Temperature sensor settling time ⁽²⁾ | | | 2.5 | 10 | us |

(1) Higher absolute accuracy may be achieved through user calibration.

(2) This is the maximum time required for the temperature sensor to settle when measured by the ADC. It may be used to specify the minimum ADC sample time when measuring the temperature sensor.

7.14 VREF

7.14.1 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|-----------------|-------|-----|-------|------|
| VDD _{min} | Minimum supply voltage needed for VREF operation | BUFCONFIG = 1 | 1.62 | | | V |
| | | BUFCONFIG = 0 | 2.7 | | | |
| VREF | Voltage reference output voltage | BUFCONFIG = 1 | 1.379 | 1.4 | 1.421 | V |
| | | BUFCONFIG = 0 | 2.462 | 2.5 | 2.538 | |

7.14.2 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--|---|-----|-----|-----|--------|
| I _{VREF} | VREF operating supply current | BUFCONFIG = {0, 1}, No load | | 74 | 100 | μA |
| TC _{VREF} | Temperature coefficient of VREF ⁽¹⁾ | BUFCONFIG = {0, 1} | | | 200 | ppm/°C |
| TC _{drift} | Long term VREF drift | Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25°C | | | 300 | ppm |
| PSRR _{DC} | VREF Power supply rejection ratio, DC | VDD = 1.7 V to VDDmax, BUFCONFIG = 1 | 59 | 64 | | dB |
| | | VDD = 2.7 V to VDDmax, BUFCONFIG = 0 | 49 | 53 | | |
| V _{noise} | RMS noise at VREF output (0.1 Hz to 100 MHz) | BUFFCONFIG = 1 | | 500 | | μVrms |
| | | BUFFCONFIG = 0 | | 750 | | |
| ADC F _S | Max supported ADC sampling frequency | Using VREF as ADC reference | | | 200 | ksps |
| T _{startup} | VREF startup time | BUFCONFIG = {0, 1}, VDD = 2.8 V | | | 15 | us |

(1) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.

7.15 COMP

7.15.1 Comparator Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------------|-----------------|-----|-----|-----|------|
| Comparator Electrical Characteristics | | | | | | |
| V _{cm} | Common mode input range | | 0 | | VDD | V |
| V _{offset} | Input offset voltage | | | | ±25 | mV |

7.15.1 Comparator Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|----------------------------------|--|-----|-----|-----|------|
| V _{hys} | DC input hysteresis | HYST=00h | | 0.4 | | mV |
| | | HYST=01h | | 11 | | |
| | | HYST=02h | | 20 | | |
| | | HYST=03h | | 30 | | |
| t _{PD_ls} | Propagation delay, response time | Output Filter off, Overdrive = 100 mV, High Speed Mode | | 32 | 50 | ns |
| | | Output Filter off, Overdrive = 100 mV, Low Power Mode | | | 5 | μs |
| t _{en} | Comparator enable time | Startup time to reach propagation delay specification, High Speed Mode | | | 10 | μs |
| | | Startup time to reach propagation delay specification, Low Power Mode | | | 10 | μs |
| I _{comp} | Comparator current consumption. | V _{cm} = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, High Speed Mode | | 120 | 200 | μA |
| | | V _{cm} = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, Low Power Mode | | 0.8 | 2.7 | μA |
| | | V _{cm} = VDD/2, 100mV overdrive, comparator only, High Speed Mode | | 100 | 180 | μA |
| | | V _{cm} = VDD/2, 100mV overdrive, comparator only, Low Power Mode | | 0.7 | 2.1 | μA |

8-bit DAC Electrical Characteristics

| | | | | | | |
|-------------------------|---|---|----|-----------------------------|-----|----------|
| V _{dac} | DAC output range | | 0 | | VDD | V |
| V _{dac-code} | 8-bit DAC output voltage for a given code | V _{IN} = reference voltage into 8-bit DAC, code n = 0 to 255 | | $V_{IN} \times (n+1) / 256$ | | V |
| INL | Integral nonlinearity of 8-bit DAC | | -1 | | 1 | LSB |
| DNL | Differential nonlinearity of 8-bit DAC | | -1 | | 1 | LSB |
| Gain error | Gain error of 8-bit DAC | Reference voltage = VDD | -2 | | 2 | % of FSR |
| Offset error | Offset error of 8-bit DAC | | -5 | | 5 | mV |
| t _{dac_settle} | 8-bit DAC settling time in static mode | DACCODE0 = 0 → 255, DAC output accurate to 1 LSB | | 1.5 | | μs |

7.16 GPAMP

7.16.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|-------------------------------|---|-------------------|-------|---------|------|
| V _{CM} | Common mode voltage range | RRI = 0x0 | -0.1 | | VDD-1 | V |
| | | RRI = 0x1 | 1 | | VDD-0.2 | |
| | | RRI = 0x2 | -0.1 | | VDD-0.2 | |
| I _q | Quiescent current, per op-amp | I _O = 0 mA, RRI = 0x0 | | 97 | | μA |
| | | I _O = 0 mA, RRI = 0x1 or 0x2 | | 93 | | |
| GBW | Gain-bandwidth product | C _L = 200pF | | 0.32 | | MHz |
| V _{OS} | Input offset voltage | Noninverting, unity gain, T _A = 25°C, VDD = 3.3V | CHOPCLKMODE = 0x0 | ±0.2 | ±6.5 | mV |
| | | | CHOPCLKMODE = 0x1 | ±0.08 | ±0.4 | |

7.16.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------|--|--|------------------------|-------|-----|-----|--------|
| dV _{OS} /dT | Input offset voltage temperature drift | Noninverting, unity gain | CHOPCLKMODE = 0x0 | 7.7 | | | μV/°C |
| | | | CHOPCLKMODE = 0x1 | 0.34 | | | |
| I _{bias} | Input bias for muxed I/O pin at SoC | 0.1V < V _{in} < VDD-0.3V, VDD=3.3V, CHOPCLKMODE=0x0 | T _A = 25°C | ±40 | | | pA |
| | | | T _A = 125°C | ±4000 | | | |
| | | 0.1V < V _{in} < VDD-0.3V, VDD=3.3V, CHOPCLKMODE=0x1 | T _A = 25°C | ±200 | | | |
| | | | T _A = 125°C | ±4000 | | | |
| CMRR _{DC} | Common mode rejection ratio, DC | Over common mode voltage range | CHOPCLKMODE = 0x0 | 48 | 77 | | dB |
| | | | CHOPCLKMODE = 0x1 | 56 | 105 | | |
| e _n | Input voltage noise density | Noninverting, unity gain | f = 1 kHz | 43 | | | nV/√Hz |
| | | | f = 10 kHz | 19 | | | |
| R _{in} | Input resistance ⁽¹⁾ | | | 0.65 | | | kΩ |
| C _{in} | Input capacitance | Common mode | | 4 | | | pF |
| | | Differential | | 2 | | | |
| A _{OL} | Open-loop voltage gain, DC | R _L = 350 kΩ, 0.3 < V _o < VDD-0.3 | | 82 | 90 | 107 | dB |
| PM | phase margin | C _L = 200 pF, R _L = 350 kΩ | | 69 | 70 | 72 | degree |
| SR | Slew rate | Noninverting, unity gain, C _L = 40 pF | | 0.32 | | | V/μs |
| THDN | Total Harmonic Distortion + Noise | | | 0.012 | | | % |
| I _{Load} | Output load current | | | ±4 | | | mA |
| C _{Load} | Output load capacitance | | | | | 200 | pF |

(1) The term 'Rin' refers to the input resistance of the multiplexer (mux) in the GPAMP.

7.16.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------|---------------------|---|--------------------------|-----|-----|-----|---------------|
| t _{EN} | GPAMP enable time | ENABLE = 0x0 to 0x1, Bandgap reference ON, 0.1% | Noninverting, unity gain | | 12 | 20 | μs |
| t _{disable} | GPAMP disable time | | | | 4 | | ULPCLK Cycles |
| t _{SETTLE} | GPAMP settling time | C _L = 200 pF, Vstep = 0.3V to VDD - 0.3V, 0.1%, ENABLE = 0x1 | Noninverting, unity gain | | 9 | | μs |

7.17 OPA

7.17.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------------------|--|--|------|-----|---------|------|
| V _{CM} | Common mode voltage range | RRI = 0x0 | | -0.1 | | VDD-1.1 | V |
| | | RRI = 0x1 | | -0.1 | | VDD-0.3 | |
| V _O | Voltage output swing from rail range | R _L = 10kΩ connected to VDD/2 | | | 20 | 68 | mV |

7.17.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------|---|--|---------------------------|-----------|------------|------------------|------------------------------|
| I_q | Quiescent current, per op-amp ⁽³⁾ | $I_O = 0\text{mA}$, RRI = 0x0 | GBW = 0x0 | | 100 | | μA |
| | | | GBW = 0x1 | | 350 | | |
| | | $I_O = 0\text{mA}$, RRI = 0x1 | GBW = 0x0 | | 140 | 170 | |
| | | | GBW = 0x1 | | 450 | 600 | |
| I_{BCS} | Burn-out current source current | | | 2 | | μA | |
| GBW | Gain-bandwidth product | Noninverting, unity gain, $C_L = 40\text{pF}$ | GBW = 0x0 | | 1.5 | | MHz |
| | | | GBW = 0x1 | | 6 | | |
| V_{OS} | Input offset voltage | Noninverting, unity gain, $V_{DD} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$ | CHOP = 0x0 | | ± 0.4 | ± 2 | mV |
| | | | CHOP = 0x1 or 0x2 | | | ± 0.3 | |
| | | Noninverting, unity gain, $V_{DD} = 3.3\text{V}$ | CHOP = 0x0 | | ± 1.5 | ± 3.5 | |
| | | | CHOP = 0x1 or 0x2 | | ± 0.1 | ± 0.5 | |
| dV_{OS}/dT | Input offset voltage temperature drift | Noninverting, unity gain, CHOP = 0x0 | GBW = 0x0 | | ± 8.5 | | $\mu\text{V}/^\circ\text{C}$ |
| | | | GBW = 0x1 | | ± 6 | | |
| | | Noninverting, unity gain, CHOP = 0x1 or 0x2 | | ± 0.5 | | | |
| $PSRR_{DC}$ | Power Supply Rejection Ratio, DC | Noninverting, unity gain | CHOP = 0x0 | 74 | 86 | | dB |
| | | | CHOP = 0x1 or 0x2 | 74 | 86 | | |
| I_{bias} | Input bias current | $0.1\text{V} < V_{in} < V_{DD} - 0.3\text{V}$, $V_{DD} = 3.3\text{V}$, CHOP=0x0 | $T_A = 25^\circ\text{C}$ | | ± 50 | | pA |
| | | | $T_A = 125^\circ\text{C}$ | | ± 0.35 | ± 100 | nA |
| | | $0.1\text{V} < V_{in} < V_{DD} - 0.3\text{V}$, $V_{DD} = 3.3\text{V}$, CHOP=0x1 | $T_A = 25^\circ\text{C}$ | | ± 0.4 | | nA |
| | | | $T_A = 125^\circ\text{C}$ | | ± 0.4 | ± 104 | nA |
| I_{bias} | Input bias current for dedicated OPA input pin ⁽¹⁾ | $0.1\text{V} < V_{in} < V_{DD} - 0.3\text{V}$, $V_{DD} = 3.3\text{V}$, CHOP=0x0 | $T_A = 25^\circ\text{C}$ | | ± 6 | | pA |
| | | | $T_A = 125^\circ\text{C}$ | | ± 0.35 | ± 0.4 | nA |
| | | $0.1\text{V} < V_{in} < V_{DD} - 0.3\text{V}$, $V_{DD} = 3.3\text{V}$, CHOP=0x1 | $T_A = 25^\circ\text{C}$ | | ± 0.4 | | nA |
| | | | $T_A = 125^\circ\text{C}$ | | ± 0.4 | ± 0.5 | nA |
| $CMRR_{DC}$ | Common mode rejection ratio, DC | RRI = 0x0: $0\text{V} < V_{CM} < V_{DD} - 1.1\text{V}$ RRI = 0x1: $0\text{V} < V_{CM} < V_{DD} - 0.3\text{V}$ | CHOP = 0x0 | | 89 | | dB |
| | | | CHOP = 0x1 or 0x2 | 73 | 102 | | |
| e_n | Input voltage noise density | GBW = 0x0, Noninverting, unity gain, CHOP = 0x0 | f = 1kHz | | 240 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | | | f = 10kHz | | 88 | | |
| R_{in} | Input resistance ⁽²⁾ | | | 2.6 | | $\text{k}\Omega$ | |
| C_{in} | Input capacitance | Common mode | | 3 | | pF | |
| A_{OL} | Open-loop voltage gain, DC | $R_L = 20\text{k}\Omega$ to GND, $0.3 < V_o < V_{DD} - 0.3$ | | 105 | | dB | |
| PM | phase margin | $C_L = 40\text{pF}$ | GBW = 0x0 | | 57 | | degree |
| | | | GBW = 0x1 | | 50 | | |
| SR | Slew rate | Noninverting, unity gain, $C_L = 40\text{pF}$ | GBW = 0x0 | | 1.3 | | $\text{V}/\mu\text{s}$ |
| | | | GBW = 0x1 | | 4.9 | | |
| THDN | Total harmonic distortion + noise | Noninverting, unity gain, GBW = 0x0, f = 1.5kHz, Integration BW = 100kHz | | 0.0034 | | % | |
| | | Noninverting, unity gain, GBW = 0x1, f = 6kHz, Integration BW = 100kHz | | 0.004 | | | |
| I_{Load} | Short circuit current | GBW = 0x0, $T_A = 25^\circ\text{C}$ | | ± 9 | | mA | |
| | | GBW = 0x1, $T_A = 25^\circ\text{C}$ | | ± 30 | | | |
| C_{Load} | Output load capacitance | | | | 40 | pF | |

(1) MSPM0L134x devices only

(2) R_{in} here means the input resistance of mux in OPA.

(3) Excluding VBOOST current. VBOOST must be enabled when OPA is enabled.

7.17.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------|------------------------|--|------------|--------|-----|---------------|------|
| t _{EN} | OPA enable time | ENABLE = 0x0 to 0x1, Bandgap reference ON, 0.1%, Noninverting, unity gain | GBW = 0x0 | 7.3 | 12 | μs | |
| | | | GBW = 0x1 | 4.4 | 6 | | |
| t _{disable} | OPA disable time | | | 4 | | ULPCLK cycles | |
| f _{CHOP} | OPA Chopping Frequency | CHOP = 0x1 | GAIN = 0x0 | 125 | | kHz | |
| | | | GAIN = 0x1 | 62.5 | | | |
| | | | GAIN = 0x2 | 31.25 | | | |
| | | | GAIN = 0x3 | 15.625 | | | |
| | | | GAIN = 0x4 | 7.8 | | | |
| | | | GAIN = 0x5 | 3.9 | | | |
| t _{SETTLE} | OPA settling time | C _L = 40 pF, Vstep = 0.3V to VDD-0.3V, 0.1%, ENABLE = 0x1, Noninverting, unity gain | GBW = 0x0 | 2.5 | 9 | μs | |
| | | | GBW = 0x1 | 1.3 | 5 | | |

7.17.3 PGA Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|------------------------------------|----------------------------|------------------------|--------|-------|-------|------|
| G | Non- inverting gain accuracy | Buffer Mode ⁽¹⁾ | Unity Gain | -0.05 | | +0.05 | % |
| | | GAIN = 0x1 | Gain of 2 | -0.6 | | +0.6 | |
| | | GAIN = 0x2 | Gain of 4 | -0.8 | | +0.8 | |
| | | GAIN = 0x3 | Gain of 8 | -1 | | +1 | |
| | | GAIN = 0x4 | Gain of 16 | -1.5 | | 1.5 | |
| | | GAIN = 0x5 | Gain of 32 | -2.6 | | +2.6 | |
| | Inverting gain accuracy | GAIN = 0x1 | Gain of -1 | -0.8 | | +0.8 | |
| | | GAIN = 0x2 | Gain of -3 | -1.0 | | +1.0 | |
| | | GAIN = 0x3 | Gain of -7 | -1.2 | | 1.2 | |
| | | GAIN = 0x4 | Gain of -15 | -1.5 | | 1.5 | |
| R _{PGA} | Programmable gain stage resistance | GAIN = 0x1 | R1 | | 64 | kΩ | |
| | | | R2 (feedback resistor) | | 64 | | |
| | | GAIN = 0x2 | R1 | | 32 | | |
| | | | R2 (feedback resistor) | | 96 | | |
| | | GAIN = 0x3 | R1 | | 16 | | |
| | | | R2 (feedback resistor) | | 112 | | |
| | | GAIN = 0x4 | R1 | | 8 | | |
| | | | R2 (feedback resistor) | | 120 | | |
| GAIN = 0x5 | R1 | | 4 | | | | |
| | R2 (feedback resistor) | | 124 | | | | |
| G/dV | Gain supply drift | | | 0.026 | 0.84 | %/V | |
| G/dT | Gain temperature drift | | | 0.0007 | 0.014 | %/C | |

7.17.3 PGA Mode (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---------------------------|---|-----|-----|-----|------|
| THD | Total harmonic distortion | f = 3kHz, R _L = 1.5kOhm to VDD/2, GBW = 0x1, GAIN = 0x1 | | 88 | | dB |
| | | f = 188Hz, R _L = 1.5kOhm to VDD/2, GBW = 0x1, GAIN = 0x5 | | 61 | | |

(1) OPA operates with unity gain in buffer mode, providing impedance matching and signal buffering without the amplification.

7.18 I2C

7.18.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | Standard mode | | Fast mode | | Fast mode plus | | UNIT |
|---------------------|--|----------------------|---------------|------|-----------|-----|----------------|------|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{I2C} | I2C input clock frequency | I2C in Power Domain0 | 2 | 32 | 8 | 32 | 20 | 32 | MHz |
| f _{SCL} | SCL clock frequency | | | 0.1 | | 0.4 | | 1 | MHz |
| t _{HD,STA} | Hold time (repeated) START | | 4 | | 0.6 | | 0.26 | | us |
| t _{LOW} | Low period of the SCL clock | | 4.7 | | 1.3 | | 0.5 | | us |
| t _{HIGH} | High period of the SCL clock | | 4 | | 0.6 | | 0.26 | | us |
| t _{SU,STA} | Setup time for a repeated START | | 4.7 | | 0.6 | | 0.26 | | us |
| t _{HD,DAT} | Data hold time | | 0 | | 0 | | 0 | | ns |
| t _{SU,DAT} | Data setup time | | 250 | | 100 | | 50 | | ns |
| t _{SU,STO} | Setup time for STOP | | 4 | | 0.6 | | 0.26 | | us |
| t _{BUF} | Bus free time between a STOP and START condition | | 4.7 | | 1.3 | | 0.5 | | us |
| t _{VD,DAT} | Data valid time | | | 3.45 | | 0.9 | | 0.45 | us |
| t _{VD,ACK} | Data valid acknowledge time | | | 3.45 | | 0.9 | | 0.45 | us |

7.18.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---|-----------------|-----|-----|-----|------|
| f _{SP} | Pulse duration of spikes suppressed by input filter | AGFSELx = 0 | | 6 | | ns |
| | | AGFSELx = 1 | | 14 | 35 | ns |
| | | AGFSELx = 2 | | 22 | 60 | ns |
| | | AGFSELx = 3 | | 35 | 90 | ns |

7.18.3 I²C Timing Diagram

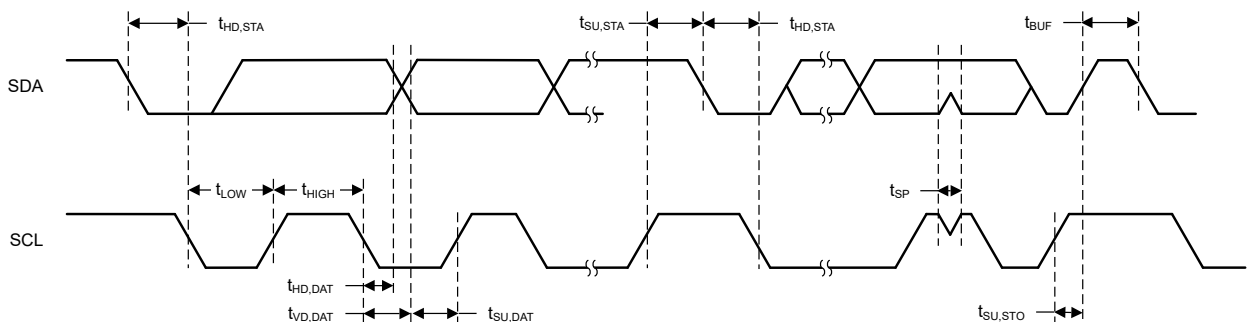


Figure 7-3. I2C Timing Diagram

7.19 SPI

7.19.1 SPI

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|---|---------------------------|----------------------|---------------------------|------|
| SPI | | | | | | |
| f _{SPI} | SPI clock frequency | Clock max speed = 32MHz 1.62 < VDD < 3.6V Controller mode | | | 16 | MHz |
| f _{SPI} | SPI clock frequency | Clock max speed = 32MHz 1.62 < VDD < 3.6V Peripheral mode | | | 16 | MHz |
| DC _{SCK} | SCK Duty Cycle | | 40 | 50 | 60 | % |
| Controller | | | | | | |
| t _{SCLK_H/L} | SCLK High or Low time | | (t _{SPI/2}) - 1 | t _{SPI} / 2 | (t _{SPI/2}) + 1 | ns |
| t _{SU.CI} | POCI input data setup time ⁽¹⁾ | 2.7 < VDD < 3.6V, delayed sampling enabled | 1 | | | ns |
| | | 1.62 < VDD < 2.7V, delayed sampling enabled | 1 | | | |
| t _{SU.CI} | POCI input data setup time ⁽¹⁾ | 2.7 < VDD < 3.6V, no delayed sampling | 27 | | | ns |
| | | 1.62 < VDD < 2.7V, no delayed sampling | 35 | | | |
| t _{HD.CI} | POCI input data hold time | | 9 | | | ns |
| t _{VALID.CO} | PICO output data valid time ⁽²⁾ | | | | 10 | ns |
| t _{HD.CO} | PICO output data hold time ⁽³⁾ | | 1 | | | ns |
| Peripheral | | | | | | |
| t _{CS.LEAD} | CS lead-time, CS active to clock | | 8 | | | ns |
| t _{CS.LAG} | CS lag time, Last clock to CS inactive | | 1 | | | ns |
| t _{CS.ACC} | CS access time, CS active to POCI data out | | | | 23 | ns |
| t _{CS.DIS} | CS disable time, CS inactive to POCI high impedance | | | | 19 | ns |
| t _{SU.PI} | PICO input data setup time | | 7 | | | ns |
| t _{HD.PI} | PICO input data hold time | | 31.25 | | | ns |
| t _{VALID.PO} | POCI output data valid time ⁽²⁾ | 2.7 < VDD < 3.6V | | | 24 | ns |
| t _{VALID.PO} | POCI output data valid time ⁽²⁾ | 1.62 < VDD < 2.7V | | | 31 | ns |
| t _{HD.PO} | POCI output data hold time ⁽³⁾ | | 5 | | | ns |

- (1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.19.2 SPI Timing Diagram

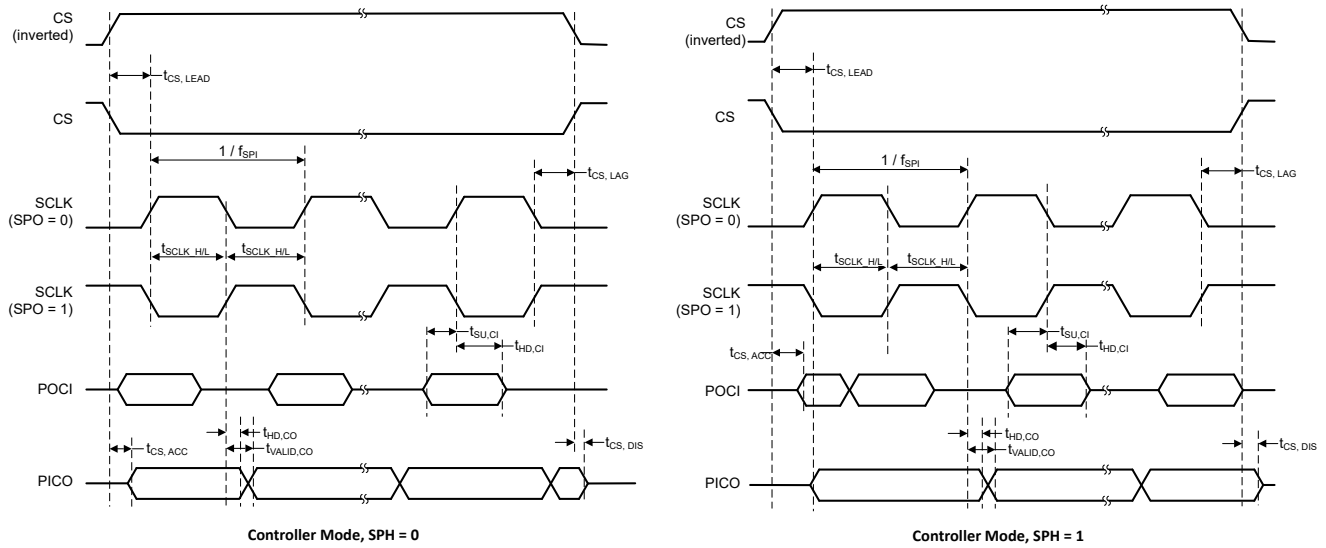


Figure 7-4. SPI Timing Diagram - Controller Mode

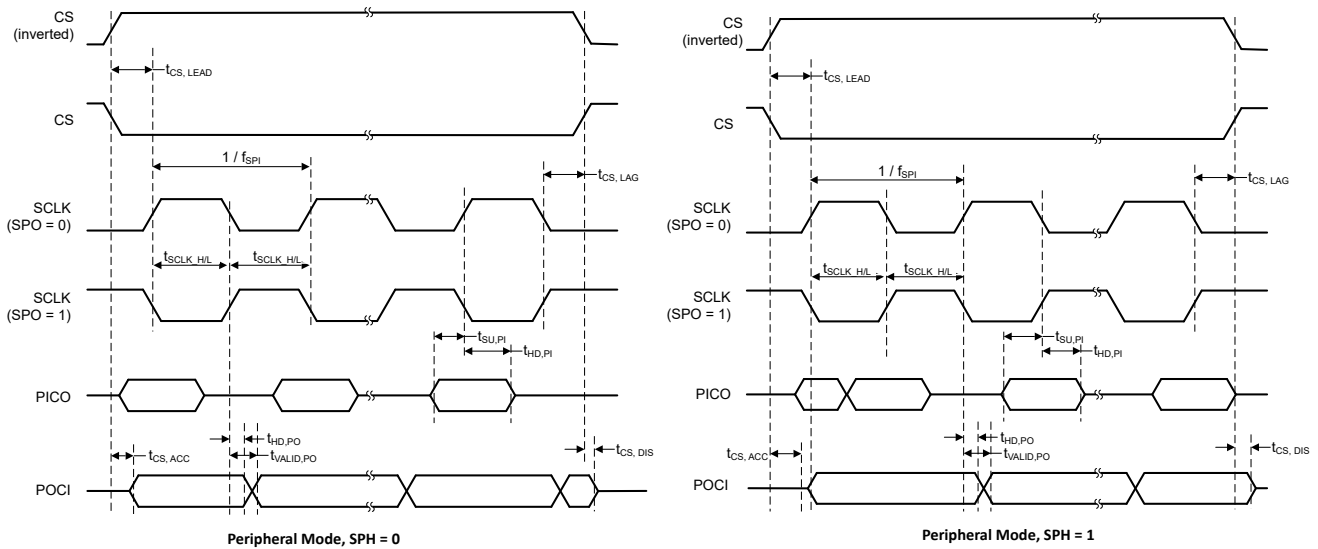


Figure 7-5. SPI Timing Diagram - Peripheral Mode

7.20 UART

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|-----------------|-----|-----|-----|------|
| f_{UART} | UART input clock frequency | | | | 32 | MHz |
| f_{BITCLK} | BITCLK clock frequency (equals baud rate in MBaud) | | | | 4 | MHz |
| t_{SP} | Pulse duration of spikes suppressed by input filter | AGFSELx = 0 | | 6 | | ns |
| | | AGFSELx = 1 | | 14 | 35 | ns |
| | | AGFSELx = 2 | | 22 | 60 | ns |
| | | AGFSELx = 3 | | 35 | 90 | ns |

7.21 TIMx

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|-----------------------------|------------------------------|---------|-----|-------|----------------------|
| t _{res} | Timer resolution time | f _{TIMxCLK} = 32MHz | 31.25 | | | ns |
| | | | 1 | | | t _{TIMxCLK} |
| t _{res} | Timer resolution time | TIMx with 16bit counter | | | 16 | bit |
| t _{COUNTER} | 16-bit counter clock period | f _{TIMxCLK} = 32MHz | 0.03125 | | 2048 | us |
| | | | 1 | | 65536 | t _{TIMxCLK} |

7.22 Emulation and Debug

7.22.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---------------|-----------------|-----|-----|-----|------|
| f _{SWD} | SWD frequency | | | | 10 | MHz |

8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.1 CPU

The CPU subsystem (MCPUSS) implements an Arm Cortex-M0+ CPU, an instruction prefetch and cache, a system timer, and interrupt management features. The Arm Cortex-M0+ is a cost-optimized 32-bit CPU that delivers high performance and low power to embedded applications. Key features of the CPU Sub System include:

- Arm Cortex-M0+ CPU supports clock frequencies from 32 kHz to 32 MHz
 - ARMv6-M Thumb instruction set (little endian) with single-cycle 32×32 multiply instruction
 - Single-cycle access to GPIO registers through Arm single-cycle IO port
- Prefetch logic to improve sequential code execution, and I-cache with 2 64-bit cache lines
- System timer (SysTick) with 24-bit down counter and automatic reload
- Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail chaining
- Interrupt groups for expanding the total interrupt sources, with jump index for low interrupt latency

8.2 Operating Modes

MSPM0L MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD, or a logic level match on certain IOs. RUN, SLEEP, STOP, and STANDBY modes also include several configurable policy options (for example, RUN.x) for balancing performance with power consumption.

To further balance performance and power consumption, MSPM0L devices implement two power domains: PD1 (for the CPU, memories, and high performance peripherals), and PD0 (for low speed, low power peripherals). PD1 is always powered in RUN and SLEEP modes, but is disabled in all other modes. PD0 is always powered in RUN, SLEEP, STOP, and STANDBY modes. PD1 and PD0 are both disabled in SHUTDOWN mode.

8.2.1 Functionality by Operating Mode

Supported functionality in each operating mode is given in [Table 8-1](#).

Functional key:

- **EN:** The function is enabled in the specified mode.
- **DIS:** The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT:** The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS:** The function is not automatically disabled in the specified mode, but its use is not supported.
- **OFF:** The function is fully powered off in the specified mode, and no configuration information is retained.

Table 8-1. Supported Functionality by Operating Mode

| Operating Mode | | RUN | | | SLEEP | | | STOP | | | STANDBY | | SHUTDOWN |
|----------------|--------|------|------|------|--------|--------|--------|--------------------|-------|-------|----------|----------|----------|
| | | RUN0 | RUN1 | RUN2 | SLEEP0 | SLEEP1 | SLEEP2 | STOP0 | STOP1 | STOP2 | STANDBY0 | STANDBY1 | |
| Oscillators | SYSOSC | EN | EN | DIS | EN | EN | DIS | OPT ⁽¹⁾ | EN | DIS | DIS | DIS | OFF |
| | LFOSC | EN | | | | | | | | | | | OFF |

Table 8-1. Supported Functionality by Operating Mode (continued)

| Operating Mode | | RUN | | | SLEEP | | | STOP | | | STANDBY | | SHUTDOWN |
|---------------------|-------------------|------------|----------------------|------|---------|----------------------|-------------------------|-------------------|-------------------------|----------------------|----------|------------------------|----------------|
| | | RUN0 | RUN1 | RUN2 | SLEEP0 | SLEEP1 | SLEEP2 | STOP0 | STOP1 | STOP2 | STANDBY0 | STANDBY1 | |
| Clocks | CPUCLK | 32M | 32k | 32k | DIS | | | | | | | | OFF |
| | MCLK to PD1 | 32M | 32k | 32k | 32M | 32k | 32k | DIS | | | | | OFF |
| | ULPCLK to PD0 | 32M | 32k | 32k | 32M | 32k | 32k | 4M ⁽¹⁾ | 4M | 32k | | DIS | OFF |
| | ULPCLK to TIMG0/1 | 32M | 32k | 32k | 32M | 32k | 32k | 4M ⁽¹⁾ | 4M | 32k | | | OFF |
| | MFCLK | OPT | DIS | | OPT | DIS | | OPT | | DIS | | | OFF |
| | LFCLK | 32k | | | | | | | | | | DIS | OFF |
| | LFCLK to TIMG0/1 | 32k | | | | | | | | | | | OFF |
| | MCLK Monitor | OPT | | | | | | | | | | DIS | OFF |
| PMU | POR Monitor | EN | | | | | | | | | | | |
| | BOR Monitor | EN | | | | | | | | | | | OFF |
| | Core Regulator | FULL DRIVE | | | | | REDUCED DRIVE | | | LOW DRIVE | | | OFF |
| Core Functions | CPU | EN | | | DIS | | | | | | | | OFF |
| | DMA | OPT | | | | | NS (triggers supported) | | | | | OFF | |
| | Flash | EN | | | | | DIS | | | | | OFF | |
| | SRAM | EN | | | | | DIS | | | | | OFF | |
| PD1 Peripherals | SPI0 | OPT | | | | | DIS | | | | | OFF | |
| | CRC | OPT | | | | | DIS | | | | | OFF | |
| PD0 Peripherals | TIMG0/1 | OPT | | | | | | | | | | | OFF |
| | TIMG2/4 | OPT | | | | | | | | | | OPT ⁽²⁾ | OFF |
| | UART0/1 | OPT | | | | | | | | | | OPT ⁽²⁾ | OFF |
| | I2C0/1 | OPT | | | | | | | | | | OPT ⁽²⁾ | OFF |
| | GPIOA | OPT | | | | | | | | | | OPT ⁽²⁾ | OFF |
| | WWDT0 | OPT | | | | | | | | | | DIS | OFF |
| Analog | ADC0 | OPT | | | | | | | NS (triggers supported) | | | | OFF |
| | OPA0/1 | OPT | NS | | OPT | NS | | OPT | | NS | | OFF | |
| | GPAMP | OPT | | | | | | | | | | | OFF |
| | COMP0 | OPT | OPT _(ULP) | | OPT | OPT _(ULP) | | OPT | | OPT _(ULP) | | OFF | |
| IOMUX and IO Wakeup | | EN | | | | | | | | | | | DIS w/ WAKE |
| Wake Sources | | N/A | | | ANY IRQ | | | PD0 IRQ | | | | IOMUX, NRST, SWD | |

- (1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as in RUN1 and ULPCLK remains at 32 kHz as in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as in RUN2 and ULPCLK remains at 32 kHz as in RUN2.
- (2) When using the STANDBY1 policy for STANDBY, only TIMG0 and TIMG1 are clocked. Other PD0 peripherals can generate an asynchronous fast clock request upon external activity but are not actively clocked.

8.3 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brownout reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY operating modes to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.4 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32 kHz)
- **SYSOSC**: Internal high-frequency oscillator (4 MHz or 32 MHz with factory trim, 16 MHz or 24 MHz with user trim)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals, derived from SYSOSC or LFCLK, active in RUN and SLEEP modes
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4-MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- **LFCLK**: 32-kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **ADCCLK**: ADC clock, available in RUN, SLEEP and STOP modes
- **CLK_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes

For more details, see the CKM chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.5 DMA

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA in these devices support the following key features:

- 3 independent DMA transfer channels
 - 1 full-feature channel (DMA0), supporting repeated transfer modes
 - 2 basic channels (DMA1, DMA2), supporting single transfer modes
- Configurable DMA channel priorities
- Byte (8-bit), short word (16-bit), word (32-bit) and long word (64-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon completion of activity on another channel
- Stride mode to support data re-organization

Table 8-2 lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

Table 8-2. DMA Trigger Mapping

| TRIGGER 0:6 | SOURCE | TRIGGER 7:13 | SOURCE |
|-------------|----------|--------------|------------------|
| 0 | Software | 7 | I2C1 Publisher 2 |

Table 8-2. DMA Trigger Mapping (continued)

| TRIGGER 0:6 | SOURCE | TRIGGER 7:13 | SOURCE |
|-------------|-------------------------------|--------------|-------------------|
| 1 | Generic Subscriber 0 (FSUB_0) | 8 | SPI0 Publisher 1 |
| 2 | Generic Subscriber 1 (FSUB_1) | 9 | SPI0 Publisher 2 |
| 3 | ADC0 Publisher 2 | 10 | UART0 Publisher 1 |
| 4 | I2C0 Publisher 1 | 11 | UART0 Publisher 2 |
| 5 | I2C0 Publisher 2 | 12 | UART1 Publisher 1 |
| 6 | I2C1 Publisher 1 | 13 | UART1 Publisher 2 |

8.6 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) that are interconnected through an event fabric containing a combination of static and programmable routes.

Events that are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
 - Example: GPIO interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
 - Example: UART data receive trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)
 - Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

For more details, see the Event chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

Table 8-3. Generic Event Channels

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish the event to another entity (or entities, in the case of a splitter route). An entity can be another peripheral, a generic DMA trigger event, or a generic CPU event.

| CHANID | Generic Route Channel Selection | Channel Type |
|--------|-----------------------------------|------------------|
| 0 | No generic event channel selected | N/A |
| 1 | Generic event channel 1 selected | 1 : 1 |
| 2 | Generic event channel 2 selected | 1 : 1 |
| 3 | Generic event channel 3 selected | 1 : 2 (splitter) |

8.7 Memory

8.7.1 Memory Organization

The following table summarizes the memory map of the devices. For more information about the memory region detail, see the [Platform Memory Map](#) chapter in the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

Table 8-4. Memory Organization

| Memory Region | Subregion | MSPM0L1304, MSPM0L1344 | MSPM0L1305, MSPM0L1345 | MSPM0L1306, MSPM0L1346 |
|---------------|---------------------------------|--|---|---|
| Code (Flash) | MAIN ⁽³⁾ | 16KB - 8B 0x0000.0000 to 0x0000.3FF8 | 32KB - 8B ⁽¹⁾ 0x0000.0000 to 0x0000.7FF8 | 64KB - 8B ⁽¹⁾ 0x0000.0000 to 0x0000.FFF8 |
| | Aliased MAIN ^{(2) (3)} | 0x0040.0000 to 0x0040.3FF8 | 0x0040.0000 to 0x0040.7FF8 | 0x0040.0000 to 0x0040.FFF8 |

Table 8-4. Memory Organization (continued)

| Memory Region | Subregion | MSPM0L1304, MSPM0L1344 | MSPM0L1305, MSPM0L1345 | MSPM0L1306, MSPM0L1346 |
|---------------|---------------------------------|--|--|--|
| SRAM (SRAM) | SRAM | 2KB 0x2000.0000 to 0x2000.0800 | 4KB 0x2000.0000 to 0x2000.1000 | 4KB 0x2000.0000 to 0x2000.1000 |
| | Aliased SRAM ⁽²⁾ | 0x2000.0000 to 0x2000.0800 | 0x2000.0000 to 0x2000.1000 | 0x2000.0000 to 0x2000.1000 |
| Peripheral | Peripherals | 0x4000.0000 to 0x40FF.FFFF | 0x4000.0000 to 0x40FF.FFFF | 0x4000.0000 to 0x40FF.FFFF |
| | MAIN ⁽³⁾ | 0x0000.0000 to 0x0000.3FF8 | 0x0000.0000 to 0x0000.7FF8 | 0x0000.0000 to 0x0000.FFF8 |
| | Aliased MAIN ^{(2) (3)} | 0x0040.0000 to 0x0040.3FF8 | 0x0040.0000 to 0x0040.7FF8 | 0x0040.0000 to 0x0040.FFF8 |
| | NONMAIN | 512 bytes 0x41C0.0000 to 0x41C0.0200 | 512 bytes 0x41C0.0000 to 0x41C0.0200 | 512 bytes 0x41C0.0000 to 0x41C0.0200 |
| | Aliased NONMAIN ⁽²⁾ | 0x41C1.0000 to 0x41C1.0200 | 0x41C1.0000 to 0x41C1.0200 | 0x41C1.0000 to 0x41C1.0200 |
| | FACTORY | 0x41C4.0000 to 0x41C4.0080 | 0x41C4.0000 to 0x41C4.0080 | 0x41C4.0000 to 0x41C4.0080 |
| | Aliased FACTORY ⁽²⁾ | 0x41C5.0000 to 0x41C5.0080 | 0x41C5.0000 to 0x41C5.0080 | 0x41C5.0000 to 0x41C5.0080 |
| Subsystem | | 0x6000.0000 to 0x7FFF.FFFF | 0x6000.0000 to 0x7FFF.FFFF | 0x6000.0000 to 0x7FFF.FFFF |
| System PPB | | 0xE000.0000 to 0xE00F.FFFF | 0xE000.0000 to 0xE00F.FFFF | 0xE000.0000 to 0xE00F.FFFF |

- (1) First 32KB flash memory (address 0x0000.0000 to 0x0000.8000) has up to 100000 program and erase cycles.
- (2) Aliased memory reads the same as the corresponding memory region. Aliased memory is included to keep the compatibility with devices that have ECC.
- (3) CPU access to one of the last 8 bytes of a flash region will cause a hard fault. This occurs because the prefetch logic tries to read one flash word (64 bits) ahead, resulting in a read attempt to an invalid memory location.

8.7.2 Peripheral File Map

Table 8-5 lists the available peripherals and the register base address for each.

Table 8-5. Peripherals Summary

| Peripheral Name | Base Address | Size |
|-----------------|--------------|--------|
| ADC0 | 0x40004000 | 0x2000 |
| COMP0 | 0x40008000 | 0x2000 |
| OPA0 | 0x40020000 | 0x2000 |
| OPA1 | 0x40022000 | 0x2000 |
| VREF | 0x40030000 | 0x2000 |
| WWDT0 | 0x40080000 | 0x2000 |
| TIMG0 | 0x40084000 | 0x2000 |
| TIMG1 | 0x40086000 | 0x2000 |
| TIMG2 | 0x40088000 | 0x2000 |
| TIMG4 | 0x4008C000 | 0x2000 |
| GPIO0 | 0x400A0000 | 0x2000 |
| SYSCTL | 0x400AF000 | 0x3000 |
| DEBUGSS | 0x400C7000 | 0x2000 |
| EVENT | 0x400C9000 | 0x3000 |
| NVMNW | 0x400CD000 | 0x2000 |

Table 8-5. Peripherals Summary (continued)

| Peripheral Name | Base Address | Size |
|---------------------|--------------|--------|
| I2C0 | 0x400F0000 | 0x2000 |
| I2C1 | 0x400F2000 | 0x2000 |
| UART1 | 0x40100000 | 0x2000 |
| UART0 | 0x40108000 | 0x2000 |
| MCPUSS | 0x40400000 | 0x2000 |
| WUC | 0x40424000 | 0x1000 |
| IOMUX | 0x40428000 | 0x2000 |
| DMA | 0x4042A000 | 0x2000 |
| CRC | 0x40440000 | 0x2000 |
| SPI0 | 0x40468000 | 0x2000 |
| ADC0 ⁽¹⁾ | 0x4055A000 | 0x1000 |

⁽¹⁾ Aliased region of ADC0 memory-mapped registers.

8.7.3 Peripheral Interrupt Vector

Table 8-6 shows the IRQ number and the interrupt group number for each peripherals in this device.

Table 8-6. Interrupt Vector Number

| Peripheral Name | NVIC IRQ | Group IIDX |
|-----------------|----------|------------|
| WWDT0 | 0 | 0 |
| DEBUGSS | 0 | 2 |
| NVMNW | 0 | 3 |
| EVENT SUB PORT0 | 0 | 4 |
| EVENT SUB PORT1 | 0 | 5 |
| SYSCTL | 0 | 6 |
| GPIO0 | 1 | 0 |
| COMP0 | 1 | 2 |
| TIMG1 | 2 | – |
| ADC | 4 | – |
| SPI0 | 9 | – |
| UART1 | 13 | – |
| UART0 | 15 | – |
| TIMG0 | 16 | – |
| TIMG2 | 18 | – |
| TIMG4 | 20 | – |
| I2C0 | 24 | – |
| I2C1 | 25 | – |
| DMA | 31 | – |

8.8 Flash Memory

A single bank of nonvolatile flash memory is provided for storing executable program code and application data.

Key features of the flash include:

- In-circuit program and erase operations supported across the entire recommended supply range
- Small 1KB sector sizes (minimum erase resolution of 1KB)

- Up to 100000 program and erase cycles on the lower 32KB of the flash memory, with up to 10000 program and erase cycles on the remaining flash memory (devices with 32KB or less support 100000 cycles on the entire flash memory)

For a complete description of the flash memory, see the NVM chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.9 SRAM

MSPM0Lxx MCUs include a low-power high-performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code. The SRAM memory content is fully retained in run, sleep, stop, and standby operating modes and is lost in shutdown mode. A write protection mechanism is provided to allow the application to prevent unintended modifications to a portion of the SRAM memory. SRAM write protection is useful when placing executable code into SRAM to provide a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption.

8.10 GPIO

The general purpose input/output (GPIO) peripheral lets the application write data out and read data in through the device pins. Through the use of the Port A GPIO peripheral, these devices support up to 28 GPIO pins.

The key features of the GPIO module include:

- 0 wait state MMR access from CPU
- Set, clear, or toggle multiple bits without the need of a read-modify-write construct in software
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port
- User controlled input filtering

8.11 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO pad configuration registers allow for programmable drive strength, speed, pullup or pulldown, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.12 ADC

The 12-bit analog-to-digital converter (ADC) module in these devices support fast 12-bit conversions with single-ended inputs.

ADC features include:

- 12-bit output resolution at up to 1.68 Msps with greater than 11-bit ENOB
- HW averaging enables 14-bit conversion resolution at 105ksps
- Up to 10 external input channels
- Internal channels for temperature sensing, supply monitoring, and analog signal chain (interconnection with OPA, GPAMP, and others)
- Software selectable reference:
 - Configurable internal dedicated ADC reference voltage of 1.4 V and 2.5 V (VREF)
 - MCU supply voltage (VDD)
 - External reference supplied to the ADC through the VREF+ and VREF- pins
- Operates in RUN, SLEEP, and STOP modes and supports triggers from STANDBY mode

Table 8-7. ADC0 Channel Mapping

| CHANNEL[0:7] | SIGNAL NAME | CHANNEL[8:15] | SIGNAL NAME ^{(1) (2)} |
|--------------|-------------|---------------|--------------------------------|
| 0 | A0 | 8 | A8 |
| 1 | A1 | 9 | A9 |
| 2 | A2 | 10 | – |
| 3 | A3 | 11 | <i>Temperature Sensor</i> |
| 4 | A4 | 12 | <i>OPA0 output</i> |
| 5 | A5 | 13 | <i>OPA1 output</i> |
| 6 | A6 | 14 | <i>GPAMP output</i> |
| 7 | A7 | 15 | <i>Supply/Battery Monitor</i> |

- (1) *Italicized* signal names are internal to the SoC. These signals are used for internal peripheral interconnections.
- (2) For more information about device analog connections see [Section 8.24](#).

For more details, see the ADC chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.13 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with VDD = 3.3V at the factory trim temperature (T_{TRIM}). The ADC and VREF configuration for the above measurement is as the following: RES=0 (12-bit mode), VRSEL=0h (VDD), ADC t_{sample}=12.5μs. This calibration value can be used with the temperature sensor temperature coefficient (T_{S_c}) to estimate the device temperature. See the temperature sensor section of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#) for guidance on estimating the device temperature with the factory trim value.

8.14 VREF

The voltage reference module (VREF) in these devices contains a configurable voltage reference buffer dedicated for the on-board ADC. The devices also support connection of an external reference for applications in which higher accuracy is required.

VREF features include:

- 1.4-V and 2.5-V user-selectable internal reference for ADC
- Internal reference supports ADC operation up to 200 ksp/s
- Support for bringing in an external reference for the ADC as well as for other analog peripherals on the VREF+ and VREF- device pins (24, 28, and 32-pin packages only)

For more details, see the VREF chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.15 COMP

The comparator peripheral in the device compares the voltage levels on two inputs terminals and provides a digital output based on this comparison. The COMP supports the following key features:

- Programmable hysteresis
- Programmable reference voltage:
 - Integrated 8-bit reference DAC, the output can also connect to OPA input terminal internally as an output buffer.
- Configurable operation modes:
 - High-speed mode (for the lowest propagation delay in timing-critical applications)

- Low-power mode (for monitoring slow-moving signals at the lowest power consumption)
- Programmable output glitch filter delay
- "Support output wake up device from all but the lowest low-power mode
- The IPSEL and IMSEL bits in comparator registers can be used to select the comparator channel inputs from device pins or from internal analog modules.

Table 8-8. COMP0 Input Channel Selection⁽¹⁾

| IPSEL / IMSEL Bits | Positive Terminal Input | Negative Terminal Input |
|--------------------|-------------------------|-------------------------|
| 0x0 | COMP0_IN0+ | COMP0_IN0- |
| 0x1 | COMP0_IN1+ | COMP0_IN1- |
| 0x6 | OPA1 output | OPA0 output |

(1) For more information about device analog connections, see [Section 8.24](#).

Table 8-9. COMP0 Blanking Source Table

| CTL2.BLANKSRC | Blanking Source Selected |
|---------------|--------------------------|
| 0x0 | Blanking source disabled |
| 0x1 | TIMG0.CC1 |
| 0x2 | TIMG1.CC1 |
| 0x3 | TIMG2.CC1 |

For more details, see the COMP chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.16 CRC

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for 32-bit CRC based on CRC32-ISO3309
- Support for bit reversal

For more details, see the CRC chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.17 GPAMP

The general-purpose amplifier (GPAMP) peripheral is a chopper-stabilized general-purpose operational amplifier with rail-to-rail input and output.

The GPAMP supports the following features:

- Software selectable chopper stabilization
- Rail-to-rail input and output
- Programmable internal unity gain feedback loop

For more details, see the ADC chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.18 OPA

The zero-drift op amps (OPAs) in these devices, OPA0 and OPA1, are chopper stabilized operational amplifiers with rail-to-rail input/output and a programmable gain stage feedback loop.

The OPA peripherals support the following key features:

- Software-selectable zero-drift chopper stabilization for improved accuracy and drift performance
- Factory trimming to remove offset error
- Burnout current source (BCS) integrated to monitor sensor health

- Programmable gain amplifier (PGA) up to 32x

The OPA features configurable input muxes P-MUX, N-MUX, and M-MUX to support various analog signal chain amplifier configurations that include general purpose, inverting, noninverting, unity gain, cascade, noninverting cascade, difference, and more. The following tables list the input channel mapping for each OPA.

For more information about device analog connections, see [Section 8.24](#)

For more details, see the OPA chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.19 I2C

The inter-integrated circuit interface (I²C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100 kbit/s
- Support Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Support Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
 - Supported on open drain IOs only (ODIO)
- Separated transmit and receive FIFOs support DMA data transfer
- Support SMBus 3.0 with PEC, ARP, timeout detection and host support
- Wakeup from low power mode on address match
- Support analog and digital glitch filter for input signal glitch suppression
- 8-entry transmit and receive FIFOs

For more details, see the I2C chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.20 SPI

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support ULPCLK/2 bit rate and up to 16Mbits/s in both controller and peripheral mode
- Configurable as a controller or a peripheral
- Configurable chip select for both controller and peripheral
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode) and 7 bits to 16 bit (peripheral mode)
- Supports PACKEN feature that allows the packing of 2 16 bit FIFO entries into a 32-bit value to improve CPU performance
- Transmit and receive FIFOs (4 entries each with 16 bits per entry) supporting DMA data transfer
- Supports TI mode, Motorola mode and National Microwire format

For more details, see the SPI chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.21 UART

The UART peripherals provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
 - 5, 6, 7 or 8 data bits
 - Even, odd, stick, or no-parity bit generation and detection
 - 1 or 2 stop bit generation
 - Line-break detection
 - Glitch filter on the input signals

- Programmable baud rate generation with oversampling by 16, 8 or 3
- Local Interconnect Network (LIN) mode support
- Separated transmit and receive FIFOs support DAM data transfer
- Support transmit and receive loopback mode operation
- See [Table 8-10](#) for detail information on supported protocols

Table 8-10. UART Features

| UART Features | UART0 (Extend) | UART1 (Main) |
|-------------------------------------|----------------|--------------|
| Active in Stop and Standby Mode | Yes | Yes |
| Separate transmit and receive FIFOs | Yes | Yes |
| Support hardware flow control | Yes | Yes |
| Support 9-bit configuration | Yes | Yes |
| Support LIN mode | Yes | - |
| Support DALI | Yes | - |
| Support IrDA | Yes | - |
| Support ISO7816 Smart Card | Yes | - |
| Support Manchester coding | Yes | - |
| FIFO Depth | 4 entries | 4 entries |

For more details, see the UART chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.22 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.23 Timers (TIMx)

The timer peripherals in these devices support the following key features. For specific configuration, see [Table 8-11](#).

Specific features for the **general-purpose timer (TIMGx)** include:

- 16-bit timers with up, down or up-down counting modes, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent channels for
 - Output compare
 - Input capture
 - PWM output
 - One-shot mode
- Support quadrature encoder interface (QEI) for positioning and movement sensing
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt/DMA trigger generation and cross peripherals (such as ADC) trigger capability

- Cross-trigger event logic for Hall sensor inputs

Table 8-11. Different TIMG Configurations

| TIM Name | Power Domain | Resolution | Prescaler | Capture/ Compare Channels | External PWM Channels | Phase Load | Shadow Load | Shadow CC |
|----------|--------------|------------|-----------|---------------------------|-----------------------|------------|-------------|-----------|
| TIMG0 | PD0 | 16-bit | 8-bit | 2 | 2 | - | - | - |
| TIMG1 | PD0 | 16-bit | 8-bit | 2 | 2 | - | - | - |
| TIMG2 | PD0 | 16-bit | 8-bit | 2 | 2 | - | - | - |
| TIMG4 | PD0 | 16-bit | 8-bit | 2 | 2 | - | Yes | Yes |

Table 8-12. TIMG Cross Trigger Map

| TSEL.ETSEL Selection | TIMG0 | TIMG1 | TIMG2 | TIMG4 |
|----------------------|---------------------------------|-------------|-------------|-------------|
| 0 | TIMG0.TRIG0 | TIMG0.TRIG0 | TIMG0.TRIG0 | TIMG0.TRIG0 |
| 1 | TIMG1.TRIG0 | TIMG1.TRIG0 | TIMG1.TRIG0 | TIMG1.TRIG0 |
| 2 | TIMG2.TRIG0 | TIMG2.TRIG0 | TIMG2.TRIG0 | TIMG2.TRIG0 |
| 3 | TIMG4.TRIG0 | TIMG4.TRIG0 | TIMG4.TRIG0 | TIMG4.TRIG0 |
| 4 to 15 | Reserved | | | |
| 16 | Event Subscriber Port 0 (FSUB0) | | | |
| 17 | Event Subscriber Port 1 (FSUB1) | | | |
| 18to 31 | Reserved | | | |

For more details, see the timer chapters of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.24 Device Analog Connections

Figure 8-1 shows the internal analog connection of the device.

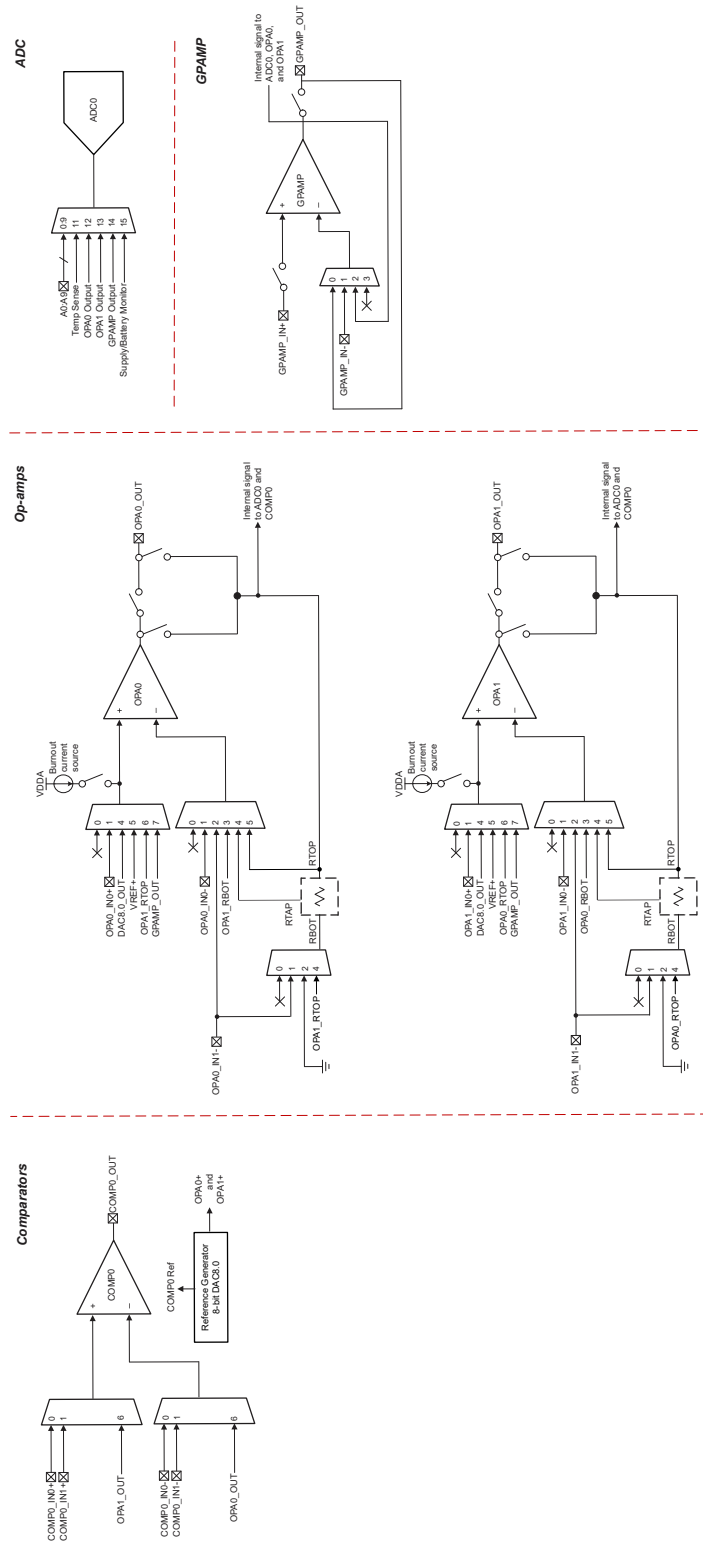


Figure 8-1. Analog Connections

8.25 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO and provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For

more information, see the IOMUX section of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 8-2. Not all pins have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the device-specific data sheet for detailed information on what features are supported for a specific pin.

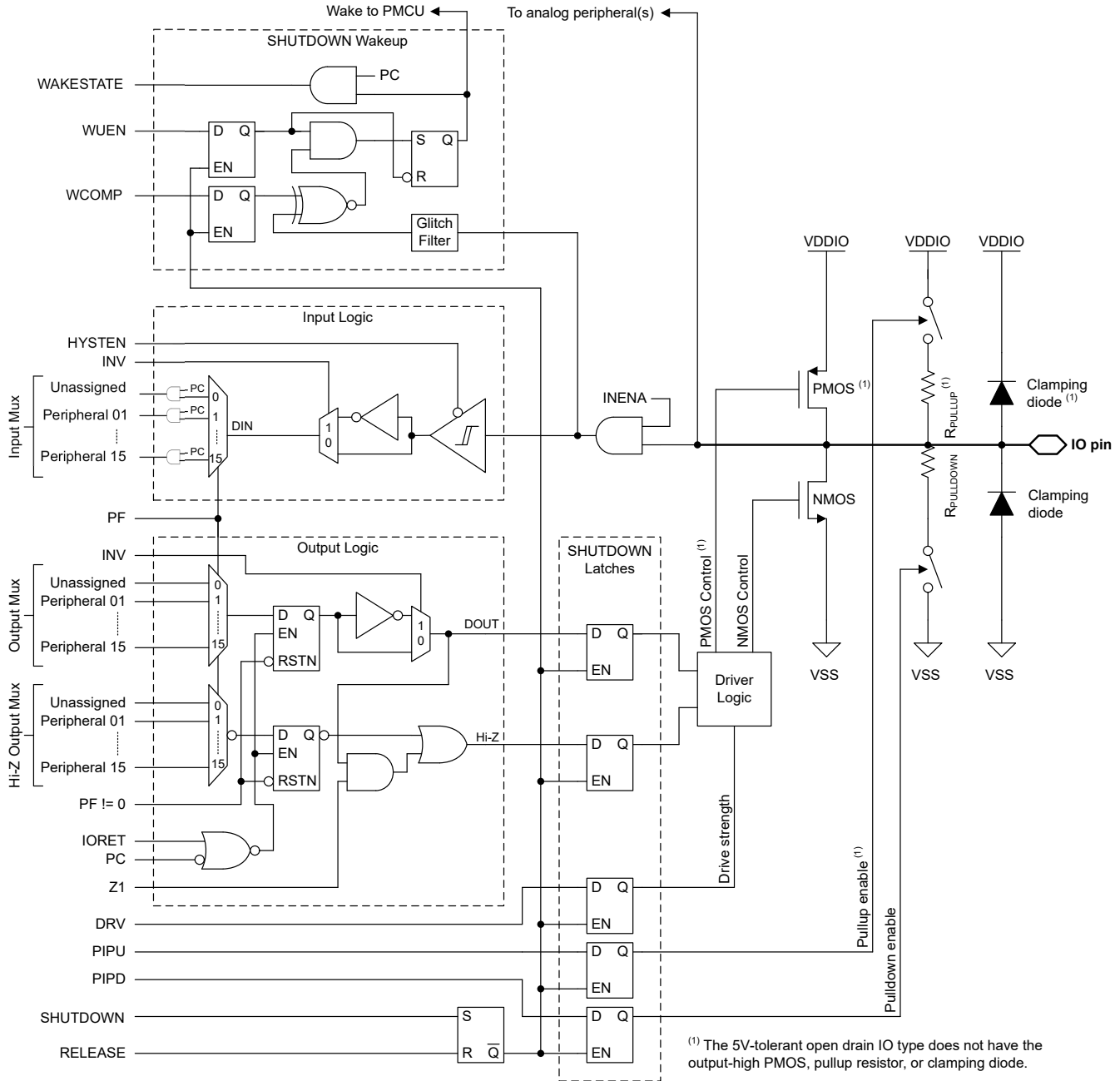


Figure 8-2. Superset Input/Output Diagram

8.26 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device. For a complete description of the debug functionality offered on MSPM0 devices, see the debug chapter of the technical reference manual.

Table 8-13. Serial Wire Debug Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | SWD FUNCTION |
|---------------|--------------|--|
| SWCLK | Input | Serial wire clock from debug probe |
| SWDIO | Input/Output | Bi-directional (shared) serial wire data |

8.27 Bootstrap Loader (BSL)

The bootstrap loader (BSL) enables configuration of the device as well as programming of the device memory through a UART or I2C serial interface. Access to the device memory and configuration through the BSL is protected by a 256-bit user-defined password, and it is possible to completely disable the BSL in the device configuration, if desired. The BSL is enabled by default from TI to support use of the BSL for production programming.

A minimum of two pins are required to use the BSL: the BSLRX and BSLTX signals (for UART), or the BSLSCL and BSLSDA signals (for I²C). Additionally, one or two additional pins (BSL_invoke and NRST) may be used for controlled invocation of the bootloader by an external host.

If enabled, the BSL may be invoked (started) in the following ways:

- The BSL is invoked during the boot process if the BSL_invoke pin state matches the defined BSL_invoke logic level. If the device fast boot mode is enabled, this invocation check is skipped. An external host can force the device into the BSL by asserting the invoke condition and applying a reset pulse to the NRST pin to trigger a BOOTRST, after which the device will verify the invoke condition during the reboot process and start the BSL if the invoke condition matches the expected logic level.
- The BSL is automatically invoked during the boot process if the reset vector and stack pointer are left unprogrammed. As a result, a blank device from TI will invoke the BSL during the boot process without any need to provide a hardware invoke condition on the BSL_invoke pin. This enables production programming using just the serial interface signals.
- The BSL may be invoked at runtime from application software by issuing a SYSRST with BSL entry command.

Table 8-14. BSL Pin Requirements and Functions

| DEVICE SIGNAL | CONNECTION | BSL FUNCTION |
|---------------|-------------------|---|
| BSLRX | Required for UART | UART receive signal (RXD), an input |
| BSLTX | Required for UART | UART transmit signal (TXD) an output |
| BSLSCL | Required for I2C | I ² C BSL clock signal (SCL) |
| BSLSDA | Required for I2C | I ² C BSL data signal (SDA) |
| BSL_invoke | Optional | Active-high digital input used to start the BSL during boot |
| NRST | Optional | Active-low reset pin used to trigger a reset and subsequent check of the invoke signal (BSL_invoke) |

8.28 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Refer to the *Factory Constants* chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

Table 8-15. DEVICEID

DEVICEID address is 0x41C4.0004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

| DEVICE | DEVICEID.PARTNUM | DEVICEID.MANUFACTURER |
|------------------------|------------------|-----------------------|
| MSPM0L1304, MSPM0L1344 | 0xBB82 | 0x17 |
| MSPM0L1305, MSPM0L1345 | 0xBB82 | 0x17 |
| MSPM0L1306, MSPM0L1346 | 0xBB82 | 0x17 |

Table 8-16. USERID

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

| DEVICE | PART | VARIANT | DEVICE | PART | VARIANT |
|-------------------|--------|---------|-------------------|--------|---------|
| MSPM0L1306SRHBR | 0xBB70 | 0x3C | MSPM0L1304TDGS20R | 0xD717 | 0x33 |
| MSPM0L1306TRHBR | 0xBB70 | 0x52 | MSPM0L1304SDYYR | 0xD717 | 0xB7 |
| MSPM0L1306SDGS28R | 0xBB70 | 0x5 | MSPM0L1304TDYYR | 0xD717 | 0xF9 |
| MSPM0L1306TDGS28R | 0xBB70 | 0x63 | MSPM0L1305SRHBR | 0x4D03 | 0x2D |
| MSPM0L1306SRGER | 0xBB70 | 0x7F | MSPM0L1305TRHBR | 0x4D03 | 0x85 |
| MSPM0L1306TRGER | 0xBB70 | 0xAA | MSPM0L1305SDGS28R | 0x4D03 | 0x64 |
| MSPM0L1306SDGS20R | 0xBB70 | 0xF4 | MSPM0L1305TDGS28R | 0x4D03 | 0xFB |
| MSPM0L1306TDGS20R | 0xBB70 | 0xA | MSPM0L1305SRGER | 0x4D03 | 0x73 |
| MSPM0L1306SDYYR | 0xBB70 | 0xE | MSPM0L1305TRGER | 0x4D03 | 0xEA |
| MSPM0L1306TDYYR | 0xBB70 | 0x35 | MSPM0L1305SDGS20R | 0x4D03 | 0xC7 |
| MSPM0L1304SRHBR | 0xD717 | 0xE4 | MSPM0L1305TDGS20R | 0x4D03 | 0xA0 |
| MSPM0L1304TRHBR | 0xD717 | 0x5A | MSPM0L1305SDYYR | 0x4D03 | 0x91 |
| MSPM0L1304SDGS28R | 0xD717 | 0x73 | MSPM0L1305TDYYR | 0x4D03 | 0xDE |
| MSPM0L1304TDGS28R | 0xD717 | 0xA8 | MSPM0L1303SRGER | 0xEF0 | 0x17 |
| MSPM0L1304SRGER | 0xD717 | 0x26 | MSPM0L1303TRGER | 0xEF0 | 0xE2 |
| MSPM0L1304TRGER | 0xD717 | 0xB7 | MSPM0L1345TDGS28R | 0x98B4 | 0x74 |
| MSPM0L1304SDGS20R | 0xD717 | 0xFA | MSPM0L1344TDGS20R | 0x40B0 | 0xD0 |

8.29 Identification

Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region (see the Device Factory Constants section) which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. For more information, see the *Factory Constants* chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata describes these markings.

9 Applications, Implementation, and Layout

9.1 Typical Application

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1.1 Schematic

TI recommends connecting a combination of a 10- μF and a 0.1- μF low-ESR ceramic decoupling capacitor across the VDD and VSS pins, as well as placing these capacitors as close as possible to the supply pins that they decouple (within a few millimeters) to achieve a minimal loop area. The 10- μF bulk decoupling capacitor is a recommended value for most applications, but this capacitance may be adjusted if needed based upon the PCB design and application requirements. For example, larger bulk capacitors can be used, but this can affect the supply rail ramp-up time.

The NRST reset pin must be pulled up to VDD (supply level) for the device to release from RESET state and start the boot process. TI recommends connecting an external 47-k Ω pullup resistor with a 10-nF pulldown capacitor for most applications, enabling the NRST pin to be controlled by another device or a debug probe.

The SYSOSC frequency correction loop (FCL) circuit utilizes an external 100-k Ω with 0.1% tolerance resistor between the ROSC pin and VSS. This resistor establishes a reference current to stabilize the SYSOSC frequency through a correction loop. This resistor is required if the FCL feature is used for higher accuracy, and it is not required if the SYSOSC FCL is not enabled. When the FCL mode is not used, the PA2 pin may be used as a digital input/output pin.

A 0.47- μF tank capacitor is required for the VCORE pin and must be placed close to the device with minimum distance to the device ground. Do not connect other circuits to the VCORE pin.

For the 5-V-tolerant open drain (ODIO), a pullup resistor is required to output high for I2C and UART functions, as the open drain IO only implement a low-side NMOS driver and no high-side PMOS driver. The 5V-tolerant open drain IO are fail-safe and may have a voltage present even if VDD is not supplied.

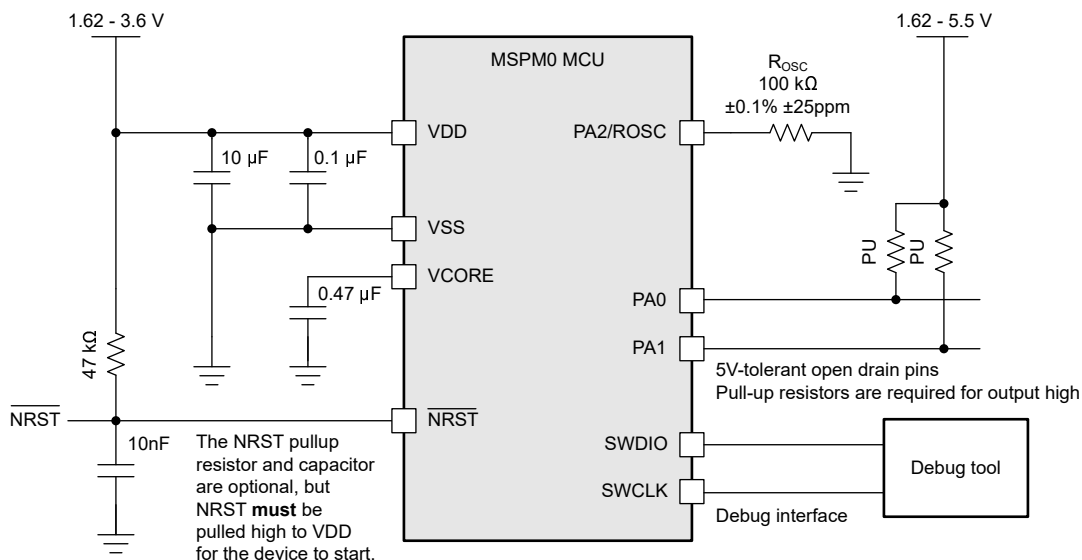


Figure 9-1. Basic Application Schematic

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X or XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

X and XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [Figure 10-1](#) provides a legend for reading the complete device name.

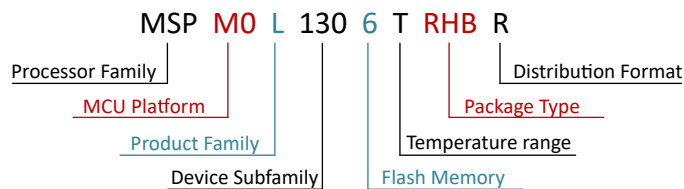


Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

| | |
|----------------------------|---|
| Processor Family | MSP = Mixed-signal processor X, XMS = Experimental silicon |
| MCU Platform | M0 = Arm-based 32-bit M0+ |
| Product Family | L = 32-MHz frequency |
| Device Subfamily | 130 = ADC, 2x OPA, COMP 134 = ADC, 2x OPA (10-pA input bias current), COMP |
| Internal Memory | 3 = 8KB flash, 2KB SRAM 4 = 16KB flash, 2KB SRAM 5 = 32KB flash, 4KB SRAM 6 = 64KB flash, 4KB SRAM |
| Temperature Range | T = -40°C to 105°C S = -40°C to 125°C |
| Package Type | See Section 5 and www.ti.com/packaging |
| Distribution Format | T = Small reel R = Large reel No marking = Tube or tray |

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

10.2 Tools and Software

Design Kits and Evaluation Modules

[MSPM0 LaunchPad Development Kit: LP-MSPM0L1306](#)

Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming, debugging, and EnergyTrace™ technology. The LaunchPad ecosystem includes dozens of [BoosterPack™](#) stackable plug-in modules to extend functionality.

Embedded Software

[MSPM0 Software Development Kit \(SDK\)](#)

Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

Software Development Tools

[TI Cloud Tools](#)

Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.

[TI Resource Explorer SysConfig](#)

Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.

Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE or in TI Cloud Tools. ([offline version](#))

[MSP Academy](#)

Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.

[GUI Composer](#)

GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

IDE and compiler tool chains

[Code Composer Studio™ \(CCS\)](#)

Includes [TI Arm-Clang](#) compiler. Supports all TI Arm Cortex MCUs and boasts competitive code size performance advantages, fast compile time, code coverage support, safety certification support, and completely free to use.

[IAR Embedded Workbench® IDE](#)

[Keil® MDK IDE](#)

[GNU Arm Embedded Tool Chain](#)

10.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the MSPM0 MCUs. Copies of these documents are available on the Internet at [www.ti.com](#).

Technical Reference Manual

[MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#)

This manual describes the modules and peripherals of the MSPM0L family of devices. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in their exact implementation on different

devices. Pin functions, internal signal connections, and operational parameters differ from device to device. See the device-specific data sheet for these details.

10.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.5 Trademarks

LaunchPad™, Code Composer Studio™, TI E2E™, EnergyTrace™, and BoosterPack™ are trademarks of Texas Instruments.

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10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|--------------|----------|---|
| January 2024 | D | <ul style="list-style-type: none"> Released WQFN16 package Improved wording of the descriptions Corrected the pinout issue for VSSOP28 TIA and WQFN16 Added the size of the pins for the leaded frame packages Added footnote for BOR in AMR table Added the specification for COMP settling time (static mode) Corrected the capacitor in Application schematics Changed the parameters for OPA PSRR and PGA Changed ADC minimum sampling time (without OPA) Corrected the temperature range for S version Changed the SPI low voltage Added the timer cross-trigger information Clarified for COMP and VBOOST testing condition Added a footnote for JEDEC J-STD-020 in AMR table Removed ADC-assisted CHOP in GPAMP |
| June 2023 | C | Released the MSPM0L134x devices |
| April 2023 | B | Production data release |
| January 2023 | A | Initial Public Release |

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

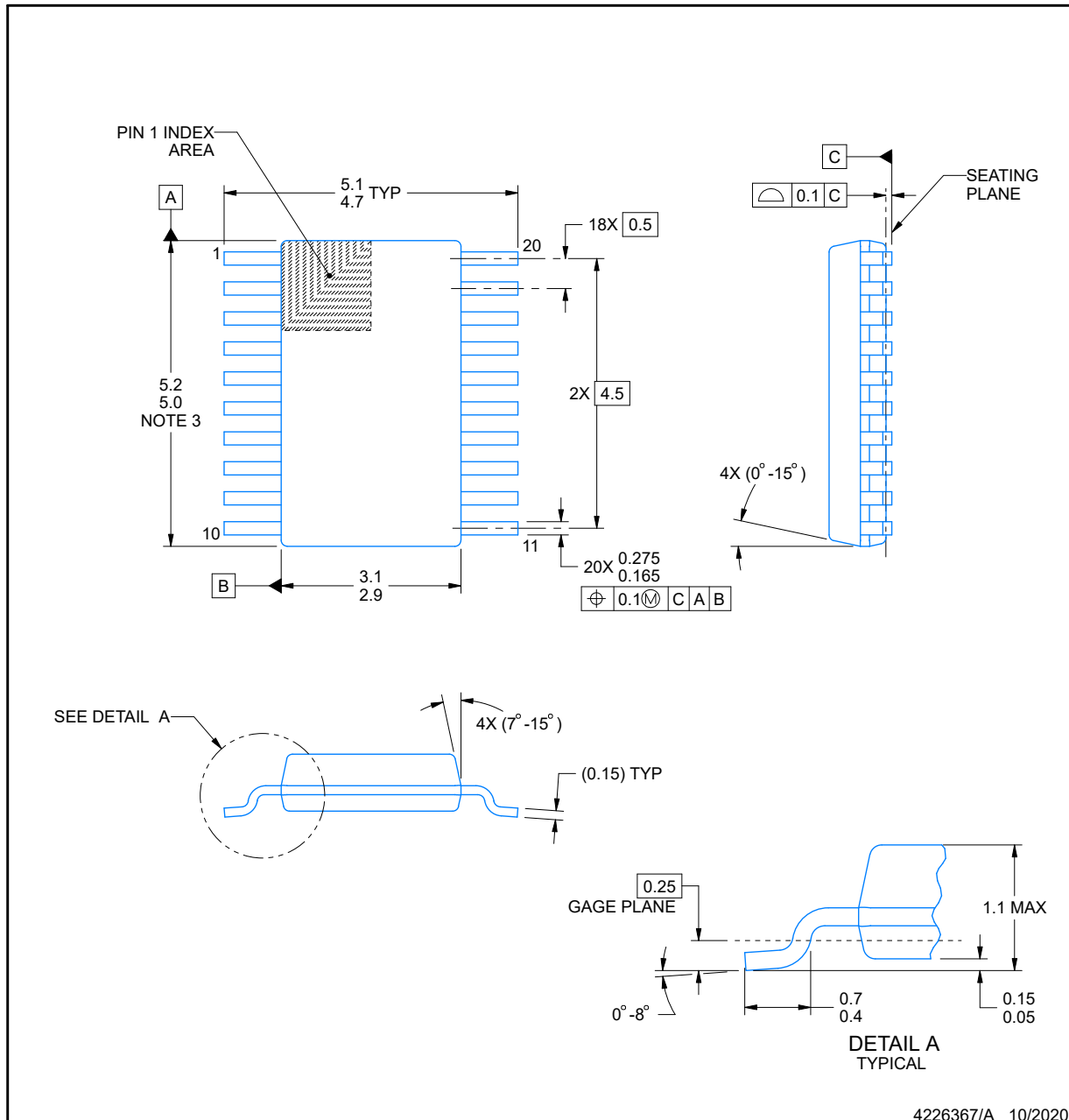
PACKAGE OUTLINE

DGS0020A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

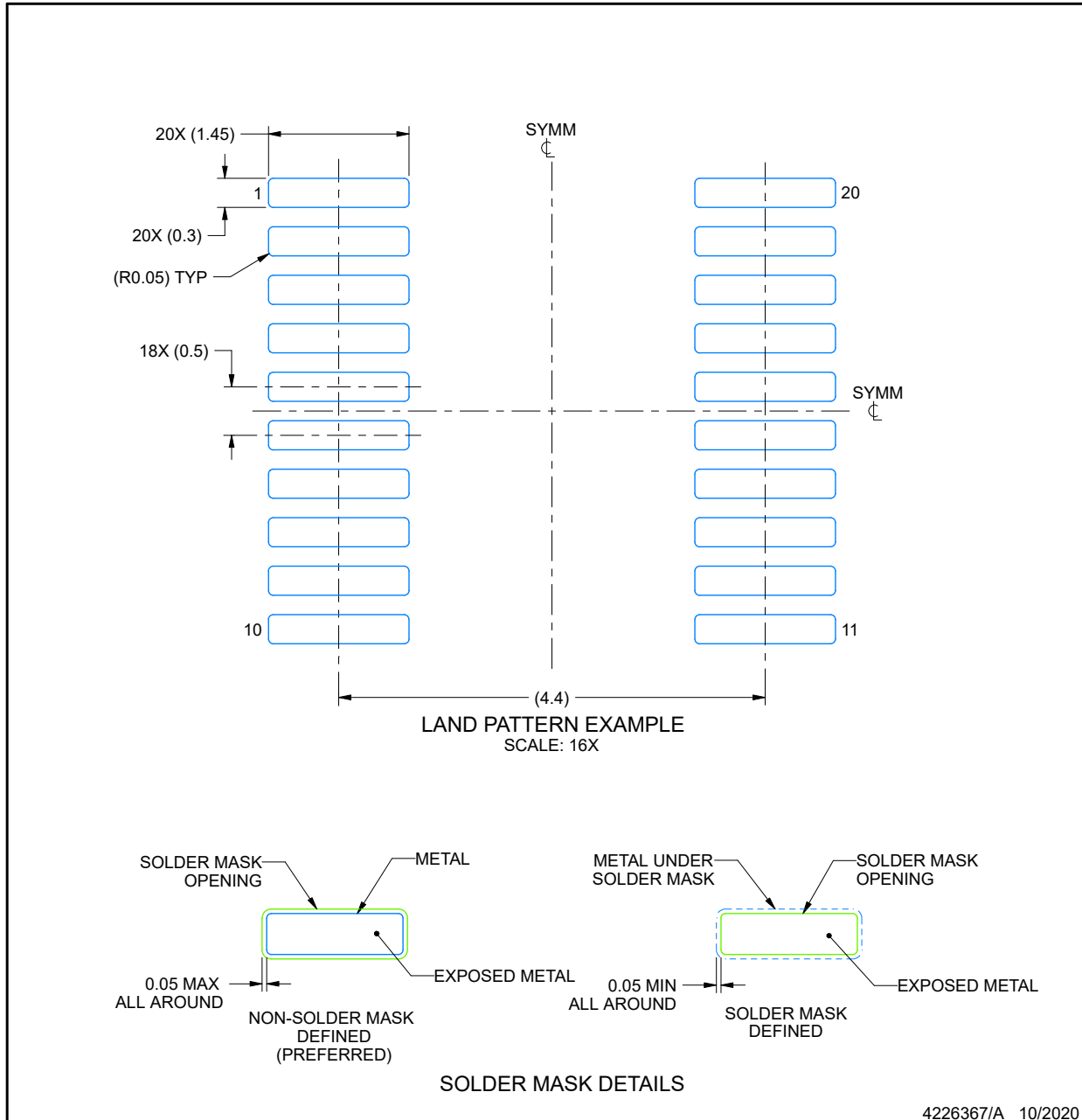
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

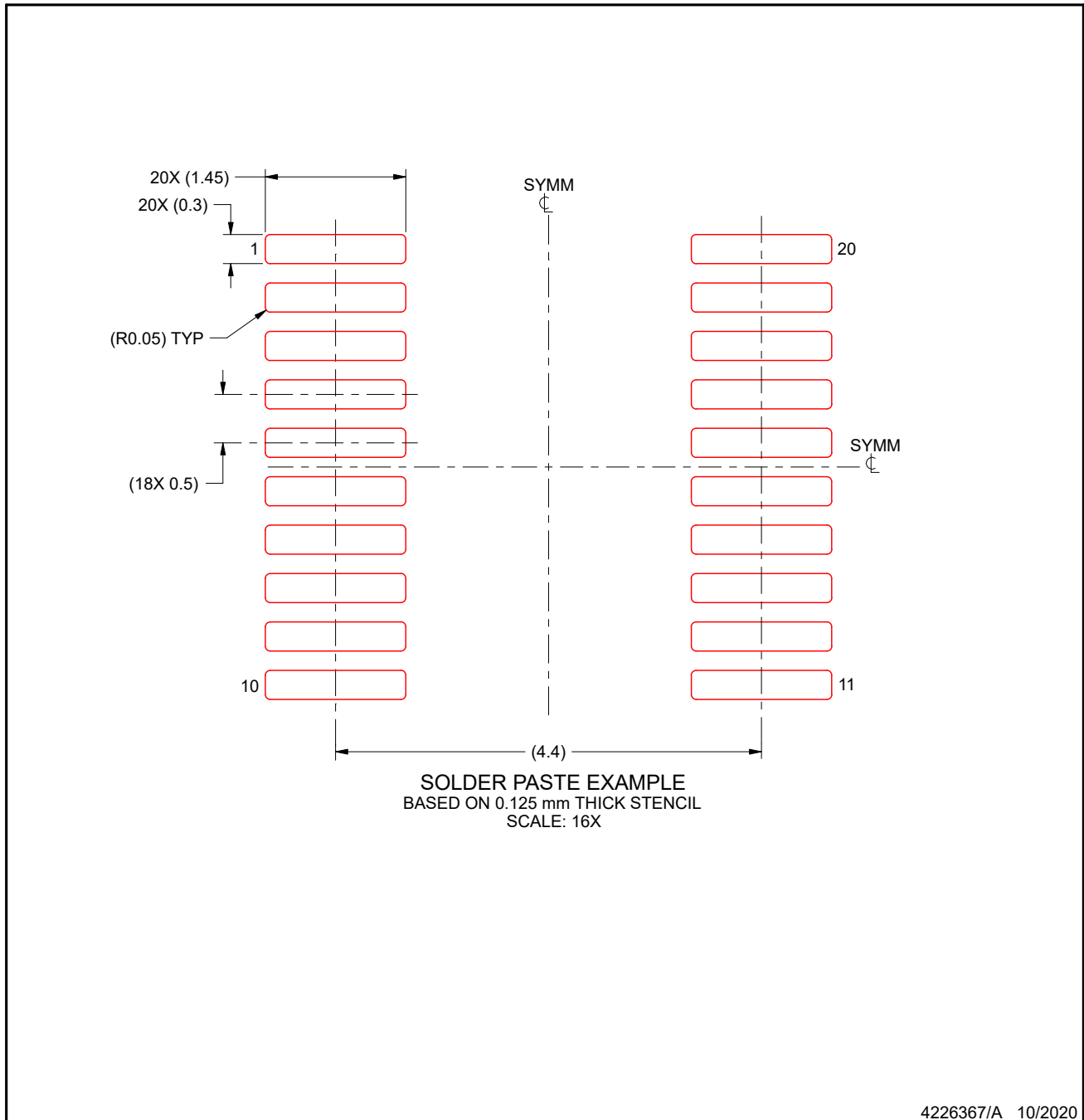
- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- Size of metal pad may vary due to creepage requirement.
- Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0020A

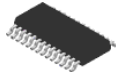
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



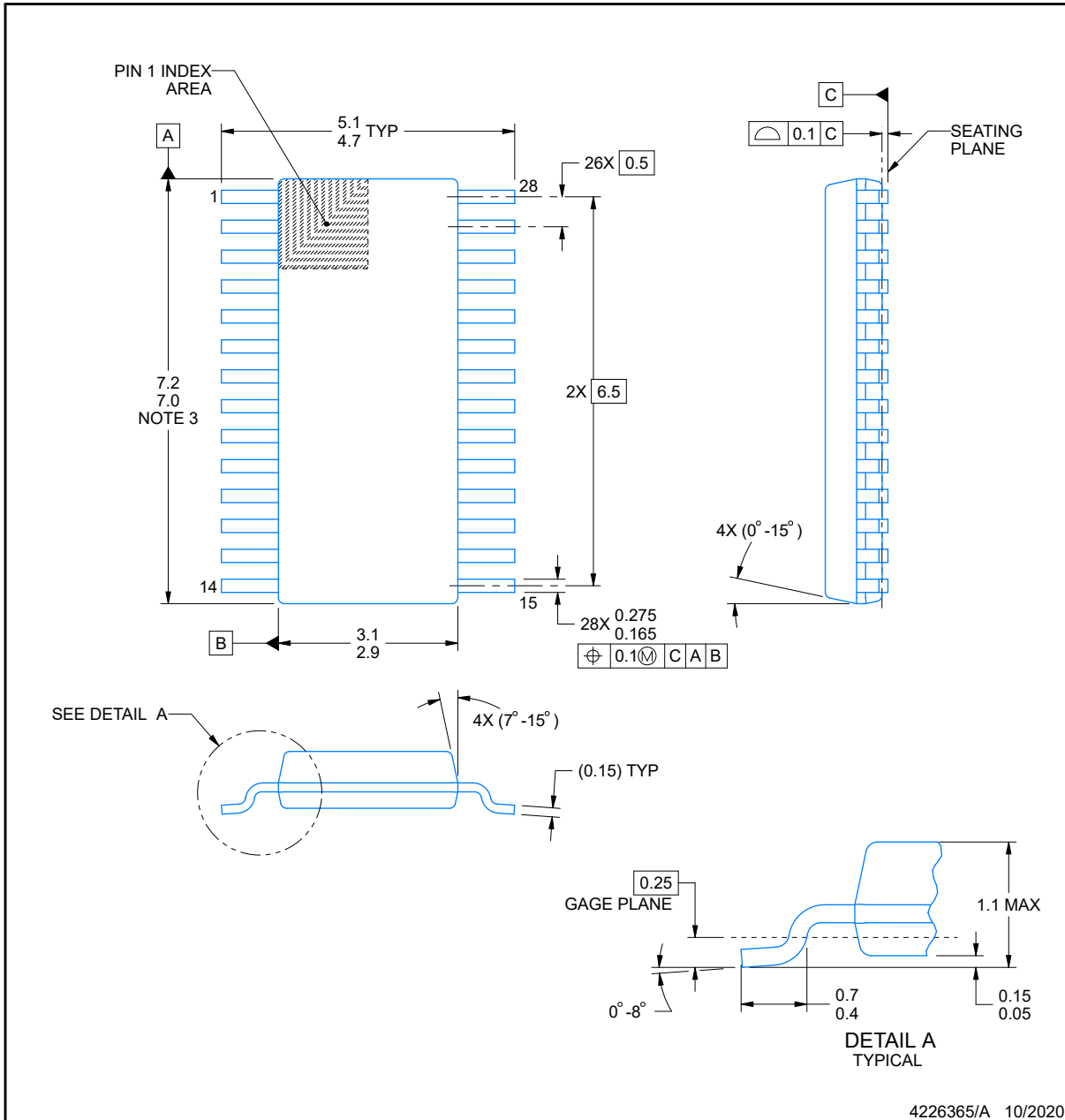
NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.



DGS0028A

PACKAGE OUTLINE
VSSOP - 1.1 mm max height
SMALL OUTLINE PACKAGE



4226365/A 10/2020

NOTES:

PowerPAD is a trademark of Texas Instruments.

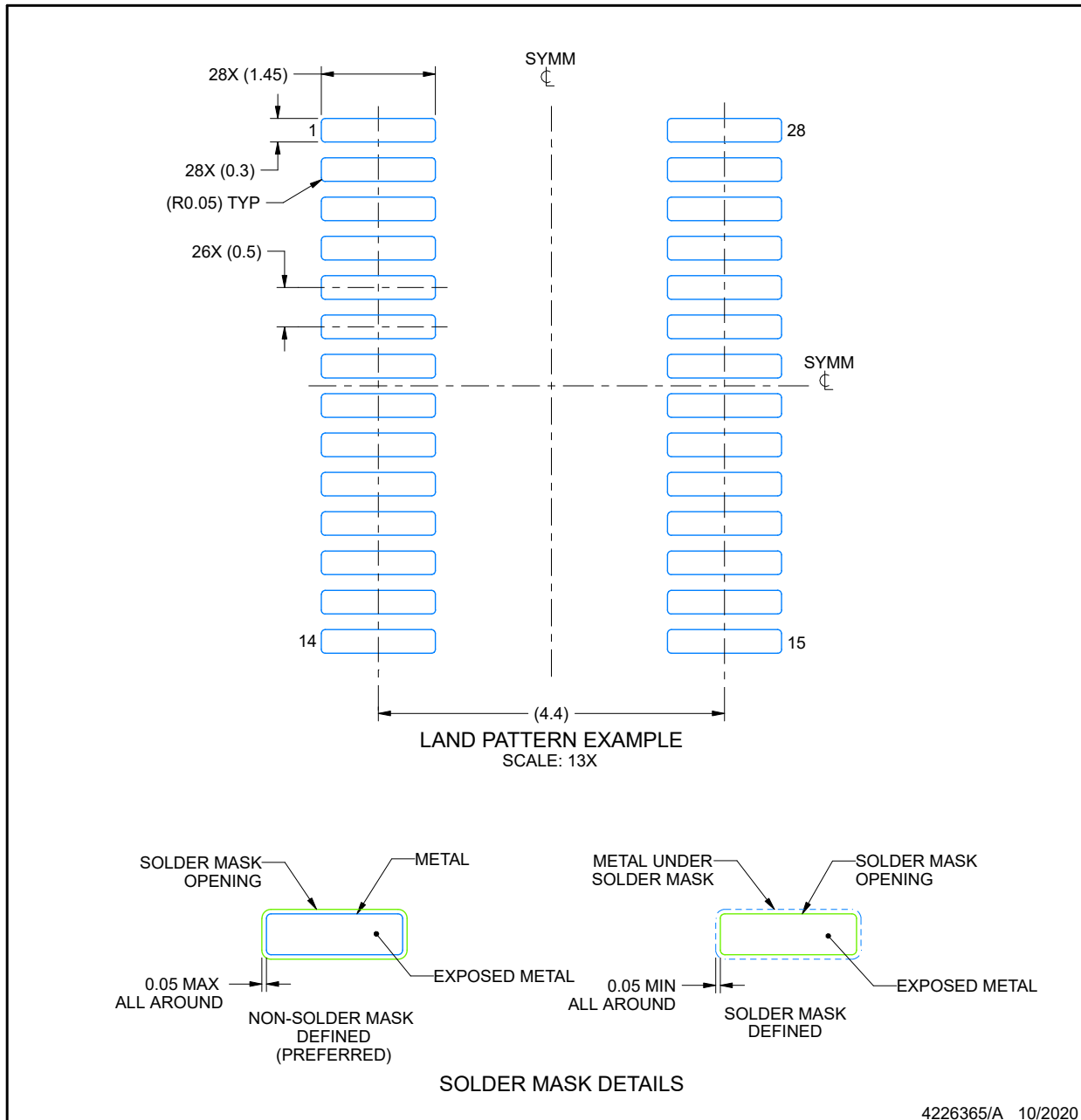
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226365/A 10/2020

NOTES: (continued)

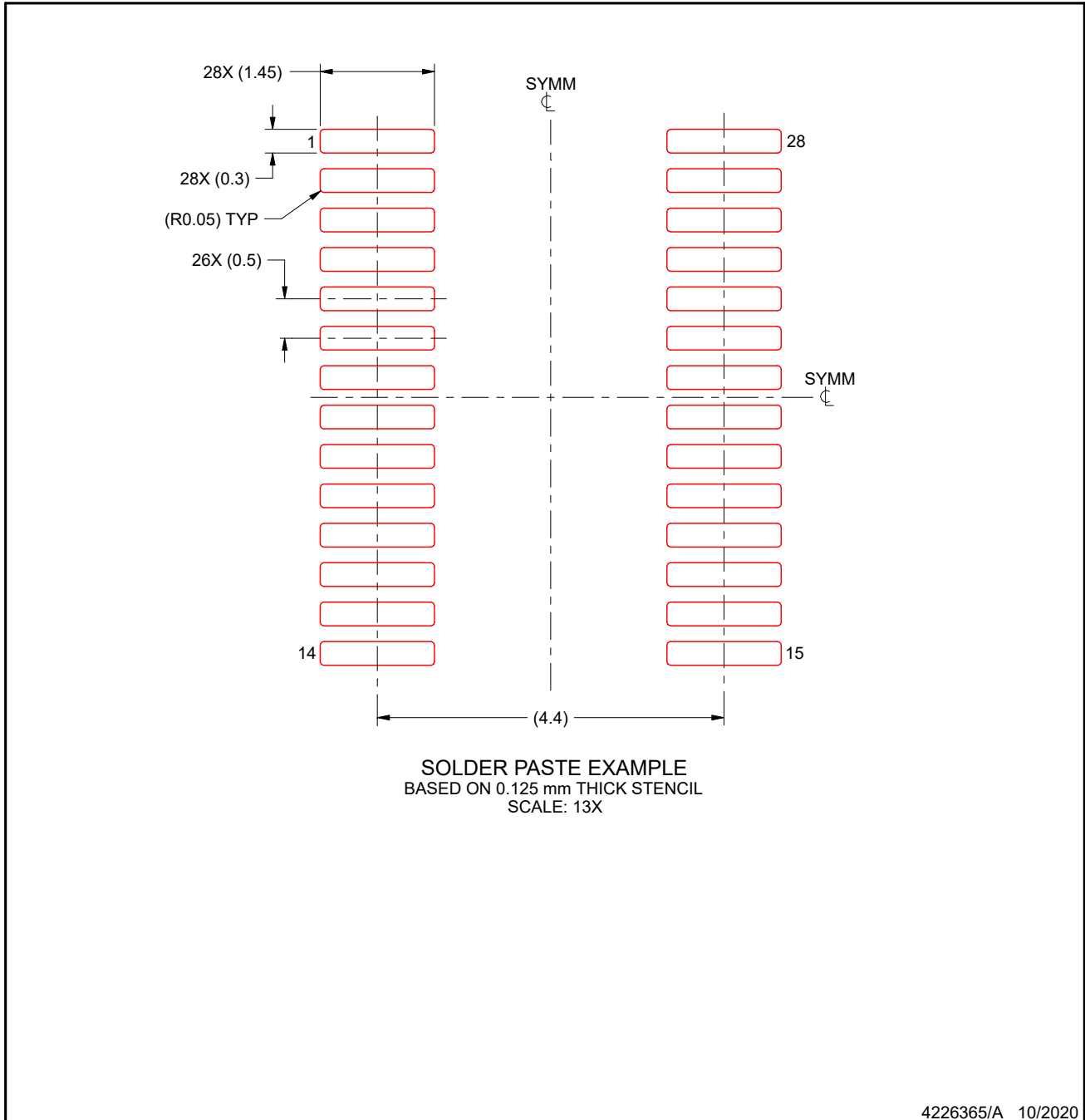
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

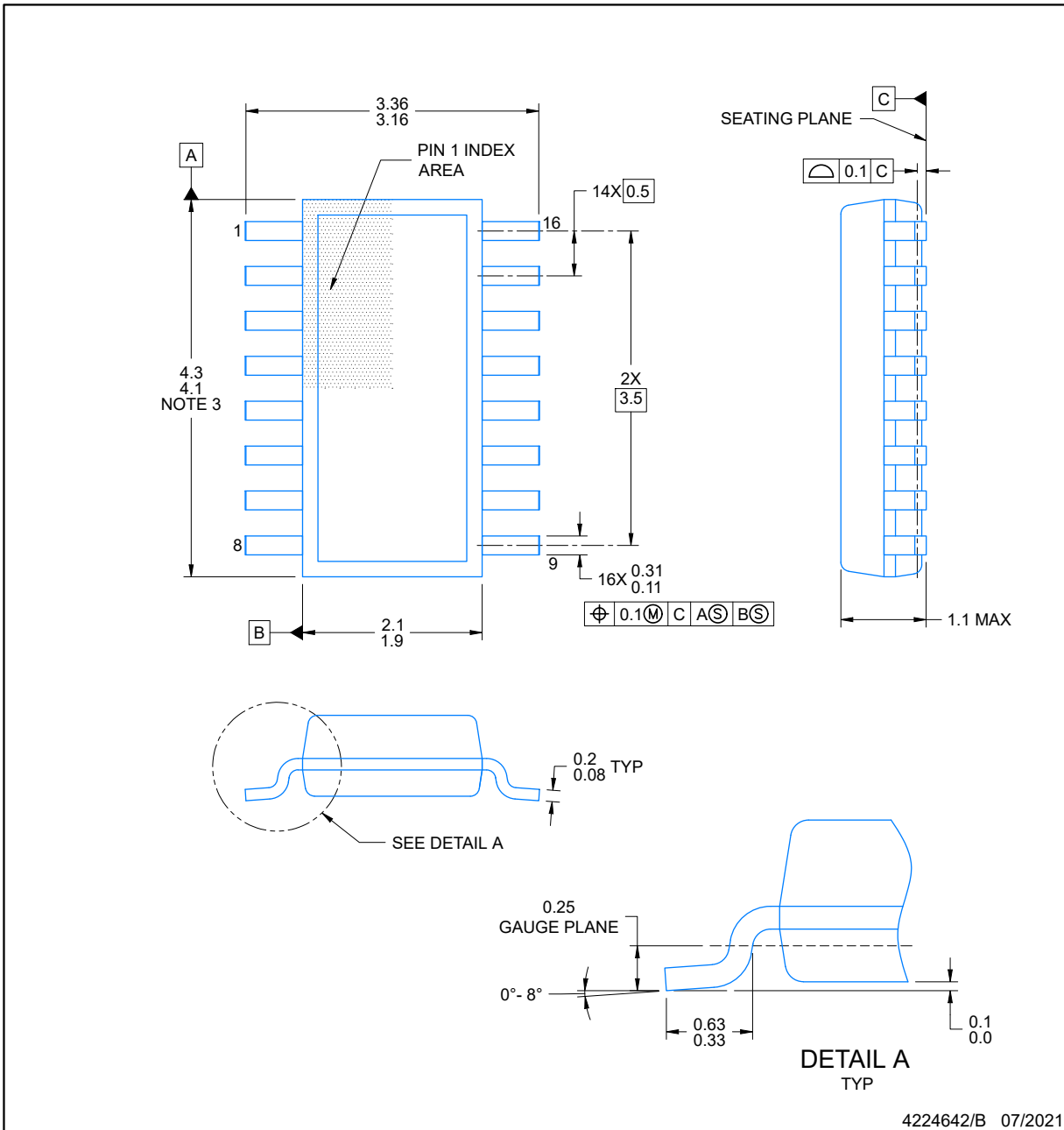
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0016A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

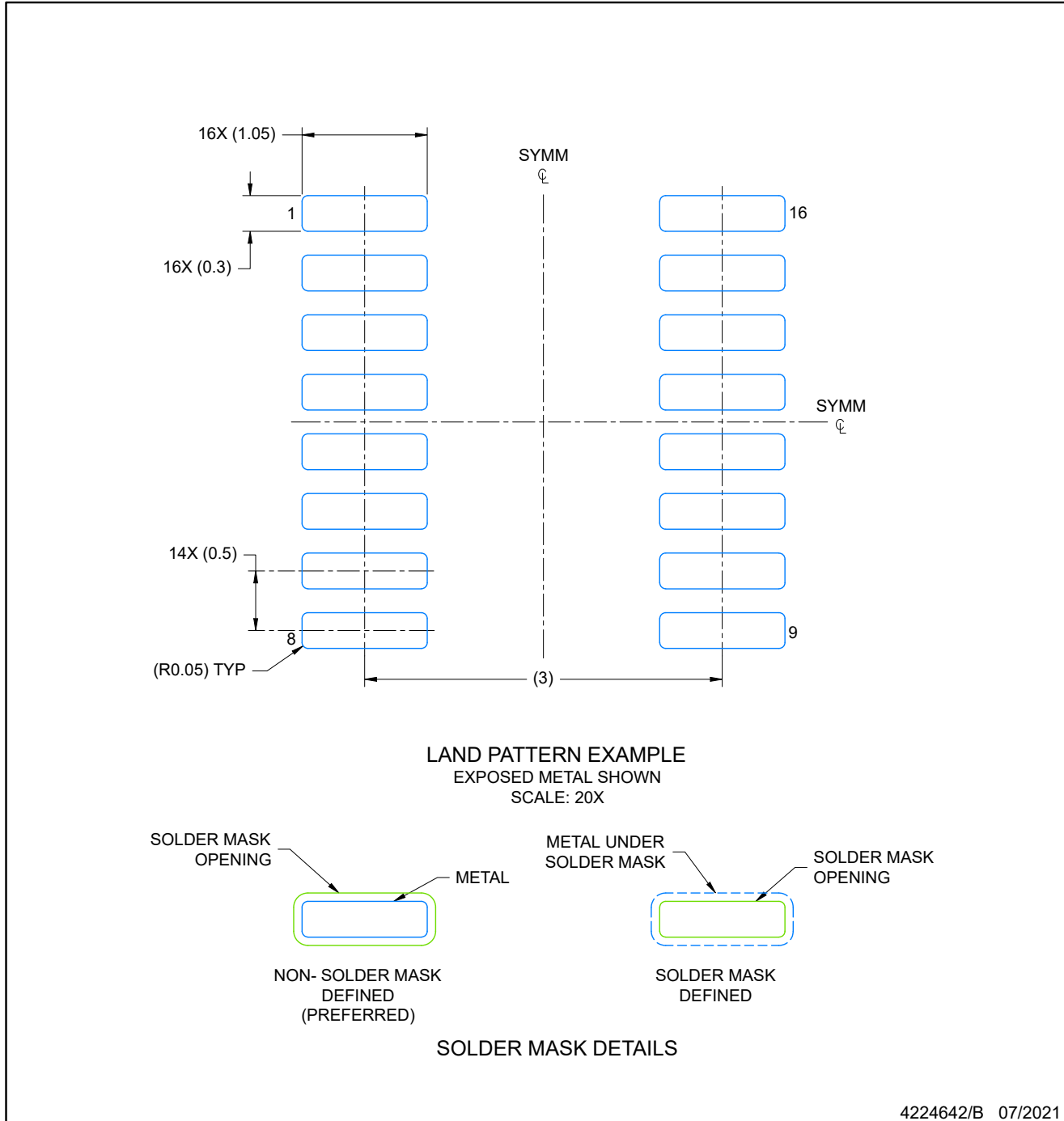
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA

EXAMPLE BOARD LAYOUT

SOT-23-THIN - 1.1 mm max height

DYY0016A

PLASTIC SMALL OUTLINE



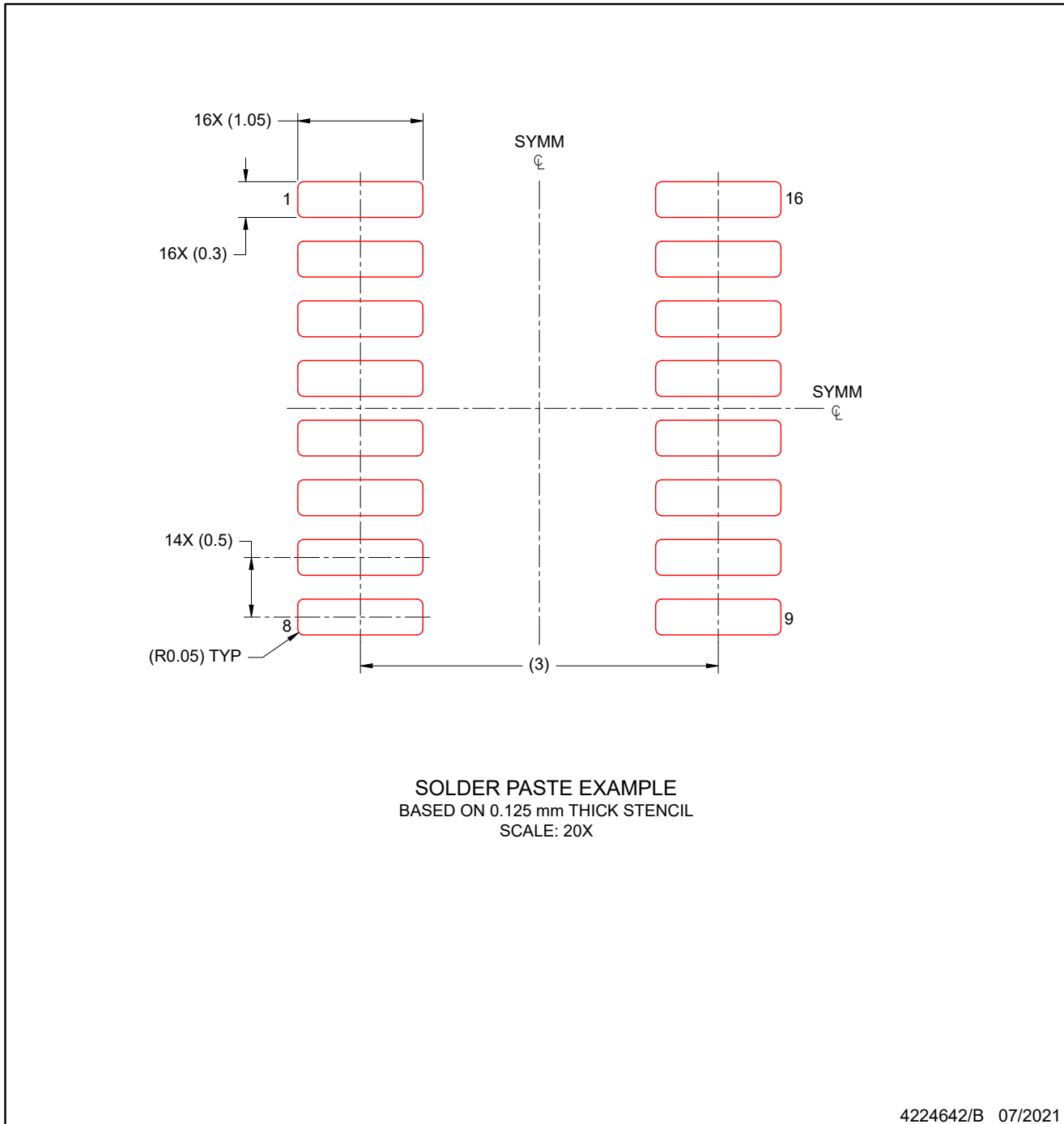
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN SOT-23-THIN - 1.1 mm max height

DYY0016A

PLASTIC SMALL OUTLINE



NOTES: (continued)

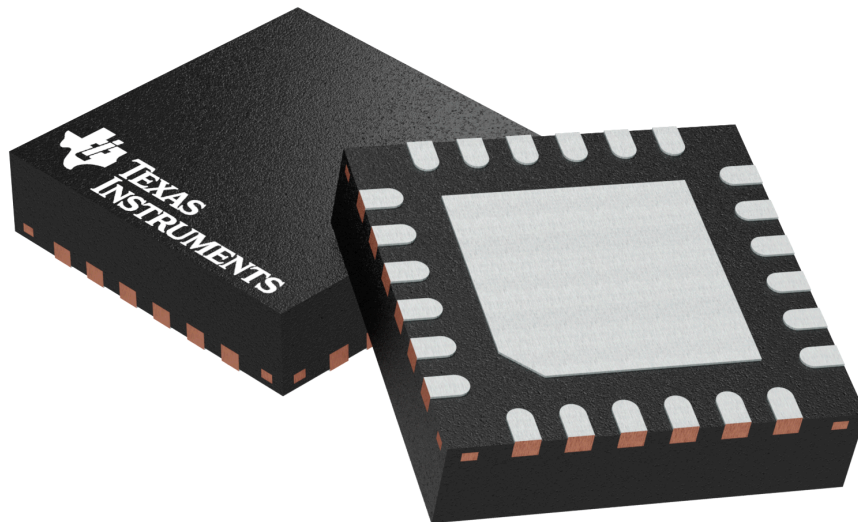
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

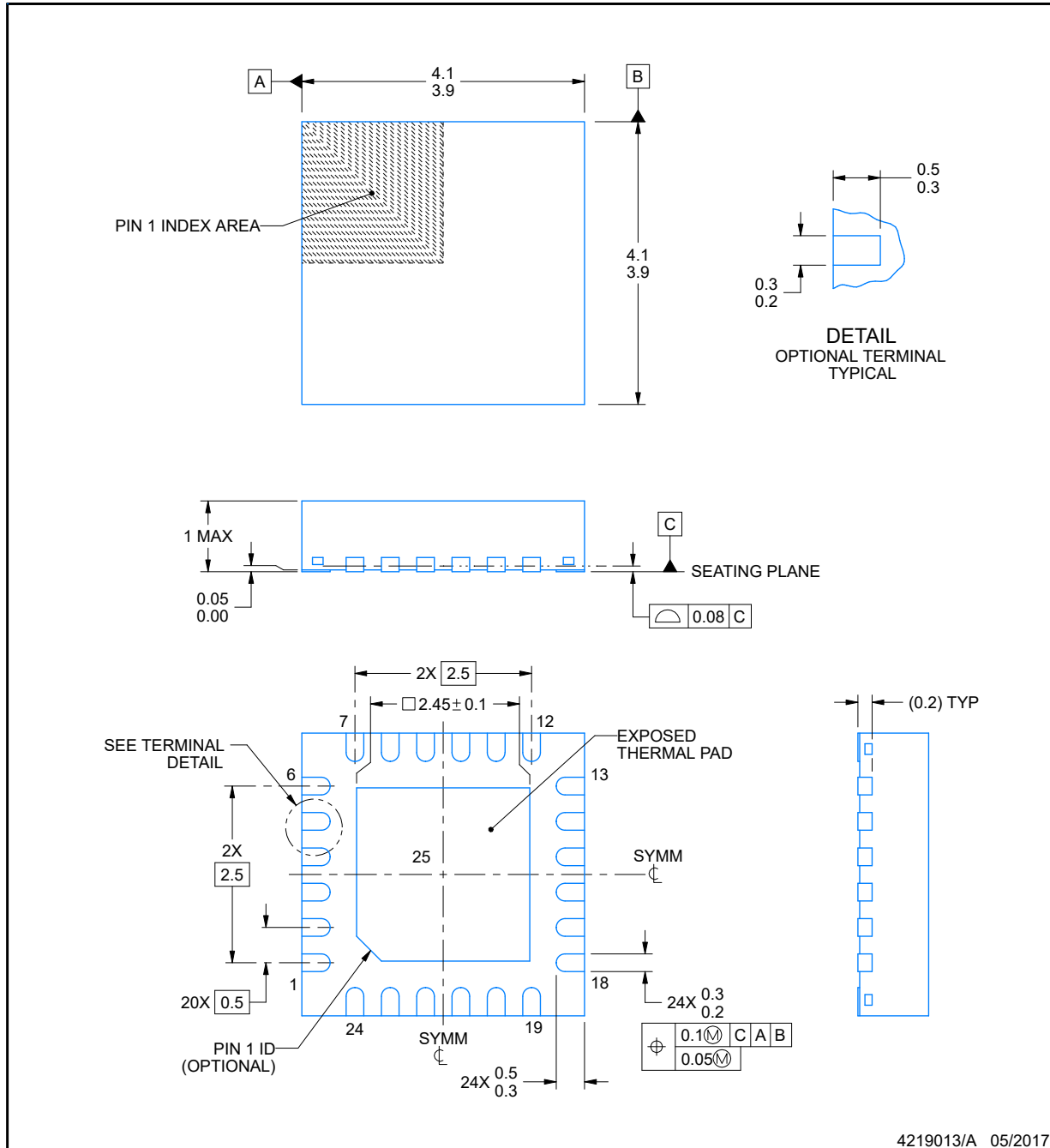


RGE0024B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

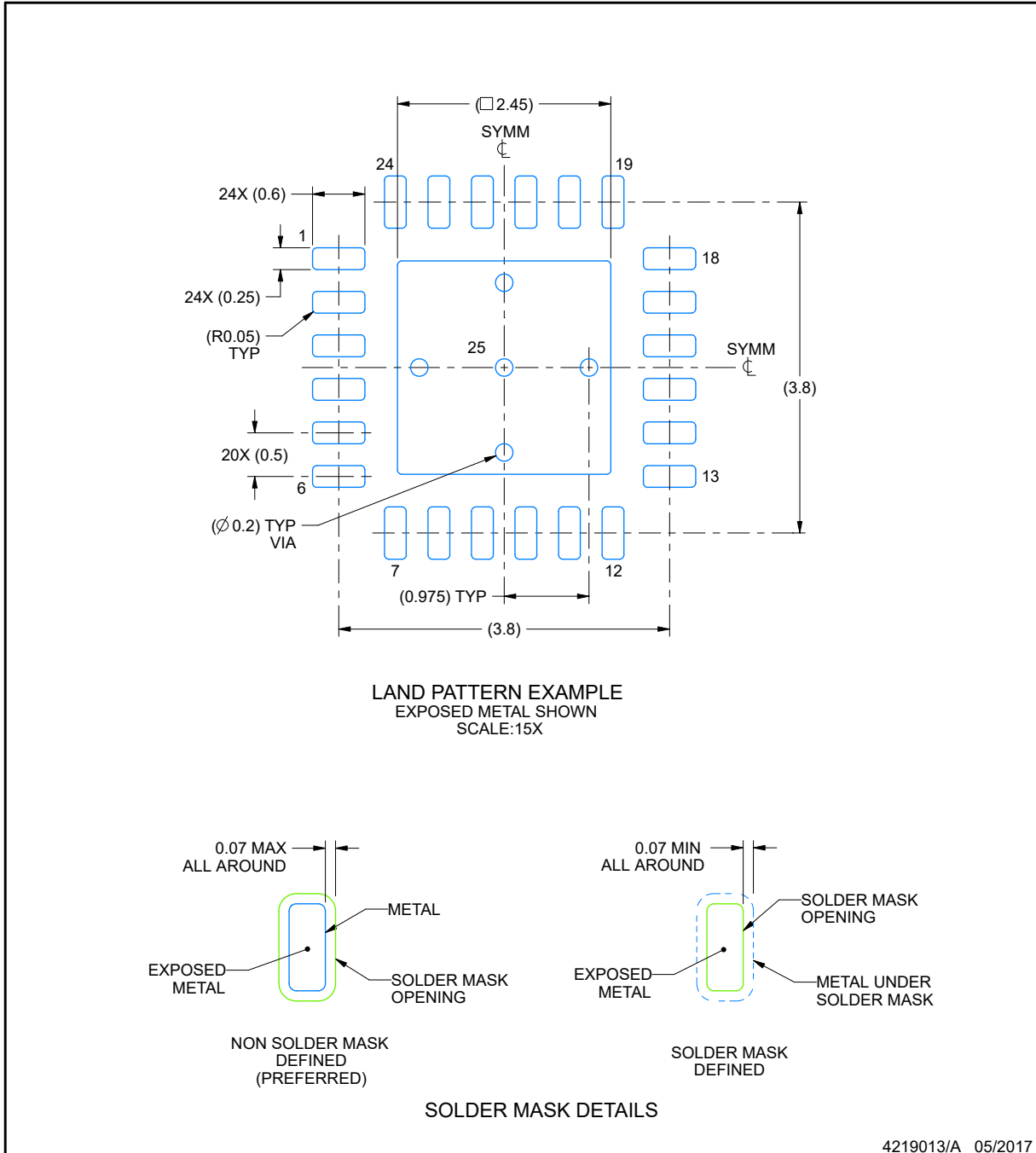
4219013/A 05/2017

EXAMPLE BOARD LAYOUT

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

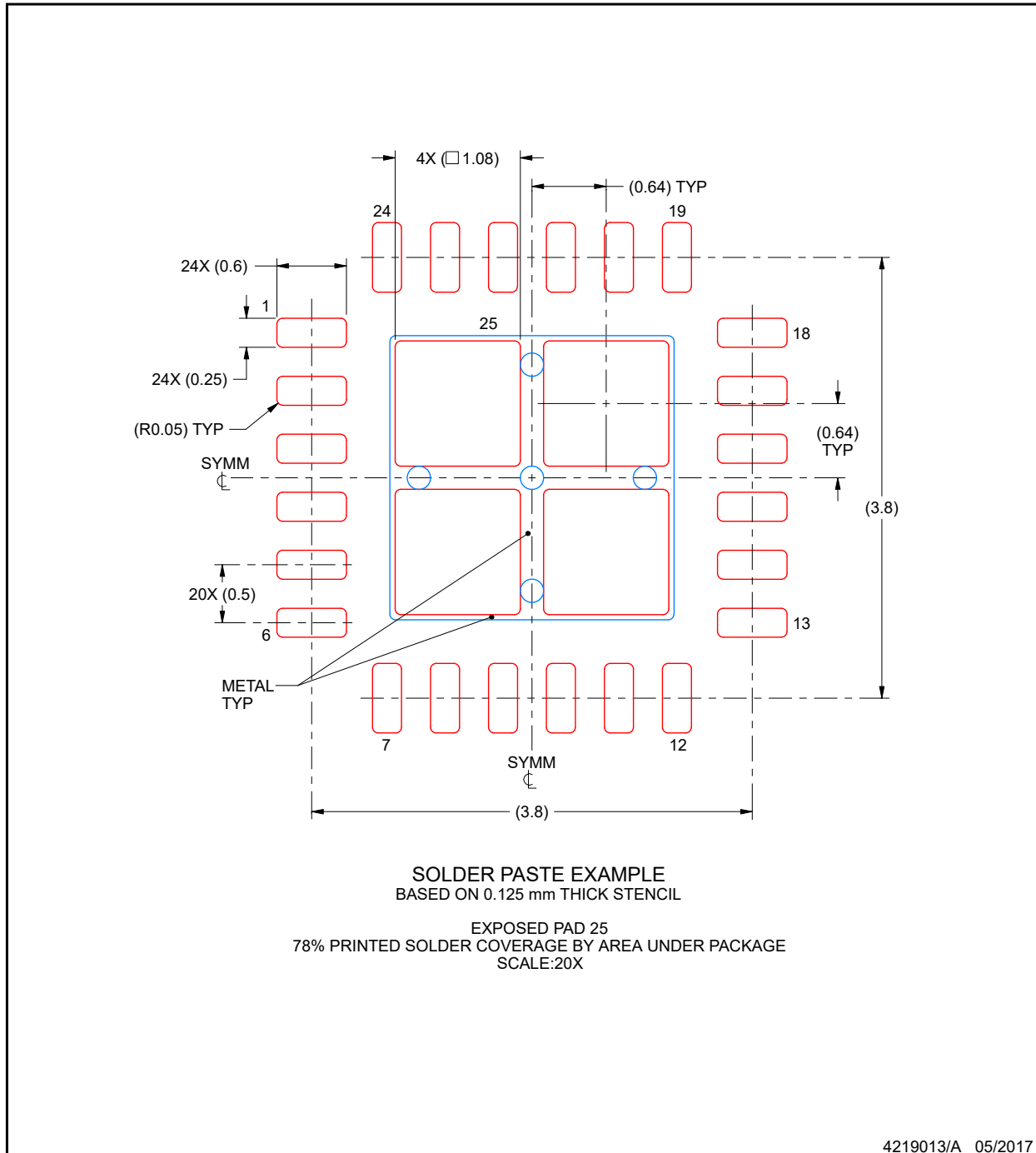
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

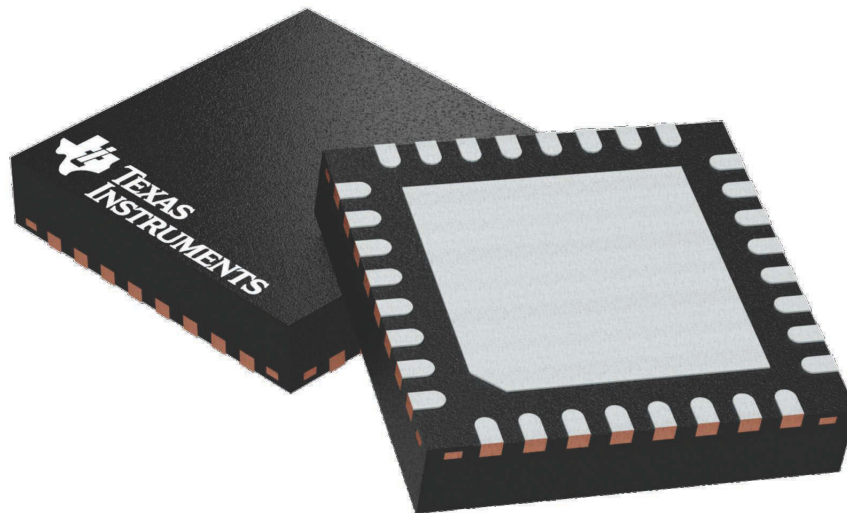
GENERIC PACKAGE VIEW

RHB 32

5 x 5, 0.5 mm pitch

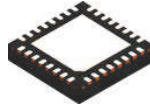
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

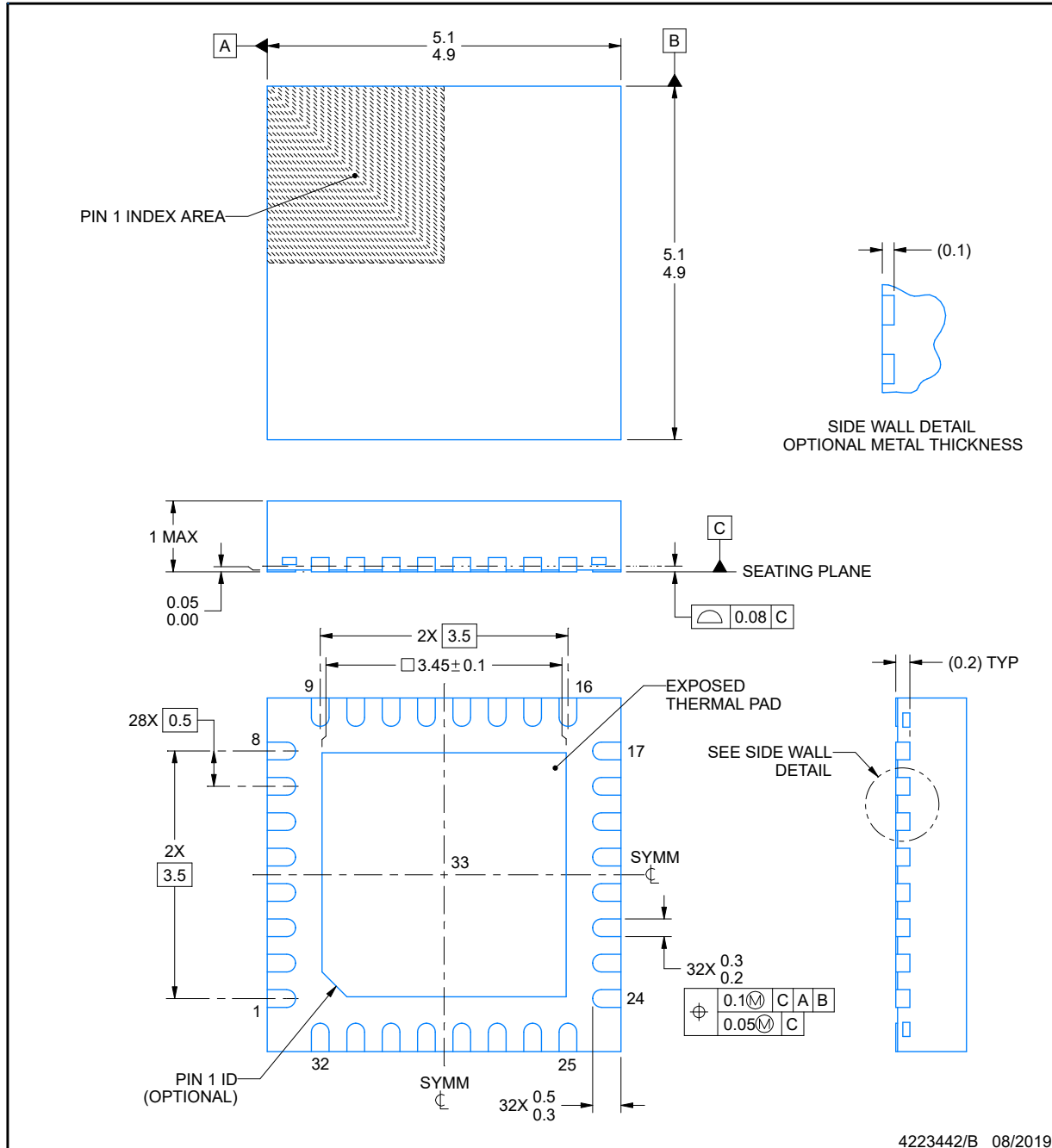


RHB0032E

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

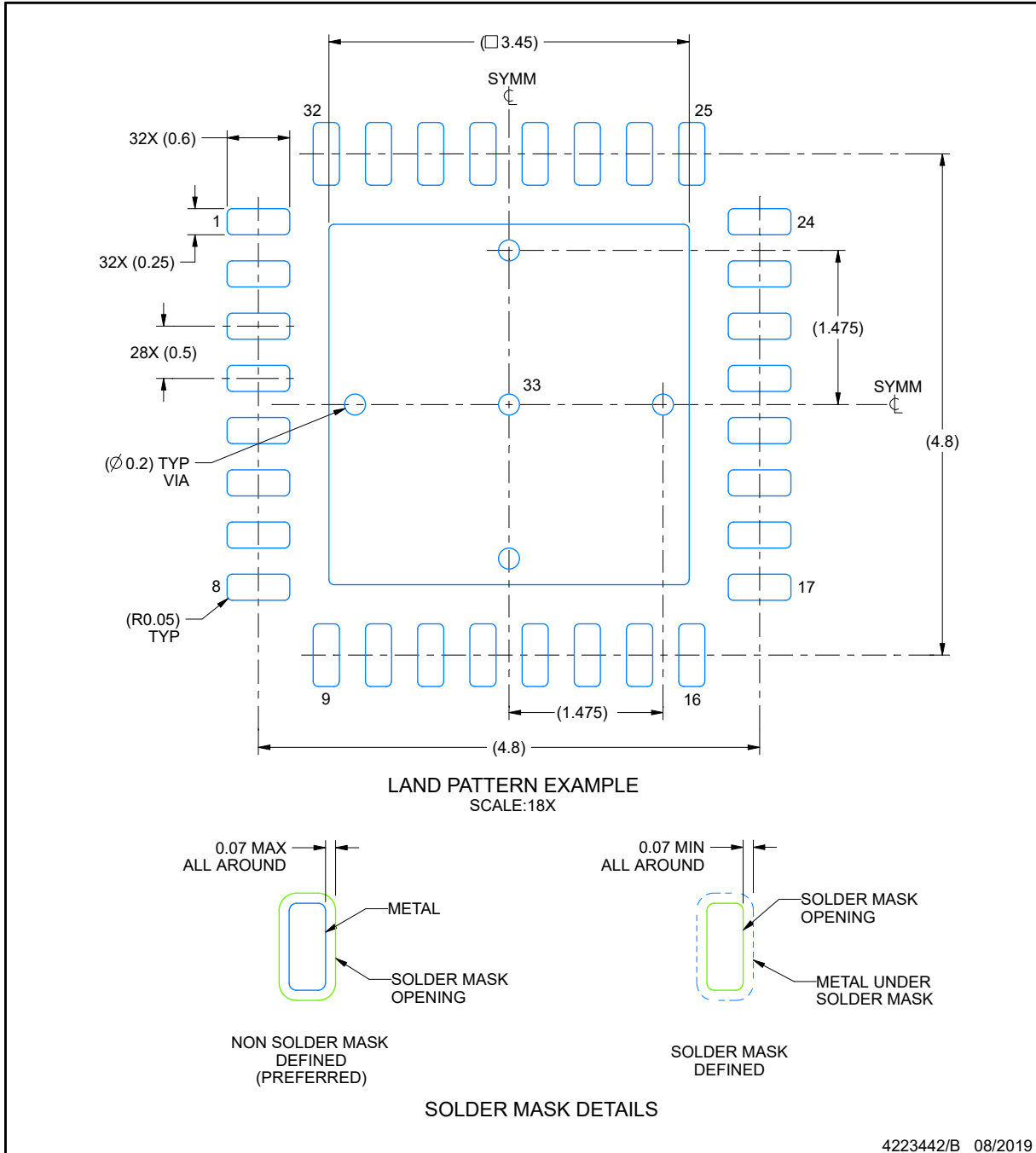
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

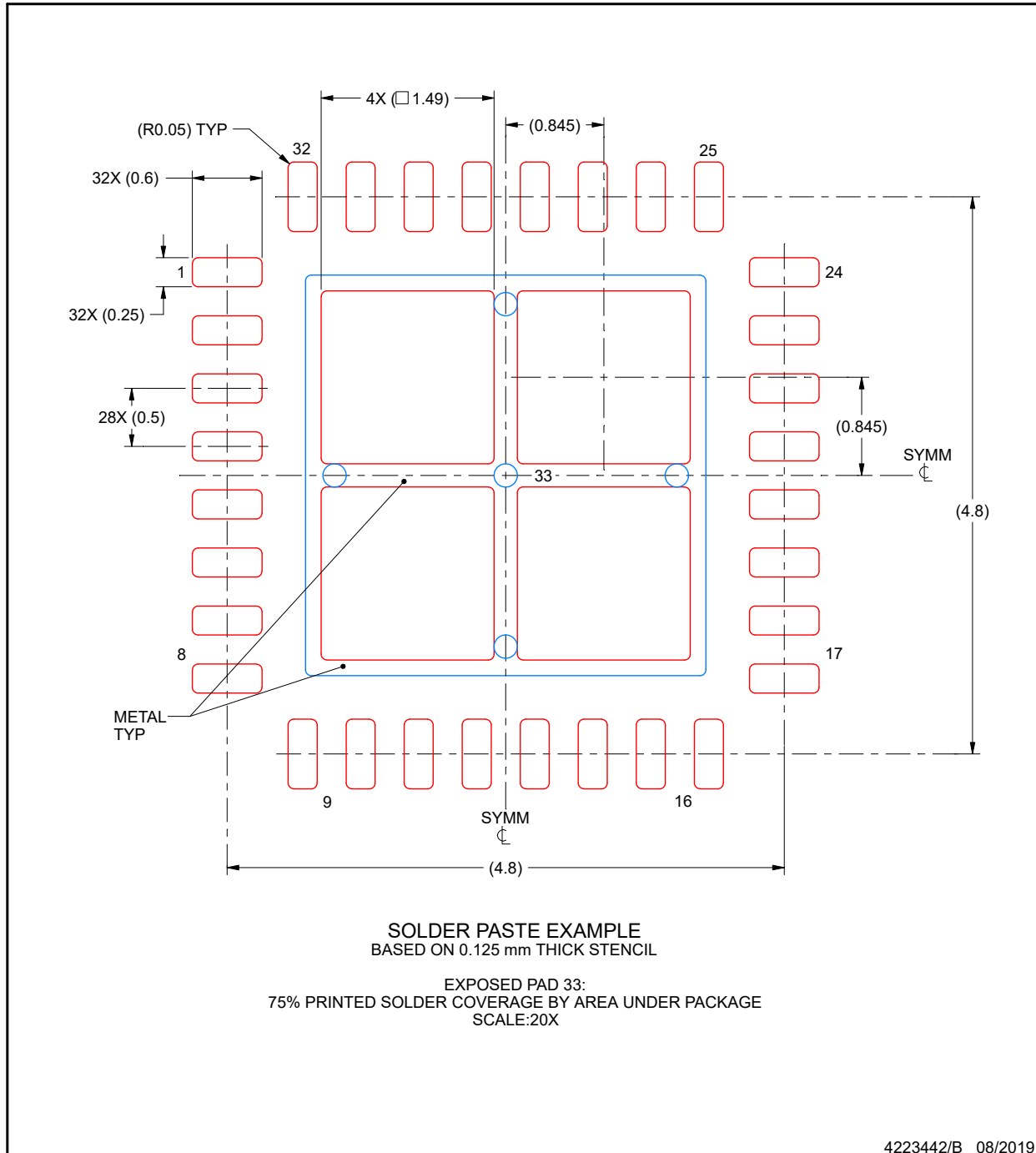
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

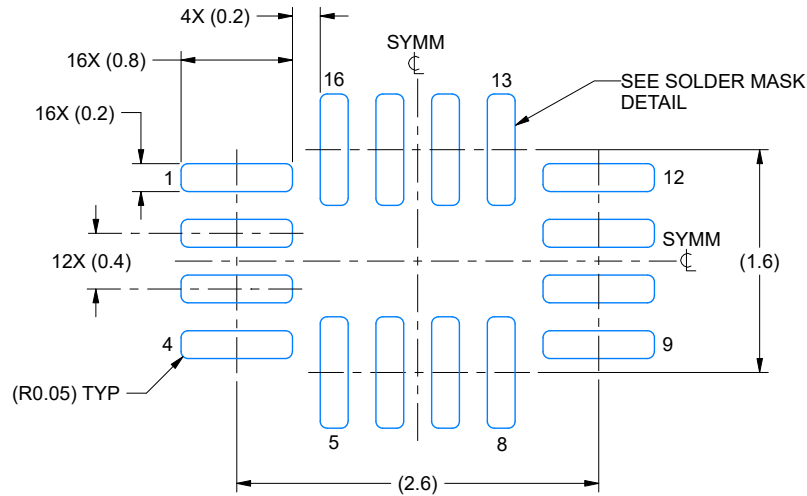
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

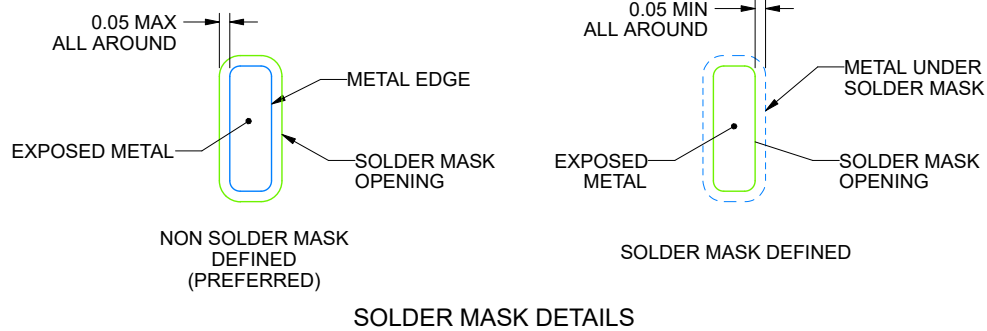
RTR0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4229337/A 01/2023

NOTES: (continued)

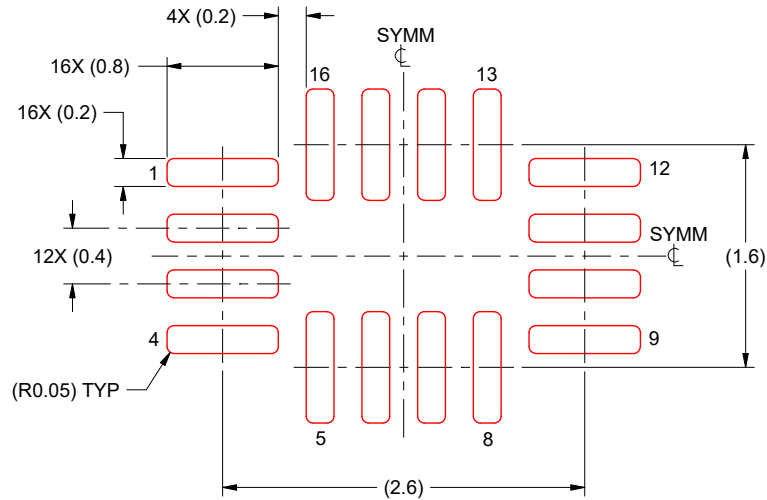
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RTR0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 MM THICK STENCIL
 SCALE: 20X

4229337/A 01/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSPM0L1303SRGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MSPM0 L1303S | Samples |
| MSPM0L1303TRGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | MSPM0 L1303T | Samples |
| MSPM0L1304SDGS20R | ACTIVE | VSSOP | DGS | 20 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | M0L1304S | Samples |
| MSPM0L1304SDGS28R | ACTIVE | VSSOP | DGS | 28 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | L1304S | Samples |
| MSPM0L1304SDYYR | ACTIVE | SOT-23-THIN | DYY | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | M0L1304S | Samples |
| MSPM0L1304SRGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MSPM0 L1304S | Samples |
| MSPM0L1304SRHBR | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | MSPM0 L1304S | Samples |
| MSPM0L1304TDGS20R | ACTIVE | VSSOP | DGS | 20 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M0L1304T | Samples |
| MSPM0L1304TDGS28R | ACTIVE | VSSOP | DGS | 28 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | L1304T | Samples |
| MSPM0L1304TDYYR | ACTIVE | SOT-23-THIN | DYY | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | M0L1304T | Samples |
| MSPM0L1304TRGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | MSPM0 L1304T | Samples |
| MSPM0L1304TRHBR | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | MSPM0 L1304T | Samples |
| MSPM0L1305SDGS20R | ACTIVE | VSSOP | DGS | 20 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | M0L1305S | Samples |
| MSPM0L1305SDGS28R | ACTIVE | VSSOP | DGS | 28 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | L1305S | Samples |
| MSPM0L1305SDYYR | ACTIVE | SOT-23-THIN | DYY | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | M0L1305S | Samples |
| MSPM0L1305SRGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MSPM0 L1305S | Samples |
| MSPM0L1305SRHBR | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | MSPM0 L1305S | Samples |
| MSPM0L1305TDGS20R | ACTIVE | VSSOP | DGS | 20 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M0L1305T | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSPM0L1305TDGS28R | ACTIVE | VSSOP | DGS | 28 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | L1305T | Samples |
| MSPM0L1305TDYYR | ACTIVE | SOT-23-THIN | DYY | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | M0L1305T | Samples |
| MSPM0L1305TRGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | MSPM0 L1305T | Samples |
| MSPM0L1305TRHBR | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | MSPM0 L1305T | Samples |
| MSPM0L1306SDGS20R | ACTIVE | VSSOP | DGS | 20 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | M0L1306S | Samples |
| MSPM0L1306SDGS28R | ACTIVE | VSSOP | DGS | 28 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | L1306S | Samples |
| MSPM0L1306SDYYR | ACTIVE | SOT-23-THIN | DYY | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | M0L1306S | Samples |
| MSPM0L1306SRGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MSPM0 L1306S | Samples |
| MSPM0L1306SRHBR | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | MSPM0 L1306S | Samples |
| MSPM0L1306TDGS20R | ACTIVE | VSSOP | DGS | 20 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M0L1306T | Samples |
| MSPM0L1306TDGS28R | ACTIVE | VSSOP | DGS | 28 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | L1306T | Samples |
| MSPM0L1306TDYYR | ACTIVE | SOT-23-THIN | DYY | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | M0L1306T | Samples |
| MSPM0L1306TRGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | MSPM0 L1306T | Samples |
| MSPM0L1306TRHBR | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | MSPM0 L1306T | Samples |
| MSPM0L1343TDGS20R | ACTIVE | VSSOP | DGS | 20 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M0L1343T | Samples |
| MSPM0L1344TDGS20R | ACTIVE | VSSOP | DGS | 20 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M0L1344T | Samples |
| MSPM0L1345TDGS28R | ACTIVE | VSSOP | DGS | 28 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | L1345T | Samples |
| MSPM0L1346TDGS28R | ACTIVE | VSSOP | DGS | 28 | 5000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | L1346T | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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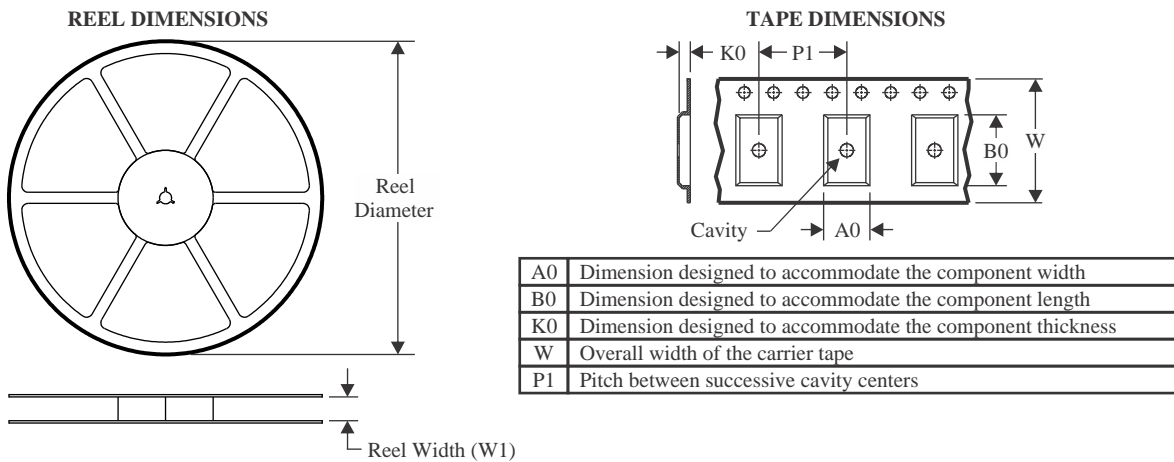
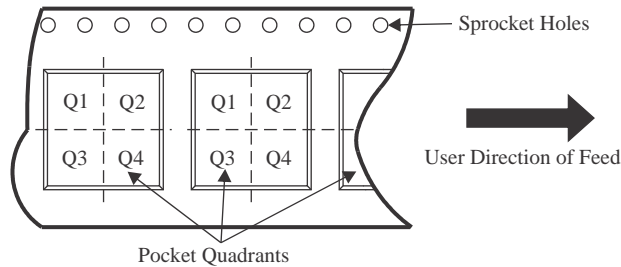
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSPM0L1305, MSPM0L1306 :

- Automotive : [MSPM0L1305-Q1](#), [MSPM0L1306-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSPM0L1303SRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSPM0L1303TRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSPM0L1304SDGS20R | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1304SDGS28R | VSSOP | DGS | 28 | 5000 | 330.0 | 16.4 | 5.5 | 7.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1304SDYYR | SOT-23-THIN | DYY | 16 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| MSPM0L1304SRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSPM0L1304SRHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| MSPM0L1304TDGS20R | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1304TDGS28R | VSSOP | DGS | 28 | 5000 | 330.0 | 16.4 | 5.5 | 7.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1304TDYYR | SOT-23-THIN | DYY | 16 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| MSPM0L1304TRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSPM0L1304TRHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| MSPM0L1305SDGS20R | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1305SDGS28R | VSSOP | DGS | 28 | 5000 | 330.0 | 16.4 | 5.5 | 7.4 | 1.45 | 8.0 | 16.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSPM0L1305SDYYR | SOT-23-THIN | DYY | 16 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| MSPM0L1305SRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSPM0L1305SRHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| MSPM0L1305TDGS20R | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1305TDGS28R | VSSOP | DGS | 28 | 5000 | 330.0 | 16.4 | 5.5 | 7.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1305TDYYR | SOT-23-THIN | DYY | 16 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| MSPM0L1305TRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSPM0L1305TRHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| MSPM0L1306SDGS20R | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1306SDGS28R | VSSOP | DGS | 28 | 5000 | 330.0 | 16.4 | 5.5 | 7.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1306SDYYR | SOT-23-THIN | DYY | 16 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| MSPM0L1306SRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSPM0L1306SRHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| MSPM0L1306TDGS20R | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1306TDGS28R | VSSOP | DGS | 28 | 5000 | 330.0 | 16.4 | 5.5 | 7.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1306TDYYR | SOT-23-THIN | DYY | 16 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| MSPM0L1306TRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSPM0L1306TRHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| MSPM0L1343TDGS20R | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1344TDGS20R | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1345TDGS28R | VSSOP | DGS | 28 | 5000 | 330.0 | 16.4 | 5.5 | 7.4 | 1.45 | 8.0 | 16.0 | Q1 |
| MSPM0L1346TDGS28R | VSSOP | DGS | 28 | 5000 | 330.0 | 16.4 | 5.5 | 7.4 | 1.45 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSPM0L1303SRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1303TRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1304SDGS20R | VSSOP | DGS | 20 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1304SDGS28R | VSSOP | DGS | 28 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1304SDYYR | SOT-23-THIN | DYY | 16 | 3000 | 336.6 | 336.6 | 31.8 |
| MSPM0L1304SRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1304SRHBR | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1304TDGS20R | VSSOP | DGS | 20 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1304TDGS28R | VSSOP | DGS | 28 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1304TDYYR | SOT-23-THIN | DYY | 16 | 3000 | 336.6 | 336.6 | 31.8 |
| MSPM0L1304TRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1304TRHBR | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1305SDGS20R | VSSOP | DGS | 20 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1305SDGS28R | VSSOP | DGS | 28 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1305SDYYR | SOT-23-THIN | DYY | 16 | 3000 | 336.6 | 336.6 | 31.8 |
| MSPM0L1305SRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1305SRHBR | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1305TDGS20R | VSSOP | DGS | 20 | 5000 | 356.0 | 356.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSPM0L1305TDGS28R | VSSOP | DGS | 28 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1305TDYYR | SOT-23-THIN | DYY | 16 | 3000 | 336.6 | 336.6 | 31.8 |
| MSPM0L1305TRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1305TRHBR | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1306SDGS20R | VSSOP | DGS | 20 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1306SDGS28R | VSSOP | DGS | 28 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1306SDYYR | SOT-23-THIN | DYY | 16 | 3000 | 336.6 | 336.6 | 31.8 |
| MSPM0L1306SRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1306SRHBR | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1306TDGS20R | VSSOP | DGS | 20 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1306TDGS28R | VSSOP | DGS | 28 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1306TDYYR | SOT-23-THIN | DYY | 16 | 3000 | 336.6 | 336.6 | 31.8 |
| MSPM0L1306TRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1306TRHBR | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0L1343TDGS20R | VSSOP | DGS | 20 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1344TDGS20R | VSSOP | DGS | 20 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1345TDGS28R | VSSOP | DGS | 28 | 5000 | 356.0 | 356.0 | 35.0 |
| MSPM0L1346TDGS28R | VSSOP | DGS | 28 | 5000 | 356.0 | 356.0 | 35.0 |

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