MSPM0L130x Mixed-Signal Microcontrollers

1 Features

- **Core**
  - Arm® 32-bit Cortex®-M0+ CPU, frequency up to 32 MHz
- **Operating characteristics**
  - Extended temperature: –40°C to 125°C
  - Wide supply voltage range: 1.62 V to 3.6 V
- **Memories**
  - Up to 64KB of flash
  - Up to 4KB of SRAM
- **High-performance analog peripherals**
  - One 12-bit 1.68-Msps analog-to-digital converter (ADC) with up to 10 total external channels
  - Configurable 1.4-V or 2.5-V internal ADC voltage reference (VREF)
  - Two zero-drift, zero-crossover chopper operational amplifiers (OPA)
    - 0.5-µV/°C drift with chopping
    - 6-pA input bias current [1]
    - Integrated programmable gain stage (1-32x)
  - One general-purpose amplifier (GPAMP)
  - One high-speed comparator (COMP) with 8-bit reference DAC
    - 32-ns propagation delay
    - Low power mode down to <1-µA
  - Programmable analog connections between ADC, OPAs, COMP, and DAC
  - Integrated temperature sensor
- **Optimized low-power modes**
  - RUN: 71 µA/MHz (CoreMark)
  - STOP: 151 µA at 4 MHz and 44 µA at 32 kHz
  - STANDBY: 1.0 µA with 32-kHz 16-bit timer running, SRAM/registers fully retained, and 32MHz clock wakeup in 3.2µs
  - SHUTDOWN: 61 nA with IO wakeup capability
- **Intelligent digital peripherals**
  - 3-channel DMA controller
  - 3-channel event fabric signaling system
  - Four 16-bit general-purpose timers, each with two capture/compare registers supporting low-power operation in STANDBY mode, supporting a total of 8 PWM channels
  - Windowed watchdog timer
- **Enhanced communication interfaces**
  - Two UART interfaces; one supports LIN, IrDA, DALI, Smart Card, Manchester and both support low-power operation in STANDBY
  - Two I^2C interfaces; one supports FM+ (1 Mbit/s) and both support SMBus, PMBus, and wakeup from STOP
  - One SPI supports up to 16 Mbit/s
- **Clock system**
  - Internal 4- to 32-MHz oscillator with ±1.2% accuracy (SYSOSC)
  - Internal 32-kHz low-frequency oscillator with ±3% accuracy (LFOSC)
- **Data integrity**
  - Cyclic redundancy checker (CRC-16 or CRC-32)
- **Flexible I/O features**
  - Up to 28 GPIOs
  - Two 5-V-tolerant open-drain IOs with fail-safe protection
- **Development support**
  - 2-pin serial wire debug (SWD)
- **Package options**
  - 32-pin VQFN (RHB)
  - 28-pin VSSOP (DGS)
  - 24-pin VQFN (RGE)
  - 20-pin VSSOP (DGS)
  - 16-pin SOT (DYY), WQFN (RTR)[2]
- **Family members** (also see *Device Comparison*)
  - MSPM0L13x3: 8KB of flash, 2KB of RAM
  - MSPM0L13x4: 16KB of flash, 2KB of RAM
  - MSPM0L13x5: 32KB of flash, 4KB of RAM
  - MSPM0L13x6: 64KB of flash, 4KB of RAM
- **Development kits and software** (also see *Tools and Software*)
  - LP-MSPM0L1306 LaunchPad™ development kit
  - MSP Software Development Kit (SDK)

2 Applications

- Battery charging and management
- Power supplies and power delivery
- Personal electronics
- Building security and fire safety
- Connected peripherals and printers
- Grid infrastructure
- Smart metering
- Communication modules
- Medical and healthcare
- Lighting

[1] MSPM0L134x only
[2] The 16-pin WQFN package is product preview.

3 Description

MSPM0L134x and MSPM0L130x microcontrollers (MCUs) are part of MSP's highly-integrated, ultra-low-power 32-bit MSPM0 MCU family based on the enhanced Arm® Cortex®-M0+ core platform operating at up to 32-MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages ranging from 1.62 V to 3.6 V.

The MSPM0L134x and MSPM0L130x devices provide up to 64KB embedded flash program memory with up to 4KB SRAM. These MCUs incorporate a high-speed on-chip oscillator with an accuracy up to ±1.2%, eliminating the need for an external crystal. Additional features include a 3-channel DMA, 16- and 32-bit CRC accelerator, and a variety of high-performance analog peripherals such as one 12-bit 1.68-MSPS ADC with configurable internal voltage reference, one high-speed comparator with built-in reference DAC, two zero-drift zero-crossover operational amplifiers with programmable gain, one general-purpose amplifier, and an on-chip temperature sensor. These devices also offer intelligent digital peripherals such as four 16-bit general purpose timers, one windowed watchdog timer, and a variety of communication peripherals including two UARTs, one SPI, and two I^2Cs. These communication peripherals offer protocol support for LIN, IrDA, DALI, Manchester, Smart Card, SMBus, and PMBus.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers find the MCU that meets their project's needs. The architecture combined with extensive low-power modes are optimized to achieve extended battery life in portable measurement applications.

MSPM0L134x and MSPM0L130x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad available for purchase and design files for a Target-Socket Board. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM0 MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

For complete module descriptions, see the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

> **CAUTION**
>
> System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See MSP430™ System-Level ESD Considerations for more information; the principles in this application note are applicable to MSPM0 MCUs.

4 Functional Block Diagram

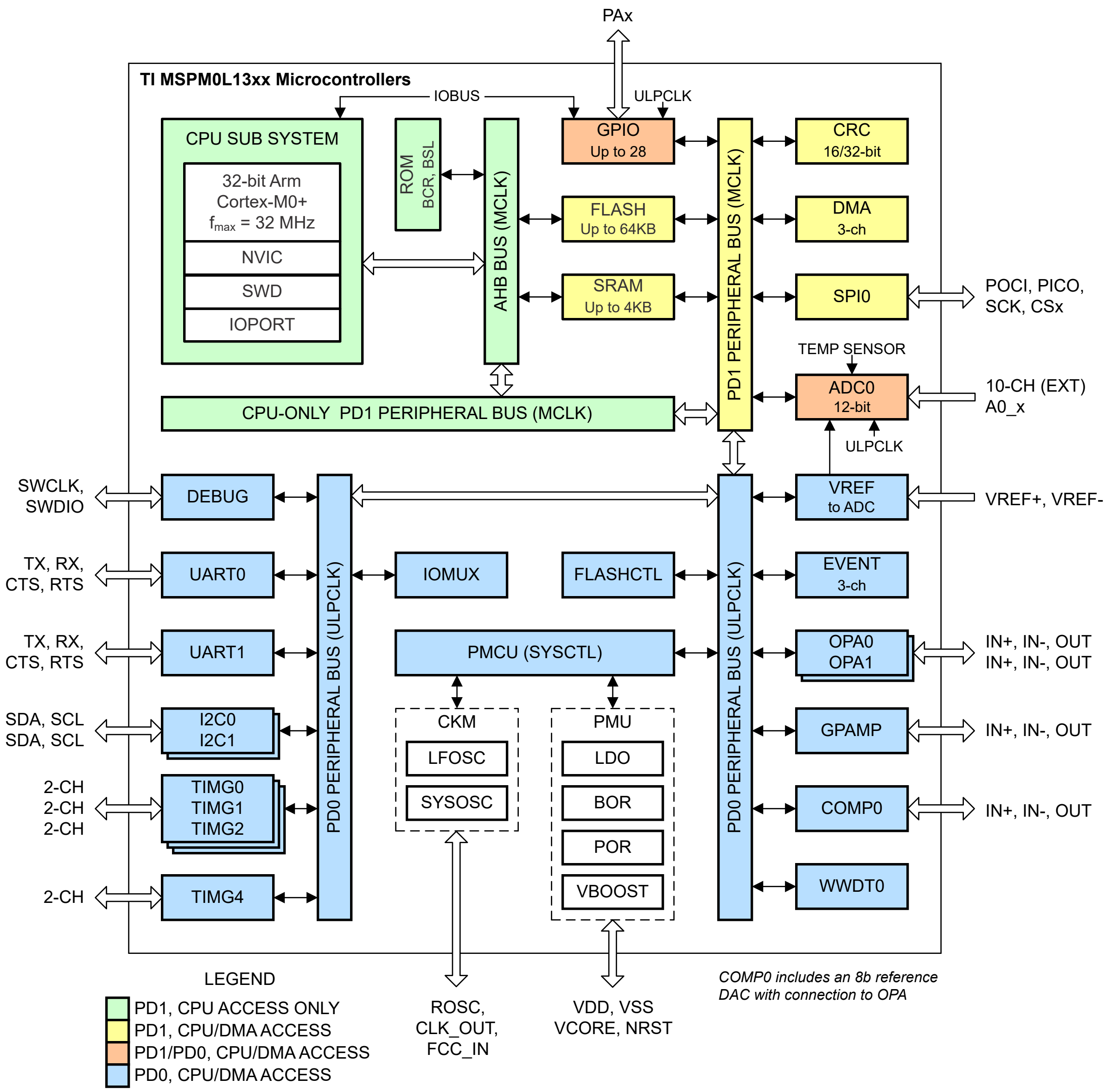


Figure 4-1. MSPM0L130x Functional Block Diagram

Table of Contents

5 Device Comparison

Table 5-1. Device Comparison

<table>
<tr><th>DEVICE NAME (1) (2)</th><th>FLASH / SRAM (KB)</th><th>QUAL(3)</th><th>ADC CH.</th><th>COMP</th><th>OPA</th><th>GPAMP</th><th>UART/I2C/SPI</th><th>TIMG</th><th>GPIOs</th><th>5-V TOL. IO</th><th>PACKAGE [BODY SIZE] (4)</th></tr>
<tr><td>MSPM0L1306xRHB</td><td>64 / 4</td><td rowspan="3">T/S</td><td rowspan="3">10</td><td rowspan="3">1</td><td rowspan="3">2</td><td rowspan="3">1</td><td rowspan="3">2 / 2 / 1</td><td rowspan="3">4</td><td rowspan="3">28</td><td rowspan="3">2</td><td rowspan="3">32 VQFN [5 mm × 5 mm]</td></tr>
<tr><td>MSPM0L1305xRHB</td><td>32 / 4</td></tr>
<tr><td>MSPM0L1304xRHB</td><td>16 / 2</td></tr>
<tr><td>MSPM0L1306xDGS28</td><td>64 / 4</td><td rowspan="3">T/S</td><td rowspan="3">10</td><td rowspan="5">1</td><td rowspan="5">2</td><td rowspan="5">1</td><td rowspan="5">2 / 2 / 1</td><td rowspan="5">4</td><td rowspan="3">24</td><td rowspan="5">2</td><td rowspan="5">28 VSSOP [7.1 mm × 3 mm]</td></tr>
<tr><td>MSPM0L1305xDGS28</td><td>32 / 4</td></tr>
<tr><td>MSPM0L1304xDGS28</td><td>16 / 2</td></tr>
<tr><td>MSPM0L1346xDGS28</td><td>64 / 4</td><td rowspan="2">T</td><td rowspan="2">9</td><td rowspan="2">22</td></tr>
<tr><td>MSPM0L1345xDGS28</td><td>32 / 4</td></tr>
<tr><td>MSPM0L1306xRGE</td><td>64 / 4</td><td rowspan="4">T/S</td><td rowspan="4">9</td><td rowspan="4">1</td><td rowspan="4">2</td><td rowspan="4">1</td><td rowspan="4">2 / 2 / 1</td><td rowspan="4">4</td><td rowspan="4">20</td><td rowspan="4">2</td><td rowspan="4">24 VQFN [4 mm × 4 mm]</td></tr>
<tr><td>MSPM0L1305xRGE</td><td>32 / 4</td></tr>
<tr><td>MSPM0L1304xRGE</td><td>16 / 2</td></tr>
<tr><td>MSPM0L1303xRGE</td><td>8 / 2</td></tr>
<tr><td>MSPM0L1306xDGS20</td><td>64 / 4</td><td rowspan="3">T/S</td><td rowspan="3">8</td><td rowspan="5">1</td><td rowspan="5">2</td><td rowspan="5">1</td><td rowspan="5">2 / 2 / 1</td><td rowspan="5">4</td><td rowspan="3">17</td><td rowspan="5">2</td><td rowspan="5">20 VSSOP [5.1 mm × 3 mm]</td></tr>
<tr><td>MSPM0L1305xDGS20</td><td>32 / 4</td></tr>
<tr><td>MSPM0L1304xDGS20</td><td>16 / 2</td></tr>
<tr><td>MSPM0L1344xDGS20</td><td>16 / 2</td><td rowspan="2">T</td><td rowspan="2">7</td><td rowspan="2">15</td></tr>
<tr><td>MSPM0L1343xDGS20</td><td>8 / 2</td></tr>
<tr><td>MSPM0L1306xRTR(5)</td><td>64 / 4</td><td rowspan="3">T/S</td><td rowspan="3">6</td><td rowspan="3">1</td><td rowspan="3">2</td><td rowspan="3">1</td><td rowspan="3">2 / 2 / 1</td><td rowspan="3">4</td><td rowspan="3">13</td><td rowspan="3">2</td><td rowspan="3">16 WQFN [3 mm × 2 mm]</td></tr>
<tr><td>MSPM0L1305xRTR(5)</td><td>32 / 4</td></tr>
<tr><td>MSPM0L1304xRTR(5)</td><td>16 / 2</td></tr>
<tr><td>MSPM0L1306xDYY</td><td>64 / 4</td><td rowspan="3">T/S</td><td rowspan="3">6</td><td rowspan="3">1</td><td rowspan="3">2</td><td rowspan="3">1</td><td rowspan="3">2 / 2 / 1</td><td rowspan="3">4</td><td rowspan="3">13</td><td rowspan="3">2</td><td rowspan="3">16 SOT [4.2 mm × 2 mm]</td></tr>
<tr><td>MSPM0L1305xDYY</td><td>32 / 4</td></tr>
<tr><td>MSPM0L1304xDYY</td><td>16 / 2</td></tr>
</table>

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 11, or see the TI website.
(2) For more information about the device name, see Section 10.1.
(3) Device qualifications:
- T = –40°C to 105°C
- S = –40°C to 125°C

(4) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 11.
(5) The 16-pin WQFN package is product preview.

6 Pin Configuration and Functions

6.1 Pin Diagrams

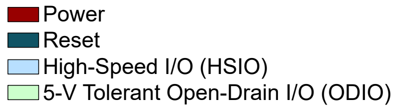


Figure 6-1. Pin Diagram Color Coding

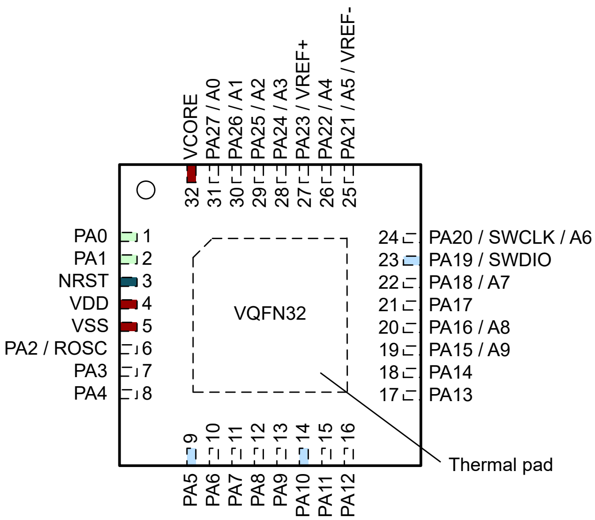


Figure 6-2. 32-Pin RHB (VQFN) (Top View) - MSPM0L130x

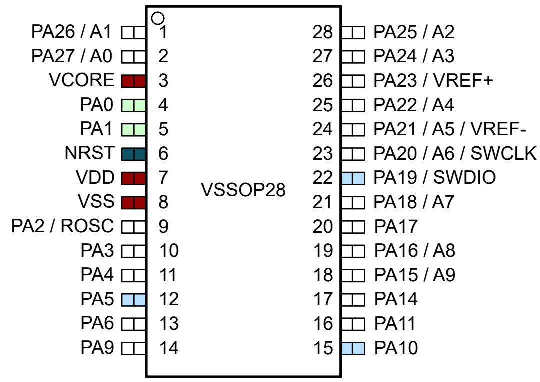


Figure 6-3. 28-Pin DGS28 (VSSOP) (Top View) - MSPM0L130x

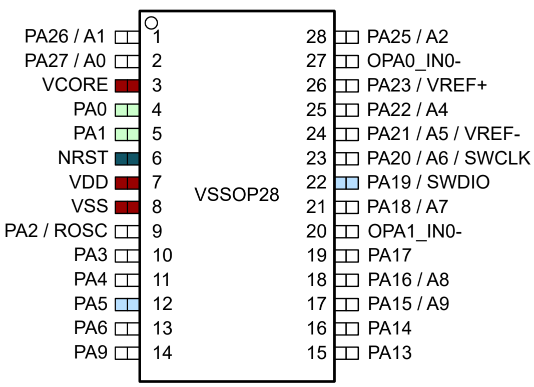


Figure 6-4. 28-Pin DGS28 (VSSOP) (Top View) - MSPM0L134x

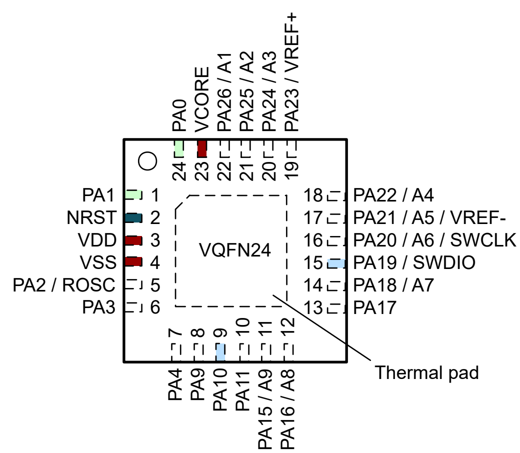


Figure 6-5. 24-Pin RGE (VQFN) (Top View) - MSPM0L130x

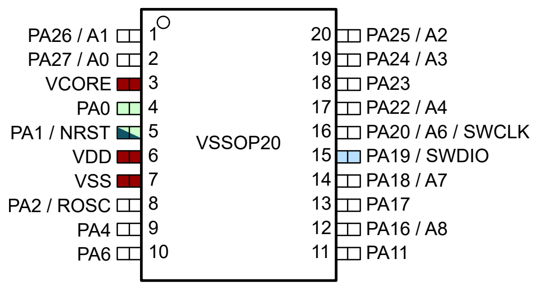


Figure 6-6. 20-Pin DGS20 (VSSOP) (Top View) - MSPM0L130x

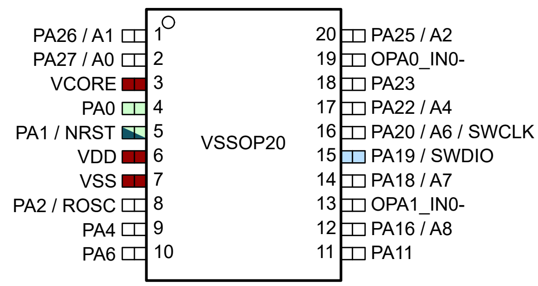


Figure 6-7. 20-Pin DGS20 (VSSOP) (Top View) - MSPM0L134x

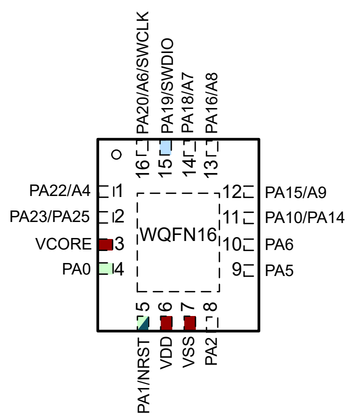


Figure 6-8. 16-Pin RTR (WQFN) (Top View) - MSPM0L130x

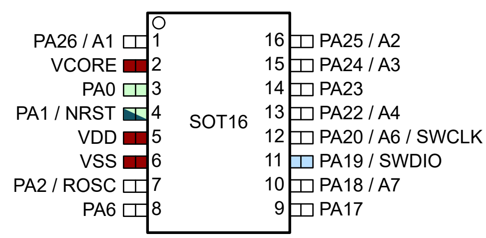


Figure 6-9. 16-Pin DYY (SOT) (Top View) - MSPM0L130x

6.2 Pin Attributes

Table 6-1 describes the functions available on every pin for each device package.

> **Note**
>
> Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which allows users to configure the desired *Pin Function* using the PINCM.PF control bits.

Table 6-1. Pin Attributes

PINCMx	PIN NAME	PIN FUNCTION		PIN NUMBER							I/O STRUCTURE
		ANALOG	DIGITAL(1)	32 VQFN	28 VSSOP (2)	28 VSSOP (3)	24 VQFN	20 VSSOP	16 WQFN	16 SOT	
N/A	N/A	VDD		4	7	7	3	6	6	5	Power
N/A	N/A	VSS		5	8	8	4	7	7	6	Power
N/A	N/A	VCORE		32	3	3	23	3	3	2	Power
1	PA0		UART1_TX *[2]* / I2C0_SDA *[3]* / TIMG1_C0 *[4]* / SPI0_CS1 *[5](Default BSL I2C_SDA)*	1	4	4	24	4	4	3	5-V tolerant Open-Drain
2	PA1		UART1_RX *[2]* / I2C0_SCL *[3]* / TIMG1_C1 *[4](Default BSL I2C_SCL)*	2	5	5	1	5	5	4	5-V tolerant Open-Drain
N/A	N/A	NRST		3	6	6	2				Reset(4)

Table 6-1. Pin Attributes (continued)

<table>
<tr><th rowspan="2">PINCMx</th><th rowspan="2">PIN NAME</th><th colspan="2">PIN FUNCTION</th><th colspan="7">PIN NUMBER</th><th rowspan="2">I/O STRUCTURE</th></tr>
<tr><th>ANALOG</th><th>DIGITAL(1)</th><th>32 VQFN</th><th>28 VSSOP (2)</th><th>28 VSSOP (3)</th><th>24 VQFN</th><th>20 VSSOP</th><th>16 WQFN</th><th>16 SOT</th></tr>
<tr><td>3</td><td>PA2</td><td>ROSC</td><td>TIMG1_C1 [2] / SPI0_CS0 [3]</td><td>6</td><td>9</td><td>9</td><td>5</td><td>8</td><td>8</td><td>7</td><td>Standard</td></tr>
<tr><td>4</td><td>PA3</td><td></td><td>TIMG2_C0 [2] / SPI0_CS1 [3] / UART1_CTS [4] / COMP0_OUT [5]</td><td>7</td><td>10</td><td>10</td><td>6</td><td>–</td><td>–</td><td>–</td><td>Standard</td></tr>
<tr><td>5</td><td>PA4</td><td></td><td>TIMG2_C1 [2] / SPI0_POCI [3] / UART1_RTS [4]</td><td>8</td><td>11</td><td>11</td><td>7</td><td>9</td><td>–</td><td>–</td><td>Standard</td></tr>
<tr><td>6</td><td>PA5</td><td></td><td>TIMG0_C0 [2] / SPI0_PICO [3]/FCC_IN[4]</td><td>9</td><td>12</td><td>12</td><td>–</td><td>–</td><td>9</td><td>–</td><td>High-Speed</td></tr>
<tr><td>7</td><td>PA6</td><td></td><td>TIMG0_C1 [2] / SPI0_SCK [3]</td><td>10</td><td>13</td><td>13</td><td>–</td><td>10</td><td>10</td><td>8</td><td>Standard</td></tr>
<tr><td>8</td><td>PA7</td><td></td><td>COMP0_OUT [2] / CLK_OUT [3] / TIMG1_C0 [4]</td><td>11</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>Standard</td></tr>
<tr><td>9</td><td>PA8</td><td></td><td>UART0_TX [2] / SPI0_CS0 [3] / UART1_RTS [4] / TIMG2_C0 [5]</td><td>12</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>Standard</td></tr>
<tr><td>10</td><td>PA9</td><td></td><td>UART0_RX [2] / SPI0_PICO [3] / UART1_CTS [4] / TIMG2_C1 [5]/ CLK_OUT[6]</td><td>13</td><td>14</td><td>14</td><td>8</td><td>–</td><td>–</td><td>–</td><td>Standard</td></tr>
<tr><td>11</td><td>PA10</td><td></td><td>UART1_TX [2] / SPI0_POCI [3] / I2C0_SDA [4] / TIMG4_C0 [5]/ CLK_OUT[6]</td><td>14</td><td>15</td><td>–</td><td>9</td><td>–</td><td>11</td><td>–</td><td>High-Speed</td></tr>
<tr><td>12</td><td>PA11</td><td></td><td>UART1_RX [2] / SPI0_SCK [3] / I2C0_SCL [4] / TIMG4_C1 [5] / COMP0_OUT [6]</td><td>15</td><td>16</td><td>–</td><td>10</td><td>11</td><td>–</td><td>–</td><td>Standard</td></tr>
<tr><td>13</td><td>PA12</td><td></td><td>UART0_CTS [2] / TIMG0_C0 [3]/ FCC_IN[4]</td><td>16</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>Standard</td></tr>
<tr><td>14</td><td>PA13</td><td></td><td>UART0_RTS [2] / TIMG0_C1 [3] / UART1_RX [4]</td><td>17</td><td>–</td><td>15</td><td>–</td><td>–</td><td>–</td><td>–</td><td>Standard</td></tr>
<tr><td>15</td><td>PA14</td><td></td><td>UART1_CTS [2] / CLK_OUT [3] / UART1_TX [4] / TIMG1_C0 [5]</td><td>18</td><td>17</td><td>16</td><td>–</td><td>–</td><td>11</td><td>–</td><td>Standard</td></tr>
<tr><td>16</td><td>PA15</td><td>A9</td><td>UART1_RTS [2] / I2C1_SCL [3] / SPI0_CS2 [4] / TIMG4_C1 [5]</td><td>19</td><td>18</td><td>17</td><td>11</td><td>–</td><td>12</td><td>–</td><td>Standard</td></tr>
<tr><td>17</td><td>PA16</td><td>A8 / OPA1_OUT</td><td>COMP0_OUT [2] / I2C1_SDA [3] / SPI0_POCI [4] / TIMG0_C0 [5]/FCC_IN[6]</td><td>20</td><td>19</td><td>18</td><td>12</td><td>12</td><td>13</td><td>–</td><td>Standard</td></tr>
<tr><td rowspan="2">18</td><td>PA17</td><td>OPA1_IN1-</td><td>UART0_TX [2] / I2C1_SCL [3] / SPI0_SCK [4] / TIMG4_C0 [5] / SPI0_CS1 [6]</td><td rowspan="2">21</td><td rowspan="2">20</td><td>19</td><td rowspan="2">13</td><td rowspan="2">13 (2)</td><td rowspan="2">–</td><td rowspan="2">9</td><td rowspan="2">Standard with wake</td></tr>
<tr><td>N/A</td><td>OPA1_IN0-</td><td></td><td>–</td></tr>
<tr><td>N/A</td><td>N/A</td><td colspan="2">OPA1_IN0-</td><td>–</td><td>–</td><td>20</td><td>–</td><td>13 (3)</td><td rowspan="2">14</td><td>–</td><td>Analog</td></tr>
<tr><td>19</td><td>PA18</td><td>A7 / OPA1_IN0+ / GPAMP_IN-</td><td>UART0_RX [2] / SPI0_PICO [3] / I2C1_SDA [4] / TIMG4_C1 [5](BSL Invoke)</td><td>22</td><td>21</td><td>21</td><td>14</td><td>14</td><td>10</td><td>Standard with wake</td></tr>
<tr><td>20</td><td>PA19</td><td></td><td>SWDIO [2] / I2C1_SDA [3] / SPI0_POCI [4]</td><td>23</td><td>22</td><td>22</td><td>15</td><td>15</td><td>15</td><td>11</td><td>High-Speed</td></tr>
<tr><td>21</td><td>PA20</td><td>A6 / COMP0_IN1+</td><td>SWCLK [2] / I2C1_SCL [3] / TIMG4_C0 [4]</td><td>24</td><td>23</td><td>23</td><td>16</td><td>16</td><td>16</td><td>12</td><td>Standard</td></tr>
<tr><td>22</td><td>PA21</td><td>A5 / VREF-</td><td>TIMG2_C0 [2] / UART0_CTS [3] / UART0_TX [4]</td><td>25</td><td>24</td><td>24</td><td>17</td><td>–</td><td>–</td><td>–</td><td>Standard</td></tr>
<tr><td>23</td><td>PA22</td><td>A4 / GPAMP_OUT / OPA0_OUT</td><td>UART0_RX [2] / TIMG2_C1 [3] / UART0_RTS [4] / CLK_OUT [5] / UART1_RX [6](Default BSL UART_RX)</td><td>26</td><td>25</td><td>25</td><td>18</td><td>17</td><td>1</td><td>13</td><td>Standard</td></tr>
</table>

Table 6-1. Pin Attributes (continued)

PINCMx	PIN NAME	PIN FUNCTION		PIN NUMBER							I/O STRUCTURE
		ANALOG	DIGITAL[(1)]	32 VQFN	28 VSSOP [(2)]	28 VSSOP [(3)]	24 VQFN	20 VSSOP	16 WQFN	16 SOT	
24	PA23	VREF+ / COMP0_IN1-	UART0_TX *[2]* / SPI0_CS3 *[3]* / TIMG0_C0 *[4]* / UART0_CTS *[5]* / UART1_TX *[6]* *(Default BSL UART_TX)*	27	26	26	19	18	2	14	Standard
25	PA24	A3 / OPA0_IN1- / OPA0_IN0-	SPI0_CS2 *[2]* / TIMG0_C1 *[3]* / UART0_RTS *[4]*	28	27	–	20	19[(2)]	–	15	Standard
N/A	N/A	OPA0_IN0-		–	–	27	–	19[(3)]	–	–	Analog
26	PA25	A2 / OPA0_IN0+	TIMG4_C1 *[2]* / UART0_TX *[3]* / SPI0_PICO *[4]*	29	28	28	21	20	2	16	Standard
27	PA26	A1 / GPAMP_IN+ / COMP0_IN0+	TIMG1_C0 *[2]* / UART0_RX *[3]* / SPI0_POCI *[4]*	30	1	1	22	1	–	1	Standard
28	PA27	A0 / COMP0_IN0-	TIMG1_C1 *[2]* / SPI0_CS3 *[3]*	31	2	2	–	2	–	–	Standard

(1) PINCM.PF and PINCM.PC in IOMUX must be set to 0 for analog functions (for example, OPA inputs or outputs or COMP inputs). Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which lets software configure the desired *Pin Function* using the PINCM.PF control bits.
(2) MSPM0L130x only
(3) MSPM0L134x only
(4) Reset PIN is muxed with PA1 for 16-pin and 20-pin devices.

Table 6-2. Digital IO Features by IO Type

IO STRUCTURE	INVERSION CONTROL	DRIVE STRENGTH CONTROL	HYSTERESIS CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR	WAKEUP LOGIC
Standard drive	Y			Y	Y	
Standard drive with wake	Y			Y	Y	Y
High speed	Y	Y		Y	Y	
5-V tolerant open drain	Y		Y		Y	Y

6.3 Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO. (1)							PIN TYPE (2)	DESCRIPTION
		32 VQFN	28 VSSOP (3)	28 VSSOP (4)	24 VQFN	20 VSSOP	16 WQFN	16 SOT		
ADC	A0	31	2	2	–	2	–	–	I	ADC0 analog input 0
	A1	30	1	1	22	1	–	1	I	ADC0 analog input 1
	A2	29	28	28	21	20	2	16	I	ADC0 analog input 2
	A3	28	27	–	20	19 (3)	–	15	I	ADC0 analog input 3
	A4	26	25	25	18	17	1	13	I	ADC0 analog input 4
	A5	25	24	24	17	–	–	–	I	ADC0 analog input 5
	A6	24	23	23	16	16	16	12	I	ADC0 analog input 6
	A7	22	21	21	14	14	14	10	I	ADC0 analog input 7
	A8	20	19	18	12	12	13	–	I	ADC0 analog input 8
	A9	19	18	17	11	–	12	–	I	ADC0 analog input 9
BSL	BSL_invoke	22	21	21	14	14	14	10	I	Input pin used to invoke bootloader
BSL (I^2C)	BSLSCL	2	5	5	1	5	5	4	I/O	Default I^2C BSL clock
	BSLSDA	1	4	4	24	4	4	3	I/O	Default I^2C BSL data
BSL (UART)	BSLRX	26	25	25	18	17	1	13	I	Default UART BSL receive
	BSLTX	27	26	26	19	18	2	14	O	Default UART BSL transmit
Clock	CLK_OUT	11 18 26	17 25	16 25	18	17	1 11	13	O	Configurable clock output
	ROSC	6	9	9	5	8	8	7	I	External resistor used for improving oscillator accuracy
Comparator	COMP0_IN0-	31	2	2	–	2	–	–	I	Comparator 0 inverting input 0
	COMP0_IN0+	30	1	1	22	1	–	1	I	Comparator 0 non-inverting input 0
	COMP0_IN1-	27	26	26	19	18	2	14	I	Comparator 0 inverting input 1
	COMP0_IN1+	24	23	23	16	16	16	12	I	Comparator 0 non-inverting input 1
	COMP0_OUT	7 11 15 20	10 16 19	10 18	6 12	11 12	13	–	O	Comparator 0 output
Debug	SWCLK	24	23	23	16	16	16	12	I	Serial wire debug input clock
	SWDIO	23	22	22	15	15	15	11	I/O	Serial wire debug data input/output
General-Purpose Amplifier	GPAMP_IN+	30	1	1	22	1	–	1	I	GPAMP non-inverting terminal input
	GPAMP_OUT	26	25	25	18	17	1	13	O	GPAMP output
	GPAMP_IN-	22	21	21	14	14	14	10	I	GPAMP inverting terminal input

FUNCTION	SIGNAL NAME	PIN NO. (1)							PIN TYPE (2)	DESCRIPTION
		32 VQFN	28 VSSOP (3)	28 VSSOP (4)	24 VQFN	20 VSSOP	16 WQFN	16 SOT		
GPIO	PA0	1	4	4	24	4	4	3	I/O	General-purpose digital I/O with wake up from SHUTDOWN
	PA1	2	5	5	1	5	5	4	I/O	General-purpose digital I/O with wake up from SHUTDOWN
	PA2	6	9	9	5	8	8	7	I/O	General-purpose digital I/O
	PA3	7	10	10	6	–	–	–	I/O	General-purpose digital I/O
	PA4	8	11	11	7	9	–	–	I/O	General-purpose digital I/O
	PA5	9	12	12	–	–	9	–	I/O	General-purpose digital I/O
	PA6	10	13	13	–	10	10	8	I/O	General-purpose digital I/O
	PA7	11	–	–	–	–	–	–	I/O	General-purpose digital I/O
	PA8	12	–	–	–	–	–	–	I/O	General-purpose digital I/O
	PA9	13	14	14	8	–	–	–	I/O	General-purpose digital I/O
	PA10	14	15	–	9	–	11	–	I/O	General-purpose digital I/O
	PA11	15	16	–	10	11	–	–	I/O	General-purpose digital I/O
	PA12	16	–	–	–	–	–	–	I/O	General-purpose digital I/O
	PA13	17	–	15	–	–	–	–	I/O	General-purpose digital I/O
	PA14	18	17	16	–	–	11	–	I/O	General-purpose digital I/O
	PA15	19	18	17	11	–	12	–	I/O	General-purpose digital I/O
	PA16	20	19	18	12	12	13	–	I/O	General-purpose digital I/O
	PA17	21	20	19	13	13 (3)	14	9	I/O	General-purpose digital I/O with wake up from SHUTDOWN
	PA18	22	21	21	14	14	14	10	I/O	General-purpose digital I/O with wake up from SHUTDOWN
	PA19	23	22	22	15	15	15	11	I/O	General-purpose digital I/O
	PA20	24	23	23	16	16	16	12	I/O	General-purpose digital I/O
	PA21	25	24	24	17	–	–	–	I/O	General-purpose digital I/O
	PA22	26	25	25	18	17	1	13	I/O	General-purpose digital I/O
	PA23	27	26	26	19	18	2	14	I/O	General-purpose digital I/O
	PA24	28	27	–	20	19 (3)	–	15	I/O	General-purpose digital I/O
	PA25	29	28	28	21	20	2	16	I/O	General-purpose digital I/O
	PA26	30	1	1	22	1	–	1	I/O	General-purpose digital I/O
	PA27	31	2	2	–	2	–	–	I/O	General-purpose digital I/O
I^2C	I2C0_SCL	2 15	5 16	5	1 10	5 11	5	4	I/O	I2C0 serial clock
	I2C0_SDA	1 14	4 15	4	24 9	4	4 11	3	I/O	I2C0 serial data
	I2C1_SCL	19 21 24	18 20 23	17 19 23	11 13 16	13 (3) 16	12 16	9 12	I/O	I2C1 serial clock
	I2C1_SDA	20 22 23	19 21 22	18 21 22	12 14 15	12 14 15	13 14 15	10 11	I/O	I2C1 serial data

FUNCTION	SIGNAL NAME	PIN NO. (1) 32 VQFN	28 VSSOP (3)	28 VSSOP (4)	24 VQFN	20 VSSOP	16 WQFN	16 SOT	PIN TYPE (2)	DESCRIPTION
Operational Amplifier with Chopping (Zero-Drift Op-Amp)	OPA0_IN0+	29	28	28	21	20	2	16	I	OPA0 non-inverting terminal input 0
	OPA0_IN0-	28	27	27	20	19	–	15	I	OPA0 inverting terminal input 0
	OPA0_IN1-	28	27	–	20	19 (3)	–	15	I	OPA0 inverting terminal input 1
	OPA0_OUT	26	25	25	18	17	1	13	O	OPA0 output
	OPA1_IN0+	22	21	21	14	14	14	10	I	OPA1 non-inverting terminal input 0
	OPA1_IN0-	21	20	20	13	13	14	9	I	OPA1 inverting terminal input 0
	OPA1_IN1-	21	20	19	13	13 (3)	–	9	I	OPA1 inverting terminal input 1
	OPA1_OUT	20	19	18	12	12	13	–	O	OPA1 output
Power	VSS	5	8	8	4	7	7	6	P	Ground supply
	VDD	4	7	7	3	6	6	5	P	Power supply
	VCORE	32	3	3	23	3	3	2	P	Regulated core power supply output
	QFN Pad	Pad	–	–	Pad	–	Pad	–	P	QFN package exposed thermal pad. TI recommends connection to V_{SS}.
SPI	SPI0_CS0	6 12	9	9	5	8	8	7	I/O	SPI0 chip-select 0
	SPI0_CS1	1 7 21	4 10 20	4 10 19	6 13 24	4 13 (3)	4	3 9	I/O	SPI0 chip-select 1
	SPI0_CS2	19 28	18 27	17	11 20	19 (3)	12	15	I/O	SPI0 chip-select 2
	SPI0_CS3	27 31	2 26	2 26	19	2 18	2	14	I/O	SPI0 chip-select 3
	SPI0_SCK	10 15 21	13 16 20	13 19	10 13	10 11 13 (3)	10	8 9	I/O	SPI0 clock signal input – SPI peripheral mode Clock signal output – SPI controller mode
	SPI0_POCI	8 14 20 23 30	1 11 15 19 22	1 11 18 22	7 9 12 15 22	1 9 12 15	11 13 15	1 11	I/O	SPI0 controller in/peripheral out
	SPI0_PICO	9 13 22 29	12 14 21 28	12 14 21 28	8 14 21	14 20	2 9 14	10 16	I/O	SPI0 controller out/peripheral in
System	NRST	3	6	6	2	5	5	4	I	Reset input active low

FUNCTION	SIGNAL NAME	PIN NO. [1]							PIN TYPE [2]	DESCRIPTION
		32 VQFN	28 VSSOP [3]	28 VSSOP [4]	24 VQFN	20 VSSOP	16 WQFN	16 SOT		
Timer	TIMG0_C0	9 16 20 27	12 19 26	12 18 26	12 19	12 18	2 9 13	14	I/O	General purpose timer 0 CCR0 capture input/ compare output
	TIMG0_C1	10 17 28	13 27	13 15	20	10 19 [3]	10	8 15	I/O	General purpose timer 0 CCR1 capture input/ compare output
	TIMG1_C0	1 11 18 30	1 4 17	1 4 16	22 24	1 4	4 11	1 3	I/O	General purpose timer 1 CCR0 capture input/ compare output
	TIMG1_C1	2 6 31	2 5 9	2 5 9	1 5	2 5 8	5 8	4 7	I/O	General purpose timer 1 CCR1 capture input/ compare output
	TIMG2_C0	7 12 25	10 24	10 24	6 17	–	–	–	I/O	General purpose timer 2 CCR0 capture input/ compare output
	TIMG2_C1	8 13 26	11 14 25	11 14 25	7 8 18	9 17	1	13	I/O	General purpose timer 2 CCR1 capture input/ compare output
	TIMG4_C0	14 21 24	15 20 23	19 23	9 13 16	13 [3] 16	11 16	9 12	I/O	General purpose timer 4 CCR0 capture input/ compare output
	TIMG4_C1	15 19 22 29	16 18 21 28	17 21 28	10 11 14 21	11 14 20	2 12 14	10 16	I/O	General purpose timer 4 CCR1 capture input/ compare output

FUNCTION	SIGNAL NAME	PIN NO. (1)							PIN TYPE (2)	DESCRIPTION
		32 VQFN	28 VSSOP (3)	28 VSSOP (4)	24 VQFN	20 VSSOP	16 WQFN	16 SOT		
UART	UART0_TX	12 21 25 27 29	20 24 26 28	19 24 26 28	13 17 19 21	13 (3) 18 20	2	9 14 16	O	UART0 transmit data
	UART0_RX	13 22 26 30	1 14 21 25	1 14 21 25	8 14 18 22	1 14 17	1 14	1 10 13	I	UART0 receive data
	UART0_CTS	16 25 27	24 26	24 26	17 19	18	2	14	I	UART0 "clear to send" flow control input
	UART0_RTS	17 26 28	25 27	15 25	18 20	17 19 (3)	1	13 15	O	UART0 "request to send" flow control output
	UART1_TX	1 14 18 27	4 15 17 26	4 16 26	9 19 24	4 18	2 4 11	3 14	O	UART1 transmit data
	UART1_RX	2 15 17 26	5 16 25	5 15 25	1 10 18	5 11 17	1 5	4 13	I	UART1 receive data
	UART1_CTS	7 13 18	10 14 17	10 14 16	6 8	–	11	–	I	UART1 "clear to send" flow control input
	UART1_RTS	8 12 19	11 18	11 17	7 11	9	12	–	O	UART1 "request to send" flow control output
Voltage Reference(5)	VREF+	27	26	26	19	18	2	14	I	Voltage reference power supply - external reference input
	VREF-	25	24	24	17	–	–	–	I	Voltage reference ground supply - external reference input

(1) – = not available
(2) I = input, O = output, I/O = input or output, P = power
(3) MSPM0L130x only
(4) MSPM0L134x only
(5) When using VREF+ and VREF- to bring in an external voltage reference for analog peripherals such as the ADC, a decoupling capacitor must be placed on VREF+ to VREF-/GND with a capacitance based on the external reference source

6.4 Connections for Unused Pins

Table 6-3 lists the correct termination of unused pins.

Table 6-3. Connection of Unused Pins

PIN (1)	POTENTIAL	COMMENT
PAx	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup or pulldown resistor.
OPAx_IN0-	Open	This pin is high-impedance
NRST	VCC	NRST is an active-low reset signal; the pin must be pulled high to VCC or the device cannot start. For more information, see Section 9.1.

(1) Any unused pin with a function that is shared with general-purpose I/O must follow the "PAx" unused pin connection guidelines.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin, with respect to VSS	–0.3	4.1	V
V_I	Input voltage	Applied to any 5-V tolerant open-drain pins	–0.3	5.5	V
V_I	Input voltage	Applied to any common tolerance pins	–0.3	V_{DD} + 0.3 (4.1 MAX)	V
I_{VDD}	Current into VDD pin (source)	-40℃ ≤ Tj ≤ 130℃		80	mA
		-40℃ ≤ Tj ≤ 85℃		100	mA
I_{VSS}	Current out of VSS pin (sink)	-40℃ ≤ Tj ≤ 130℃		80	mA
		-40℃ ≤ Tj ≤ 85℃		100	mA
I_{IO}	Current for SDIO pin	Current sunk or sourced by SDIO pin		6	mA
	Current for HSIO pin	Current sunk or sourced by HSIO pin		6	mA
	Current for ODIO pin	Current sunk by ODIO pin		20	mA
I_D	Supported diode current	Diode current at any device pin		±2	mA
Tj	Junction temperature		-40	130	°C
T_{stg}	Storage temperature		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.62		3.6	V
VCORE	Voltage on VCORE pin (2)		1.35		V
C_{VDD}	Capacitor placed between VDD and VSS (1)		10		uF
C_{VCORE}	Capacitor placed between VCORE and VSS (1) (2)		470		nF
T_A	Ambient temperature, T version	–40		105	°C
	Ambient temperature, S version	–40		125	
T_J	Max junction temperature, T version			125	°C
T_J	Max junction temperature, S version			130	°C
f_{MCLK}	MCLK, CPUCLK, ULPCLK frequency with 1 flash wait state (3)			32	MHz
	MCLK, CPUCLK, ULPCLK frequency with 0 flash wait states (3)			24	

(1) Connect C_{VDD} and C_{VCORE} between VDD/VSS and VCORE/VSS, respectively, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD} and C_{VCORE}.
(2) The VCORE pin must only be connected to C_{VCORE}. Do not supply any voltage or apply any external load to the VCORE pin.

(3) Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software.

7.4 Thermal Information

THERMAL METRIC[(1)]		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-32 (RHB)	36.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		28.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		17.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		17.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		6.9	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VSSOP-28 (DGS28)	78.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		38.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		41.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		3.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		41.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-24 (RGE)	44.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		38.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		21.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		21.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		7.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VSSOP-20 (DGS20)	91.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		29.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		48.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		47.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	SOT-16 (DYY)	86.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		39.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		27.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		27.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Supply Current Characteristics

7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER		MCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
RUN Mode													
IDD_{RUN}	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	2.3		2.3		2.3		2.3		2.4		mA
		4MHz	0.52		0.52		0.54		0.56		0.60		

7.5.1 RUN/SLEEP Modes (continued)

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER		MCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IDD_{RUN}, per MHz	MCLK=SYSOSC, While(1), execute from flash	32MHz	40	48	40	50	41	50	42	51	43	56	uA/Mhz
	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	72		72		72		73		74		
	MCLK=SYSOSC, CoreMark, execute from flash	4MHz	130		130		135		140		150		
SLEEP Mode													
IDD_{SLEEP}	MCLK=SYSOSC, CPU is halted	32MHz	967	1047	978	1066	1002	1192	1024	1301	1070	1416	uA
		4MHz	356	416	363	441	389	577	411	689	458	809	

7.5.2 STOP/STANDBY Modes

VDD=3.3V unless otherwise noted. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
STOP Mode													
IDD_{STOP0}	SYSOSC=32MHz, USE4MHZSTOP=0, DISABLESTOP=0	4MHz	316	342	320	344	323	347	327	352	334	361	uA
IDD_{STOP1}	SYSOSC=4MHz, USE4MHZSTOP=1, DISABLESTOP=0	4MHz	146	167	151	171	155	176	158	182	166	192	
IDD_{STOP2}	SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK	32kHz	42	51	44	54	47	58	50	64	56	76	
STANDBY Mode													
IDD_{STBY0}	STOPCLKSTBY=0, TIMG0 enabled	32kHz	1.2	1.3	1.3	1.7	2.7	6.2	4.7	12	11	25	uA
IDD_{STBY1}	STOPCLKSTBY=1, TIMG0 enabled		0.9	1.0	1.0	1.4	2.4	5.9	4.4	12	11	25	
	STOPCLKSTBY=1, GPIOA enabled		0.9	1.0	1.0	1.4	2.4	5.9	4.4	12	10	25	

7.5.3 SHUTDOWN Mode

All inputs tied to 0V or VDD. Outputs do not source or sink any current. Core regulator is powered down.

PARAMETER		VDD	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IDD_{SHDN}	Supply current in SHUTDOWN mode	3.3V	47		61		352		793		2020		nA

7.6 Power Supply Sequencing

7.6.1 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dVDD/dt	VDD (supply voltage) slew rate	Rising			1	V/us
		Falling (2)			0.01	
		Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising (1)	0.95	1.30	1.51	V
V_{POR-}		Falling (1)	0.9	1.25	1.48	V

7.6.1 POR and BOR (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HYS, POR}$	POR hysteresis	(1)	30	45	60	mV
$V_{BOR0+, COLD}$	Brown-out reset voltage level 0 (default level)	Cold start, rising (1)	1.54	1.58	1.62	V
V_{BOR0+}		Rising (1) (2)	1.54	1.59	1.62	
V_{BOR0-}		Falling (1) (2)	1.53	1.58	1.61	
$V_{BOR0, STBY}$		STANDBY mode (1)	1.51	1.57	1.61	
V_{BOR1+}	Brown-out-reset voltage level 1	Rising (1) (2)	2.13	2.18	2.23	V
V_{BOR1-}		Falling (1) (2)	2.10	2.15	2.19	
V_{BOR2+}	Brown-out-reset voltage level 2	Rising (1) (2)	2.72	2.77	2.82	V
V_{BOR2-}		Falling (1) (2)	2.69	2.74	2.79	
V_{BOR3+}	Brown-out-reset voltage level 3	Rising (1) (2)	2.91	2.97	3.02	V
V_{BOR3-}		Falling (1) (2)	2.88	2.94	2.99	
$V_{HYS,BOR}$	Brown-out reset hysteresis	Level 0 (1)		15	21	mV
		Levels 1-3 (1)		34	40	
$T_{PD, BOR}$	BOR propagation delay	RUN/SLEEP/STOP mode			10	us
		STANDBY mode			100	us

(1) |dVDD/dt| ≤ 3V/s
(2) Device operating in RUN, SLEEP, or STOP mode.

7.6.2 Power Supply Ramp

Figure 7-1 gives the relationship of POR- POR+, BOR0-, and BOR0+ during power-up and power-down.

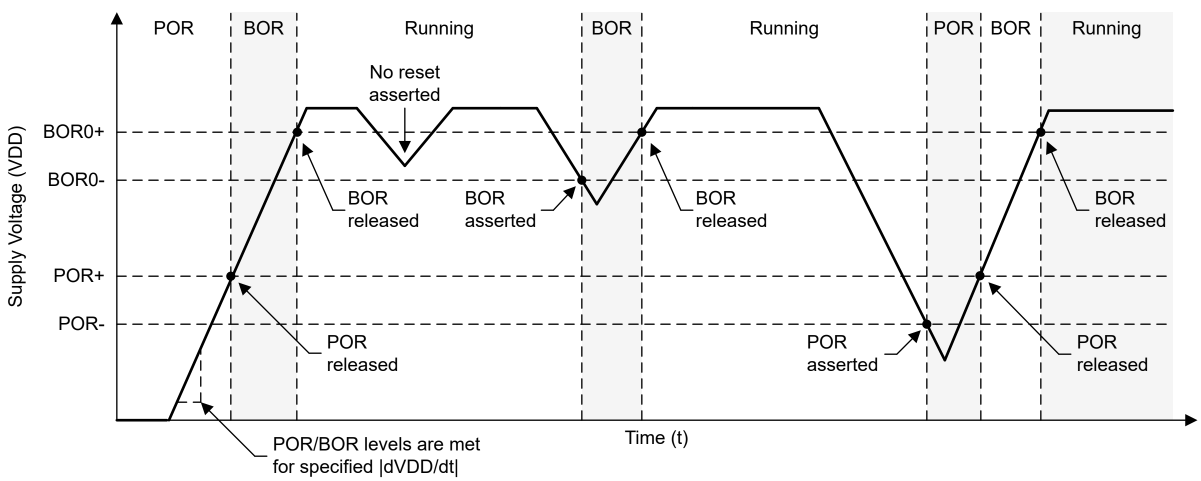


Figure 7-1. Power Cycle POR/BOR Conditions

7.7 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
$VDD_{PGM/ERASE}$	Program and erase supply voltage		1.62		3.6	V
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta		2		mA

7.7 Flash Memory Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta		2.5		mA
Endurance						
$NWEC_{(LOWER)}$	Erase/program cycle endurance (lower 32kB flash) (1)		100			k cycles
$NWEC_{(UPPER)}$	Erase/program cycle endurance (remaining flash) (1)		10			k cycles
$NE_{(MAX)}$	Total erase operations before failure (2)		802			k erase operations
$NW_{(MAX)}$	Write operations per word line before sector erase (3)				83	write operations
Retention						
t_{RET_85}	Flash memory data retention	-40°C ≤T_j ≤ 85°C	60			years
t_{RET_105}	Flash memory data retention	-40°C ≤T_j ≤ 105°C	11.4			years
Program and Erase Timing						
$t_{PROG\ (WORD,\ 64)}$	Program time for flash word (4) (6)			50	275	µs
$t_{PROG\ (SEC,\ 64)}$	Program time for 1kB sector (5) (6)			6.4		ms
$t_{ERASE\ (SEC)}$	Sector erase time	≤2k erase/program cycles, T_j≥25°C		4	20	ms
$t_{ERASE\ (SEC)}$	Sector erase time	≤10k erase/program cycles, T_j≥25°C		20	150	ms
$t_{ERASE\ (SEC)}$	Sector erase time	≤10k erase/program cycles		20	200	ms
$t_{ERASE\ (BANK)}$	Bank erase time	≤10k erase/program cycles		22	220	ms

(1) The lower 32kB flash address space supports higher erase/program endurance to enable EEPROM emulation applications. On devices with <=32kB flash memory, the entire flash memory supports $NWEC_{(LOWER)}$ erase/program cycles.
(2) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.
(3) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.
(4) Program time is defined as the time from when the program command is triggered until the command completion interrupt flag is set in the flash controller.
(5) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.
(6) Flash word size is 64 data bits (8 bytes). On devices with ECC, the total flash word size is 72 bits (64 data bits plus 8 ECC bits).

7.8 Timing Characteristics

VDD=3.3V, T_a=25 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wakeup Timing						
$t_{WAKE,\ SLEEP}$	Wakeup time from SLEEP to RUN (1)			2		cycles
$t_{WAKE,\ STOP}$	Wakeup time from STOP1 to RUN (SYSOSC enabled) (1)			14		us
	Wakeup time from STOP2 to RUN (SYSOSC disabled) (1)			13		us
$t_{WAKE,\ STBY}$	Wakeup time from STANDBY to RUN (1)			15		us
$t_{WAKE,\ SHDN}$	Wakeup time from SHUTDOWN to RUN	Fast boot enabled		214		us
$t_{WAKE,\ SHDN}$	Wakeup time from SHUTDOWN to RUN	Fast boot disabled		230		us

7.8 Timing Characteristics (continued)

VDD=3.3V, T_a=25 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Asynchronous Fast Clock Request Timing						
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP2		0.9		us
		Mode is STOP1		2.4		us
		Mode is STOP2		0.9		us
		Mode is STANDBY1		3.2		us
Startup Timing						
$t_{START, RESET}$	Device cold start-up time from reset/ power-up (2)	Fast boot enabled		241		us
		Fast boot disabled		284		us
NRST Timing						
$t_{RST, BOOTRST}$	Minimum pulse length on NRST pin to generate BOOTRST	ULPCLK≥4MHz		2		us
		ULPCLK=32kHz		100		us
$t_{RST, POR}$	Minimum pulse length on NRST pin to generate POR			1		s

(1) The wake-up time is measured from the edge of an external signal (GPIO wake-up event) to the time that the first CPU instruction is executed, with the GPIO glitch filter disabled (FILTEREN=0x0) and fast wake enabled (FASTWAKEONLY=1)
(2) The start-up time is measured from the time that VDD crosses VBOR0+ (cold start-up) to the time that the first instruction of the user program is executed.

7.9 Clock Specifications

7.9.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=00 (BASE)		32		MHz
		SYSOSCCFG.FREQ=01		4		MHz
	User trimmed SYSOSC frequency	SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=10		24		MHz
		SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=01		16		MHz
	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled and an ideal ROSC resistor is assumed (1) (2)	SETUSEFCL=1, T_a = 25 ℃	-0.41		0.58	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 85 ℃	-0.80		0.93	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 105 ℃	-0.80		1.09	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃	-0.80		1.30	%
	SYSOSC accuracy when frequency correction loop (FCL) is enabled, with R_{OSC} resistor put at R_{OSC} pin), for factory trimmed frequencies (1)	SETUSEFCL=1, T_a = 25 ℃, ±0.1% ±25ppm R_{OSC}	–0.5		0.7	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 85 ℃, ±0.1% ±25ppm R_{OSC}	–1.1		1.2	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 105 ℃, ±0.1% ±25ppm R_{OSC}	–1.1		1.4	%
		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃, ±0.1% ±25ppm R_{OSC}	–1.1		1.7	%
	SYSOSC accuracy when frequency correction loop (FCL) is disabled, 32MHz	SETUSEFCL=0, SYSOSCCFG.FREQ=00, -40 ℃ ≤ T_a ≤ 125 ℃	–2.6		1.8	%
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, for factory trimmed frequencies, 4MHz	SETUSEFCL=0, SYSOSCCFG.FREQ=01, -40 ℃ ≤ T_a ≤ 125 ℃	–2.7		2.3	%
R_{OSC}	External resistor put between ROSC pin and VSS (1)	SETUSEFCL=1		100		kΩ

7.9.1 System Oscillator (SYSOSC) (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{settle, SYSOSC}$	Settling time to target accuracy (3)	SETUSEFCL=1, ±0.1% 25ppm R_{OSC} (1)			30	us
$f_{settle, SYSOSC}$	f_{SYSOSC} additional undershoot accuracy during t_{settle} (3)	SETUSEFCL=1, ±0.1% 25ppm R_{OSC} (1)	-11			%

(1) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an external reference resistor (R_{OSC}) which must be connected between the device ROSC pin and VSS when using the FCL. Accuracies are shown for a ±0.1% ±25ppm R_{OSC}; relaxed tolerance resistors may also be used (with reduced SYSOSC accuracy). See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy for various R_{OSC} accuracies. R_{OSC} does not need to be populated if the FCL is not enabled.

(2) Represents the device accuracy only. The tolerance and temperature drift of the ROSC resistor used must be combined with this spec to determine final accuracy. Performance for a ±0.1% ±25ppm R_{OSC} is given as a reference point.

(3) When SYSOSC is waking up (for example, when exiting a low power mode) and FCL is enabled, the SYSOSC will initially undershoot the target frequency f_{SYSOSC} by an additional error of up to $f_{settle,SYSOSC}$ for the time $t_{settle,SYSOSC}$, after which the target accuracy is achieved.

7.9.1.1 SYSOSC Typical Frequency Accuracy

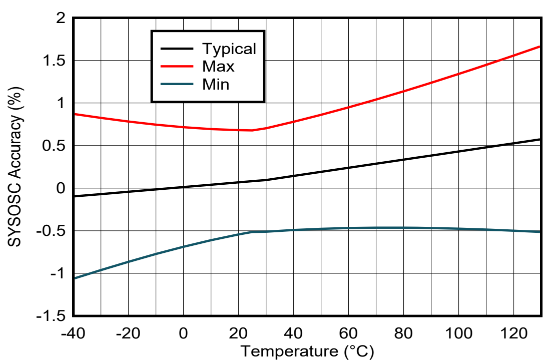


Figure 7-2. SYSOSC Accuracy with FCL On (32MHz)

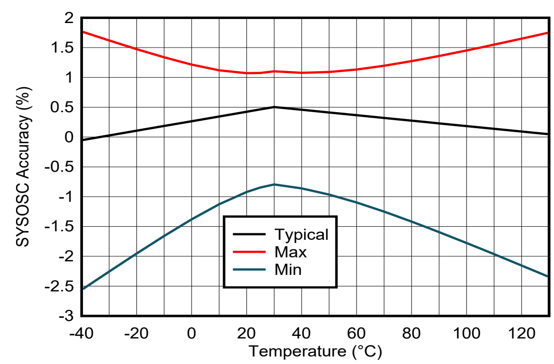


Figure 7-3. SYSOSC Accuracy with FCL Off (32MHz)

FCL-on accuracy is based on a 0.1% tolerance 25 ppm/°C ROSC resistor.

7.9.2 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	LFOSC frequency			32768		Hz
	LFOSC accuracy	-40 °C ≤ T_a ≤ 125 °C	–5		5	%
		-40 °C ≤ T_a ≤ 85 °C	–3		3	%
$t_{start, LFOSC}$	LFOSC start-up time			1.7		ms

7.10 Digital IO

7.10.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	ODIO (1)	VDD≥1.62V	0.7*VDD		5.5	V
			VDD≥2.7V	2		5.5	V
		All I/O except ODIO & Reset	VDD≥1.62V	0.7*VDD		VDD+0.3	V

7.10.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low level input voltage	ODIO	VDD≥1.62V	-0.3		0.3*VDD	V
			VDD≥2.7V	-0.3		0.8	V
		All I/O except ODIO & Reset	VDD≥1.62V	-0.3		0.3*VDD	V
V_{HYS}	Hysteresis	ODIO		0.05*VDD			V
		All I/O except ODIO		0.1*VDD			V
I_{lkg}	High-Z leakage current	SDIO(2) (3)				±50	nA
R_{PU}	Pull up resistance	All I/O except ODIO			40		kΩ
R_{PD}	Pull down resistance				40		kΩ
C_I	Input capacitance				5		pF
V_{OH}	High level output voltage	SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤25 °C	VDD-0.4			V
			VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤130 °C	VDD-0.45			
		HSIO	VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_j≤25 °C	VDD-0.4			
			VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_j≤130 °C	VDD-0.4			
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, DRV=0, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤25 °C	VDD-0.45			
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤130 °C	VDD-0.45			

7.10.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤25 °C			0.4	V
			VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤130 °C			0.45	
		HSIO	VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA T_j≤85 °C			0.4	
			VDD≥2.7V, DRV=1, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, DRV=1, $\|I_{IO}\|_{,max}$=3mA VDD≥1.62V, DRV=1, $\|I_{IO}\|_{,max}$=2mA -40 °C ≤T_j≤130 °C			0.45	
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, DRV=0, $\|I_{IO}\|_{,max}$=1.5mA T_j≤85 °C			0.4	
			VDD≥2.7V, DRV=0, $\|I_{IO}\|_{,max}$=4mA VDD≥1.71V, DRV=0, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, DRV=0, $\|I_{IO}\|_{,max}$=1.5mA -40 °C ≤T_j≤130 °C			0.45	
		ODIO	VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA -40 °C ≤T_j≤25 °C			0.4	
			VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA -40 °C ≤T_j≤130 °C			0.45	

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed
(2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

7.10.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency	SDIO [(1)]	VDD ≥ 1.71V, C_L= 20pF			16	MHz
			VDD ≥ 2.7V, CL= 20pF			32	
		HSIO	VDD ≥ 1.71V, DRV = 0, CL= 20pF			16	
			VDD ≥ 1.71V, DRV = 1, CL= 20pF			24	
			VDD ≥ 2.7V, DRV = 0, CL= 20pF			32	
		ODIO	VDD ≥ 1.71V, FM⁺, CL= 20pF - 100pF			1	
t_r,t_f	Output rise/fall time	All output ports except ODIO	VDD ≥ 1.71V			$0.3*f_{max}$	s
t_f	Output fall time	ODIO	VDD ≥ 1.71V, FM⁺, CL= 20pF-100pF	20*VDD/5.5		120	ns

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed

7.11 Analog Mux VBOOST

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBST}	VBOOST current adder	MCLK/ULPCLK is LFCLK		0.8		uA
		MCLK/ULPCLK is not LFCLK		8.5		
$t_{START,VBST}$	VBOOST startup time			12		us

7.12 ADC

7.12.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Vin_{(ADC)}$	Analog input voltage range(1)	Applies to all ADC analog input pins	0		VDD	V
V_{R+}	Positive ADC reference voltage	V_{R+} sourced from VDD		VDD		V
		V_{R+} sourced from external reference pin (VREF+)	1.4		VDD	V
		V_{R+} sourced from internal reference (VREF)		VREF		V
V_{R-}	Negative ADC reference voltage			0		V
F_S	ADC sampling frequency	RES = 0x0 (12-bit mode), External Reference			1.68	Msps
$I_{(ADC)}$ (2)	Operating supply current into VDD terminal	F_S = 1MSPS, Internal reference OFF, V_{R+} = VDD		454	600	µA
		F_S = 200ksps, Internal reference ON, V_{R+} = VREF = 2.5V		300	435	
$C_{S/H}$	ADC sample-and-hold capacitance			3.3	7	pF
Rin	ADC sampling switch resistance			0.5	1	kΩ
ENOB	Effective number of bits	Internal reference, V_{R+} = VREF = 2.5V, F_{in} = 10KHz	10	10.2		bit
		External reference, F_{in} = 10KHz (4)	11	11.1		
SNR	Signal-to-noise ratio	External reference (3)	68	71		dB
		Internal reference, V_{R+} = VREF = 2.5V	63	65		
$PSRR_{DC}$	Power supply rejection ratio, DC	External reference (3), VDD = $VDD_{(min)}$ to $VDD_{(max)}$	63	68		dB
		VDD = $VDD_{(min)}$ to $VDD_{(max)}$ Internal reference, V_{R+} = VREF = 2.5V	49	55		
$PSRR_{AC}$	Power supply rejection ratio, AC	External reference (3), ΔVDD = 0.1 V at 1 kHz		61		dB
		ΔVDD = 0.1 V at 1 kHz Internal reference, V_{R+} = VREF = 2.5V		49		
T_{wakeup}	ADC Wakeup Time	Assumes internal reference is active		1		us
$V_{SupplyMon}$	Supply Monitor voltage divider (VDD/3) accuracy	ADC input channel: Supply Monitor(4)	-1.5		+1.5	%
$I_{SupplyMon}$	Supply Monitor voltage divider current consumption	ADC input channel: Supply Monitor		10		uA

(1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) The internal reference (VREF) supply current is not included in current consumption parameter $I_{(ADC)}$.
(3) All external reference specifications are measured with V_{R+} = VREF+ = VDD = 3.3V and V_{R-} = VREF- = VSS = 0V
(4) Analog power supply monitor. Analog input on channel 15 is disconnected and is internally connected to the voltage divider which is VDD/3.

7.12.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{ADCCLK}	ADC clock frequency		4		32	MHz
$t_{ADC\ trigger}$	Software trigger minimum width		3			ADCCLK cycles
t_{Sample}	Sampling time without OPA	12-bit mode, R_S = 50Ω, C_{pext} = 10pF		62.5		ns

7.12.2 Switching Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{Sample_PGA}	Sampling time with OPA (1)	12-bit mode	GBW = 0x1, PGA gain = x1		0.22		µs
			GBW = 0x1, PGA gain = x32		1.5		µs
t_{Sample_GPAMP}	Sampling time with GPAMP				1.5		µs
$t_{Sample\_SupplyMon}$	Sample time with Supply Monitor (VDD/3)				2		µs

(1) Only applies for devices with OPA

7.12.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (INL)	External reference (2)	-2.0		+2.0	LSB
E_D	Differential linearity error (DNL) Guaranteed no missing codes	External reference (2)	-1.0		+1.0	LSB
E_O	Offset error	External reference (2)	-3		3	mV
		Internal reference, V_{R+} = VREF = 2.5V	-3		3	mV
E_G	Gain error	External reference (2)	-3		3	LSB

(1) Total Unadjusted Error (TUE) can be calculated from E_I , E_O , and E_G using the following formula: TUE = $\sqrt{E_I^2 + |E_O|^2 + E_G^2}$
Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate
(2) All external reference specifications are measured with V_{R+} = VREF+ = VDD and V_{R-} = VSS = 0V

7.12.4 Typical Connection Diagram

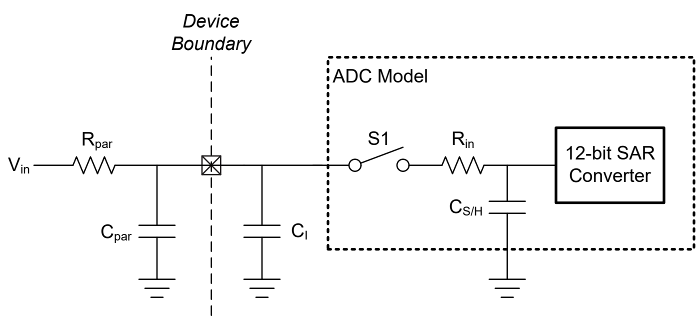


Figure 7-4. ADC Input Network

1. Refer to ADC Electrical Characteristics for the values of R_{in} and $C_{S/H}$
2. Refer to Digital IO Electrical Characteristics for the value of C_I
3. C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1. $Tau = (R_{par} + R_{in}) * C_{S/H} + R_{par} * (C_{par} + C_I)$
2. $K = \ln(2^n/\text{Settling error}) - \ln((C_{par} + C_I)/C_{S/H})$
3. T (Min sampling time) = K*Tau

7.13 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS_{TRIM}	Factory trim temperature (1)		27	30	33	℃
TS_c	Temperature coefficient		-1.84	-1.75	-1.66	mV/℃
$t_{SET, TS}$	Temperature sensor settling time (2)			2.5	10	us

(1) Higher absolute accuracy may be achieved through user calibration.

(2) This is the maximum time required for the temperature sensor to settle when measured by the ADC. It may be used to specify the minimum ADC sample time when measuring the temperature sensor.

7.14 VREF

7.14.1 Voltage Characterisitcs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 1	1.62			V
		BUFCONFIG = 0	2.7			
VREF	Voltage reference output voltage	BUFCONFIG = 1	1.379	1.4	1.421	V
		BUFCONFIG = 0	2.462	2.5	2.538	

7.14.2 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VREF}	VREF operating supply current	BUFCONFIG = {0, 1}, No load		74	100	µA
TC_{VREF}	Temperature coefficient of VREF (2)	BUFCONFIG = {0, 1}			200	ppm/°C
TC_{drift}	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25℃			300	ppm
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD = 1.7 V to VDDmax, BUFCONFIG = 1	59	64		dB
		VDD = 2.7 V to VDDmax, BUFCONFIG = 0	49	53		
V_{noise}	RMS noise at VREF output (0.1 Hz to 100 MHz)	BUFFCONFIG = 1		500		µVrms
		BUFFCONFIG = 0		750		
ADC F_S	Max supported ADC sampling frequency	Using VREF as ADC reference			200	ksps
$T_{startup}$	VREF startup time	BUFCONFIG = {0, 1} , VDD = 2.8 V			15	us

(1) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.

7.15 *COMP*

7.15.1 Comparator Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparator Electrical Characteristics						
Vcm	Common mode input range		0		VDD	V
V_{offset}	Input offset voltage				±25	mV
V_{hys}	DC input hysteresis			0.4		mV
				11		
				20		
				30		
t_{PD_ls}	Propagation delay, response time	Output Filter off, Overdrive = 100 mV, High Speed Mode		32	50	ns
		Output Filter off, Overdrive = 100 mV, Low Power Mode			5	µs
t_{en}	Comparator enable time	Startup time to reach propagation delay specification, High Speed Mode			10	µs
		Startup time to reach propagation delay specification, Low Power Mode			10	µs

7.15.1 Comparator Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{comp}	Comparator current consumption.	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, High Speed Mode		120	200	µA
		Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, Low Power Mode		0.8	2.7	µA
		Vcm = VDD/2, 100mV overdrive, comparator only. High Speed Mode		100	180	µA
		Vcm = VDD/2, 100mV overdrive, comparator only, Low Power Mode		0.7	2.1	µA
8-bit DAC Electrical Characteristics						
V_{dac}	DAC output range		0		VDD	V
$V_{dac\text{-}code}$	8-bit DAC output voltage for a given code	VIN = reference voltage into 8-bit DAC, code n = 0 to 255		VIN × (n+1) / 256		V
INL	Integral nonlinearity of 8-bit DAC		-1		1	LSB
DNL	Differential nonlinearity of 8-bit DAC		-1		1	LSB
Gain error	Gain error of 8-bit DAC	Reference voltage = VDD	-2		2	% of FSR
Offset error	Offset error of 8-bit DAC		-5		5	mV

7.16 GPAMP

7.16.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CM}	Common mode voltage range	RRI = 0x0		-0.1		VDD–1	V
		RRI = 0x1		1		VDD-0.2	
		RRI = 0x2		-0.1		VDD-0.2	
I_q	Quiescent current, per op-amp	I_O= 0 mA, RRI = 0x0			97		µA
		I_O= 0 mA, RRI = 0x1 or 0x2			93		
GBW	Gain-bandwidth product	C_L = 200pF			0.32		MHz
V_{OS}	Input offset voltage	Noninverting, unity gain, T_A = 25°C, VDD = 3.3V	CHOP = 0x0		±0.2	±6.5	mV
			CHOP = 0x1 or 0x2		±0.08	±0.4	
dV_{OS}/dT	Input offset voltage temperature drift	Noninverting, unity gain	CHOP = 0x0		7.7		µV/°C
			CHOP = 0x1 or 0x2		0.34		
I_{bias}	Input bias for muxed I/O pin at SoC	0.1V<V_{in}<VDD-0.3V, VDD=3.3V, CHOP=0x0	T_A = 25°C		±40		pA
			T_A = 125°C		±4000		
		0.1V<V_{in}<VDD-0.3V, VDD=3.3V, CHOP=0x1	T_A = 25°C		±200		
			T_A = 125°C		±4000		
$CMRR_{DC}$	Common mode rejection ratio, DC	Over common mode voltage range	CHOP = 0x0	48	77		dB
			CHOP = 0x1 or 0x2	56	105		
e_n	Input voltage noise density	Noninverting, unity gain	f = 1 kHz		43		nV/√Hz
			f = 10 kHz		19		
R_{in}	Input resistance[(1)]				0.65		kΩ
C_{in}	Input capacitance	Common mode			4		pF
		Differential			2		
A_{OL}	Open-loop voltage gain, DC	R_L = 350 kΩ, 0.3 < Vo < VDD-0.3		82	90	107	dB

7.16.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PM	phase margin	C_L = 200 pF, R_L= 350 kΩ	69	70	72	degree
SR	Slew rate	Noninverting, unity gain, C_L = 40 pF		0.32		V/µs
THDN	Total Harmonic Distortion + Noise			0.012		%
I_{Load}	Output load current			±10		µA
C_{Load}	Output load capacitance				200	pF

(1) The term 'Rin' refers to the input resistance of the multiplexer (mux) in the GPAMP.

7.16.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{EN}	GPAMP enable time	ENABLE = 0x0 to 0x1, Bandgap reference ON, 0.1%	Noninverting, unity gain		12	20	µs
$t_{disable}$	GPAMP disable time				4		ULPCLK Cycles
t_{SETTLE}	GPAMP settling time	C_L = 200 pF, Vstep = 0.3V to VDD - 0.3V, 0.1%, ENABLE = 0x1	Noninverting, unity gain		9		µs

7.17 *OPA*

7.17.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CM}	Common mode voltage range	RRI = 0x0		-0.1		VDD-1.1	V
		RRI = 0x1		-0.1		VDD-0.3	
V_O	Voltage output swing from rail range	R_L = 10kΩ connected to VDD/2			20	68	mV
I_q	Quiescent current, per op-amp	I_O= 0mA, RRI = 0x0	GBW = 0x0		100		µA
			GBW = 0x1		350		
		I_O= 0mA, RRI = 0x1	GBW = 0x0		140	170	
			GBW = 0x1		450	600	
I_{BCS}	Burn-out current source current				2		µA
GBW	Gain-bandwidth product	C_L = 40 pF	GBW = 0x0		1.5		MHz
			GBW = 0x1		6		
V_{OS}	Input offset voltage	Noninverting, unity gain, VDD = 3.3V, T_A = 25°C	CHOP = 0x0		±0.4	±2	mV
			CHOP = 0x1 or 0x2			±0.3	
		Noninverting, unity gain, VDD = 3.3V	CHOP = 0x0		±1.5	±3.5	
			CHOP = 0x1 or 0x2		±0.1	±0.5	
dV_{OS}/dT	Input offset voltage temperature drift	Noninverting, unity gain, CHOP = 0x0	GBW = 0x0		±6		µV/°C
			GBW = 0x1		±5.2		
		Noninverting, unity gain, CHOP = 0x1 or 0x2			±0.5		
$PSRR_{DC}$	Power Supply Rejection Ratio, DC	Noninverting, unity gain	CHOP = 0x0		25	200	µV/V
			CHOP = 0x1 or 0x2		45	200	

7.17.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{bias}	Input bias current	$0.1V<V_{in}<VDD-0.3V$, VDD = 3.3V, CHOP=0x0	T_A = 25°C		±50		pA
			T_A = 125°C		±0.35	±100	nA
		$0.1V<V_{in}<VDD-0.3V$, VDD = 3.3V, CHOP=0x1	T_A = 25°C		±0.4		nA
			T_A = 125°C		±0.4	±104	nA
I_{bias}	Input bias current for dedicated OPA input pin (1)	$0.1V<V_{in}<VDD-0.3V$, VDD = 3.3V, CHOP=0x0	T_A = 25°C		±6		pA
			T_A = 125°C		±0.35	±0.4	nA
		$0.1V<V_{in}<VDD-0.3V$, VDD = 3.3V, CHOP=0x1	T_A = 25°C		±0.4		nA
			T_A = 125°C		±0.4	±0.5	nA
$CMRR_{DC}$	Common mode rejection ratio, DC	RRI = 0x0: $0V<V_{CM}<VDD-1.1V$ RRI = 0x1: $0V<V_{CM}<VDD-0.3V$	CHOP = 0x0		89		dB
			CHOP = 0x1 or 0x2	73	102		
e_n	Input voltage noise density	GBW = 0x0, Noninverting, unity gain, CHOP = 0x0	f = 1kHz		240		nV/√Hz
			f = 10kHz		88		
R_{in}	Input resistance (2)				2.6		kΩ
C_{in}	Input capacitance	Common mode			3		pF
A_{OL}	Open-loop voltage gain, DC	R_L = 20kΩ to GND, 0.3<Vo<VDD-0.3			93		dB
PM	phase margin	C_L = 40pF	GBW = 0x0		57		degree
			GBW = 0x1		78		
SR	Slew rate	Noninverting, unity gain, C_L = 40 pF	GBW = 0x0		1.3		V/µs
			GBW = 0x1		4.9		
THDN	Total harmonic distortion + noise	Noninverting, unity gain, GBW = 0x0, f = 1.5kHz, Integration BW = 100kHz			0.0034		%
		Noninverting, unity gain, GBW = 0x1, f = 6kHz, Integration BW = 100kHz			0.004		
I_{Load}	Short circuit current	GBW = 0x0, T_A = 25°C			±9		mA
		GBW = 0x1, T_A = 25°C			±30		
C_{Load}	Output load capacitance					40	pF

(1) MSPM0L134x devices only
(2) R_{in} here means the input resistance of mux in OPA.

7.17.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{EN}	OPA enable time	ENABLE = 0x0 to 0x1, Bandgap reference ON, 0.1%, Noninverting, unity gain	GBW = 0x0		7.3	12	µs
			GBW = 0x1		4.4	6	
$t_{disable}$	OPA disable time				4		ULPCLK cycles
f_{CHOP}	OPA Chopping Frequency	CHOP = 0x1 or 0x2	GAIN = 0x0		125		kHz
			GAIN = 0x1		62.5		
			GAIN = 0x2		31.25		
			GAIN = 0x3		15.625		
			GAIN = 0x4		7.8		
			GAIN = 0x5		3.9		

7.17.2 Switching Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{SETTLE}	OPA settling time	C_L = 40 pF, Vstep = 0.3V to VDD-0.3V, 0.1%, ENABLE = 0x1, Noninverting, unity gain	GBW = 0x0		2.5	9	µs
			GBW = 0x1		1.3	5	

7.17.3 PGA Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
G	Non- inverting gain accuracy	GAIN = 0x0	Gain of 1	–0.09		+0.09	%
		GAIN = 0x1	Gain of 2	-0.33		+0.33	
		GAIN = 0x2	Gain of 4	–0.6		+0.6	
		GAIN = 0x3	Gain of 8	–1.1		+1	
		GAIN = 0x4	Gain of 16	–1.9		1.5	
		GAIN = 0x5	Gain of 32	–3.5		+1.7	
	Inverting gain accuracy	GAIN = 0x1	Gain of -1	–0.4		+0.6	
		GAIN = 0x2	Gain of -3	–0.8		+0.8	
		GAIN = 0x3	Gain of -7	–1		1.3	
		GAIN = 0x4	Gain of -15	–1.1		1.7	
		GAIN = 0x5	Gain of -31	–2.2		2.6	
R_{PGA}	Programmable gain stage resistance	GAIN = 0x1	R1		64		kΩ
			R2 (feedback resistor)		64		
		GAIN = 0x2	R1		32		
			R2 (feedback resistor)		96		
		GAIN = 0x3	R1		16		
			R2 (feedback resistor)		112		
		GAIN = 0x4	R1		8		
			R2 (feedback resistor)		120		
		GAIN = 0x5	R1		4		
			R2 (feedback resistor)		124		
G/dV	Gain supply drift				0.026	0.84	%/V
G/dT	Gain temperature drift				0.0007	0.014	%/C
THD	Total harmonic distortion	f = 3kHz, R_L = 1.5kOhm to VDD/2, GBW = 0x1, GAIN = 0x1			88		dB
		f = 188Hz, R_L = 1.5kOhm to VDD/2, GBW = 0x1, GAIN = 0x5			61		

7.18 I2C

7.18.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain0	2	32	8	32	20	32	MHz
f_{SCL}	SCL clock frequency			0.1		0.4		1	MHz
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	Low period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us

7.18.1 I2C Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{HD,DAT}$	Data hold time		0		0		0		ns
$t_{SU,DAT}$	Data setup time		250		100		50		ns
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	Bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	Data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	Data valid acknowledge time			3.45		0.9		0.45	us

7.18.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.18.3 I²C Timing Diagram

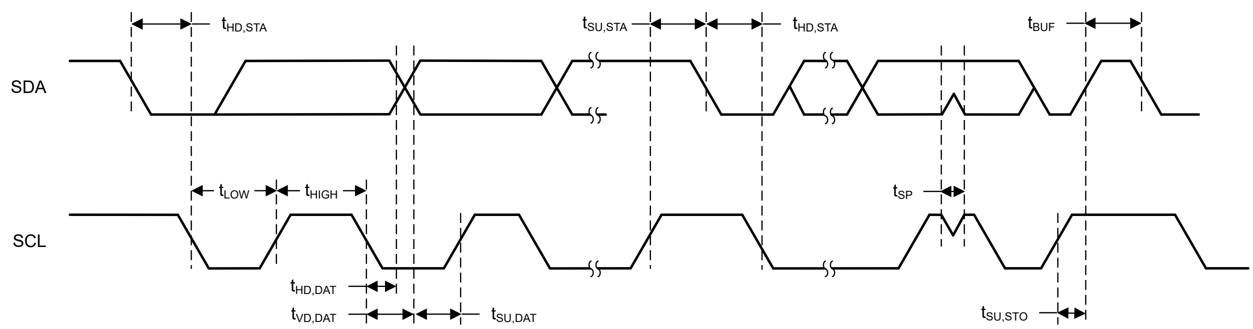


Figure 7-5. I2C Timing Diagram

7.19 SPI

7.19.1 SPI

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
f_{SPI}	SPI clock frequency	Clock max speed = 32MHz 1.71 < VDD < 3.6V Controller mode			16	MHz
f_{SPI}	SPI clock frequency	Clock max speed = 32MHz 1.71 < VDD < 3.6V Peripheral mode			16	MHz
DC_{SCK}	SCK Duty Cycle		40	50	60	%
Controller						
$t_{SCLK\_H/L}$	SCLK High or Low time		(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns

7.19.1 SPI (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, delayed sampling enabled	1			ns
		1.71 < VDD < 2.7V, delayed sampling enabled	1			
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, no delayed sampling	27			ns
		1.71 < VDD < 2.7V, no delayed sampling	35			
$t_{HD.CI}$	POCI input data hold time		9			ns
$t_{VALID.CO}$	PICO output data valid time (2)				10	ns
$t_{HD.CO}$	PICO output data hold time (3)		1			ns
Peripheral						
$t_{CS.LEAD}$	CS lead-time, CS active to clock		8			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out				23	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high inpedance				19	ns
$t_{SU.PI}$	PICO input data setup time		7			ns
$t_{HD.PI}$	PICO input data hold time		31.25			ns
$t_{VALID.PO}$	POCI output data valid time(2)	2.7 < VDD < 3.6V			24	ns
$t_{VALID.PO}$	POCI output data valid time(2)	1.71 < VDD < 2.7V			31	ns
$t_{HD.PO}$	POCI output data hold time(3)		5			ns

(1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.19.2 SPI Timing Diagram

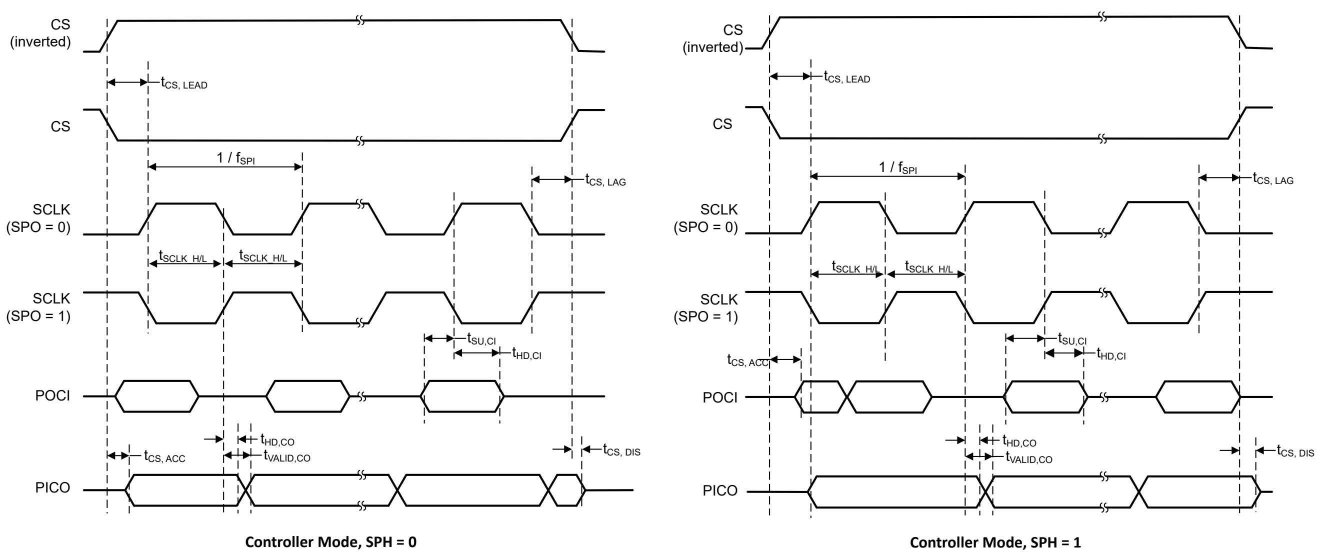


Figure 7-6. SPI timing diagram - Controller Mode

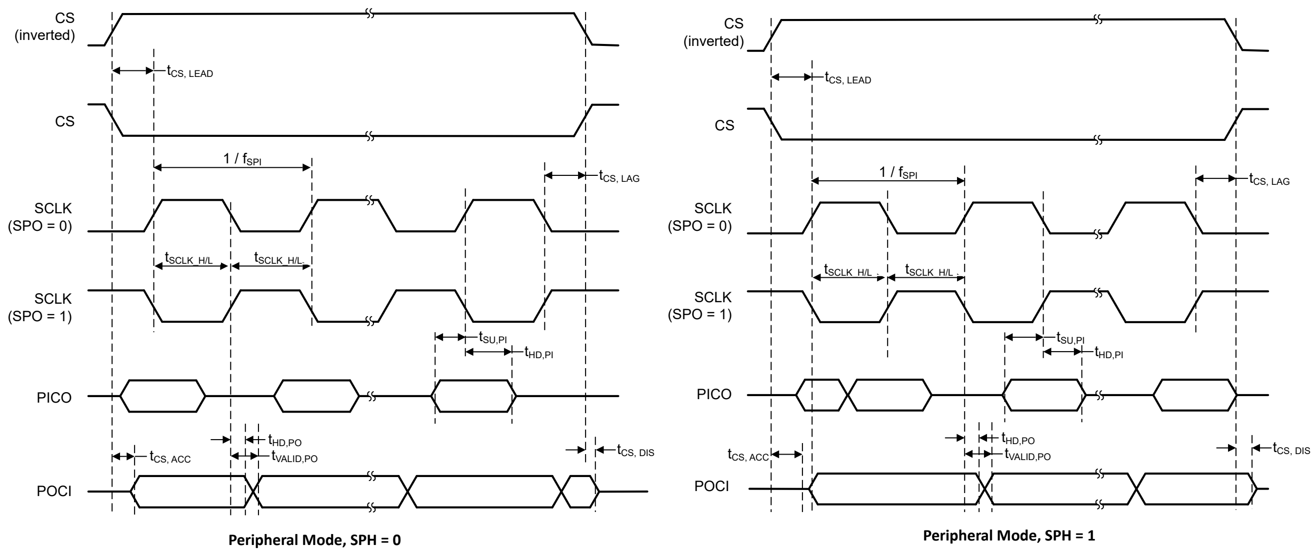


Figure 7-7. SPI timing diagram - Peripheral Mode

7.20 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency				32	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)				4	MHz
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.21 TIMx

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{res}	Timer resolution time	$f_{TIMxCLK}$ = 32MHz	31.25			ns
			1			$t_{TIMxCLK}$
t_{res}	Timer resolution time	TIMx with 16bit counter			16	bit
$t_{COUNTER}$	16-bit counter clock period	$f_{TIMxCLK}$ = 32MHz	0.03125		2048	us
			1		65536	$t_{TIMxCLK}$

7.22 Emulation and Debug

7.22.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SWD}	SWD frequency				10	MHz

8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.1 CPU

The CPU subsystem (MCPUSS) implements an Arm Cortex-M0+ CPU, an instruction prefetch and cache, a system timer, and interrupt management features. The Arm Cortex-M0+ is a cost-optimized 32-bit CPU that delivers high performance and low power to embedded applications. Key features of the CPU Sub System include:

- Arm Cortex-M0+ CPU supports clock frequencies from 32 kHz to 32 MHz
  - ARMv6-M Thumb instruction set (little endian) with single-cycle 32×32 multiply instruction
  - Single-cycle access to GPIO registers through Arm single-cycle IO port
- Prefetch logic to improve sequential code execution, and I-cache with 2 64-bit cache lines
- System timer (SysTick) with 24-bit down counter and automatic reload
- Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail chaining
- Interrupt groups for expanding the total interrupt sources, with jump index for low interrupt latency

8.2 Operating Modes

MSPM0L MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD, or a logic level match on certain IOs. RUN, SLEEP, STOP, and STANDBY modes also include several configurable policy options (for example, RUN.x) for balancing performance with power consumption.

To further balance performance and power consumption, MSPM0L devices implement two power domains: PD1 (for the CPU, memories, and high performance peripherals), and PD0 (for low speed, low power peripherals). PD1 is always powered in RUN and SLEEP modes, but is disabled in all other modes. PD0 is always powered in RUN, SLEEP, STOP, and STANDBY modes. PD1 and PD0 are both disabled in SHUTDOWN mode.

8.2.1 Functionality by Operating Mode

Supported functionality in each operating mode is given in Table 8-1.

Functional key:

- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode, but its use is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained.

Table 8-1. Supported Functionality by Operating Mode

Operating Mode		RUN			SLEEP			STOP			STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1	
Oscillators	SYSOSC	EN	EN	DIS	EN	EN	DIS	OPT(1)	EN	DIS	DIS	DIS	OFF
	LFOSC	EN											OFF

Table 8-1. Supported Functionality by Operating Mode (continued)

<table>
<tr><th colspan="2" rowspan="2">Operating Mode</th><th colspan="3">RUN</th><th colspan="3">SLEEP</th><th colspan="3">STOP</th><th colspan="2">STANDBY</th><th rowspan="2">SHUTDOWN</th></tr>
<tr><th>RUN0</th><th>RUN1</th><th>RUN2</th><th>SLEEP0</th><th>SLEEP1</th><th>SLEEP2</th><th>STOP0</th><th>STOP1</th><th>STOP2</th><th>STANDBY0</th><th>STANDBY1</th></tr>
<tr><td rowspan="8">Clocks</td><td>CPUCLK</td><td>32M</td><td>32k</td><td>32k</td><td colspan="8">DIS</td><td>OFF</td></tr>
<tr><td>MCLK to PD1</td><td>32M</td><td>32k</td><td>32k</td><td>32M</td><td>32k</td><td>32k</td><td colspan="5">DIS</td><td>OFF</td></tr>
<tr><td>ULPCLK to PD0</td><td>32M</td><td>32k</td><td>32k</td><td>32M</td><td>32k</td><td>32k</td><td>4M(1)</td><td>4M</td><td colspan="2">32k</td><td>DIS</td><td>OFF</td></tr>
<tr><td>ULPCLK to TIMG0/1</td><td>32M</td><td>32k</td><td>32k</td><td>32M</td><td>32k</td><td>32k</td><td>4M(1)</td><td>4M</td><td colspan="3">32k</td><td>OFF</td></tr>
<tr><td>MFCLK</td><td>OPT</td><td colspan="2">DIS</td><td>OPT</td><td colspan="2">DIS</td><td colspan="2">OPT</td><td colspan="3">DIS</td><td>OFF</td></tr>
<tr><td>LFCLK</td><td colspan="10">32k</td><td>DIS</td><td>OFF</td></tr>
<tr><td>LFCLK to TIMG0/1</td><td colspan="11">32k</td><td>OFF</td></tr>
<tr><td>MCLK Monitor</td><td colspan="10">OPT</td><td>DIS</td><td>OFF</td></tr>
<tr><td rowspan="3">PMU</td><td>POR Monitor</td><td colspan="12">EN</td></tr>
<tr><td>BOR Monitor</td><td colspan="11">EN</td><td>OFF</td></tr>
<tr><td>Core Regulator</td><td colspan="6">FULL DRIVE</td><td colspan="3">REDUCED DRIVE</td><td colspan="2">LOW DRIVE</td><td>OFF</td></tr>
<tr><td rowspan="4">Core Functions</td><td>CPU</td><td colspan="3">EN</td><td colspan="8">DIS</td><td>OFF</td></tr>
<tr><td>DMA</td><td colspan="6">OPT</td><td colspan="5">NS (triggers supported)</td><td>OFF</td></tr>
<tr><td>Flash</td><td colspan="6">EN</td><td colspan="5">DIS</td><td>OFF</td></tr>
<tr><td>SRAM</td><td colspan="6">EN</td><td colspan="5">DIS</td><td>OFF</td></tr>
<tr><td rowspan="2">PD1 Peripherals</td><td>SPI0</td><td colspan="6">OPT</td><td colspan="5">DIS</td><td>OFF</td></tr>
<tr><td>CRC</td><td colspan="6">OPT</td><td colspan="5">DIS</td><td>OFF</td></tr>
<tr><td rowspan="6">PD0 Peripherals</td><td>TIMG0/1</td><td colspan="11">OPT</td><td>OFF</td></tr>
<tr><td>TIMG2/4</td><td colspan="10">OPT</td><td>OPT(2)</td><td>OFF</td></tr>
<tr><td>UART0/1</td><td colspan="10">OPT</td><td>OPT(2)</td><td>OFF</td></tr>
<tr><td>I2C0/1</td><td colspan="10">OPT</td><td>OPT(2)</td><td>OFF</td></tr>
<tr><td>GPIOA</td><td colspan="10">OPT</td><td>OPT(2)</td><td>OFF</td></tr>
<tr><td>WWDT0</td><td colspan="10">OPT</td><td>DIS</td><td>OFF</td></tr>
<tr><td rowspan="4">Analog</td><td>ADC0</td><td colspan="8">OPT</td><td colspan="3">NS (triggers supported)</td><td>OFF</td></tr>
<tr><td>OPA0/1</td><td>OPT</td><td colspan="2">NS</td><td>OPT</td><td colspan="2">NS</td><td colspan="2">OPT</td><td colspan="3">NS</td><td>OFF</td></tr>
<tr><td>GPAMP</td><td colspan="8">OPT</td><td colspan="3">NS</td><td>OFF</td></tr>
<tr><td>COMP0</td><td>OPT</td><td colspan="2">OPT (ULP)</td><td>OPT</td><td colspan="2">OPT (ULP)</td><td colspan="2">OPT</td><td colspan="3">OPT (ULP)</td><td>OFF</td></tr>
<tr><td colspan="2">IOMUX and IO Wakeup</td><td colspan="11">EN</td><td>DIS w/ WAKE</td></tr>
<tr><td colspan="2">Wake Sources</td><td colspan="3">N/A</td><td colspan="3">ANY IRQ</td><td colspan="5">PD0 IRQ</td><td>IOMUX, NRST, SWD</td></tr>
</table>

(1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as in RUN1 and ULPCLK remains at 32 kHz as in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as in RUN2 and ULPCLK remains at 32 kHz as in RUN2.

(2) When using the STANDBY1 policy for STANDBY, only TIMG0 and TIMG1 are clocked. Other PD0 peripherals can generate an asynchronous fast clock request upon external activity but are not actively clocked.

8.3 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brown-out reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY operating modes to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.4 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32 kHz)
- **SYSOSC**: Internal high-frequency oscillator (4 MHz or 32 MHz with factory trim, 16 MHz or 24 MHz with user trim)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals, derived from SYSOSC or LFCLK, active in RUN and SLEEP modes
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4-MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- **LFCLK**: 32-kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **ADCCLK**: ADC clock, available in RUN, SLEEP and STOP modes
- **CLK_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes

For more details, see the CKM chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.5 DMA

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA in these devices support the following key features:

- 3 independent DMA transfer channels
  - 1 full-feature channel (DMA0), supporting repeated transfer modes
  - 2 basic channels (DMA1, DMA2), supporting single transfer modes
- Configurable DMA channel priorities
- Byte (8-bit), short word (16-bit), word (32-bit) and long word (64-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon competion of activity on another channel
- Stride mode to support data re-organization

Table 8-2 lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

Table 8-2. DMA Trigger Mapping

TRIGGER 0:6	SOURCE	TRIGGER 7:13	SOURCE
0	Software	7	I2C1 Publisher 2

Table 8-2. DMA Trigger Mapping (continued)

TRIGGER 0:6	SOURCE	TRIGGER 7:13	SOURCE
1	Generic Subscriber 0 (FSUB_0)	8	SPI0 Publisher 1
2	Generic Subscriber 1 (FSUB_1)	9	SPI0 Publisher 2
3	ADC0 Publisher 2	10	UART0 Publisher 1
4	I2C0 Publisher 1	11	UART0 Publisher 2
5	I2C0 Publisher 2	12	UART1 Publisher 1
6	I2C1 Publisher 1	13	UART1 Publisher 2

8.6 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) that are interconnected through an event fabric containing a combination of static and programmable routes.

Events that are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
  - Example: GPIO interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
  - Example: UART data receive trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)
  - Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

For more details, see the Event chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

Table 8-3. Generic Event Channels

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish the event to another entity (or entities, in the case of a splitter route). An entity can be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
0	No generic event channel selected	N/A
1	Generic event channel 1 selected	1 : 1
2	Generic event channel 2 selected	1 : 1
3	Generic event channel 3 selected	1 : 2 (splitter)

8.7 Memory

8.7.1 Memory Organization

Table 8-4 summarizes the memory map of the devices. For more information about the memory region detail, see the *Platform Memory Map* chapter in the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

Table 8-4. Memory Organization

Memory Region	Subregion	MSPM0L1304, MSPM0L1344	MSPM0L1305, MSPM0L1345	MSPM0L1306, MSPM0L1346
Code (Flash)	MAIN (3)	16KB - 8B 0x0000.0000 to 0x0000.3FF8	32KB - 8B(1) 0x0000.0000 to 0x0000.7FF8	64KB - 8B(1) 0x0000.0000 to 0x0000.FFF8
	Aliased MAIN (2) (3)	0x0040.0000 to 0x0040.3FF8	0x0040.0000 to 0x0040.7FF8	0x0040.0000 to 0x0040.FFF8

Table 8-4. Memory Organization (continued)

Memory Region	Subregion	MSPM0L1304, MSPM0L1344	MSPM0L1305, MSPM0L1345	MSPM0L1306, MSPM0L1346
SRAM (SRAM)	SRAM	2KB 0x2000.0000 to 0x2000.0800	4KB 0x2000.0000 to 0x2000.1000	4KB 0x2000.0000 to 0x2000.1000
	Aliased SRAM(2)	0x2000.0000 to 0x2000.0800	0x2000.0000 to 0x2000.1000	0x2000.0000 to 0x2000.1000
Peripheral	Peripherals	0x4000.0000 to 0x40FF.FFFF	0x4000.0000 to 0x40FF.FFFF	0x4000.0000 to 0x40FF.FFFF
	MAIN (3)	0x0000.0000 to 0x0000.3FF8	0x0000.0000 to 0x0000.7FF8	0x0000.0000 to 0x0000.FFF8
	Aliased MAIN(2) (3)	0x0040.0000 to 0x0040.3FF8	0x0040.0000 to 0x0040.7FF8	0x0040.0000 to 0x0040.FFF8
	NONMAIN	512 bytes 0x41C0.0000 to 0x41C0.0200	512 bytes 0x41C0.0000 to 0x41C0.0200	512 bytes 0x41C0.0000 to 0x41C0.0200
	Aliased NONMAIN (2)	0x41C1.0000 to 0x41C1.0200	0x41C1.0000 to 0x41C1.0200	0x41C1.0000 to 0x41C1.0200
	FACTORY	0x41C4.0000 to 0x41C4.0080	0x41C4.0000 to 0x41C4.0080	0x41C4.0000 to 0x41C4.0080
	Aliased FACTORY (2)	0x41C5.0000 to 0x41C5.0080	0x41C5.0000 to 0x41C5.0080	0x41C5.0000 to 0x41C5.0080
Subsystem		0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFFF
System PPB		0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF

(1) First 32KB flash memory (address 0x0000.0000 to 0x0000.8000) has up to 100000 program and erase cycles.
(2) Aliased memory reads the same as the corresponding memory region. Aliased memory is included to keep the compatibility with devices that have ECC.
(3) CPU access to one of the last 8 bytes of a flash region will cause a hard fault. This occurs because the prefetch logic tries to read one flash word (64 bits) ahead, resulting in a read attempt to an invalid memory location.

8.7.2 Peripheral File Map

Table 8-5 lists the available peripherals and the register base address for each.

Table 8-5. Peripherals Summary

Peripheral Name	Base Address	Size
ADC0	0x40004000	0x2000
COMP0	0x40008000	0x2000
OPA0	0x40020000	0x2000
OPA1	0x40022000	0x2000
VREF	0x40030000	0x2000
WWDT0	0x40080000	0x2000
TIMG0	0x40084000	0x2000
TIMG1	0x40086000	0x2000
TIMG2	0x40088000	0x2000
TIMG4	0x4008C000	0x2000
GPIO0	0x400A0000	0x2000
SYSCTL	0x400AF000	0x3000
DEBUGSS	0x400C7000	0x2000
EVENT	0x400C9000	0x3000
NVMNW	0x400CD000	0x2000

Table 8-5. Peripherals Summary (continued)

Peripheral Name	Base Address	Size
I2C0	0x400F0000	0x2000
I2C1	0x400F2000	0x2000
UART1	0x40100000	0x2000
UART0	0x40108000	0x2000
MCPUSS	0x40400000	0x2000
WUC	0x40424000	0x1000
IOMUX	0x40428000	0x2000
DMA	0x4042A000	0x2000
CRC	0x40440000	0x2000
SPI0	0x40468000	0x2000
ADC0 (1)	0x4055A000	0x1000

(1) Aliased region of ADC0 memory-mapped registers.

8.7.3 Peripheral Interrupt Vector

Table 8-6 shows the IRQ number and the interrupt group number for each peripherals in this device.

Table 8-6. Interrupt Vector Number

Peripheral Name	NVIC IRQ	Group IIDX
WWDT0	0	0
DEBUGSS	0	2
NVMNW	0	3
EVENT SUB PORT0	0	4
EVENT SUB PORT1	0	5
SYSCTL	0	6
GPIO0	1	0
COMP0	1	2
TIMG1	2	–
ADC	4	–
SPI0	9	–
UART1	13	–
UART0	15	–
TIMG0	16	–
TIMG2	18	–
TIMG4	20	–
I2C0	24	–
I2C1	25	–
DMA	31	–

8.8 Flash Memory

A single bank of nonvolatile flash memory is provided for storing executable program code and application data.

Key features of the flash include:

- In-circuit program and erase operations supported across the entire recommended supply range
- Small 1KB sector sizes (minimum erase resolution of 1KB)

- Up to 100000 program and erase cycles on the lower 32KB of the flash memory, with up to 10000 program and erase cycles on the remaining flash memory (devices with 32KB or less support 100000 cycles on the entire flash memory)

For a complete description of the flash memory, see the NVM chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.9 SRAM

MSPM0Lxx MCUs include a low-power high-performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code. The SRAM memory content is fully retained in run, sleep, stop, and standby operating modes and is lost in shutdown mode. A write protection mechanism is provided to allow the application to prevent unintended modifications to a portion of the SRAM memory. SRAM write protection is useful when placing executable code into SRAM to provide a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption.

8.10 GPIO

The general purpose input/output (GPIO) peripheral lets the application write data out and read data in through the device pins. Through the use of the Port A GPIO peripheral, these devices support up to 28 GPIO pins.

The key features of the GPIO module include:

- 0 wait state MMR access from CPU
- Set, clear, or toggle multiple bits without the need of a read-modify-write construct in software
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port
- User controlled input filtering

8.11 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO pad configuration registers allow for programmable drive strength, speed, pullup or pulldown, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.12 ADC

The 12-bit analog-to-digital converter (ADC) module in these devices support fast 12-bit conversions with single-ended inputs.

ADC features include:

- 12-bit output resolution at up to 1.68 Msps with greater than 11-bit ENOB
- Up to 10 external input channels
- Internal channels for temperature sensing, supply monitoring, and analog signal chain (interconnection with OPA, GPAMP, and others)
- Software selectable reference:
  - Configurable internal dedicated ADC reference voltage of 1.4 V and 2.5 V (VREF)
  - MCU supply voltage (VDD)
  - External reference supplied to the ADC through the VREF+ and VREF- pins
- Operates in RUN, SLEEP, and STOP modes and supports triggers from STANDBY mode

Table 8-7. ADC0 Channel Mapping

CHANNEL[0:7]	SIGNAL NAME	CHANNEL[8:15]	SIGNAL NAME (1) (2)
0	A0	8	A8

Table 8-7. ADC0 Channel Mapping (continued)

CHANNEL[0:7]	SIGNAL NAME	CHANNEL[8:15]	SIGNAL NAME (1) (2)
1	A1	9	A9
2	A2	10	–
3	A3	11	*Temperature Sensor*
4	A4	12	*OPA0 output*
5	A5	13	*OPA1 output*
6	A6	14	*GPAMP output*
7	A7	15	*Supply/Battery Monitor*

(1) *Italicized* signal names are internal to the SoC. These signals are used for internal peripheral interconnections.
(2) For more information about device analog connections see Section 8.24.

For more details, see the ADC chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.13 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with the 1.4-V internal VREF at the factory trim temperature (TS_{TRIM}). This calibration value can be used with the temperature sensor temperature coefficient (TS_c) to estimate the device temperature. See the temperature sensor section of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual* for guidance on estimating the device temperature with the factory trim value.

8.14 VREF

The voltage reference module (VREF) in these devices contains a configurable voltage reference buffer dedicated for the on-board ADC. The devices also support connection of an external reference for applications in which higher accuracy is required.

VREF features include:

- 1.4-V and 2.5-V user-selectable internal reference for ADC
- Internal reference supports ADC operation up to 200 ksps
- Support for bringing in an external reference for the ADC as well as for other analog peripherals on the VREF+ and VREF- device pins (24, 28, and 32-pin packages only)

For more details, see the VREF chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.15 COMP

The comparator peripheral in the device compares the voltage levels on two inputs terminals and provides a digital output based on this comparison. The COMP supports the following key features:

- Programmable hysteresis
- Programmable reference voltage:
  - Integrated 8-bit reference DAC, the output can also can connect to OPA input terminal internally as an output buffer.
- Configurable operation modes:
  - High-speed mode (40-ns propagation delay)
  - Low-power mode (1.5-µA power consumption)
- Programmable output glitch filter delay

- Support output wake up device from all low-power modes
- Output connected to advanced timer fault handling mechanism
- The IPSEL and IMSEL bits in comparator registers can be used to select the comparator channel inputs from device pins or from internal analog modules.

Table 8-8. COMP0 Input Channel Selection(1)

IPSEL / IMSEL Bits	Positive Terminal Input	Negative Terminal Input
0x0	COMP0_IN0+	COMP0_IN0-
0x1	COMP0_IN1+	COMP0_IN1-
0x6	OPA1 output	OPA0 output

(1) For more information about device analog connections, see Section 8.24.

For more details, see the COMP chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.16 CRC

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for 32-bit CRC based on CRC32-ISO3309
- Support for bit reversal

For more details, see the CRC chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.17 GPAMP

The general-purpose amplifier (GPAMP) peripheral is a chopper-stabilized general-purpose operational amplifier with rail-to-rail input and output.

The GPAMP supports the following features:

- Software selectable chopper stabilization
- Rail-to-rail input and output
- Programmable internal unity gain feedback loop

For more details, see the ADC chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.18 OPA

The zero-drift op amps (OPAs) in these devices, OPA0 and OPA1, are chopper stabilized operational amplifiers with rail-to-rail input/output and a programmable gain stage feedback loop.

The OPA peripherals support the following key features:

- Software-selectable zero-drift chopper stabilization for improved accuracy and drift performance
- MSPM0L134x devices feature dedicated OPA inverting input pins for ultra-low I_b performance
- Factory trimming to remove offset error
- Burnout current source (BCS) integrated to monitor sensor health
- Programmable gain amplifier (PGA) up to 32x

The OPA features configurable input muxes P-MUX, N-MUX, and M-MUX to support various analog signal chain amplifier configurations that include general purpose, inverting, noninverting, unity gain, cascade, noninverting cascade, difference, and more. The following tables list the input channel mapping for each OPA.

For more information about device analog connections, see Section 8.24

For more details, see the OPA chapter of the *MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual*.

8.19 I2C

The inter-integrated circuit interface (I^2C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100 kbit/s
- Support Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Support Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
- Separated transmit and receive FIFOs support DMA data transfer
- Support SMBus 3.0 with PEC, ARP, timeout detection and host support
- Wakeup from low power mode on address match
- Support analog and digital glitch filter for input signal glitch suppression
- 8-entry transmit and receive FIFOs

For more details, see the I2C chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.20 SPI

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support ULPCLK/2 bit rate and up to 16Mbits/s in both controller and peripheral mode
- Configurable as a controller or a peripheral
- Configurable chip select for both controller and peripheral
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode)[3]
- Programmable data frame size from 7 bits to 16 bits (peripheral mode)(2)
- Transmit and receive FIFOs (4 entries each with 16 bits per entry) supporting DMA data transfer
- Supports TI mode, Motorola mode and National Microwire format

For more details, see the SPI chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.21 UART

The UART peripherals provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
  - 5, 6, 7 or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - Line-break detection
  - Glitch filter on the input signals
  - Programmable baud rate generation with oversampling by 16, 8 or 3
  - Local Interconnect Network (LIN) mode support
- Separated transmit and receive FIFOs support DAM data transfer
- Support transmit and receive loopback mode operation
- See Table 8-9 for detail information on supported protocols

Table 8-9. UART Features

UART Features	UART0 (Extend)	UART1 (Main)
Active in Stop and Standby Mode	Yes	Yes
Separate transmit and receive FIFOs	Yes	Yes
Support hardware flow control	Yes	Yes

[3] MSPM0L does not support PACKEN feature that allows the packing of 2 16-bit FIFO entries into a 32-bit value.

Table 8-9. UART Features (continued)

UART Features	UART0 (Extend)	UART1 (Main)
Support 9-bit configuration	Yes	Yes
Support LIN mode	Yes	-
Support DALI	Yes	-
Support IrDA	Yes	-
Support ISO7816 Smart Card	Yes	-
Support Manchester coding	Yes	-
FIFO Depth	4 entries	4 entries

For more details, see the UART chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.22 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.23 Timers (TIMx)

The timer peripherals in these devices support the following key features. For specific configuration, see Table 8-10.

Specific features for the **general-purpose timer (TIMGx)** include:

- 16-bit down, up/down, or up counter with repeat-reload mode
- 32-bit down, up/down, or up counter with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Support quadrature encoder interface (QEI) for positioning and movement sensing
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt/DMA trigger generation and cross peripherals (such as ADC) trigger capability
- Cross-trigger event logic for Hall sensor inputs

Table 8-10. Different TIMG Configurations

TIM Name	Power Domain	Resolution	Prescaler	Capture/ Compare Channels	External PWM Channels	Phase Load	Shadow Load	Shadow CC
TIMG0	PD0	16-bit	8-bit	2	2	-	-	-
TIMG1	PD0	16-bit	8-bit	2	2	-	-	-

Table 8-10. Different TIMG Configurations (continued)

TIM Name	Power Domain	Resolution	Prescaler	Capture/ Compare Channels	External PWM Channels	Phase Load	Shadow Load	Shadow CC
TIMG2	PD0	16-bit	8-bit	2	2	-	-	-
TIMG4	PD0	16-bit	8-bit	2	2	-	Yes	Yes

For more details, see the timer chapters of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

8.24 Device Analog Connections

Figure 8-1 shows the internal analog connection of the device.

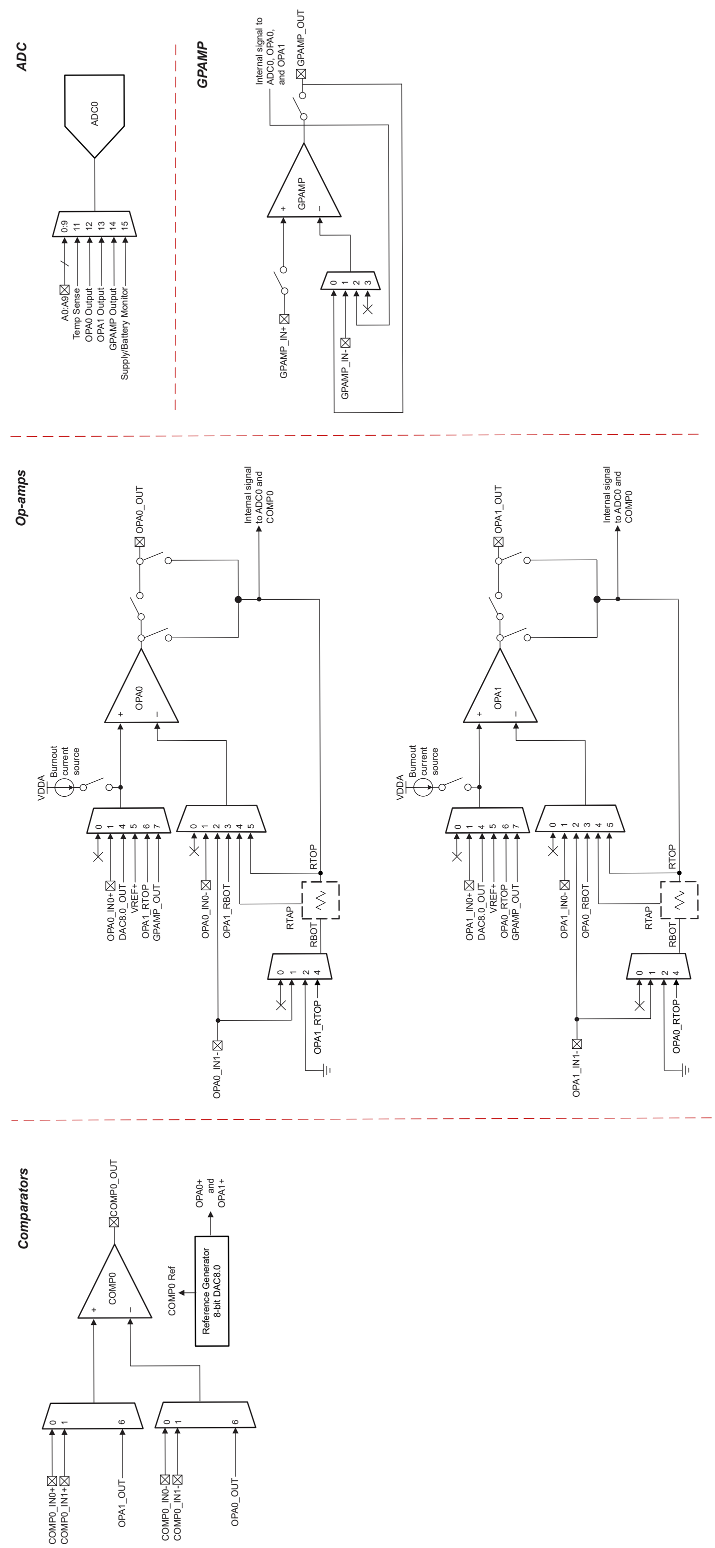


Figure 8-1. Analog Connections

8.25 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO and provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For more information, see the IOMUX section of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 8-2. Not all pins have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the device-specific data sheet for detailed information on what features are supported for a specific pin.

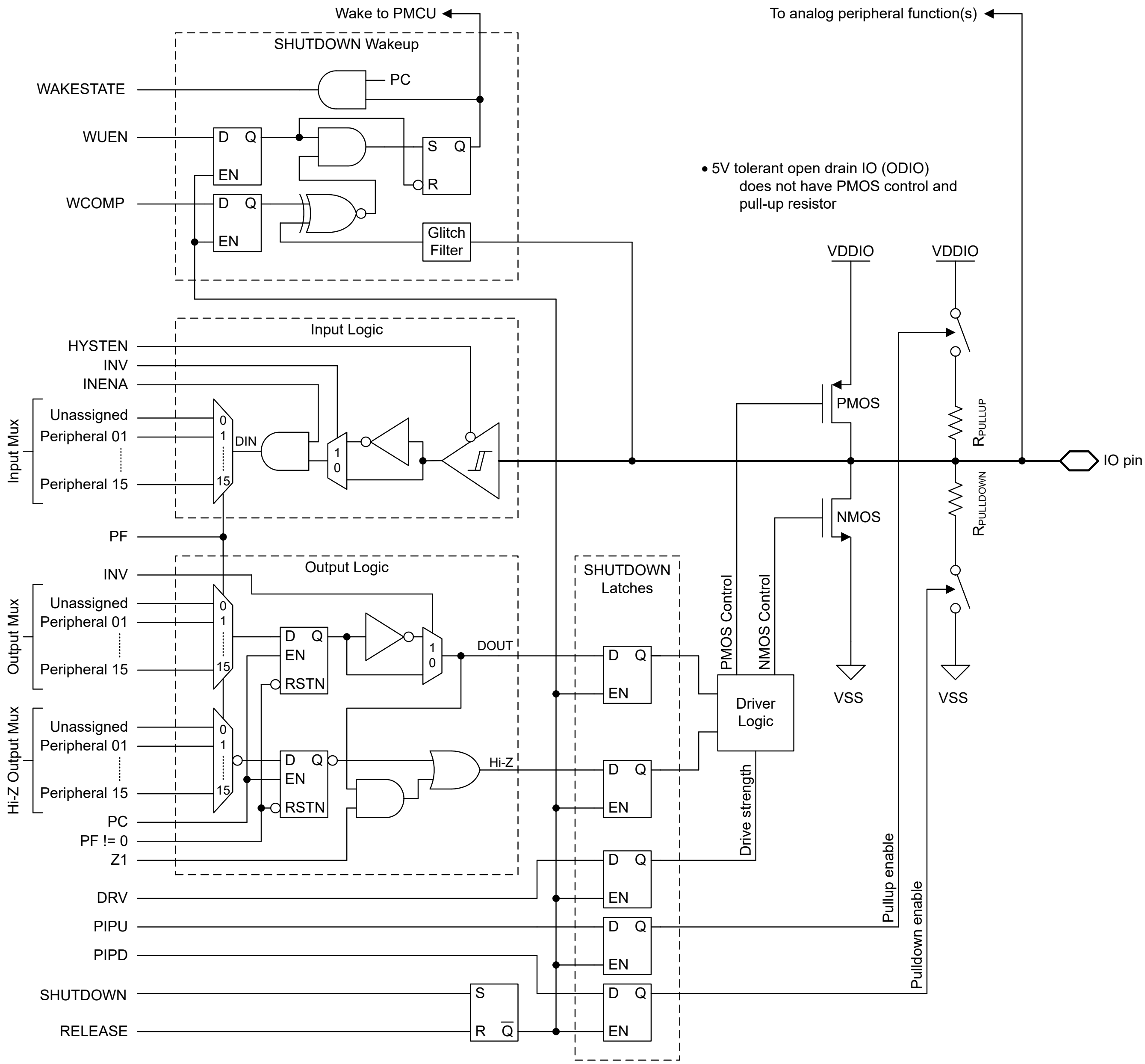


Figure 8-2. Superset Input/Output Diagram

8.26 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device. For a complete description of the debug functionality offered on MSPM0 devices, see the debug chapter of the technical reference manual.

Table 8-11. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

8.27 Bootstrap Loader (BSL)

The bootstrap loader (BSL) enables configuration of the device as well as programming of the device memory through a UART or I2C serial interface. Access to the device memory and configuration through the BSL is protected by a 256-bit user-defined password, and it is possible to completely disable the BSL in the device configuration, if desired. The BSL is enabled by default from TI to support use of the BSL for production programming.

A minimum of two pins are required to use the BSL: the BSLRX and BSLTX signals (for UART), or the BSLSCL and BSLSDA signals (for I^2C). Additionally, one or two additional pins (BSL_invoke and NRST) may be used for controlled invocation of the bootloader by an external host.

If enabled, the BSL may be invoked (started) in the following ways:

- The BSL is invoked during the boot process if the BSL_invoke pin state matches the defined BSL_invoke logic level. If the device fast boot mode is enabled, this invocation check is skipped. An external host can force the device into the BSL by asserting the invoke condition and applying a reset pulse to the NRST pin to trigger a BOOTRST, after which the device will verify the invoke condition during the reboot process and start the BSL if the invoke condition matches the expected logic level.
- The BSL is automatically invoked during the boot process if the reset vector and stack pointer are left unprogrammed. As a result, a blank device from TI will invoke the BSL during the boot process without any need to provide a hardware invoke condition on the BSL_invoke pin. This enables production programming using just the serial interface signals.
- The BSL may be invoked at runtime from application software by issuing a SYSRST with BSL entry command.

Table 8-12. BSL Pin Requirements and Functions

DEVICE SIGNAL	CONNECTION	BSL FUNCTION
BSLRX	Required for UART	UART receive signal (RXD), an input
BSLTX	Required for UART	UART transmit signal (TXD) an output
BSLSCL	Required for I2C	I^2C BSL clock signal (SCL)
BSLSDA	Required for I2C	I^2C BSL data signal (SDA)
BSL_invoke	Optional	Active-high digital input used to start the BSL during boot
NRST	Optional	Active-low reset pin used to trigger a reset and subsequent check of the invoke signal (BSL_invoke)

8.28 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Refer to the *Factory Constants* chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

Table 8-13. DEVICEID

DEVICEID address is 0x41C4.0004, VERSION is bit 28 to 31, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

DEVICE	DEVICEID.VERSION	DEVICEID.PARTNUM	DEVICEID.MANUFACTURER
MSPM0L1304, MSPM0L1344	Monotonic increasing value indicating hardware revision	0xBB82	0x17
MSPM0L1305, MSPM0L1345		0xBB82	0x17
MSPM0L1306, MSPM0L1346		0xBB82	0x17

Table 8-14. USERID

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

DEVICE	PART	VARIANT	DEVICE	PART	VARIANT
MSPM0L1306SRHBR	0xBB70	0x3C	MSPM0L1305SRHBR	0x4D03	0x2D
MSPM0L1306TRHBR	0xBB70	0x52	MSPM0L1305TRHBR	0x4D03	0x85
MSPM0L1306QRHBR	0xBB70	0xC2	MSPM0L1305QRHBR	0x4D03	0x78
MSPM0L1306SDGS28R	0xBB70	0x5	MSPM0L1305SDGS28R	0x4D03	0x64
MSPM0L1306TDGS28R	0xBB70	0x63	MSPM0L1305TDGS28R	0x4D03	0xFB
MSPM0L1306QDGS28R	0xBB70	0xF7	MSPM0L1305QDGS28R	0x4D03	0x74
MSPM0L1306SRGER	0xBB70	0x7F	MSPM0L1305SRGER	0x4D03	0x73
MSPM0L1306TRGER	0xBB70	0xAA	MSPM0L1305TRGER	0x4D03	0xEA
MSPM0L1306SDGS20R	0xBB70	0xF4	MSPM0L1305SDGS20R	0x4D03	0xC7
MSPM0L1306TDGS20R	0xBB70	0xA	MSPM0L1305TDGS20R	0x4D03	0xA0
MSPM0L1306QDGS20R	0xBB70	0x59	MSPM0L1305QDGS20R	0x4D03	0xB7
MSPM0L1306SDYYR	0xBB70	0xE	MSPM0L1305SDYYR	0x4D03	0x91
MSPM0L1306TDYYR	0xBB70	0x35	MSPM0L1305TDYYR	0x4D03	0xDE
MSPM0L1306QDYYR	0xBB70	0x9F	MSPM0L1305QDYYR	0x4D03	0xEC
MSPM0L1304SRHBR	0xD717	0xE4	MSPM0L1303SRGER	0xEF0	0x17
MSPM0L1304TRHBR	0xD717	0x5A	MSPM0L1303TRGER	0xEF0	0xE2
MSPM0L1304QRHBR	0xD717	0xA9	MSPM0L1346TDGS28R	0xF2B5	0xEF
MSPM0L1304SDGS28R	0xD717	0x73	MSPM0L1345TDGS28R	0x98B4	0x74
MSPM0L1304TDGS28R	0xD717	0xA8	MSPM0L1344TDGS20R	0x40B0	0xD0
MSPM0L1304QDGS28R	0xD717	0xB6	MSPM0L1343TDGS20R	0xB231	0x2E
MSPM0L1304SRGER	0xD717	0x26			
MSPM0L1304TRGER	0xD717	0xB7			
MSPM0L1304SDGS20R	0xD717	0xFA			
MSPM0L1304TDGS20R	0xD717	0x33			
MSPM0L1304QDGS20R	0xD717	0x91			
MSPM0L1304SDYYR	0xD717	0xB7			
MSPM0L1304TDYYR	0xD717	0xF9			
MSPM0L1304QDYYR	0xD717	0xA0			

8.29 Identification

Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region (see the Device Factory Constants section) which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. For more information, see the *Factory Constants* chapter of the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata describes these markings.

9 Applications, Implementation, and Layout

9.1 Typical Application

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1.1 Schematic

TI recommends connecting a combination of a 10-µF and a 0.1-µF low-ESR ceramic decoupling capacitor across the VDD and VSS pins, as well as placing these capacitors as close as possible to the supply pins that they decouple (within a few millimeters) to achieve a minimal loop area. The 10-µF bulk decoupling capacitor is a recommended value for most applications, but this capacitance may be adjusted if needed based upon the PCB design and application requirements. For example, larger bulk capacitors can be used, but this can affect the supply rail ramp-up time.

The NRST reset pin must be pulled up to VDD (supply level) for the device to release from RESET state and start the boot process. TI recommends connecting an external 47-kΩ pullup resistor with a 10-nF pulldown capacitor for most applications, enabling the NRST pin to be controlled by another device or a debug probe.

The SYSOSC frequency correction loop (FCL) circuit utilizes an external 100-kΩ with 0.1% tolerance resistor with a temperature coefficient (TCR) of 25ppm/C or better populated between the ROSC pin and VSS. This resistor establishes a reference current to stabilize the SYSOSC frequency through a correction loop. This resistor is required if the FCL feature is used for higher accuracy, and it is not required if the SYSOSC FCL is not enabled. When the FCL mode is not used, the PA2 pin may be used as a digital input/output pin.

A 0.47-µF tank capacitor is required for the VCORE pin and must be placed close to the device with minimum distance to the device ground. Do not connect other circuits to the VCORE pin.

For the 5-V-tolerant open drain (ODIO), a pullup resistor is required to output high for I2C and UART functions, as the open drain IO only implement a low-side NMOS driver and no high-side PMOS driver. The 5V-tolerant open drain IO are fail-safe and may have a voltage present even if VDD is not supplied.

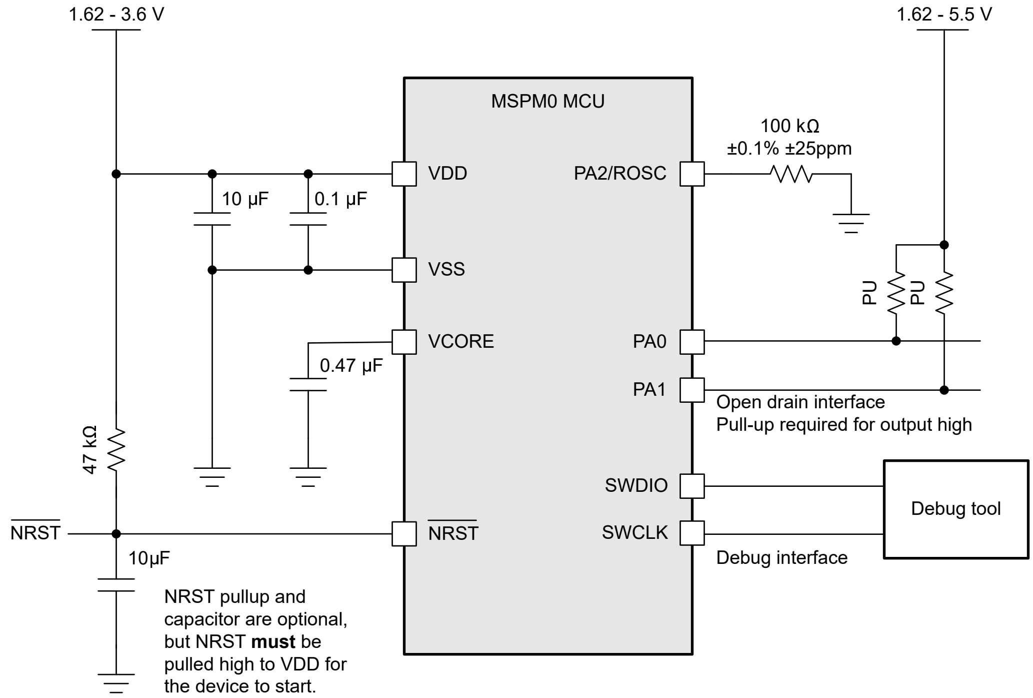


Figure 9-1. Basic Application Schematic

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. . Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X or XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

X and XMSdevices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 10-1 provides a legend for reading the complete device name.

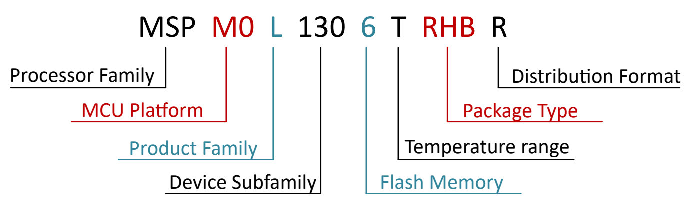


Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

Processor Family	MSP = Mixed-signal processor X, XMS = Experimental silicon
MCU Platform	M0 = Arm-based 32-bit M0+
Product Family	L = 32-MHz frequency
Device Subfamily	130 = ADC, 2x OPA, COMP 134 = ADC, 2x OPA (10-pA input bias current), COMP
Internal Memory	3 = 8KB flash, 2KB SRAM 4 = 16KB flash, 2KB SRAM 5 = 32KB flash, 4KB SRAM 6 = 64KB flash, 4KB SRAM
Temperature Range	T = –40°C to 105°C S = –40°C to 125°C
Package Type	See Table 5-1 and www.ti.com/packaging
Distribution Format	T = Small reel R = Large reel No marking = Tube or tray

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

10.2 Tools and Software

Design Kits and Evaluation Modules

MSPM0 LaunchPad (LP) Boards: LP-MSPM0L1306	Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming, debugging, and EnergyTrace™ technology. The LP ecosystem includes dozens of BoosterPack™ stackable plug-in modules to extend functionality.
Embedded Software	
MSPM0 Software Development Kit (SDK)	Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.
Software Development Tools	
TI Cloud Tools	Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.
TI Resource Explorer	Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.
SysConfig	Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE or in TI Cloud Tools. (offline version)
MSP Academy	Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.
GUI Composer	GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.
IDE & compiler tool chains	
Code Composer Studio™ (CCS)	Includes TI Arm-Clang compiler. Supports all TI Arm Cortex MCUs and boasts competitive code size performance advantages, fast compile time, code coverage support, safety certification support, and completely free to use.
IAR Embedded Workbench® IDE	
Keil® MDK IDE	
GNU Arm Embedded Tool Chain	

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

LaunchPad™, Code Composer Studio™, TI E2E™, EnergyTrace™, and BoosterPack™ are trademarks of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

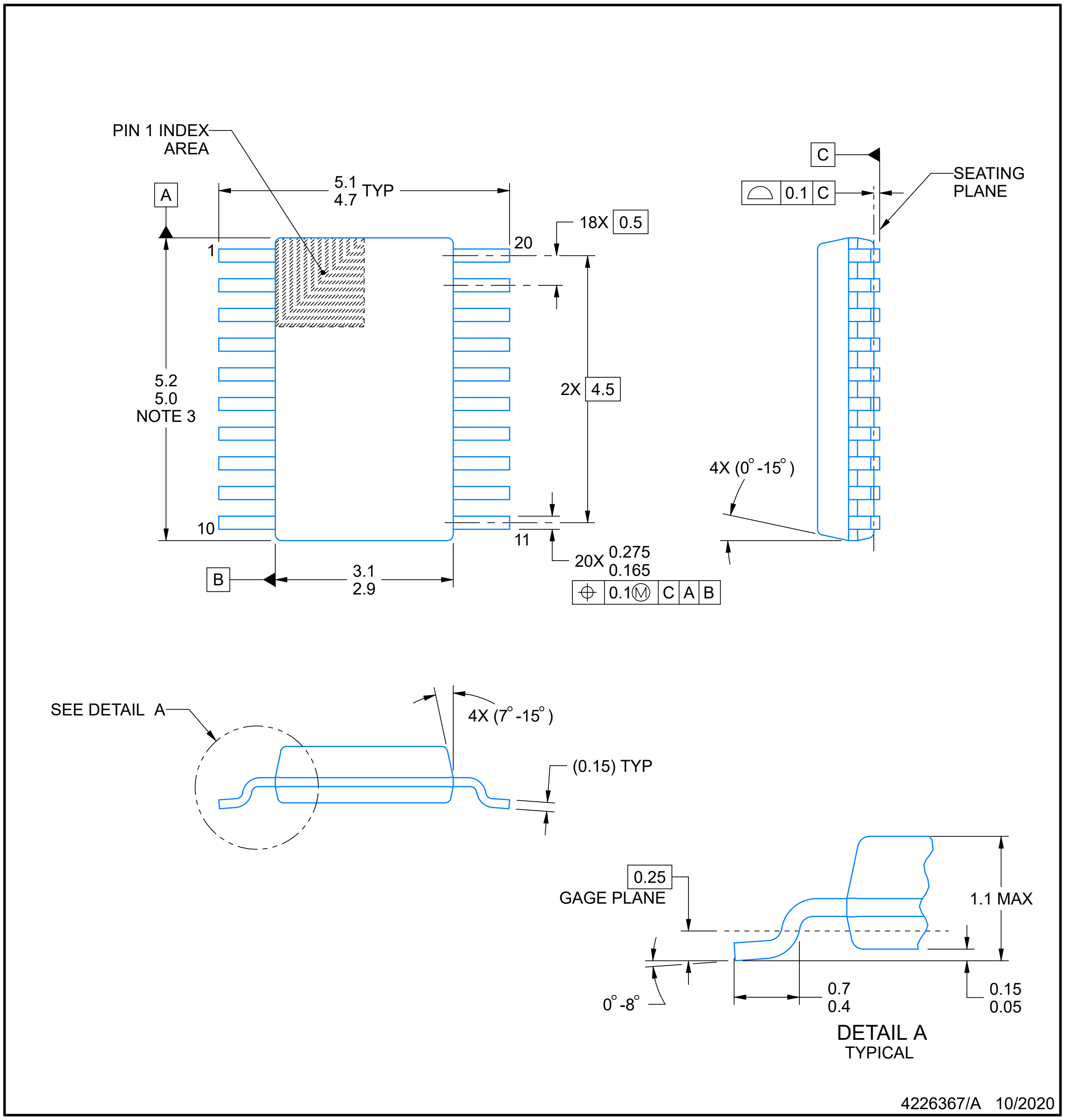
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

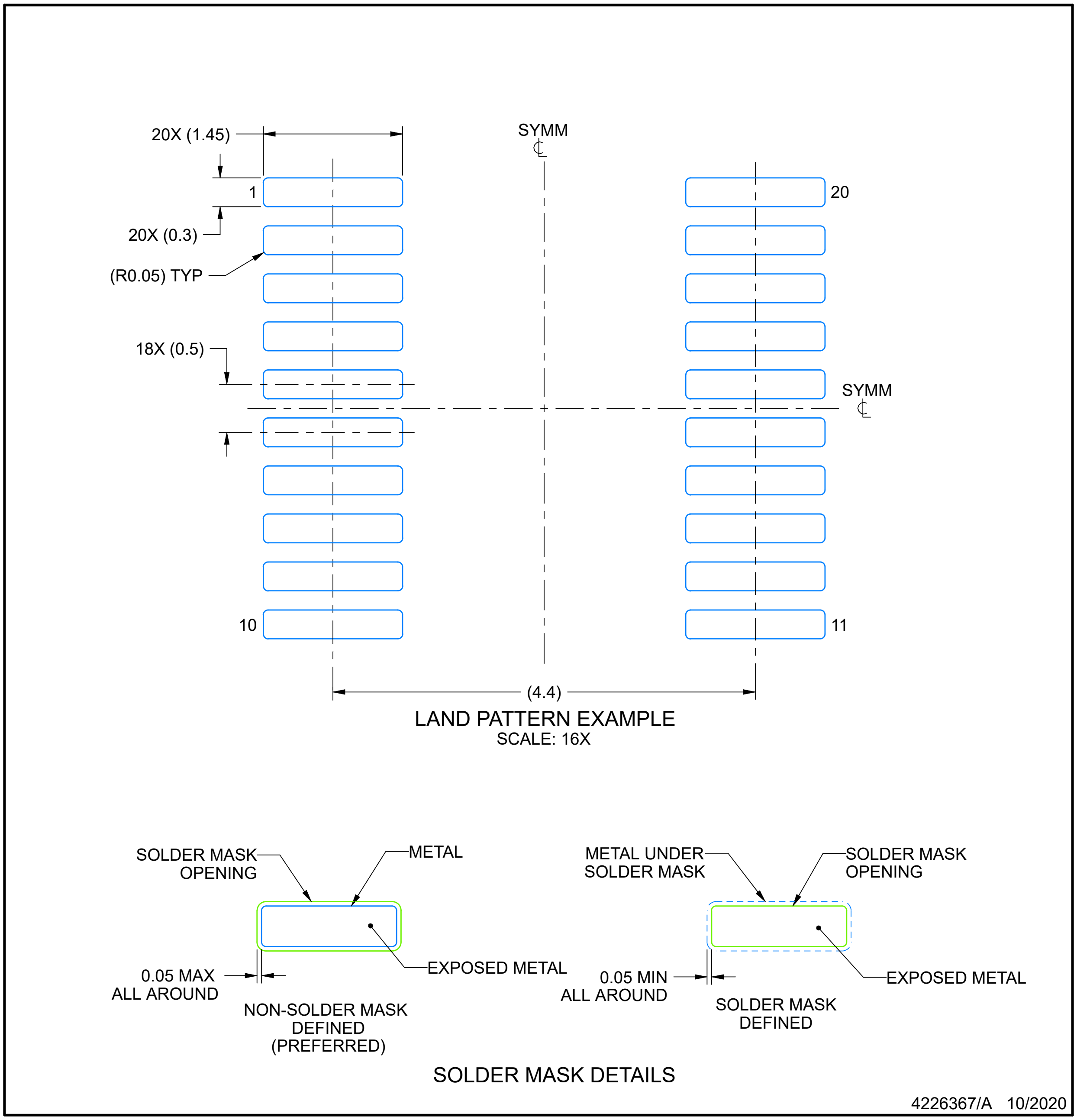
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

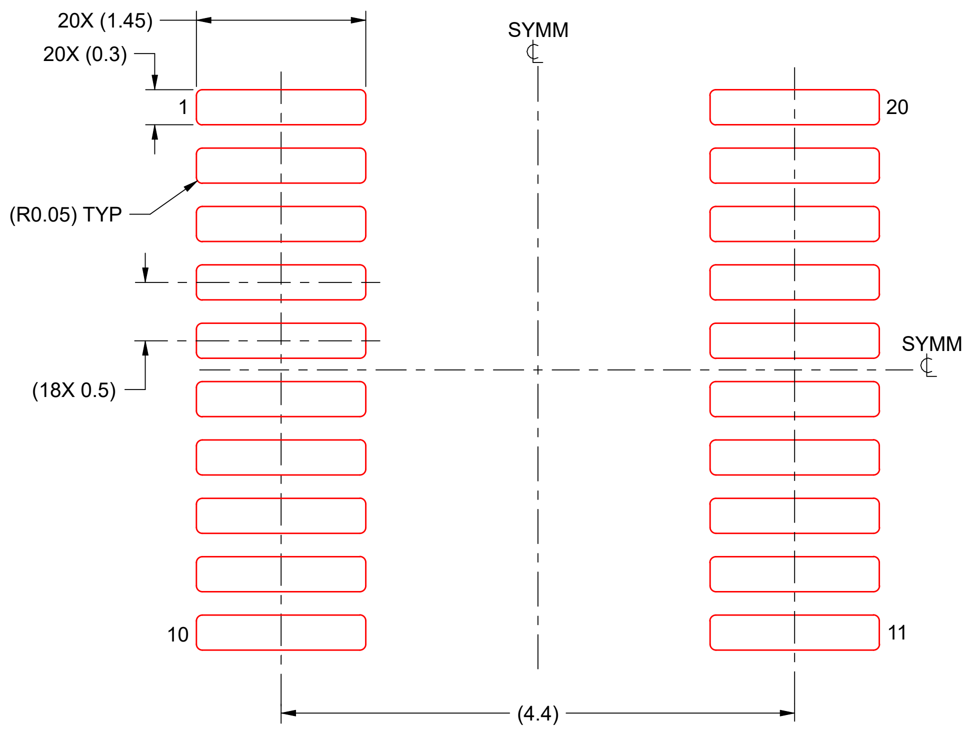
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

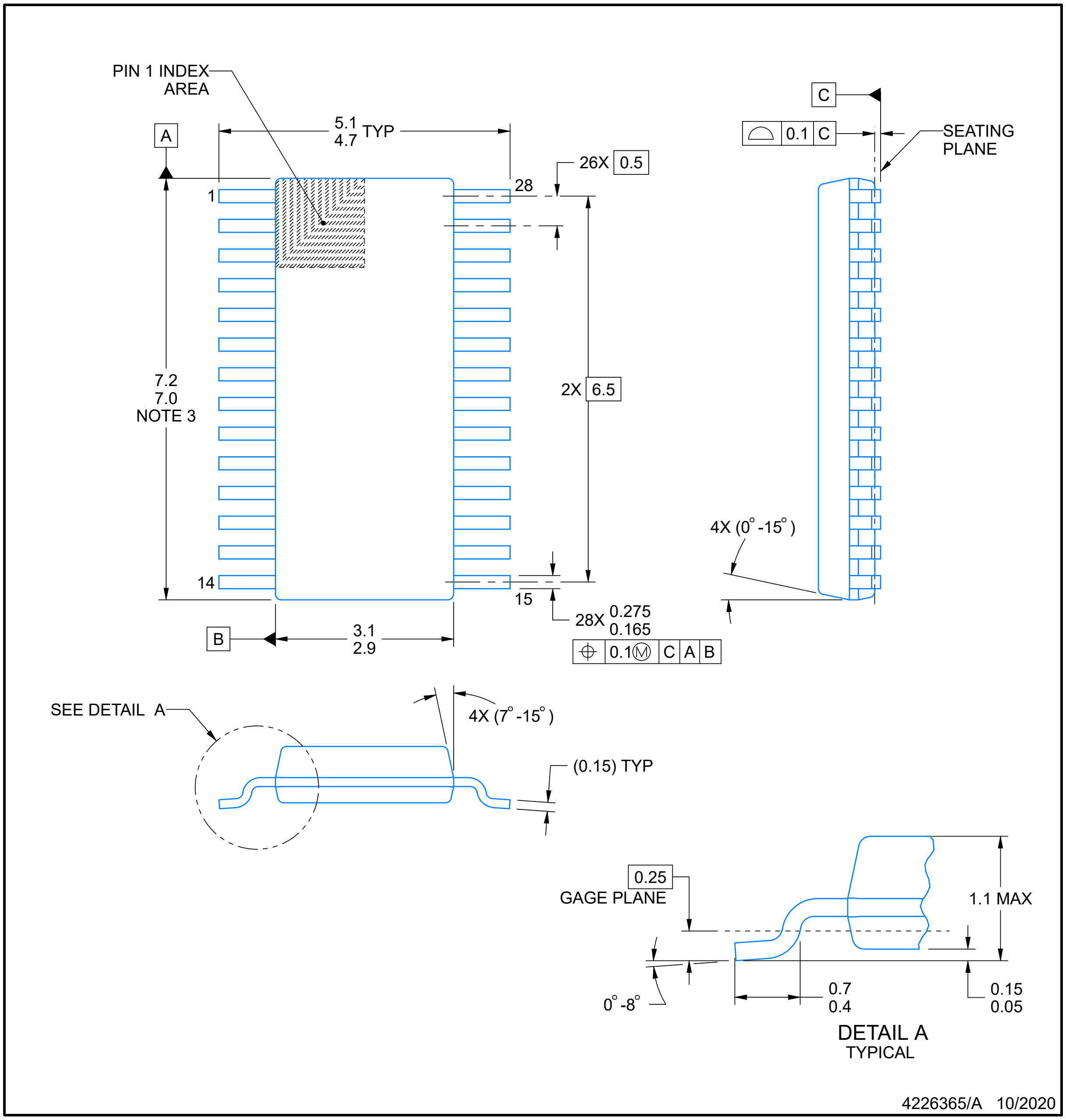
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

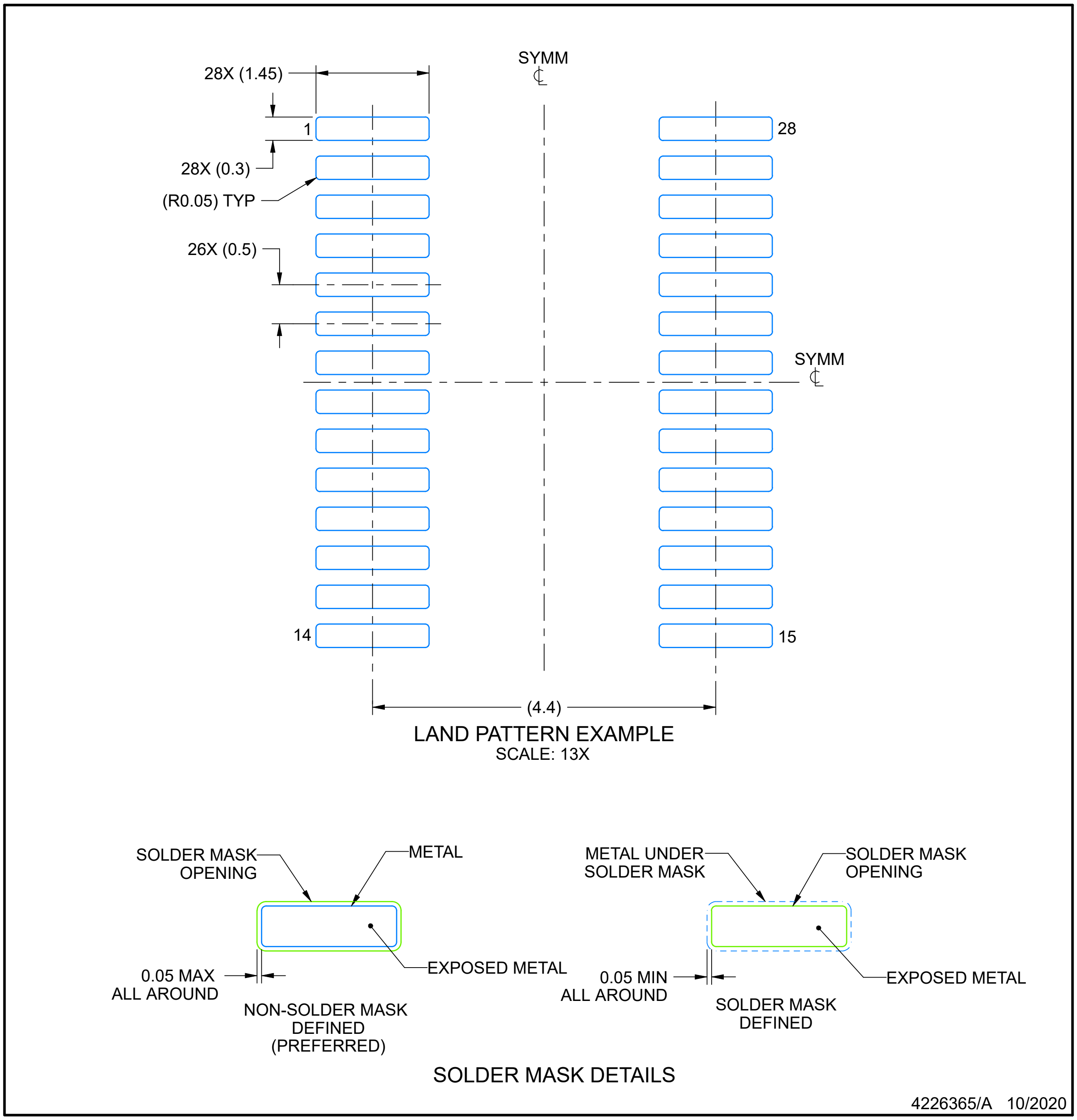
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

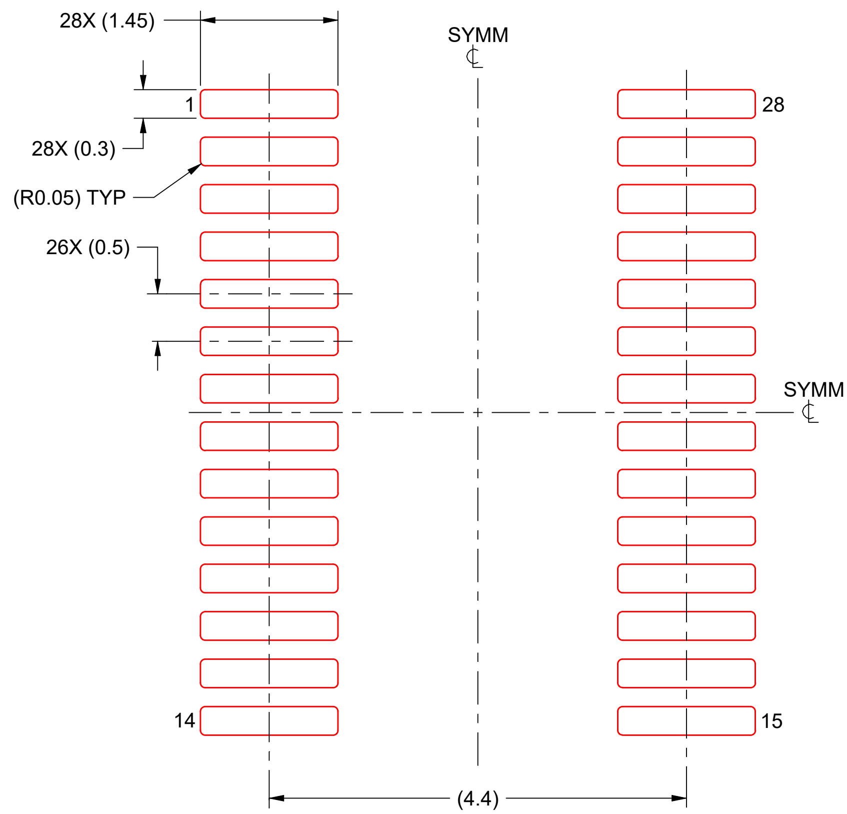
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 13X

4226365/A 10/2020

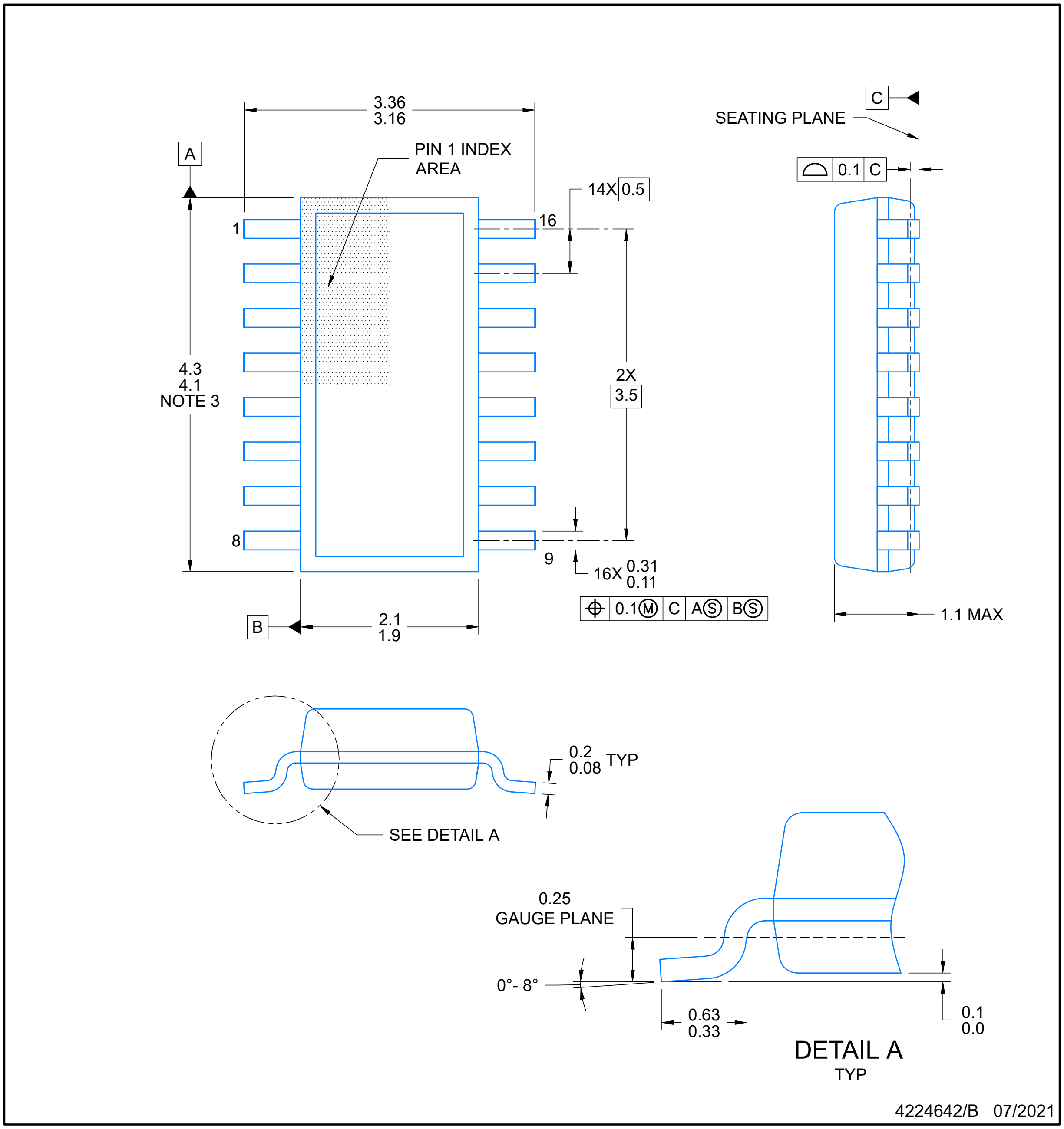
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0016A SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



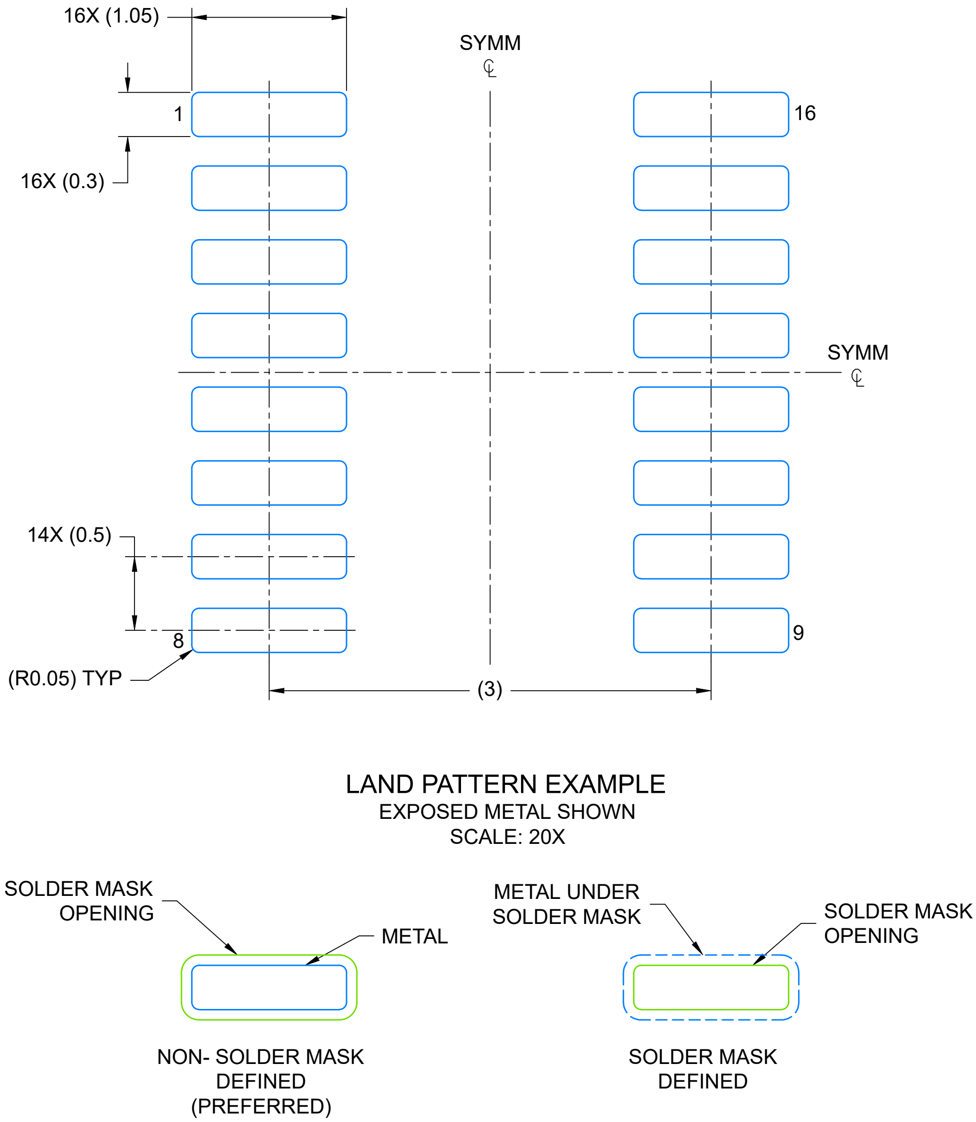
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA

EXAMPLE BOARD LAYOUT

DYY0016A SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

SOLDER MASK DETAILS

4224642/B 07/2021

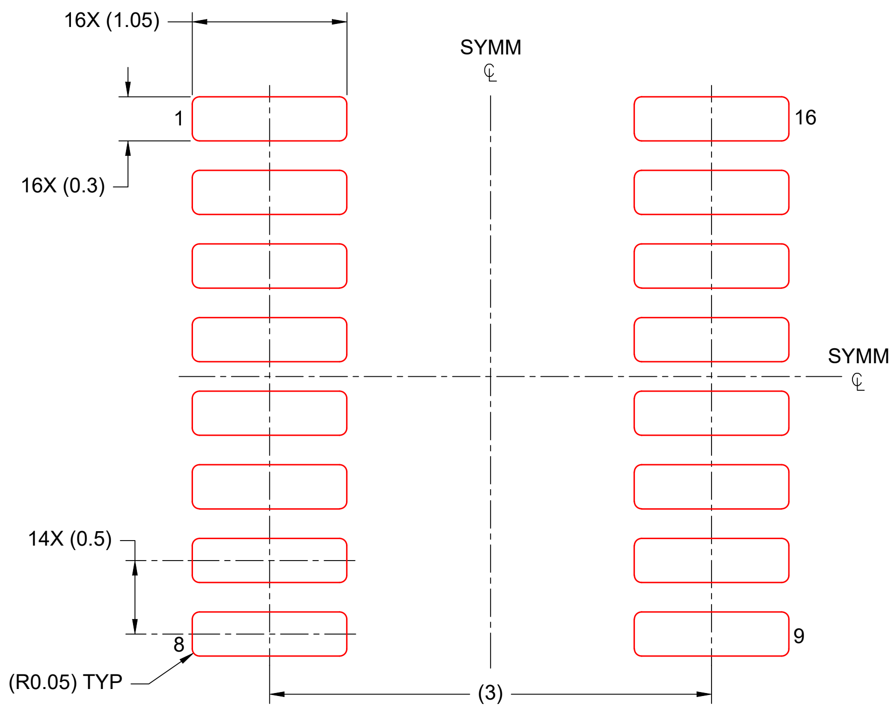
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYY0016A SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/B 07/2021

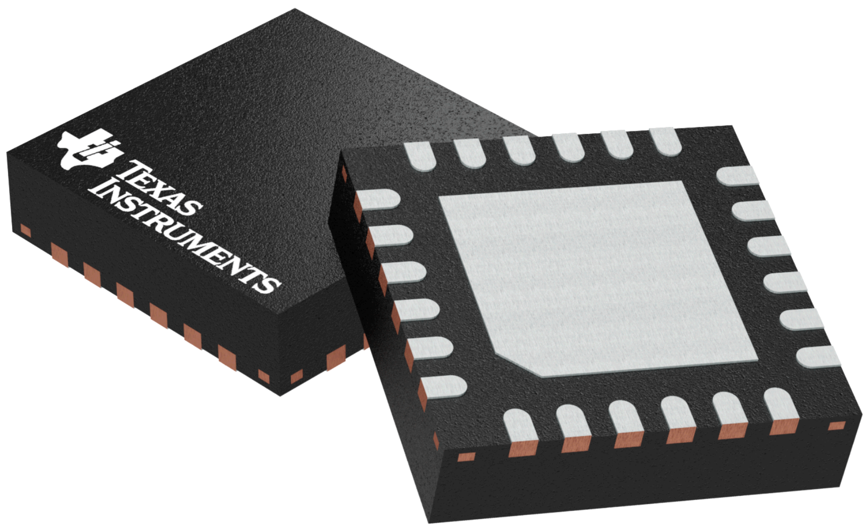
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

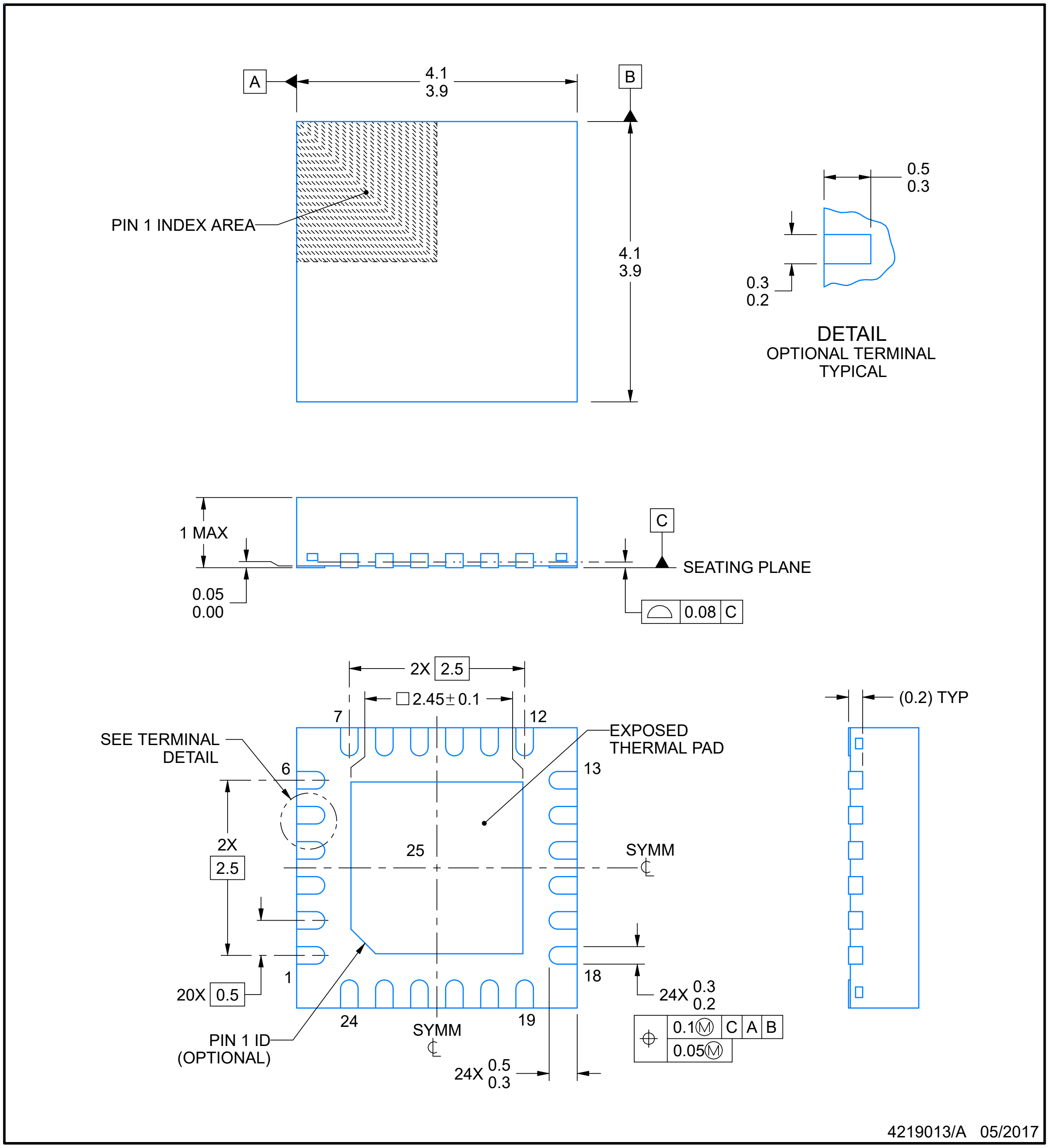
4204104/H

PACKAGE OUTLINE

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

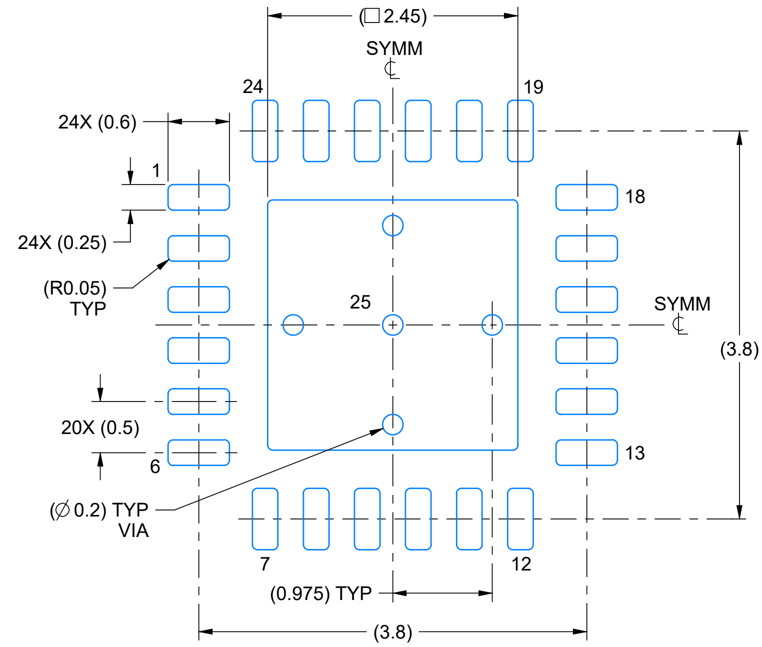
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

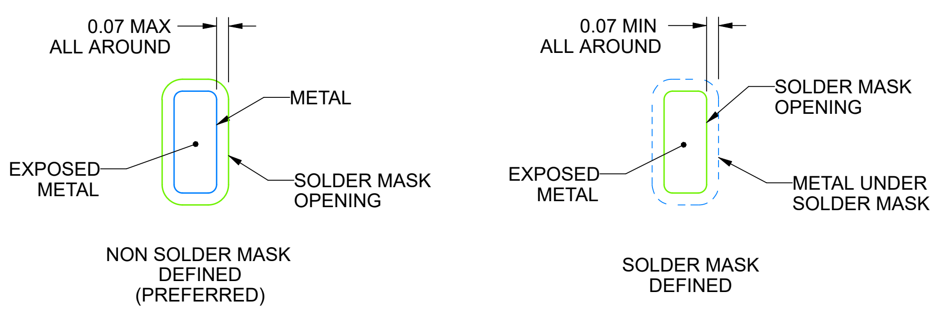
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

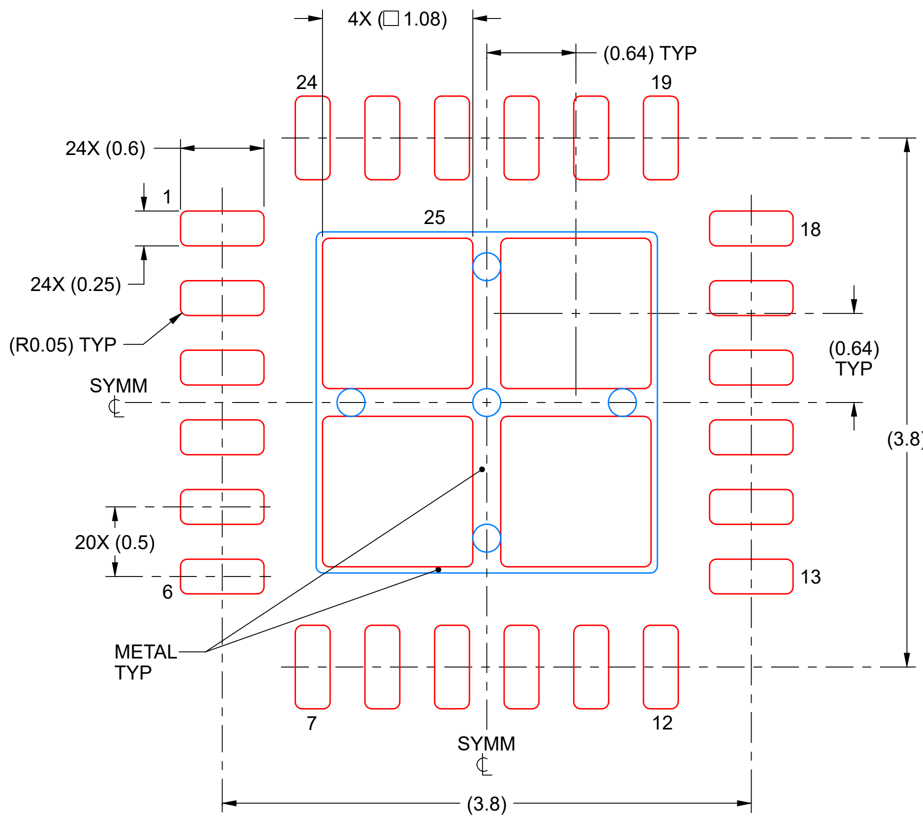
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

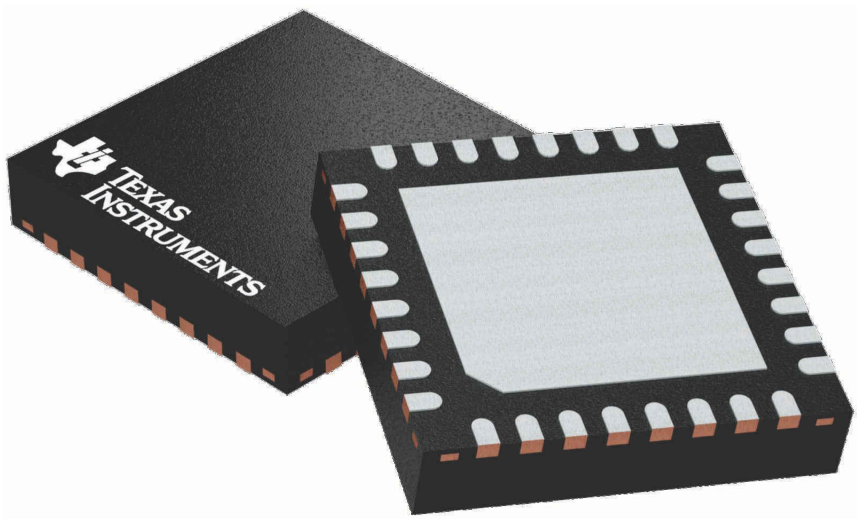
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

RHB 32 — VQFN - 1 mm max height

5 x 5, 0.5 mm pitch — PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

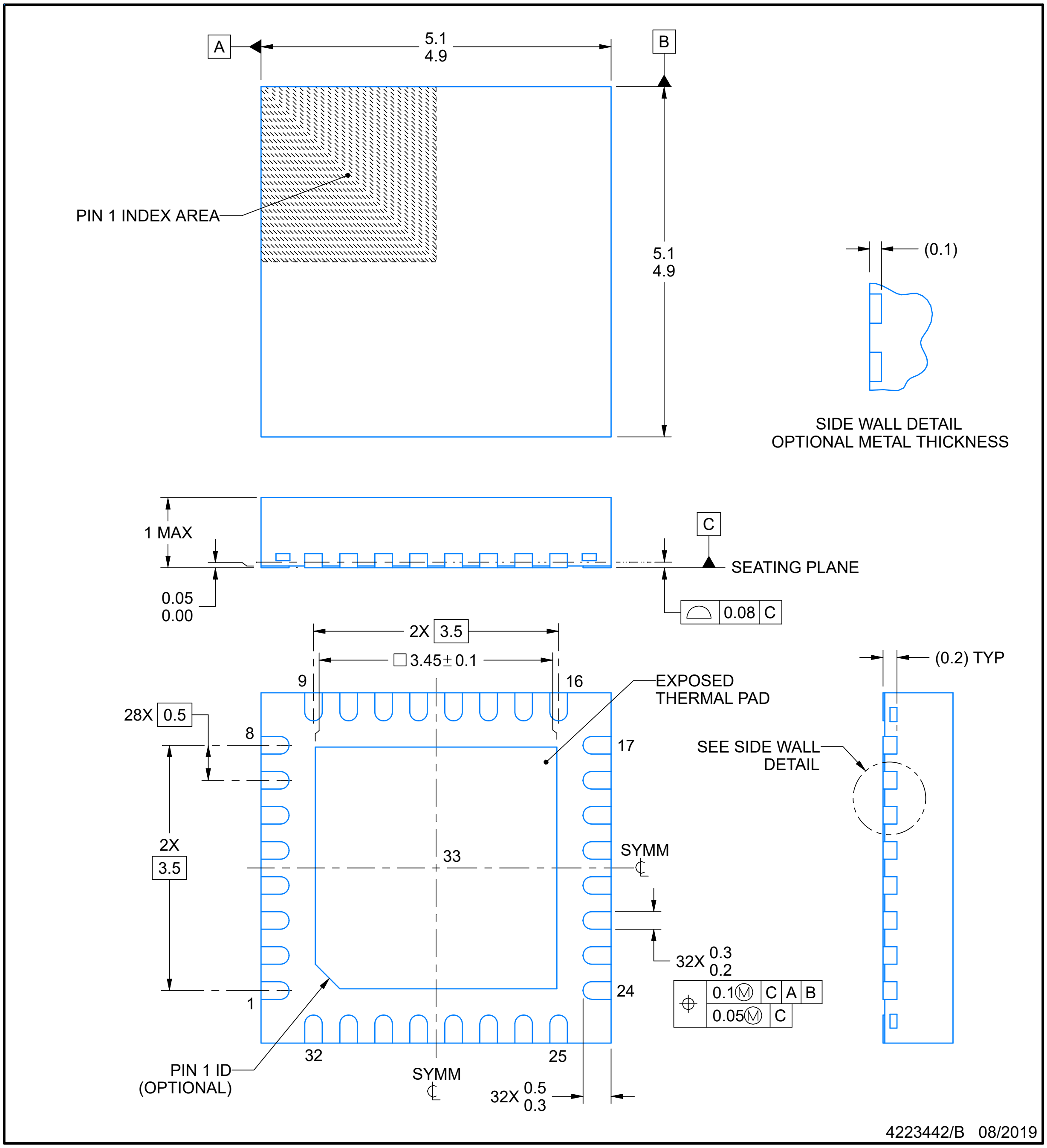
4224745/A

PACKAGE OUTLINE

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

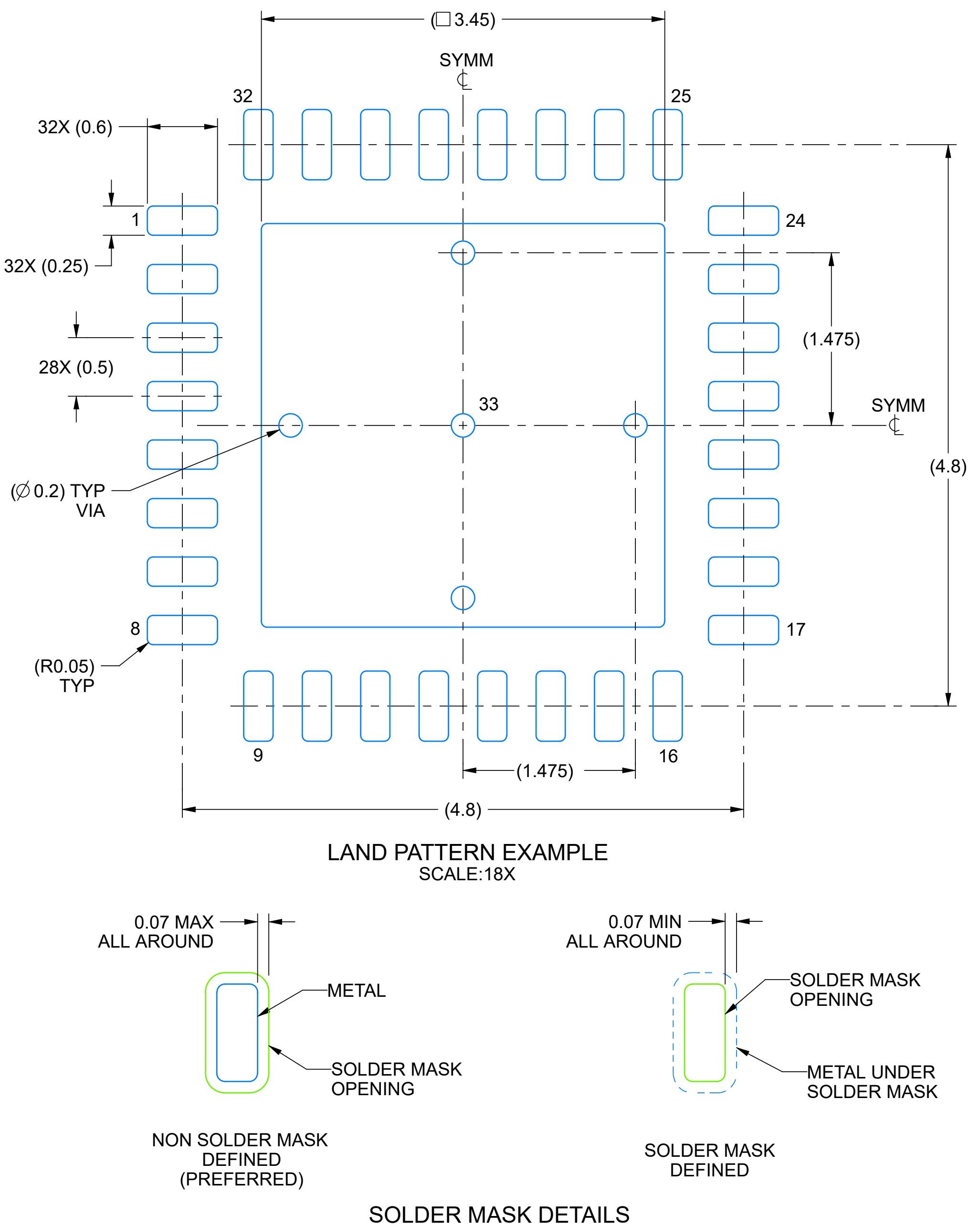
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4223442/B 08/2019

NOTES: (continued)

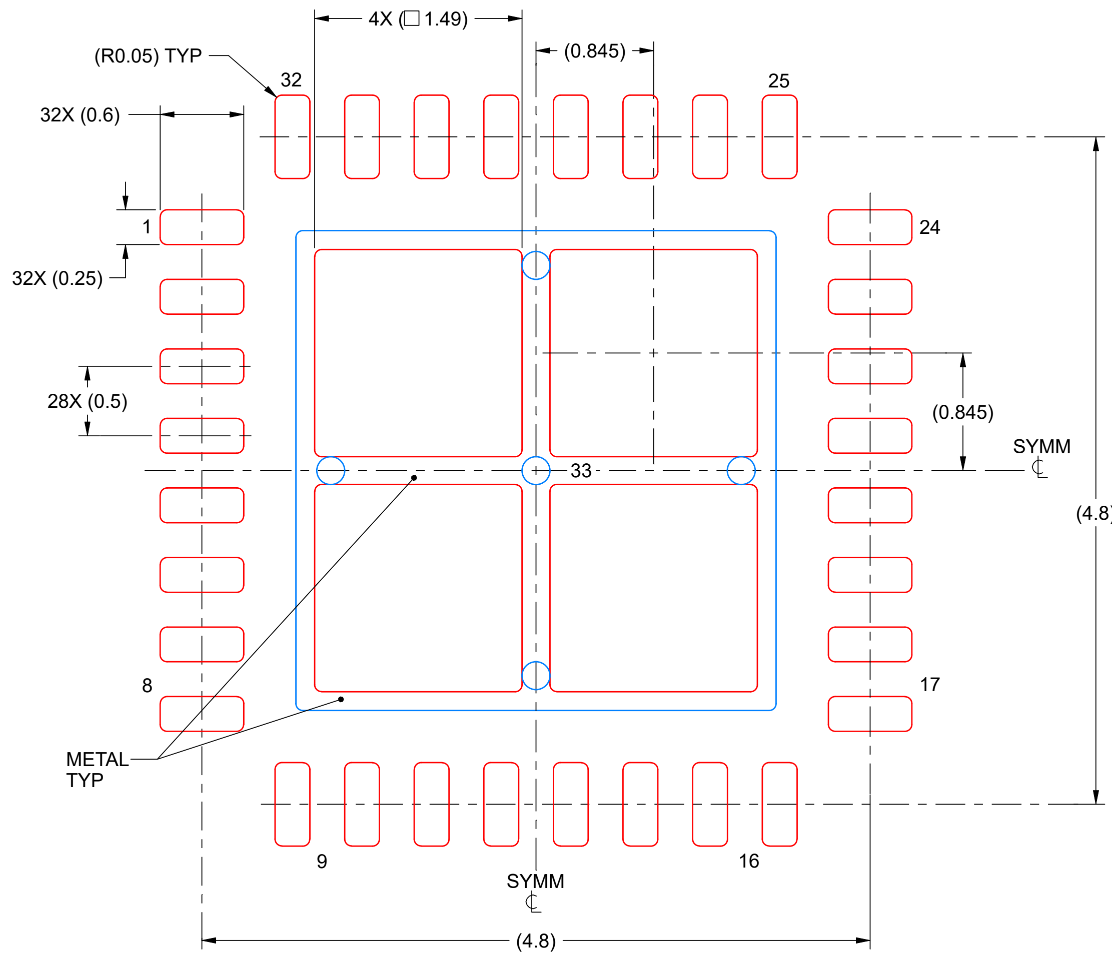
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

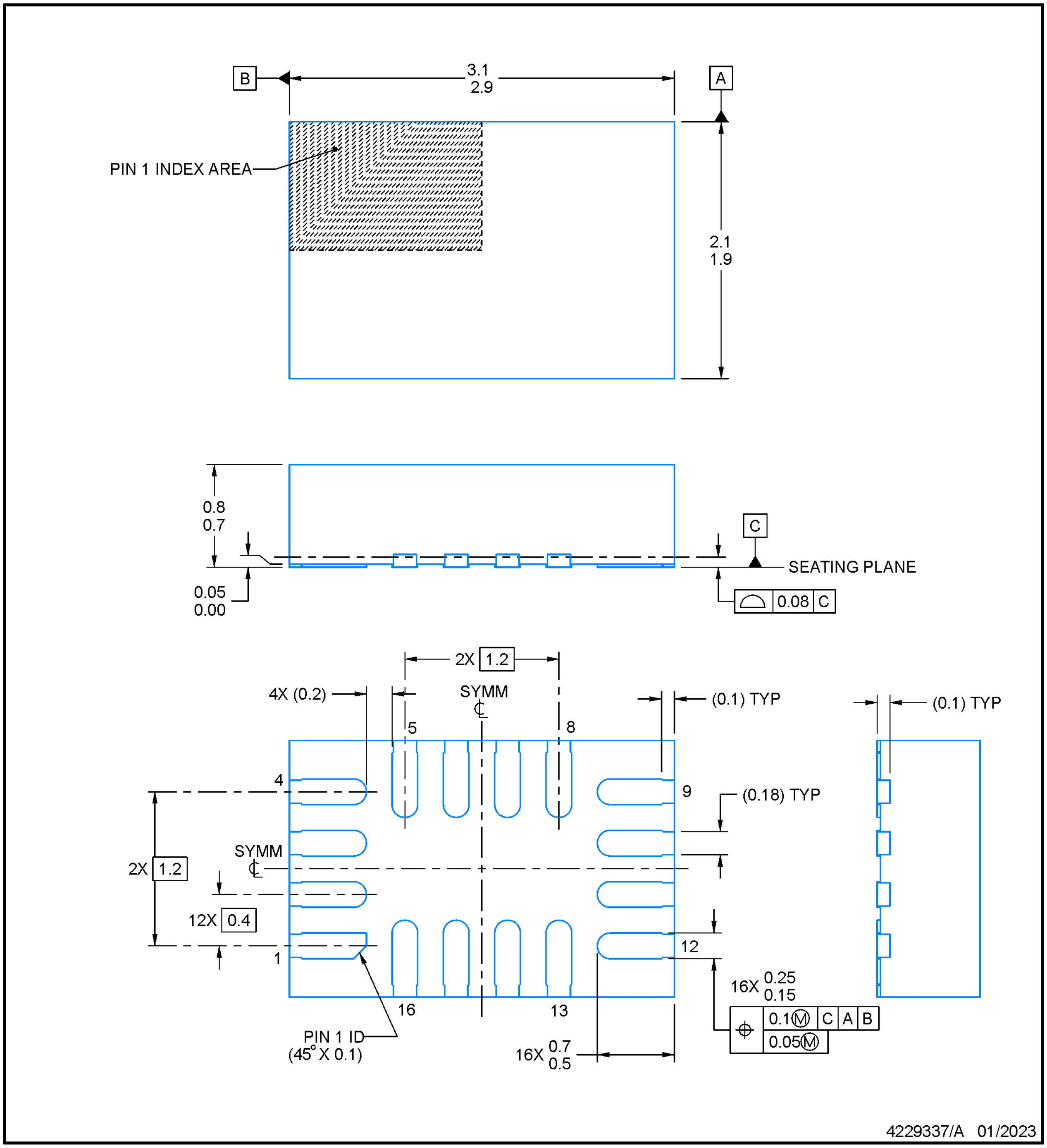
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RTR0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

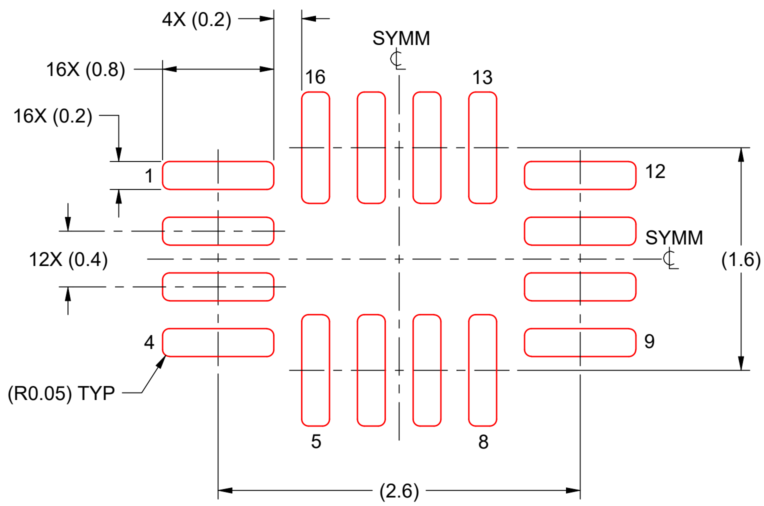
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE STENCIL DESIGN

RTR0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4229337/A 01/2023

NOTES: (continued)

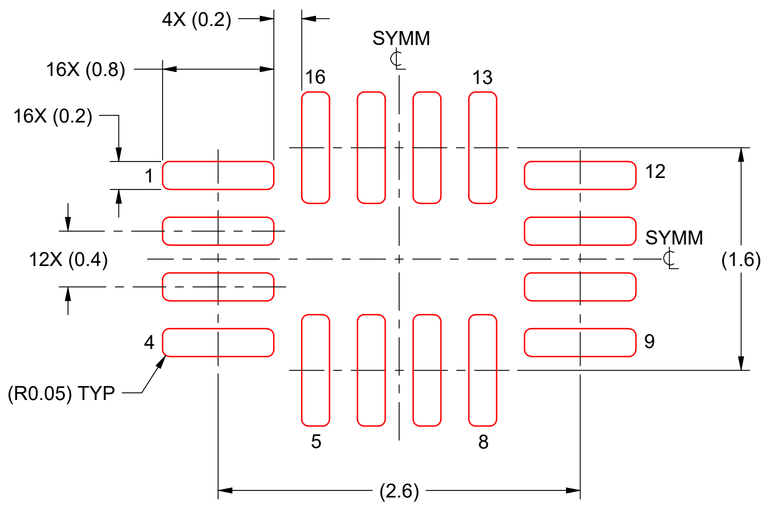
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE STENCIL DESIGN

RTR0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4229337/A 01/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 28, 2023 to June 26, 2023	Page
• Released the MSPM0L134x devices	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSPM0L1303SRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1303S	Samples
MSPM0L1303TRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	MSPM0 L1303T	Samples
MSPM0L1304SDGS20R	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1304S	Samples
MSPM0L1304SDGS28R	ACTIVE	VSSOP	DGS	28	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L1304S	Samples
MSPM0L1304SDYYR	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M0L1304S	Samples
MSPM0L1304SRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1304S	Samples
MSPM0L1304SRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1304S	Samples
MSPM0L1304TDGS20R	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	M0L1304T	Samples
MSPM0L1304TDGS28R	ACTIVE	VSSOP	DGS	28	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	L1304T	Samples
MSPM0L1304TDYYR	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	M0L1304T	Samples
MSPM0L1304TRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	MSPM0 L1304T	Samples
MSPM0L1304TRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	MSPM0 L1304T	Samples
MSPM0L1305SDGS20R	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1305S	Samples
MSPM0L1305SDGS28R	ACTIVE	VSSOP	DGS	28	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L1305S	Samples
MSPM0L1305SDYYR	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M0L1305S	Samples
MSPM0L1305SRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1305S	Samples
MSPM0L1305SRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1305S	Samples
MSPM0L1305TDGS20R	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	M0L1305T	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSPM0L1305TDGS28R	ACTIVE	VSSOP	DGS	28	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	L1305T	Samples
MSPM0L1305TDYYR	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	M0L1305T	Samples
MSPM0L1305TRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	MSPM0 L1305T	Samples
MSPM0L1305TRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	MSPM0 L1305T	Samples
MSPM0L1306SDGS20R	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0L1306S	Samples
MSPM0L1306SDGS28R	ACTIVE	VSSOP	DGS	28	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L1306S	Samples
MSPM0L1306SDYYR	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M0L1306S	Samples
MSPM0L1306SRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1306S	Samples
MSPM0L1306SRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MSPM0 L1306S	Samples
MSPM0L1306TDGS20R	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	M0L1306T	Samples
MSPM0L1306TDGS28R	ACTIVE	VSSOP	DGS	28	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	L1306T	Samples
MSPM0L1306TDYYR	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	M0L1306T	Samples
MSPM0L1306TRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	MSPM0 L1306T	Samples
MSPM0L1306TRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	MSPM0 L1306T	Samples
MSPM0L1343TDGS20R	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	M0L1343T	Samples
MSPM0L1344TDGS20R	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	M0L1344T	Samples
MSPM0L1345TDGS28R	ACTIVE	VSSOP	DGS	28	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	L1345T	Samples
MSPM0L1346TDGS28R	ACTIVE	VSSOP	DGS	28	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	L1346T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

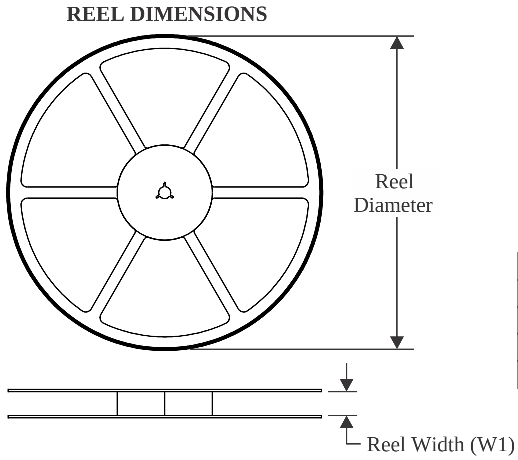
OTHER QUALIFIED VERSIONS OF MSPM0L1305, MSPM0L1306 :

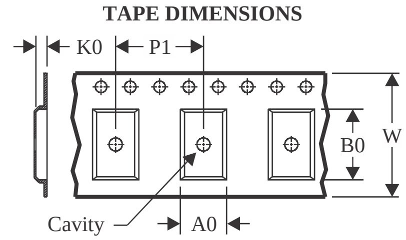
- Automotive : MSPM0L1305-Q1, MSPM0L1306-Q1

NOTE: Qualified Version Definitions:

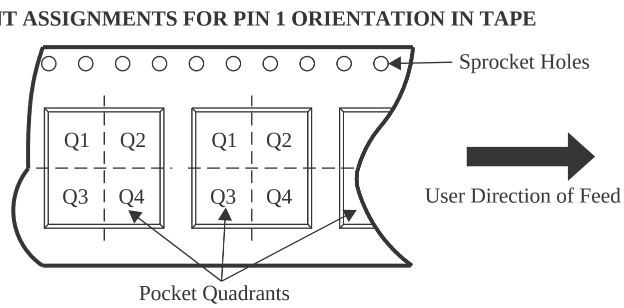
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

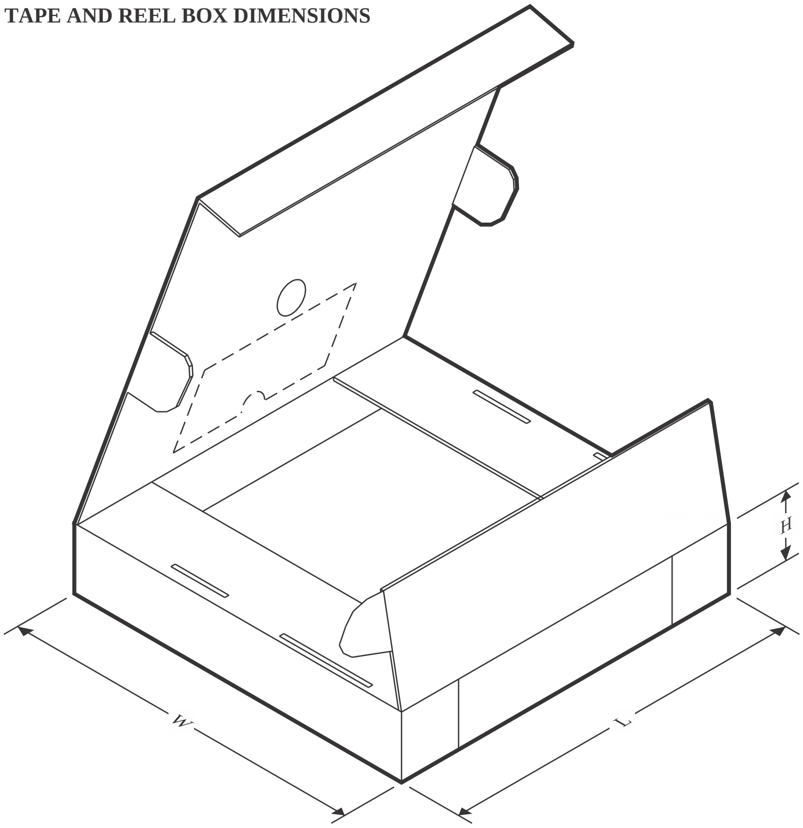


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSPM0L1303SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSPM0L1303TRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSPM0L1304SDGS20R	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
MSPM0L1304SDGS28R	VSSOP	DGS	28	5000	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1
MSPM0L1304SDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
MSPM0L1304SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSPM0L1304SRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSPM0L1304TDGS20R	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
MSPM0L1304TDGS28R	VSSOP	DGS	28	5000	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1
MSPM0L1304TDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
MSPM0L1304TRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSPM0L1304TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSPM0L1305SDGS20R	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
MSPM0L1305SDGS28R	VSSOP	DGS	28	5000	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSPM0L1305SDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
MSPM0L1305SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSPM0L1305SRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSPM0L1305TDGS20R	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
MSPM0L1305TDGS28R	VSSOP	DGS	28	5000	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1
MSPM0L1305TDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
MSPM0L1305TRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSPM0L1305TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSPM0L1306SDGS20R	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
MSPM0L1306SDGS28R	VSSOP	DGS	28	5000	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1
MSPM0L1306SDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
MSPM0L1306SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSPM0L1306SRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSPM0L1306TDGS20R	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
MSPM0L1306TDGS28R	VSSOP	DGS	28	5000	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1
MSPM0L1306TDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
MSPM0L1306TRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
MSPM0L1306TRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSPM0L1343TDGS20R	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
MSPM0L1344TDGS20R	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
MSPM0L1345TDGS28R	VSSOP	DGS	28	5000	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1
MSPM0L1346TDGS28R	VSSOP	DGS	28	5000	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSPM0L1303SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSPM0L1303TRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSPM0L1304SDGS20R	VSSOP	DGS	20	5000	356.0	356.0	35.0
MSPM0L1304SDGS28R	VSSOP	DGS	28	5000	356.0	356.0	35.0
MSPM0L1304SDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
MSPM0L1304SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSPM0L1304SRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSPM0L1304TDGS20R	VSSOP	DGS	20	5000	356.0	356.0	35.0
MSPM0L1304TDGS28R	VSSOP	DGS	28	5000	356.0	356.0	35.0
MSPM0L1304TDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
MSPM0L1304TRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSPM0L1304TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSPM0L1305SDGS20R	VSSOP	DGS	20	5000	356.0	356.0	35.0
MSPM0L1305SDGS28R	VSSOP	DGS	28	5000	356.0	356.0	35.0
MSPM0L1305SDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
MSPM0L1305SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSPM0L1305SRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSPM0L1305TDGS20R	VSSOP	DGS	20	5000	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSPM0L1305TDGS28R	VSSOP	DGS	28	5000	356.0	356.0	35.0
MSPM0L1305TDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
MSPM0L1305TRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSPM0L1305TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSPM0L1306SDGS20R	VSSOP	DGS	20	5000	356.0	356.0	35.0
MSPM0L1306SDGS28R	VSSOP	DGS	28	5000	356.0	356.0	35.0
MSPM0L1306SDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
MSPM0L1306SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSPM0L1306SRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSPM0L1306TDGS20R	VSSOP	DGS	20	5000	356.0	356.0	35.0
MSPM0L1306TDGS28R	VSSOP	DGS	28	5000	356.0	356.0	35.0
MSPM0L1306TDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
MSPM0L1306TRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
MSPM0L1306TRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
MSPM0L1343TDGS20R	VSSOP	DGS	20	5000	356.0	356.0	35.0
MSPM0L1344TDGS20R	VSSOP	DGS	20	5000	356.0	356.0	35.0
MSPM0L1345TDGS28R	VSSOP	DGS	28	5000	356.0	356.0	35.0
MSPM0L1346TDGS28R	VSSOP	DGS	28	5000	356.0	356.0	35.0

IMPORTANT NOTICE AND DISCLAIMER