

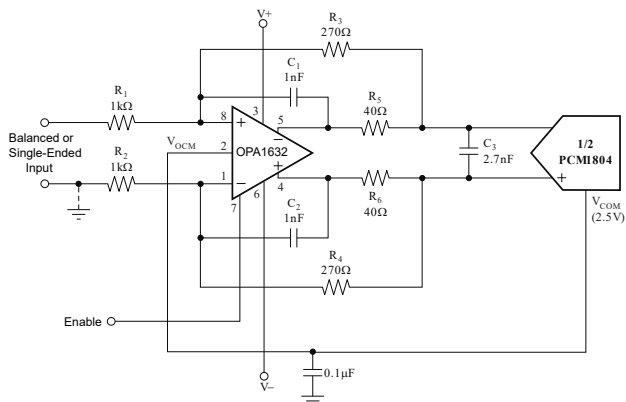
## OPA1632 高性能、全差分音频运算放大器

### 1 特性

- 出色音质
- 超低失真：0.000028%
- 低噪声：1.25nV/√Hz
- 高速：
  - 压摆率：72V/μs
  - 增益带宽积：180 MHz
- 完全差分架构：
  - 平衡输入和输出将单端输入转换为平衡差分输出
- 宽电源电压范围：±2.5V 至 ±15V
- 关断电流：0.85mA ( $V_S = \pm 5V$ )
- 温度范围：-40°C 至 +85°C

### 2 应用

- 专业音频混合器或控制平面
- 专业麦克风和无线系统
- 专业扬声器系统
- 专业音频放大器
- 条形音箱
- 转盘
- 专业摄像机
- 吉他和其他乐器放大器
- 数据采集 (DAQ)



应用示意图

### 3 说明

OPA1632 是一款全差分放大器，旨在驱动高性能音频模数转换器 (ADC) 或用作 D 类放大器的前置驱动器。它可实现卓越的音频质量、极低的噪声、大输出电压摆幅和高电流驱动。OPA1632 具有 180MHz 的出色增益带宽以及 72V/μs 的超快压摆率，可实现极低的失真。非常低的输入电压噪声 1.25nV/√Hz 可进一步确保更大信噪比和动态范围。

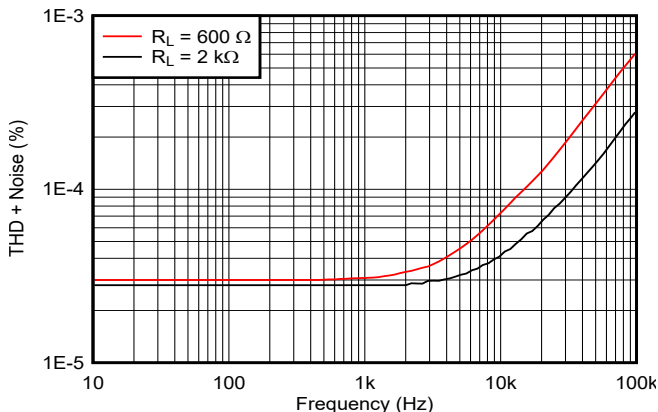
全差分架构的灵活性有助于轻松实现单端到全差分输出转换。差分输出可减少偶次谐波并最大限度地减少共模噪声干扰。OPA1632 在用于驱动高性能音频 ADC (如 PCM1804) 时可提供卓越的性能。添加了关断功能以在器件未使用时节省电量。

OPA1632 可在 -40°C 至 +85°C 的温度范围内正常运行，采用 SO-8 封装和散热增强型 MSOP-8 PowerPAD™ 封装。

#### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
OPA1632	SOIC (8)	4.90mm × 3.91mm
	MSOP-PowerPAD (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



THD+N 与频率间的关系



## Table of Contents

<b>1 特性</b> .....	1	<b>8 Application and Implementation</b> .....	18
<b>2 应用</b> .....	1	8.1 Application Information.....	18
<b>3 说明</b> .....	1	8.2 Typical Application.....	19
<b>4 Revision History</b> .....	2	<b>9 Power Supply Recommendations</b> .....	21
<b>5 Pin Configuration and Functions</b> .....	5	<b>10 Layout</b> .....	21
<b>6 Specifications</b> .....	6	10.1 Layout Guidelines.....	21
6.1 Absolute Maximum Ratings.....	6	10.2 Layout Example.....	23
6.2 ESD Ratings.....	6	<b>11 Device and Documentation Support</b> .....	25
6.3 Recommended Operating Conditions.....	6	11.1 Documentation Support.....	25
6.4 Thermal Information.....	7	11.2 第三方产品免责声明.....	25
6.5 Electrical Characteristics: OPA1632D.....	8	11.3 接收文档更新通知.....	25
6.6 Electrical Characteristics: OPA1632DGN.....	10	11.4 支持资源.....	25
6.7 Typical Characteristics: OPA1632D.....	12	11.5 Trademarks.....	25
6.8 Typical Characteristics: OPA1632DGN.....	14	11.6 Electrostatic Discharge Caution.....	25
<b>7 Detailed Description</b> .....	16	11.7 Export Control Notice.....	25
7.1 Overview.....	16	11.8 术语表.....	26
7.2 Functional Block Diagram.....	16	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	26
7.3 Feature Description.....	16		
7.4 Device Functional Modes.....	17		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (September 2015) to Revision D (March 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 更新了 <i>特性</i> 部分.....	1
• 更新了 <i>应用</i> 部分.....	1
• 更新了 <i>说明</i> 部分.....	1
• 更改了 <i>说明</i> 部分中 SOIC 和 MSOP-PowerPAD 封装的标称封装尺寸.....	1
• Updated <i>Pin Configuration and Functions</i> section.....	5
• Added Supply turn-on/off dV/dT specification to <i>Absolute Maximum Ratings</i> table.....	6
• Added continuous input current specification to <i>Absolute Maximum Ratings</i> table.....	6
• Changed differential input voltage in <i>Absolute Maximum Ratings</i> table from $\pm 3V$ to $\pm 1.5V$ .....	6
• Changed charged-device model (CDM) reference from JESD22-C101 to JS-002 in <i>ESD Ratings</i> table.....	6
• Changed minimum temperature range from $0.4^{\circ}C$ to $-40^{\circ}C$ in <i>Recommended Operating Conditions</i> table.....	6
• Updated thermal specifications for D package in <i>Thermal Information</i> table.....	7
• Changed typical offset voltage vs temperature from $\pm 5 \mu V^{\circ}C$ to $\pm 2.5 \mu V^{\circ}C$ in <i>Electrical Characteristics: OPA1632D</i> table.....	8
• Changed PSRR minimum limit of $316 \mu V/V$ to maximum limit in <i>Electrical Characteristics: OPA1632D</i> table ...	8
• Changed typical input bias current limit from $2\mu A$ to $7.9\mu A$ in <i>Electrical Characteristics: OPA1632D</i> table.....	8
• Changed Max input bias current limit from $6\mu A$ to $14\mu A$ in <i>Electrical Characteristics: OPA1632D</i> table.....	8
• Changed typical input voltage noise from $1.3nV/\sqrt{Hz}$ to $1.25nV/\sqrt{Hz}$ in <i>Electrical Characteristics: OPA1632D</i> table.....	8
• Changed typical input current noise from $0.4 pA/\sqrt{Hz}$ to $1.7 pA/\sqrt{Hz}$ in <i>Electrical Characteristics: OPA1632D</i> table.....	8
• Changed input impedance spec to show both common-mode and differential impedances in <i>Electrical Characteristics: OPA1632D</i> table.....	8
• Changed SSBW at $G = +2$ , $R_F = 602 \Omega$ from $90 MHz$ to $104 MHz$ in <i>Electrical Characteristics: OPA1632D</i> table.....	8

- Changed SSBW at  $G = +5$ ,  $R_F = 1.5 \text{ k}\Omega$  from 36 MHz to 46 MHz in *Electrical Characteristics: OPA1632D* table..... 8
- Changed SSBW at  $G = +5$ ,  $R_F = 1.5 \text{ k}\Omega$  from 18 MHz to 24 MHz in *Electrical Characteristics: OPA1632D* table..... 8
- Changed typical Large-Signal Bandwidth from 800 kHz to 1.8 MHz in *Electrical Characteristics: OPA1632D* table..... 8
- Changed typical slew rate from 50 V/  $\mu\text{s}$  to 72 V/  $\mu\text{s}$  in *Electrical Characteristics: OPA1632D* table ..... 8
- Changed typical rise/fall time from 100 ns to 69 ns in *Electrical Characteristics: OPA1632D* table..... 8
- Changed typical settling time to 0.1% from 75 ns to 36 ns in *Electrical Characteristics: OPA1632D* table..... 8
- Changed typical settling time to 0.01% from 200 ns to 49ns in *Electrical Characteristics: OPA1632D* table .... 8
- Changed typical THD+N with Differential Input/Output and  $R_L = 600 \Omega$  from 0.0003% to 0.00003% in *Electrical Characteristics: OPA1632D* table..... 8
- Changed typical THD+N with Differential Input/Output and  $R_L = 2\text{k}\Omega$  from 0.000022% to 0.000028% in *Electrical Characteristics: OPA1632D* table ..... 8
- Changed typical THD+N with single-ended Input/Output and  $R_L = 600\Omega$  from 0.000059% to 0.000036% in *Electrical Characteristics: OPA1632D* table ..... 8
- Changed typical THD+N with single-ended Input/Output and  $R_L = 2\text{k}\Omega$  from 0.000043% to 0.000031% in *Electrical Characteristics: OPA1632D* table ..... 8
- Changed IMD at differential input/output and  $R_L = 600\Omega$  from 0.00008% to 0.000061% in *Electrical Characteristics: OPA1632D* table..... 8
- Changed IMD at differential input/output and  $R_L = 2\text{k}\Omega$  from 0.00005% to 0.000061% in *Electrical Characteristics: OPA1632D* table ..... 8
- Changed IMD at single-ended input/output and  $R_L = 600\Omega$  from 0.0001% to 0.00007% in *Electrical Characteristics: OPA1632D* table ..... 8
- Changed IMD at single-ended input/output and  $R_L = 2\text{k}\Omega$  from 0.0007% to 0.000073% in *Electrical Characteristics: OPA1632D* table ..... 8
- Removed specified operating voltage specifications from *Electrical Characteristics: OPA1632D* table ..... 8
- Changed typical  $I_Q$  from 14mA to 13mA in *Electrical Characteristics: OPA1632D* table..... 8
- Changed title of Electrical Characteristics table to Electrical Characteristics: OPA1632DGN..... 10
- Changed test condition of power-down shutdown current from  $V_{\text{ENABLE}} = -15 \text{ V}$  to  $V_S = \pm 5 \text{ V}$ ,  $V_{\text{ENABLE}} = -5 \text{ V}$  for *Electrical Characteristics: OPA1632DGN* Package..... 10
- Added power-down shutdown current spec at  $V_{\text{ENABLE}} = -15 \text{ V}$  for *Electrical Characteristics: OPA1632DGN* table..... 10
- Changed max specified operating voltage from  $\pm 16 \text{ V}$  to  $\pm 15 \text{ V}$  on *Electrical Characteristics: OPA1632DGN* table to align with recommended operating conditions..... 10
- Removed typical specified operating voltage from *Electrical Characteristics: OPA1632DGN* table..... 10
- Changed typical sinking short-circuit current from 85 mA to -85 mA on *Electrical Characteristics: OPA1632DGN* table..... 10
- Added new Typical Characteristics section for D package..... 12
- Updated *Fully-Differential Amplifiers* section..... 16
- Updated *Feature Description* section..... 16
- Updated *Output Common-Mode Voltage* section..... 18
- Updated *Resistor Matching* section..... 18
- Updated *Application Curves* section..... 20
- Updated *Power Supply Recommendations* section..... 21
- Updated the *Power Dissipation and Thermal Considerations* section..... 22
- Updated *Layout Example* section..... 23
- Changed list of documentation in *Related Documentation* section..... 25

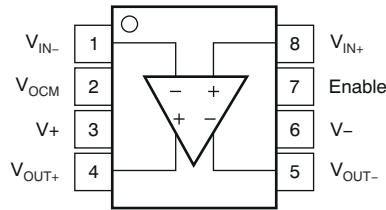
---

**Changes from Revision B (January 2010) to Revision C (September 2015)**

**Page**

- 添加了 ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。 ..... 1
-

## 5 Pin Configuration and Functions



**图 5-1. D or DGN<sup>(1)</sup> Package  
 8-Pin SOIC or MSOP-PowerPAD  
 Top View**

**表 5-1. Pin Functions**

PIN		TYPE <sup>(2)</sup>	DESCRIPTION
NAME	NO.		
Enable	7	I	Active high enable pin
V+	3	I/O	Positive supply voltage pin
V-	6	I/O	Negative supply voltage pin
V <sub>IN+</sub>	8	I	Positive input voltage pin
V <sub>IN-</sub>	1	I	Negative input voltage pin
V <sub>OCM</sub>	2	I	Output common-mode control voltage pin
V <sub>OUT+</sub>	4	O	Positive output voltage pin
V <sub>OUT-</sub>	5	O	Negative output voltage pin

- (1) Solder the exposed DGN package thermal pad to a heat-spreading power or ground plane. This pad is electrically isolated from the die, but must be connected to a power or ground plane and not floated.
- (2) I = input, O = output.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
$\pm V_S$	Supply Voltage		$\pm 16.5$	V
	Supply turn-on/off $dV/dT$ <sup>(3)</sup>		1.7	V/ $\mu$ s
$V_I$	Input Voltage		$\pm V_S$	V
$I_O$	Output Current		150	mA
$I_{IN}$	Continuous Input Current		10	mA
$V_{ID}$	Differential Input Voltage		$\pm 1.5$	V
$T_J$	Maximum Junction Temperature		150	$^{\circ}$ C
	Operating Free-Air Temperature Range	- 40	85	$^{\circ}$ C
$T_{STG}$	Storage Temperature Range	- 65	150	$^{\circ}$ C

- Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- The OPA1632 MSOP-8 package version incorporates a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally-dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature, which can permanently damage the device. See TI technical brief [SLMA002](#) for more information about using the PowerPAD thermally-enhanced package.
- Staying below this specification ensures that the edge-triggered ESD absorption devices across the supply pins remain off.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 1000$	V
		Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	$\pm 500$	V
		Machine Model	$\pm 200$	V

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage ( $V_+$ - $V_-$ )	Dual	$\pm 2.5$	$\pm 15$	V
	Single	5	30	
$T_A$	C-suffix	0	70	$^{\circ}$ C
	I-suffix	-40	85	

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	OPA1632		UNIT
	D (SOIC)	DGN (MSOP-PowerPAD)	
	8 PINS	8 PINS	
$R_{\theta JA}$	126.3	59.8	°C/W
$R_{\theta JC(top)}$	67.3	57.7	°C/W
$R_{\theta JB}$	69.8	38.7	°C/W
$\psi_{JT}$	19.5	2.7	°C/W
$\psi_{JB}$	69.0	38.4	°C/W
$R_{\theta JC(bot)}$	n/a	8.4	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).

## 6.5 Electrical Characteristics: OPA1632D

$V_S = \pm 15\text{ V}$ ;  $R_F = 390\ \Omega$ ,  $R_L = 800\ \Omega$ , and  $G = +1$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Offset Voltage</b>						
Input Offset Voltage				$\pm 0.5$	$\pm 3$	mV
	vs temperature, dc	$dV_{OS}/dT$		$\pm 2.5$		$\mu\text{V}/^\circ\text{C}$
	vs Power Supply, dc	PSRR		13	316	$\mu\text{V}/\text{V}$
<b>Input Bias Current</b>						
Input Bias Current	$I_B$			7.9	14	$\mu\text{A}$
Input Offset Current	$I_{OS}$			$\pm 100$	$\pm 500$	nA
<b>Noise</b>						
Input Voltage Noise		$f = 10\text{ kHz}$		1.25		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise		$f = 10\text{ kHz}$		1.7		$\text{pA}/\sqrt{\text{Hz}}$
<b>Input Voltage</b>						
Common-Mode Input Range			$(V^-) + 1.5$		$(V^+) - 1$	V
Common-Mode Rejection Ratio, dc			74	90		dB
<b>Input Impedance</b>						
Input Impedance		Measured into each input terminal, common-mode		$215 \parallel 1.4$		$\text{M}\Omega \parallel \text{pF}$
		Measured into each input terminal, differential		$10 \parallel 3.1$		$\text{k}\Omega \parallel \text{pF}$
<b>Open-Loop Gain</b>						
Open-Loop Gain, dc			66	78		dB
<b>Frequency Response</b>						
Small-Signal Bandwidth	$(V_O = 100\text{mV}_{PP}, \text{Peaking} < 0.5\text{ dB})$	$G = +1, R_F = 348\ \Omega$		180		MHz
		$G = +2, R_F = 602\ \Omega$		104		
		$G = +5, R_F = 1.5\text{ k}\Omega$		46		
		$G = +10, R_F = 3.01\text{ k}\Omega$		24		
Bandwidth for 0.1dB Flatness		$G = +1, V_O = 100\text{ mV}_{PP}$		40		MHz
Peaking at a Gain of 1		$V_O = 100\text{ mV}_{PP}$		0.5		dB
Large-Signal Bandwidth		$G = +2, V_O = 20\text{ V}_{PP}$		1.8		MHz
Slew Rate (25% to 75% )		$G = +1$		72		$\text{V}/\mu\text{s}$
Rise and Fall Time		$G = +1, V_O = 5\text{-V Step}$		69		ns
Settling Time to	0.1%	$G = +1, V_O = 2\text{-V Step}$		36		ns
	0.01%			49		ns
Total Harmonic Distortion + Noise	Differential Input/Output	$G = +1, f = 1\text{ kHz}, V_O = 3\text{ V}_{RMS}$	$R_L = 600\ \Omega$		0.00003%	
			$R_L = 2\text{ k}\Omega$		0.000028%	
	Single-Ended In/Differential Out		$R_L = 600\ \Omega$		0.000036%	
			$R_L = 2\text{ k}\Omega$		0.000031%	
Intermodulation Distortion	Differential Input/Output	$G = +1, \text{ SMPTE/DIN}, V_O = 2\text{ V}_{PP}$	$R_L = 600\ \Omega$		0.000061%	
			$R_L = 2\text{ k}\Omega$		0.000061%	
	Single-Ended In/Differential Out		$R_L = 600\ \Omega$		0.000073%	
			$R_L = 2\text{ k}\Omega$		0.00007%	
Headroom		$\text{THD} < 0.01\%, R_L = 2\text{ k}\Omega$		20		$V_{PP}$



## 6.5 Electrical Characteristics: OPA1632D (continued)

$V_S = \pm 15\text{ V}$ ;  $R_F = 390\ \Omega$ ,  $R_L = 800\ \Omega$ , and  $G = +1$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Output</b>						
Voltage Output Swing Low		$R_L = 2\text{ k}\Omega$	(V-) + 1.6			V
		$R_L = 1\text{ k}\Omega$			(V-) + 3.5	V
Voltage Output Swing High		$R_L = 2\text{ k}\Omega$	(V+) - 1.6			V
		$R_L = 1\text{ k}\Omega$	(V+) - 3.5			V
Short-Circuit Current	$I_{sc}$	Sourcing	50	85		mA
		Sinking	-60	-85		
Closed-Loop Output Impedance		$G = +1$ , $f = 100\text{ kHz}$		0.22		$\Omega$
<b>Power-Down<sup>(1)</sup></b>						
Enable Voltage Threshold				(V-) + 1.45		V
Disable Voltage Threshold				(V-) + 1.4		V
Shutdown Current		$V_S = \pm 5\text{ V}$ , $V_{ENABLE} = -5\text{ V}$		0.85		mA
		$V_{ENABLE} = -15\text{ V}$		1.7		mA
Turn-On Delay		Time for $I_Q$ to Reach 50%		2		$\mu\text{ s}$
Turn-Off Delay					2	
<b>Power Supply</b>						
Quiescent Current	$I_Q$			13	17.1	mA

(1) Amplifier has internal 250-k $\Omega$  pull-up resistor to V+ pin. This enables the amplifier with no connection to shutdown pin.

## 6.6 Electrical Characteristics: OPA1632DGN

$V_S = \pm 15\text{ V}$ ;  $R_F = 390\ \Omega$ ,  $R_L = 800\ \Omega$ , and  $G = +1$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Offset Voltage</b>						
Input Offset Voltage				$\pm 0.5$	$\pm 3$	mV
	vs Power Supply, dc	$dV_{OS}/dT$		$\pm 5$		$\mu\text{V}/^\circ\text{C}$
	vs Power Supply, dc	PSRR	316	13		$\mu\text{V}/\text{V}$
<b>Input Bias Current</b>						
Input Bias Current	$I_B$			2	6	$\mu\text{A}$
Input Offset Current	$I_{OS}$			$\pm 100$	$\pm 500$	nA
<b>Noise</b>						
Input Voltage Noise		$f = 10\text{ kHz}$		1.3		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise		$f = 10\text{ kHz}$		0.4		$\text{pA}/\sqrt{\text{Hz}}$
<b>Input Voltage</b>						
Common-Mode Input Range			$(V_-) + 1.5$		$(V_+) - 1$	V
Common-Mode Rejection Ratio, dc			74	90		dB
<b>Input Impedance</b>						
Input Impedance (each input pin)				$34 \parallel 4$		$\text{M}\Omega \parallel \text{pF}$
<b>Open-Loop Gain</b>						
Open-Loop Gain, dc			66	78		dB
<b>Frequency Response</b>						
Small-Signal Bandwidth	$(V_O = 100\text{mV}_{PP}, \text{Peaking} < 0.5\text{ dB})$	$G = +1, R_F = 348\ \Omega$		180		MHz
		$G = +2, R_F = 602\ \Omega$		90		MHz
		$G = +5, R_F = 1.5\text{ k}\Omega$		36		MHz
		$G = +10, R_F = 3.01\text{ k}\Omega$		18		MHz
Bandwidth for 0.1dB Flatness		$G = +1, V_O = 100\text{ mV}_{PP}$		40		MHz
Peaking at a Gain of 1		$V_O = 100\text{ mV}_{PP}$		0.5		dB
Large-Signal Bandwidth		$G = +2, V_O = 20\text{ V}_{PP}$		800		kHz
Slew Rate (25% to 75% )		$G = +1$		50		$\text{V}/\mu\text{s}$
Rise and Fall Time		$G = +1, V_O = 5\text{-V Step}$		100		ns
Settling Time to	0.1%	$G = +1, V_O = 2\text{-V Step}$		75		ns
	0.01%	$G = +1, V_O = 2\text{-V Step}$		200		ns
Total Harmonic Distortion + Noise	Differential Input/Output	$G = +1, f = 1\text{ kHz}, V_O = 3\text{ V}_{RMS}$	$R_L = 600\ \Omega$		0.0003%	
	Differential Input/Output		$R_L = 2\text{ k}\Omega$		0.000022%	
	Single-Ended In/Differential Out		$R_L = 600\ \Omega$		0.000059%	
	Single-Ended In/Differential Out		$R_L = 2\text{ k}\Omega$		0.000043%	
Intermodulation Distortion	Differential Input/Output	$G = +1, \text{ SMPTE/DIN}, V_O = 2\text{ V}_{PP}$	$R_L = 600\ \Omega$		0.00008%	
	Differential Input/Output		$R_L = 2\text{ k}\Omega$		0.00005%	
	Single-Ended In/Differential Out		$R_L = 600\ \Omega$		0.0001%	
	Single-Ended In/Differential Out		$R_L = 2\text{ k}\Omega$		0.0007%	
Headroom		$\text{THD} < 0.01\%, R_L = 2\text{ k}\Omega$		20.0		$V_{PP}$
<b>Output</b>						
Voltage Output Swing		$R_L = 2\text{ k}\Omega$	$(V_+) - 1.9$		$(V_-) + 1.9$	V
		$R_L = 800\ \Omega$	$(V_+) - 4.5$		$(V_-) + 4.5$	V
Short-Circuit Current $I_{SC}$		Sourcing	+50	85		mA
		Sinking	-60	-85		
Closed-Loop Output Impedance		$G = +1, f = 100\text{ kHz}$		0.3		$\Omega$

## 6.6 Electrical Characteristics: OPA1632DGN (continued)

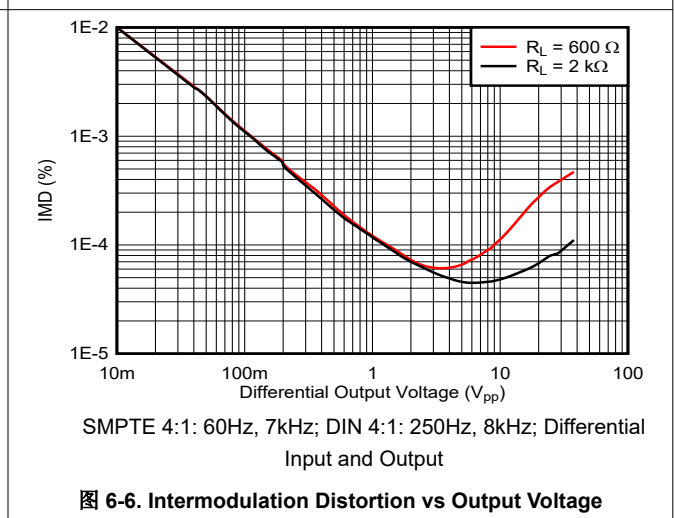
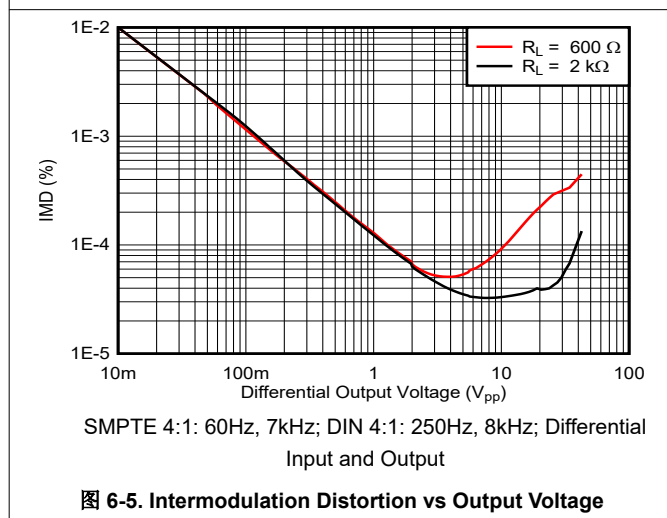
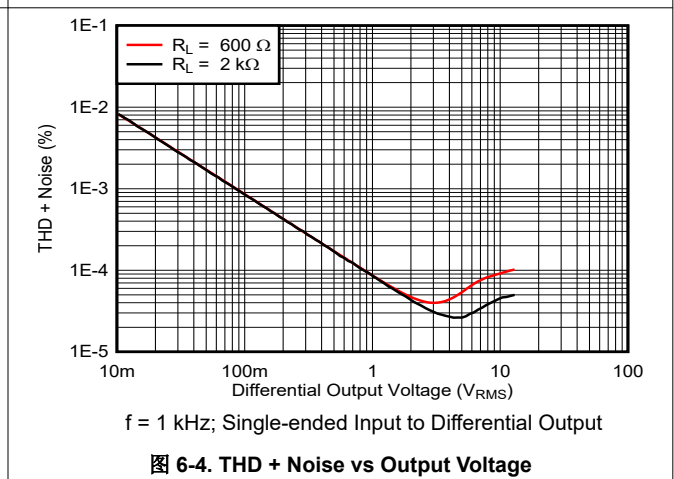
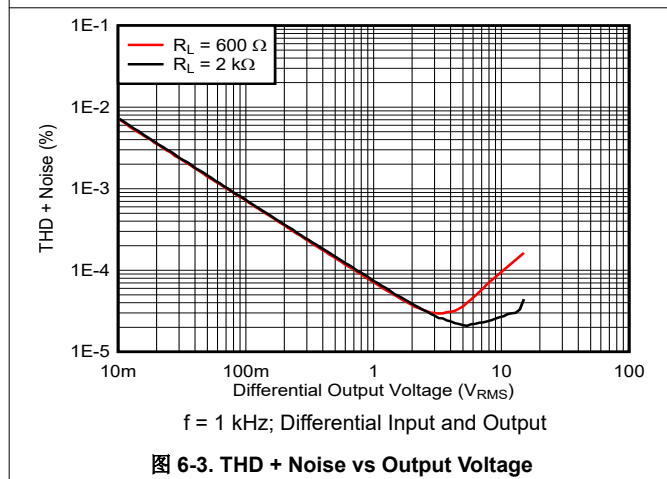
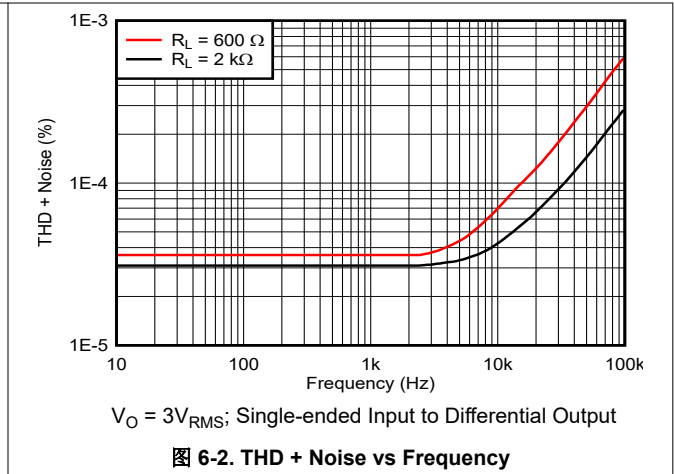
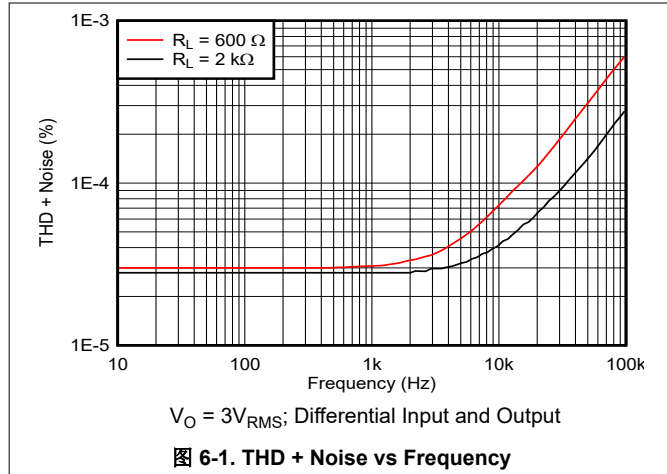
$V_S = \pm 15\text{ V}$ ;  $R_F = 390\ \Omega$ ,  $R_L = 800\ \Omega$ , and  $G = +1$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Power-Down<sup>(1)</sup></b>					
Enable Voltage Threshold			(V-) + 2		V
Disable Voltage Threshold			(V-) + 0.8		V
Shutdown Current	$V_{ENABLE} = -15\text{ V}$		1.7		mA
Shutdown Current	$V_S = \pm 5\text{ V}$ , $V_{ENABLE} = -5\text{ V}$		0.85		mA
Turn-On Delay	Time for $I_Q$ to Reach 50%		2		$\mu\text{ s}$
Turn-Off Delay	Time for $I_Q$ to Reach 50%		2		$\mu\text{ s}$
<b>Power Supply</b>					
Specified Operating Voltage				$\pm 15$	V
Operating Voltage		$\pm 2.5$			V
Quiescent Current $I_Q$	Per Channel		14	17.1	mA
<b>Temperature Range</b>					
Specified Range		- 40		+85	$^{\circ}\text{C}$
Operating Range		- 40		+125	$^{\circ}\text{C}$
Storage Range		- 65		+150	$^{\circ}\text{C}$

(1) Amplifier has internal 50-k $\Omega$  pull-up resistor to V+ pin. This enables the amplifier with no connection to shutdown pin.

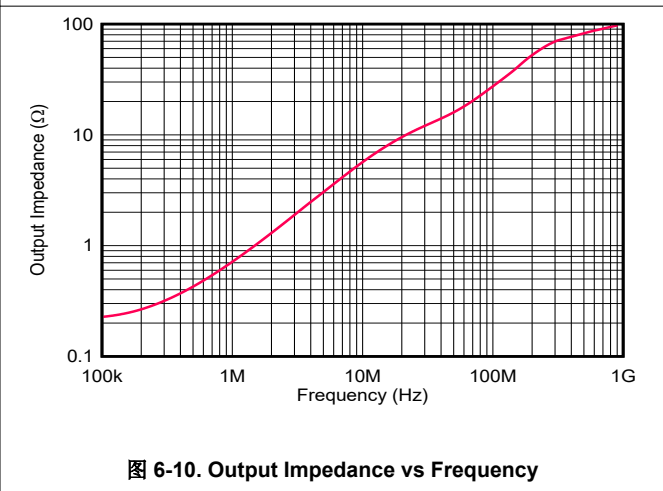
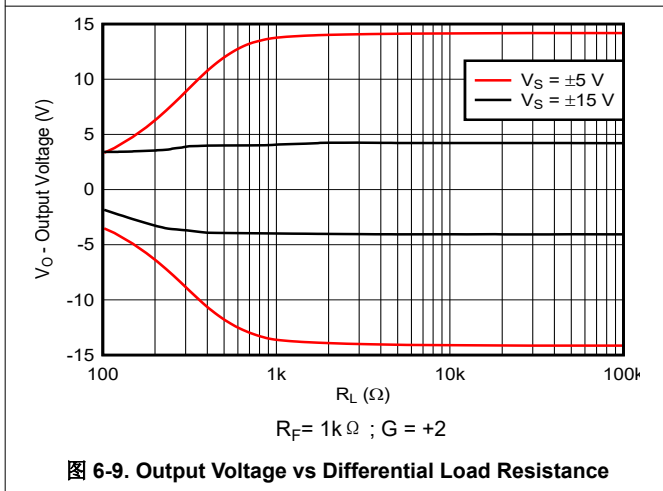
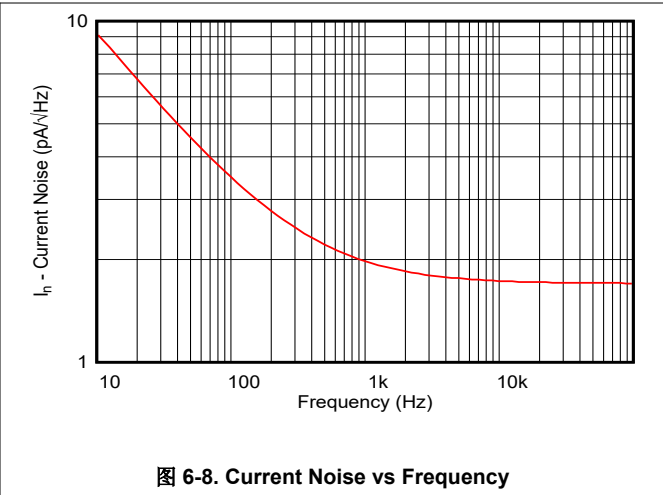
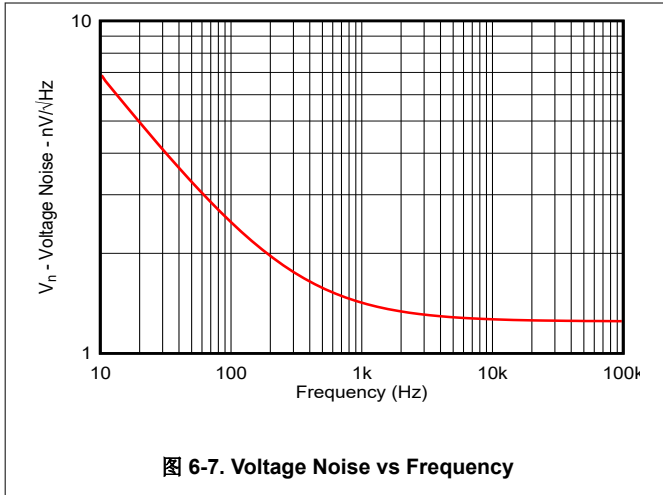
## 6.7 Typical Characteristics: OPA1632D

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_F = 348\ \Omega$ ,  $G = +1$  and  $R_L = 2\text{ k}\Omega$  (unless otherwise noted)



## 6.7 Typical Characteristics: OPA1632D (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_F = 348\ \Omega$ ,  $G = +1$  and  $R_L = 2\text{ k}\Omega$  (unless otherwise noted)



### 6.8 Typical Characteristics: OPA1632DGN

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$  (unless otherwise noted)

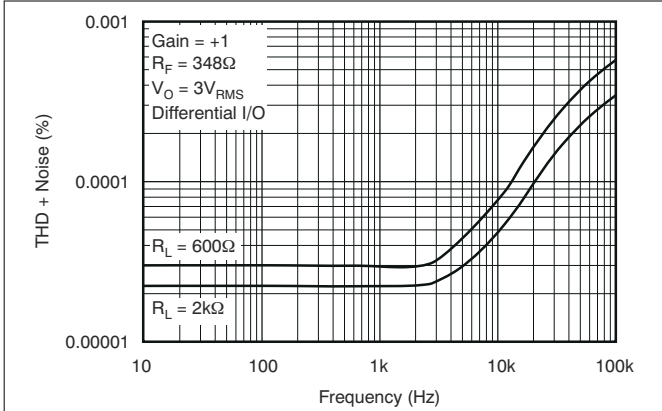


图 6-11. THD + Noise vs Frequency

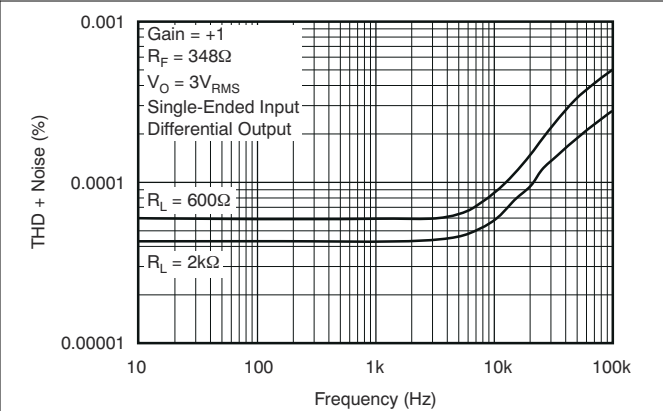


图 6-12. THD + Noise vs Frequency

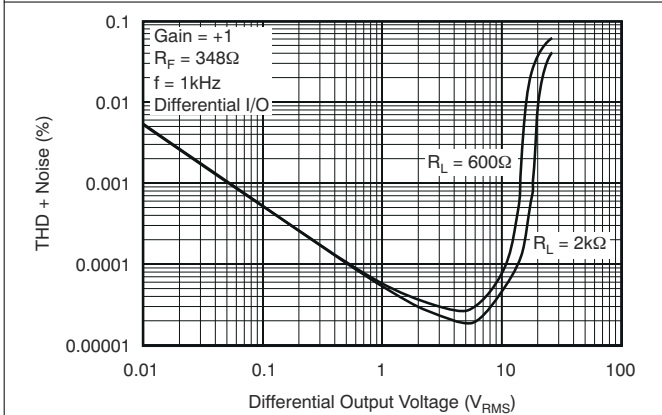


图 6-13. THD + Noise vs Output Voltage

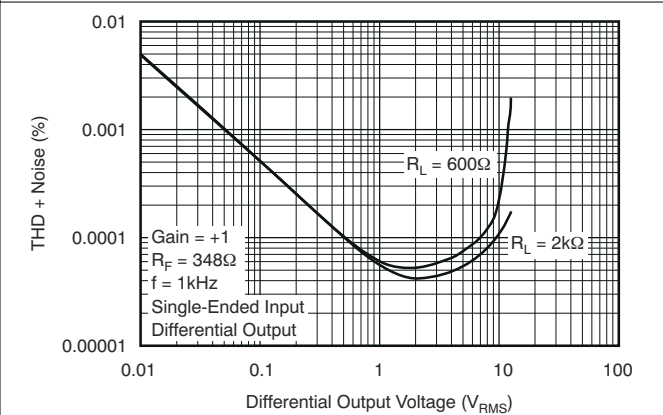


图 6-14. THD + Noise vs Output Voltage

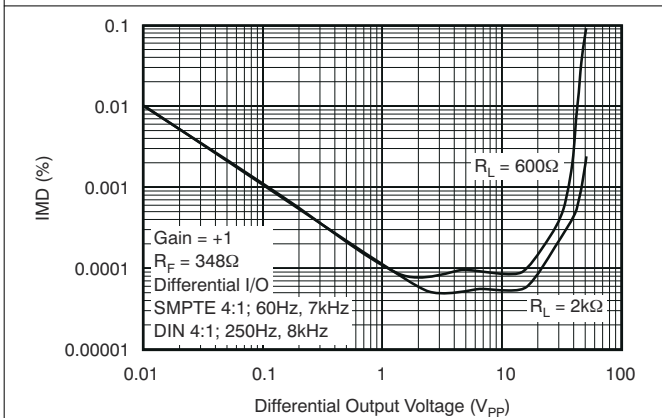


图 6-15. Intermodulation Distortion vs Output Voltage

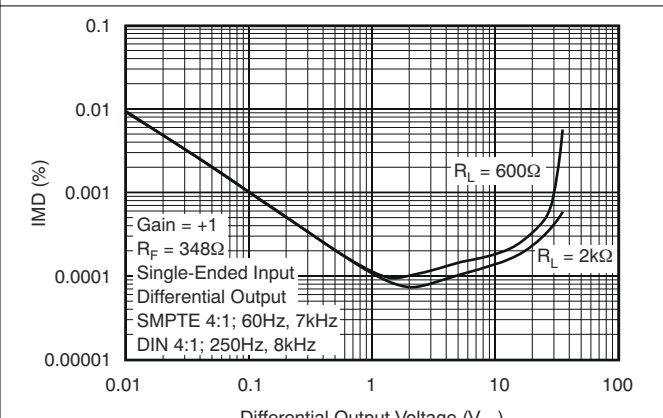
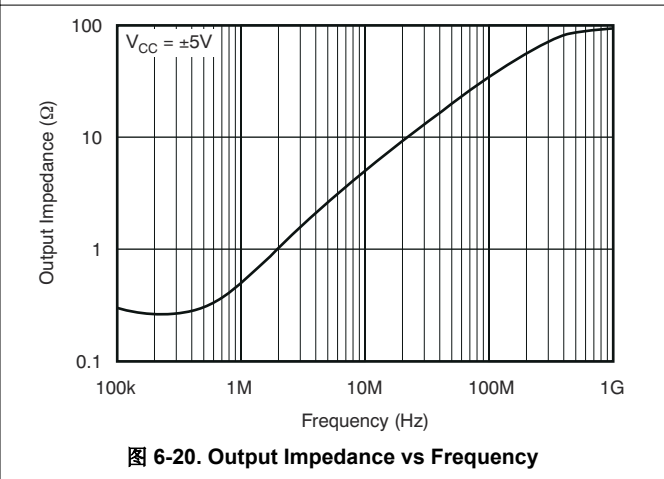
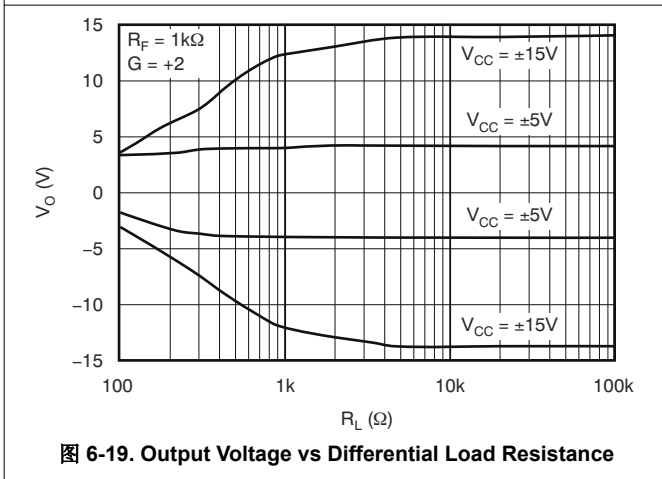
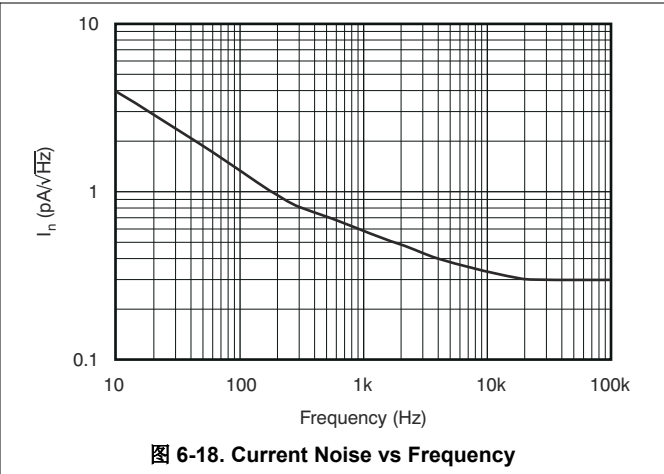
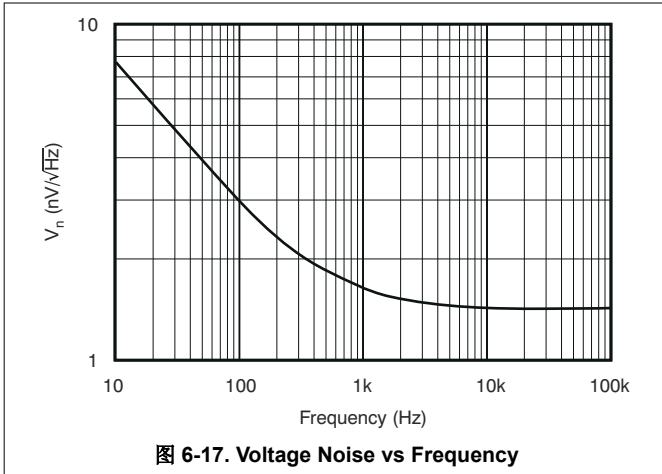


图 6-16. Intermodulation Distortion vs Output Voltage

### 6.8 Typical Characteristics: OPA1632DGN (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$  (unless otherwise noted)



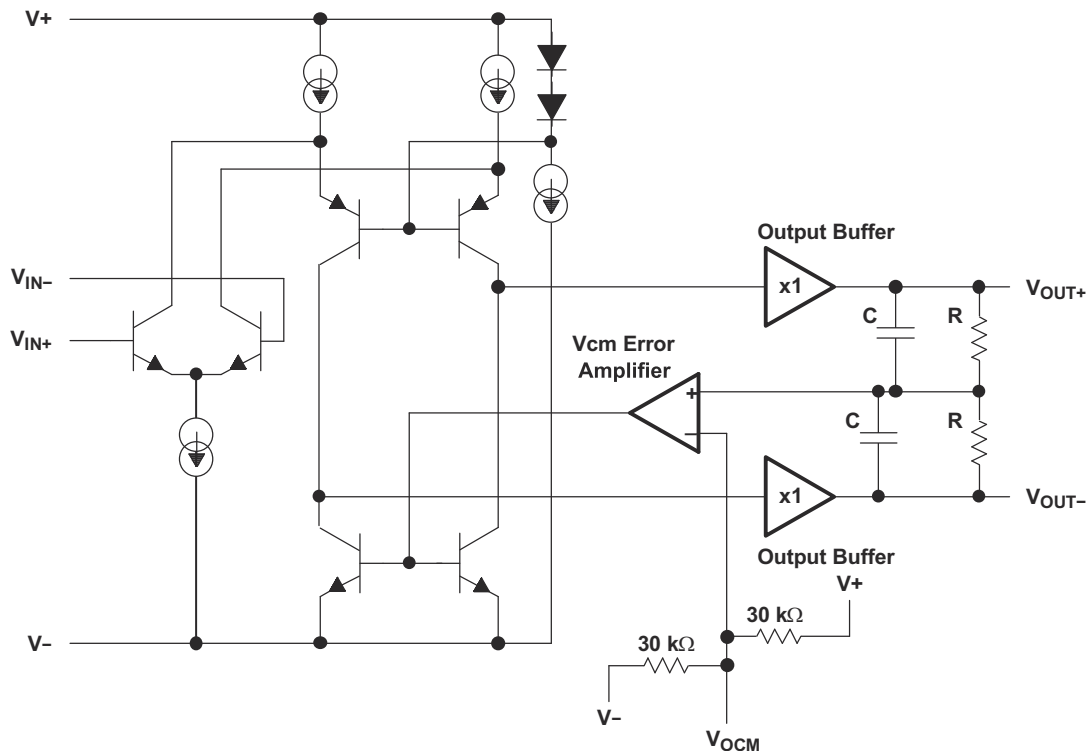
## 7 Detailed Description

### 7.1 Overview

#### 7.1.1 Fully-Differential Amplifiers

The OPA1632 is a fully differential amplifier (FDA). Differential signal processing offers a number of performance advantages in high-speed analog signal processing systems, including immunity to external common-mode noise, suppression of even-order non-linearities, and increased dynamic range. FDAs not only serve as the primary means of providing gain to a differential signal chain, but also provide a monolithic solution for converting single-ended signals into differential signals allowing for easy, high-performance processing. For more information on the basic theory of operation for FDAs, refer to the [Fully Differential Amplifiers application note](#).

### 7.2 Functional Block Diagram



### 7.3 Feature Description

Figure 7-1 and Figure 7-2 depict the differences between the operation of the OPA1632 in two different modes. FDAs can work with differential input or can be implemented as single in/differential out.

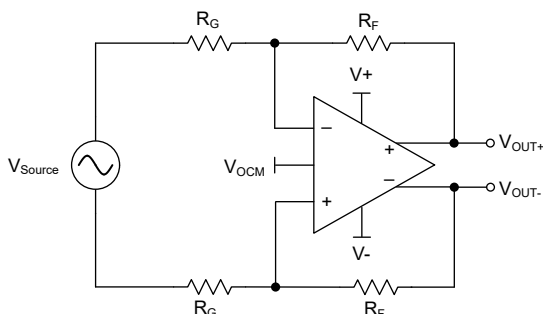


图 7-1. Amplifying Differential Input Signals

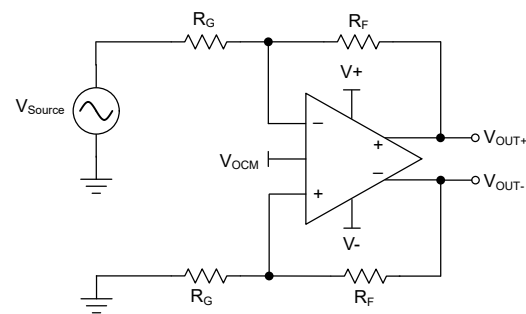


图 7-2. Amplifying Single-ended Input Signals



## 7.4 Device Functional Modes

### 7.4.1 Shutdown Function

The shutdown (enable) function of the OPA1632 is referenced to the negative supply of the operational amplifier. A valid logic low ( $< 0.8$  V above negative supply) applied to the enable pin (pin 7) disables the amplifier output. Voltages applied to pin 7 that are greater than 2 V above the negative supply place the amplifier output in an active state, and the device is enabled. If pin 7 is left disconnected, an internal pull-up resistor enables the device. Turn-on and turn-off times are approximately 2  $\mu$ s each.

Quiescent current is reduced to approximately 0.85 mA when the amplifier is disabled. When disabled, the output stage is *not* in a high-impedance state. Thus, the shutdown function cannot be used to create a multiplexed switching function in series with multiple amplifiers.

## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

#### 8.1.1 Output Common-Mode Voltage

The output common-mode voltage pin sets the dc output voltage of the OPA1632. A voltage applied to the  $V_{OCM}$  pin from a low-impedance source can be used to directly set the output common-mode voltage. If the  $V_{OCM}$  pin is left floating it defaults to the mid-rail voltage, defined as:

$$\frac{(V_+) + (V_-)}{2} \quad (1)$$

To minimize common-mode noise, connect a 0.1- $\mu$ F bypass capacitor to the  $V_{OCM}$  pin. Output common-mode voltage causes additional current to flow in the feedback resistor network. Since this current is supplied by the output stage of the amplifier, this creates additional power dissipation. For commonly-used feedback resistance values, this current is easily supplied by the amplifier. The additional internal power dissipation created by this current may be significant in some applications and may dictate use of the MSOP PowerPAD package to effectively control self-heating.

##### 8.1.1.1 Resistor Matching

Resistor matching is important in FDAs to maintain good output balance. An ideal differential output signal implies the two outputs of the FDA should be exactly equal in amplitude and shifted 180° in phase. Any imbalance in amplitude or phase between the two output signals results in an undesirable common-mode signal at the output. The output balance error is a measure of how well the outputs are balanced and is defined as the ratio of the output common-mode voltage to the output differential signal.

$$\text{Output Balance Error} = \frac{\left(\frac{V_{OUT+} - V_{OUT-}}{2}\right)}{V_{OUT+} - V_{OUT-}} \quad (2)$$

At low frequencies, resistor mismatch is the primary contributor to output balance errors. Additionally CMRR, PSRR, and HD2 performance diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to optimize performance. See [表 8-1](#) for recommended resistor values to use for a particular gain.

**表 8-1. Recommended Resistor Values**

Gain (V/V)	$R_G$ ( $\Omega$ )	$R_F$ ( $\Omega$ )
1	390	390
2	374	750
5	402	2010
10	402	4020

## 8.2 Typical Application

图 8-1 shows the OPA1632 used as a differential-output driver for the PCM1804 high-performance audio ADC.

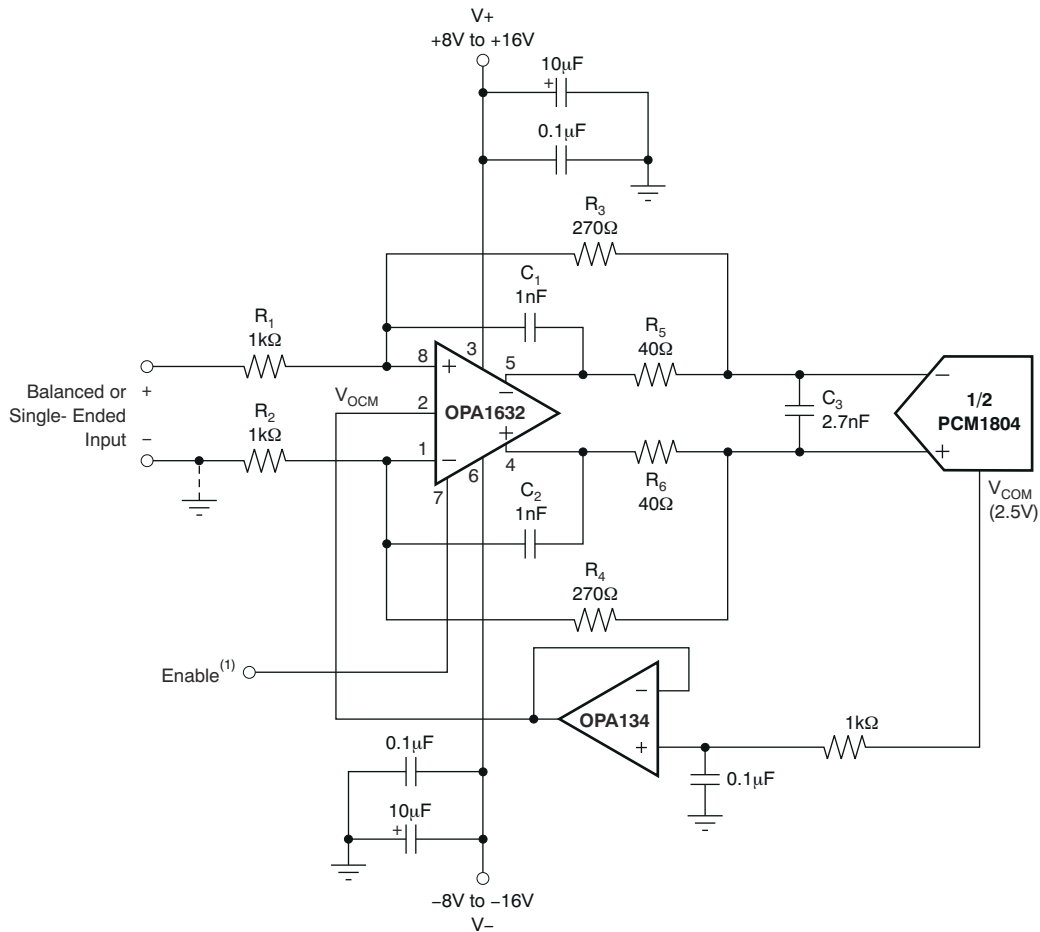


图 8-1. ADC Driver for Professional Audio

### 8.2.1 Design Requirements

表 8-2 shows example design parameters and values for the typical application design example in 图 7-1.

表 8-2. Design Parameters

DESIGN PARAMETERS	VALUE
Supply voltage	±2.5 V to ±15 V
Amplifier topology	Voltage feedback
Output control	DC coupled with output common mode control capability
Filter requirement	500 kHz, Multiple feedback low pass filter

## 8.2.2 Detailed Design Procedure

Supply voltages of  $\pm 15$  V are commonly used for the OPA1632. The relatively low input voltage swing required by the ADC allows use of lower power-supply voltage, if desired. Power supplies as low as  $\pm 8$  V can be used in this application with excellent performance. This reduces power dissipation and heat rise. Power supplies should be bypassed with 10- $\mu$ F tantalum capacitors in parallel with 0.1- $\mu$ F ceramic capacitors to avoid possible oscillations and instability.

The  $V_{COM}$  reference voltage output on the PCM1804 ADC provides the proper input common-mode reference voltage (2.5 V). This  $V_{COM}$  voltage is buffered with op amp  $A_2$  and drives the output common-mode voltage pin of the OPA1632. This biases the average output voltage of the OPA1632 to 2.5 V.

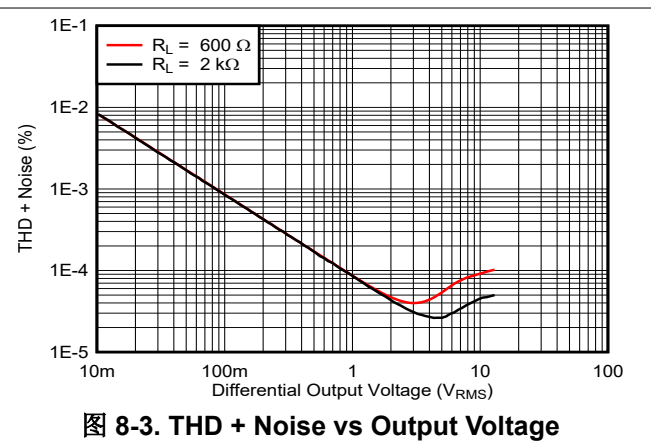
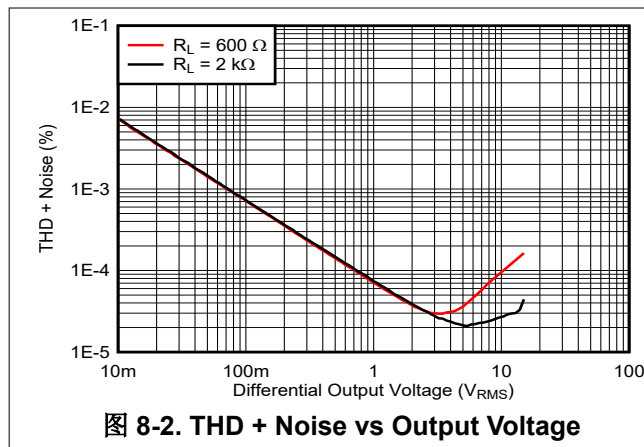
The signal gain of the circuit is generally set to approximately 0.25 to be compatible with commonly-used audio line levels. Gain can be adjusted, if necessary, by changing the values of  $R_1$  and  $R_2$ . The feedback resistor values ( $R_3$  and  $R_4$ ) should be kept relatively low, as indicated, for best noise performance.

$R_5$ ,  $R_6$ , and  $C_3$  provide an input filter and charge glitch reservoir for the ADC. The values shown are generally satisfactory. Some adjustment of the values may help optimize performance with different ADCs.

It is important to maintain accurate resistor matching on  $R_1/R_2$  and  $R_3/R_4$  to achieve good differential signal balance. Use 1% resistors for highest performance. When connected for single-ended inputs (inverting input grounded, as shown in [图 8-1](#)), the source impedance must be low. Differential input sources must have well-balanced or low source impedance.

Capacitors  $C_1$ ,  $C_2$ , and  $C_3$  should be chosen carefully for good distortion performance. Polystyrene, polypropylene, NPO ceramic, and mica types are generally excellent. Polyester and high-K ceramic types such as Z5U can create distortion.

## 8.2.3 Application Curves



## 9 Power Supply Recommendations

The OPA1632 device was designed to be operated on power supplies ranging from  $\pm 2.5$  V to  $\pm 15$  V. Single power supplies ranging from 5 V to 30 V can also be used. TI recommends using a power-supply accuracy of 5%, or better. When operated on a board with high-speed digital signals, it is important to provide isolation between digital signal noise and the analog input pins. The OPA1632 is connected to power supplies through pin 3 ( $V_+$ ) and pin 6 ( $V_-$ ). Each supply pin should be decoupled to GND as close to the device as possible with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF. When vias are used to connect the bypass capacitors to a ground plane the vias should be configured for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems, two capacitors per supply pin are advised.

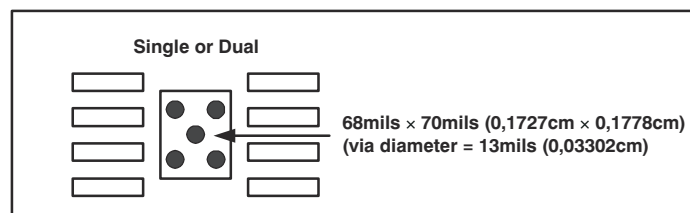
To avoid undesirable signal transients, the OPA1632 device should not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

## 10 Layout

### 10.1 Layout Guidelines

1. The PowerPAD is electrically isolated from the silicon and all leads. Connecting the PowerPAD to any potential voltage between the power-supply voltages is acceptable, but it is recommended to tie to ground because it is generally the largest conductive plane.
2. Prepare the PCB with a top-side etch pattern, as shown in [图 10-1](#). There should be etch for the leads as well as etch for the thermal pad.
3. Place five holes in the area of the thermal pad. These holes should be 13 mils (0,03302 cm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
4. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA1632 IC, and may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
5. Connect all holes to the internal ground plane.
6. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA1632 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
7. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

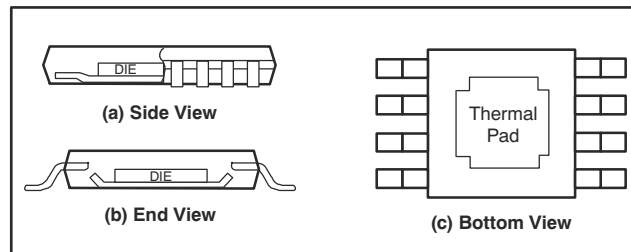
With these preparatory steps in place, the IC is simply placed in position and runs through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.



**图 10-1. PowerPAD PCB Etch and Via Pattern**

### 10.1.1 PowerPAD Design Considerations

The OPA1632 is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted (see [图 10-2\(a\)](#) and [图 10-2\(b\)](#)). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see [图 10-2\(c\)](#)). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.



**图 10-2. Views of the Thermally-Enhanced Package**

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. It provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

### 10.1.2 Power Dissipation and Thermal Considerations

The OPA1632 does not have thermal shutdown protection. Take care to assure that the maximum junction temperature is not exceeded. Excessive junction temperature can degrade performance or cause permanent damage. For best performance and reliability, assure that the junction temperature does not exceed 125°C.

The thermal characteristics of the device are dictated by the package and the circuit board. Maximum power dissipation for a given package can be calculated using the following formula:

$$P_{DMax} = \frac{T_{Max} - T_A}{\theta_{JA}}$$

where:

- $P_{DMax}$  is the maximum power dissipation in the amplifier (W)
- $T_{Max}$  is the absolute maximum junction temperature (°C)
- $T_A$  is the ambient temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- $\theta_{JC}$  is the thermal coefficient from the silicon junctions to the case (°C/W)
- $\theta_{CA}$  is the thermal coefficient from the case to ambient air (°C/W)

For systems where heat dissipation is more critical, the OPA1632 is offered in an MSOP-8 with PowerPAD. The thermal coefficient for the MSOP PowerPAD (DGN) package is substantially improved over the traditional SO package. Maximum power dissipation levels are depicted in [图 10-3](#) for the two packages. The data for the DGN package assume a board layout that follows the PowerPAD layout guidelines.

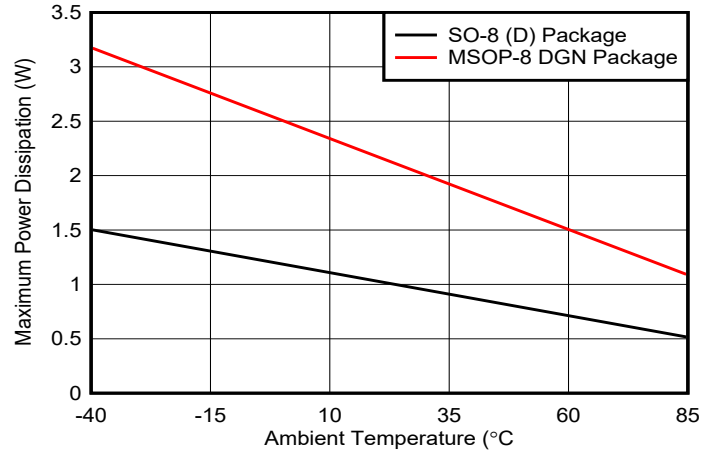


图 10-3. Maximum Power Dissipation vs Ambient Temperature

## 10.2 Layout Example

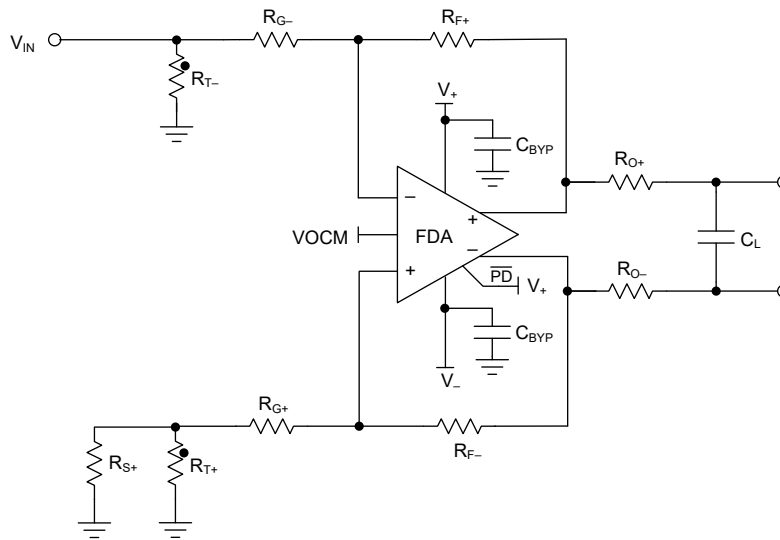


图 10-4. Representative Schematic for Example Layout

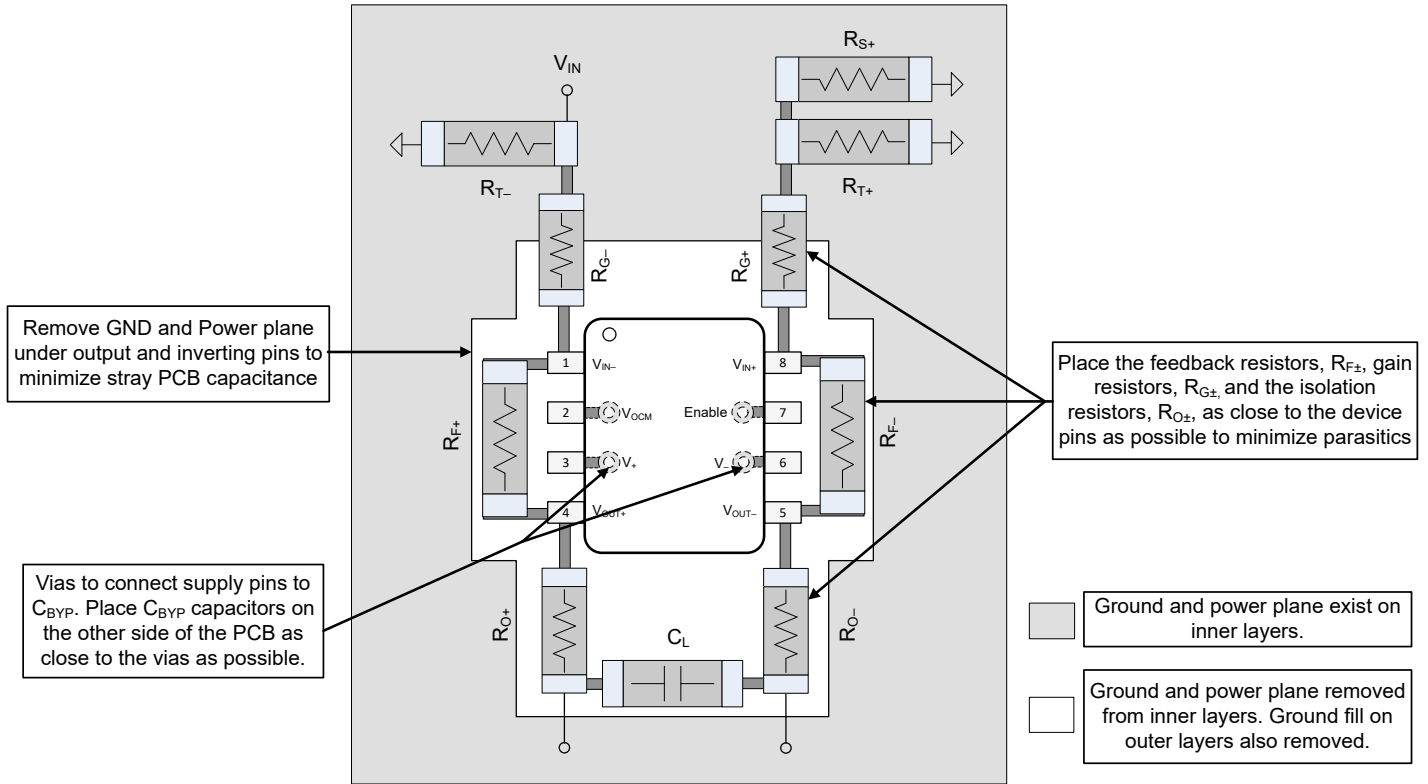


图 10-5. Example Layout



## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Fully Differential Amplifiers application note](#)
- Texas Instruments, [TI Precision Labs - Fully Differential Amplifiers video series](#)
- Texas Instruments, [Maximizing Signal Chain Distortion Performance Using High Speed Amplifiers application note](#)
- Texas Instruments, [Analog Audio Amplifier Front-end Reference Design with Improved Noise and Distortion](#)
- Texas Instruments, [Public Announcement Audio Reference Design utilizing best in class Boost Controller](#)
- Texas Instruments, [Motherboard/controller for the AMC1210 reference design](#)
- Texas Instruments, [TPA6120A2 Stereo, 9.0 to 33.0-V, analog input headphone amplifier with 128 dB dynamic range](#)
- Texas Instruments, [OPA2863 Dual, low-power, 110-MHz, 12-V, RRIO voltage feedback amplifier](#)
- Texas Instruments, [OPA2834 Ultra-low power, 50MHz rail-to-rail out, negative rail in, voltage-feedback op amp](#)

#### 11.2 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

#### 11.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 11.4 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

#### 11.5 Trademarks

PowerPAD™ is a trademark of Texas Instruments.

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

#### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.7 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## 11.8 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1632D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	<a href="#">Samples</a>
OPA1632DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	<a href="#">Samples</a>
OPA1632DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1632	<a href="#">Samples</a>
OPA1632DGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1632	<a href="#">Samples</a>
OPA1632DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1632	<a href="#">Samples</a>
OPA1632DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

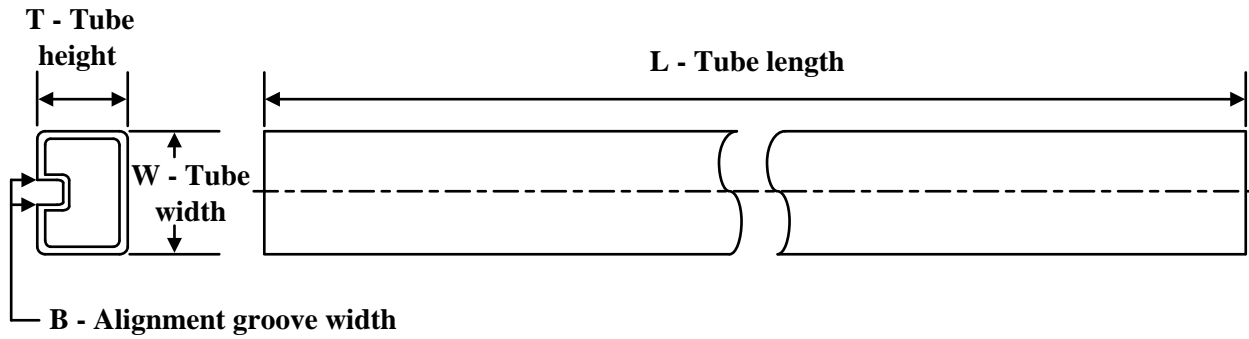

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1632DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1632DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1632DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
OPA1632DR	SOIC	D	8	2500	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA1632D	D	SOIC	8	75	505.46	6.76	3810	4
OPA1632DG4	D	SOIC	8	75	505.46	6.76	3810	4

## GENERIC PACKAGE VIEW

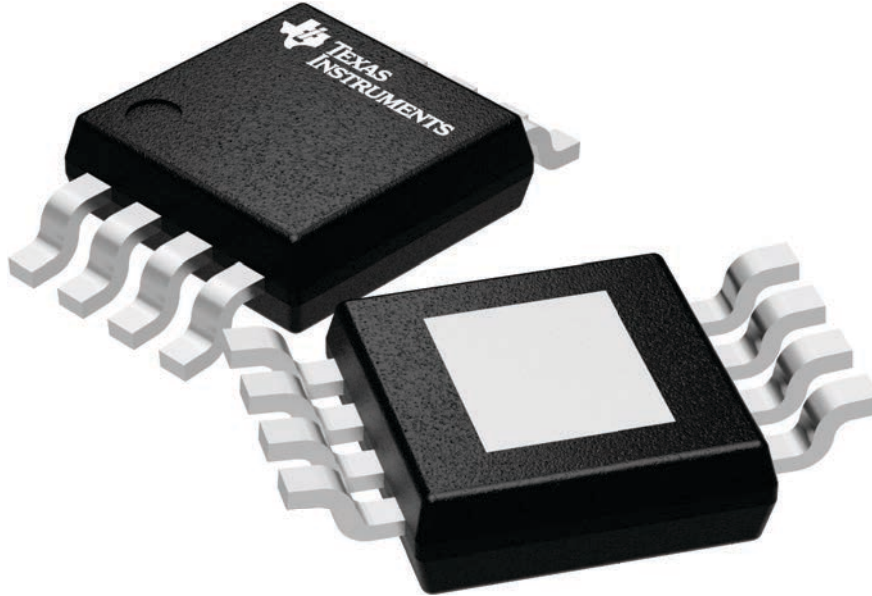
**DGN 8**

**PowerPAD VSSOP - 1.1 mm max height**

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225482/A





4225481/A 11/2019

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

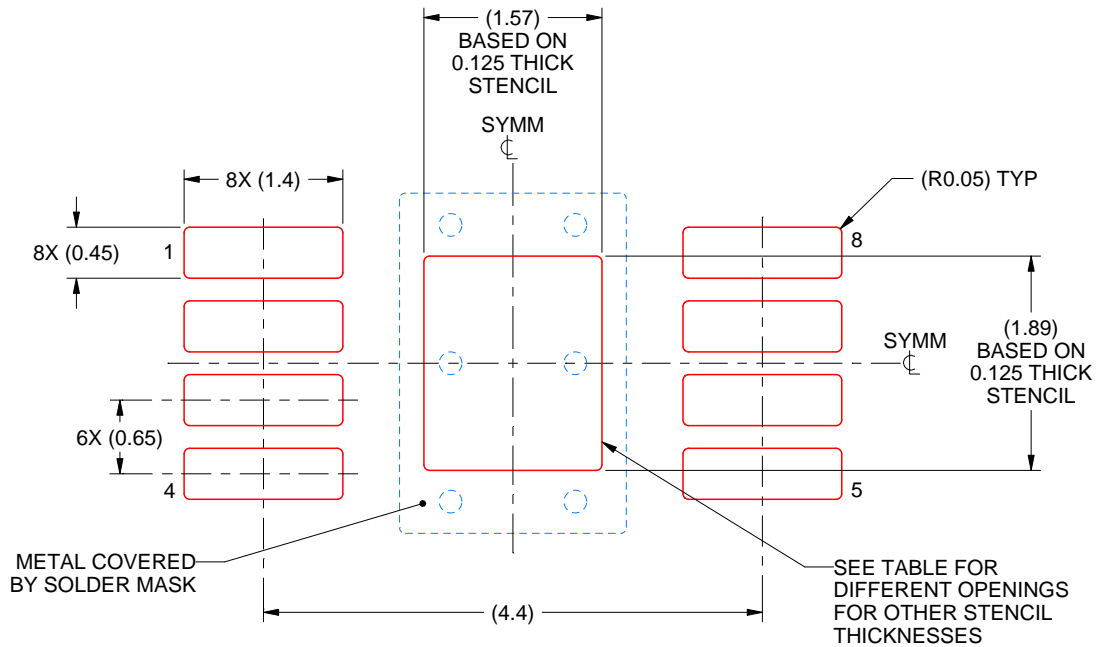


# EXAMPLE STENCIL DESIGN

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
EXPOSED PAD 9:  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

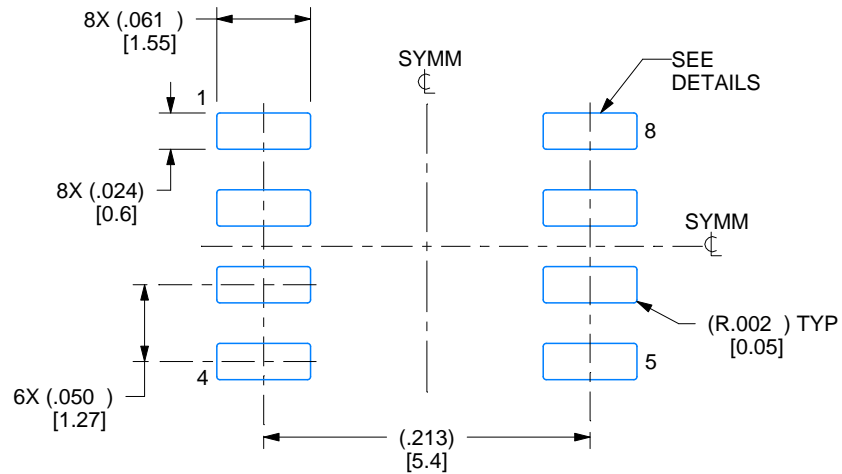
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [Audio Amplifiers](#) category:*

*Click to view products by [Texas Instruments](#) manufacturer:*

Other Similar products are found below :

[LV47002P-E](#) [NCP2890AFCT2G](#) [NTE1192](#) [LC706200CM](#) [IS31AP4915A-QFLS2-TR](#) [TDA1591T](#) [TS2012EIJT](#) [NCP2809BMUTXG](#)  
[NJW1157BFC2](#) [IS31AP4996-GRLS2-TR](#) [NCP2823BFCT1G](#) [BD88420GUL-E2](#) [LA4450L-E](#) [IS31AP2036A-CLS2-TR](#) [NTE1110](#) [NTE7100](#)  
[NTE7114](#) [NTE7163](#) [NTE7168](#) [NTE7177](#) [NTE7178](#) [NTE7186](#) [NTE7198](#) [NTE7202](#) [NTE7217](#) [BD88400GUL-E2](#) [BD88200GUL-E2](#)  
[SABRE9601K](#) [THAT1646W16-U](#) [PAM8965ZLA40-13](#) [TSDP10XX1NLGXZBX](#) [TSDP11XX1NKGIZBX](#) [TSDP11XX1NLGXZBX](#)  
[TSDP10XX1NKGIZBX](#) [NJM4580CV-TE1](#) [NJU7084R-TE1](#) [OPA1655DR](#) [LV4910T-MPB-E](#) [NCP2890AFCT2](#) [NCV2211DR2G](#)  
[SCY99091FCT2G](#) [TAS5720MRSMR](#) [AW87389FCR](#) [AW8737AFCR](#) [TDA2005R](#) [TDA2030](#) [TDA7265L-J11-A-T](#) [CD2050CZ](#)  
[AW88261FCR](#) [TDA7377-JSM](#)